CY23S02

Spread Aware™, Frequency Multiplier, and Zero Delay Buffer

Features

- Spread Aware™ – designed to work with SSFTG reference signals
- 90 ps typical jitter OUT2
- 200 ps typical jitter OUT1
- 65 ps typical output-to-output skew
- 90 ps typical propagation delay
- Voltage range: 3.3 V ± 5%, or 5 V ± 10%
- Output frequency range: 20 MHz - 133 MHz
- Two outputs
- Configuration options allow various multiplication of the reference frequency, refer to Configuration Options to determine the specific option which meets your multiplication needs
- Available in 8-pin SOIC package

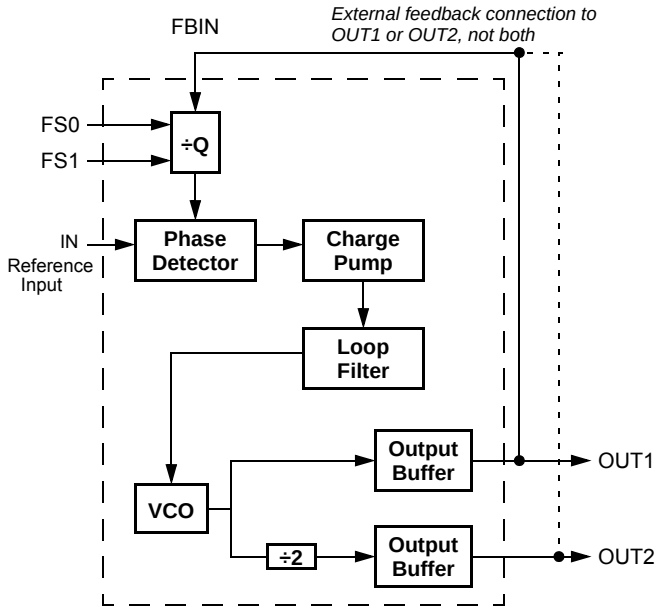
Configuration Options

FBIN	FS0	FS1	OUT1	OUT2
OUT1	0	0	2 X REF	REF
OUT1	1	0	4 X REF	2 X REF
OUT1	0	1	REF	REF/2
OUT1	1	1	8 X REF	4 X REF
OUT2	0	0	4 X REF	2 X REF
OUT2	1	0	8 X REF	4 X REF
OUT2	0	1	2 X REF	REF
OUT2	1	1	16 X REF	8 X REF

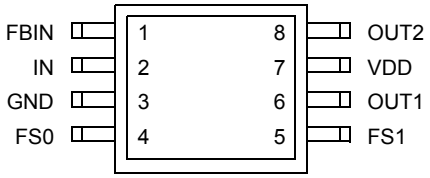
Functional Description

For a complete list of related documentation, click here.

Block Diagram



Pin Configuration



Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
IN	2	I	**Reference Input:** The output signals will be synchronized to this signal.
FBIN	1	I	**Feedback Input:** This input must be fed by one of the outputs (OUT1 or OUT2) to ensure proper functionality. If the trace between FBIN and the output pin being used for feedback is equal in length to the traces between the outputs and the signal destinations, then the signals received at the destinations will be synchronized to the REF signal input (IN).
OUT1	6	O	**Output 1:** The frequency of the signal provided by this pin is determined by the feedback signal connected to FBIN, and the FS0:1 inputs (see Table).
OUT2	8	O	**Output 2:** The frequency of the signal provided by this pin is one-half of the frequency of OUT1. See Table .
V_{DD}	7	P	**Power Connections:** Connect to 3.3 V or 5 V. This pin should be bypassed with a 0.1-µF decoupling capacitor. Use ferrite beads to help reduce noise for optimal jitter performance.
GND	3	P	**Ground Connection:** Connect all grounds to the common system ground plane.
FS0:1	4, 5	I	**Function Select Inputs:** Tie to VDD (HIGH, 1) or GND (LOW, 0) as desired per Table .

Overview

The CY23S02 is a two-output zero delay buffer and frequency multiplier. It provides an external feedback path allowing maximum flexibility when implementing the Zero Delay feature. This is explained further in the sections of this data sheet titled “How to Implement Zero Delay,” and “Inserting Other Devices in Feedback Path.”

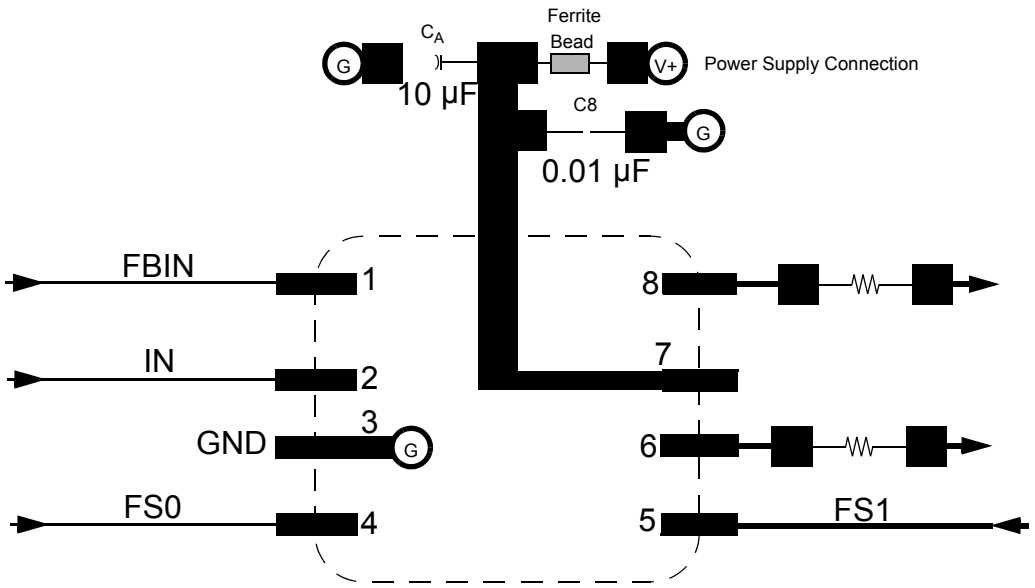
The CY23S02 is a pin-compatible upgrade of the Cypress W42C70-01. The CY23S02 addresses some application dependent problems experienced by users of the older device. Most importantly, it addresses the tracking skew problem induced by a reference that has Spread Spectrum Timing enabled on it.

Spread Aware

Many systems being designed now utilize a technology called spread spectrum frequency timing generation. Cypress has been one of the pioneers of SSFTG development, and we designed this product so as not to filter off the Spread Spectrum feature of the Reference input, assuming it exists. When a zero delay buffer is not designed to pass the SS feature through, the result is a significant amount of tracking skew which may cause problems in systems requiring synchronization.

For more details on Spread Spectrum timing technology, please see the Cypress application note titled, “EMI Suppression Techniques with Spread Spectrum Frequency Timing Generator (SSFTG) ICs.”

Figure 1. Schematic/Suggested Layout



How to Implement Zero Delay

Typically, zero delay buffers (ZDBs) are used because a designer wants to provide multiple copies of a clock signal in phase with each other. The whole concept behind ZDBs is that the signals at the destination chips are all going HIGH at the same time as the input to the ZDB. In order to achieve this, layout must compensate for trace length between the ZDB and the target devices. The method of compensation is described below.

External feedback is the trait that allows for this compensation. The PLL on the ZDB causes the feedback signal to be in phase with the reference signal. When laying out the board, match the trace lengths between the output being used for feed back and the FBIN input to the PLL.

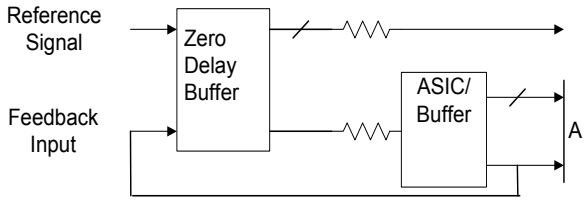
If it is desirable to either add a little delay, or slightly precede the input signal, this may also be affected by either making the trace to the FBIN pin a little shorter or a little longer than the traces to the devices being clocked.

Inserting Other Devices in Feedback Path

Another nice feature available due to the external feedback is the ability to synchronize signals up to the signal coming from some other device. This implementation can be applied to any device (ASIC, multiple output clock buffer/driver, and so on) that is put into the feedback path.

Referring to Figure 2, if the traces between the ASIC/Buffer and the destination of the clock signal(s) (A) are equal in length to the trace between the buffer and the FBIN pin, the signals at the destination(s) device is driven HIGH at the same time the Reference clock provided to the ZDB goes HIGH. Synchronizing the other outputs of the ZDB to the outputs from the ASIC/Buffer is more complex however, as any propagation delay in the ASIC/Buffer must be accounted for.

Figure 2. Six Output Buffer in the Feedback Path



Phase Alignment

In cases where OUT1 (i.e., the higher frequency output) is connected to FBIN input pin the output OUT2 rising edges may be either 0° or 180° phase aligned to the IN input waveform (as set randomly when the input and/or power is supplied). If OUT2 is desired to be rising-edge aligned to the IN input's rising edge, then connect the OUT2 (i.e., the lowest frequency output) to the FBIN pin. This setup provides a consistent input-output phase relationship.

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage temperature	–65 to +150	°C
T_A	Operating temperature	0 to +70	°C
T_B	Ambient temperature under bias	–55 to +125	°C
P_D	Power dissipation	0.5	W

DC Electrical Characteristics

T_A = 0 °C to 70 °C or –40 °C to 85 °C, V_{DD} = 3.3 V ± 5%

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
I_{DD}	Supply current	Unloaded, 133 MHz	–	17	35	mA
V_{IL}	Input low voltage		–	–	0.8	V
V_{IH}	Input high voltage		2.0	–	–	V
V_{OL}	Output low voltage	I_{OL} = 8 mA	–	–	0.4	V
V_{OH}	Output high voltage	I_{OH} = 8 mA	2.4	–	–	V
I_{IL}	Input low current	V_{IN} = 0 V	–40	–	5	µA
I_{IH}	Input high current	V_{IN} = V_{DD}	–	–	5	µA

DC Electrical Characteristics

T_A = 0 °C to 70 °C or –40 °C to 85 °C, V_{DD} = 5 V ± 10%

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current	Unloaded, 133 MHz	–	31	50	mA
V_{IL}	Input Low Voltage		–	–	0.8	V
V_{IH}	Input High Voltage		2.0	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 8 mA	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = 8 mA	2.4	–	–	V
I_{IL}	Input Low Current	V_{IN} = 0 V	–80	–	5	µA
I_{IH}	Input High Current	V_{IN} = V_{DD}	–	–	5	µA

Thermal Resistance

Parameter [1]	Description	Test Conditions	8-pin SOIC	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	132	°C/W
θ_{JC}	Thermal resistance (junction to case)		43	°C/W

Note
1. These parameters are guaranteed by design and are not tested.

AC Electrical Characteristics

T_A = 0 °C to +70 °C or –40 °C to 85 °C, V_{DD} = 3.3 V ± 5%

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
f_{IN}	Input frequency [2]	OUT2 = REF	10	–	133	MHz
f_{OUT}	Output frequency	OUT1	20	–	133	MHz
t_R	Output rise time	0.8 V to 2.0 V, 15-pF load	–	–	3.5	ns
t_F	Output fall time	2.0 V to 0.8 V, 15-pF load	–	–	2.5	ns
t_{ICLKR}	Input clock rise time [3]		–	–	10	ns
t_{ICLKF}	Input clock fall time [3]		–	–	10	ns
t_{PD}	FBIN to IN (Reference Input) Skew [4, 5]		–	–	300	ps
t_{DC}	Duty cycle [6]	Note 6	40	50	60	%
t_{LOCK}	PLL lock time	Power supply stable	–	–	1.0	ms
t_{JC}	Jitter, Cycle-to-Cycle [7]	OUT1	–	200	300	ps
		OUT2	–	90	300	ps
t_{SKEW}	Output-output Skew		–	65	250	ps
t_{PD}	Propagation delay		–350	90	350	ps

AC Electrical Characteristics

T_A = 0 °C to +70 °C or –40 °C to 85 °C, V_{DD} = 5 V ± 10%

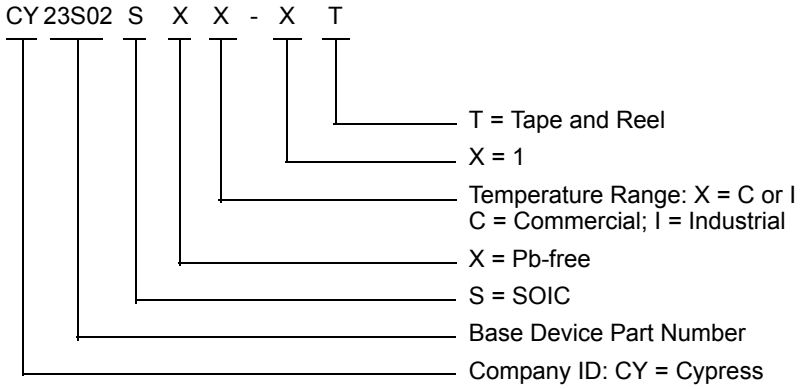
Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
f_{IN}	Input frequency [2]	OUT2 = REF	10	—	133	MHz
f_{OUT}	Output frequency	OUT1	20	—	133	MHz
t_R	Output rise time	0.8 V to 2.0 V, 15-pF load	—	—	3.5	ns
t_F	Output fall time	2.0 V to 0.8 V, 15-pF load	—	—	2.5	ns
t_{ICLKR}	Input clock rise time [3]		—	—	10	ns
t_{ICLKF}	Input clock fall time [3]		—	—	10	ns
t_{PD}	FBIN to IN (Reference Input) Skew [4, 5]		—	—	300	ps
t_D	Duty cycle [8, 9]		40	50	60	%
t_{LOCK}	PLL lock time	Power supply stable	—	—	1.0	ms
t_{JC}	Jitter, Cycle-to-Cycle [7]	OUT1	—	200	300	ps
		OUT2	—	90	300	ps
t_{SKEW}	Output-output skew		—	65	250	ps
t_{PD}	Propagation delay		–350	90	350	ps

Notes
2. Input frequency is limited by output frequency range and input to output frequency multiplication factor (that is determined by circuit configuration).
3. Longer input rise and fall time will degrade skew and jitter performance.
4. All AC specifications are measured with a 50 Ω transmission line, load terminated with 50 Ω to 1.4 V.
5. Skew is measured at 1.4 V on rising edges.
6. Duty cycle is measured at 1.4 V.
7. Jitter is measured on 133-MHz signal at 1.4 V, low frequency jitter = 350 ps.
8. Duty cycle is measured at 1.4 V, 120 MHz.
9. Duty cycle at 133 MHz is 35/65 worst case.

Ordering Information

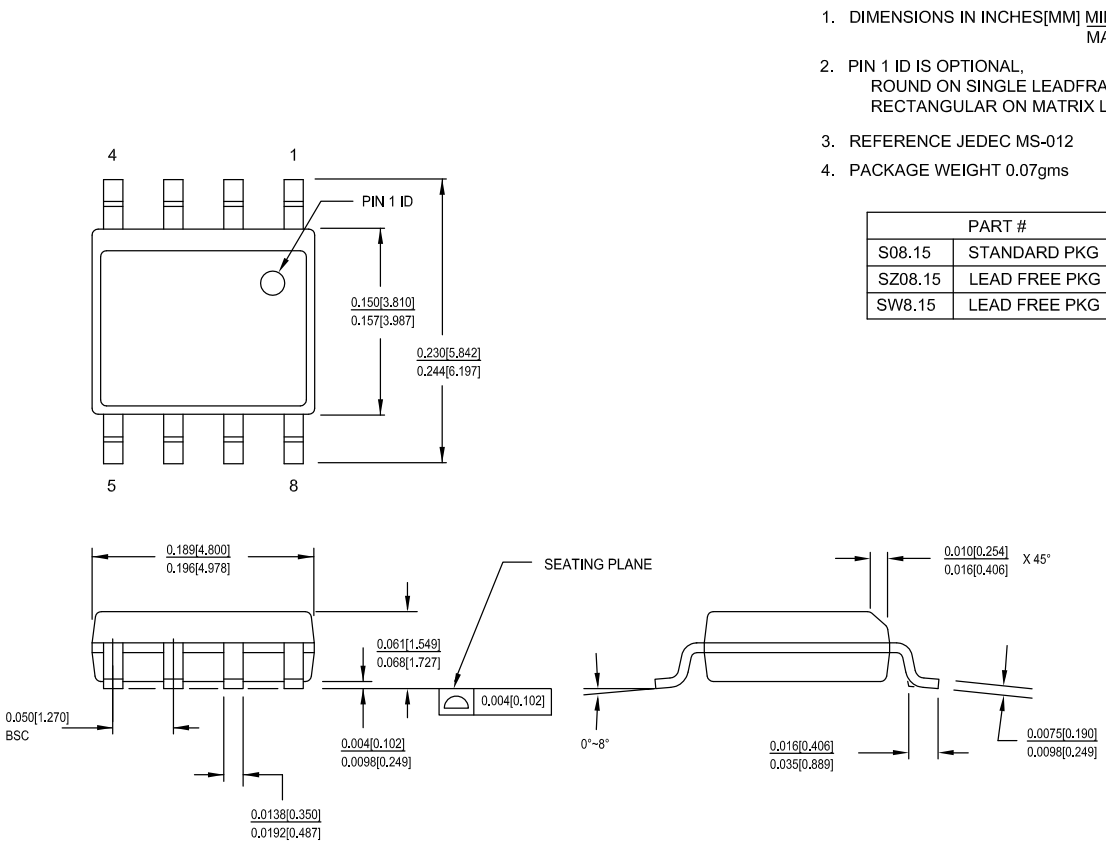
Ordering Code	Package Type	Temperature Grade
Pb-free		
CY23S02SXI-1	8-pin SOIC (150 mil)	Industrial, –40 °C to 85 °C
CY23S02SXI-1T	8-pin SOIC (150 mil) - Tape and Reel	Industrial, –40 °C to 85 °C

Ordering Code Definitions



Package Diagram

Figure 3. 8-pin SOIC (150 Mils) S0815/SZ815/SW815 Package Outline, 51-85066



Acronyms

Acronym	Description
ASIC	application-specific integrated circuit
EMI	electromagnetic interference
PLL	phase-locked loop
SOIC	small outline integrated circuit
SSFTG	Spread Spectrum Frequency Timing Generator
VCO	voltage controlled oscillator
ZDB	zero delay buffer

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
µA	microampere
mA	milliampere
ms	millisecond
MHz	megahertz
ns	nanosecond
pF	picofarad
ps	picosecond
V	volt
W	watt

Document History Page

Document Title: CY23S02, Spread Aware™, Frequency Multiplier, and Zero Delay Buffer Document Number: 38-07155				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110265	12/18/01	SZV	Change from Spec number: 38-00795 to 38-07155
OBS	292037	See ECN	RGL	To Obsolete the DS
*B	348376	See ECN	RGL	Minor Change: Re-activate the Spec (Only commercial are obsoleted, all industrial parts area still active).
*C	378857	See ECN	RGL	Updated Overview: Added Phase Alignment. Add typical char data.
*D	2894970	03/23/2010	KVM	Updated Ordering Information (Removed inactive parts). Updated Package Diagram.
*E	3339549	08/08/2011	PURU	Added Ordering Code Definitions under Ordering Information. Updated Package Diagram. Added Acronyms and Units of Measure.
*F	4499739	09/11/2014	TAVA	Updated Package Diagram: spec 51-85066 – Changed revision from *E to *F. Updated to new template. Completing Sunset Review.
*G	4580603	11/26/2014	TAVA	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*H	5276080	05/18/2016	PSR	Added Thermal Resistance. Updated Package Diagram: spec 51-85066 – Changed revision from *F to *H. Updated to new template.

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