CY2037

High-Accuracy EPROM-Programmable PLL Die for Crystal Oscillators

Features

- Erasable programmable read only memory (EPROM) - programmable die for in-package programming of crystal oscillators
- High resolution Phase locked loop (PLL) with 12-bit multiplier and 10-bit divider
- EPROM programmable capacitor tuning array with optional shadow register
- Twice programmable die
- Simple two-wire programming interface
- On-chip oscillator runs from 10 MHz to 30 MHz fundamental tuned crystal
- EPROM-selectable Transistor transistor logic (TTL) or Complementary metal oxide semiconductor (CMOS) duty cycle levels
- Operating frequency:
  - 1 MHz to 133 MHz at 5 V
  - 1 MHz to 100 MHz at 3.3 V
  - 1 MHz to 66.6 MHz at 2.7 V
- Eight selectable post divide options, using PLL or reference oscillator output
- Programmable asynchronous or synchronous OE and power-down (PD#) modes(CY2037 and CY2037-2)
- Frequency select (CY2037-3)
- Low jitter outputs typically:
  - < ±100 ps (pk-pk) at 5 V and f > 33 MHz
  - < ±125 ps (pk-pk) at 3.3 V and f > 33 MHz
- 3.3 V or 5 V operation
- Small die
- Controlled rise and fall times and output slew rate

Table 1. Device Functionality: Output Frequencies

Parameter	Description	Condition	Min	Max	Unit
Fo	Output frequency	V_{DD} = 4.5 V to 5.5 V	1	133	MHz
		V_{DD} = 3.0 V to 3.6 V	1	100	MHz
		V_{DD} = 2.7 V to 3.0 V	1	66	MHz

Functional Description

CY2037 is an EPROM-programmable, high-accuracy, PLL-based die designed for the crystal oscillator market. The die attaches directly to a low cost 10 to 30 MHz crystal and can be packaged into a 4-pin through-hole or surface mount packages. The oscillator devices may be stocked as blank parts and custom frequencies programmed in-package at the last stage before shipping. This enables fast-turn manufacture of custom and standard crystal oscillators without the need for dedicated, expensive crystals.

CY2037 contains an on-chip oscillator and a unique oscillator tuning circuit for fine-tuning of the output frequency. The crystal C_{load} may be selectively adjusted by programming a set of seven EPROM bits. This feature is used to compensate for crystal variations or to obtain a more accurate synthesized frequency.

CY2037 uses EPROM programming with a simple two-wire, 4-pin interface that includes V_{SS} and V_{DD}. Clock outputs may be generated up to 133 MHz at 5 V or up to 100 MHz at 3.3 V. The entire configuration can be reprogrammed once, which allows the programmed inventory to be altered or reused.

CY2037 PLL die is designed for very high resolution. It has a 12-bit feedback counter multiplier and a 10-bit reference counter divider. This enables the synthesis of highly accurate and stable output clock frequencies with zero or low PPM error. The clock is further modified by eight output divider options of 1, 2, 4, 8, 16, 32, 64, and 128. The divider input can be selected as the PLL or crystal oscillator output, providing a total of 16 separate output options. For further flexibility, the ouput is selectable between TTL and CMOS duty cycle levels.

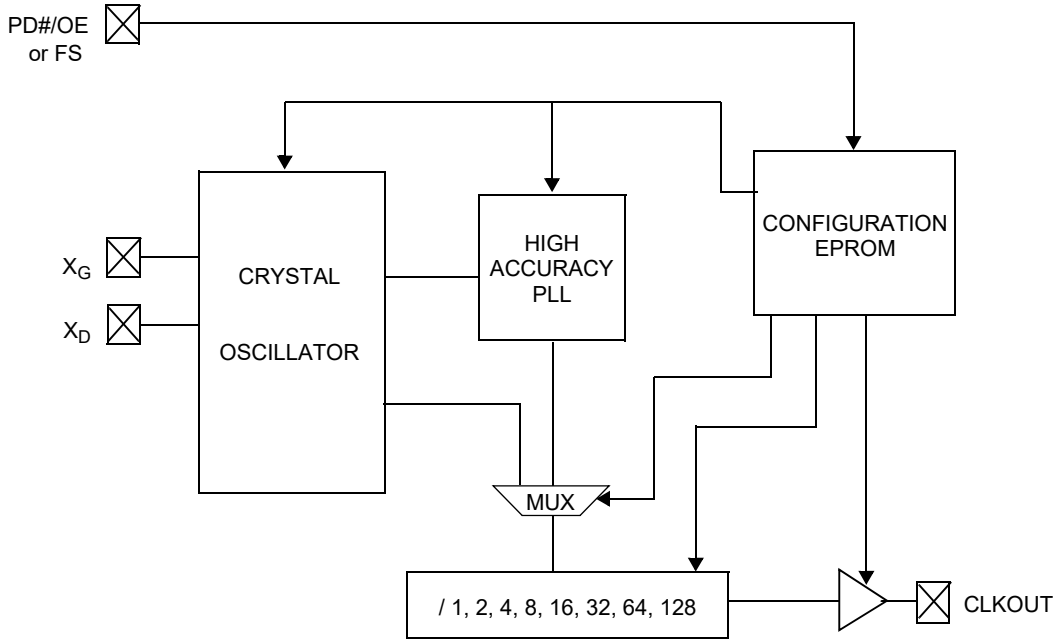
CY2037 also contain flexible power management controls. These parts include both power down (PD#) and output enable (OE) features with integrated pull-up resistors. The PD# and OE modes have an additional setting to determine timing (asynchronous or synchronous) with respect to the output signal. When PD# or OE modes are enabled, CLKOUT is tri-stated and pulled low by a weak pull-down. In PD# mode, all active circuitry on chip get shutdown, where in OE mode PLL and oscillator remain operating.

Controlled rise and fall times, unique output driver circuits, and innovative circuit layout techniques enable CY2037 to have low jitter and accurate outputs, making it suitable for most PC, networking, and consumer applications.

On the other hand, CY2037-3 contains a frequency select function in place of the power-down and output enable modes. For example, consumer products often require frequency compatibility with different electrical standards around the world. With this frequency select feature, a product that incorporates CY2037-3 could be compatible with both NTSC for North American, and PAL for Europe by simply changing the FS line. The twice programmable feature is absent in CY2037-3, because the second EPROM row is now being used for the alternate frequency.

For a complete list of related documentation, click here.

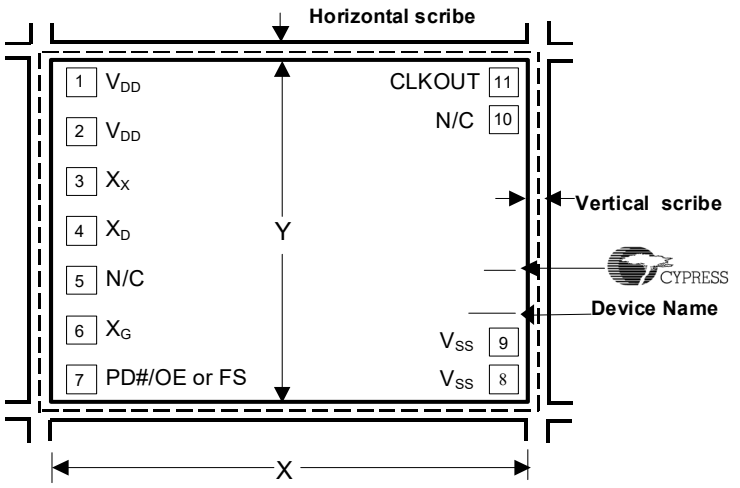
Logic Block Diagram



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Die Pad Description



Note:
Active die size:
X = 55.9 mils / 1420.1 µm
Y = 40.9 mils / 1039.4 µm
Scribe:
X (horizontal) = 3.1mils / 80 µm
Y (vertical) = 3.1 mils / 80 µm
Bond pad opening: 85 µm x 85 µm
Pad pitch: 125 µm x 125 µm
(pad center to pad center)
Bottom side of Die can be connected to Vss or can be isolated. Do not connect to V_{DD}.

CY2037EBWAF-IL	7C80383A
CY2037-2WAF-IL	7C80381A
CY2037-311WAF-IL	7C80340A
CY2037-209WAF-IL	7C80381A

Die Pad Summary

Name	Die Pad	X Coordinate (µm)	Y Coordinate (µm)	Description
V_{DD}	1, 2	124.7	855.6, 731	Voltage supply
V_{SS}	8, 9	1291.35	99.6, 225.2	Ground
X_D	4	124.7	481.8	Crystal connection
X_X	3	124.7	606.4	No connect [1]
X_G	6	124.7	232.6	Crystal connection
PD#/OE or FS	7	124.7	108	CY2037 and CY2037-2: EPROM-programmable power-down or output enable pad CY2037-3: Frequency select. Serves as V_{PP} in programming mode for all devices
CLKOUT	11	1282.45	901.8	Clock output. Also serves as three-state input during programming.
N/C	5, 10	124.7, 1282.45	357.2, 769.4	No connect (so do not bond to these pads)

Note
1. For customers not bonding the X_D or X_G pad to external pins, an alternative bonding option would be shorting the Xx pad to the X_D pad.

EPROM Configuration Block

Table 2 summarizes the features that are configurable by EPROM. Refer “7C8038x/7C8034X Proprietary Specification” for further details. This specification can be obtained from your Cypress factory representative.

Table 2. EPROM Adjustable Features

Adjustable Features	
Adjust frequency	Feedback counter value (P)
	Reference counter value (Q)
	Output divider selection
Oscillator tuning (load capacitance values)	
Duty cycle levels (TTL or CMOS)	
Power management mode (OE or PD#)	
Power management timing (synchronous or asynchronous)	

PLL Output Frequency

CY2037 contains a high resolution PLL with 12-bit multiplier and 10-bit divider. The output frequency of the PLL is determined by the following formula:

$$F_{PLL} = \frac{2 \bullet (P + 5)}{(Q + 2)} \bullet F_{REF}$$

In this formula, P is the feedback counter value and Q is the reference counter value. P and Q are EPROM programmable values.

Power Management Features

CY2037 contains EPROM-programmable PD# and OE functions. If power-down (PD#) is selected, all active circuitry on the chip is shut down, output is tri-stated and pulled low by a weak pull-down when the control pin goes LOW. The weak pull-down is easily overdriven by another active CLKOUT for applications that require multiple CLKOUTs on a single signal path.The oscillator and PLL circuits must relock when the part leaves the power-down mode. If output enable (OE) mode is selected, the output is tri-stated and weakly pulled low when the control pin goes low. In this mode the oscillator and PLL circuits continue to operate, allowing a rapid return to normal operation when the control input is deasserted.

In addition, the PD# and OE modes can be programmed to occur synchronously or asynchronously with respect to the output signal. When the asynchronous setting is used, the power-down or output disable occurs immediately (allowing for logic delays), regardless of the position in the clock cycle. However, when the synchronous setting is used, the part waits for a falling edge at the output before the power-down or output enable signal is initiated, thus preventing output glitches. In asynchronous or synchronous setting, the output is always enabled synchronously by waiting for the next falling edge of the output.

Crystal Oscillator Tuning Circuit

CY2037 contains a unique tuning circuit to fine-tune the output frequency of the device. The tuning circuit consists of an array of eleven load capacitors on both sides of the oscillator drive inverter. The capacitor load values are EPROM-programmable and may be increased in small increments. As the capacitor load is increased the circuit is fine-tuned to a lower frequency. The capacitor load values vary from 0.17 pF to 8 pF for a 100:1 total control ratio. The tuning increments are shown in Table 3 on page 6. Refer to “7C8038x/7C8034x Proprietary Specification” for further details.

Figure 1. Crystal Oscillator Tuning Circuit

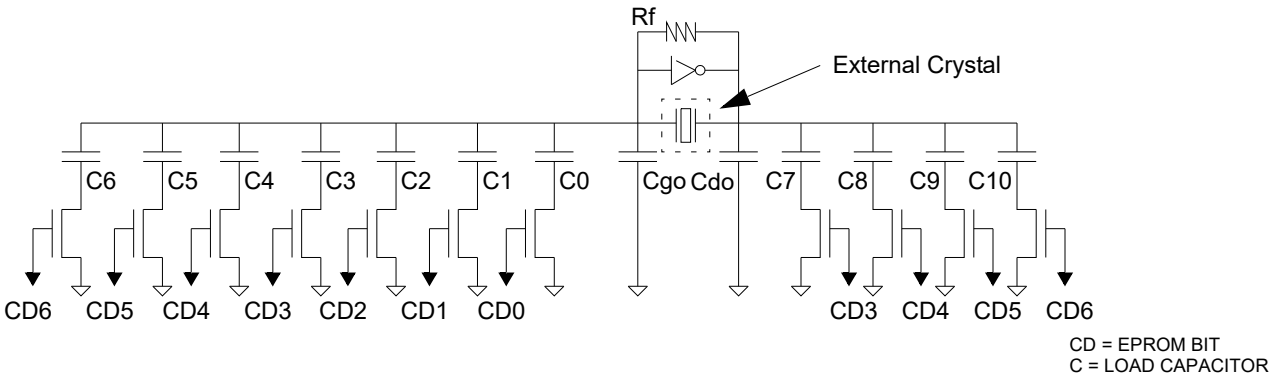


Table 3. Crystal Oscillator Parameter

Parameter	Description	Min	Typ	Max	Unit
R_f	Feedback resistor, V_{DD} = 4.5 V to 5.5 V Feedback resistor, V_{DD} = 2.7 V to 3.6 V	0.5 1.0	2 4	3.5 9.0	MΩ MΩ
Capacitors have ± 20% tolerance					
C_g	Gate capacitor	–	13	–	pF
C_d	Drain capacitor	–	9	–	pF
C_0	Series capacitor	–	0.27	–	pF
C_1	Series capacitor	–	0.52	–	pF
C_2	Series capacitor	–	1.00	–	pF
C_3	Series capacitor	–	0.7	–	pF
C_4	Series capacitor	–	1.4	–	pF
C_5	Series capacitor	–	2.6	–	pF
C_6	Series capacitor	–	5.0	–	pF
C_7	Series capacitor	–	0.45	–	pF
C_8	Series capacitor	–	0.85	–	pF
C_9	Series capacitor	–	1.7	–	pF
C_{10}	Series capacitor	–	3.3	–	pF

CY2037 Vs CY2037-2

CY2037 contains a shadow register in addition to the EPROM register. The shadow register is an exact copy of the EPROM register and is the default register when the valid bit is not set. It is useful when the prototype or production environment calls for measuring and adjusting the CLKOUT frequency several times. Multiple adjustments can be performed with the shadow register. After the required frequency is achieved the EPROM register is permanently programmed.

Some production flows do not require the use of the shadow register. If this is the case, then CY2037-2 is the chosen device and CY2037-2 has a disabled shadow register. CY2037-3 contains the shadow register.

Frequency Select Feature of CY2037-3

CY2037-3 contains a frequency select function in place of the power-down and the output enable functions. With the frequency select feature, customers can switch two different frequencies that are configured in the two EPROM rows. Table 4 lists the definition of the frequency select pin (FS).

Table 4. Frequency Select Pin Decoding for CY2037-3

FS Pin	Output Frequency
0	From EPROM row 0 configuration
1	From EPROM row 1 configuration

Inkless Die Pick Map (DPM) Format

Cypress ships inkless wafers to customers with an accompanying die pick map, which is used to determine the good die for assembly and programming. Customers can also access individual DPM files at their convenience through ftp.cypress.com with a valid user account login and password. Contact your local Cypress Field Application Engineer (FAE) or sales representative for a customer FTP account. The DPM files are named with the fab lot number and wafer number scribed on the wafer. The DPM files are transferred to the customer's FTP account when the factory ships out the wafers against their purchase order (PO).

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.[2]

Supply voltage .....–0.5 V to +7.0 V

Input voltage .....–0.5 V to V_{DD} + 0.5 V

Storage temperature (non-condensing) ..... 55 °C to +150 °C

Junction temperature ..... –40 °C to +100 °C

Static discharge voltage
(per MIL-STD-883, method 3015) ..... 2000 V

Operating Conditions

Parameter	Description	Min	Max	Unit
V_{DD}	Supply voltage (3.3 V) Supply voltage (5.0 V)	2.7 4.5	3.6 5.5	V V
T_{AJ} [3]	Operating temperature, Junction	–10	+100	°C
C_{TTL}	Max. capacitive load on outputs for TTL levels V_{DD} = 4.5 V to 5.5 V, output frequency = 1 MHz to 40 MHz V_{DD} = 4.5 V to 5.5 V, output frequency = 40 MHz to 133 MHz	–	 50 25	 pF pF
C_{CMOS}	Max. capacitive load on outputs for CMOS levels V_{DD} = 4.5 V to 5.5 V, output frequency = 1 MHz to 66.6 MHz V_{DD} = 4.5 V to 5.5 V, output frequency = 66.6 MHz to 133 MHz V_{DD} = 3.0 V to 3.6 V, output frequency = 1 MHz to 40 MHz V_{DD} = 3.0 V to 3.6 V, output frequency = 40 MHz to 100 MHz V_{DD} = 2.7 V to 3.0 V, output frequency = 1 MHz to 66 MHz	–	 50 25 30 15 15	 pF pF pF pF pF
X_{REF}	Reference frequency, input crystal. Fundamental tuned crystals only	10	30	MHz
t_{PU}	Power up time for all V_{DD}'s to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Notes
2. Stresses greater than listed can impair the life of the device.
3. This product is sold in die form so operating conditions are specified for the die, or junction temperature.

Electrical Characteristics

Over the Operating Range

Parameter [4]	Description	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Low-level input voltage	V_{DD} = 4.5 V to 5.5 V V_{DD} = 2.7 V to 3.6 V	–	–	0.8 0.2 × V_{DD}	V V
V_{IH}	High-level input voltage	V_{DD} = 4.5 V to 5.5 V V_{DD} = 2.7 V to 3.6 V	2.0 0.7 × V_{DD}	–	–	V V
V_{OL}	Low-level output voltage	V_{DD} = 4.5 V to 5.5 V, I_{OL} = 16 mA V_{DD} = 2.7 V to 3.6 V, I_{OL} = 8 mA	–	–	0.4 0.4	V V
V_{OHCMOS}	High-level output voltage, CMOS levels	V_{DD} = 4.5 V to 5.5 V, I_{OH} = –16 mA V_{DD} = 2.7 V to 3.6 V, I_{OH} = –8 mA	V_{DD} – 0.4 V_{DD} – 0.4	–	–	V V
V_{OHTTL}	High-level output voltage, TTL levels	V_{DD} = 4.5 V to 5.5 V, I_{OH} = –8 mA	2.4	–	–	V
I_{IL}	Input low-current	V_{IN} = 0 V	–	–	10	µA
I_{IH}	Input high-current	V_{IN} = V_{DD}	–	–	5	µA
I_{DD}	Power supply current, Unloaded	V_{DD} = 4.5 V to 5.5 V, output frequency ≤ 133 MHz V_{DD} = 2.7 V to 3.6 V, output frequency ≤ 100 MHz	–	–	45 25	mA mA
I_{DDS} [5]	Standby current	V_{DD} = 2.7 V to 3.6 V	–	10	50	µA
R_{UP}	Input pull-up resistor	V_{DD} = 4.5 V to 5.5 V, V_{IN} = 0 V V_{DD} = 4.5 V to 5.5 V, V_{IN} = 0.7 × V_{DD}	1.1 50	3.0 100	8.0 200	MΩ kΩ
I_{PD_CLKOUT}	CLKOUT pull-down current (OE or PD# mode)	V_{DD} = 5.0 V	–	20	–	µA

Notes
4. This part was characterized in a 20-pin SOIC package with external crystal, Electrical Characteristics can change with other package types.
5. If external reference is used, it is required to stop the reference (set reference to LOW) during power-down.

Output Clock Switching Characteristics

Over the Operating Range

Parameter [6]	Description	Test Conditions	Min	Typ	Max	Unit
t_{1w}	Output duty cycle at 1.4 V, V_{DD} = 4.5 V to 5.5 V $t_{1w} = t_{1A} \div t_{1B}$ Figure 2 on page 11.	1 MHz to 40 MHz, $C_L \le 50$ pF 40 MHz to 66 MHz, $C_L \le 15$ pF 66 MHz to 125 MHz, $C_L \le 25$ pF 125 MHz to 133 MHz, $C_L \le 15$ pF	45 45 40 40	–	55 55 60 60	% % % %
t_{1x}	Output duty cycle at $V_{DD}/2$, V_{DD} = 4.5 V to 5.5 V $t_{1x} = t_{1A} \div t_{1B}$ Figure 2 on page 11.	1 MHz to 66.6 MHz, $C_L \le 25$ pF 66.6 MHz to 125 MHz, $C_L \le 25$ pF 125 MHz to 133 MHz, $C_L \le 15$ pF	45 40 40	–	55 60 60	% % %
t_{1y}	Output duty cycle at $V_{DD}/2$, V_{DD} = 3.0 V to 3.6 V $t_{1y} = t_{1A} \div t_{1B}$ Figure 2 on page 11.	1 MHz to 40 MHz, $C_L \le 30$ pF 40 MHz to 100 MHz, $C_L \le 15$ pF	45 40	–	55 60	% %
t_{1z}	Output duty cycle at $V_{DD}/2$, V_{DD} = 2.7 V to 3.0 V $t_{1z} = t_{1A} \div t_{1B}$ Figure 2 on page 11.	1 MHz to 40 MHz, $C_L \le 15$ pF 40 MHz to 66.6 MHz, $C_L \le 10$ pF	40 40	–	60 60	% %
t_2	Output clock rise time Figure 3 on page 11.	Between 0.8 V to 2.0 V, V_{DD} = 4.5 V to 5.5 V, C_L = 50 pF Between 0.8 V to 2.0 V, V_{DD} = 4.5 V to 5.5 V, C_L = 25 pF Between 0.8 V to 2.0 V, V_{DD} = 4.5 V to 5.5 V, C_L = 15 pF Between 0.2 V_{DD} to 0.8 V_{DD}, V_{DD} = 4.5 V to 5.5 V, C_L = 50 pF Between 0.2 V_{DD} to 0.8 V_{DD}, V_{DD} = 3.0 V to 3.6 V, C_L = 30 pF Between 0.2 V_{DD} to 0.8 V_{DD}, V_{DD} = 2.7 V to 3.6 V, $_L$ = 15 pF	–	–	1.8 1.2 0.9 3.4 4.0 2.4	ns ns ns ns ns ns
t_3	Output clock fall time Figure 3 on page 11.	Between 0.8 V to 2.0 V, V_{DD} = 4.5 V to 5.5 V, C_L = 50 pF Between 0.8 V to 2.0 V, V_{DD} = 4.5 V to 5.5 V, C_L = 25 pF Between 0.8 V to 2.0 V, V_{DD} = 4.5 V to 5.5 V, C_L = 15 pF Between 0.2 V_{DD} to 0.8 V_{DD}, V_{DD} = 4.5 V to 5.5 V, C_L = 50 pF Between 0.2 V_{DD} to 0.8 V_{DD}, V_{DD} = 3.0 V to 3.6 V, C_L = 30 pF Between 0.2 V_{DD} to 0.8 V_{DD}, V_{DD} = 2.7 V to 3.6 V, C_L = 15 pF	–	–	1.8 1.2 0.9 3.4 4.0 2.4	ns ns ns ns ns ns
t_4	Startup time out of power-down Figure 4 on page 11.	PD# pin LOW to HIGH[7]	–	1	2	ms

Notes
6. Not all parameters measured in production testing.
7. Oscillator start time cannot be guaranteed for all crystal types. This specification is for operation with AT cut crystals with ESR < 70 ohms.

Output Clock Switching Characteristics *(continued)*

Over the Operating Range

Parameter [6]	Description	Test Conditions	Min	Typ	Max	Unit
t_{5a}	Power-down delay time (synchronous setting) Figure 4 on page 11.	PD# pin LOW to output LOW (T = period of output clk)	–	T/2	T + 10	ns
t_{5b}	Power-down delay time (asynchronous setting) Figure 4 on page 11.	PD# pin LOW to output LOW	–	10	15	ns
t_6	Power-up time Figure 5 on page 11.	From power-on[8]	–	1	2	ms
t_{7a}	Output disable time (synchronous setting) Figure on page 13.	OE pin LOW to output high Z (T = period of output clk)	–	T/2	T + 10	ns
t_{7b}	Output disable time (asynchronous setting) Figure on page 13.	OE pin LOW to output high Z	–	10	15	ns
t_8	Output enable time (always synchronous enable) Figure on page 13.	OE pin LOW to HIGH (T = period of output clk)	–	T	1.5T + 25	ns
t_9	Peak-to-peak period jitter Figure 7 on page 12.	V_{DD} = 4.5 V to 5.5 V, F_O > 33 MHz, VCO > 100 MHz V_{DD} = 2.7 V to 3.6 V, F_O > 33 MHz, VCO > 100 MHz V_{DD} = 2.7 V to 5.5 V, F_O < 33 MHz	–	±100 ±125 ±250	±125 ±200 1% of F_O	ps ps ps

Note

8. Oscillator start time cannot be guaranteed for all crystal types. This specification is for operation with AT cut crystals with ESR < 70 ohms.

Switching Waveforms

Figure 2. Duty Cycle Timing (t_{1w}, t_{1x}, t_{1y}, t_{1z})

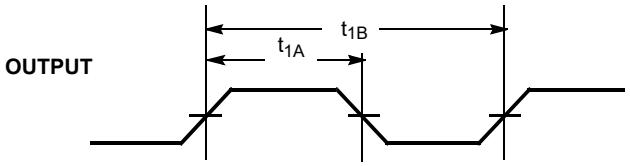


Figure 3. Output Rise/Fall Time

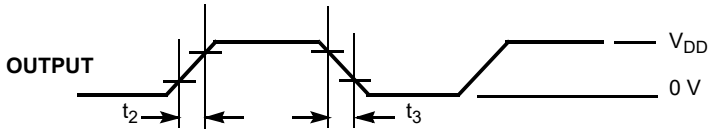


Figure 4. Power Down Timing (Synchronous and Asynchronous Modes)

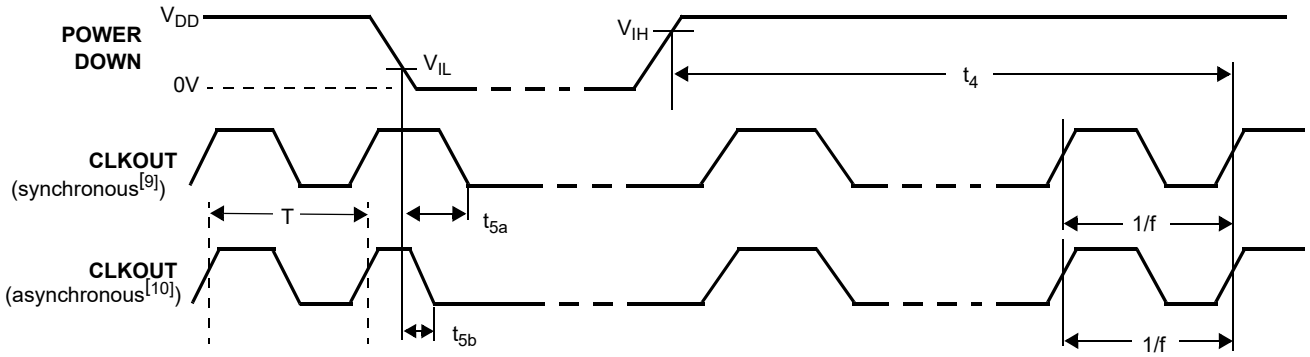
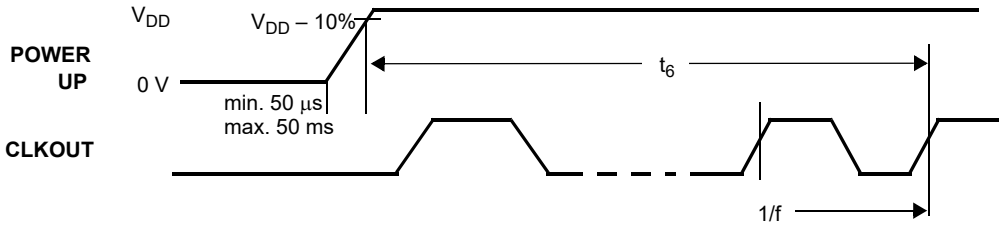


Figure 5. Power-Up Timing



Notes
9. In synchronous mode the power down or output tri-state is not initiated until the next falling edge of the output clock.
10. In asynchronous mode the power down or output tri-state occurs within 25 ns regardless of position in the output clock cycle.

Switching Waveforms *(continued)*

Figure 6. Output Enable Timing (Synchronous and Asynchronous Modes)

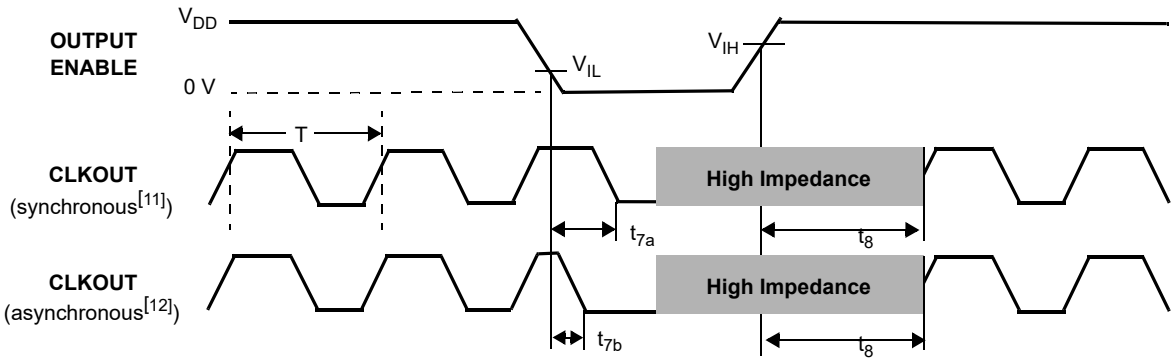
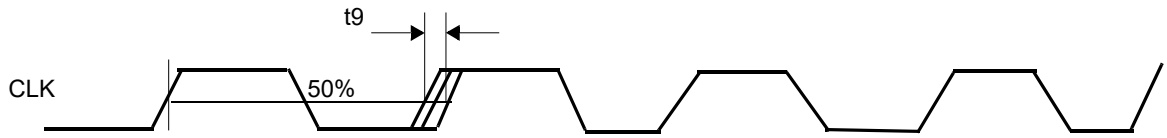


Figure 7. Period Jitter

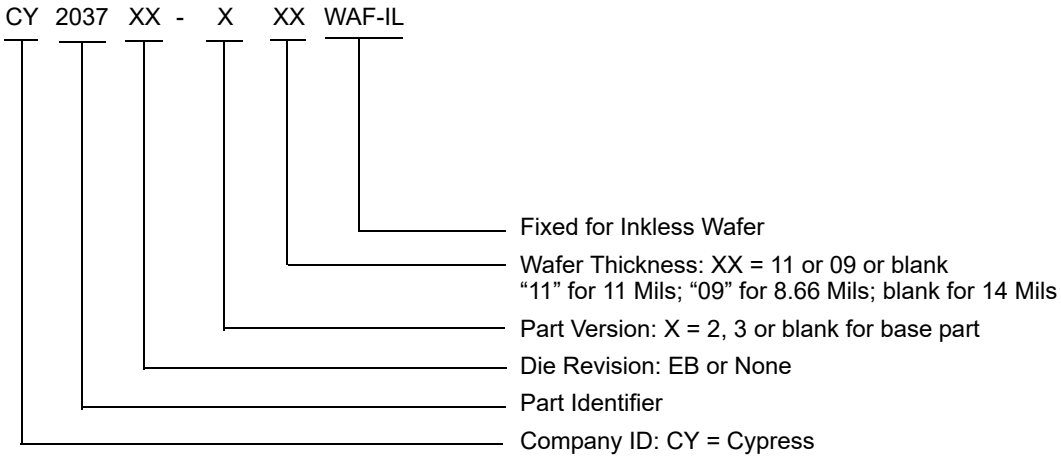


Notes
11. In synchronous mode the power down or output tri-state is not initiated until the next falling edge of the output clock.
12. In asynchronous mode the power down or output tri-state occurs within 25 ns regardless of position in the output clock cycle.

Ordering Information

Ordering Code	Type	Wafer Thickness	Operating Range
CY2037-2WAF-IL	Inkless wafer	14 ± 0.5 Mils	–10 °C to 100 °C
CY2037-311WAF-IL	Inkless wafer	11 ± 0.5 Mils	–10 °C to 100 °C
CY2037-209WAF-IL	Inkless wafer	8.66 ± 0.3 Mils	–10 °C to 100 °C

Ordering Code Definitions



Acronyms

Acronym	Description
CLKOUT	Clock Output
CMOS	Complementary Metal Oxide Semiconductor
DPM	Die Pick Map
EPROM	Erasable Programmable Read Only Memory
NTSC	National Television System Committee
OE	Output Enable
PAL	Phase Alternate Line
PD	Power Down
PLL	Phase Locked Loop
PPM	Parts Per Million
TTL	Transistor-Transistor Logic

Reference Documents

Reference documents are available through your local Cypress sales representative. You can also direct your requests to tsbusdev@cypress.com.

Document Number	Document Title	Description
71-00005	7C8038x/7C8034X proprietary specification	Appendix C contains programming specification for customer use

Document Conventions

Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degrees Celsius	µW	micro Watts
dB	decibels	mA	milli Amperes
dBc/Hz	decibels relative to the carrier per Hertz	mm	milli meters
fC	femto Coulomb	ms	milli seconds
fF	femto Farads	mV	milli Volts
Hz	Hertz	nA	nano Amperes
KB	1024 bytes	ns	nano seconds
Kbit	1024 bits	nV	nano Volts
kHz	kilo Hertz	Ω	ohms
kΩ	kilo ohms	pA	pico Amperes
MHz	mega Hertz	pF	pico Farads
MΩ	mega Ohms	pp	peak-to-peak
µA	micro Amperes	ppm	parts per million
µF	micro Farads	ps	pico seconds
µH	micro Henrys	sps	samples per second
µs	micro seconds	σ	sigma: one standard deviation
µV	micro Volts		
µVrms	micro Volts root-mean-square		

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Document Title: CY2037, High-Accuracy EPROM-Programmable PLL Die for Crystal Oscillators Document Number: 38-07354				
Revision	**ECN**	**Orig. of Change**	**Submission date**	**Description of Change**
**	112248	DSG	03/01/2002	Changed from Spec number: 38-00679 to 38-07354.
*A	121857	RBI	12/14/2002	Updated Operating Conditions: Added t_{PU} parameter and its details.
*B	291092	RGL	11/18/2004	Updated Absolute Maximum Ratings: Replaced “–40°C to +100°C” with “–10°C to +100°C” in ratings corresponding to “Junction Temperature”.
*C	522769	RGL	10/18/2006	Added CY2037B related information in all instances across the document. Added Die Pad Description. Updated Absolute Maximum Ratings: Replaced “–10°C to +100°C” with “–40°C to +100°C” in ratings corresponding to “Junction Temperature”. Updated Ordering Information: Updated part numbers.
*D	804376	RGL	02/26/2007	Minor Change: Post to external web.
*E	2192266	DPF / PYRS	03/11/2008	Added Inkless Die Pick Map (DPM) Format. Updated Ordering Information: Updated part numbers.
*F	2748211	TSAI	08/10/2009	Minor Change: Post to external web.
*G	2761988	KVM	09/14/2009	Updated Ordering Information: Removed the column “Status”. Updated part numbers. Added Note “Not for new designs. New designs should use inkless wafer ordering codes.” and referred in some MPNs. Added Note “Not for new designs. New designs should use CY2037BWAF-IL.” and referred in some MPNs.
*H	2906472	CXQ	04/07/2010	Updated Ordering Information: Updated part numbers.
*I	3022612	BASH	09/03/2010	Removed CY2037A part related information in all instances across the document. Updated Features: Replaced “Sixteen selectable post divide options” with “Eight selectable post divide options”. Updated Die Pad Description. Updated Crystal Oscillator Tuning Circuit: Updated Figure 1 (Removed “T” for Transistor). Updated Electrical Characteristics: Removed I_{OE_CLKOUT} parameter and its details. Added $I_{PD_CLOCKOUT}$ parameter and its details. Updated Switching Waveforms: Added Figure 6. Added Figure 7. Updated Ordering Information: Updated part numbers. Added Ordering Code Definitions. Added Acronyms, Reference Documents and Units of Measure. Completing Sunset Review.
*J	3069175	BASH	10/25/2010	Updated Die Pad Description: Removed CY2037B. Updated Ordering Information: Updated part numbers.

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Revision	**ECN**	**Orig. of Change**	**Submission date**	**Description of Change**
*K	4175824	CINM	11/13/2013	Updated Die Pad Description. Updated Ordering Information: Updated part numbers. Updated to new template. Completing Sunset Review.
*L	4575273	CINM	11/20/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*M	5542641	TAVA	12/05/2016	Updated to new template. Completing Sunset Review.
*N	6011854	PAWK	01/03/2018	Updated Ordering Information: Updated part numbers. Updated to new template.

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