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Continuity of document content
The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

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Continuity of Ordering Part Numbers

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For More Information

Please contact your local sales office for additional information about Cypress products and solutions.

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SUPPLEMENT

Am29F040B in Die Form

4 Megabit (512 K x 8-Bit)
CMOS 5.0 Volt-only, Uniform Sector Flash Memory

DISTINCTIVE CHARACTERISTICS

- **5.0 V ± 10% for read and write operations**
  - — Minimizes system level power requirements
- **Manufactured on 0.32 µm process technology**
  - — Compatible with 0.5 µm Am29F040 device
- **Low power consumption**
  - — 20 mA typical active read current
  - — 30 mA typical program/erase current
  - — 1 µA typical standby current (standard access time to active mode)
- **Flexible sector architecture**
  - — 8 uniform sectors of 64 Kbytes each
  - — Any combination of sectors can be erased
  - — Supports full chip erase
  - — Sector protection:

    A hardware method of locking sectors to prevent any program or erase operations within that sector
- **Embedded Algorithms**
  - — Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - — Embedded Program algorithm automatically writes and verifies bytes at specified addresses
- **Minimum 100,000 program/erase cycles per sector guaranteed**
- **20-year data retention at 125°C**
  - — Reliable operation for the life of the system
- **Compatible with JEDEC standards**
  - — Pinout and software compatible with single-power-supply Flash standard
  - — Superior inadvertent write protection
- **Data# Polling and toggle bits**
  - — Provides a software method of detecting program or erase cycle completion
- **Erase Suspend/Erase Resume**
  - — Suspends a sector erase operation to read data from, or program data to, a non-erasing sector, then resumes the erase operation

Not Recommended for New Design

Publication# **22930** Rev: **A** Amendment/**1**
Issue Date: **November 9, 2009**

GENERAL DESCRIPTION

The Am29F040B is a 4 Mbit, 5.0 volt-only Flash memory organized as 524,288 Kbytes of 8 bits each. The 512 Kbytes of data are divided into eight sectors of 64 Kbytes each for flexible erase capability. The 8 bits of data appear on DQ0–DQ7. This device is designed to be programmed in-system with the standard system 5.0 volt V_{CC} supply. A 12.0 volt V_{PP} is not required for write or erase operations. The device can also be programmed in standard EPROM programmers.

This device is manufactured using AMD's 0.32 µm process technology, and offers all the features and benefits of the Am29F040, which was manufactured using 0.5 µm process technology. In addtion, the Am29F040B has a second toggle bit, DQ2, and also offers the ability to program in the Erase Suspend mode.

To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device requires only a **single 5.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved via programming equipment.

The **Erase Suspend** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The system can place the device into the **standby mode**. Power consumption is greatly reduced in this mode.

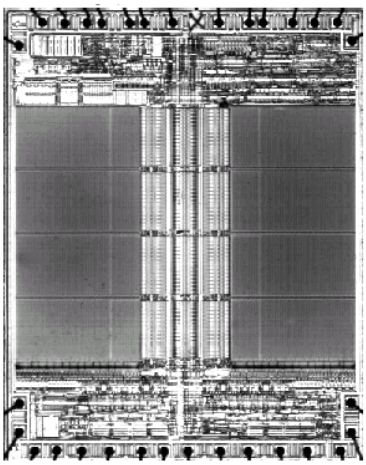
AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

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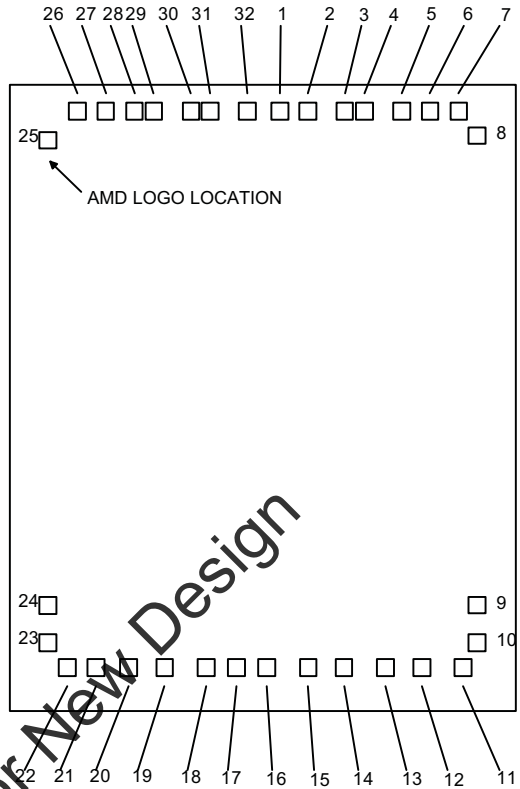
Electrical Specifications

Refer to the Am29F040B data sheet, document number 22286, for full electrical specifications on the Am29F040B in die form.

DIE PHOTOGRAPH



DIE PAD LOCATIONS



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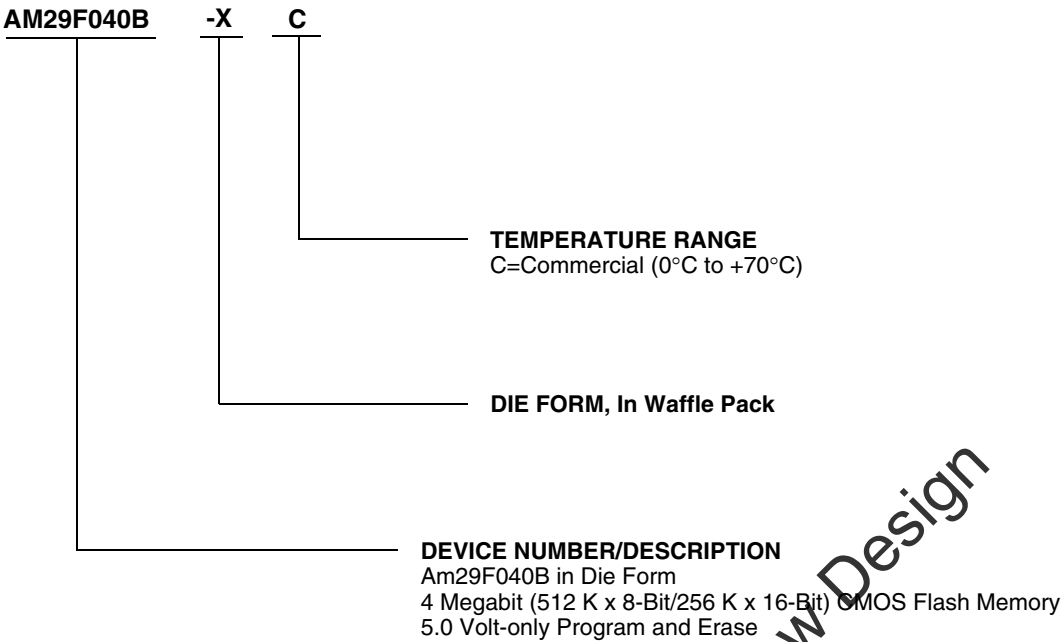
PAD DESCRIPTION

Pad	Signal	Pad Center (mils)		Pad Center (millimeters)	
		X	Y	X	Y
1	V_{CC}	0.00	0.00	0.0000	0.0000
2	WE#	7.90	0.00	0.2007	0.0000
3	A17	18.30	0.00	0.4648	0.0000
4	A14	23.80	0.00	0.6045	0.0000
5	A13	34.30	0.00	0.8712	0.0000
6	A8	42.30	0.00	1.0744	0.0000
7	A9	50.40	0.00	1.2802	0.0000
8	A11	55.60	–6.90	1.4122	–0.1753
9	OE#	55.50	–139.20	1.4097	–3.5357
10	A10	55.50	–149.80	1.4097	–3.8049
11	CE#	51.60	–156.80	1.3106	–3.9827
12	DQ7	40.00	–156.80	1.0160	–3.9827
13	DQ6	29.80	–156.80	0.7569	–3.9827
14	DQ5	18.10	–156.80	0.4597	–3.9827
15	DQ4	8.00	–156.80	0.2032	–3.9827
16	DQ3	–3.70	–156.80	–0.0940	–3.9827
17	V_{SS}	–12.20	–156.80	–0.3099	–3.9827
18	DQ2	–20.70	–156.80	–0.5258	–3.9827
19	DQ1	–32.40	–156.80	–0.8230	–3.9827
20	DQ0	–42.50	–156.80	–1.0795	–3.9827
21	A0	–51.70	–156.80	–1.3132	–3.9827
22	A1	–59.80	–156.80	–1.5189	–3.9827
23	A2	–65.30	–149.80	–1.6586	–3.8049
24	A3	–65.30	–139.30	–1.6586	–3.5382
25	A4	–65.30	–8.20	–1.6586	–0.2083
26	A5	–57.00	0.00	–1.4478	0.0000
27	A6	–49.00	0.00	–1.2446	0.0000
28	A7	–40.90	0.00	–1.0389	0.0000
29	A12	–35.50	0.00	–0.9017	0.0000
30	A15	–25.00	0.00	–0.6350	0.0000
31	A16	–19.60	0.00	–0.4978	0.0000
32	A18	–9.10	0.00	–0.2311	0.0000

Note: *The coordinates above are relative to the center of pad 1 and can be used to operate wire bonding equipment.*

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ORDERING INFORMATION



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PHYSICAL SPECIFICATIONS

Die Dimensions . . . . . 134 mils x 176 mils
. . . . . 3.42 mm x 5.02 mm

Die Thickness. . . . . ~500 µm/~20 mils

Bond Pad Size . . . . . 4.7 mils x 4.7 mils
. . . . . 119.7 µm x 119.7 µm

Pad Area Free of Passivation . . . . . 13.98 $mils^2$
. . . . . 9,025 μm^2

Pads Per Die 32

Bond Pad Metallization . . . . . Al/Cu

Die Backside . . . . . No metal,
. . . . . may be grounded (optional)

Passivation. . . . . SiN/SOG/SiN

DC OPERATING CONDITIONS

V_{CC} (Supply Voltage) . . . . . 4.5 V to 5.5 V

Junction Temperature Under Bias . . T_J (max) = 130°C

Operating Temperature
Commercial . . . . . 0°C to +70°C

MANUFACTURING INFORMATION

Manufacturing . . . . . FASL

Test . . . . . SDC

Manufacturing ID 98E07A

Preparation for Shipment . . . . . Penang, Malaysia

Fabrication Process. CS39S

Die Revision 2

SPECIAL HANDLING INSTRUCTIONS

Processing

Do not expose products in die form to ultraviolet light or process them at temperatures greater than 250°C. Failure to adhere to these handling instructions will result in irreparable damage to the devices. For best yield, AMD recommends assembly in a Class 10K clean room with 30% to 60% relative humidity.

Storage

Store at a maximum temperature of 30°C in a nitrogen-purged cabinet or vacuum-sealed bag. Observe all standard ESD handling procedures.

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TERMS AND CONDITIONS OF SALE FOR AMD NON-VOLATILE MEMORY DIE

All transactions relating to unpackaged die under this agreement shall be subject to AMD's standard terms and conditions of sale, or any revisions thereof, which revisions AMD reserves the right to make at any time and from time to time. In the event of conflict between the provisions of AMD's standard terms and conditions of sale and this agreement, the terms of this agreement shall be controlling.

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The liability of AMD under this warranty is limited, at AMD's option, solely to repair the Die, to send replacement Die, or to make an appropriate credit adjustment or refund in an amount not to exceed the original purchase price actually paid for the Die returned to AMD, provided that: (a) AMD is promptly notified by Buyer in writing during the applicable warranty period of any defect or nonconformity in the Die; (b) Buyer obtains authorization from AMD to return the defective Die; (c) the defective Die is returned to AMD by Buyer in accordance with AMD's shipping instructions set forth below; and (d) Buyer shows to AMD's satisfaction that such alleged defect or nonconformity actually exists and was not caused by any of the above-referenced Warranty Exclusions. Buyer shall ship such defective Die to AMD via AMD's carrier, collect. Risk of loss will transfer to AMD when the defective Die is provided to AMD's carrier. If Buyer fails to adhere to these warranty returns guidelines, Buyer shall assume all risk of loss and shall pay for all freight to AMD's specified location. The aforementioned provisions do not extend the original warranty period of any Die that has either been repaired or replaced by AMD.

WITHOUT LIMITING THE FOREGOING, EXCEPT TO THE EXTENT THAT AMD EXPRESSLY WARRANTS TO BUYER IN A SEPARATE AGREEMENT SIGNED BY AMD, AMD MAKES NO WARRANTY WITH RESPECT TO THE DIE'S PROCESSING OF DATE DATA, AND SHALL HAVE NO LIABILITY FOR DAMAGES OF ANY KIND, UNDER EQUITY, LAW, OR ANY OTHER THEORY, DUE TO THE FAILURE OF SUCH DIE TO PROCESS ANY PARTICULAR DATA CONTAINING DATES, INCLUDING DATES IN AND AFTER THE YEAR 2000, WHETHER OR NOT AMD RECEIVED NOTICE OF THE POSSIBILITY OF SUCH DAMAGES.

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Buyer agrees that it will make no warranty representations to its customers which exceed those given by AMD to Buyer unless and until Buyer shall agree to indemnify AMD in writing for any claims which exceed AMD's warranty.

Die are not designed or authorized for use as components in life support appliances, devices or systems where malfunction of the Die can reasonably be expected to result in a personal injury. Buyer's use of Die for use in life support applications is at Buyer's own risk and Buyer agrees to fully indemnify AMD for any damages resulting in such use or sale.

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DRAFT REVISION SUMMARY

June 9, 1999

Initial Release.

August 5, 1999

Placed new die photo.

Inserted new die pad coordinates.

Updated the following sections: physical specifications, DC operating conditions, and manufacturing information.

November 9, 2009

Inserted die pad locations

Removed Industrial Temperature range and Extended Temperature range from Operating Temperature.

Colophon

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