

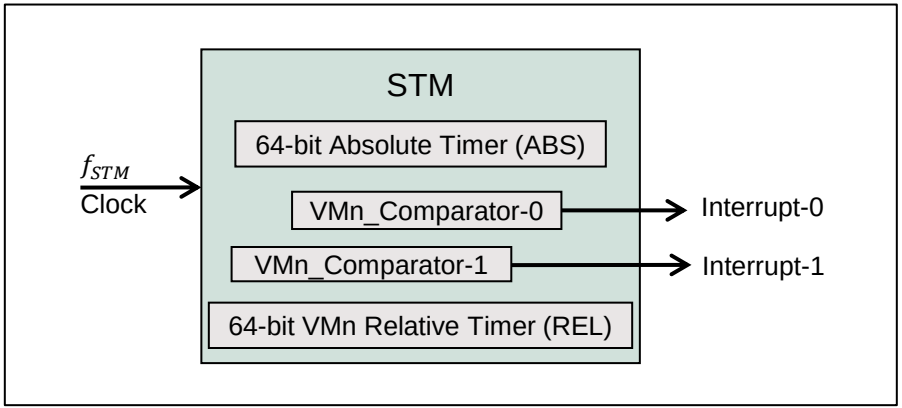
STM
System timer

AURIX™ TC4xx Microcontroller

V1.0.0 2024-09

Please read the Important Notice and Warnings at the end of this document

STM
System timer



Highlights

- The System Timer Module (STM) is used to generate a time base e.g. for an OS, as well as to generate trigger events
- There are as many STM modules as there are CPUs in the system. Thus each CPU can use one STM for its time base. STM is part of CPU
- Per Virtual Machine (VM) relative timer & interrupt generation. STM is completely virtualized

Key Features

Free-running 64-bit counter

Support for virtualization (8 REL Timers for 8 VMs)

Flexible interrupt service request generation

Customer Benefits

- Fits perfectly the generation of OS time base and triggering events and real-time requirements
- Global time and local time per VM
- Indication of events with assigned priority for highest flexibility

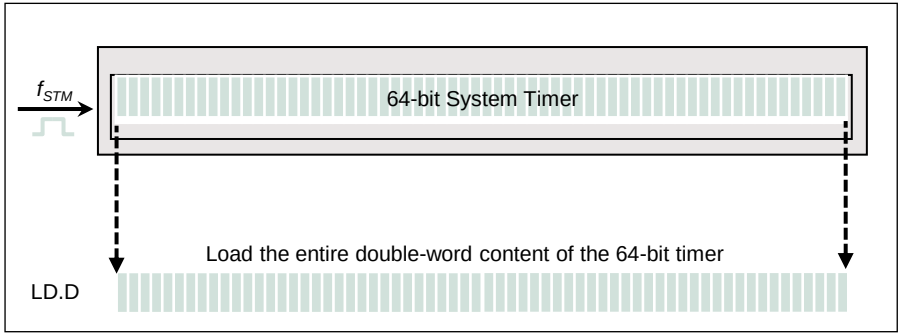
Copyright © Infineon Technologies AG 2024. All rights reserved.

STM
Reading the timers

The STM has a 64-bit counter is clocked by f_{STM} from the CCU (Clock Control Unit) in order to allow the timer to be consistent independently of the CPU frequency variation.

The entire 64-bit timer can only be read coherently using a 64-bit access (for example a TC1.8 LD.D instruction, or DMA single data transfer double word access). This avoids the need to have non-interruptible code if reading two component fields, which provides a performance benefit for real-time systems.

The STM can be optionally disabled for power-saving purposes, or suspended for debugging purposes. In suspend mode, the STM clock is stopped but all registers are still readable.



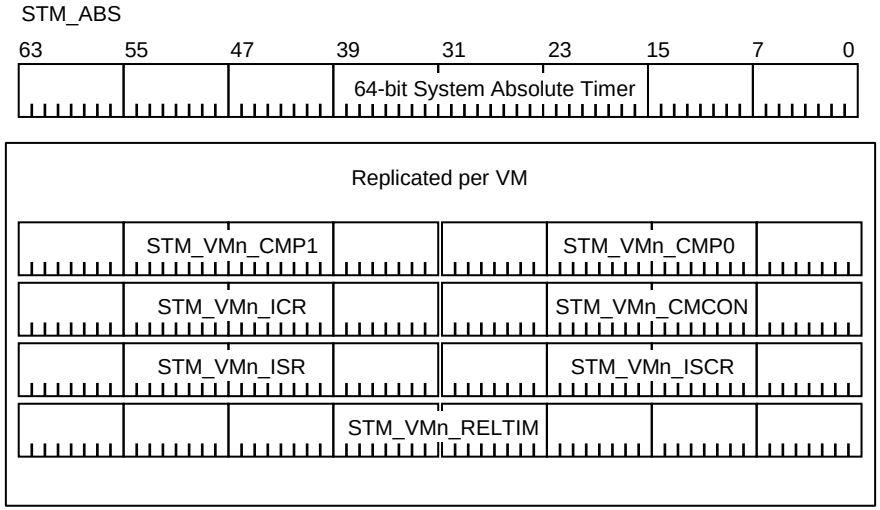
Copyright © Infineon Technologies AG 2024. All rights reserved.

STM
Support for virtualization

A 64-bit System Absolute Timer (STM_ABS) is aways active, regardeless if the VMs are active or not.

In addition to the 64-bit STM_ABS, a 64-bit relative timer (STM_VMn_RELTIM) is implemented per virtual machine, running from the same clock source.
This timer is active only when relative VM is active.
This timer holds the relative time value of the relative VM when it is not currently active.

Each virtual machine has 2 comparators (STM_VMn_CMP0, STM_VMn_CMP1) and its own set of Control and Interrupt configuration registers (STM_VMn_ICR/ISR/ISCR/CMCON) in order to ensure a flexible service request generation based on compare match with partial STM_ABS or STM_VMn_RELTIM field.



Copyright © Infineon Technologies AG 2024. All rights reserved.

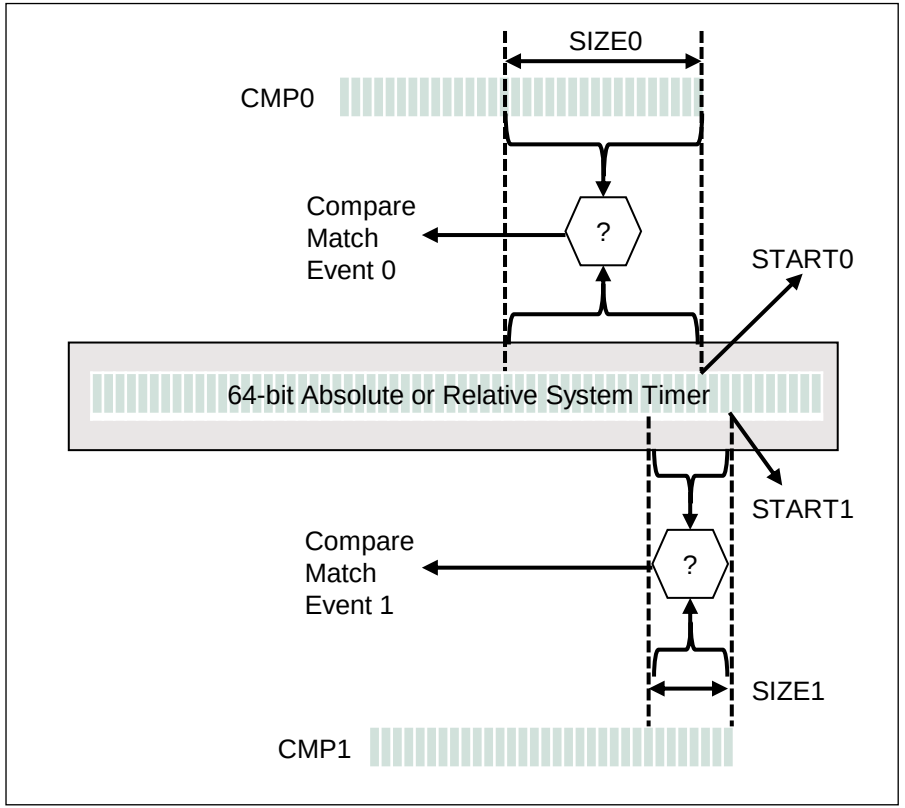
STM
Flexible interrupt service request generation

The STM counter can be compared against the values in two comparison registers (CMP0 or CMP1).
The comparison can be against the global timer or the relative timer per VM. The relative timer counts when the corresponding VM is in execution.
If the values match, a compare match event is generated from either of the comparisons.
Two parameters are programmable for the compare operations:

- START: First bit (LSB) location to be taken for the compare operation
- SIZE: Number of bits to be compared (starting from zero)

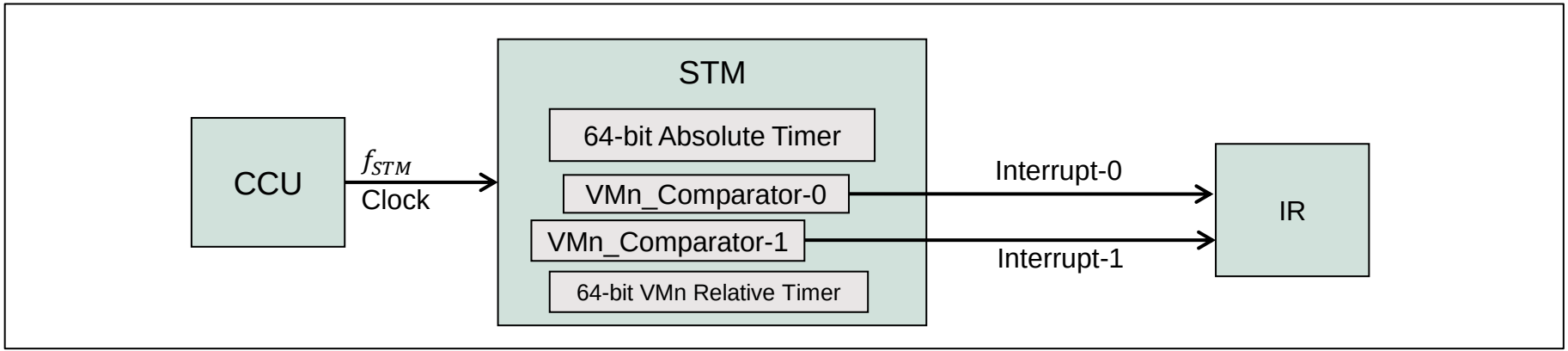
Using the START and SIZE configuration, it is even possible to check for single bit transitions (setting the size to 0 and the start to the bit of interest.
In the right side figure – the following parameters are assumed to be configured:

- SIZE0 = 17; START0 = 10 ;SIZE1 = 7; START1 = 7



Copyright © Infineon Technologies AG 2024. All rights reserved.

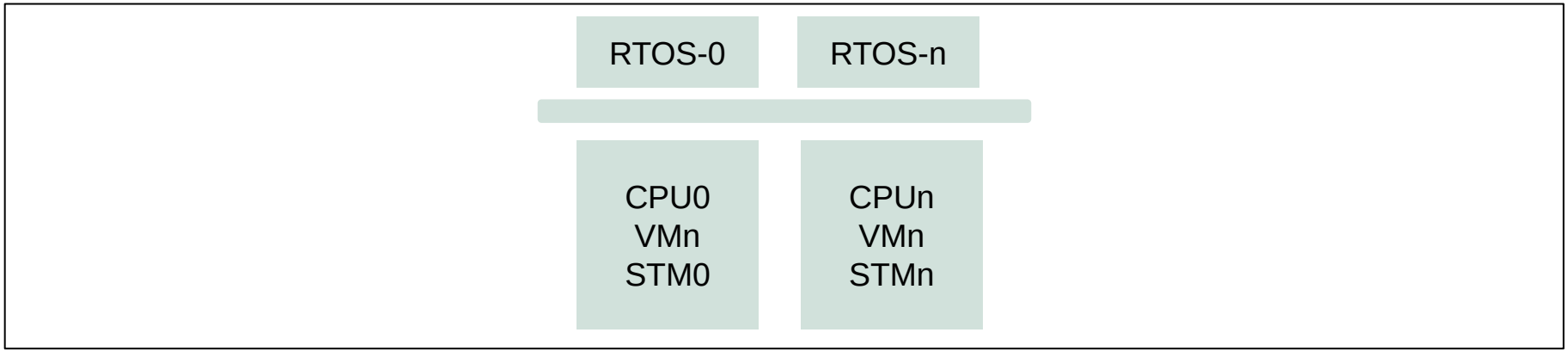
STM
System integration



- Clock to the STM (f_{STM}) is generated from the Control Clock Unit (CCU)
  - This is generated from the system PLL after it is enabled
  - The clock divider should be configured via CCU
- It must be ensured that the f_{STM} is on an integer to System Resource Interconnect (SRI) clock (f_{SRI})
  - If the integer ratio is not ensured, then the counter value can be wrong
- STM is connected to system reset (therefore it is not affected by CPU kernel reset functionality)

Copyright © Infineon Technologies AG 2024. All rights reserved.

Application example
Operating system time base generation



Overview

› STM can be used to generate the time base for a Real-Time Operating System (RTOS), for example as a base for the scheduler

Advantages

› Different rates of timer interrupt can be configured

› In a multicore system, each CPU can have its own time base

› In a virtualized system, each VM can have its own time base

Copyright © Infineon Technologies AG 2024. All rights reserved.

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2024-09
Published by
Infineon Technologies AG
81726 Munich, Germany

© 2024 Infineon Technologies AG.
All Rights Reserved.

Do you have a question about this document?
Email: erratum@infineon.com

Document reference
AURIX_3_System_ Timer

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie") .

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (www.infineon.com).

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.

Copyright © Infineon Technologies AG 2024. All rights reserved.


Infineon