

SDMA
System Direct Memory Access

AURIX™ TC4xx Microcontroller

V1.0.0 2024-09

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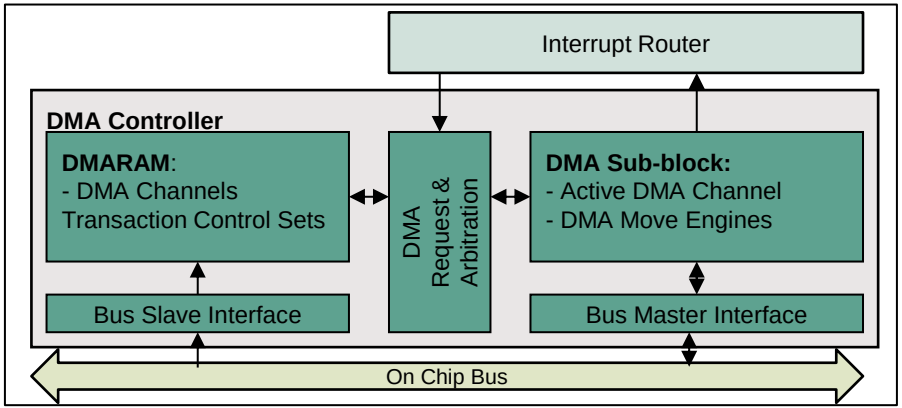
SDMA
System Direct Memory Access



Highlights

- The DMA moves data from source locations to destination locations without the intervention of the CPU or other on chip devices
- Two DMA instances are available
- Up to 192 individually programmable DMA channels
  - 128 channels DMA0 and 64 channels DMA1
- The DMA implements a lockstep mechanism using a redundant checker core for safety

Key Features

Flexible DMA channels requests

DMA double buffering

DMA linked list

Customer Benefits

- Possible configuration of the request type (SW, HW, Auto, ..) per DMA channel
- Transfer continuous data stream to two destination buffers
- Perform multi DMA transactions from noncontiguous memory regions

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SDMA
Flexible DMA channels requests

- The DMA Channel supports the following types of requests:
  - **DMA Software Request**: initiated by CPU
  - **DMA Hardware Request**: any peripheral that can trigger an interrupt can initiate a DMA transaction through the Interrupt Router
  - **DMA Daisy Chain Request**: DMA transaction initiated by the next higher priority DMA channel
  - **DMA Auto Start Request:** initiated by the loading of the next Transaction Control Set (TCS) during a DMA Linked List operation

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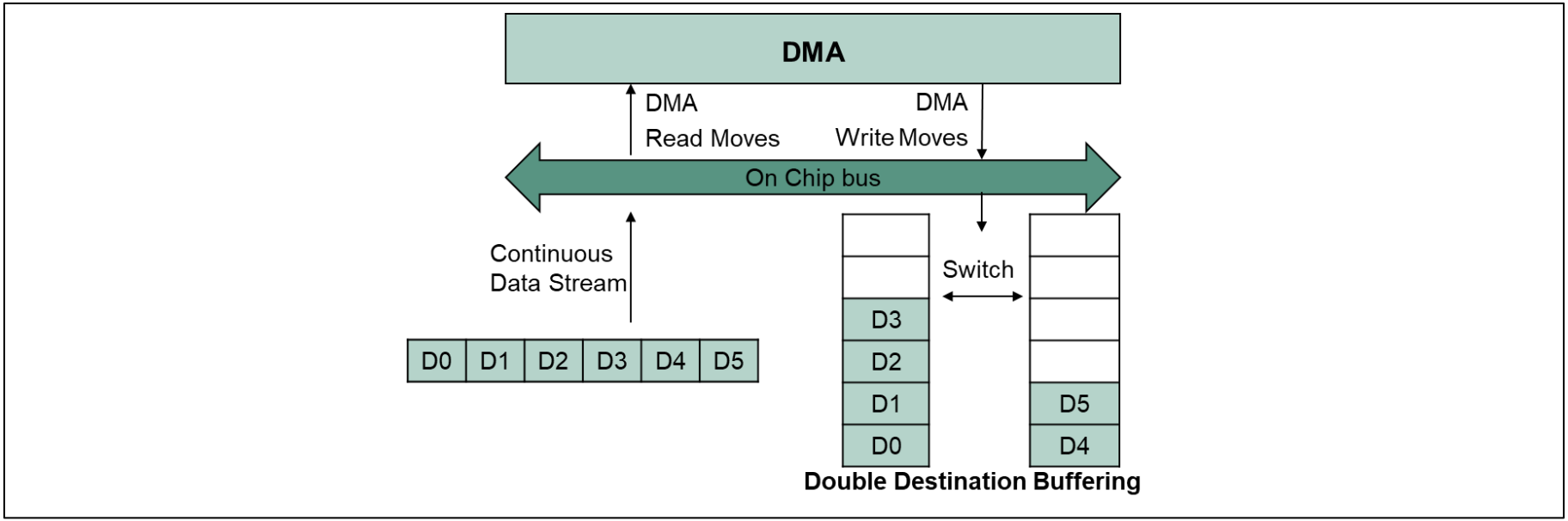
DMA double buffering

- Double buffering could be selected for source or destination buffering
- The application is able to freeze one of the destination buffers for cyclic software tasks while the other buffer continues to be filled



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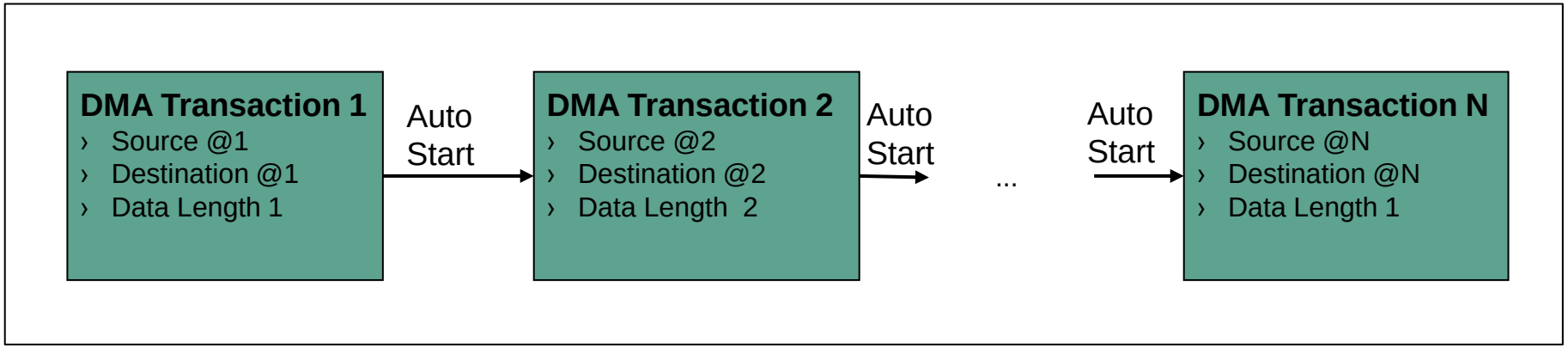
DMA linked list

- A linked list operation consists of a series of DMA transactions executed by **the same DMA channel**. Each DMA transaction has an unique configuration Set
- If the Auto start request is selected, a DMA transaction will be triggered after the end of the previous one in the list ➔ no HW or SW trigger is needed



- DMA linked lists are useful when user wants to transfer data from/to non contiguous memory locations using one DMA channel and/or one service request

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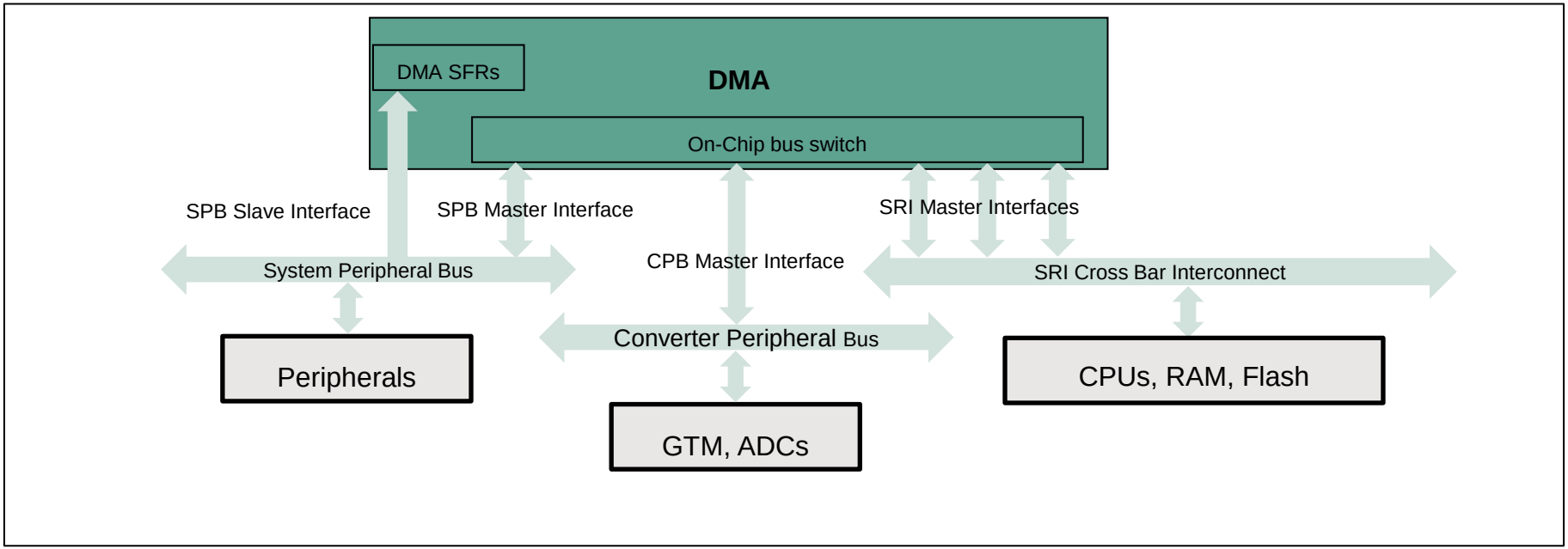
SDMA
System integration



- The DMA is connected to SRI, CPB and SPB with master interfaces
- This enables the DMA to read and write data from/to any module

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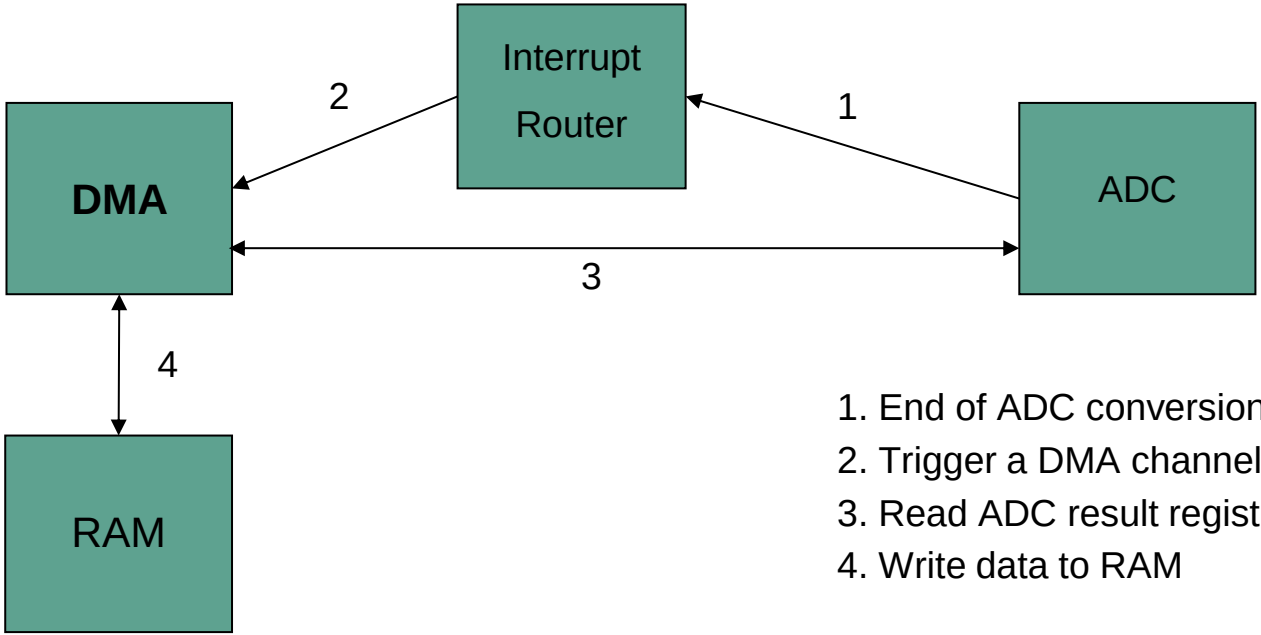
Application example
DMA hardware requests

› In this example, data is transferred from the ADC output registers to internal memory without any CPU intervention



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