

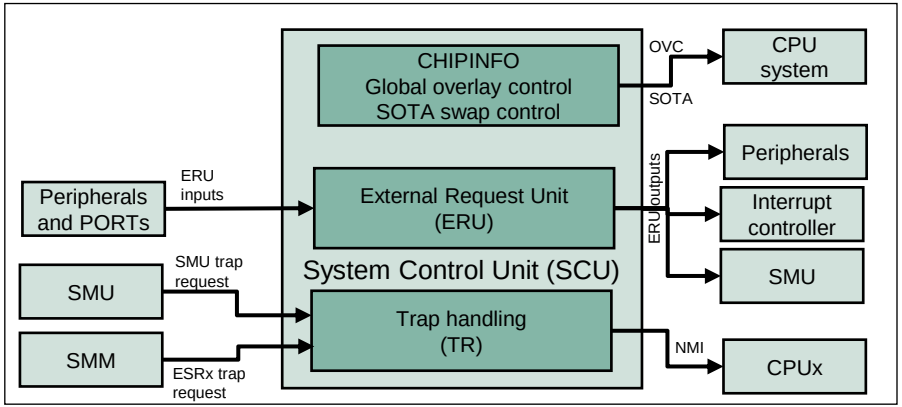
SCU
System Control Unit

AURIX™ TC4xx Microcontroller

V1.0.0 2024-09

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SCU
System Control Unit



Highlights

- SCU globally controls Non-Maskable Interrupt (NMI) trap handling, Data Access Overlay (OVC) and Software-Over-The-Air (SOTA) swap
- It also provides various system functions like the External Request Unit (ERU), basic chip-information (CHIPINFO)

Key Features

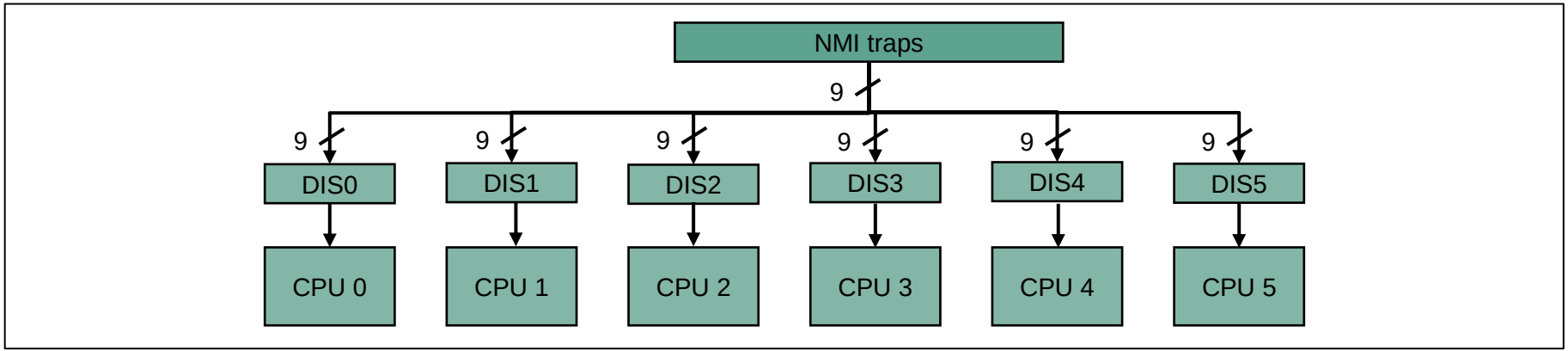
- Trap Generation
- External Request Unit (ERU)
- Global Overlay Controls (OVC)
- Miscellaneous System Control

Customer Benefits

- NMI trap can be served by any CPU(s)
- Triggers e.g. on GPIO can trigger internal events
- Enable or disable CPU(s) Data Access Overlay
- SOTA for remote software update, CHIPINFO for µC version info

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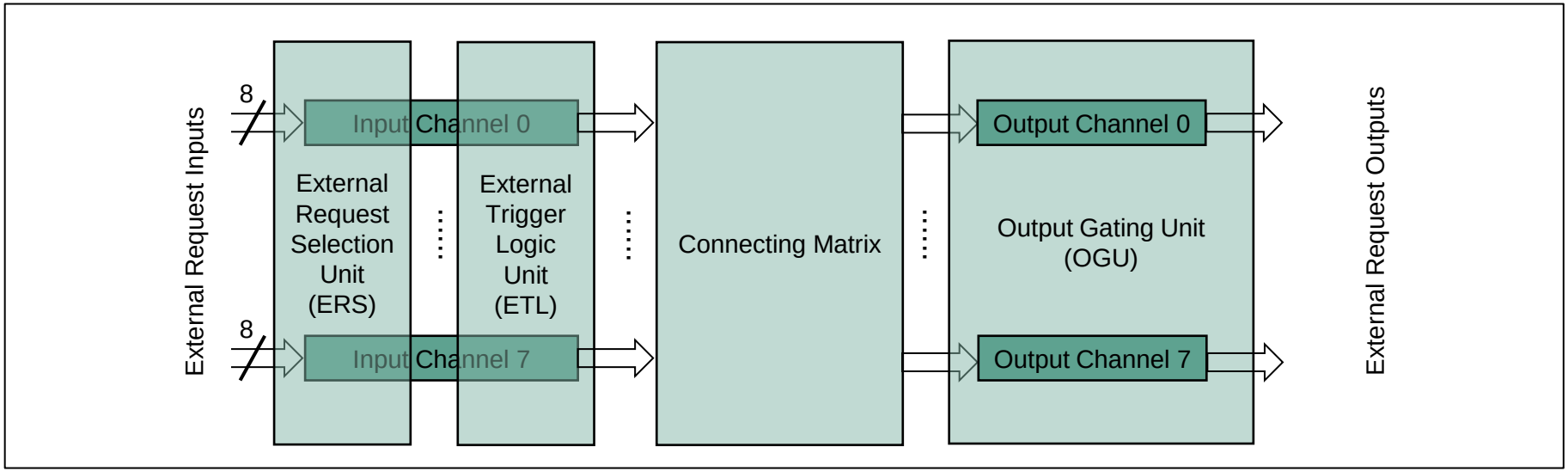
SCU
Trap Generation



- There are 9 NMI trap sources:
  - ESR0…2
  - NMI0…3 from Safety and security alarm Management Unit (SMU)
  - Software triggered NMI
  - SMU Trap from Cyber Security domain (SMUTCS)
- User shall decide which CPU(s) will react on which NMI trap(s) through the disable registers TRAPS_CPU_DISy (y=0...5)

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SCU
External Request Unit (ERU)



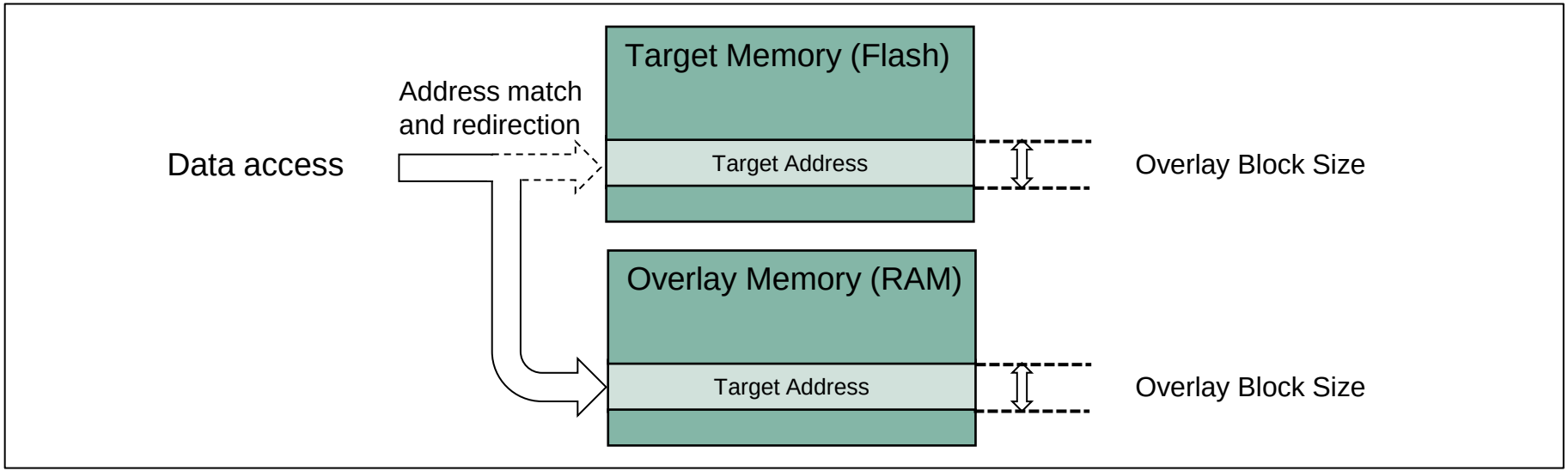
› This block diagram shows part of ERU

› Each Input Channel has 8 possible External Request Inputs. Each input (selected by ERS) can be either a GPIO or an internal signal

- ETL configures which events on Input Channel shall be captured
- Connecting Matrix routes events and status flags generated by the input channels to the output channels
- An OGU per output channel that combines the available trigger events and status information from the input channels. Output can be an interrupt or trigger to other modules

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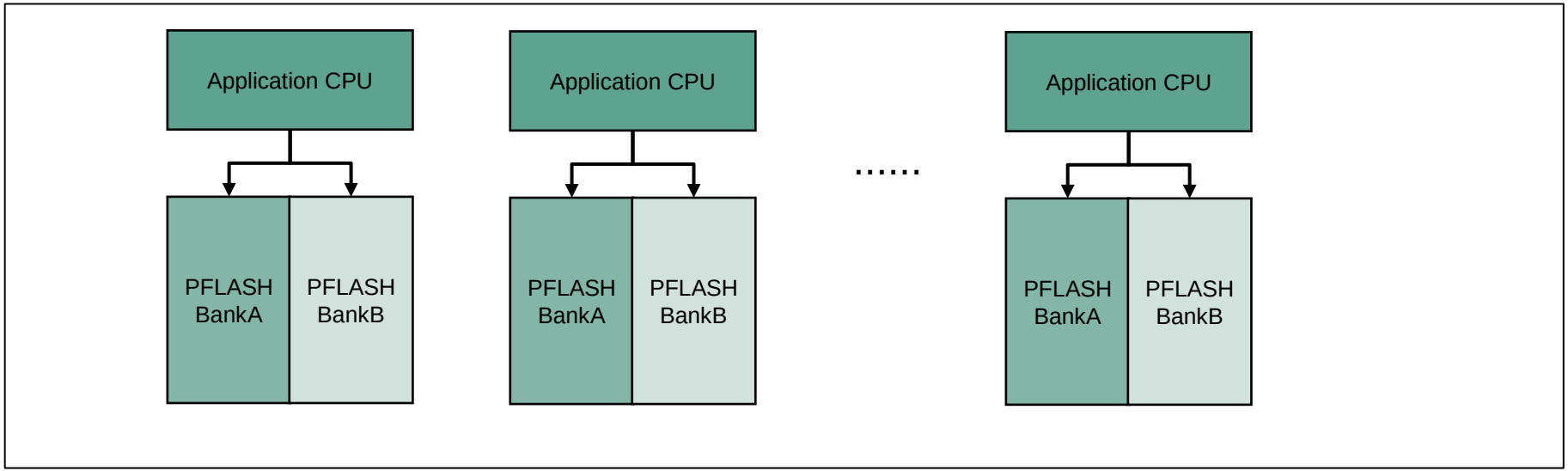
SCU
Global Overlay Controls (OVC)



- OVC redirects data accesses addressed to Program Flash and RAM. This feature is typically used in calibration
- SCU OVC globally controls the following features:
  - Register OVCENABLE globally enables or disables OVC for each CPU or all CPUs
  - Register OVCCON concurrently enables or disables selected overlay blocks for CPU(s). It can also invalidate data cache

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SCU
Miscellaneous System Control - SOTA



- The SOTA functionality can be enabled through configuration in the SOTA UCBs (User Configuration Block)
  - When SOTA is disabled, the MCU addresses the respective application PFLASH in the linear addressing mode
  - When SOTA is enabled, the MCU splits the respective application PFLASH into two address regions, one of which can be set as the active region
- Register SOTACTRL controls the currently used address region

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SCU
Miscellaneous System Control - CHIPINFO

CHIPINFO Offset address: $1A8_H$

Chip information register

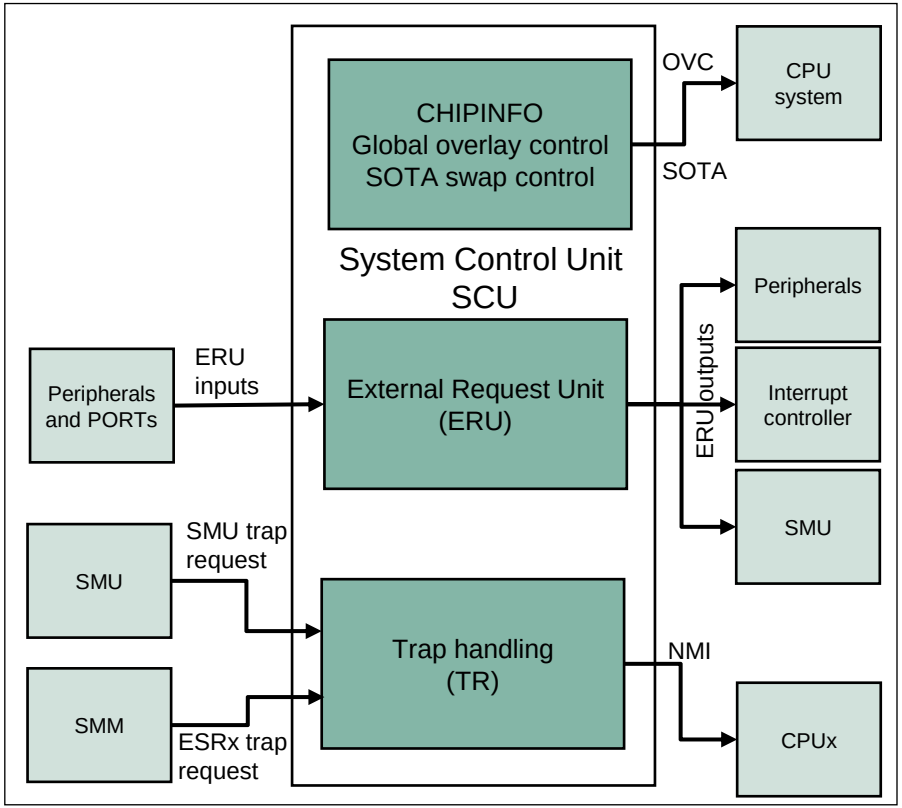
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								CHTEC		CHREV					
r								rh		rh					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MANUF											DEPT				
r											r				

- Register CHIPINFO is used to determine basic information about the device, it contains
  - Department within Infineon Technologies AG (for example Automotive), through the DEPT bit-field
  - The JEDEC normalized manufacturer code, through the MANUF bit-field (0xC1 = Infineon)
  - Revision number (A-step, B-step etc) of the AURIX™ TC4xx device, through the CHREV bit-field
  - Product family, through CHTEC bit-field (0x3 = TC4xx)

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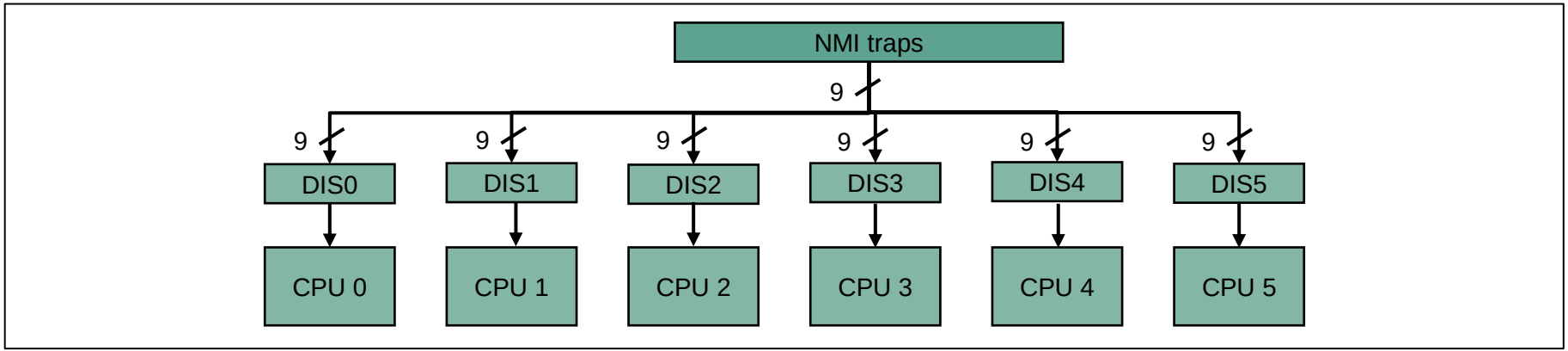
SCU
System integration



- SCU has interaction with many other modules
  - SCU registers can be accessed via SPB bus
  - Trap handling defines which CPU(s) shall service NMI traps triggered from software, SMU or SMM (System Mode Management)
  - ERU detects expected event pattern on GPIO or events from other peripherals, and generates interrupts or triggers to other peripherals and SMU
  - OVC, SOTA and CHIPINFO control memory access redirection, flash swap and device version information for CPU system

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Application example
Trap Generation



Overview

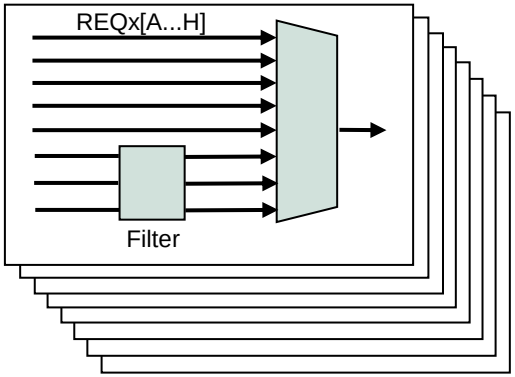
- SCU configures which CPU(s) shall service NMI traps
- SCU can also trigger NMI by software, which provides more flexibility

Advantages

- The user can decide for a certain NMI and which CPU(s) will service it. For example, typically it is not necessary to have all CPUs to responsd to the same NMI, because it will make all CPUs jump from intensive task to trap handler, which may cause unnecessary voltage overshoot due to sudden CPU offload
- Flexible NMI mapping also supports better software partitioning

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Application example
ERU



ERU pattern detection

Possible SCU ERU outputs (example)

SCU_IR_INT_SCUERU[7:0]	Out	ERU: Interrupts
SCU_SMU_ALM_SCUERU[7:0]	Out	ERU: Alarms
SCU_ADC_SCUERU[7:0]	Out	ERU: ADC outputs

Overview

- ERU detects expected event pattern from either GPIO or internal signals. For GPIO, ERU additionally provides filter possibility to prevent unexpected spikes
- Once detected, ERU will route a trigger or signal to other peripheral and SMU
- If necessary, more complicated event pattern (logic OR / AND) can also be supported

Advantages

- ERU provides more possibility to react on external events
- Typical use cases are when ADC may start conversion on the rising edge of the selected GPIO or an interrupt/safety alarm is triggered when the pre-configured event is captured

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Document reference
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