

PMS
Power Management System

AURIX™ TC4xx Microcontroller

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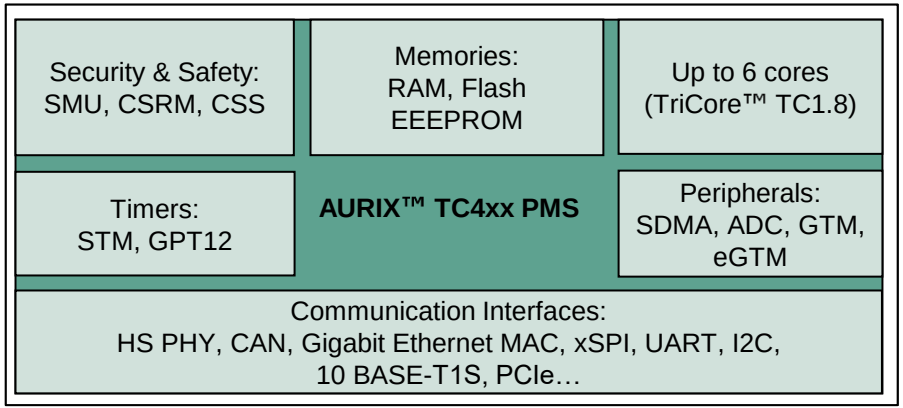
PMS
Power Management System



Highlights

- The Power Management System (PMS) ensures adequate power delivery to all modules, load transient management and interfaces to external regulators
- Input supply for core buck regulator (EVRC) up to 7 V

Key Features

Multiple core power modes and domains supported

Secondary voltage monitors

Separate port power domains for different modules

Customer Benefits

- Reduces the overall power consumption
- Voltage monitoring independent from the primary band-gap reference
- Minimize the noise interference from the digital core and pad domains

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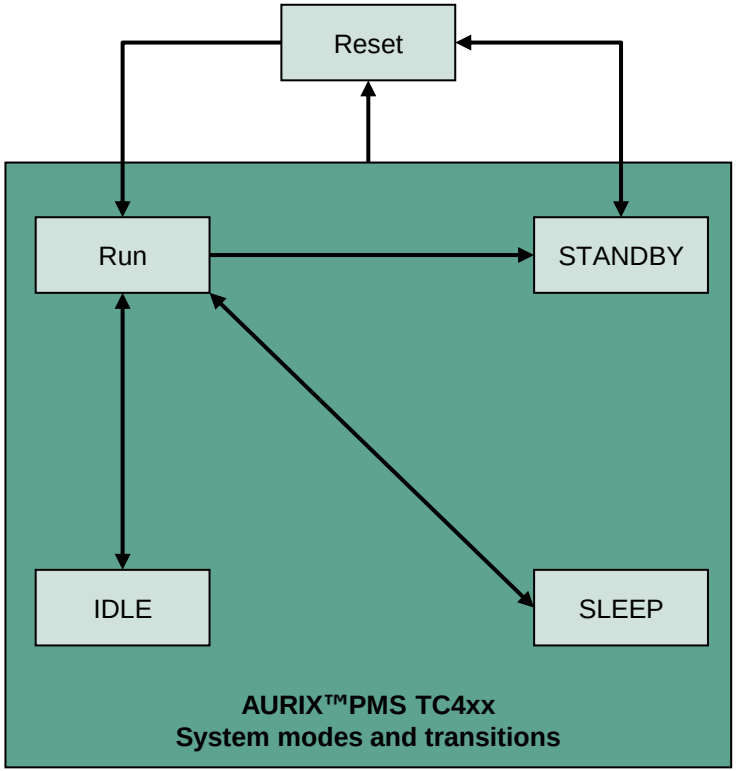
PMS
Multiple core power mode and domains supported

- The power management scheme allows activation of power down modes and domains so that the system operates with the minimum required power for the corresponding application state
- A progressive reduction in power consumption is achieved by invoking Idle, Sleep or Standby modes
- Run mode: it is considered to be the “normal functioning mode” where all CPUs, core power domains and peripherals can be active
- The IDLE mode is specific to each individual core (CPU, PPU), while the Sleep and Standby modes influence the complete system. Processing units can be individually set into IDLE mode depending on the application needs. The cores can be woken by interrupts, watchdog or other wake-up sources
- Using SLEEP mode, an arbitrary selection of peripherals and processing units can be clock gated depending on the application needs. They can be woken up by interrupts, watchdog and other wake-up sources
- Using the STANDBY mode, the lowest power state can be reached. Standby RAM is kept supplied and only the Standby Controller (SCR), the Real-Time Clock (RTC) or the Watchdog Unit Timer (WUT) are kept active.



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PMS
Secondary voltage monitors

- Secondary over-voltage (OV) and under-voltage (UV) monitoring against programmable thresholds is provided for the supply rails
  - The secondary monitors are based on a secondary band-gap reference independent from the primary band-gap reference used by the embedded PMS voltage regulators
  - In case of a threshold violation, an SMU alarm event is generated (as configured by the SW) or an interrupt is triggered (if enabled by the SW)
  - In case both OV and UV thresholds are configured to the same value (or within a distance lower than the accuracy of the voltage monitors), then both OV and UV alarms could be triggered at the same time
  - The secondary voltage monitors have an individually configurable spike filtering function

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PMS
Separate port power domains for different modules

- Support of multiple core power domains for CPU, PPU, and LMU functional blocks to reduce overall power consumption for use cases where the modules are not required
- Separate ADC power domain supplied by VDDM/VSSM supply rails to ensure minimum noise interference from the digital core and pad domains (separate reference supply for ADC modules)
- Mixed IO support - Flexport (VDDFLEX) has separate dedicated supply pins and may be supplied with either 5 V or 3.3 V
- XTAL/Oscillator/PLL supply with separate supply and ground pins for minimal noise interference
- Separate port domain for standby controller and standby functions supplied by VDDEVRSB supply rail
- Separate port power domains for high speed communication interfaces
  - - SGMIIx and PCIe modules supplied by dedicated VDDPHPHYx and VDDPHYx supply rails
  - - NOR Flash interface or ethernet RGMII supplied by dedicated VDDHSIF supply rail
  - - Ethernet RMII/MII supplied by dedicated VDDFLEX supply rail

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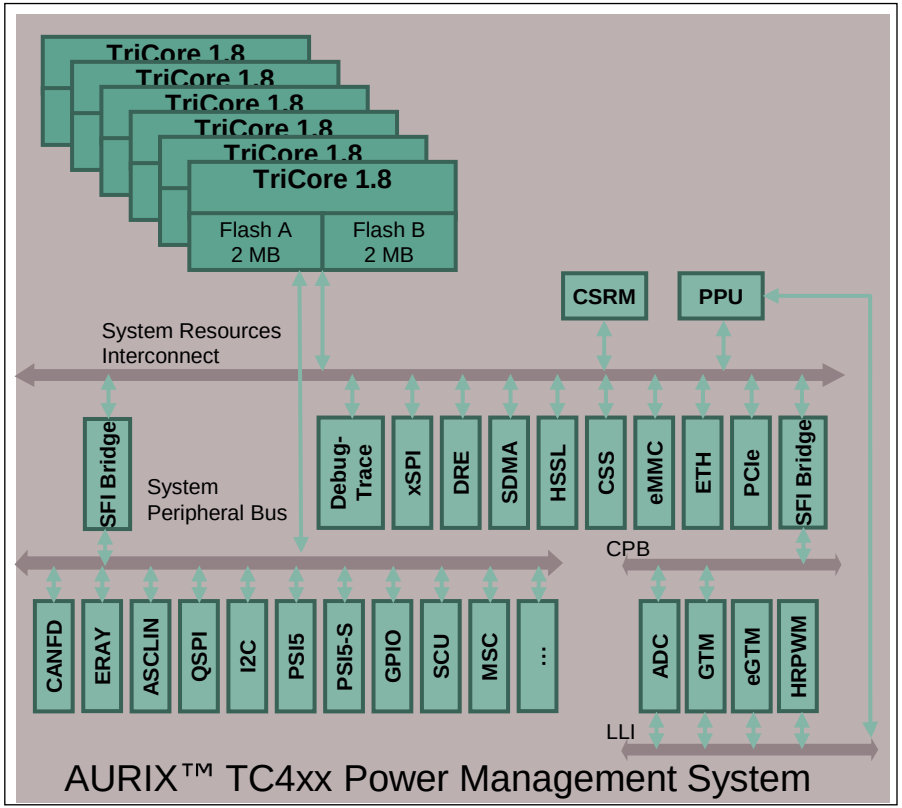
PMS
System integration



- The power management system is not a monolithic module, but more of an infrastructure that enables the control of power related sub-functions of all modules, power domains and voltage rails
- This infrastructure contains internal regulators for supply generation and supply voltage monitors in order to ensure the safe functionality of the power system
- For sensitive peripherals like ADC or high-speed communication, the PMS ensures separate power domains to reduce the noise interface
- Additionally, PMS allows the correct transitions between different power modes and domains
- In case of a misbehavior, PMS can trigger an alarm in the Safety Management System

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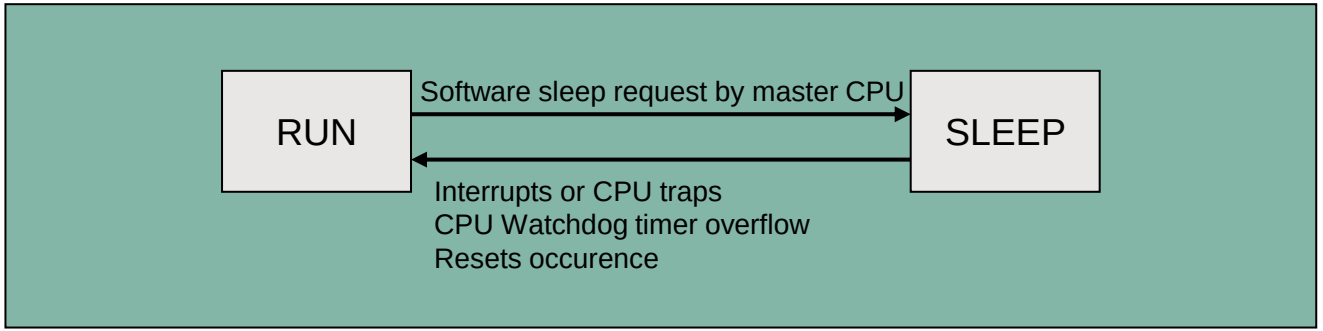
Application example
Wake up from sleep mode



Overview

- SLEEPx Modes: All CPUs are in Idle mode and only a few selected peripherals are active to realize the wake-up functions
- When a software Sleep request is issued through register setting by the master CPU, CPU code execution is halted and CPU Idle state is entered. Peripherals are set into sleep state if so configured. Ports retain their earlier programmed state

Advantages

- Minimize dynamic power consumption due to gated clocks, idle CPUs and peripherals
- Sleep mode maybe used to cater to Pretended Networking or ECU Degradation requirements

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