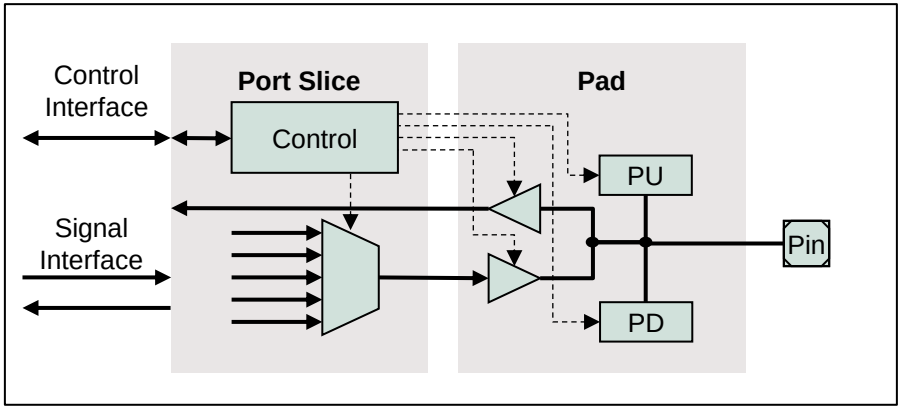


PORTS
Ports

AURIX™ TC4xx Microcontroller

V1.0.0 2024-09

Please read the Important Notice and Warnings at the end of this document



Highlights

- Digital input and output pins controlled by software or by peripherals
- Capable to drive 5 V, 3.3 V and 1.8V output level
- TTL or CMOS input hysteresis
- Pin toggle with one CPU instruction
- Increased alternate functions per pin

Key Features

- High configuration capabilities
- Improved access protection
- Port emergency stop

Customer Benefits

- Flexible adaption of pin characteristics to application needs e.g. EMC
- Protection against unintended modification of port configuration
- Well-defined and configurable pin states for critical situations

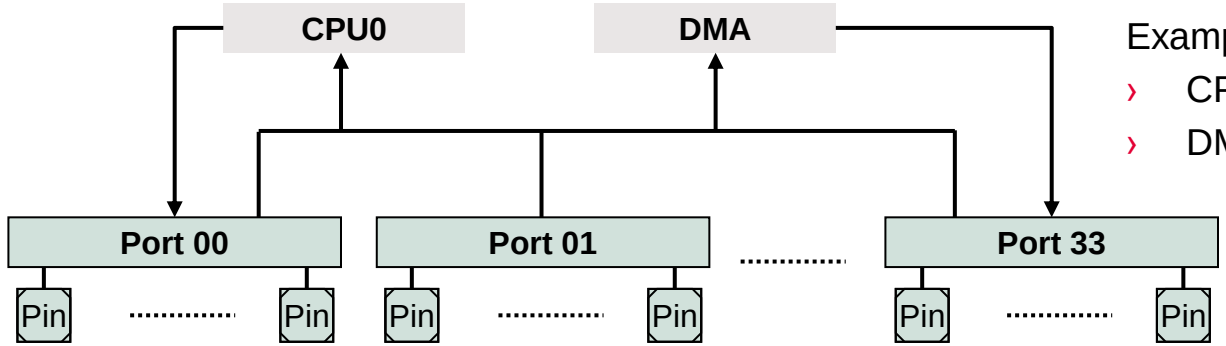
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PORTS
High configuration capabilities

- Each port pin can be configured and controlled by software for input or output operation (general-purpose mode) or can be assigned to one of the 15 alternative functions available
- The level of a pin can always be read by software independent of whether the port pin operates as input or output
- Configured as input:
  - an internal **pull-down** or **pull-up** device can be connected
  - the user can select between 3 different **input hysteresis**
- Configured as output:
  - **push-pull** mode or **open-drain** mode can be selected
  - up to 4 different **speed grades** are available to apply the optimal balance between speed needs and EMC behavior of the application

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PORTS
Improved access protection



Example:

› CPU0 can write to Port00 only

› DMA can write to Port33 only

› Unintended settings of port pins could cause serious and irreversible damages of the application hardware especially in high power applications

› To avoid unintended modifications of port pin configurations during operation, AURIX™ provides a write protection for ports

– The registers group of each port (e.g. P00, P01, P33, …) can be protected against write accesses

– Write accesses can be disabled separately for each bus master like e.g. CPUx, DMA, and HSSL

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PORTS
Improved access protection

- The AURIX™ TC4xx GPIO offers a grouped fashion protection concept, where each pin can be assigned to an access group

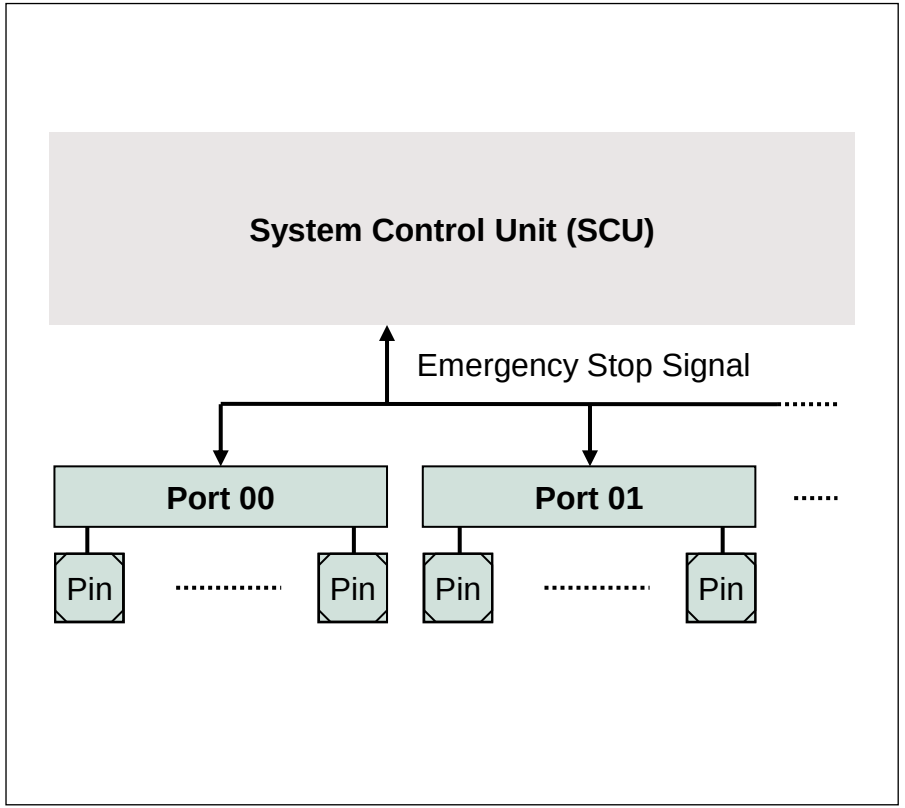
- These pins can only be accessed by their dedicated Master/Virtual Machines
  - Giving us the Freedom From Interreference
  - All the port slices i.e. pins (16 pins per port) can be grouped in max 8 access groups

- Therefore, unintended setting of the port pins through overwrite settings is avoided (e.g. CPU0 cannot overwrite the configuration of DMA)

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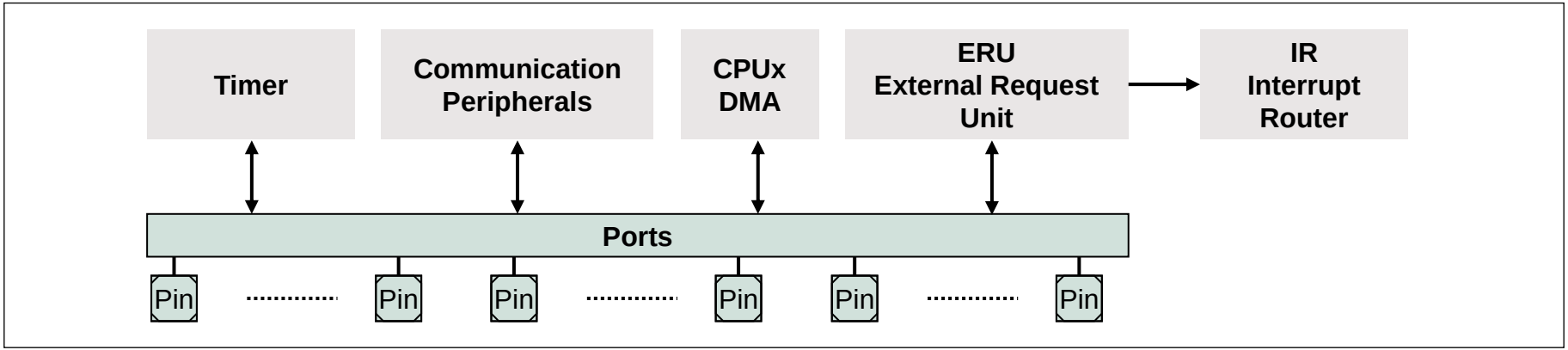
PORTS
Port emergency stop

- The emergency stop signal from the System Control Unit (SCU) forces port pins from output mode to general-purpose input mode
- Emergency stop logic can be individually enabled for each port pin
- Along with enabling/disabling functionality the register **PADCFG_SAFSEC** can achieve
  - Push-Pull level of the GPIO during emergency
  - Pad Configuration of the GPIO during emergency



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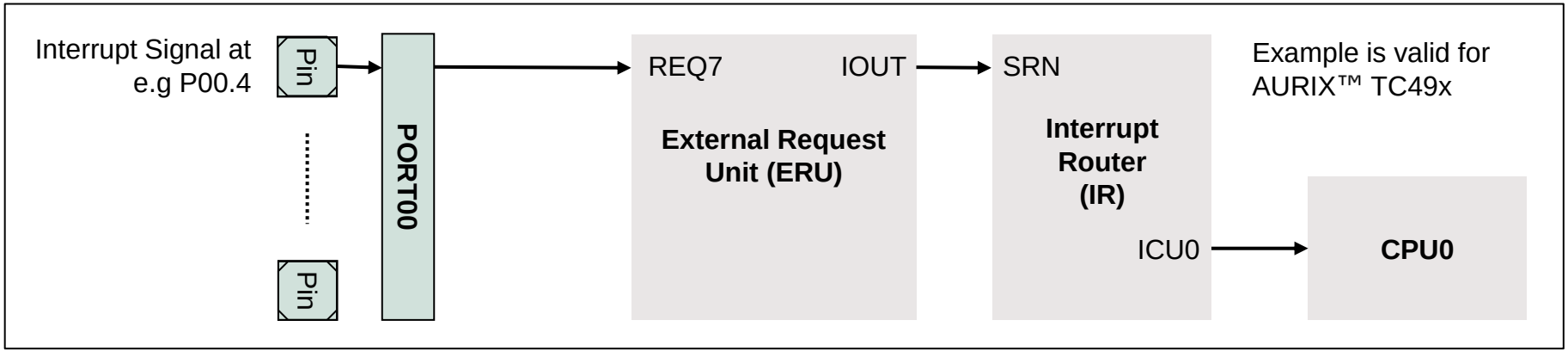
PORTS
System integration



- Almost all peripherals interact with the outside world through the port pins
- External interrupt signals (service requests) can be routed via the External Request Unit (ERU) to the Interrupt Router (IR)

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Application example
External interrupt



Overview

- The selected interrupt input pin P00.4 must be configured as an input (optional: open drain mode, pull-device activated)
- In the ERU, the input REQ7 must be selected and routed to an output

Advantages

- Several interrupt signals can be combined in the ERU and routed to one interrupt node
- Up to 16 possible external interrupt inputs per port

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Document reference
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