

PCIe
Peripheral Component Interconnect Express

AURIX™ TC4xx Microcontroller

V1.0.0 2024-09

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PCIe
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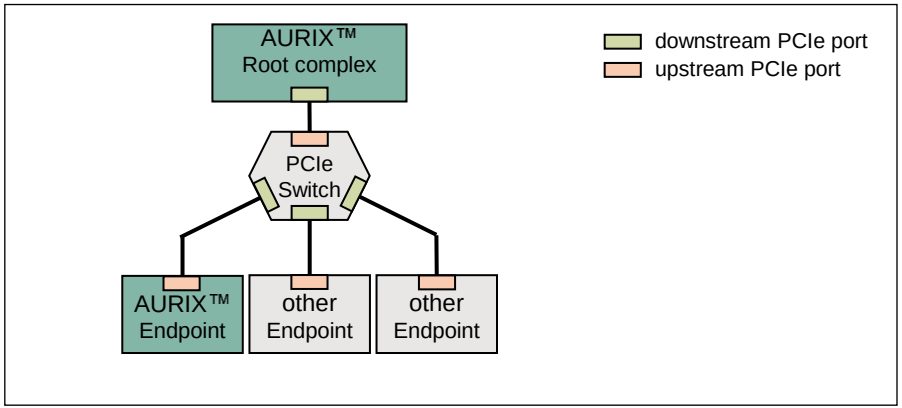

Highlights

- PCIe Express Gen3 (compliant to PCIe 3.1); 1 lane
- Available capabilities: AER, OBFF, PTM, ASPM, LTR
- End-to-end protection: ECRC
- All PCIe interrupt models supported:
  MSI, MSI-X and legacy; endpoints can receive interrupts
- Clocking architectures: Common RefClk, SRNS, SRIS
- Up to 256byte payload size

Key Features

Dual mode controller (root complex and endpoint)

Embedded DMA support (streaming)

Address translation unit for inbound/outbound traffic

Customer Benefits

- Flexible placement within PCIe topology and possible interconnect of two AURIX™
- Offload CPUs on both devices for efficient data bandwidth utilization and short latency use cases
- Memory mapped access to address map on remote device

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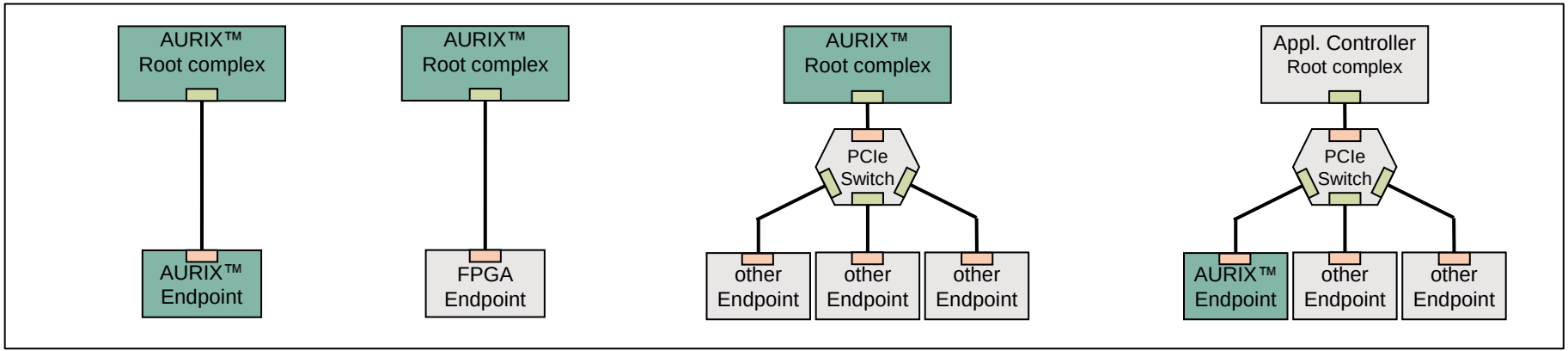
PCIe
Dual mode controller (root complex and endpoint)



- Because AURIX™ can act in endpoint and root-complex mode, two AURIX™ can seamlessly be integrated into a PCIe fabric, without the need for other PCIe components
- Dual mode controller implementation allows seamless AURIX™ integration into a variety of use case scenarios and PCI topologies

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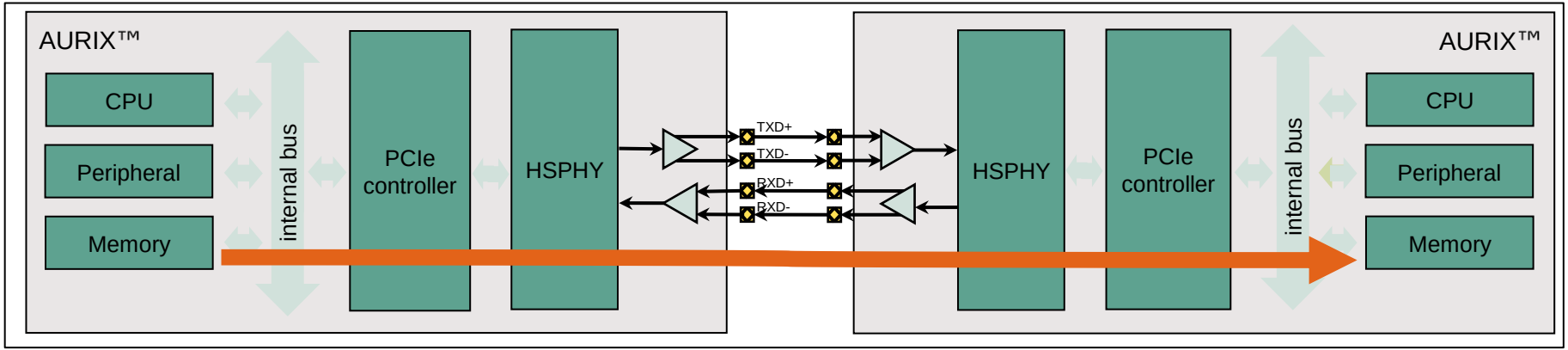
PCIe
Embedded DMA support (streaming)



- PCIe peripheral has an embedded DMA to autonomously execute data streaming from any memory location of the local device to any memory location on the remote device and vice versa
- Embedded DMA has 4 seperate channels in each streaming direction (read/write)
- Linked list mode allows, to efficiently move data from source to destination with minimal need for intervention from the local CPUx
- Embedded DMA can take full bandwidth advantage of PCIe peripheral. Up to 4 GB can be transferred at one time
- Endpoints allow setup and execution of DMA also from remote CPUx through the wire

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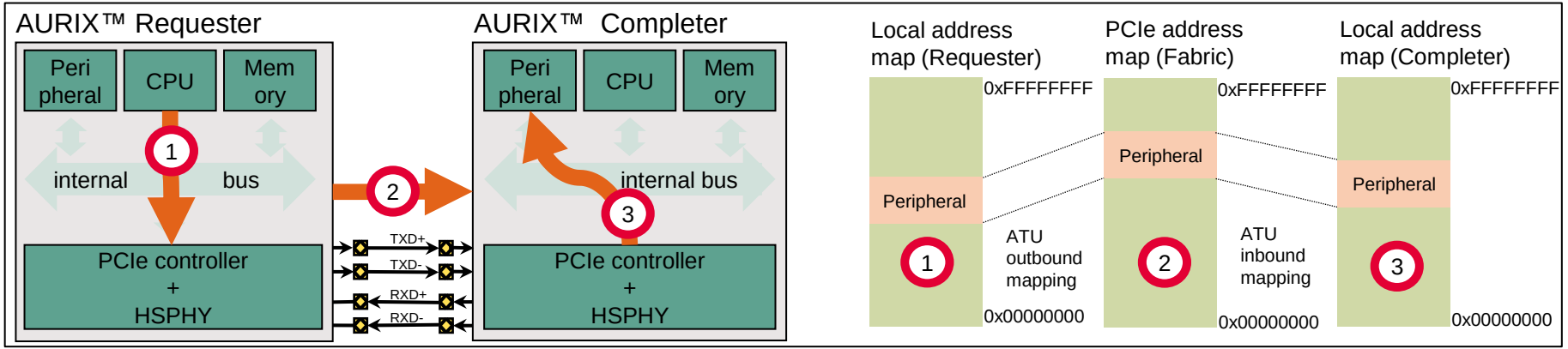
PCIe
Address translation for inbound/outbound traffic



- Address translation is provided in outbound and inbound direction
- CPUx accesses to the PCIe peripheral‘s 64 MB outbound window are translated into transactions on the fabric
- Inbound transactions arriving from fabric are mapped to the internal address map
- Eight independent ATU regions for outbound mapping and eight independent regions for inbound mapping
- Build-in PCIe transaction type conversion and attribute settings for outbound regions
- Filtering and mapping of inbound regions to BARs
- 32-bit or 64-bit address range supported on PCIe address map (fabric)

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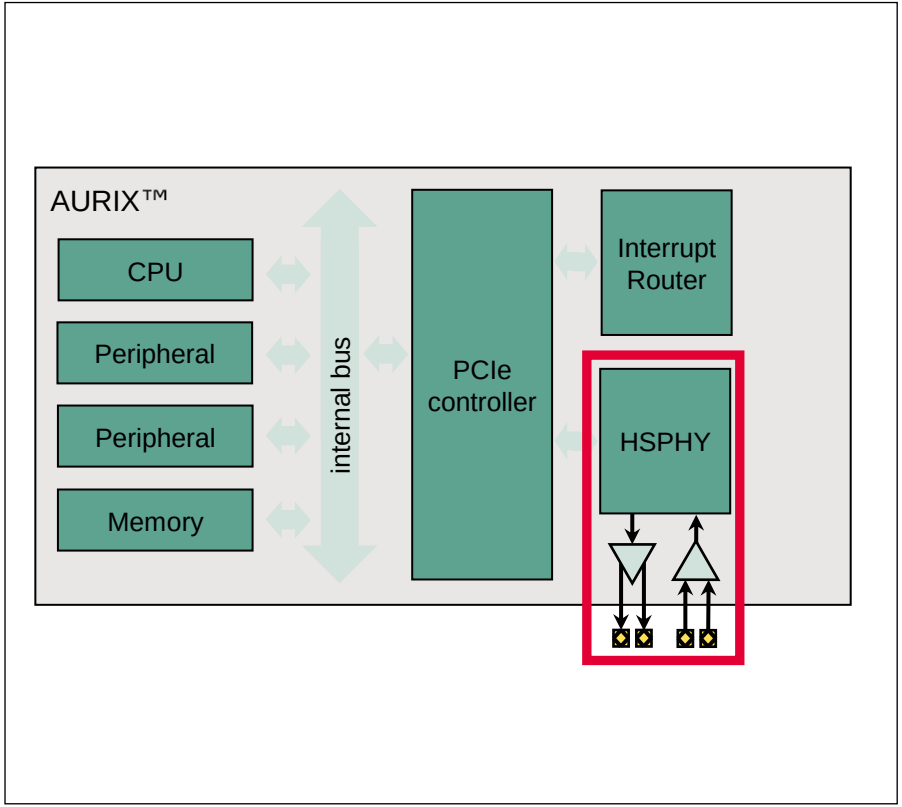
PCIe
System integration

- On HSPHY-peripheral, AURIX™ implements one PCIe lane which is compliant to PCIe 3.1 specification
- Communication flow and control between PCIe controller and HSPHY is based on so called PIPE interface
- Simple usage of HSPHY peripheral in context with PCIe: Once HSPHY peripheral is enabled for PCIe communication, PCIe controller hardware takes over the autonomous control of HSPHY through PIPE interface
- HSPHY peripheral is also used among other highspeed communication interfaces like GETH and XSPI



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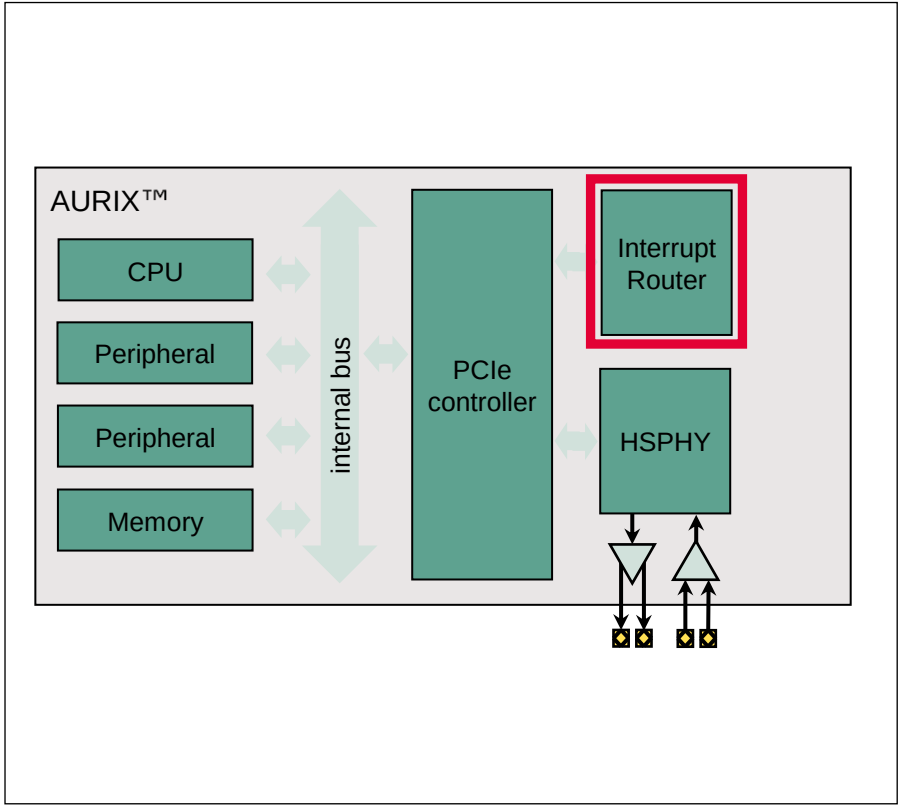
PCIe
System integration

- All standardized PCIe interrupt mechanisms are available inside AURIX™: Legacy, MSI and MSI-X
- Standard PCIe does not allow triggering of interrupts on endpoints.
  Still AURIX™ implements a proprietary method, which allows to trigger interrupts on endpoints similar to MSI, MSI-X
- While forwarding the interrupts to the interrupt router, the standardized PCIe interrupt mechanisms are narrowed down to max. 8 interrupts



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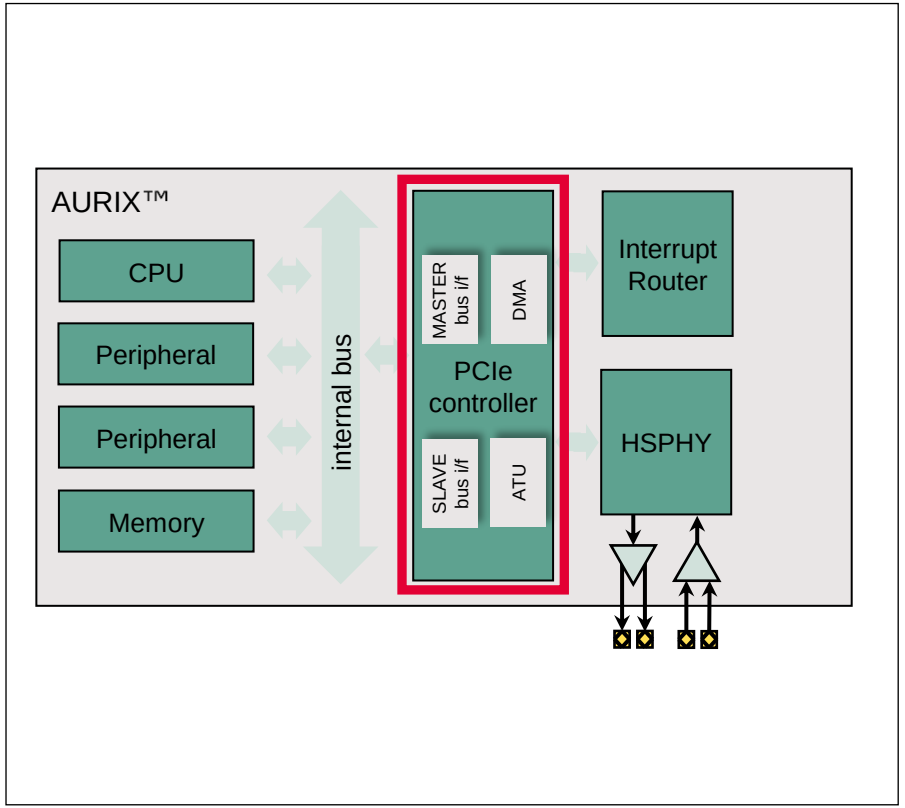
PCIe
System integration

- PCIe controller implements …
  - … PCIe protocol layers. PCIe controller supports PCIe up to Gen5. For AURIX™, utilization is limited to PCIe Gen3 by the integrated HSPHY
  - … an embedded DMA, for autonomous data transfers without necessary CPUx intervention (4 channels)
  - … an address translation unit (ATU), to map transaction layer packets from/to internal SRI transactions

- PCIe controller's internal bus slave i/f …
  - … allows CPUx to access the PCIe controller owned registers for setup and configuration by CPU
  - … provides access to 64 MB outbound window for bus masters (typically CPUx). Are translated to outbound transactions by the controller

- PCIe controller's internal bus master i/f …
  - … used to carry forward the completion of inbound transaction layer packets to the internal bus
  - … used to initiate transactions by the embedded DMA on the internal bus



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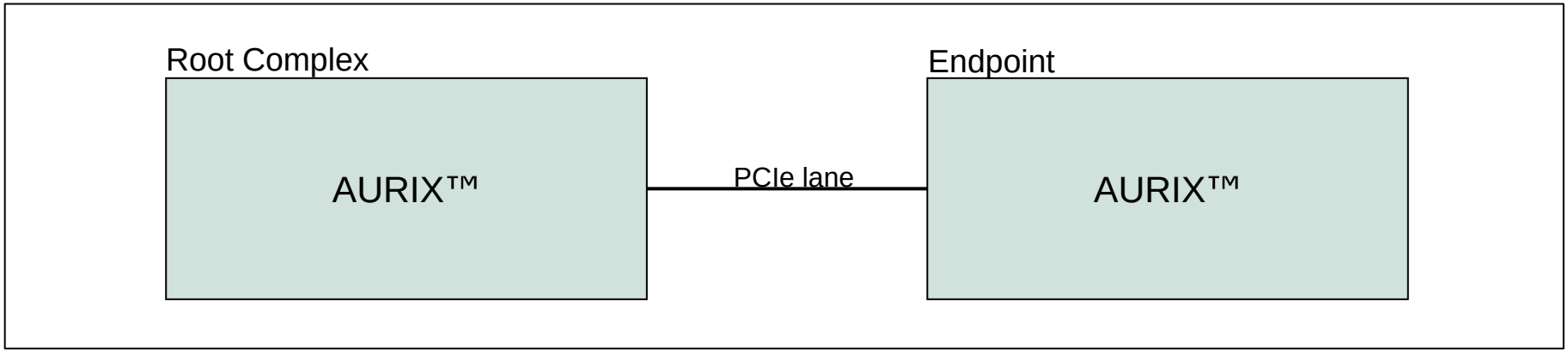
Application example
Integrate resources of two AURIX™ into one system



Overview

- Smoothly integrate two AURIX™ into one system, allowing both devices to have full control and flexibility in controlling the resources of each other

Advantages

- Enable safety applications with upscaled performance and functional extension, if the resources given by only one AURIX™ device do not meet the system requirements
- Both devices are mapped into each others address spaces

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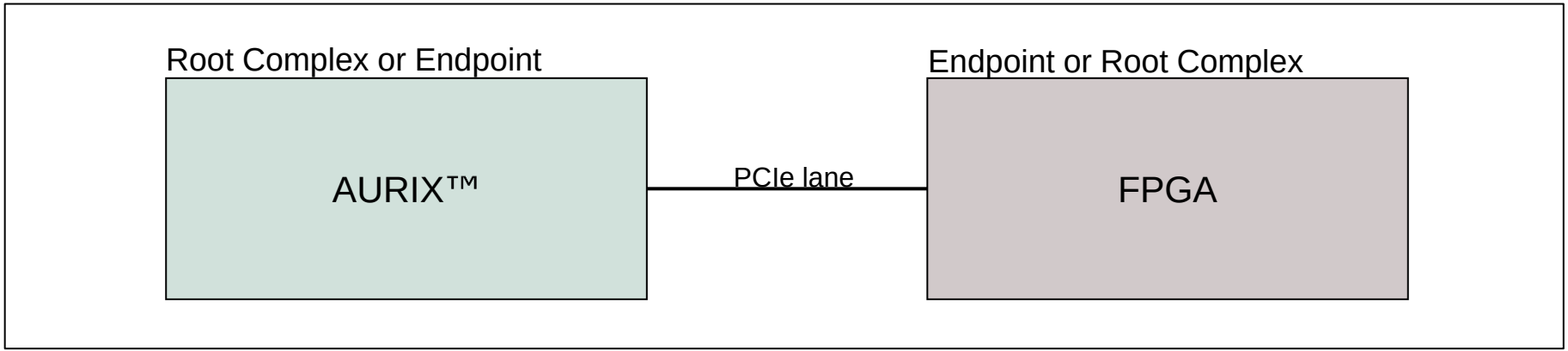
Application example
Integrate AURIX™ and FPGA into one system



Overview

- Smoothly integrate AURIX™ and FPGA into one system, allowing both systems to have full control and flexibility in controlling the resources of each other

Advantages

- Extend functional safety applications up to ASIL-D level provided by AURIX™ with the flexibility and feature set brought to the table by FPGA
- FPGA's modules are memory mapped into AURIX™ local address space and allows appliance, like they would sit on the local bus

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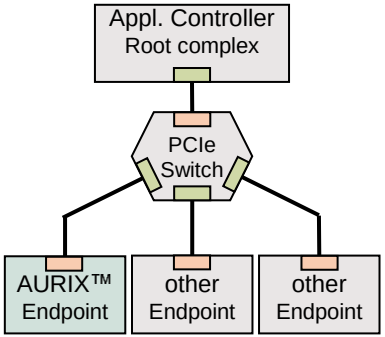
Application example
Integrate AURIX™ into a PCIe topology



Overview

› Smoothly integrate AURIX™ into a PCIe topology as an endpoint

Advantages

› Easy and simple integration of AURIX™ into an available PCIe topology (i.e. as safety companion)

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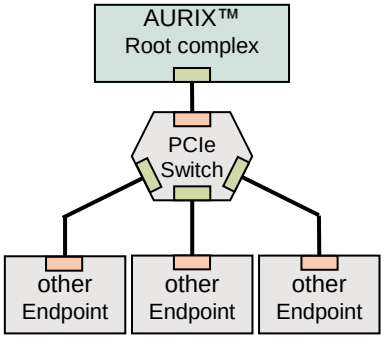
Application example
Build up a PCIe topology based on a root complex AURIX™



Overview

› Build up a PCIe topology based on AURIX™ operating in root complex mode

Advantages

› AURIX™ operating as a root complex and safety controller combo. AURIX™ configuring and monitoring the complete PCIe topology

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Document reference
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