

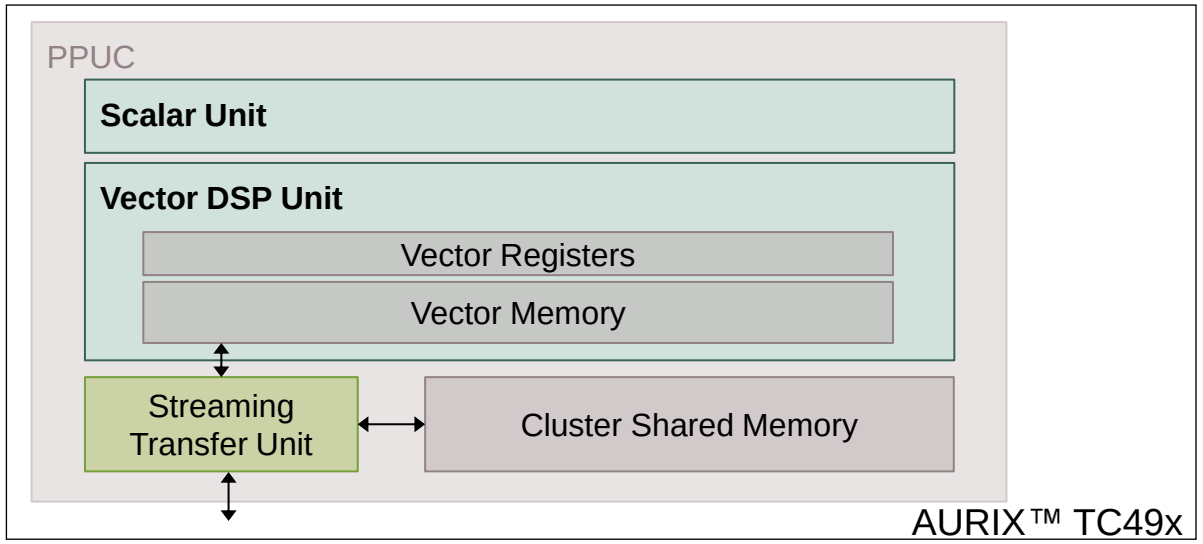
PPUC
Parallel Processing Unit Classic

AURIX™ TC4xx Microcontroller

V1.0.0 2024-09

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PPUC
Parallel Processing Unit Classic



Highlights

- Fully programmable parallel processing capabilities
- Several memory hierarchy levels with dedicated DMA engine

Key Features

Vector DSP Unit
Vector DSP multi-issue
Scalar Unit Double Precision support
Streaming Transfer Unit

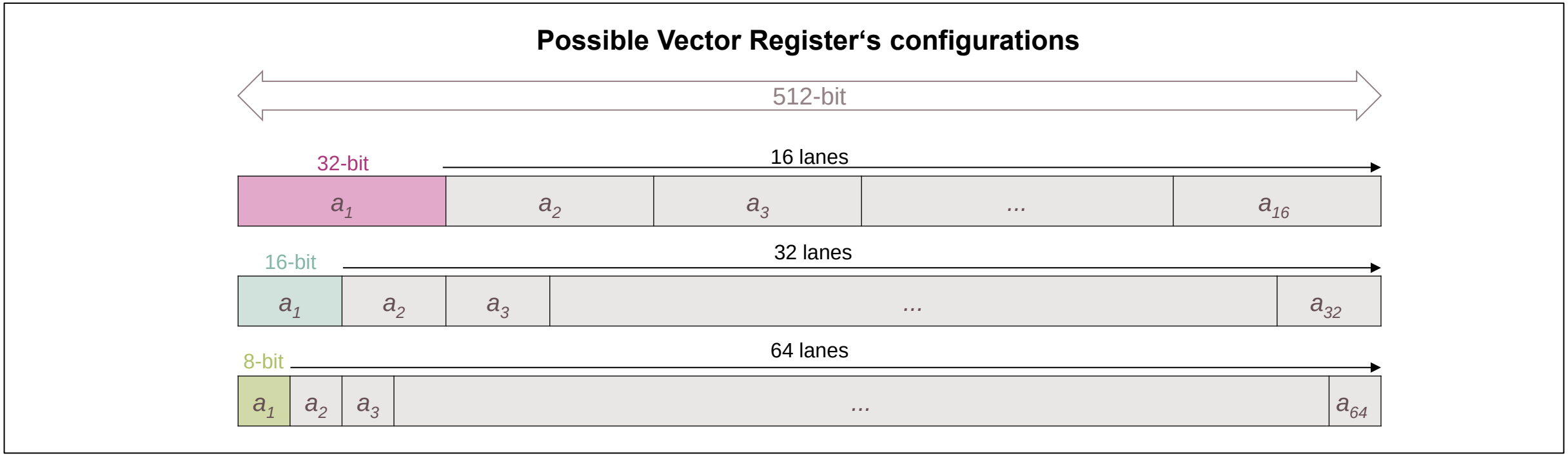
Customer Benefits

- Can process vector elements of data type 8-bit, 16-bit, or 32-bit
- Supports up to 3 concurrent vector instructions
- Supports 64-bit floating point operations
- Fast data transfers between system and PPUC internal memories

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Vector DSP Unit

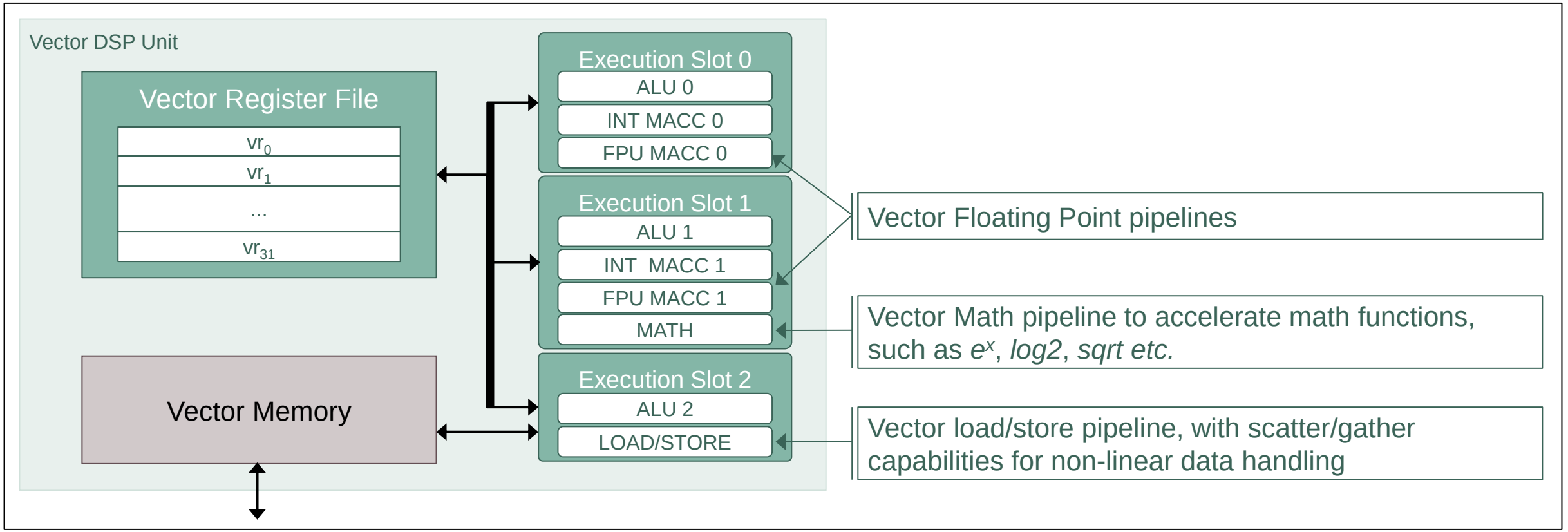
- The PPU has **32 instances** of 512-bit wide vector register
- The vector registers can be dynamically configured for different data types depending on the application‘s needs



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Vector DSP multi-issue

- The Vector DSP supports up **to 3 concurrent vector instructions** via the 3 Execution Slots
- Additionally to the vector instructions, **a scalar instruction can be concurrently issued in the Scalar Unit**



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Scalar Unit Double Precision support

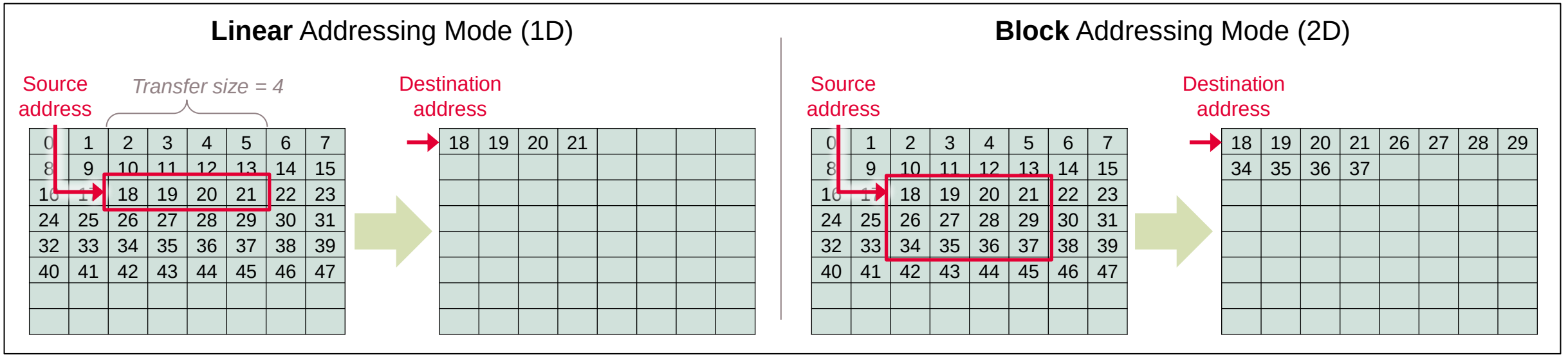
- The 32-bit Scalar Unit also supports:
  - 64-bit operands for selected instructions
  - 64-bit load/store

- The 32 general-purpose core registers can be paired for 64-bit support

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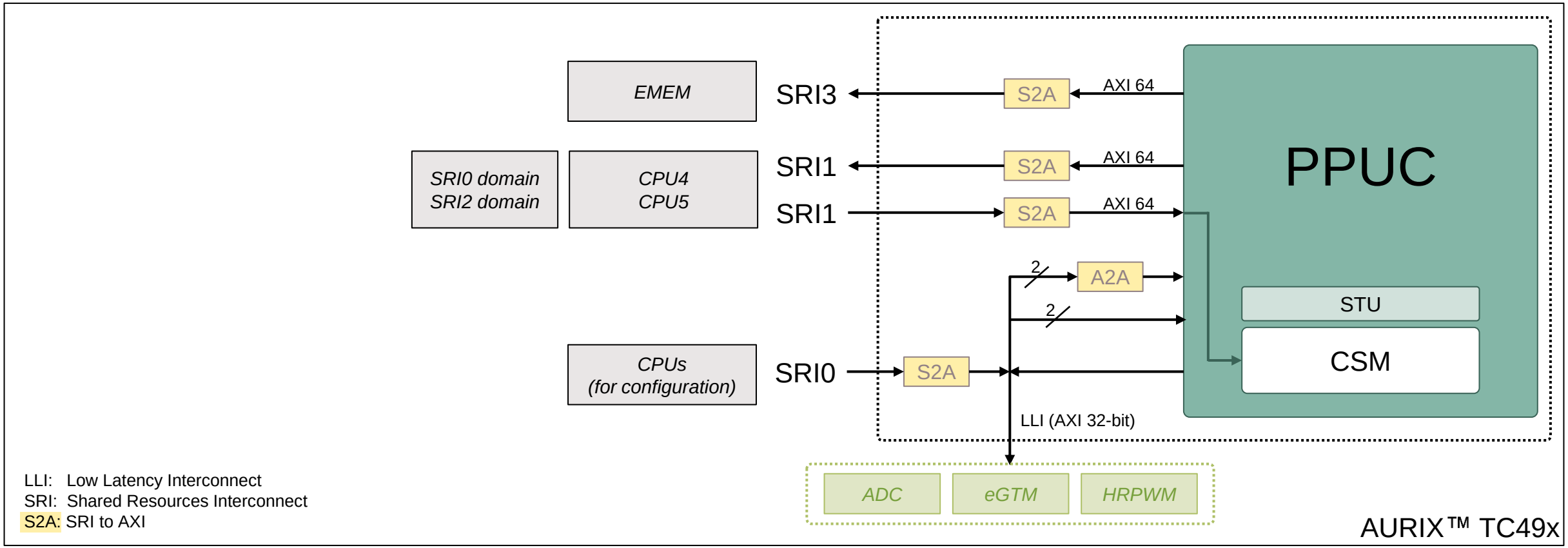
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Streaming Transfer Unit

- The **Streaming Transfer Unit** (STU) can be used for data transfers among the following available memories:
  - Vector Memory (VMEM)
  - Cluster Shared Memory (CSM)
  - External Memory outside of the PPUC functional block
- The STU can be accessed and **controled by the Scalar Unit or** by an **external master**
- The STU has **2 physical channels** to support data transfers in parallel
- Both **Linear and Block Addressing** modes are supported



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System integration



› The STU can directly access the EMEM via SRI3
› Low latency and deterministic behavior towards ADC & Timer through dedicated interconnect

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Application example
Matrix-Vector Multiply-Accumulate Operation

$$[a_0 \cdots a_{127}] \times \begin{bmatrix} b_{0\,0} & \cdots & b_{0\,127} \\ \vdots & \ddots & \vdots \\ b_{127\,0} & \cdots & b_{127\,127} \end{bmatrix} + [c_0 \cdots c_{127}]$$

Sizes		
[1x128] float32	[128x128] float32	[1x128] float32

Overview

› The PPUC enable optimized implementation for linear algebra-based algorithms

Advantages

› To execute the described operation, the PPUC requires **78 times fewer clock cycles** than the TriCore.

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Document reference
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