

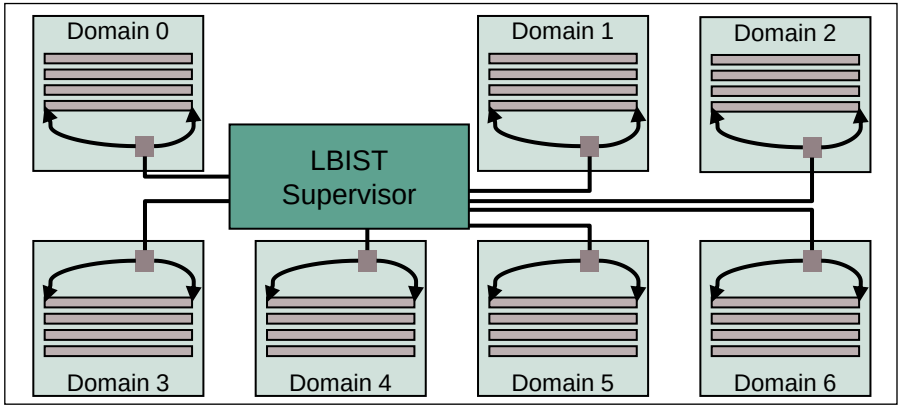
L-Test
Logic-Test

AURIX™ TC4xx Microcontroller

V1.0.0 2024-09

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L-Test
Logic-Test



Highlights

- The Logic-Test (L-Test) or Logic Built-In Self Test (LBIST) is an on-chip hardware mechanism used for detecting latent faults in the microcontroller
- The AURIX™ TC4xx implementation allows the execution of structural tests for safety mechanisms within 5-6 ms and fully automatic test of all digital logic within 50 ms

Key Features

Hierarchical scan domains

Two LBIST test scenarios

Customer Benefits

- Required test time is reduced
- Dedicated safety logic test and full logic test

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L-Test
Hierarchical scan domains

- Due to the device' complexity, the L-Test is divided into several hierarchical scan domains which enable independent scan-test and LBIST operation for multiple parts of the chip
- The domain's structure depends on the number and complexity of the domains and the LBIST runtime per each domain and, therefore, it varies from device to device
- Starting LBIST in any hierarchical domain brings the entire device automatically in scan mode during which no functional operation is possible
- After any LBIST execution, the system will trigger an LBIST reset and reboot automatically
- The execution status of each domain is available after the reboot of the device, and it can be compared against the golden signatures by application software

Hierarchical scan domain assignment to LBIST_CTRL_DOM

Domain #	LBIST_CTRL_DOM	Domain Name	Description
0	SEL0	SRI0	Compute domain 1 (CPU0, CPU1, CPU2)
1	SEL1	SRI5	Communication domain (LETH, MCAN, I2C, RGMII)
2	SEL2	SRI4_Conv	Cyber security CPU and Converter
3	SEL3	SRI2	High speed interfaces (XGETH, PCIE)
4	SEL4	SRI3_PPU	PPU
5	SEL5	PMS	Power management
6	SEL6	SRI1	Compute domain 2 (CPU3, CPU4, CPU5, LMU)
7	SEL7	unused	

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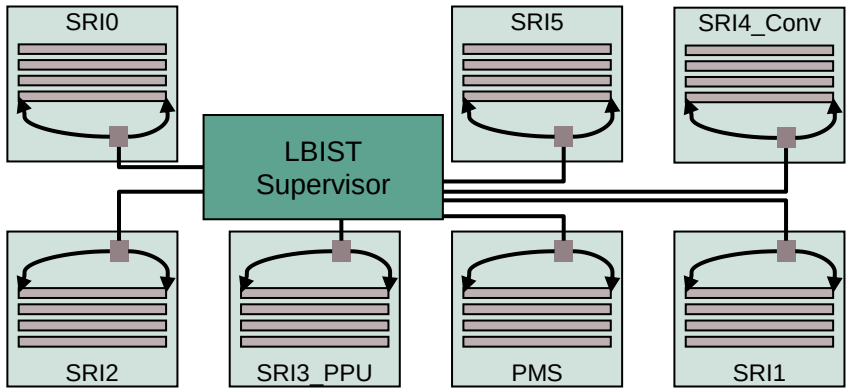
L-Test
Two LBIST test scenarios with configurable patterns

- Two LBIST test scenarios are available, and they are called Key-on and Key-off LBIST
- Key-on LBIST is targeting only the stuck-at faults of the on chip functional safety logic within each hierarchical domain:
  - It can be executed automatically during the boot sequence using the default firmware configuration
  - Only the safety-relevant flip-flops (~8-10%) within any domain are tested
  - The target stuck-at coverage is 90% with an execution time of 5-6 ms
  - Multiple domains can be tested in parallel due to the reduced toggle rate
- Key-off LBIST is targeting the stuck-at faults of all logic within each hierarchical domain:
  - It can be started for one or multiple hierarchical domains by user software during application run-time
  - All flip-flops are tested, therefore in the case of multiple domains testing the tests are performed sequentially
  - The target stuck-at coverage is 90% with an execution time of 50 ms

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L-Test
System integration

- The L-Test module is not a monolithic block, but more of structure divided over the different domains of the microcontroller such as:
  - Compute domain 1: CPU0, CPU1, CPU2
  - Communication domain(LETH, MCAN, I2C, RGMII)
  - Cyber security CPU and Converter
  - High speed interfaces (XGETH, PCIE)
  - PPU
  - Power management
  - Compute domain 2: CPU3, CPU4, CPU5, LMU
- The domains' structures are device dependent; the above example is valid for AURIX™ TC4Dx
- The LBIST supervisor is summarizing the execution status of the test and makes it available after reboot for each domain in order to be compared to the golden signatures by the application software



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0	SEL0	SRI0	Compute domain 1 (CPU0, CPU1, CPU2)
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2	SEL2	SRI4_Conv	Cyber security CPU and Converter
3	SEL3	SRI2	High speed interfaces (XGETH, PCIE)
4	SEL4	SRI3_PPU	PPU
5	SEL5	PMS	Power management
6	SEL6	SRI1	Compute domain 2 (CPU3, CPU4, CPU5, LMU)
7	SEL7	unused	

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Application example
Parallel „key-on“ safety stuck-at LBIST

Domain name	Expected key on LBIST run time [ms]
SRI0	~5.9
SRI5	~5.8
SRI4_Conv	~4.7
SRI2	~5.3
SRI3_PPU	~4.7
PMS	~4.7
SRI1	~5.7

Overview

- Check of the on-chip primary safety mechanism structures for a fault free behavior
- This LBIST operation mode involves only the logical structure of such safety mechanism logic into the test process

Advantages

- This type of LBIST test consumes significantly less power
- Due to the reduced power consumption, these tests can be done in parallel, therefore reducing the execution time
- 90% stuck-at test coverage within 5-6 ms

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