

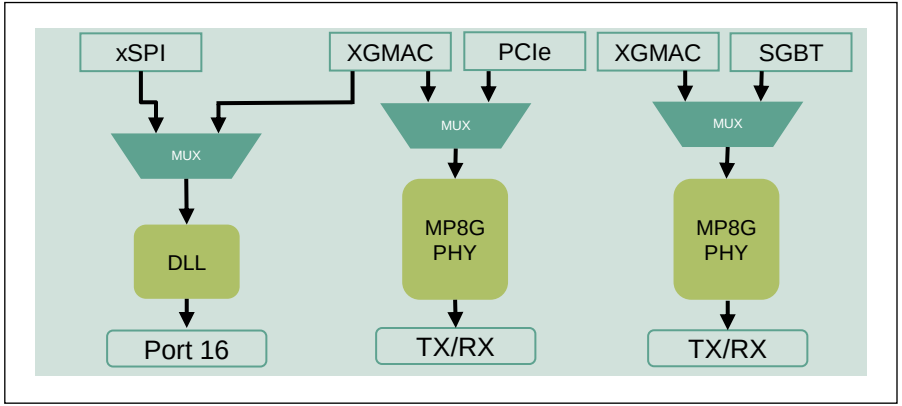
HSPHY
High Speed Physical Layer

AURIX™ TC4xx Microcontroller

V1.0.0 2024-09

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HSPHY
High Speed Physical Layer



Highlights

- Gigabit Ethernet communication via SerialGMII, USXGMII or RGMII
- PCI Express Gen 3 speeds up to 8 Gb/s
- Serial Gigabit Trace (SGBT) interface supports 1, 2.5 and 5 Gbps data rates
- Communication via xSPI interface up to 400 Mbps with a skew control of up to 138,88 ps

Key Features

Configurable serial line rate

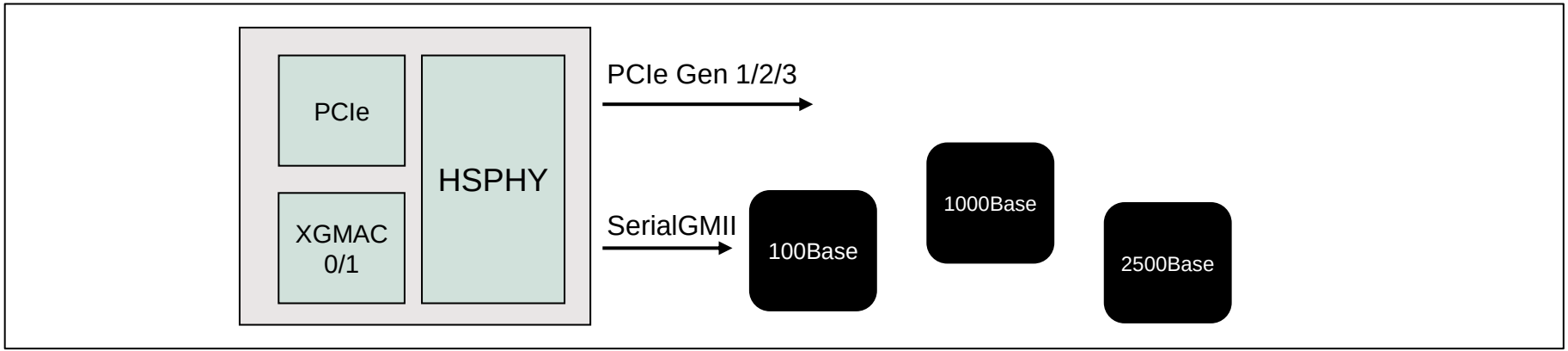
Skew generation for DDR interfaces

Customer Benefits

- Realizing high speed connection at minimum pin usage, differential signals improve power and electrical emission
- Adaptable signal skews allow optimization of PCB designs

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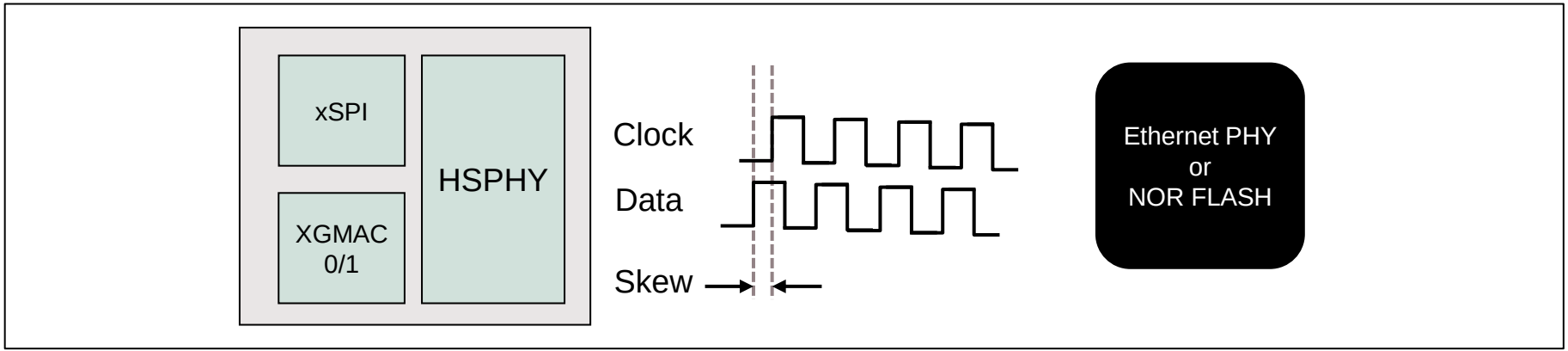
HSPHY
Configurable serial line rate



- Allows Configurable serial line rate from 0.125 till 8 Gb/s for multiple interfaces such as Ethernet and PCIe
- Ethernet interface options
  - RGMII for 10/100/1000 Mb/s connections
  - SerialGMII for 100/1000/2500/5000 Mb/s connections
- PCIe supporting all modes up to Gen3 8Gb/s connections
- Serial Gigabit Trace (SGBT) interface Supports 1, 2.5 and 5 Gbps data rates

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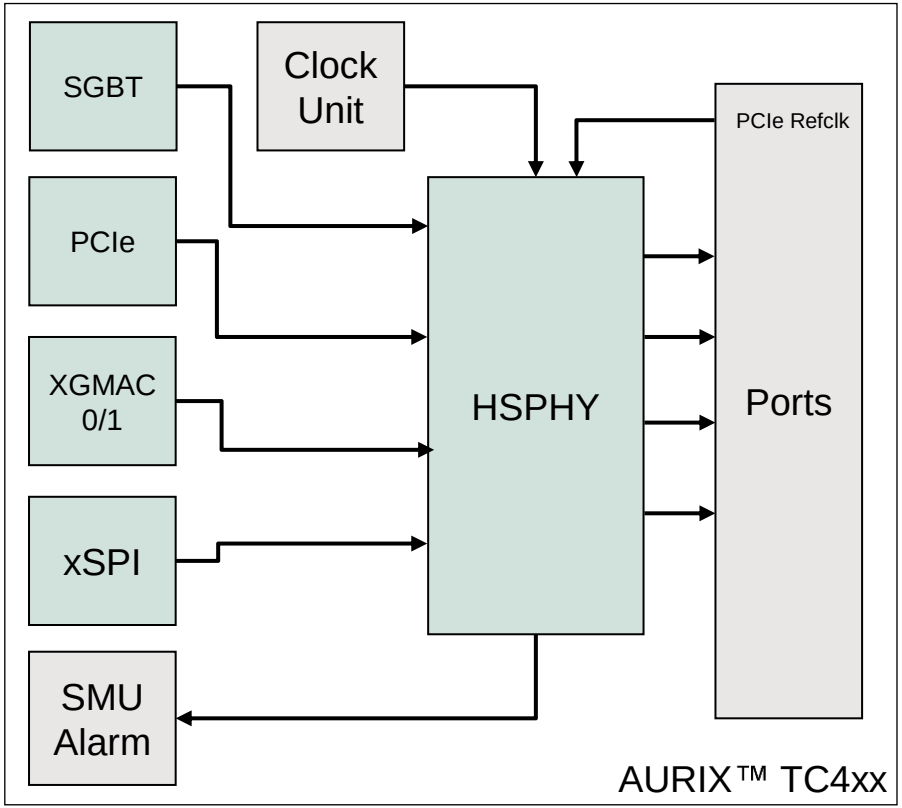
HSPHY
Skew generation for DDR interfaces



- Skew generation for DDR interfaces such as Ethernet RGMII and serial SPI interfaces (xSPI)
  - The RGMII data and clock are typically transferred by IPs simultaneously, without any skew on the clock. For proper sampling of the data signals at the receiver side, a skew shall be added to the clock signal, either by the PCB traces, or by the transmitter/receiver itself. HSPHY provides these options
  - For xSPI the HSPHY allows to skew the clock in relation to the output data and skew of the data strobe to the receive data

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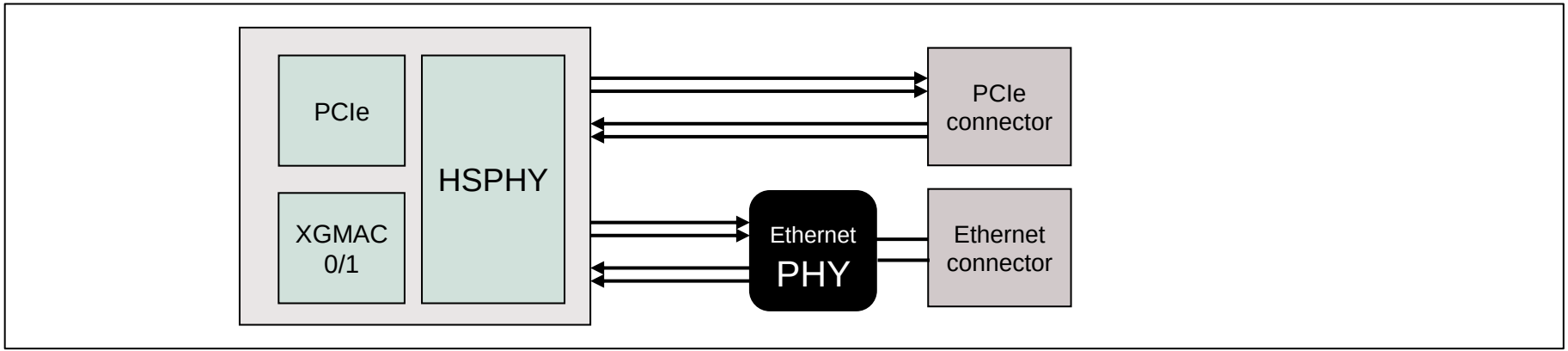
HSPHY
System integration



- The clock unit provides the necessary clocks for the HSPHY
  - For PCIe an external reference clock must be provided to the HSPHY block
- Peripherals like PCIe of Ethernet can use the HSPHY integrated MP8G PHY for serialization of data streams
- xSPI and Ethernet can use the HSPHY integrated DLL to generate a clock to data skew on the signals
- SMU Alarms can be raised by the HSPHY from safety flip flops

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Application example
Ethernet and PCIe



Overview

- Flexible usage of MP8G PHYs allows the selected usage of various types of Ethernet SerDes connection to Ethernet PHY/Switches or PCIe
- Tracing of the MCU is possible on high data rates by using HSPHY

Advantages

- Low number of IO's are used compared to parallel interfaces
- Several of market Ethernet PHYs interfaces are supported and provide flexibility on external components

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