

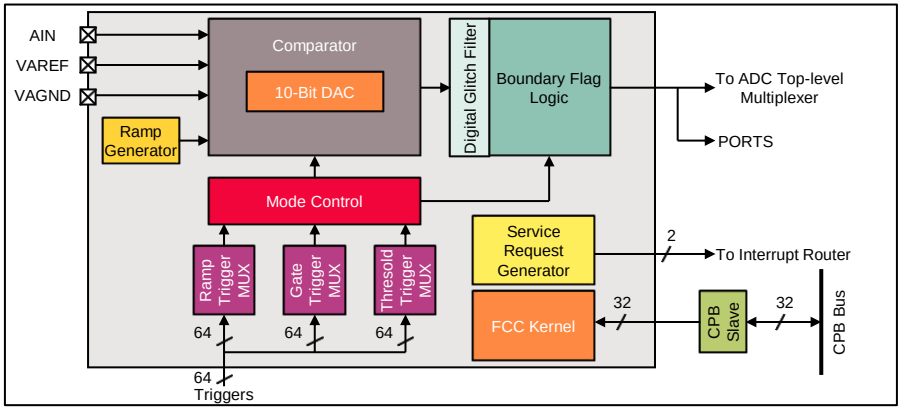
FCADC
Fast Compare Analog-to-Digital Converter

AURIX™ TC4xx Microcontroller

V1.0.0 2024-09

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ADC
Fast Compare Analog-to-Digital Converter



Highlights

- Response time up to 18.75 ns
- Ramp mode support with configurable step width and size
- Flexible trigger interface for updating 10-bit threshold, gating boundary flag and ramp start or end
- Boundary flags to timer modules (GTM or eGTM) and pads

Key Features

Fast compare rate up to 25 ns (40 MHz)

Ramp mode for automatic peak and hold support and peak current mode control for DC-DC use cases

Customer Benefits

- Fast detection of input signal crossing predefined 10-bit threshold

- No user software overhead needed
- Ideal for “peak and hold” implementation in powertrain or power conversion application

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FCADC
Fast compare rate up to 25 ns

- Programmable trigger for threshold update
- Compare event can be masked by selected gating signal
- Compare threshold can be configured by software or by hardware trigger. Pre-defined new threshold will become effective when hardware trigger is received
- Fast compare rate support e.g. immediate PWM switch off in case over voltage or over current event is detected
- Hysteresis operation mode supported
- Optional digital glitch filter to filter unintended glitches
- Boundary flags, which represent compare events, can be:
  - directly routed to e.g. timer module for reaction without software overhead
  - routed to GPIO to directly interact with externally connected peripherals
  - inverted, set, cleared by software too. This offers more flexibility to support different use cases

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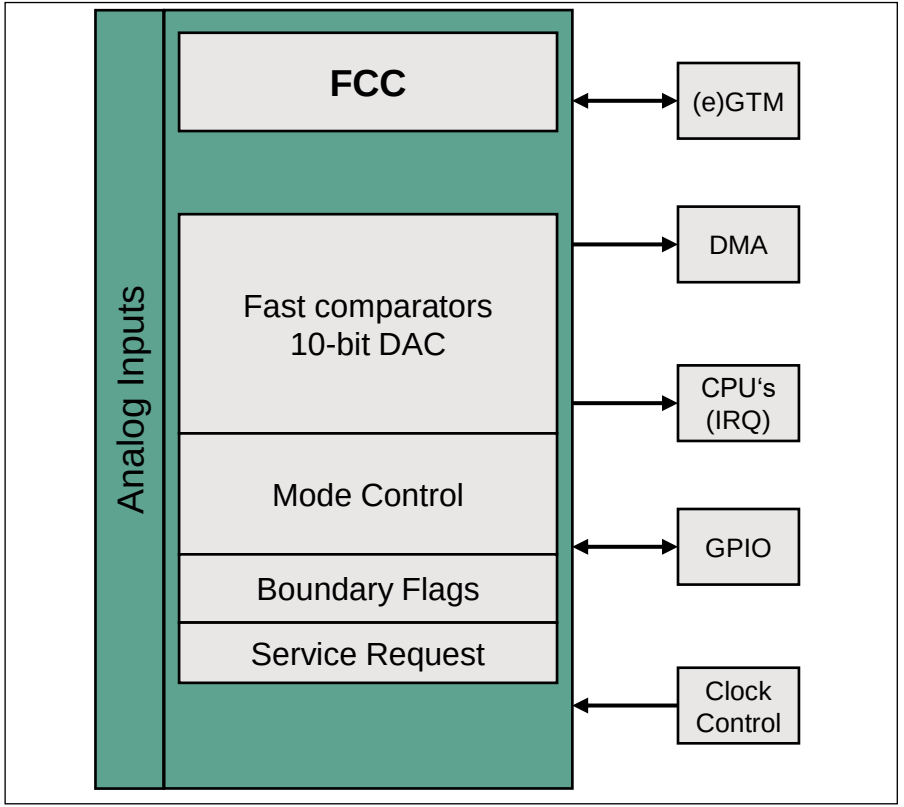
FCADC
Ramp mode for automatic “peak and hold” support

- In powertrain or power conversion applications, it is common to implement peak and hold control
- In addition, software overhead should be avoided as much as possible, due to fast reponse requirement
- Fast Compare Comparator (FCC) supports updating of the compare threshold by either software, or hardware trigger
- Ramp mode can automatically update intermediate compare thresholds without user or software interaction. User sets the ramp start and end thresholds, together with selected step width in between, then FCC will automatically update thresholds during ramp up or ramp down control
- Flexible ramp start and end possbilities provided

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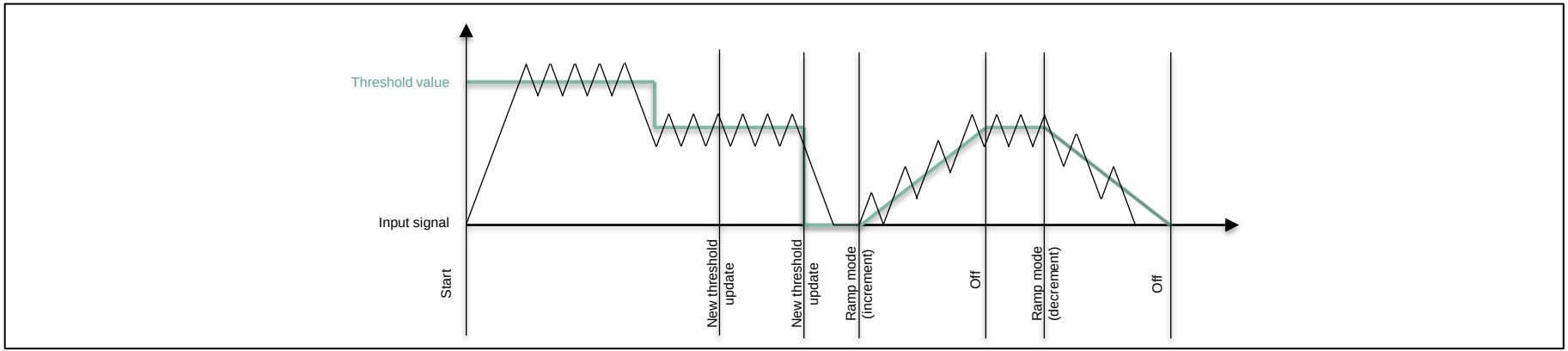
FCADC
System integration

- No input multiplexer provided for FCC analog input channel. This simplifies control overhead and ensures fast response
- Each FCC channel operates independently
- Compare event result, which is represented by boundary flag, can be processed by e.g. timer module directly
- Boundary flags can also be directly output to GPIO, user periperhal e.g. ASIC connected on GPIO can react accordingly



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Application example
Peak and hold operation modes



Overview

- “Peak and hold” is widely used in powertrain and power conversion application
- Hardware solution is required by users
- Ramp mode can be started by either hardware or software trigger
- Ramp mode can be ended by reaching configured threshold, or by hardware trigger

Advantages

- A new threshold can become effective either by hardware trigger e.g. from timer module or by software
- Software interaction or overhead in ramp mode is avoided to guarantee real time reaction without delay
- In ramp mode, control for ramp up or ramp down is implemented by FCC hardware. User just needs to input the ramp start, end and step width

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