

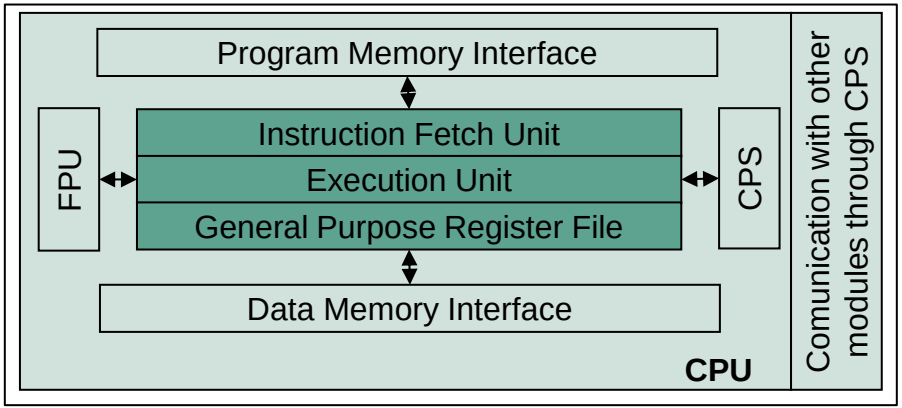
CPU
Central Processing Unit

AURIX™ TC4xx Microcontroller

V1.0.0 2024-09

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CPU
Central Processing Unit



Highlights

› The Central Processing Unit (CPU) comprises of an Instruction Fetch Unit, an Execution Unit, a General Purpose Register File (GPR), a CPU Slave interface (CPS), and Floating Point Unit (FPU)

Key Features

- Virtualization support in hardware
- Temporal protection System
- Flexible memory protection
- Wide range of supported instructions

Customer Benefits

- › Integration and separation of multiple applications
- › Time bounded real time operation
- › Multiple protection ranges over the memory
- › Wide variety of optimized SW possible

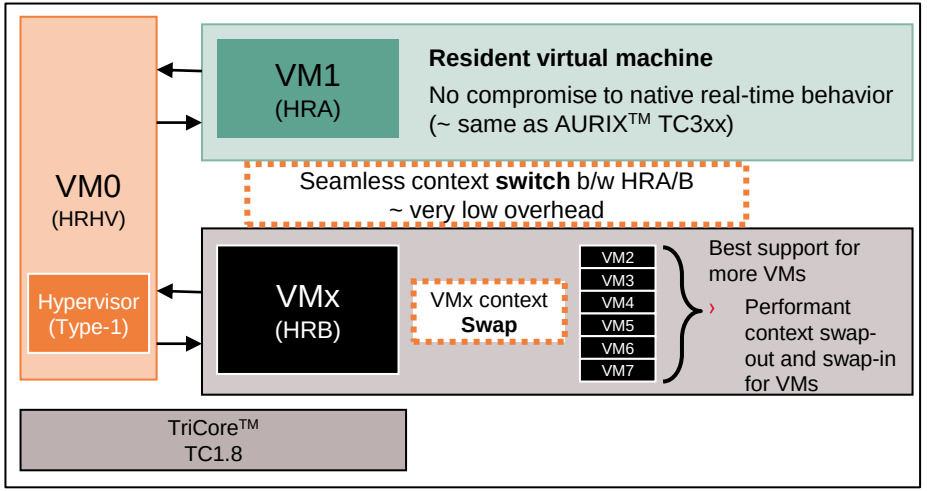
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CPU
Virtualization support in Hardware

The TC1.8 processor supports a hypervisor (HV), one real-time virtual machine, and up to 6 other virtual machines, making a total of 8 virtual machines (VMs). Three sets of dedicated hardware resources are provided to support virtualization: HRHV, HRA, and HRB.

The mapping of virtual machines to hardware resources is as follows:

- HRHV – Hypervisor hardware resource (VM0)
- HRA – Real time virtual machine hardware resource (VM1)
- HRB – Other virtual machine hardware resources (VM2-7)



Note: VM0 is used as an alias for the hypervisor

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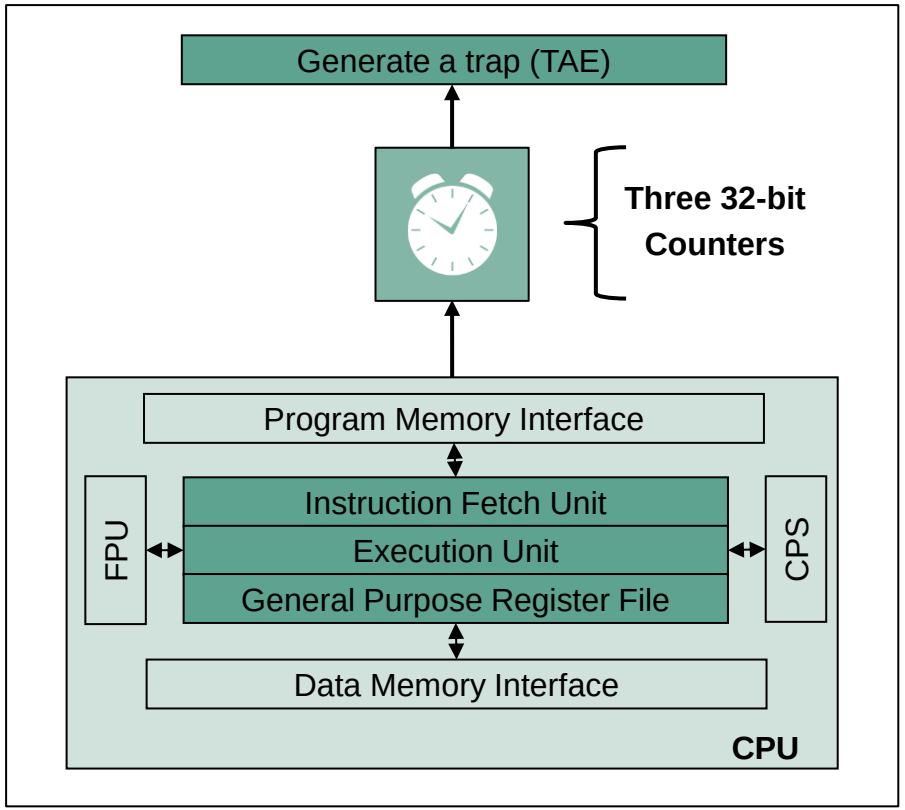
CPU
Temporal protection system

A very common problem of real time systems is given by the tasks with a defined runtime. Overrunning this can lead to overall program failures.

Each TC1.8 CPU implements a temporal protection system (TPS) formed out of three independent 32-bit decrementing counters clocked by the primary CPU clock.

The operating system (OS) loads the expected runtime at task‘s start and a temporal asynchronous exception (TAE) trap is generated when the counter reaches 0. Generating a trap, and not an interrupt, protects the system in case the task is allowed to disable interrupts for periods of time.

Based on the counters‘ values (together with the time-out flags), it is ensured that the real time application is time bounded.



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CPU
Flexible memory protection

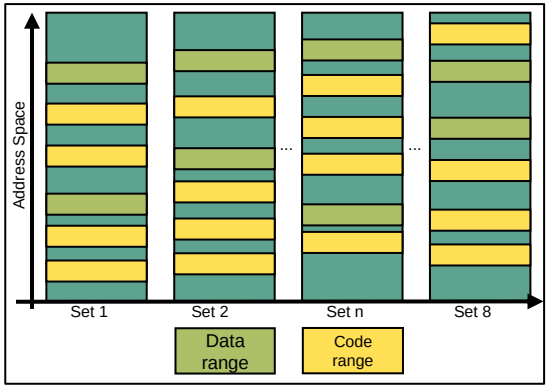
For each task or VM in the real-time system, memory resources are explicitly defined. If these resources are exceeded, failures can occur in the application.

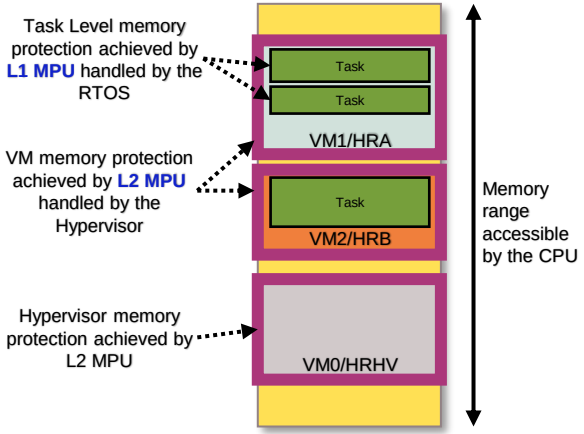
A Memory protection unit (MPU) prevents a program from overrunning its assigned region of memory by enforcing access permissions defined by specific address ranges.

Data access permissions are defined by any combination of write and read enable. Fetch access permission is based on access enable rights.

Fast permission switching is based on 8 protection sets with up to 24 defined data ranges and up to 16 defined code ranges. The range to set assignment is flexible, which enables setting the right memory protection for the application at hand.

Level 1 (L1) & Level 2 (L2) MPUs are provided for protection on task and VM level, respectively. L1 memory violations generate TRAP into task or VM context. L2 violations generate trap into HV context.



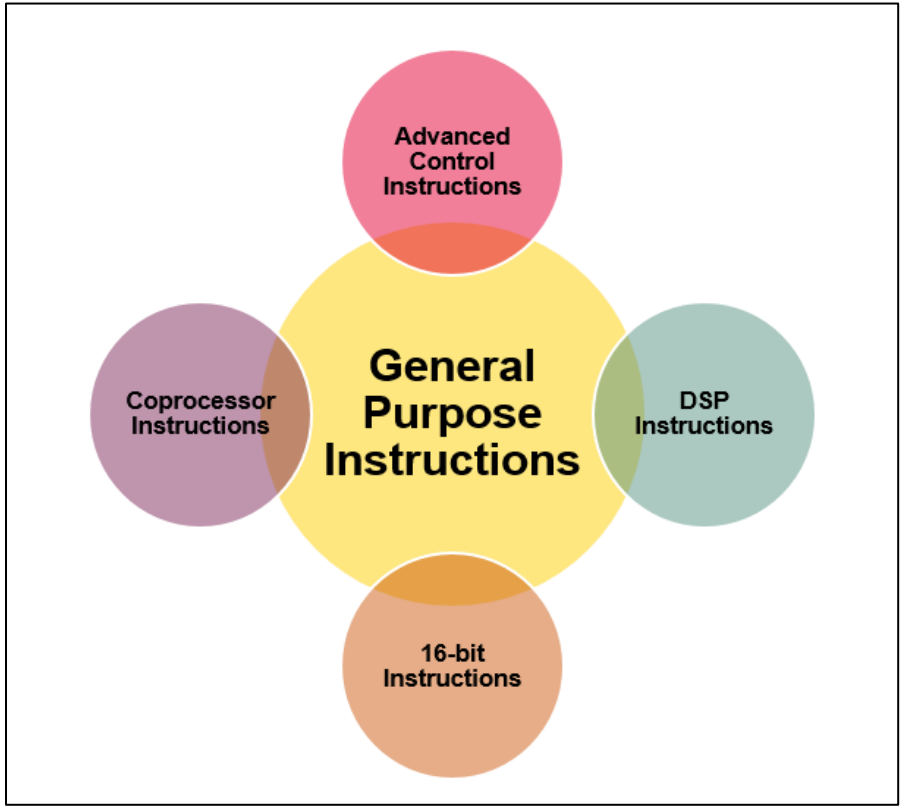


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CPU
Wide range of supported instructions

This very rich instruction set covers 16-bit and 32-bit format instructions, which can be freely mixed in the instruction stream, reducing code size and optimizing the application. The instruction set supports a number of data types including bytes, signed and unsigned integers, single precision floating-point and 16- and 32-bit signed fractions.

TriCore™ TC1.8 Instruction Set	
General Purpose Instr.	Arithmetic, Logic Address Arithmetic & Comparison, Load/Store, Context Switch, Virtualization
Advanced Control Instr.	Bit-field, Bit-logical, Min/Max Comparison, Branch
Coprocessor Instr.	Single & Double precision Floating Point
16-bit Subset	Load/Store, Arithmetic, Branch
Digital Signal Processor (DSP) Instr.	MAC, Saturated Math, DSP Addressing Modes, SIMD Packed Arithmetic



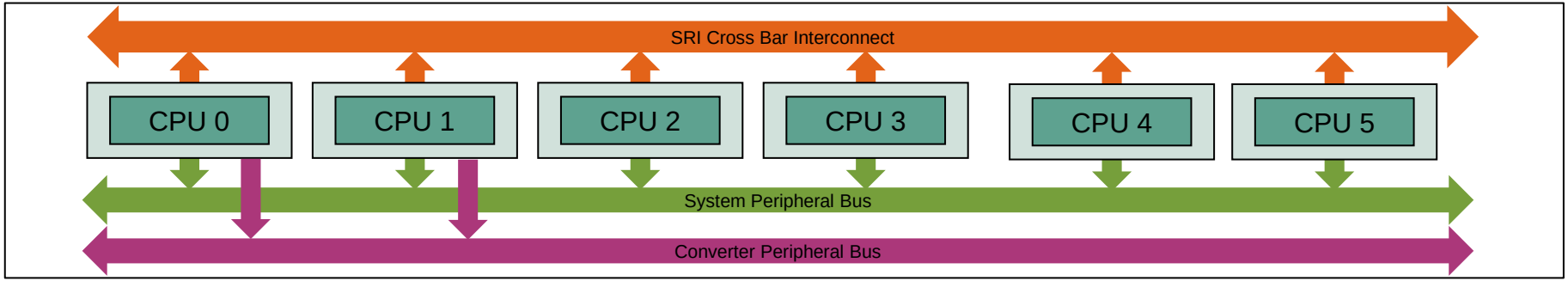
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CPU
System Integration

The AURIX™ TC4xx 32-bit microcontroller family contains a wide range of safety oriented devices.

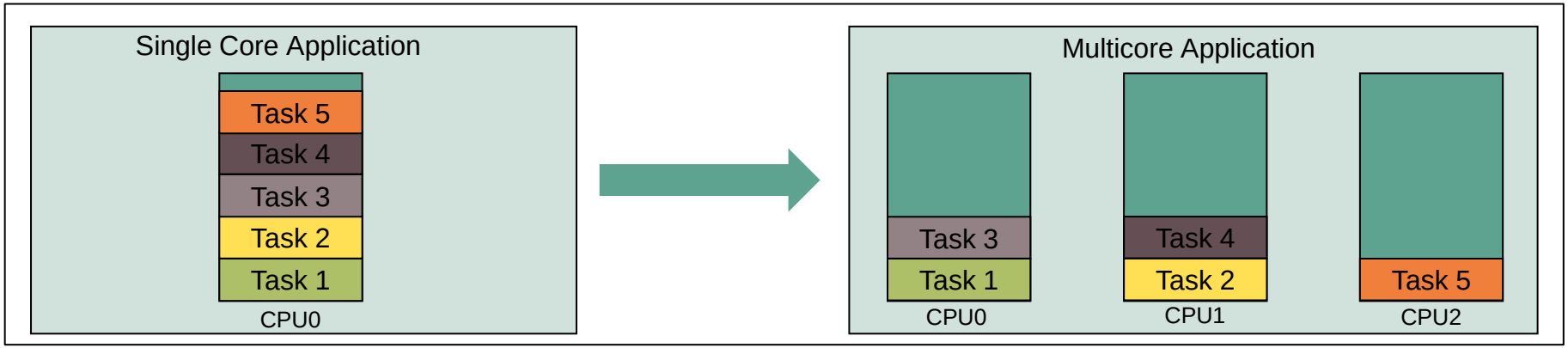
One of the most important features of the family is the "lockstep" capability. A core operating in Lockstep mode consists of a master and checker core. The checker core executes the same instructions as the master core, but it is two clock cycles out of phase. In case the outcome of a checker core is different from the master, an alarm is generated.

The CPUs are connected to the rest of the system and other peripherals via the Shared Resource Interconnect (SRI) crossbar and via the System Peripheral Bus (SPB) and Converter Peripheral Bus (CPB) if existing.



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Application Example
Multicore application



Overview

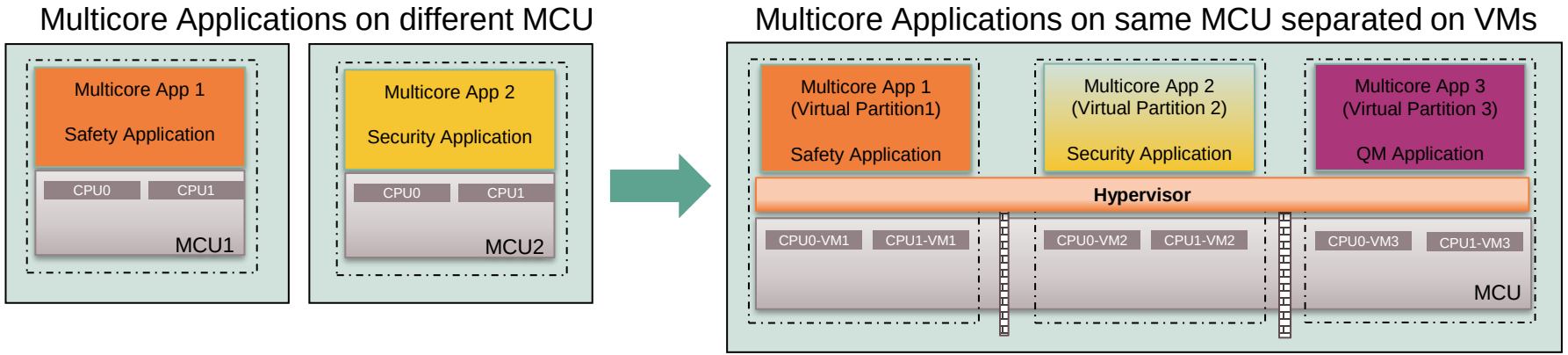
- **Issue:** Real-time applications running multiple tasks have the issue of overloading the CPU
- **Solution:** Switching to a multicore system, where tasks are divided over multiple cores. In the case of tasks depending on each other, the needed communication and scheduling will slightly reduce the performance

Advantages

- Avoid CPU overload
- Improvement of overall system‘s performance
- Clear division of tasks over the whole system (moving from „one-man show“ to „team work“)

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Application Example
Virtualization



Overview

- **Issue:** Different type of applications running on different MCUs need to be integrated on same MCU and executed without interfering each other
- **Solution:** Consolidate to one MCU multicore system, where applications are distributed over multiple Virtual Machines running over multiple cores and scheduled by a Hypervisor

Advantages

- Reduction of number of MCUs
- Efficient use of CPU computing power
- Flexible activation and deactivation of features on same MCU
- Enable the applications consolidation with different OS on one MCU

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Document reference
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