# Customer training workshop: QSPI_Flash_Read_Write for KIT_T2G-B-H_EVK

TRAVEO™ T2G CYT4BF series Microcontroller Training
V1.0.0 2022-11

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# Scope of work

- This code example demonstrates interfacing with an external NOR flash memory in Quad SPI (QSPI) mode using the serial memory interface (SMIF).

- Device
  - The TRAVEO™ T2G CYT4BFBCH device is used in this code example.

- Board
  - The TRAVEO™ T2G KIT_T2G-B-H_EVK board is used for testing.


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# Introduction

- **QSPI Flash has the following features**
  - SPI protocol
    - Supports dual-quad SPI mode
    - Supports single data rate (SDR) and dual data rate (DDR) transfers
  - Memory device
    - Supports overall device capacity in the range of 64 KB to 4 GB in power of two multiples
    - Supports configurable external device capacities
    - Supports two external memory devices
  - Memory mapped I/O (MMIO) operation mode
  - eXecute-In-Place (XIP) mode
    - XIP operation mode for both read and write accesses
    - XIP mode supports on-the-fly encryption and decryption
    - XIP operation mode via AHB interface for CM0 and AXI interface for CM7 core
    - Supports up to four outstanding transactions


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# Introduction (contd.)

- **QSPI Flash has the following features**
  - Memory interface logic
    - Supports stalling of SPI transfers to address back pressure on FIFOs
    - Supports an asynchronous SPI transmit and receive interface clock
    - Supports read-write-data-strobe (RWDS)
    - Supports multiple interface receive clocks
    - Supports flexible external SPI memory devices' data signal connections
    - Independent SPI interface transmitter clock from PLL/FLL
    - SPI interface logic supports flexible external memory devices' data signal connections


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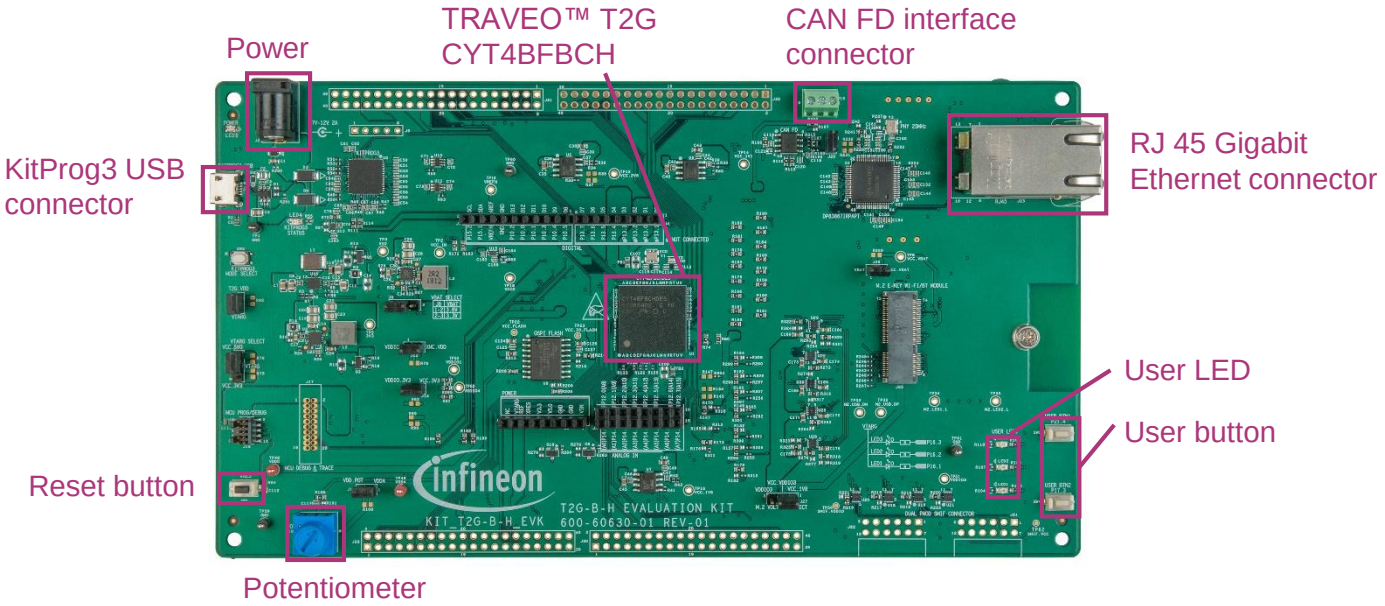
# Hardware setup

› This code example is developed for the KIT-T2G-B-H-EVK board.

› Connect your PC to the board using the provided USB cable through the KitProg3 USB connector.





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# Implementation

This code example demonstrates interfacing with an external NOR flash memory in QSPI mode using the serial memory interface (SMIF). This code example performs QSPI Flash write, sector erase, and read operation check. If the operation succeeds, then the LED blinks, and if it fails, the LED is always ON.

**Follow these steps to configure this code example:**

- STDOUT setting
- GPIO port pin initialization
- QSPI initialization
- Flash write enable
- Flash sector erase
- Flash sector read
- Flash page write to the memory
- Check status for read data matches with written data


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# Implementation (contd.)

**Re-target I/O initialization**

› Call the ***cy_retarget_io_init()*** function to use UART as STDOUT

- Initialize P13.1 as UART TX and P13.0 as UART RX (these pins are connected to KitProg3 COM port)
- The serial port parameters change to 8N1 and 115200 baud

**GPIO port pin initialization**

› The ***cyhal_gpio_init()*** function initializes the GPIO port pin as output to User LED

- User LED is connected to P16.1 as output (initial level = H, LED turns off)

**QSPI initialization**

› The ***cyhal_qspi_init()*** function initializes the QSPI peripheral

- Initializes QSPI parameters (clock pin, set of pins, bus frequency, clock polarity, phase mode)
- See also ***cyhal_qspi_slave_pin_config_t*** for parameter details


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# Implementation (contd.)

**Flash write enable**

› The ***cyhal_qspi_transfer()*** function sends the write enable command and gets a response
  – The command to be sent is described in ***device_specific_wren_command***, See ***cyhal_qspi_command_t*** for details

**Flash sector erase**

› The ***cyhal_qspi_transfer()*** function sends the sector erase command and gets a response
  – The command to be sent is described in ***device_specific_4se_command*** (***cyhal_qspi_command_t***)

**Flash sector read**

› Call the ***cyhal_qspi_read()*** function to read back the data in the erased sector
  – The command to be sent is described in ***device_specific_4qior_command*** (***cyhal_qspi_command_t***)
  – After the read data is returned from the function, it is stored in ***rx_buf***, and the data is then compared with the expected value


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# Implementation (contd.)

**Flash page write to the memory**

- The ***cyhal_qspi_write()*** function sends the write command along with block of data to be written
  - The command to be sent is described in ***device_specific_4qpp_command*** (***cyhal_qspi_command_t***), and the data is prepared in ***tx_buf***

**Check status for read data matches with written data**

- If all the processes (erase sector → verify → write sector → verify) are successfully completed, User LED blinks every 1 sec by calling the ***cyhal_gpio_toggle()*** periodically
- However, if any HAL function call shows an error, the error is caught in the ***check_status()*** function and it calls the ***cyhal_gpio_write()*** function to light up the User LED


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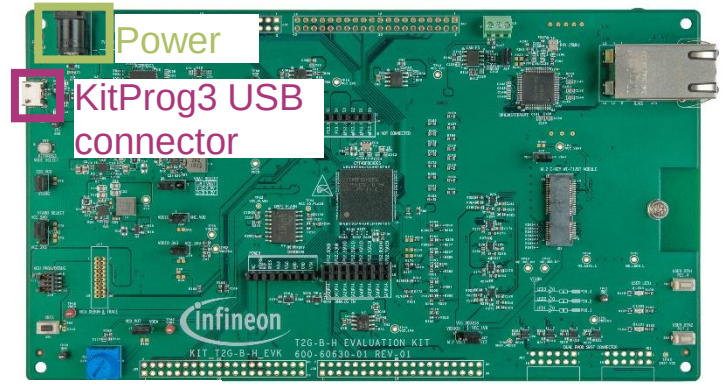
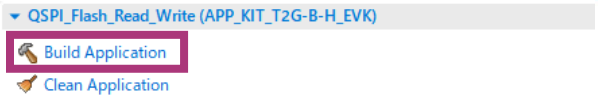
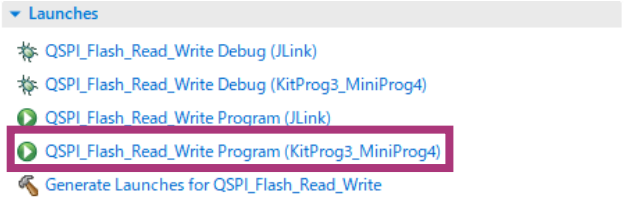
# Compiling and programming

1. Connect to power and USB cable
2. Use Eclipse IDE for ModusToolbox™ software for compiling and programming
3. Compile
   a) Select the target application project in the Project Explorer.
   b) In the Quick Panel, scroll down, and click "Build Application" in QSPI_Flash_Read_Write (APP_KIT_T2G-B-H_EVK)




4. Open a terminal program and select the KitProg3 COM port. Set the serial port parameters to 8N1 and 115200 baud.
5. Programming
   a) Select the target application project in the Project Explorer
   b) In the Quick Panel, scroll down, and click "QSPI_Flash_Read_Write Program (KitProg3_MiniProg4)" in Launches





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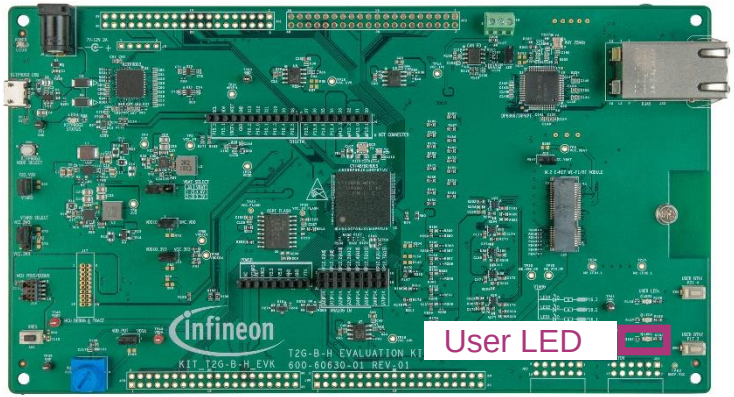
# Run and test

1. After programming, the application starts automatically. Confirm that the QSPI flash Read and Write example title is displayed on the UART terminal as follows:
2. Observe the User LED to determine the status of the read write operation. If the operation succeeds, then the LED blinks, but if it fails, the LED is always ON.




COM14 - Tera Term VT

File Edit Setup Control Window Help

```
********** HAL: QSPI Flash Read and Write **********


1.Erasing

2. Reading after Erase and verifying that each byte is 0xFF

Received Data (64 bytes):
-------------------------
0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF
0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF
0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF
0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF 0xFF

3. Writing data to memory

Written Data (64 bytes):
-------------------------
0x00 0x01 0x02 0x03 0x04 0x05 0x06 0x07 0x08 0x09 0x0A 0x0B 0x0C 0x0D 0x0E 0x0F
0x10 0x11 0x12 0x13 0x14 0x15 0x16 0x17 0x18 0x19 0x1A 0x1B 0x1C 0x1D 0x1E 0x1F
0x20 0x21 0x22 0x23 0x24 0x25 0x26 0x27 0x28 0x29 0x2A 0x2B 0x2C 0x2D 0x2E 0x2F
0x30 0x31 0x32 0x33 0x34 0x35 0x36 0x37 0x38 0x39 0x3A 0x3B 0x3C 0x3D 0x3E 0x3F

4. Reading back for verification

Received Data (64 bytes):
-------------------------
0x00 0x01 0x02 0x03 0x04 0x05 0x06 0x07 0x08 0x09 0x0A 0x0B 0x0C 0x0D 0x0E 0x0F
0x10 0x11 0x12 0x13 0x14 0x15 0x16 0x17 0x18 0x19 0x1A 0x1B 0x1C 0x1D 0x1E 0x1F
0x20 0x21 0x22 0x23 0x24 0x25 0x26 0x27 0x28 0x29 0x2A 0x2B 0x2C 0x2D 0x2E 0x2F
0x30 0x31 0x32 0x33 0x34 0x35 0x36 0x37 0x38 0x39 0x3A 0x3B 0x3C 0x3D 0x3E 0x3F

================================================================================

SUCCESS: Read data matches with written data!

================================================================================
```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# References

**Datasheet**

› CYT4BF datasheet 32-bit Arm® Cortex®-M7 microcontroller TRAVEO™ T2G family

**Architecture Technical reference manual**

› TRAVEO™ T2G automotive body controller high family architecture technical reference manual

**Registers Technical reference manual**

› TRAVEO™ T2G automotive body controller high registers technical reference manual

**PDL/HAL**

› PDL

› HAL

**Training**

› TRAVEO™ T2G Training


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# Revision History

| Revision | ECN | Submission Date | Description of Change |
|---|---|---|---|
| ** | 7836287 | 2022/11/01 | Initial release |


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