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PWM Dead Times in Automotive Traction Inverters using IGBT, SiC MOSFET, or Si/SiC Fusion Switch Power Modules

Tomas Reiter | Julius Schapdick | Michael Krug | Mark Muenzer | Frank Wolter

Automotive High Voltage Power Modules, Infineon Technologies AG, Neubiberg, Germany

Correspondence: Tomas Reiter (tomas.reiter@infineon.com)

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ABSTRACT

This article features a comprehensive methodology for analyzing and optimizing PWM dead time in automotive traction inverters, applicable to a wide range of power devices, including Si IGBT/Diodes, SiC MOSFETs, and Si/SiC Fusion switches. The proposed methodology enables a systematic comparison of dead time characteristics, focusing on part-to-part tolerances and operating point-dependent influence factors. Three traction inverter systems, each in the 200–300 kW class at 470 V, were built up utilizing Si IGBT/Diode, SiC MOSFET, and Si/SiC Fusion switches from the latest automotive-released technology. The impact of PWM dead times on power losses was experimentally investigated for all three inverter systems, supporting the analytical model. Key findings from the experimental data include: (1) PWM dead times can account for more than 10% of the total inverter power losses in high current density SiC MOSFET inverter designs operating at typical automotive switching frequencies of 10 kHz; (2) Optimizing PWM dead times in Si/SiC Fusion power modules leads to up to a 5% reduction in total inverter power losses and improved current sharing, resulting in lower thermal stress—This was evaluated using thermal infrared measurements from the Si/SiC Fusion inverter prototype; 3) Optimized PWM dead times can reduce total harmonic distortion at light load conditions by up to 2%–3% for IGBT/Diode and up to 4%–5% for SiC MOSFET and Si/SiC Fusion inverter systems; (4) A sensitivity study in addition revealed that Si/SiC Fusion switches exhibit the most stable dead time settings under parameter variations. The benefit of optimized versus conventional 2 µs PWM dead times would result in an annual energy saving of approximately 6 GWh per 1 million vehicles. This highlights the significance of optimized PWM dead times in automotive traction inverters operating at typical switching frequencies of 10 kHz. The goal of this investigation is to support the development of reliable and efficient automotive traction inverters, with the methods presented being applicable to other applications as well.

1 | Introduction

The three-phase two-level voltage source inverter topology, also known as the B6 bridge, still dominates the automotive traction inverter application for hybrid and electric vehicles [1–3]. A crucial aspect of this topology is the insertion of PWM dead times, where both the low-side and high-side switches are turned off before one of the switches turns on. This is necessary to prevent shoot-through currents via the half-bridges, which can lead to increased power dissipation and device failures. The majority of today's automotive traction inverters, with an output power of more than 100 kW, apply PWM dead times in the range of 2000–3200 ns for IGBT/Diode and 1500–2000 ns for SiC MOSFET inverters to ensure that no shoot-through occurs. However, "too long" PWM dead times can result in several drawbacks, such as increased power losses and increased harmonics on the inverter output currents, particularly when wide bandgap SiC MOSFETs are used as power switches, which have a high pn-junction voltage drop of the body diodes compared to their silicon counterparts. To mitigate these issues, it is essential to minimize the PWM dead times while ensuring they are sufficient to prevent shoot-through currents.

In DC/DC converter applications, PWM dead time optimization methods have shown remarkable benefits in terms of efficiency improvement, especially at high switching frequencies above 100 kHz [4–7]. However, in automotive traction inverter applications the switching frequency at about 10 kHz is rather low and the output current changes direction within each sinusoidal output period. Thus the switches' roles as control and rectifier switches also change. This means that the relatively constant operating conditions of a DC/DC converter are not present in DC/AC inverter applications, making optimization more complex.

Advanced inverter control algorithms can compensate for the dead time resulting duty cycle drop [8–12]. However, it is essential to know the differences between the applied signal dead time value and the effective time resulting at the power switches. Additionally, the current flow direction must be known, which can be challenging to detect precisely, especially at light load conditions. A compensation approach based on the current ripple estimation has been introduced in [13], but this method also requires a high-bandwidth sensor to feedback a signal correlating with the effective dead time.

The introduction of SiC MOSFETs has made higher switching frequencies feasible compared to traditional IGBT/Diode-based inverter systems, while maintaining high efficiency [3, 14–19]. Due to the high switching frequency, the topic of dead time optimization has gained more attention, as the impact on power losses, reduced effective duty cycle, and modulation index, and harmonics naturally increases [20, 21]. Studies, like [21], for example, have concluded that standard 10 kHz applications will not significantly benefit from dead time optimization, but the impact of high current density designs on dead time-related power losses may have been underestimated as it will be demonstrated by experimental data in Section 4.

Due to rising production volume and increasing cost pressure, combined switches with lower cost silicon IGBT/Diode and efficient SiC MOSFET die areas were researched over the last years extensively. The feasibility of paralleling IGBTs with MOSFETs was first demonstrated in the early 1990s [22] followed by several studies to obtain the right balance between performance and cost [23–25]. The optimization of control patterns for these paralleled devices was under the focus in [26–31]. In order to reduce complexity, the approach proposed in [32] combine the two technologies within the half-bridge high-side and low-side switch. Another way of complexity reduction by enabling a three terminal hybrid switch device was discussed in [33], however it still had additional circuits in between the IGBT and SiC MOSFET gate connections. A further complexity reduction was introduced by the so-called "Si/SiC Fusion" switches, which combine an IGBT/Diode and a SiC MOSFET in a parallel configuration controlled by a single gate drive command [34–37]. In focus of PWM dead times a Si/SiC Fusion switch bring an additional aspect to consider: When the active freewheeling is released, the current commutates to the anti-parallel silicon diode due to its lower forward voltage drop compared to the wide bandgap device. As a result, PWM dead time optimization influences not only the harmonics and power dissipation but also the current shares within the switch configuration, which is also addressed in this article by thermal IR pictures of a traction inverter implementing Si/SiC Fusion switches.

This article presents an approach for calculating the required PWM dead times in inverter systems utilizing IGBT/diode, full SiC MOSFET, or Si/SiC Fusion switch configurations. The proposed method relies solely on parameters readily available in standard semiconductor datasheets, making it a practical and accessible solution. With support of the analytical model, developed in this contribution, factors influencing PWM dead times are discussed and a comparative analysis of the three different switch configurations is provided. The scope of this contribution does not include dead time adjustment during inverter operation or remapping different dead times to high-side and low-side switches correlated to the flow direction of the load current. However, the insights gained from this analysis and experimental data can support future studies and advanced control patterns where dead times are adjusted during application run time. It is worth noting that the Si/SiC switch is considered only in configuration with simultaneous gate drive, which is the most favourable solution for automotive volume applications.

The article is structured as follows: Section 2 provides a clear nomenclature of PWM signal and effective dead times, including an approach to calculate the required timing for the application enabling sensitivity analysis. Section 3 presents a behavioural model to calculate the power losses during dead times. ChapterSection 4 shows the measured power losses over different PWM dead times for all three types of power modules. Section 5 discusses the influence on the current output harmonics, which provides further benefits on the vehicle system level beyond the inverter power electronics. Finally, Section 6 summarizes the key findings, and the Appendix lists the parameters of the applied parts used for the experimental comparison.

2 | PWM Dead times in Inverter Application

2.1 | Nomenclature PWM Dead Times

During a single sinusoidal output cycle, the roles of the high-side and low-side switches alternate, as illustrated in Figure 1. In the half-cycle where the load current flows into the half-bridge, the low-side switch acts as the "control switch". It operates in the first quadrant during the on-state and blocks the voltage during the rectification of the high-side switch. Before the rectification switch receives the turn-on command, a dead time ($DT1$) is inserted, during which both devices are turned off. After rectification (i.e., third quadrant operation), another dead time ($DT2$) is inserted before the control switch is turned on again. In the other half-cycle, the control and rectifier switch roles of the high-side and low-side switches are reversed. As a result, the mapping of $DT1$ and $DT2$ to the switches also changes. This is the primary reason why advanced control methods with dead time compensation require precise knowledge of the zero-crossing points of the output current. In automotive volume applications, a single "large enough" dead time setting is typically applied, which accommodates both $DT1$ and $DT2$ dead times. This approach with constant (i.e., current polarity independent) settings is different from DC/DC converter applications and

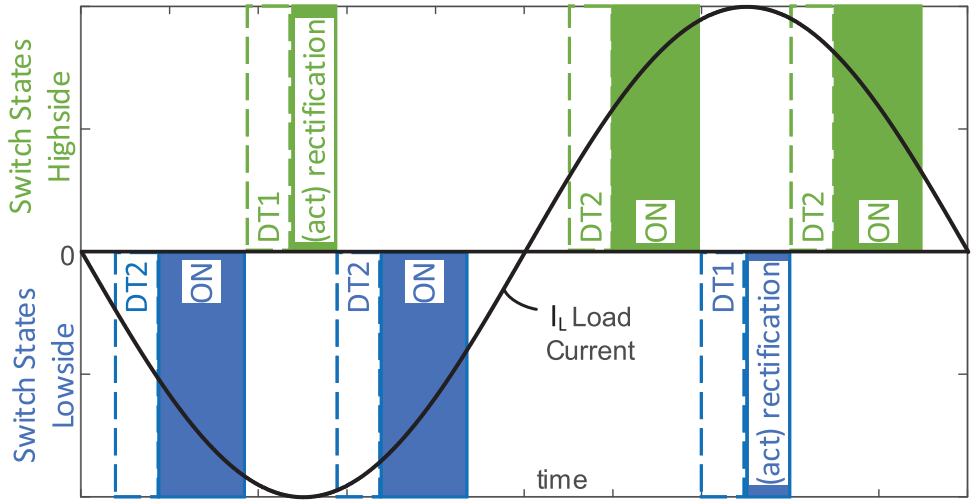


FIGURE 1 | Simplified control pattern in inverter application. During DTx both switches in the half bridge are off. The dead time insertion $DT1$ is the delay to turn-on the "rectifier switch" and $DT2$ is the delay to turn-on the "control switch". The $DT1$ and $DT2$ mapping to high- and low-side switch changes with the sign of the load current. Positive load current is flowing out of the half-bridge.

makes the inverters robust in case of errors in measuring the zero-crossing currents. However, it can lead to inefficiently long dead times if the $DT1$ and $DT2$ values deviate significantly from each other.

2.2 | Signal vs Effective PWM Dead Times

Currently, there is no standardized nomenclature for PWM dead times in inverter applications. However, due to the signal path from the microcontroller to the power switches and their switching characteristics, the applied PWM dead times in the microcontroller registers and their corresponding I/O pins differ from the time when both power switches are in the off-state (see Figure 2). A common nomenclature for PWM dead times is essential in order to support the optimization task. In this article, the term "signal PWM dead times (DT_{sig})" refers to the settings programmed in the microcontroller. Considering the total signal path, the differences between the programmed dead time and the microcontroller I/O pins can typically be neglected, as they are often less than 10 ns. The "effective dead time (DT_{eff})" is defined as the time when both power switches are in the off-state. Although this naming convention may seem straightforward, the real device characteristics, including parasitic elements and gate drive circuit properties, pose practical challenges. For instance, a device can be in the off-state but may be turned on again due to the subsequent switching slope with dV/dt phase in certain situations. To address this issue, a method with following steps is proposed:

1. Calculating the effective dead times using a simplified behavioural model, which can be populated with typical datasheet parameters. The modelling approach is explained in detail in Section 2.3, providing the basis for studying the impact of tolerances and parameter variations on the required signal dead times (Section 2.4).
2. Executing a real inverter operation with different signal dead times (Section 4).
3. Identifying the dead time setting with the lowest power losses, or in the case of an IGBT/Diode power module, the dead time setting just before the power losses increase. This condition is referred to as "zero effective PWM dead time" in this article.

The advantage of using this nomenclature, where "zero effective PWM dead time" corresponds to minimum power losses and thus maximum inverter efficiency, is that it has benefits compared to nomenclature based on current overshoot during switching transients. For instance, if a situation arises where there is a slight increase in current overshoot but a decrease in switching energies, other definitions would lead to an incorrect conclusion about the optimal operating point for efficiency. From the perspective of ensuring a safe operating area, a critical situation will not occur at the point of "zero effective PWM dead time". This is because overlapping switching with heavily increased transient current overshoot automatically results in low efficiency. This concept has been utilized in the past for online PWM dead time optimizations in DC/DC converters, as discussed in [4, 5]. Additionally, it has been applied in traction inverter power modules for the purpose of implementing an active DC-link discharge feature, as explained in [38, 39].

2.3 | Approach to Calculate PWM Dead Times

In order to calculate the needed PWM dead times, it is necessary to determine the delays in the signal path from the microcontroller's turn-on and turn-off commands to the point when the power switch begins to turn on and completes the turn-off. The required dead time is equal to the turn-on delays minus the turn-off delays. The turn-on process is the same for both the control switch and the rectifier switch, and is illustrated in Figure 3. The turn-on process involves the following steps.

1. The microcontroller's I/O pin rising edge charges the analog filters in front of the gate drive input, reaching the gate driver's input high threshold (t_{r1}).

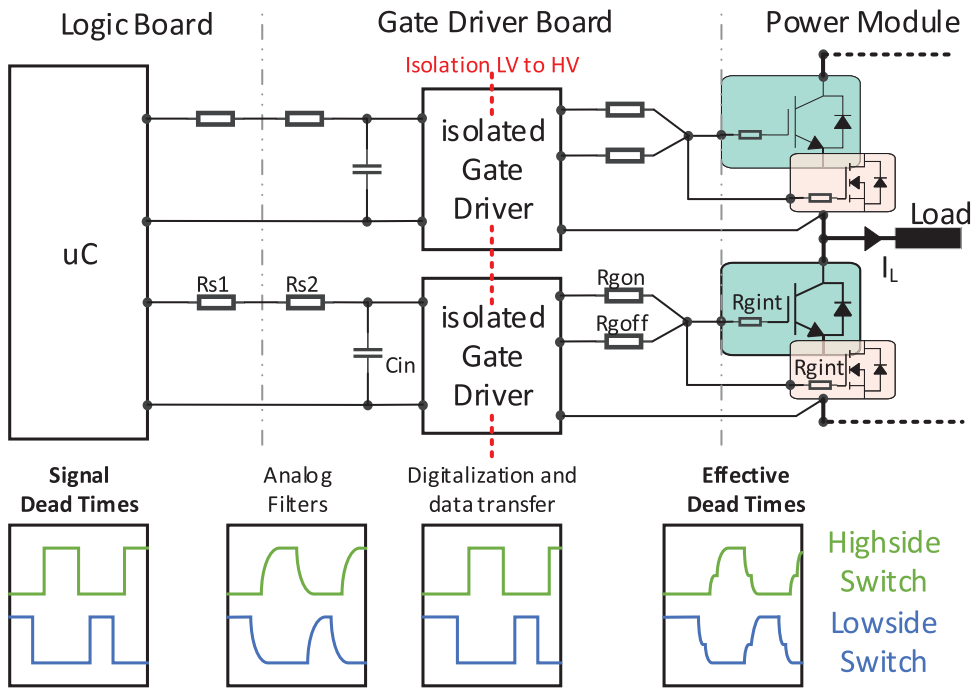


FIGURE 2 | Signal path of the PWM pattern from Microcontroller (uC) to the traction inverter power switches.

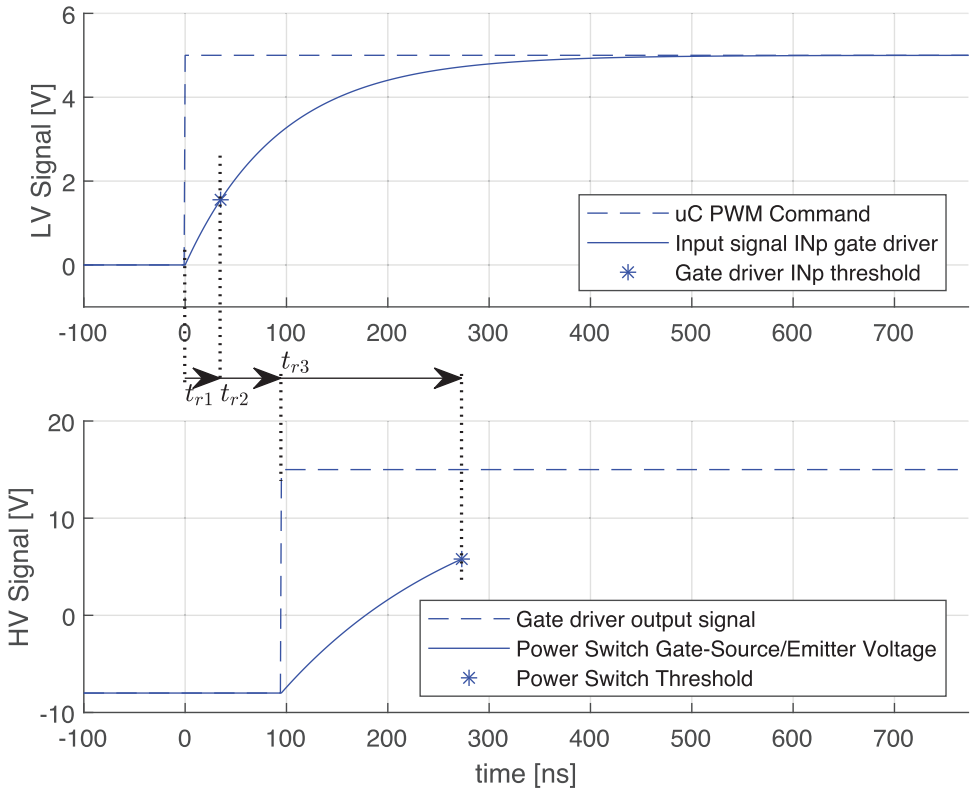


FIGURE 3 | Control switch or rectifier switch turn-on. Analytic approximation of the turn-on signal path. At the point where the switch threshold is reached the channel starts to conduct current.

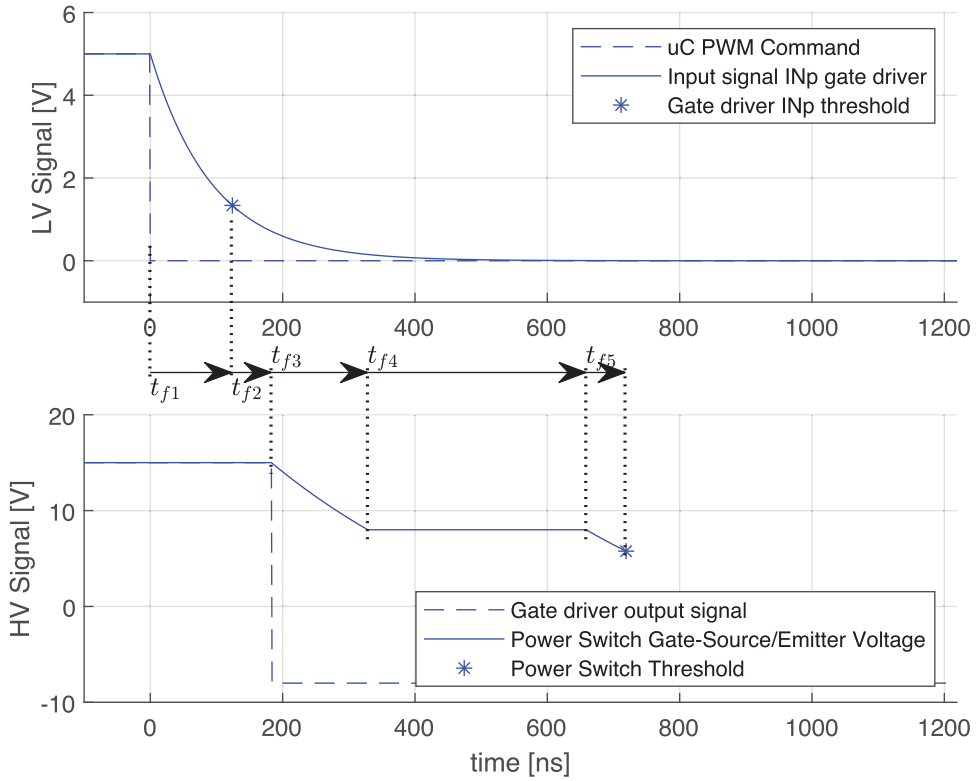


FIGURE 4 | Control switch turn-off. Analytic approximation of the signal path for turn-off for 1st quadrant operation (control switch). At end of the shown waveform the device already blocks voltage.

2. The gate driver recognizes the input high signal and transfers it via a digital transfer chain to the output side, causing a propagation delay (t_{r2}).
3. The gate driver's output charges the gate until the gate threshold is reached, where the power switch begins to conduct current (t_{r3}).

For the purpose of calculating PWM dead times, the turn-on slope beyond this point is no longer relevant. In contrast to turn-on, the turn-off process requires distinguishing between two cases: $DT1$ and $DT2$.

To calculate $DT1$, we need to consider the regular hard switching turn-off sequence of the power switch, as illustrated in Figure 4. The process involves the following steps:

1. The microcontroller's I/O pin falling edge discharges the analog filters in front of the gate drive input, reaching the gate driver's input low threshold (t_{f1}).
2. The gate driver recognizes the input low signal and transfers it via a digital transfer chain to the output side, causing a propagation delay (t_{f2}).
3. The gate driver's output charges the gate until the Miller plateau voltage ($V_{plateau}$) is reached, where the power switch begins to turn off the current (t_{f3}).
4. The Miller charge (Q_{cg}) must be discharged for the turn-off to be completed (t_{f4}), and the turn-off sequence can be considered fully completed when the gate voltage is discharged to the gate threshold voltage (t_{f5}).

It is worth noting that, especially in the case of bipolar devices like IGBTs, tail currents (i.e., stored charge) can be neglected for dead time considerations. This aspect was sometimes explained differently in literature (e.g., [13]). However, when the device channel is off, no emitter to collector conducting path is created. Only a residual amount of charge carriers remaining in the not-depleted drift region of the device, and thus the complementary switch can be turned-on without causing a real shoot-through current.

The sequence for $DT2$ has one major difference. Before $DT2$, the switch was in rectification mode (or active rectification for MOSFET, where the channel conducts current in the reverse direction instead of the body diode), making the turn-off a zero-voltage soft switching (ZVS) event without the presence of the Miller charge, as illustrated in Figure 5 (or see Figure 12 for measured waveform). However, it's essential to charge the gate voltage to a sufficiently low value to ensure safety against parasitic turn-on when the complementary switch turns on and provides a high dV/dt slope directly after the rectifier turn-off event. To achieve this, the missing Miller plateau time must be substituted by a longer and deeper gate voltage discharge (t_{f6}). The switch can be considered robust against parasitic turn-on when the gate driver output stage reaches the gate clamp voltage, typically 2 V above the negative gate driver supply rail $VEE2$. At this voltage, the gate driver clamps the gate to the negative supply rail, bridging thereby the turn-off gate resistor with near zero ohm. Waiting until the gate clamp can be considered safe, but it may not be optimal regarding minimum power losses, as will be discussed later with experimental results. For inverter systems using gate drivers without gate clamp feature, the formulas can

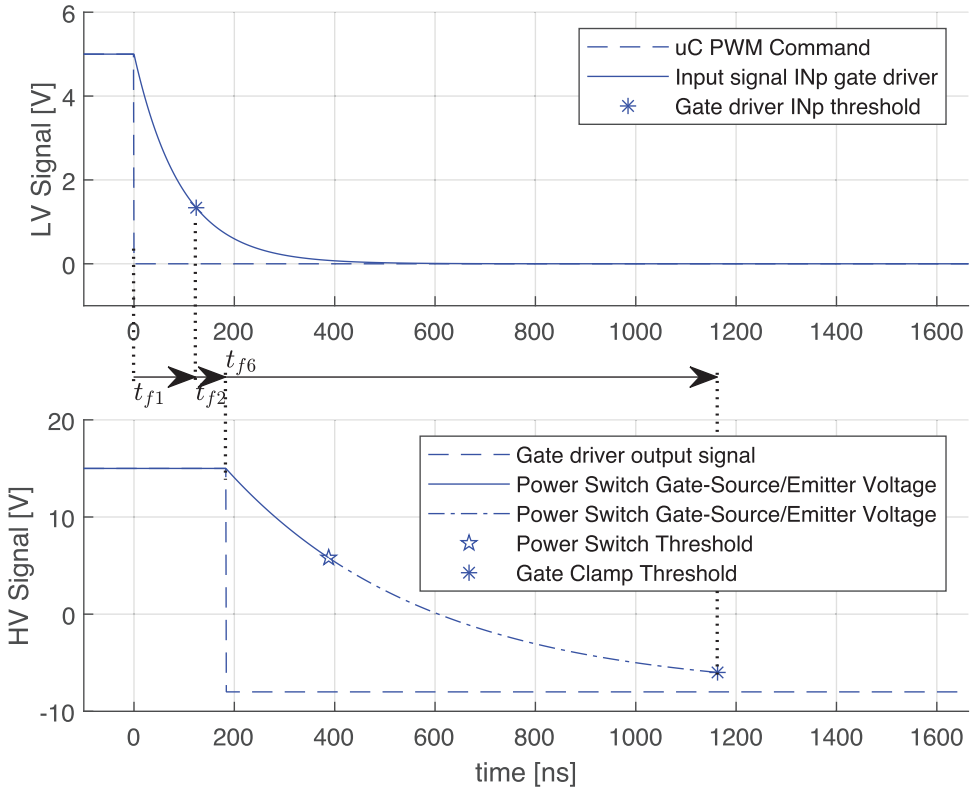


FIGURE 5 | Rectifier switch turn-off. Analytic approximation of the signal path for turn-off for 3rd quadrant operation (rectifier switch). The switch has a zero-voltage turn-off transition and the hard commutation will follow later by the complementary switch turn-on transition (for $DT2_{eff} > 0$).

be still applied, just the respective gate clamp voltage has to be substituted by a low enough gate voltage where parasitic turn-on is prevented.

The effective PWM dead times (DT_{eff}) can be calculated by summing the time sections of the turn-on event and subtracting the sum of the time sections for the turn-off event, as described by Equations (1) and (2). The signal PWM dead times (DT_{sig}) applied by the Microcontroller has to ensure positive effective times values. It is worth noting that a slight overlap (i.e., negative effective time value) will not immediately damage the switches as explained in more detail in [4, 5] and can be safely utilized for special inverter operating modes as shown in [38, 39].

$$DT1_{eff} = DT1_{sig} + (t_{r1} + t_{r2} + t_{r3}) - \left(t_{f1} + t_{f2} + t_{f3} + t_{f4} + t_{f5}\right) \tag{1}$$

$$DT2_{eff} = DT2_{sig} + (t_{r1} + t_{r2} + t_{r3}) - \left(t_{f1} + t_{f2} + t_{f6}\right) \tag{2}$$

The rise and fall times of the individual sections can be calculated using the analytical equations of RC networks, as shown in Equation (3). In this equation, V_S source represents the final voltage across the capacitor.

$$V_c(t) = V_S + (V_0 - V_S) \cdot exp\left(\frac{-t}{R \cdot C}\right) \tag{3}$$

The equation can be solved to determine the time at which the capacitor voltage reaches a certain threshold voltage. Using the formula in Equation (4) and the parameters listed in Table 1, the time sections (tx) of the switching event can be calculated.

TABLE 1 | Parameters for the time sections.

t_x (see Equation 4)	R_x	C_x	V_{xth}	V_{xS}	V_0
t_{r1}	R_{s1}+R_{s2}	C_{in}	$V_{in\_th\_high}$	$VCC1$	$GND1$
$t_{r2} = t_{PDon1}$[a]					
t_{r3}	$Rg_{on} + Rg_{int}$	C_{ies}	V_{geth}	$VCC2$	$VEE2$
t_{f1}	$R_{s1} + R_{s2}$	C_{in}	$V_{in\_th\_low}$	$GND1$	$VCC1$
$t_{f2} = t_{PDoff1}$[a]					
t_{f3}	$Rg_{off} + Rg_{int}$	C_{ies}	$V_{plateau}$	$VEE2$	$VCC2$
t_{f4} see Equation (5)					
t_{f5}	$Rg_{off} + Rg_{int}$	C_{ies}	V_{geth}	$VEE2$	$V_{plateau}$
t_{f6}	$Rg_{off} + Rg_{int}$	C_{ies}	V_{clamp}	$VEE2$	$VCC2$

[a]The digital signal transfer from low- to high-voltage side is approximated with the gate driver propagation delay

$$t_x = -R_x \cdot C_x \cdot log\left(\frac{V_{xth} - V_{xS}}{V_0 - V_{xS}}\right) \tag{4}$$

For the time section t_{f4}, which represents the time it takes to discharge the Miller charge (Q_{cg} named also as Q_{miller} later), the gate voltage remains nearly constant. In this case, the most practical solution is to calculate the gate current within the Miller plateau using the gate resistances and driving voltage (see Equation 5). The more complex minority carrier dynamics of a bipolar device are considered in this article as a current

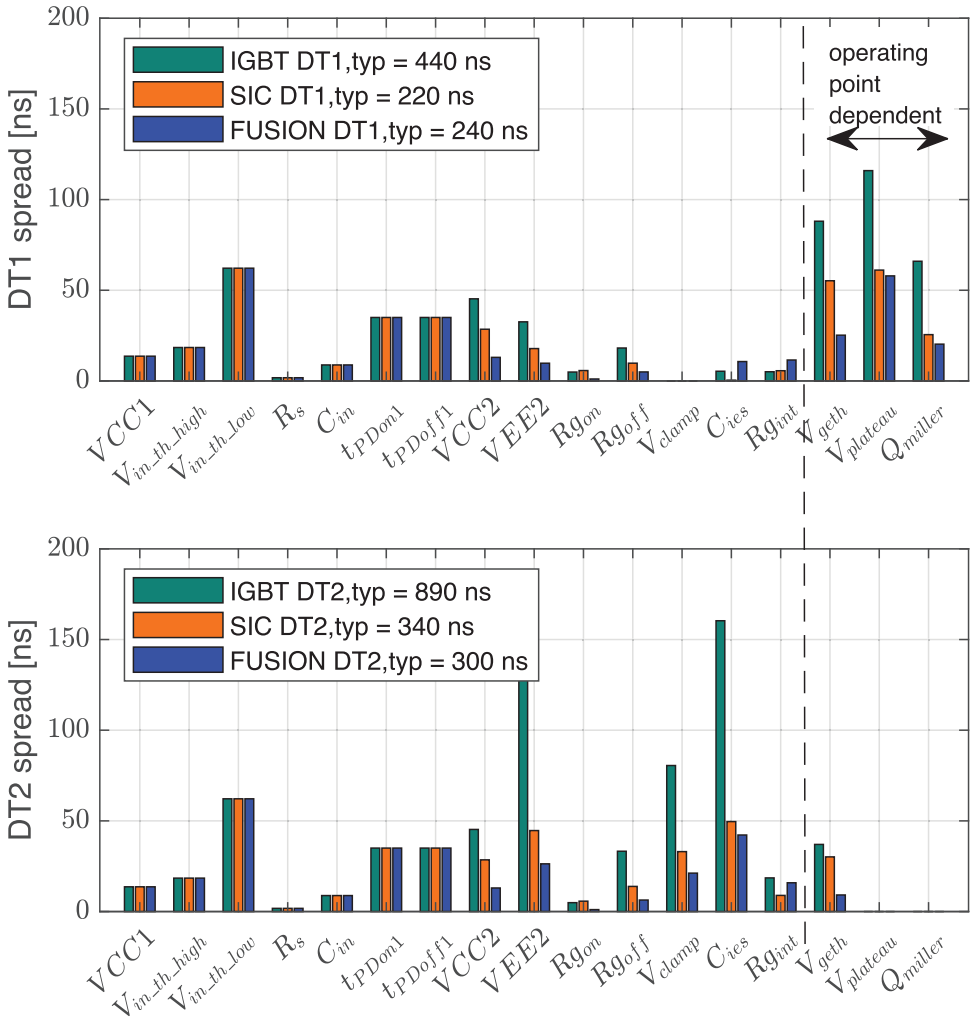


FIGURE 6 | Parameter sensitivity study. Each parameter was changed individually from min to max and the impact on dead time is plotted.

dependent Qcg, which means different values from minimum to maximum can be considered for this charge. With a constant discharge rate, it is possible to calculate the time using parameters from the vendor's product data sheets.

$$t_{f4} = \frac{Q_{cg} \cdot \left(Rg_{off} + Rg_{int}\right)}{V_{plateau} - VEE2} \tag{5}$$

It is essential to note that the proposed method for calculating dead times may result in an absolute deviation from the actual timing that achieves minimum power losses. However, in the three examples with different switch technologies the absolute deviation was within 200 ns and Section 2.4 discusses the potential shifts in case of parameter variation. The calculation provides a solid foundation for a comprehensive understanding of the relative influencing factors of PWM dead times and sensitivity studies regarding part-to-part tolerances and changing operating conditions. Furthermore, this method provides an insightful tool to predict needed dead time adjustments in case gate drivers with adaptive switching speed is applied, where gate voltages and/or supply voltages are changed during application run time and it is well suited to pre-calculate appropriate PWM timings with inputs available from standard semiconductor data sheet values.

2.4 | PWM Dead Time Sensitivity Study (Calculated)

With the support of the analytical approach presented in Section 2.3, it is possible to predict deviations in effective dead times in the event of parameter changes. The article investigates whether there are differences in PWM dead time stability among the three different switch technologies. Using the exemplary devices listed in Table A2, which address similar applications in terms of working voltage and output currents, the impact of 17 key parameters influencing dead times was analysed and plotted in the diagram shown in Figure 6. In this study, the parameters were set to their typical values, and one parameter was modified to its respective minimum and maximum value. The plot reveals that the tolerances on the analog input filters have a relatively low contribution compared to other parameters. As the threshold voltage (V_{geth}) changes with device temperature, the Miller plateau voltage ($V_{plateau}$) with operating current, and the charge (Q_{miller}) with working voltage, these parameters were indicated as operating point dependent. If gate supply voltage fluctuations are also considered as operating point dependent, then the maximum effective dead time deviation at constant signal dead times are 350 ns for the IGBT, 190 ns for the SiC MOSFETs and only 130 ns

for the Si/SiC Fusion switch in this example. Summing up all other non-operating point dependent deviations leads to 470 ns for the IGBT, 290 ns for the SiC MOSFETs and only 260 ns for the Si/SiC Fusion switch. This sensitivity study concludes that the classical signal PWM dead time of 2000 to 3200 ns for IGBT/Diode and 1500 to 2000 ns for SiC MOSFET inverters are safe settings but can be significantly shortened without risk of shoot-though. This comparison also clearly demonstrates that, with the same minimum and maximum tolerances, the impact on PWM dead times is highest for IGBT switches, moderate for SiC MOSFETs, and lowest for Si/SiC Fusion devices. This result is attributed to the fact that the damped behaviour of Si/SiC Fusion allows for low $R_g \cdot C_{ies}$ values, which minimizes the impact on relative timing.

3 | Power Loss vs Dead Time (Calculation)

In inverter power loss simulations, it is common to neglect the PWM dead times and their related power losses when using behavioural models that average over one sinusoidal period [40]. However, in this section, an approach that calculates the additional conduction loss contribution arising from the PWM dead times is introduced. This model can be added as a modular function block to existing state-of-the-art models. The dead time-related conduction losses can be calculated by summing the energy loss during each dead time conduction interval, as shown in Equation (6). In particular, T_0 is the fundamental output frequency, and the integration is carried out only over half of a cycle, where the switch/diode pair is in rectification mode.

$$P_{DT} = \frac{1}{T_0} \int_0^{\frac{T_0}{2}} V(t) \cdot I(t) dt \tag{6}$$

The current follows a sinusoidal shape for both sine (SPWM) and space vector modulated (SVPWM) inverters, as described by Equation (7). For the voltage drop during the dead time, a linearized model can be applied, as shown in Equation (8). The parameter V_{0DT} represents the constant voltage drop during the dead time, while the ohmic voltage drop during the dead time, R_{DT}, depends on the sinusoidal current. Furthermore, the voltage drop occurs only over the time interval of the effective dead times, DT_{eff}, each switching cycle. Note that DT_{eff} is the sum of both effective dead times, $DT1$ and $DT2$.

$$I(t) = I_{pk} \cdot \sin(\alpha) \tag{7}$$

$$V(t) = \left(f_{sw} \cdot DT_{eff}\right) \cdot \left(R_{DT} \cdot I_{pk} \sin(\alpha) + V_{0DT}\right) \tag{8}$$

By plugging the current of Equation (7) and voltage of Equation (8) into Equation (6), and averaging over one fundamental output period, the integral of Equation (9) will be obtained.

$$P_{DT} = \frac{1}{2\pi} \int_0^{\pi} \left(f_{sw} \cdot DT_{eff}\right) \cdot \left(R_{DT} \cdot I_{pk} \sin(\alpha) + V_{0DT}\right) \cdot \left(I_{pk} \cdot \sin(\alpha)\right) d\alpha \tag{9}$$

Due to the linearization, the integral can be solved to the formula of Equation (10). It has to be noted clearly, that effects of potential reduction of dynamic switching losses from both, a potential reduction in diode turn-off energy losses ($\Delta Erec$) as well as reduction in forward recovery diode turn-on energy losses ($\Delta Efrc$) at short diode conduction times, are not implemented in this behavioural model.

$$P_{DT} = DT_{eff} \cdot f_{sw} \sqrt{2} I_{ph} \left(\frac{\sqrt{2} I_{ph} \cdot R_{DT}}{4} + \frac{V_{0DT}}{\pi} \right) \tag{10}$$

To calculate the dead time-related conduction losses, it is essential to apply the appropriate parameters for R_{DT} and V_{0DT}, which represent the difference between passive and active rectification. For an IGBT/Diode power module, both R_{DT} and V_{0DT} are zero, as the active turn-on of the IGBT does not change the conduction characteristics of the antiparallel diodes. Consequently, optimizing PWM dead times will not affect power losses until an overlapping switching (i.e., a transient shoot-through current due to negative effective dead times) occurs. The impact of high dead times on the distortion of the sinusoidal current shape will be addressed in the next section. In contrast, for a SiC MOSFET power module, the difference between passive and active rectification (R_{DT}) can be modelled by the difference between the body diode resistance (R_d) and the on-state resistance (R_{dson}), as shown in Equation (11). A similar method is applied to model the constant voltage drop, where V_0 represents the drop of the body diode pn-junction, whereas in the active on-state, the MOSFET has no pn-junction drop (see Equation 12). The numeric values for the DUT FS01MR08A8MA2 at room temperature are provided as an example.

$$R_{DT} = R_d - R_{dson} = 1.95\ m\Omega - 1.03\ m\Omega \tag{11}$$

$$V_{0DT} = V_0 - 0 = 3.2\ V \tag{12}$$

Using the model and the exemplary parameters, the dead time-related conduction losses of a SiC MOSFET power module are illustrated in Figure 7. Due to unmodeled dynamic effects, the actual power loss savings achievable in practice are to be even higher, as will be demonstrated later in Section 4.

In the case of a Si/SiC Fusion power module, the difference between passive and active rectification (R_{DT}) can be modelled by considering the different output characteristics of the antiparallel silicon diode and the on-state resistance (R_{dson}) of the SiC MOSFETs. This is graphically illustrated in Figure 8.

Due to the significantly larger pn-junction voltage drop of the SiC MOSFET body diode compared to the Si diode, it is possible to entirely neglect the SiC MOSFET body diode, at least for normal operating currents of the inverters.

$$R_{DT} = R_{sid} - R_{dson} = 0.6\ m\Omega \tag{13}$$

$$V_{0DT} = V_{si0} - 0 = 1.05\ V \tag{14}$$

The numeric values for the DUT FS980R08A7FU32 at room temperature are provided as an example in Equations (13) and (14). Using these parameters and the model described in Equation (10), the dead time-related conduction losses for a Si/SiC Fusion power module can be calculated (see Figure 9), neglecting the effects of reduced recovery charge of rectifier diodes in cases of short conduction times.

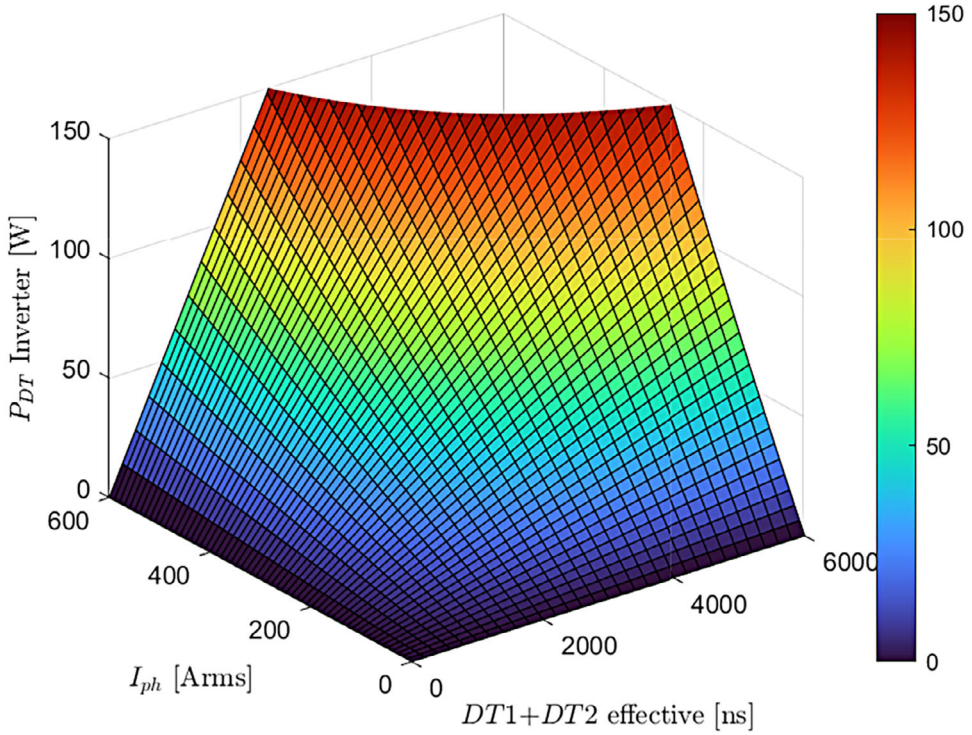


FIGURE 7 | Calculated dead time related condition losses per topological switch for a SiC MOSFET power module according model of Equation (10) with parameters of (Equations 11 and 12).

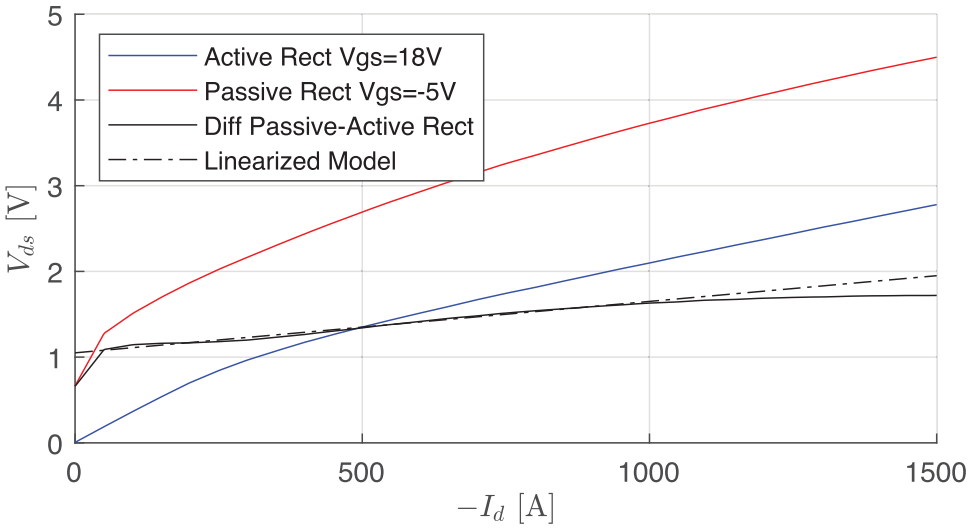


FIGURE 8 | Static output characteristics of Si/SiC Fusion switch in active and passive rectification mode as well as the difference.

4 | Power Loss vs Dead Time (Measured)

In this section, inverter systems with the three different switch types were operated in open loop on an inductive load. The test conditions for this experimental testing are noted in Table 2. Appendix B shows pictures of the test setup and Appendix C provides a detailed equipment list and settings for applied data acquisition. The Microcontroller set constant and equal signal dead times $DT1_{sig} = DT2_{sig}$ for each operating point. For each measurement, the modulation index, output frequency, etc., was kept constant after a 100 ms soft-start ramp. The power losses were measured by the power analyzer within the steady state operation. Each measurement was repeated with a reduction of signal dead times until the power losses showed a substantial increase.

4.1 | IGBT/Diode: Power Loss vs Dead Time

As anticipated in Section 3, optimizing the PWM signal dead times does not improve the power losses in IGBT inverters. In fact, applying "too short" dead times can generate additional

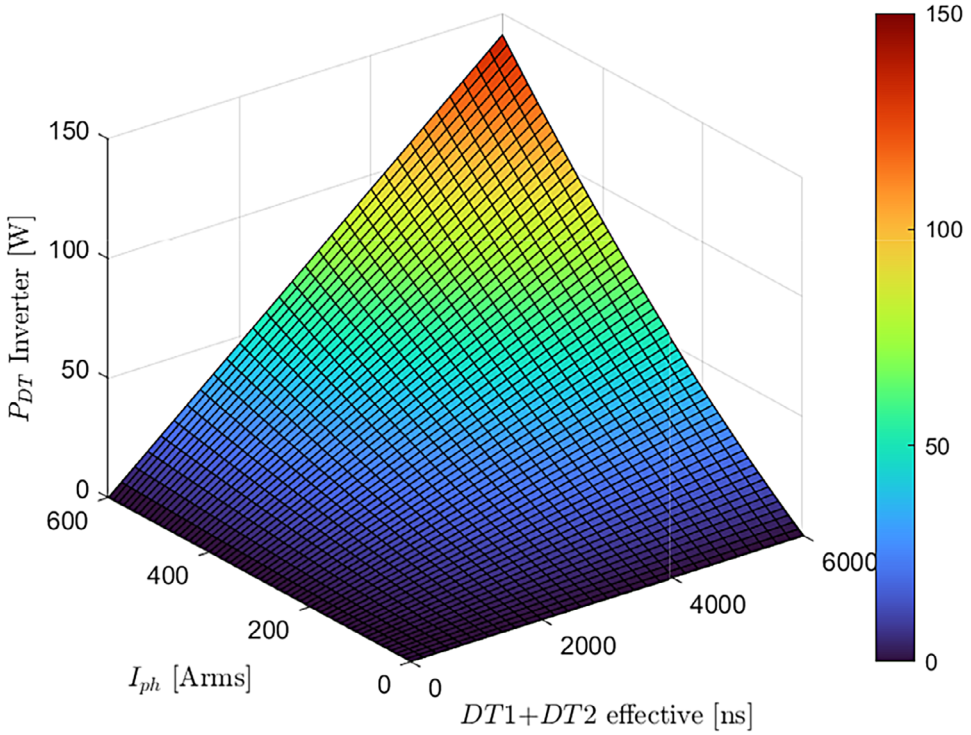


FIGURE 9 | Calculated dead time related condition losses per topological switch for a Si/SiC Fusion power module according model of (Equation 10 with parameters of Equations 13 and 14).

TABLE 2 | Standard test conditions.

Condition	Value	Unit
Topology	B6	
Modulation	SVPWM	
DC working voltage	450	V
Switching frequency	10	kHz
Output frequency	100	Hz
Coolant temperature	65	°C
Coolant flow	10	L/min
Coolant mix	50/50	%/%[a]
PF	≈ 0..0.1	
modidx	≈ 1	% per Arms
Measurement duration	≈ 8..12[b]	s

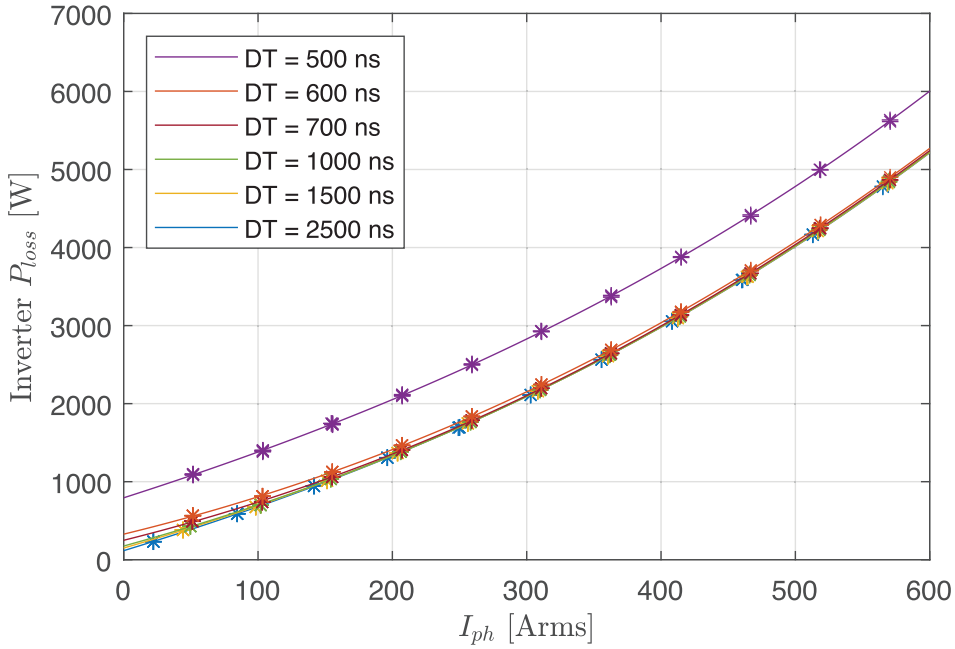
[a]Ethylene-glycol (G12evo)/water mixture.

[b]Steady state is achieved after about 5 s. The inverter power loss measurement is performed after steady state reached. During the run-time no parameters are adjusted to ensure stable conditions.

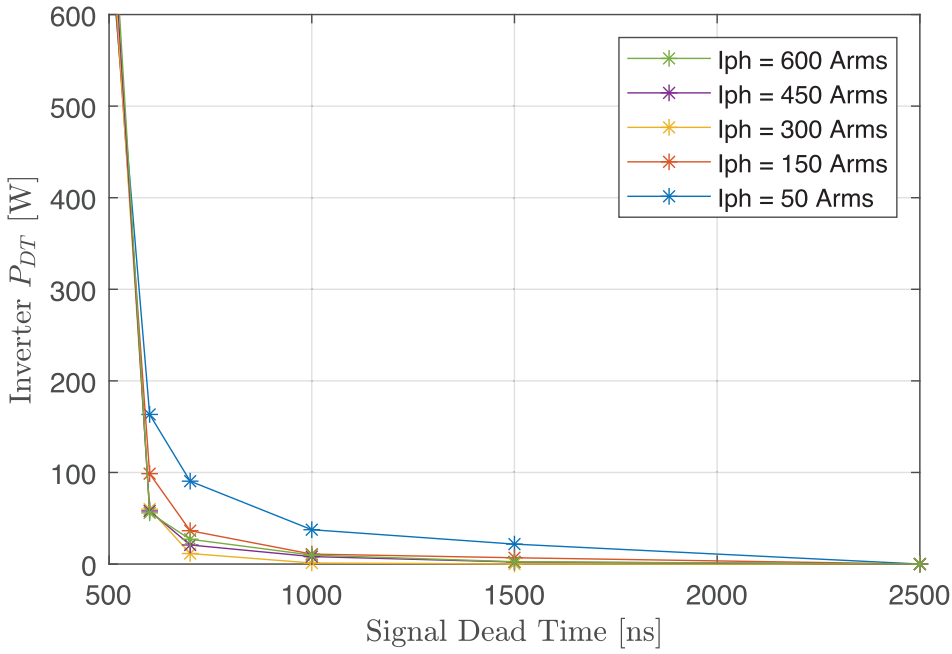
power losses due to slight overlapping switching, as evident in the measured diagram of Figure 10a. To illustrate the influence of PWM dead time related power losses, the minimum achieved total power losses of the inverter system at each operating current were subtracted from the plot and resulted in Figure 10b. Consistent with the sensitivity analysis of Section 2.4, the lowest currents (corresponding to low Miller plateau voltage $V_{plateau}$) and highest working voltages (resulting in high Miller charge Q_{Miller}) are the most critical for PWM dead times. As a result, the power loss increase at reduced dead times is first observed at low currents, before it becomes apparent at higher operating currents as it can be seen in Figure 10a.

4.2 | SiC MOSFET: Power Loss vs Dead Time

The same approach used for IGBT switches was applied to SiC MOSFET inverter power modules, resulting in the total power loss data presented in the diagram of Figure 11a. Similar to IGBTs, reducing PWM dead times in SiC MOSFETs leads to increased power losses, particularly at low currents (combined with high working voltages). This is evident when comparing the 100 ns power loss curve to higher dead time values at currents below 150 Arms. Additionally, at high currents, it is clear that very long dead times (e.g., 2500 ns) with prolonged conduction times of the SiC MOSFET body diodes result in high power losses, especially for currents above 400 Arms. By subtracting the minimum total achieved power losses over PWM dead times and plotting the PWM dead time-related power losses, the results become more insightful, as shown in Figure 11b. Reducing body diode conduction times from classical 2000 ns to optimal short PWM dead times decreases power losses of the inverter system by nearly 15%. At high currents, the improvements are significantly greater than predicted with the conduction loss related improvements in Section 3. This led to the conclusion that a major contribution of dead time related losses might also come from a modified body diode recovery charge and turn-off energy (Qrr and Erec), which was further investigated in Section 4.2.1. Even with a reasonable safety margin of 200 ns, which accounts



(a) Total inverter system power losses at different PWM signal dead times. The increasing power loss starts at low currents first.



(b) Dead time related power losses from Fig 10a. The minimum measured power losses were set to 0 W to illustrate only the PWM dead time related power losses.

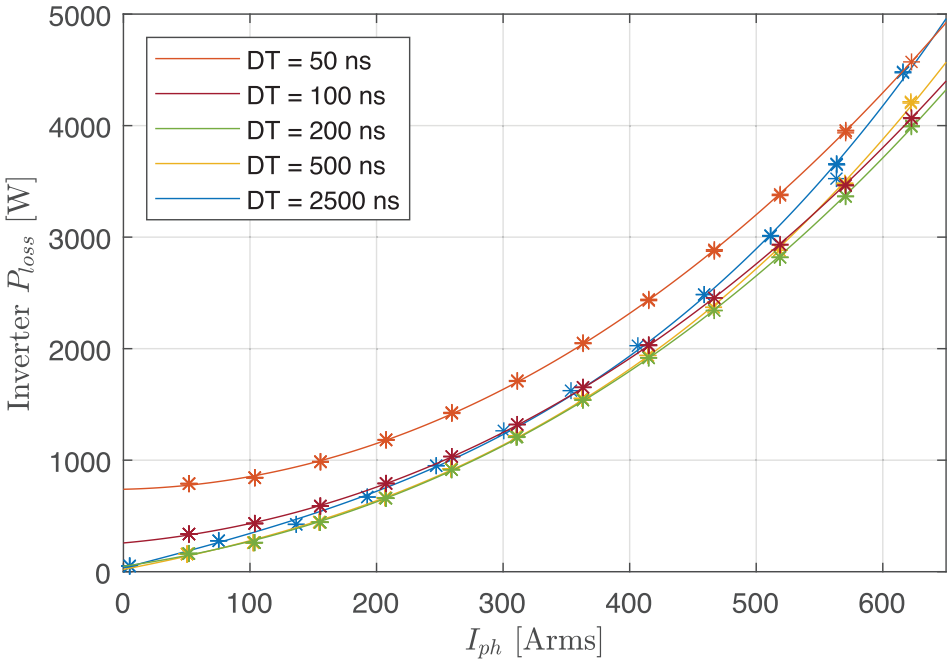
FIGURE 10 | IGBT Inverter 450 V, 10 kHz.

for part-to-part tolerances, a total inverter power loss reduction of substantially more than 5% is achievable.

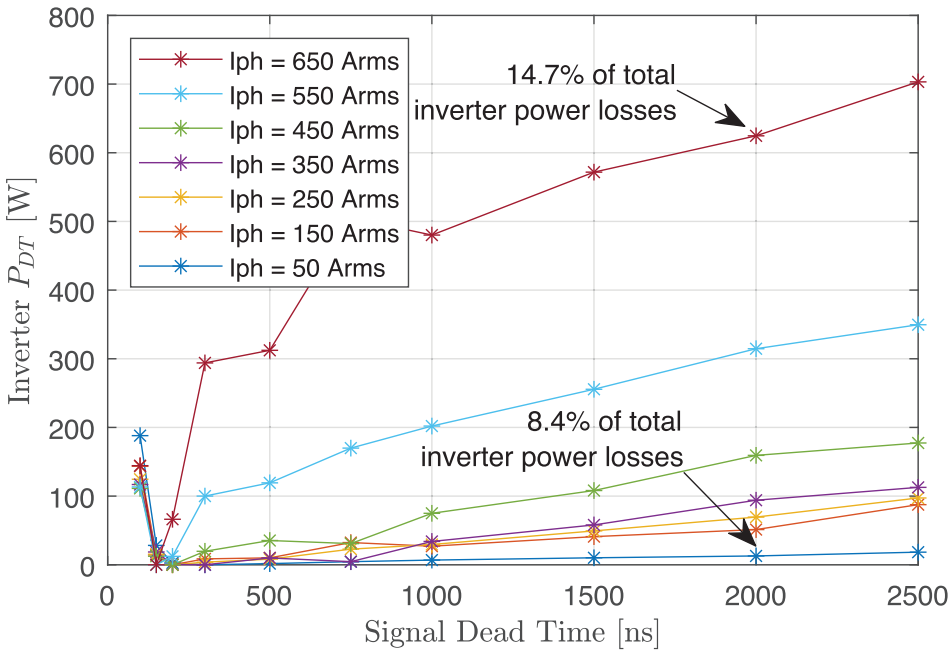
In summary, PWM dead times in SiC MOSFET-based inverters should be carefully designed to be robust against shoot-through events while also being short enough to ensure efficiency and prevent prolonged body diode conduction times.

4.2.1 | SiC MOSFET: Erec vs Dead Time

Due to the unexpectedly high power loss reduction observed at short PWM dead times, a detailed analysis of the active rectification turn-off ($DT2$) was conducted. This involved recording the switch voltage and current waveforms with equipment and data acquisition noted in Appendix C. Figure 12 presents an overlay



(a) Total inverter system power losses at different PWM signal dead times. For lower than 200 ns the increasing power losses at low currents are visible.



(b) Dead time related power losses from Fig 11a. The minimum measured power losses were set to 0 W to illustrate only the PWM dead time related power losses.

FIGURE 11 | SiC MOSFET inverter 450 V, 10 kHz.

of several waveforms, showcasing the transition from long to short signal dead times at 450 V and 850 A. For signal dead times longer than 200 ns, the measured waveforms exhibit similar characteristics in terms of voltage and current overshoot. The 100 ns short signal dead time has the switching event before the gate clamp is reached, resulting in a reduction of the voltage overshoot during commutation. This behaviour is caused by a nearly direct commutation from one MOSFET channel to the other. However, all waveforms show energy losses (*Erec*) of a similar magnitude, which cannot account for the power loss reduction measured by the power analyzer during the inverter operation depicted in Figure 11b. This discrepancy led to the

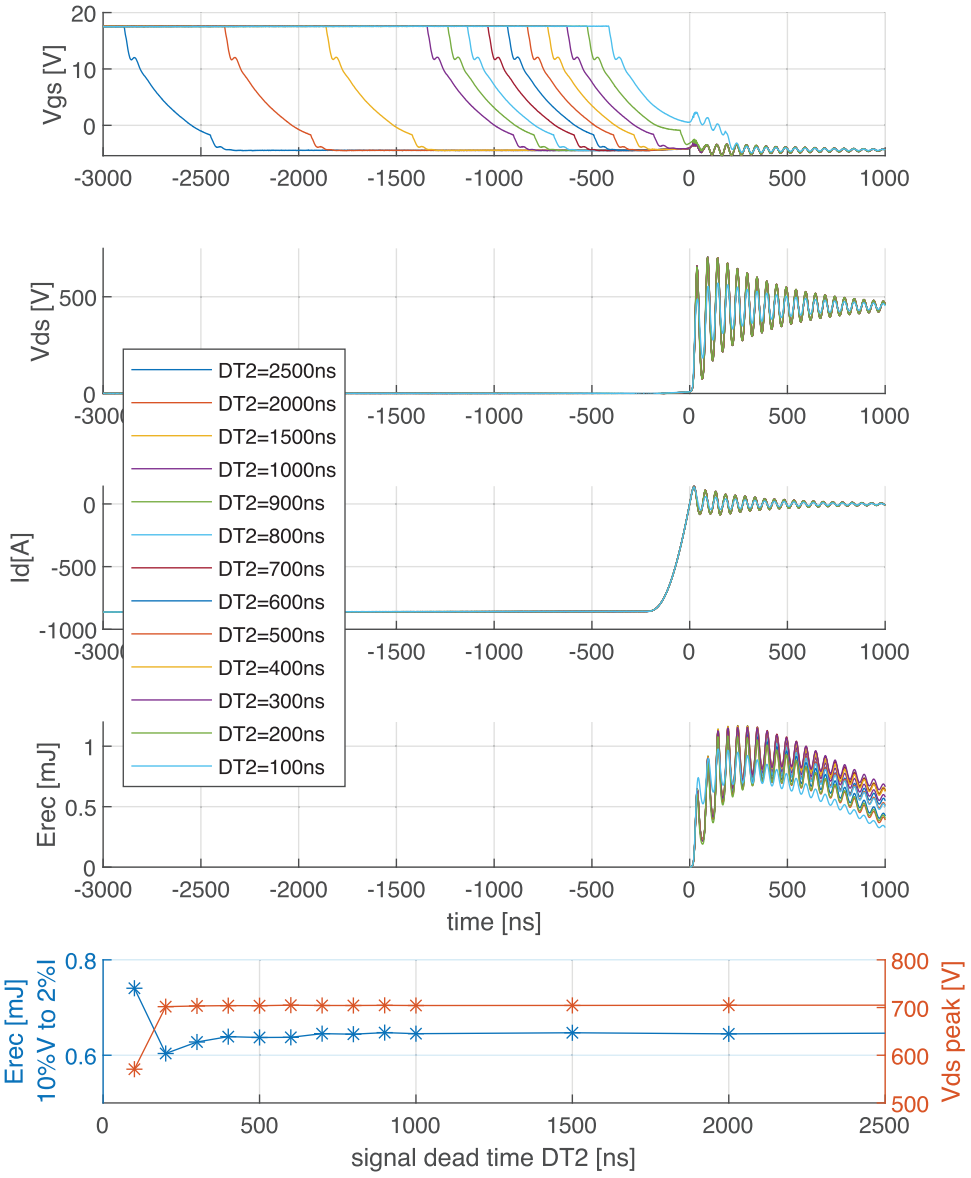
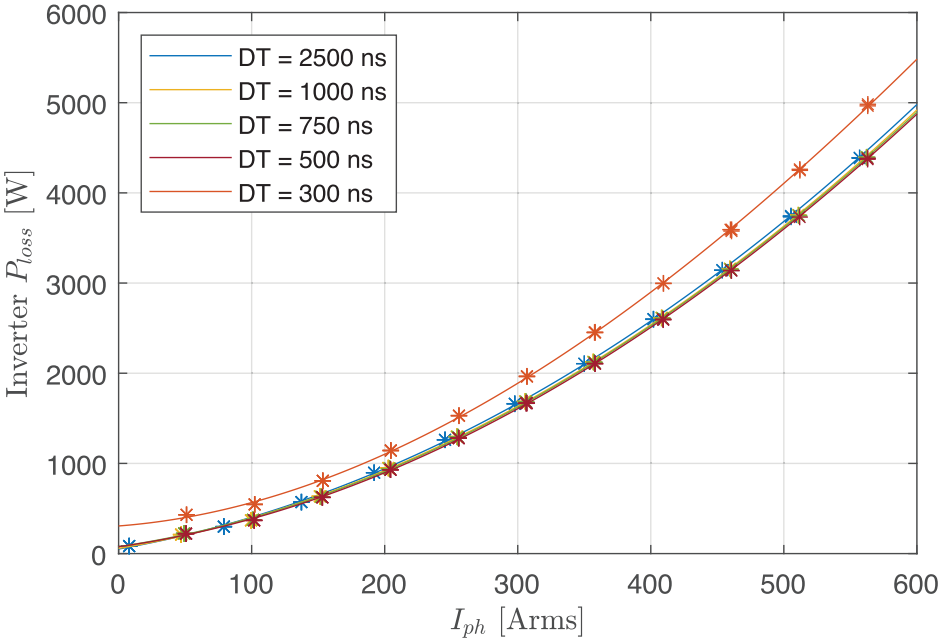


FIGURE 12 | Double pulse test waveforms of SiC MOSFET active rectifier turn-off at 450 V, 850 A, and different signal PWM dead times $DT2$. The energy losses per pulse ($Erec$) are nearly constant and low in magnitude.

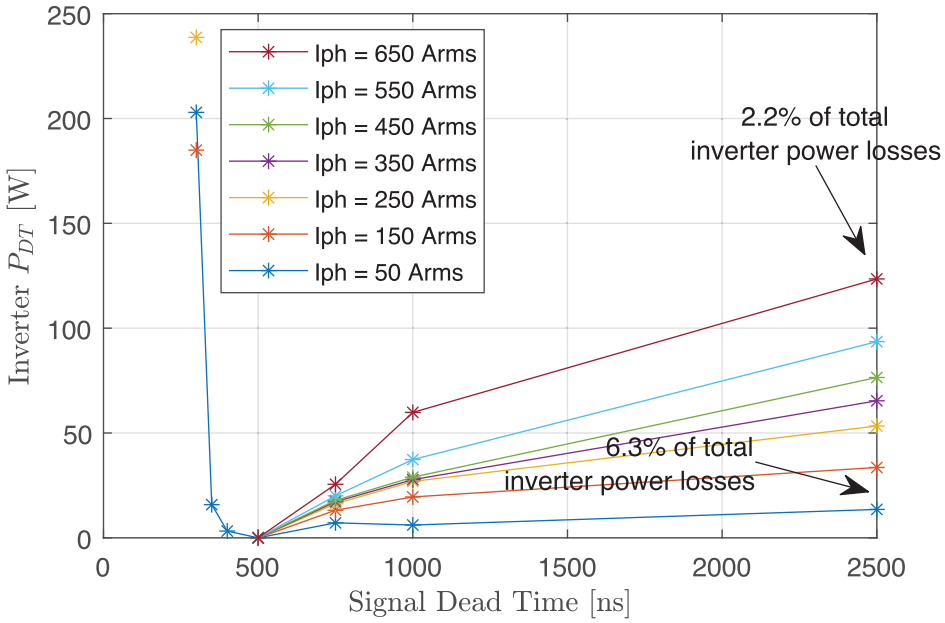
conclusion that other factors contribute to these power losses. Research studies have focused in the past on the 3rd quadrant operation, particularly for non-switching active short circuit safe-state operation [41, 42], and static conditions [43, 44] as well as the diode turn-off behaviour similar to 12 under different conditions. However, the topic of high current density body diode turn-on and the dynamic transition into channel operation has not been adequately addressed in research and might contribute to understanding the root cause for the high impact of dead time related power losses with increasing current densities.

4.3 | Si/SiC Fusion: Power Loss vs Dead Time

The total power loss data for Si/SiC Fusion inverters at various PWM signal dead times is presented in Figure 13a, while the relative dead time related power losses are shown in Figure 13b. The Fusion switch exhibits a stable optimum between 450 and 500 ns signal dead time, which was also utilized in [38] for a method of active DC-link capacitor discharge at the vehicle key-off event. The power loss reduction from 2500 ns to 1000 ns is consistent with the predicted improvement outlined in Section 3. However, an additional effect comes into play when the signal dead time is further reduced from 1000 ns to the optimal value. In Si/SiC Fusion switches, the silicon diodes conduct, and the contribution from the SiC body diode can be neglected during the effective dead times. For low conduction times of the silicon diodes, the charge carrier plasma is not fully built up, resulting in a reduction of the recovery charge of the silicon diodes similar to [45]. Consequently, short conduction times lead to a further decrease in power losses and advantageous recovery behaviour. With the PWM dead time related power losses contributing 2%–6% to the total inverter power losses, optimizing the dead time is crucial for efficient and reliable inverter operation.



(a) Total inverter system power losses at different PWM signal dead times. Slight overlap lead to increased losses especially at low load. At high load the increased losses are due to the higher device temperature which lowers the gate threshold characteristics.



(b) Dead time related power losses from Fig 13a. The minimum measured power losses were set to 0 W to illustrate the dead time related losses.

FIGURE 13 | Si/SiC fusion inverter 450 V, 10 kHz.

4.3.1 | Si/SiC Fusion: Thermal Impact of Dead Time

During the investigation of inverter operation, the impact of varying current distributions at different signal dead times was also examined. Figure 14 illustrates the measured temperatures within the Si/SiC Fusion power module, presented as a thermal difference image. Both the diode and SiC MOSFET chips exhibit a thermal resistance (Rth) junction to fluid of approximately 0.35 K/W in this application example. An increase in signal dead times from 600 ns to 2500 ns resulted in the diodes being 8.2 K hotter and the SiC MOSFETs being about 1.2 K cooler in this specific example. To calculate the additional losses in the total

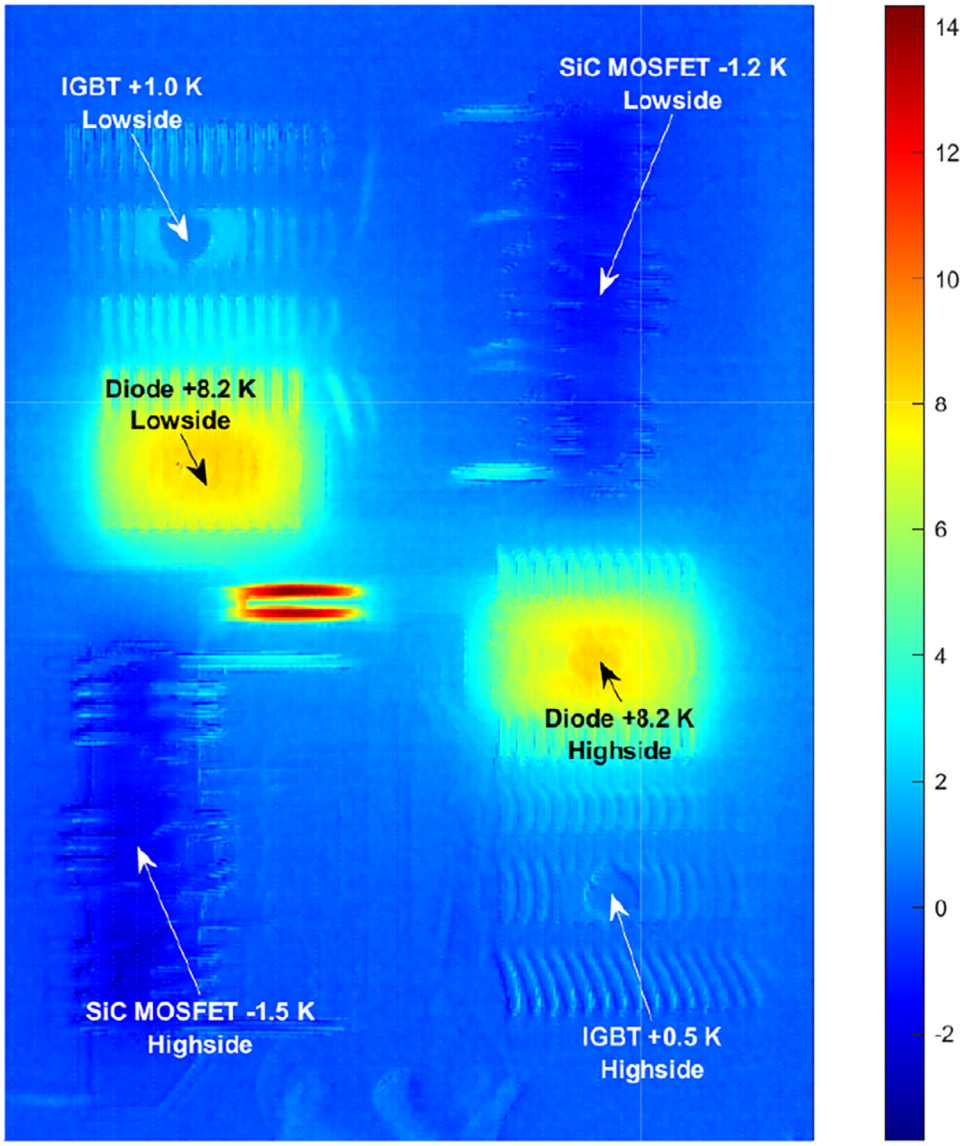


FIGURE 14 | Thermal IR Picture of Si/SiC Fusion power module at 450 V, 575 Arms, 10 kHz. The picture is an IR difference picture from two steady state measurements. The first IR picture was taken at 2500 ns and the second at 600 ns signal dead times. Positive temperatures [K] are hotter areas in case of the long dead times.

inverter, we can use the thermal images, applying the formula $P_{DT\_2500ns\_600ns} = 6 * (dT/Rth) = 6 * (8.2\ K - 1.2\ K)/0.35\ K/W$. This calculation yields a value of 120 W, which closely matches the measurements obtained using the Power Analyser, as detailed in Section 4.3. Furthermore, reducing the temperature swing of the diodes of nearly 10 K at high load condition is expected to contribute significantly to extending the power cycling application lifetime of the power modules [46]. This outcome underscores the importance of optimizing signal dead times in inverter operation to achieve better thermal management and, by extension, improved module durability.

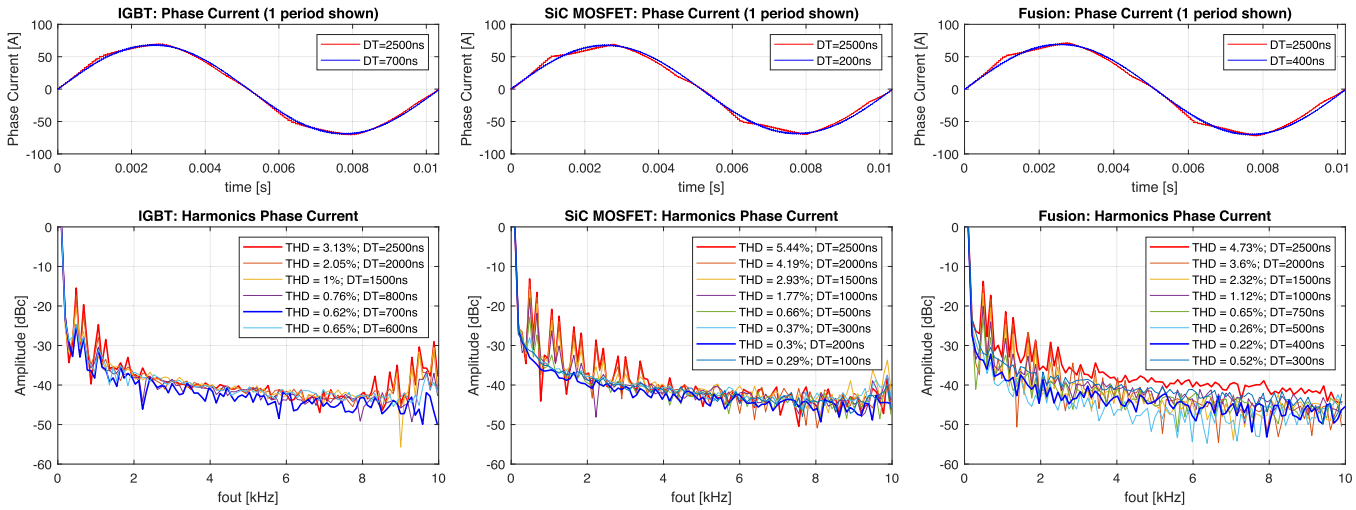
4.4 | Summary: Power Loss vs Dead Time

In both SiC and Si/SiC Fusion switch-based inverters, the reduced power losses at optimized dead times were substantial, ranging from about 5%–15%. Especially for SiC MOSFETs, the experimental data revealed an unexpectedly high optimization potential with respect to conventional PWM timings as applied today.

Assuming a standard vehicle driving profile of 15,000 km of per year, and a typical inverter energy loss without optimized dead times of 0.4 kWh per 100 km of driving, an PWM dead time optimization with a 10% power loss reduction would result in an annual energy saving of approximately 6 GWh per 1 million vehicles. Given this high energy-saving potential, more focus and research should be done to optimize PWM dead times in the traction inverters.

5 | Inverter Output Harmonics (Open Loop)

The PWM dead times, which result in voltage drops, not only cause power losses but also introduce harmonics into the output waveform. A common figure of merit used to evaluate the quality



(a) With IGBT/Diode power module. (b) With SiC MOSFET power module. (c) With Si/SiC Fusion power module.

FIGURE 15 | Measured output harmonics at different PWM signal dead times at 450 V, 10 kHz.

of the output waveform is the total harmonic distortion (THD). In this comparison, the focus is on the inverter phase currents during constant open-loop operation. The THD of the measured current signal can be calculated using Equation (15), where the fast Fourier transform (FFT) of the current signal provides the input for the currents with the index i for the harmonic order.

$$THD[\%] = 100 \cdot \frac{\sqrt{\sum_{i=2}^{\infty} I_i^2}}{I_1} \tag{15}$$

For this comparison, harmonics up to the switching frequency of 10 kHz were considered (i.e., the first 100 harmonics). The current signal was recorded using a high-resolution LeCroy 8208HD scope with high bandwidth (see also Table C1) and filtered in post-processing with a 1 MHz filter before performing the FFT and THD calculation. The signal filter with 100 times higher bandwidth compared to the highest harmonic under consideration will not remove potential sidebands. The operating point of 50 Arms at 450 V, close to 100 Hz, was chosen because this light load condition is relevant to electric car driving profiles (see also [34, 36]), and THD is more critical at light load compared to full load operation. The open loop test was performed on three-phase load of 250 μH inductance with same conditions as noted in Table 2.

5.1 | IGBT/Diode

Figure 15a illustrates one of the 10 measured output periods of the IGBT/Diode inverter, comparing the results for a long signal dead time of 2500 ns and a near-optimal dead time of 700 ns. A visual comparison of the two current waveforms reveals a higher harmonic contribution at the longer dead time, in contrast to the nearly ideal sinusoidal current waveform achieved with the optimized "low" dead time. The improvements are further evident in the fast Fourier transform (FFT) generated frequency spectrum, which includes the resulting total harmonic distortion (THD) values. An THD improvement of 2%–3% was possible by optimized dead time in the IGBT/Diode inverter system.

5.2 | SiC MOSFET

The influence of PWM dead times on harmonics is significantly more pronounced in SiC MOSFETs compared to IGBT/Diode power modules, as evident from a comparison of Figures 15a and 15b. The root cause is the high voltage drop of the SiC MOSFET body diode compared to the active freewheeling mode. Notably, a 5% reduction in total harmonic distortion (THD) can be achieved by dead time optimization.

5.3 | Si/SiC Fusion

The influence of PWM dead times on harmonics in Fusion power modules, as illustrated in Figure 15c, is more pronounced compared to IGBT/Diode power modules, but slightly less significant compared to SiC MOSFET modules. As expected, the Fusion switch achieved the lowest total harmonic distortion (THD) values at optimized dead times, owing to its extremely stable dead times across varying operating conditions. This stability is a result of the fast yet smooth switching behaviour of the Si/SiC Fusion switches. A notable reduction in THD of more than 4% was achieved.

5.4 | Summary of Harmonics Comparison

Optimized PWM dead time is beneficial for reducing harmonics in all switch types investigated. However, modern device types, such as SiC MOSFETs and Si/SiC Fusion switches, exhibit a greater impact of PWM dead times on harmonics under the same operating conditions. Besides the demonstrated light load improvements it is worth noting that lower signal PWM dead times increases also maximum possible DC-link voltage utilization at a high modulation index. Lowering signal dead time of each 100 ns will account for 0.2% higher working voltage utilization until the DC+/- clipping begins. Clipping occurs when the combined duration of dead time and turn-on period exceeds the period of the PWM switching pattern.

The reduction in output harmonics can lead to additional benefits in machine and vehicle transmission systems. In particular, the lower THD values result in reduced torque ripple, which is expected to reduce power losses in these systems, in addition to the inverter power electronics.

6 | Summary and Conclusion

Up to the current state-of-the-art, PWM dead times have not been a focus for automotive traction inverters operating at 10 kHz. The effect of dead time on overall system performance has been minor when using IGBT/Diodes. Therefore, inverter designers would typically continue using dead times of more than 1 µs in such systems. However, the calculated improvements in dead time-related power losses were found to be significantly overachieved in SiC MOSFET-based inverters and slightly in Si/SiC Fusion switch-based inverters. Experimental results demonstrated that optimized PWM dead times can account for more than 10% of total inverter system power losses at typical automotive switching frequencies of 10 kHz.

Given the substantial power loss reduction observed in SiC MOSFET inverters, future research is recommended to focus on the dynamic turn-on and turn-off of the 3rd quadrant operation. The improvements in power losses also contribute to lower thermal stress, as evidenced by lower diode temperatures (nearly 10 K at high load conditions) in a Si/SiC Fusion switch inverter. This reduction in thermal stress is also beneficial for the power cycling reliability of the power modules.

The article also evaluates the influence of PWM dead times on inverter output current harmonics under open-loop light load conditions. The results indicate that optimized PWM dead times can reduce total harmonic distortion by up to 5%. This reduction is significant, as it leads to lower torque ripple and power losses at the electric drive train beyond the inverter system, providing a substantial benefit in vehicle systems.

The findings highlight the importance of considering the specific characteristics of different switch types and the potential for significant improvements in power loss reduction by optimizing the PWM dead times. Future studies should continue to explore this optimization area to further enhance the efficiency and reliability of inverter systems. For example, optimizing PWM dead times during application run-time, particularly in cases utilizing adaptive gate drive methods, can be beneficial. In such methods, the switching speed and consequently the PWM dead times can vary during run-time, offering opportunities for dynamic optimization. The introduced analytical approach of this article, including sensitivity analysis for IGBT/Diode, SiC MOSFET, and Si/SiC Fusion switch inverters, provides a solid basis for future research and optimization methods.

Author Contributions

Tomas Reiter: conceptualization, formal analysis, investigation, methodology, software, visualization, writing – original draft. **Julius Schapdick:** investigation, validation, writing – review & editing. **Michael Krug:** conceptualization, validation, writing – review & editing. **Mark Muenzer:** methodology, resources, writing – review & editing. **Frank Wolter:** methodology, supervision, writing – review & editing.

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Conflicts of Interest

The authors declare no potential conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available on request from the authors.

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Appendix A: Parameters: Device Under Test

Table A1 lists the switch technology and die areas of the device under tests (DUT) within the studies of this article. The PWM dead time sensitivity analysis was exemplarily performed with the data of Table A2 taking into account an off-the shelf automotive gate driver 1EDI3035AS with public available datasheets of the power modules and gate drivers.

TABLE A1 | Switch technology and implemented die area per topological switch.

Technology part no	IGBT	Diode	SiC MOSFET
IGBT/diode FS1150R08A8P3B	320 mm^2	180 mm^2	—
SiC MOSFET FS01MR08A8MA2B	—	—	200 mm^2
Si/SiC fusion FS980R08A7F32B	160 mm^2	60 mm^2	60 mm^2

TABLE A2 | Parameters applied for the sensitivity study.

Parameter	Tech	min[a]	typ	max[a]
$VCC1$	n.a.	−5%	5.0 V	+5%
$V_{in\_th\_high}$	n.a.	$V_{in\_th\_low}$	1.55 V	2.0 V
$V_{in\_th\_low}$	n.a.	0.8 V	1.35 V	$V_{in\_th\_high}$
R_s	n.a.	−1%	2*470 Ω	+1%
C_{in}	n.a.	−5%	100 pF	+5%
t_{PDon1}	n.a.	55 ns	60 ns	90 ns
t_{PDoff1}	n.a.	55 ns	60 ns	90 ns
$VCC2$	IGBT; SiC; Fusion	−5%; −5%; −5%	15 V; 18 V; 18 V	+5%; +5%; +5%
$VEE2$	IGBT; SiC; Fusion	−5%; −5%; −5%	−8 V; −5 V; −5 V	+5%; +5%; +5%
Rg_{on}	IGBT; SiC; Fusion	−2%; −2%; −2%	2.2 Ω; 6.8 Ω; 1.27 Ω	+2%; +2%; +2%
Rg_{off}	IGBT; SiC; Fusion	−2%; −2%; −2%	5.6 Ω; 3.3 Ω; 1.5 Ω	+2%; +2%; +2%
V_{clamp}	IGBT; SiC; Fusion	−5.8 V; −2.8 V; −2.8 V	−6.0 V; −3.0 V; −3.0 V	−6.2 V; −3.2 V; −3.2 V
C_{ies}	IGBT; SiC; Fusion	−10%; −10%; −10%	60.8 nF; 43.0 nF; 43.3 nF	+10%; +10%; +10%
V_{geth}; V_{gsth}; V_{gsth}	IGBT; SiC; Fusion	4.9 V; 3.2 V; 3.2 V	5.8 V; 3.9 V; 3.9 V	6.65 V; 4.55 V; 4.55 V
Rg_{int}	IGBT; SiC; Fusion	−10%; −10%; −10%	1.0 Ω; 0.53 Ω; 1.0 Ω	+10%; +10%; +10%
$V_{plateau}$	IGBT; SiC; Fusion	V_{geth_min}; V_{gsth_min}; V_{gsth_min}	8 V; 7 V; 7.5 V	10.0 V; 8.8 V; 10.0 V
Q_{miller}	IGBT; SiC; Fusion	−10%; −10%; −10%	0.8 µC; 0.4 µC; 0.52 µC	+10%; +10%; +10%

[a]Relative values related to the typical value.

Appendix B: Setup Pictures

Figure B1 shows the applied DUTs power module in top view. The picture shows one single half-bridge of each switch technology under investigation. The experiments were performed with three identical half-bridges forming the B6 bridge power modules. The DUTs use the same thermal stack for all switch configuration with following data: chips attached by 15 µm Ag sinter layer to 320 µm SiN substrate with 300 µm topside and bottom side copper. The substrate is attached by 350 µm solder layer to a 3 mm thick copper baseplate with 6 mm long PinFin structure directly cooled by the liquid cooling system.

Figure B2 shows the test setup applied for the inverter testing. The #1 4 mm plugs are the voltage probe connections of the power analyzer; #2 are the voltage probes and the Rogowski current coil for the oscilloscope switching waveform recording according to Table C1; #3 is the coolant inlet; #4 the gate driver board with open design and production files on request; #5 the DC-link capacitor; #6 rapid prototyping control platform for open loop tests based on Arduino Nano system to simplify design file and software sharing on request (remark: with the Arduino Nano system the inverter system has a frequency control of worse than 0.2% and therefore does NOT fall under the 3A225 of EC dual-use regulation).

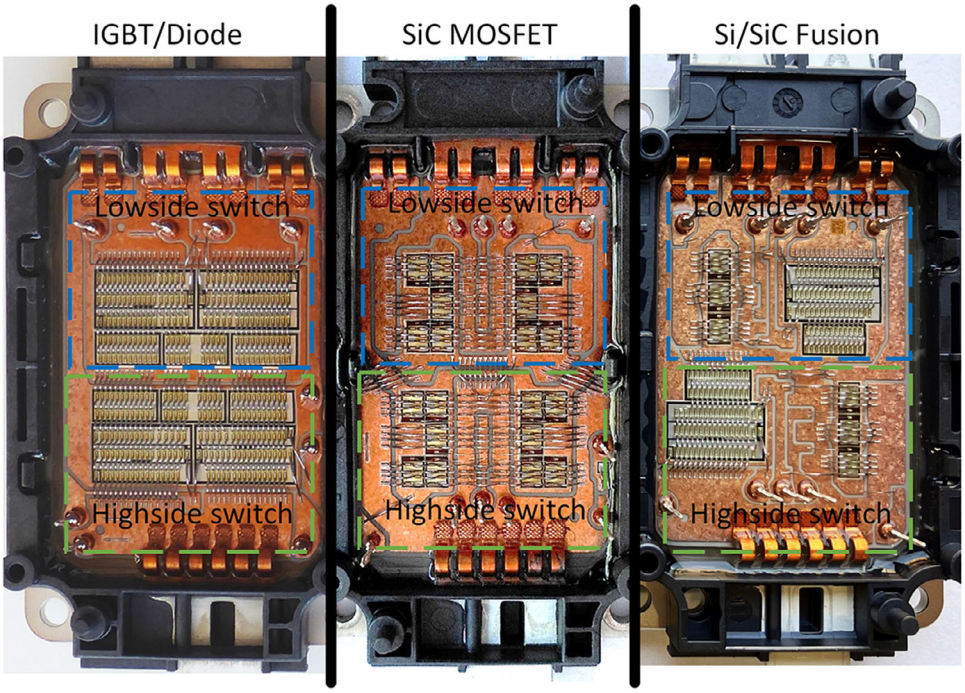

FIGURE B1 | Power module layout of device under tests. Each switch technology is shown with one third of the symmetric B6 bridge.

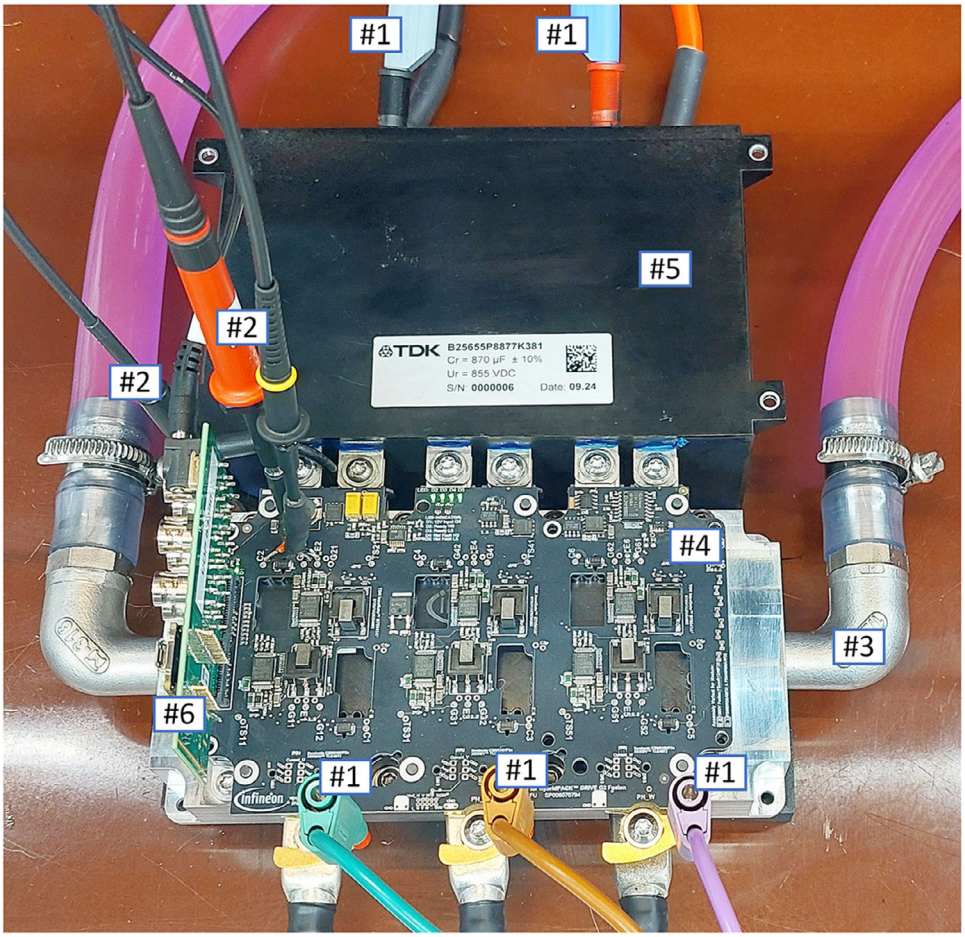

FIGURE B2 | Inverter test setup for open loop testing.

Appendix C: Equipment List

TABLE C1 | Equipment list for the experimental testing.

Device	Manufacturer, type	Bandwidth	Range, attenuation	Acquisition	Measurement
PowerAnalyzer	ZES, LMG671, L60-CH-A2[a]	10 MHz	autorange	500ms; LP:150 kHz; HP:off sync LP:15 kHz; Level: 0% Hyst: 2%	Chapter 4, except Figure 12
Probe $I_{U,V,W}$	ZES, PCT600	500 kHz	max 1000 Arms		
Probe I_{DC}	ZES, PCT600	500 kHz	max 500 Arms (2 turn)		
Supply I_U	EA, PSB11000-80				all
3ph Load	Schmidbauer, 17597A	—	900 Arms; 250 µH		all, except Figure 12
Cooling	Julabo, FL4003[a]				
Flow Rate	Vortex, AS007				
Scope	Lecroy, WaveRunner 8208HD[a]	2 GHz		625 MS/s, +3bit res bw limit: 20 Mhz, no averaging record length 0.1 sec post proc.: LP filter 1 MHz	Chapter 5
Probe I_U	CWT, Mini50HF 15/B[b]	50 MHz	20A/Div, 20 mV/A		
Scope	Lecroy, WaveRunner 8208HD[a]	2 GHz		10 GS/s, +1.5bit res bw limit: 350 Mhz, no averaging	Figure 12
Probe V_{ds}	Lecroy, HVP120[b]	400 MHz	100V/Div, 1:100		
Probe V_{gs}	Lecroy, PP021[b]	500 MHz	5V/Div, 1:10		
Probe I_{ds}	CWT, Mini50HF 15/B[b]	50 MHz	200A/Div, 2 mV/A		
Load	Aircoil, IF02906	—	6..250 µH		

[a]Within vendor calibration interval.

[b]Descew and probe compensation checked before testing. Tektronics CAL/DESCEW 067-0405-02.