SIEMENS

Microcontroller Components
Technical Support Group Munich
HL MC PD 8

Errata Sheet

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Device : **SAB 80C515 / 80C535**

Marking : **LB**

These parts of the SAB 80C515 / 80C535 can be identified by the letters "LB" below the part number. The parts are mounted in a plastic leaded chip carrier package (P-LCC-68).

This errata sheet describes both the functional problems (see part 1) and the deviations from the electrical and timing specifications (see part 2) known in this step.

If a problem was already introduced with an errata sheet of an earlier step, its initial number is still retained in this errata sheet. Thus, the numerical order of the problems described in the following may contain gaps.

At the end of this document, you will find two history tables showing the problems found in the SAB 80C515 / 80C535 up to now. Changes to the last revision are shaded light grey in the history tables.

1) Functional Problems

The following malfunctions or problems are known in this step:

Problem 1 : **Automatic Start of the Watchdog Timer after Reset**

The SAB 80C515/80C535 LB-Step provides an additional functionality at the pin PE#: an automatic start of the watchdog timer after a hardware reset. This automatic start of the watchdog timer after a hardware reset is executed when pin PE# is held at high level during the rising edge of the RESET# signal (termination of the reset state). A 0-to-1 transition at PE# during normal operating mode will not start the watchdog timer.

If pin PE# is at low level during the rising edge of RESET#, the watchdog timer is not started automatically (common to DA- and LB-Step). In this case it can be started only by software by setting bit SWDT in SFR IEN1 during the normal operating mode of the microcontroller.

If pin PE# is unconnected, it is pulled high internally by a weak pull-up transistor. This is common to DA- and LB-Step too, but in the LB-Step this additionally starts the watchdog timer after the rising edge of RESET#.

Workaround :

When pin PE# is connected to low level, no automatic start of the watchdog timer occurs after a reset operation. Further, during normal operating mode the power saving modes are enabled and can be (if required) disabled by setting PE# to high level.

Note : The next revisions of Data Sheet and User Manual will be updated with the description of the new PE# pin functionality.

1) Electrical- and Timing-Spec. Deviations

The following deviations of electrical and timing parameters from the specification are known in this step:

None.

Functional Problem No.	Marking	Description	Remarks
1	LB	Automatic Start of the Watchdog Timer after Reset	

Table 1: History of Functional Problems

Electrical- / Timing-Deviation No.	Marking	Description	Remarks
6	DA	ADC - DNLE, INLE, Gain, Offset	fixed in LB [1)]
5	BB, CA, DA	ADC - Internal Reference Error	fixed in LB [1)]
4	BB, CA, DA	Input Low Current XTAL2, I_{IL3}	fixed in LB [1)]
3	BB, CA, DA	Logic 0 Input Current, I_{IL}	fixed in LB [1)]
2	BB, CA, DA	V_{IL1} and V_{IH} for EA# pin	fixed in LB [1)]
1	BB	Power Down Current, I_{PD}	fixed in CA and later

Table 2: History of Electrical- and Timing-Spec. Deviations

[1)] see document : SAB 80C515/80C535 LB-Step
Functional Description of the new A/D Converter, DC/AC Specification, V1.1 07.97