Customer training workshop TRAVEO™ T2G Serial Memory Interface (SMIF)

Q3 2022

Target products

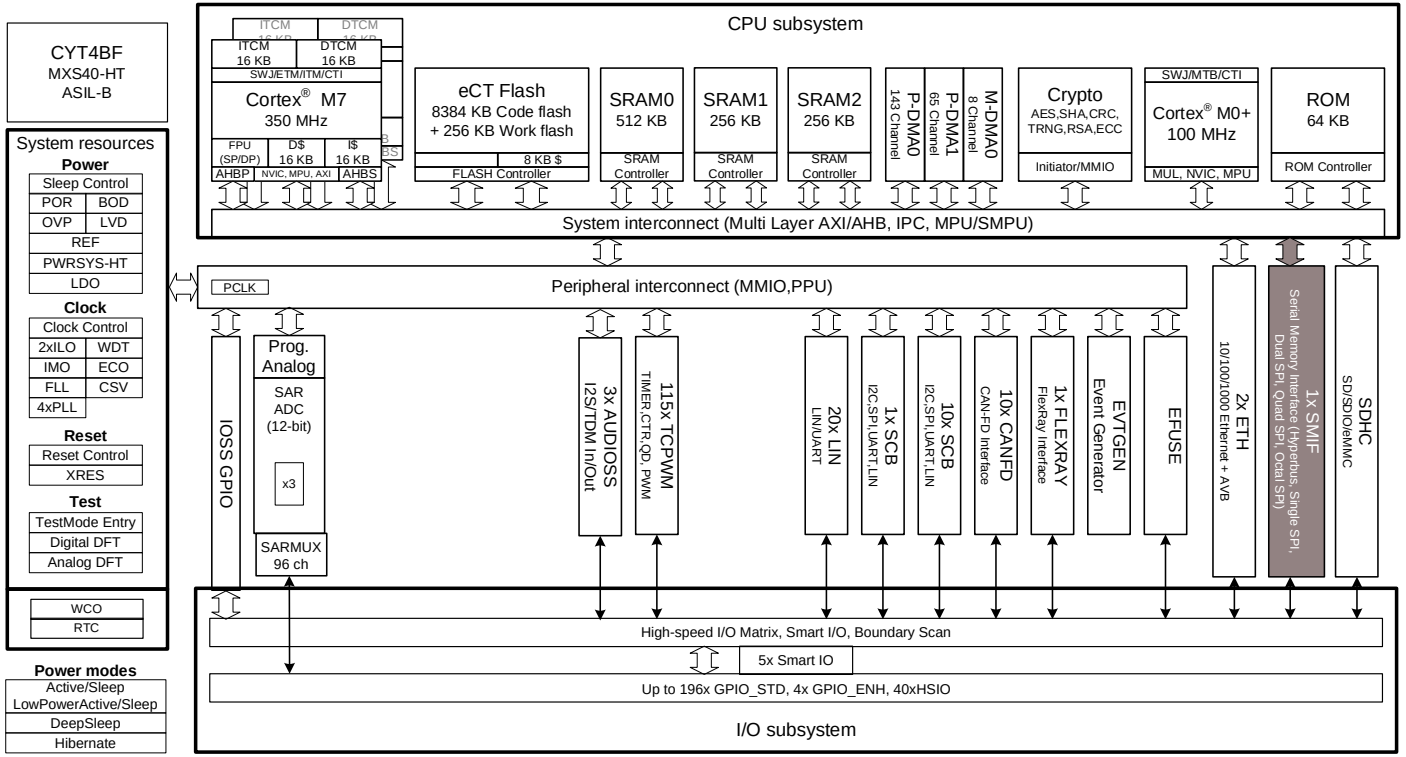
› Target product list for this training material

Family category	Series	Code flash memory size
TRAVEO™ T2G Automotive Body Controller High	CYT3BB/4BB	Up to 4160KB
TRAVEO™ T2G Automotive Body Controller High	CYT4BF	Up to 8384KB
TRAVEO™ T2G Automotive Cluster Entry	CYT2CL	Up to 4160 KB
TRAVEO™ T2G Automotive Cluster 2D	CYT3DL	Up to 4160 KB
TRAVEO™ T2G Automotive Cluster 2D	CYT4DN	Up to 6336 KB
TRAVEO™ T2G Automotive Cluster 2D	CYT4EN	Up to 6336 KB

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Introduction to TRAVEO™ T2G Body Controller High

› SMIF is located in the peripheral blocks



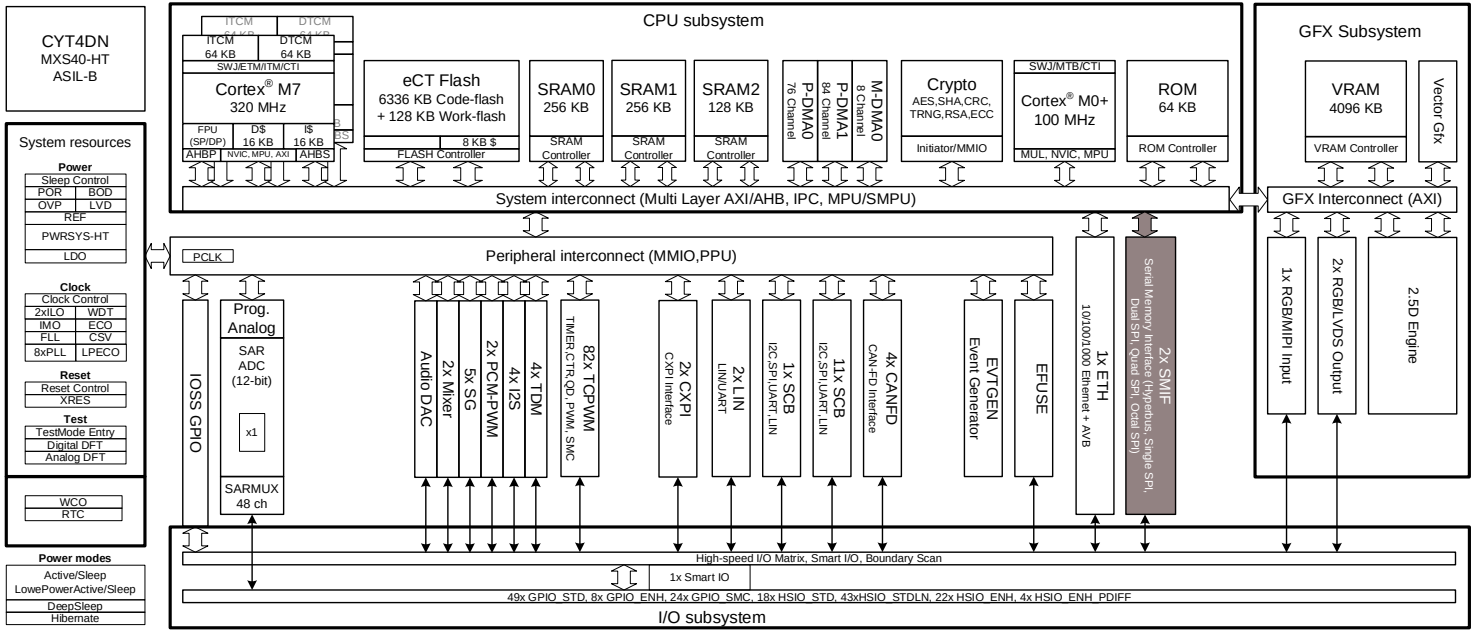
Hint Bar

Review TRM chapter 32 for additional details

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Introduction to TRAVEO™ T2G Cluster

› SMIF is located in the peripheral blocks



Hint Bar

Review TRM chapter 32 for additional details

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Serial Memory Interface (SMIF) overview (1/2)

- SMIF provides an interface to memories with SPI and HYPERBUS™ protocols
- Features
  - SPI or HYPERBUS™ master functionality only
  - SPI protocol
    - Mode 0 only, with configurable Master-In Slave-Out (MISO) sampling timing
    - Single/Dual/Quad/Octal SPI transfer mode
    - Dual-quad SPI mode (two devices sharing one address range)
    - Single Data Rate (SDR) and Double Data Rate (DDR) transfer
  - Two operation modes
    - Memory Mapped I/O (MMIO) operation mode
    - eXecute-In-Place (XIP) operation mode
      - Read and write access
      - Automatic transition access from dedicated internal memory address to SPI protocol
      - On-the-fly encryption and decryption

Hint Bar

Review TRM section 32.1 for additional details

SPI Mode 0:
Data is driven on a falling edge of SPIHB_CLK

Data is captured on a rising edge of SPIHB_CLK

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Serial Memory Interface (SMIF) overview (2/2)

- Features
  - Memory device
    - Device capacity in the range of 64KB to 4GB (memory size: 2^N)
    - Support for configurable external device capacities
    - Up to two external memory devices sharing one address range (e.g. Dual-quad mode)
    - Up to four chip selects available
      - T2G: Up to two chip selects per channel
  - Memory interface logic
    - Supports stalling of transfers to address the back pressure on FIFOs
    - Supports read-write-data-strobe (RWDS)
    - Supports data signal connections between flexible external SPI memory devices
    - Supports delay line and data learning pattern (DLP)-based data capture (for cluster devices)

Hint Bar

Review TRM section 32.1 for additional details

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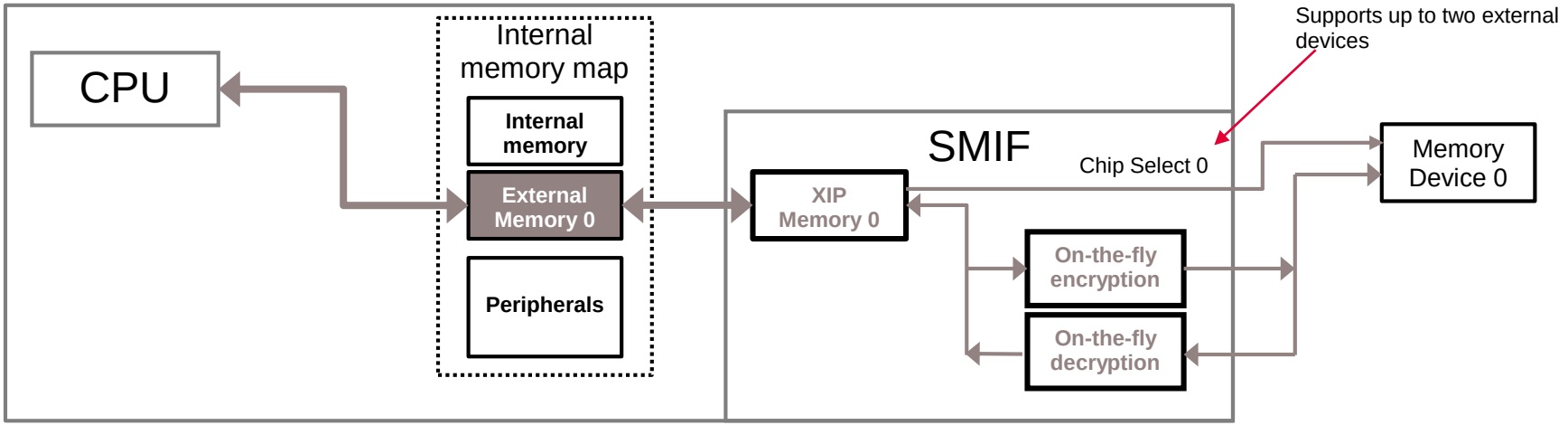
SMIF version overview

SMIF version	SMIF.2	SMIF.3	SMIF.4
Feature / Device	CYT3B/4B	CYT2C/3D	CYT4D/4E
xSPI, HYPERBUS™, Octal-SPI	Yes	Yes	Yes
SPI- SDR / DDR	Yes	Yes	Yes
NAND	Yes	Yes	Yes
1.8 V operation	-	-	Yes
3.3 V operation	Yes	Yes	Yes (CYT4E only)
XIP	Yes	Yes	Yes
MMIO	Yes	Yes	Yes
XIP + MMIO	-	Yes	Yes
Data Learning Pattern (DLP)	-	Yes	Yes
Delay-locked loop (DLL)	-	-	Yes
Single Channel FOTA	-	Yes (CS based)	Yes (address based)
Dual Channel FOTA	-	-	Yes (address based)
Interleaving of 2ch	-	-	Yes
Crypto regions	1	4	4 per channel

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Example of using SMIF

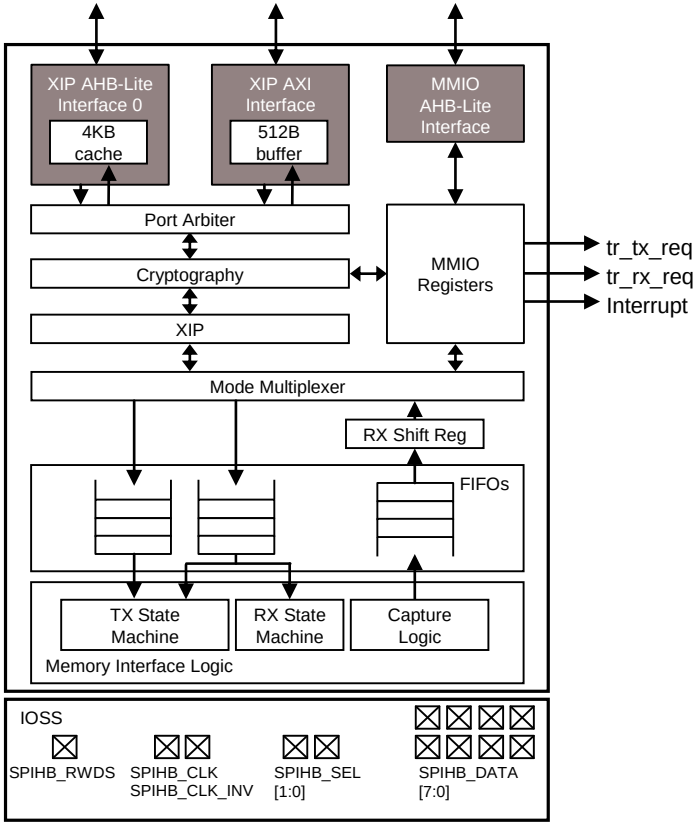
- External memory for code and data space
- Directly mapped to internal memory map (XIP operation mode)
- Encrypted/decrypted code or data in an external space



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SMIF block diagram

- SMIF block components
  - Bus interface
    - MMIO AHB-Lite interface
    - XIP AXI interface
    - XIP AHB-Lite interface



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Bus interface

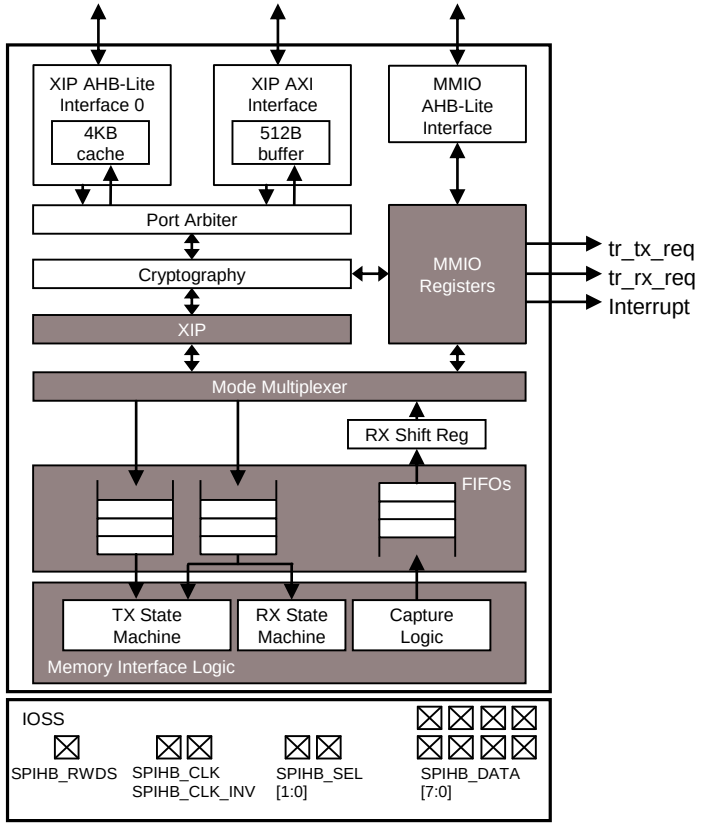
- All bus interfaces provide access to external memories
- Any of the three bus interfaces can access external memories at any time
  - MMIO AHB-Lite interface
    - Access to the MMIO registers
    - Supports MMIO operation mode
  - XIP AXI interface
    - AXI interface for CPUSS fast domain[1]
    - Supports XIP operation mode
    - Fixed 512B buffer[2]
  - XIP AHB-Lite interface
    - AHB-Lite interface for CPUSS slow domain[3]
    - Supports XIP operation mode
    - 4KB read-only cache[3]
      - The “hit” read transfers are processed by the cache
      - Four-way set associative with an LRU replacement scheme

[1] The CPUSS fast domain component is CM7 CPUs.
[2] Note that the cache and the AXI interface buffer are not retained in DeepSleep power mode.
[3] The CPUSS slow domain components are CM0+ Crypto and P-DMA.

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SMIF block diagram

- SMIF block components
  - FIFOs
  - Two operation modes
    - MMIO operation mode
    - XIP operation mode
    - Mode is switched by XIP_MODE[1]
    - Both modes are mutually exclusive up to SMIF. 2
  - Continuous transfer merging

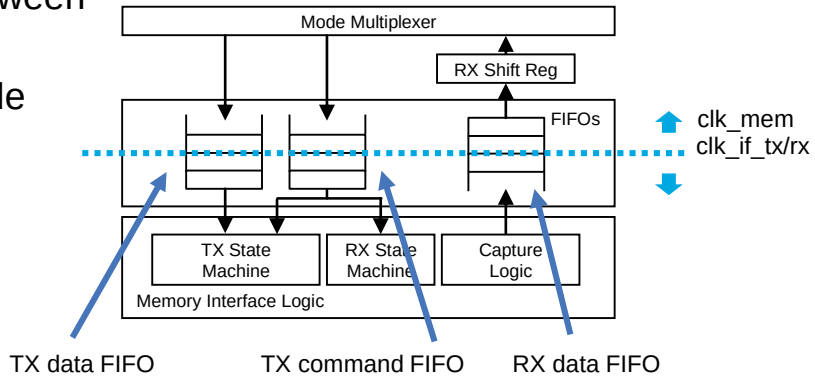


[1] Refer to the Register TRM (SMIF_CTL) for additional details.

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FIFOs

- SMIF has TX command FIFO, TX data FIFO, and RX data FIFO
  - Provides an asynchronous clock domain transfer between clk_mem and clk_if_tx/clk_if_rx
  - Software[1] controls the FIFOs in MMIO operation mode
  - MMIO registers[2] provide access to FIFOs



FIFO	Description
TX command FIFO	Transmit memory commands to the memory interface logic for memory transfer. Support five types of commands
TX data FIFO	Transmit write data to the memory interface logic
RX data FIFO	Receive read data from the memory interface logic

[1] In XIP operation mode, FIFOs are controlled by hardware.
[2] Refer to the Register TRM for additional details.

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FIFOs (1/2)

- TX command FIFO supports five command types
  - TX command FIFO is controlled by the SMIF_TX_CMD_FIFO_WR.DATA27[26:0][1] register
  - DATA27[26:24] specifies the command and DATA[23:0] sets the command specification depending on command type

Command: DATA27[26:24]	Specification: DATA27[23:0]
TX: 0	- Width of the data transfer (single, dual, quad, or octal data transfer) - Data transfer mode (SDR or DDR) - External device select (multiple devices can be selected simultaneously) - The command is for the last phase of memory transfer - Transfer of 1-2 bytes A memory transfer must start with a TX command.
TX_COUNT: 1	This command is used to transmit data from TX data FIFO to external memories - Value of memory data to be transmitted - Width of the data transfer - Data transfer mode (SDR or DDR) - Specifies if this command is for the last phase of the memory transfer

[1] Refer to the Register TRM for additional details.

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FIFOs (2/2)

- TX command FIFO supports five command types
  - TX command FIFO is controlled by the SMIF_TX_CMD_FIFO_WR.DATA27[26:0][1] register
  - DATA27[26:24] specifies the command and DATA[23:0] sets the command specification depending on command type

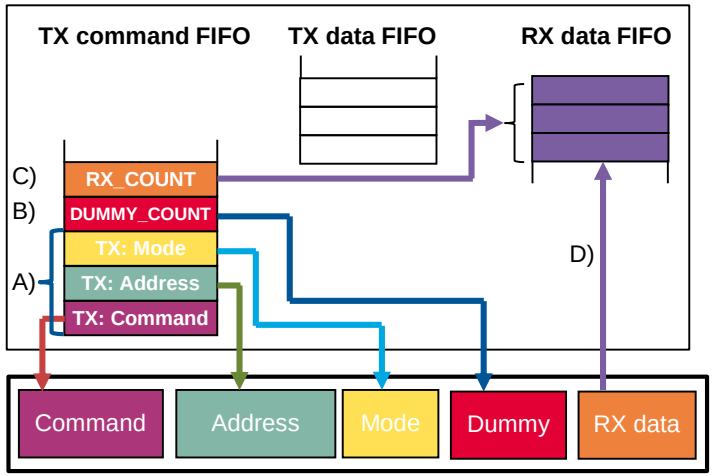
Command: DATA27[26:24]	Specification: DATA27[23:0]
RX_COUNT: 2	This command is used by RX data FIFO to receive data from external memories - Value of the memory data received - Width of the data transfer - Data transfer mode (SDR or DDR) - Specifies if this command is for the last phase of the memory transfer
DUMMY_COUNT: 3	- Number of dummy cycles (used to implement turnaround time) - If the variable latency mode for HyperRAM is enabled causing double the number of dummy cycles, this command never constitutes the last phase of the memory transfer
DESELECT: 4	Finish a transfer and deselect the memory device This command always constitutes the last phase of the memory transfer

[1] Refer to the Register TRM for additional details.

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Constructing a Read/Write command

Read command



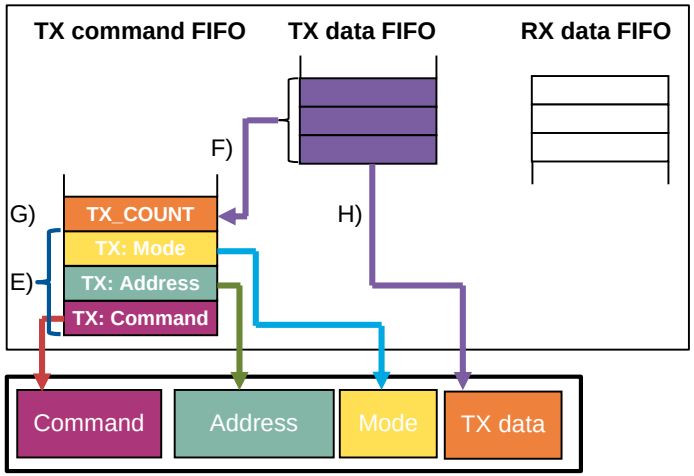
A) Set TX command FIFO in the order of Command, Address, and Mode using the “TX” command

B) Set dummy cycle to the TX command FIFO using the “DUMMY_COUNT” command

C) Set number of reception data to the TX command FIFO using the “RX_COUNT” command

D) Receive the number of data set by RX_COUNT in the RX data FIFO

Write command



E) Set TX command FIFO in the order of Command, Address, and Mode using the “TX” command

F) Fill TX data FIFO

G) Set number of transmission data to the TX command FIFO using the “TX_COUNT” command

H) Transmit the number of data set by TX_COUNT from the TX data FIFO

Hint Bar

Review TRM section 32.1 for additional details

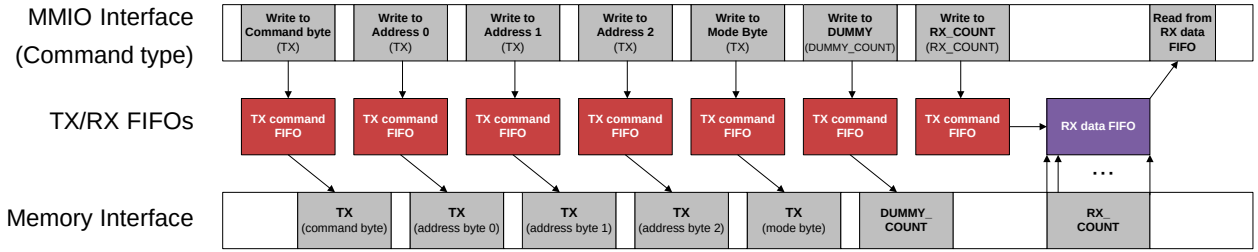
Mode:
It can eliminate the overhead of SIO instructions when repeating the same type of read command

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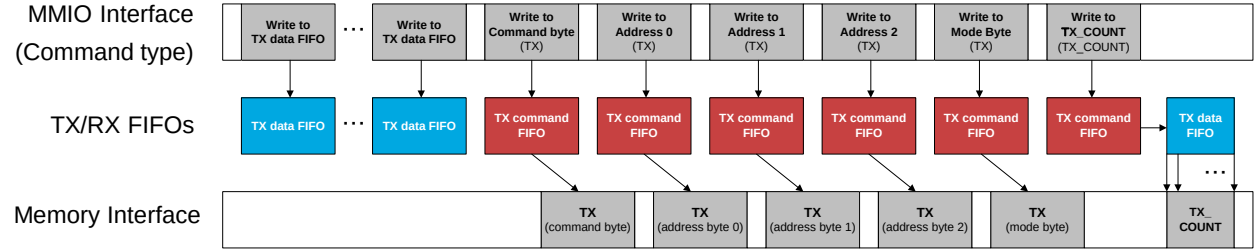
Operation mode

- MMIO operation mode
  - Active by writing “0” to XIP_MODE1
  - Supports access through software using FIFOs
  - Provides the flexibility to implement any SPI device transfer

Data Read example



Data Write example



[1] XIP_MODE default value is “0” in the MMIO mode.

Hint Bar

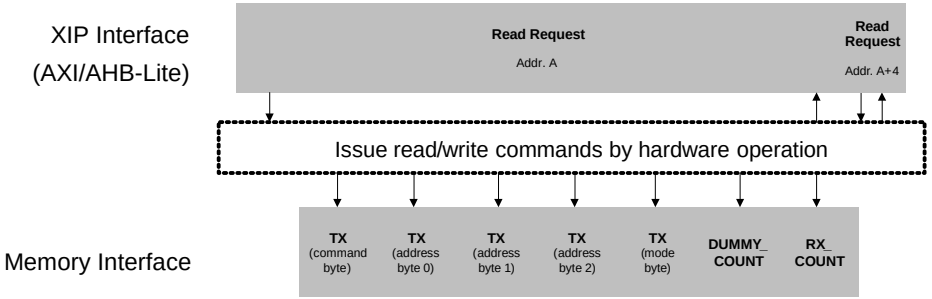
The software must ensure that it generates correct memory transfers

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Operation mode

- XIP operation mode
  - Allows mapping each external memory into an internal memory address space
  - Activates the XIP mode by writing “1” to XIP_MODE
  - Hardware generates memory transfers automatically without software intervention
  - Supports read and write access
  - FIFOs are controlled by hardware
  - Read/write commands are specified by MMIO registers[1] for each device

Data Read example



Hint Bar

Read/write commands specification includes:

Presence and value of SPI or HYPERBUS™ command byte

Number of address bytes

Presence and value of the mode byte

Number of dummy cycles

Data transfer widths and data transfer mode (SDR or DDR)

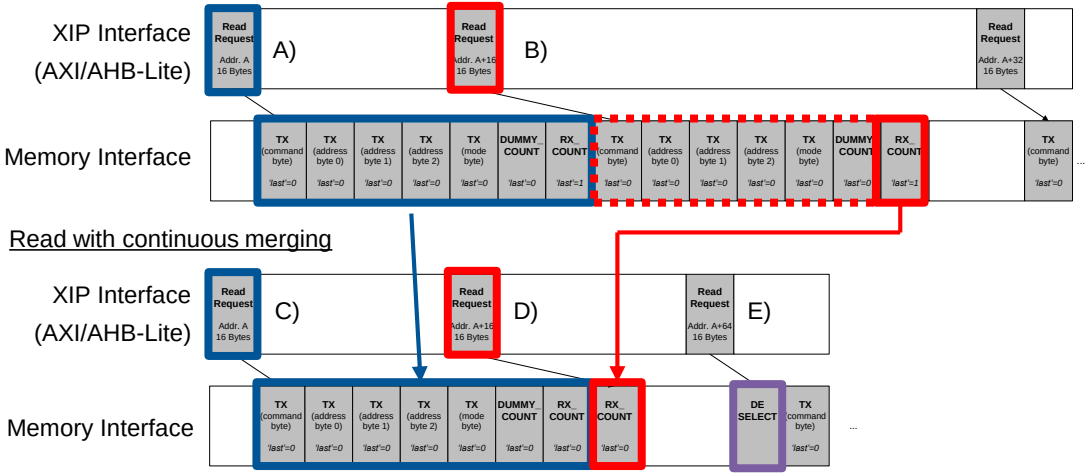
[1] Refer to the Register TRM (SMIF_DEVICE_RD/WR_CMD_CTL, _RD/WR_ADDR_CTL, _RD/WR_MODE_CTL, RD/WR_DUMMY_CTL, RD/WR_DATA_CTL) for additional details.

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Continuous transfer merging

- The transfer can be merged to a single transfer at the memory interface[1] (MMIO and XIP modes)
  - Background: Longer transactions split on the AXI bus due to arbitration and crypto support
  - Avoid the overhead of multiple commands, addresses, modes, and dummy (latency) cycles

Read without continuous merging



A) 16-byte read transfer from address A involves command, address, and dummy cycle

B) Read transfers from continuous addresses (A+16) also involve command, address, and dummy cycles

C) 16-byte read transfer from address A involves command, address, and dummy cycles

D) Read transfers from continuous addresses (A+16) do not require command, address, and dummy cycles

E) When a new transfer is requested or start address is not a continuation (A+64), a DESELECT command is generated
The next read transfer requires a command, address, and dummy cycle

- Advantage
  - Improves performance of multiple continuous transfers

[1] Refer to the Register TRM (SMIF_CTL.MERGE_EN) for additional details.

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Bus error generation

› External memory accesses cause bus error under the following conditions

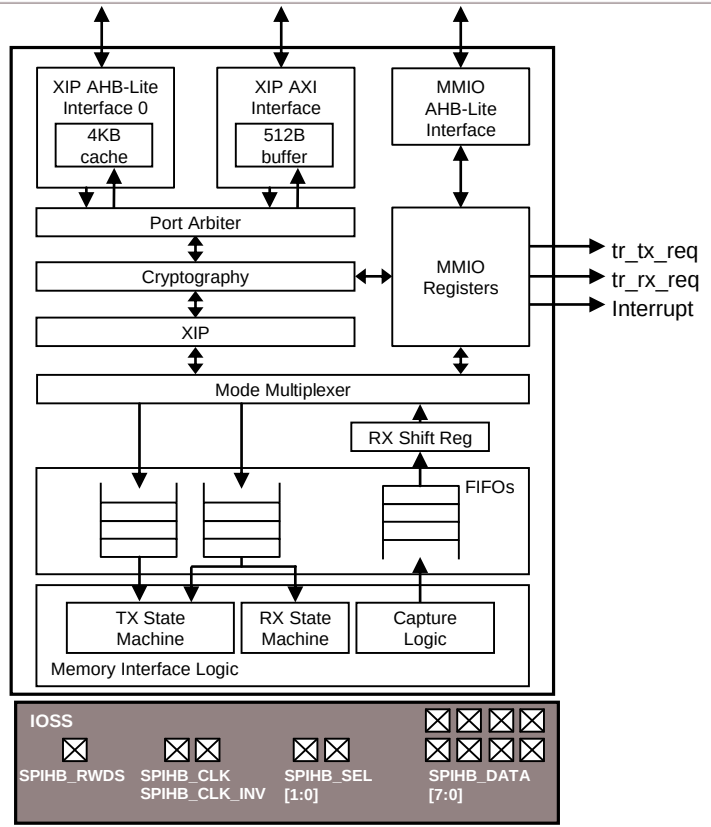
Interface	Precondition	Bus Error Factor
MMIO (AHB-Lite)	- SMIF_CTL.BLOCK = 0[1]	Software attempts to write an entry of a full TX command FIFO
		Software attempts to write more bytes than the available entries in the TX data FIFO
		Software attempts to read more bytes than the available entries in the RX data FIFO
XIP (AXI/AHB-Lite)	- SMIF_CTL.ENABLED = 0[1] - Write or read access	SMIF is disabled
	- SMIF_CTL.XIP_MODE = 0[1] - Write or read access	SMIF is not in XIP mode
	- XIP mode (SMIF_CTL.XIP_MODE = 1) - Write or read access	Transfer request is not in a memory region
	- XIP mode (SMIF_CTL.XIP_MODE = 1) - SMIF_DEVICE_CTL.WR_EN = 0[2]	Write transfer to a region that does not support writes
	- XIP mode (SMIF_CTL.XIP_MODE = 1) - Write access - Dual-quad SPI	Transfer address is not a multiple of 2
		Transfer size is not a multiple of 2
	- XIP mode (SMIF_CTL.XIP_MODE = 1) - Write access - Octal SPI DDR mode or HYPERBUS™ mode - Memory write byte masking is not supported	Transfer address is not a multiple of 2
		Transfer size is not a multiple of 2
	- SMIF_CTL.INT_CLOCK_DL_ENABLED = 1	No delay line tap resulting in a matching data learning pattern

[1] Refer to the Register TRM (SMIF_CTL) for additional details.
[2] Refer to the Register TRM (SMIF_DEVICE_CTL) for additional details.

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SMIF block diagram

- SMIF external device connection
  - Single, dual, quad, and octal data transfer
  - Memory interface clock:
    - Depends on memory and I/O type (see the device datasheet)
  - Can connect up to four devices
  - Independent SPIHB_CLK_INV outputs
    - Less latency, and no overlapping of SPIHB_CLK



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External device connection

- SPI connection
  - Support for single, dual, quad, and octal SPI protocol
  - Data signal type configuration in the MMIO register1
  - Can be set independently for each memory device (chip select)

Data signal connections

DATA_SEL[1:0]	Single SPI (Full Duplex)	Dual SPI (Half Duplex)	Quad SPI (Half Duplex)	Octal SPI (Half Duplex)
0	SPIHB_DATA [0] = SI SPIHB_DATA [1] = SO	SPIHB_DATA [0] = IO0 SPIHB_DATA [1] = IO1	SPIHB_DATA [0] = IO0 : SPIHB_DATA [3] = IO3	SPIHB_DATA [0] = IO0 : SPIHB_DATA [7] = IO7
1	SPIHB_DATA [2] = SI SPIHB_DATA [3] = SO	SPIHB_DATA [2] = IO0 SPIHB_DATA [3] = IO1	Illegal setting	Illegal setting
2	SPIHB_DATA [4] = SI SPIHB_DATA [5] = SO	SPIHB_DATA [4] = IO0 SPIHB_DATA [5] = IO1	SPIHB_DATA [4] = IO0 : SPIHB_DATA [7] = IO3	Illegal setting
3	SPIHB_DATA [6] = SI SPIHB_DATA [7] = SO	SPIHB_DATA [6] = IO0 SPIHB_DATA [7] = IO1	Illegal setting	Illegal setting

[1] Refer to the Register TRM (SMIF_DEVICE_CTL) for additional details.

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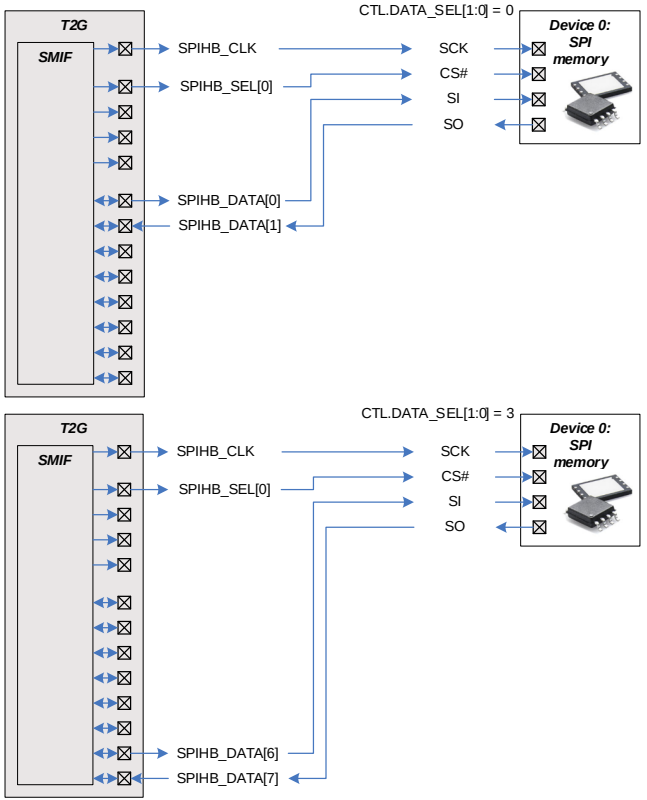
External device connection

- SPI connection
  - The following diagrams show examples of a single SPI connection
- Features
  - Data signal connections are configured by DATA_SEL
  - Chip select signal setting is configured depending on the operation mode

Operation Mode	Setting Register	Chip Select	Note
MMIO	TX command FIFO DATA[23:20][1]	DATA[21]: SPIHB0_SEL[1] DATA[20]: SPIHB0_SEL[0]	
		DATA[23]: SPIHB1_SEL[1] DATA[22]: SPIHB1_SEL[0]	Supports CYT4DN
XIP	SMIF0_DEVICE0[2]	SPIHB0_SEL[0]	
	SMIF0_DEVICE1[2]	SPIHB0_SEL[1]	
	SMIF1_DEVICE0[2]	SPIHB1_SEL[0]	Supports CYT4DN
	SMIF1_DEVICE1[2]	SPIHB1_SEL[1]	

[1] Refer to the Register TRM (SMIF_TX_CMD_FIFO_WR) for additional details. Multi chip selects can be set at the same time in dual-quad mode.
[2] Refer to Register TRM (SMIF_DEVICE) for additional details.

Single SPI connection examples

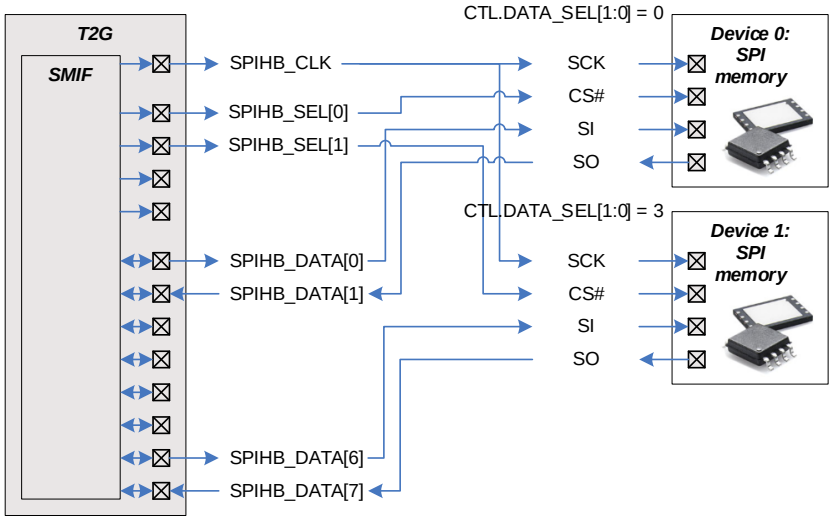


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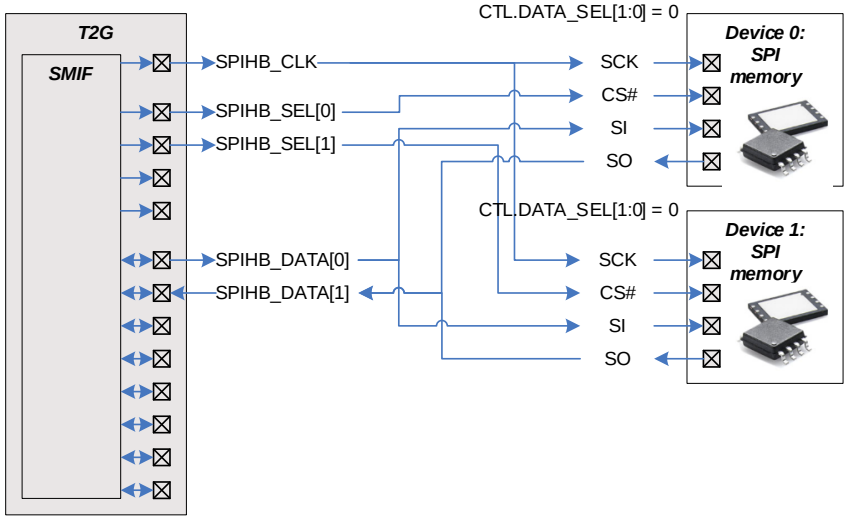
External device connection

- SPI connection
  - The following diagrams provide examples of two single SPI device connections

Single SPI with separate data signals



Single SPI with shared data signals

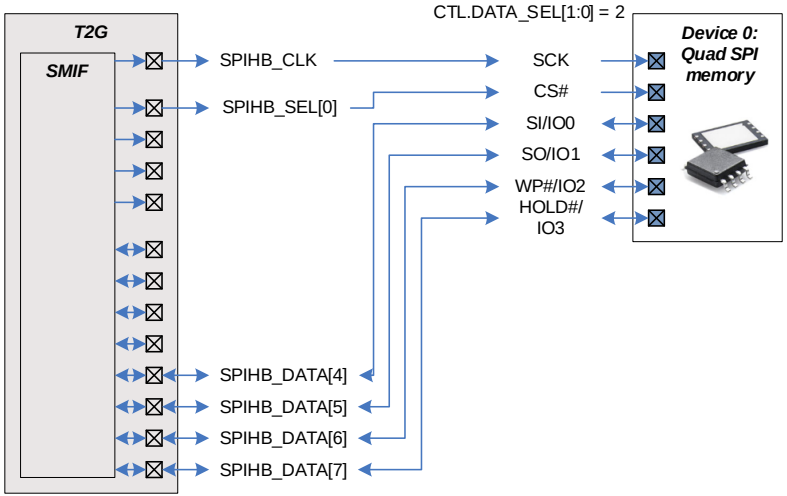


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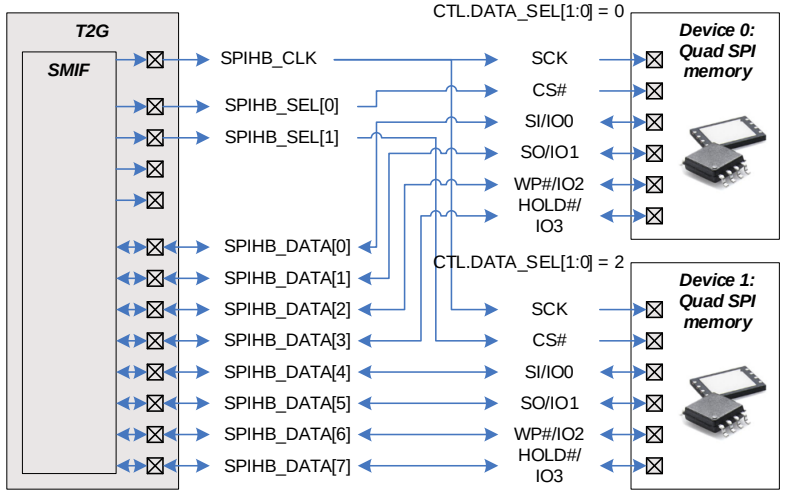
External device connection

- SPI connection
  - The following diagrams show examples of quad and dual-quad SPI connections
- Features
  - Quad SPI can also use SPIHB_DATA [4:7] by the DATA_SEL configuration

Quad SPI connection



Dual-Quad SPI connection (Pseudo Octal)

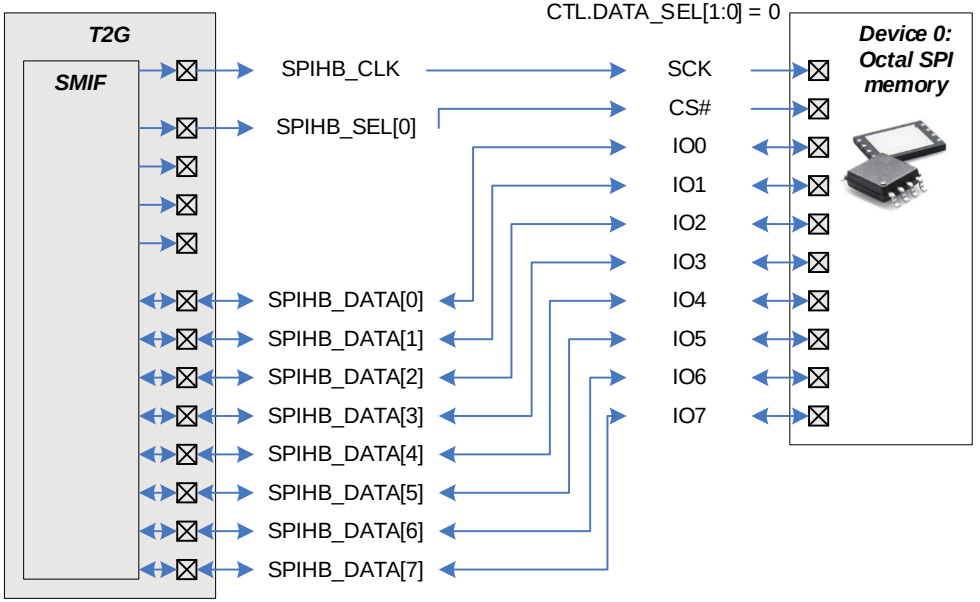


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External device connection

- SPI connection
  - The following diagram shows an example of an octal SPI connection
- Features
  - The only valid setting for DATA_SEL is “0”

Octal SPI connection

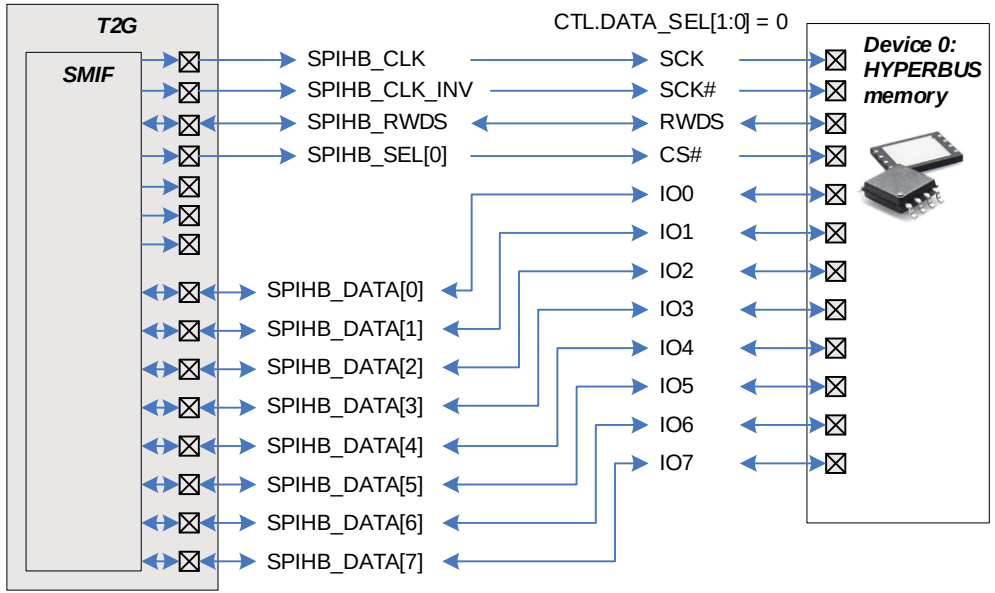


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External device connection

- HYPERBUS™ connection
  - The following diagram shows an example of the HYPERBUS™ connection
- Features
  - Supports read-write-data-strobe (RWDS)
  - Only valid setting for DATA_SEL is “0”

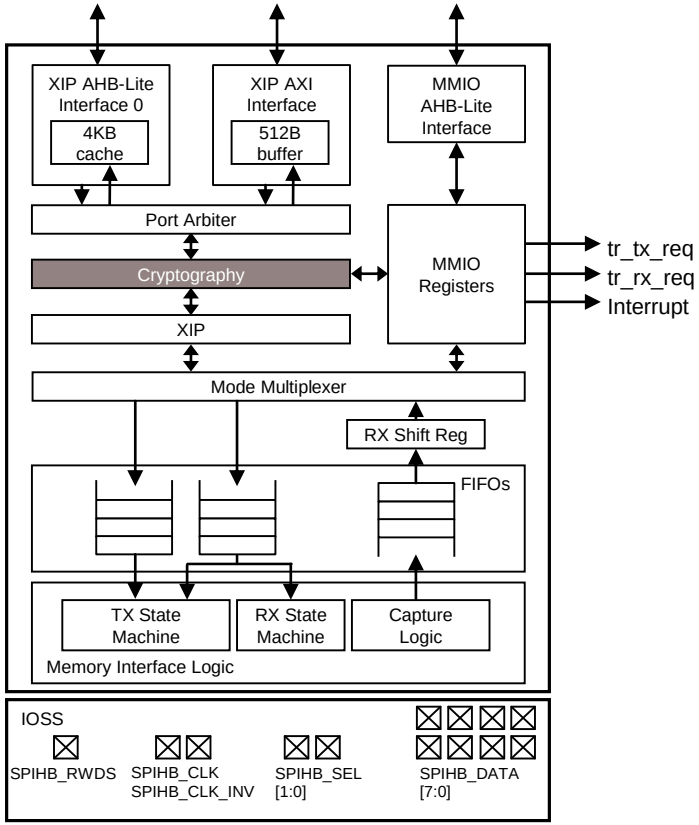
HYPERBUS™ connection



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SMIF block diagram

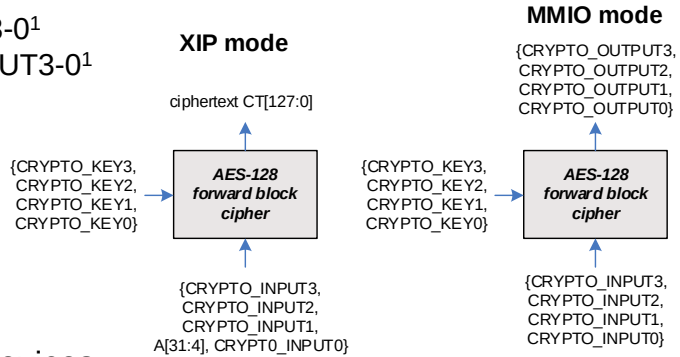
- SMIF block component
  - Cryptography



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Cryptography

- Read and write data transfers are available for encryption and decryption
  - Encryption and decryption are based on the AES-128 forward block cipher
    - The key is programmed into the SMIF_CRYPTO_KEY3-0 registers[1]
  - In MMIO mode
    - Supports offline encryption and decryption
    - Provides plaintext in SMIF_CRYPTO_INPUT3-0[1]
    - Provides ciphertext in SMIF_CRYPTO_OUTPUT3-0[1]
  - In XIP mode
    - Supports on-the-fly encryption for write data
    - Supports on-the-fly decryption for read data
    - Uses XIP address for plaintext and extends to SMIF_CRYPTO_INPUT3-0
- Advantage
  - Storing data encrypted in external memory devices prevents leakage of sensitive data



Hint Bar

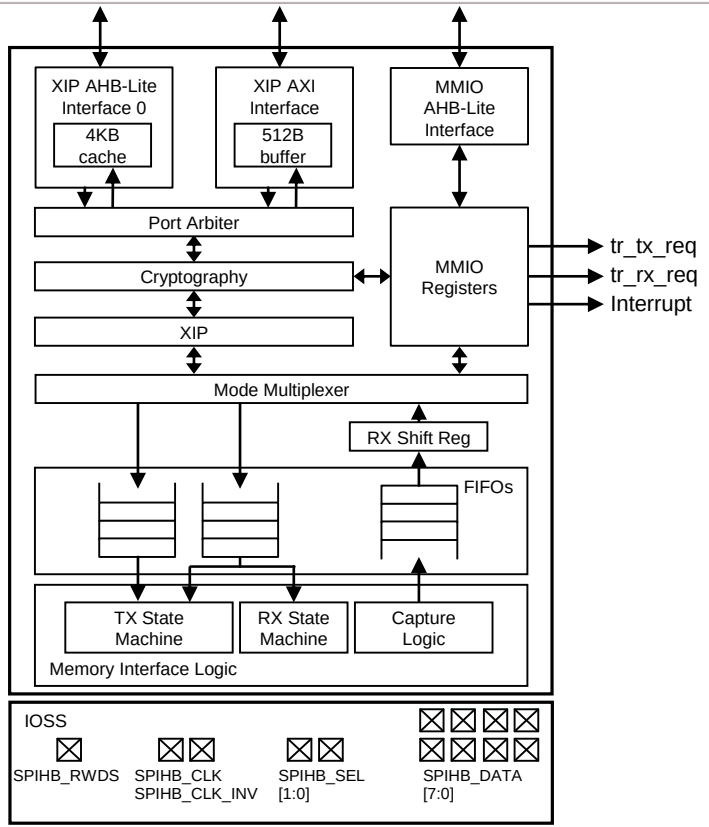
SMIF_CRYPTO_KEY registers are write-only. Software read returns “0”.

[1] Refer to the Register TRM for additional details.

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SMIF block diagram

- SMIF block components
  - Trigger and interrupt
    - tr_tx_req
    - tr_rx_req
    - Interrupt



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Trigger and interrupt

› SMIF has two triggers

Trigger	Condition
tr_tx_req	Active when the number of used TX data FIFO entries is smaller than or equal to the specified number[1]. Activated in MMIO operation mode
tr_rx_req	Active when the number of used RX data FIFO entries is greater than or equal to the specified number[2]. Activated in MMIO operation mode

[1] Refer to the Register TRM (SMIF_TX_DATA_MMIO_FIFO_CTL and SMIF_TX_DATA_MMIO_FIFO_STATUS) for additional details.
[2] Refer to the Register TRM (SMIF_RX_DATA_MMIO_FIFO_CTL and SMIF_RX_DATA_MMIO_FIFO_STATUS) for additional details.

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Trigger and interrupt (1/2)

› SMIF has one interrupt

Interrupt Cause	Condition
TR_TX_REQ	Active when the tr_tx_req trigger is activated. Activated in MMIO operation mode
TR_RX_REQ	Active when the tr_rx_req trigger is activated. Activated in MMIO operation mode
XIP_ALIGNMENT_ERROR[1]	- The XIP AHB-Lite/AXI bus transfer address is not a multiple of “2” or - The requested XIP AHB-Lite/AXI bus transfer size is not a multiple of “2” In the above conditions a) a write transfer is requested and b) Dual-Quad SPI mode is selected or Octal SPI DDR mode or HYPERBUS™ mode is selected without memory write byte masking Activated in XIP operation mode.
TX_CMD_FIFO_OVERFLOW	Write transfer to TX command FIFO[2] with not enough free entries available. Activated in MMIO operation mode

[1] Refer to the Register TRM (SMIF_INTR) for additional details.
[2] Refer to the Register TRM (SMIF_TX_CMD_FIFO_WR) for additional details.
[3] Refer to the Register TRM (SMIF_TX_DATA_FIFO_WR1,WR2,WR4) for additional details.
[4] Refer to the Register TRM (SMIF_RX_DATA_FIFO_RD1,RD2,RD4) for additional details.

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Trigger and interrupt (2/2)

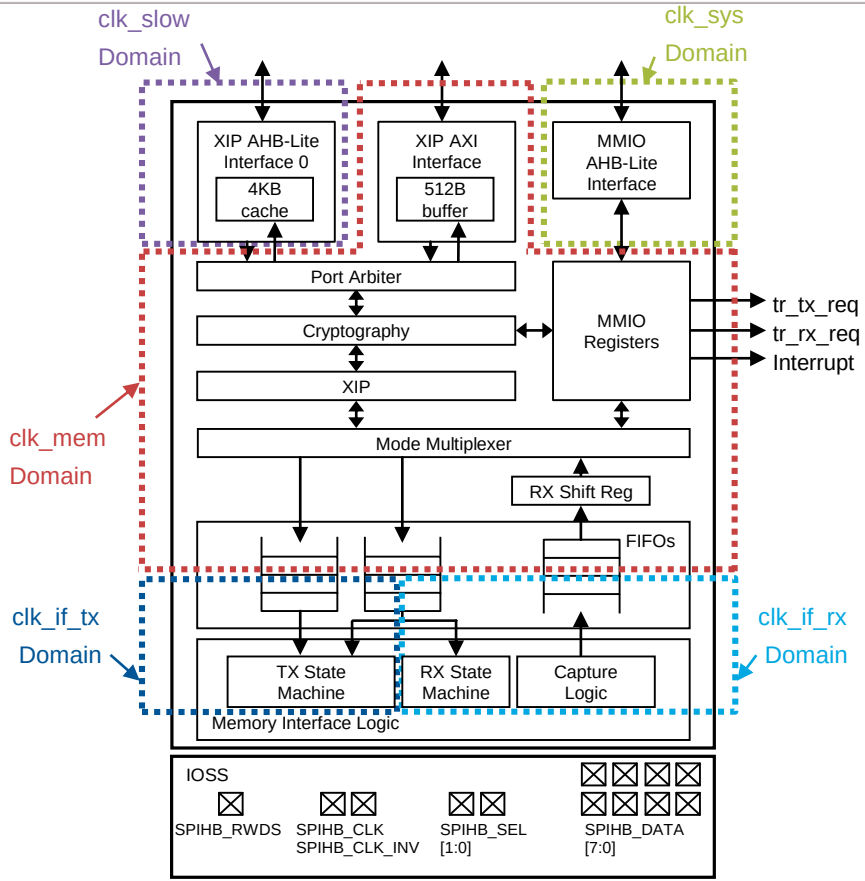
› SMIF has one interrupt

Interrupt Cause	Condition
TX_DATA_FIFO_OVERFLOW	Write transfer to TX data FIFO[3] with not enough free entries available. Activated in MMIO operation mode
RX_DATA_FIFO_OVERFLOW	Read transfer from RX data FIFO[4] with not enough entries available. Activated in MMIO operation mode
DL_FAIL	Data Learning Failed (no DLP match found on at least one of the input data lines when CTL.INT_CLOCK_DL_ENABLED = 1)
DL_WARNING	Data Learning Warning (for at least one input data line less then DLP.DL_WARNING_LEVEL delay line taps resulted in a correct DLP capturing when CTL.INT_CLOCK_DL_ENABLED = 1). This interrupt will be suppressed if DL_FAIL also occurs during the same DLP evaluation cycle
CRC_ERROR	CRC Error. A read transfer data CRC check failed
FS_STATUS_ERROR	Functional Safety Status Error. A read transfer Functional Safety Status check failed

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SMIF block diagram

- SMIF block components
  - Clock domains
    - CLK_MEM
    - CLK_SLOW
    - CLK_SYS
    - clk_if_tx/rx



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Clock

› The following clocks are used in SMIF

Source	Used Block	Function
clk_mem	SMIF Internal Block FIFOs	Used for the SMIF block; it is sourced from the mem clock The frequency range is up to 200 MHz
	AXI Master Interface	Used by the XIP AXI master interface; it is sourced from the mem clock The frequency range is up to 200 MHz
clk_slow	AHB Slave Interface	Used by the XIP AHB-Lite master interface; it is sourced from the slow clock The frequency range is up to 100 MHz
clk_sys	AHB Slave Interface	Used by the MMIO AHB-Lite slave interface; it is clocked by the PERI group clock The frequency range is up to 100 MHz
clk_if_tx/rx	Memory Interface FIFOs	Used for memory interface of transmit and receive; it is clocked by the CLK_HF6 clk_if_tx is the source clock for SPIHB_CLK

Hint Bar

Review TRM chapter 18 for additional details

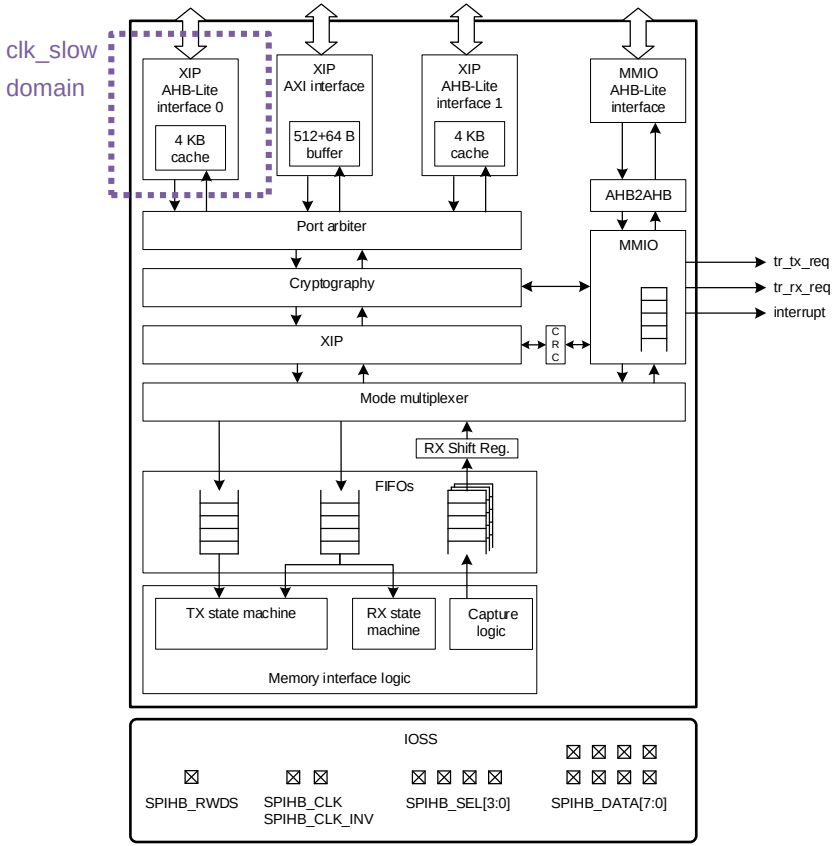
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SMIF.3

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SMIF.3 block diagram

- High level overview
  - Fast AXI interface is used by the CM7 CPU
  - Slow AHB-lite interface 0 is used by the CM0+, Crypto, P/M-DMA
  - Same as SMIF.4 without bridge



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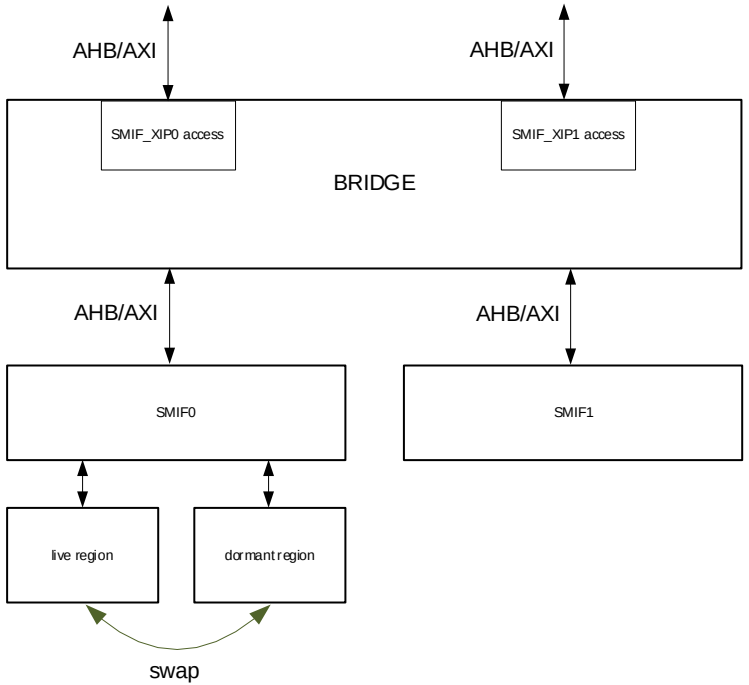
New features for SMIF.3 compared to SMIF.2

- Single-channel FOTA
  - Interleaving between MMIO (FIFO based) and XIP (memory-mapped) are possible
    - No mode change necessary
    - No wait time in µs or ms range (interleaving on command level)
    - Additional arbitration mode (“ARB_MODE”) is introduced
    - XIP accesses have always priority over MMIO accesses
  - Address change possible between CS areas
- Enhanced Crypto support
  - Supports up to 4 memory regions with a different key
  - Each memory region is divided into 4 equally sized subregions where crypto can be applied or skipped
  - Key regions can overlap; lowest key number takes priority
  - Key 0 supports only MMIO operation; all others support XIP and MMIO
- Full Data Learning Pattern (DLP) support

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Single-channel FOTA

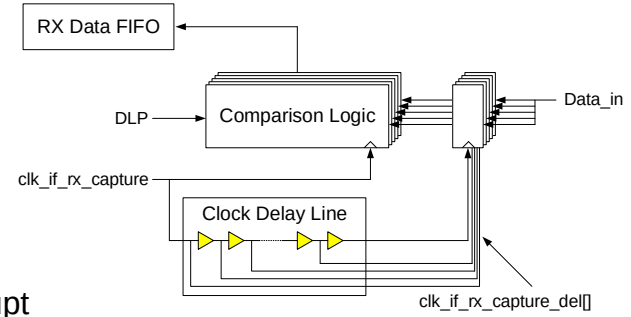
- Use case
  - The live region exists in one memory connected to a particular SMIF while the dormant region exists in a second memory connected to the same SMIF
  - The two remap regions are both mapped to the same SMIF but to separate CS spaces
  - When a swap is required, the REMAP REGION's bitfields (SMIF0_REMAP fields of the two remap regions) are simply swapped if the memory exists on SMIF0

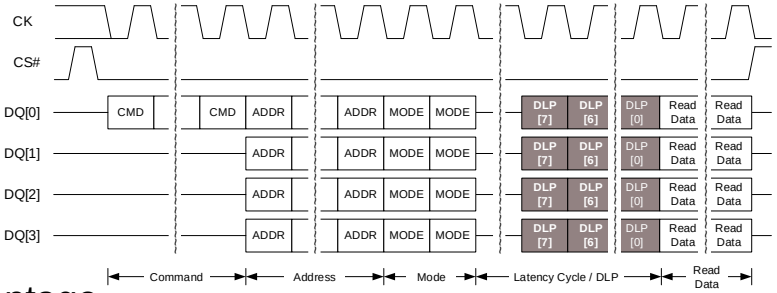


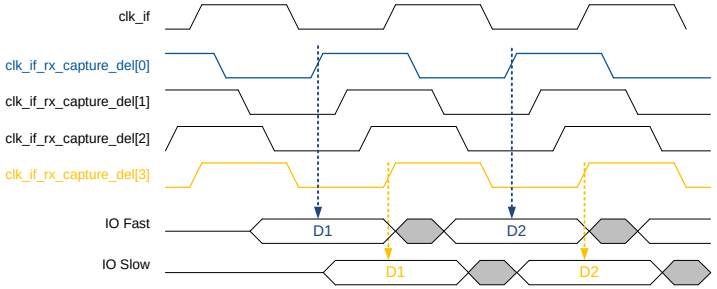
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Data Learning Pattern (DLP)

- SMIF supports delay line and DLP-based data capture
  - Provides an optimal capture point within the data window
  - Captures input data with different clocks generated by taps of a delay line
  - Finds the delay tap for each data line by comparing the captured DLP with the expected one
  - Memory device provides a known DLP on every data I/O pin before outputting read data
  - No delay line tap resulting in a matching DLP, a data learning failed interrupt (in XIP/MMIO mode), and a bus error response (in XIP mode) being generated







- Advantage
  - Adjust signal delay easily due to wiring length, process, voltage, and temperature for each data line
  - Maximize read data throughput

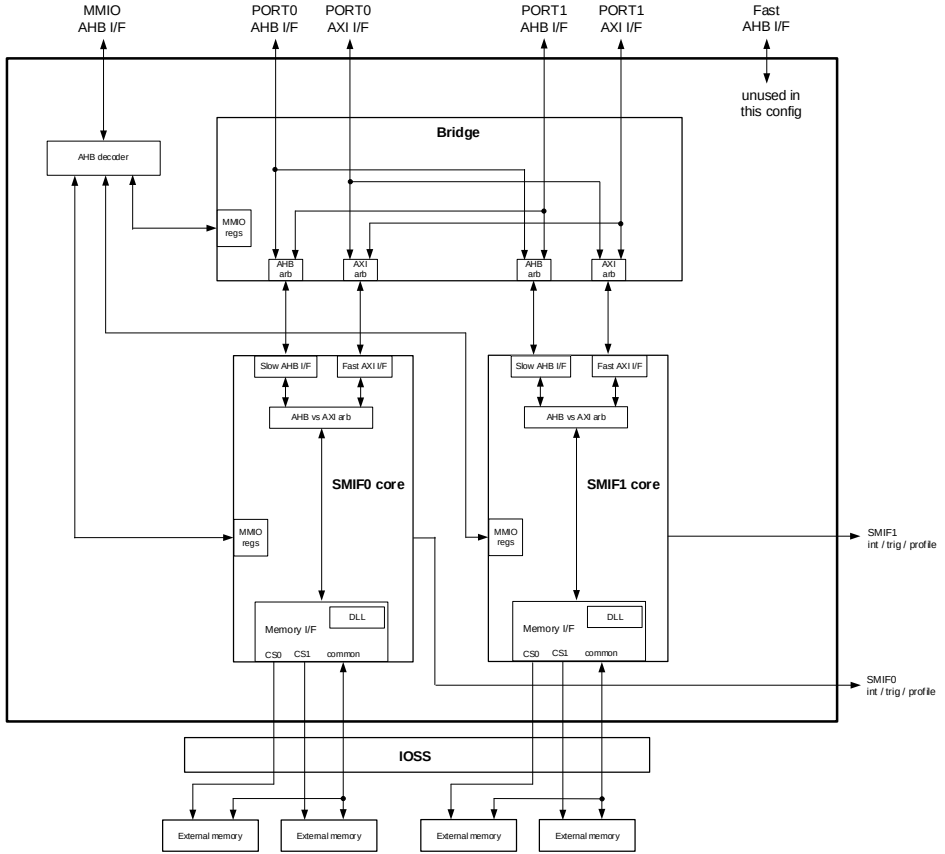
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SMIF.4

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SMIF.4 block diagram

- High-level overview
  - Including the bridge and two SMIF cores



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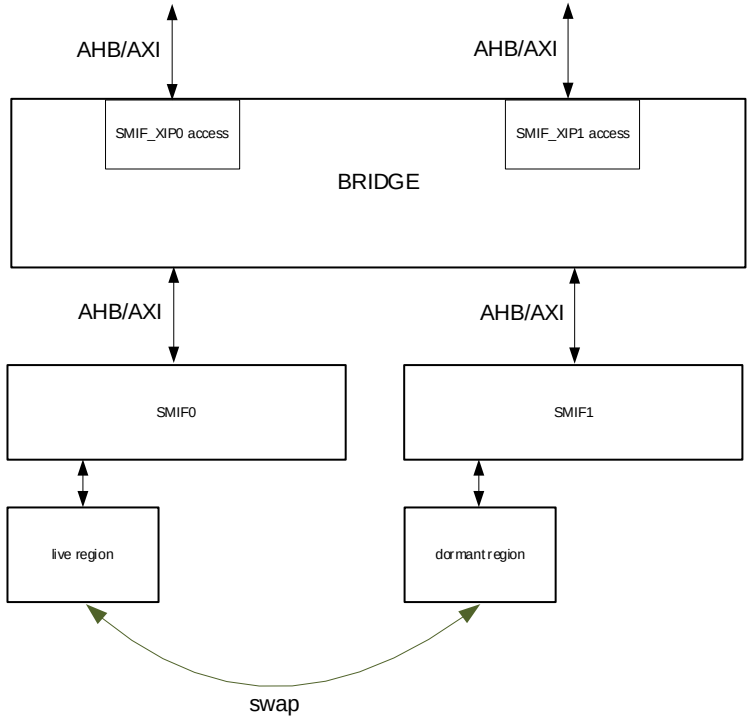
New features for SMIF. 4 compared to SMIF. 3

- Dual Channel FOTA
  - Freely map memory regions across two SMIF channels
  - Offset and Size of the regions are freely configurable
  - Memory regions are independent from CS signals
  - SMIF.3 single channel FOTA is available in addition
  - Applicable in XIP mode
- Interleaving
  - SMIF.4 supports the split of data to both SMIF channels to increase performance
  - Offset and Size of the regions are freely configurable
  - Memory regions are independent from CS signals
  - Applicable in XIP mode
- DLL for input delay adjustment
  - Precise adjustment of sample points for incoming data
  - Independent from technology, voltage- and temperature drift
  - Usable for memories with Data Learning Pattern (DLP) to adjust sample timing
- Enhanced Crypto support
  - Supports up to 4 memory regions with a different key per channel
  - Each memory region is divided into 4 equally sized subregions where crypto can be applied or skipped

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Dual channel FOTA

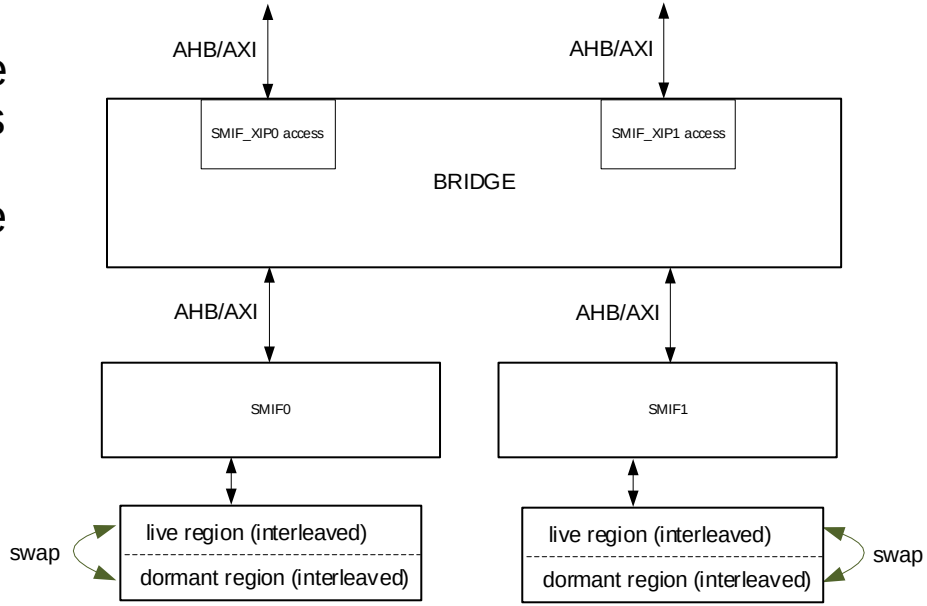
- Use case
  - The live region exists in one memory connected to a particular SMIF while the dormant region exists in a second memory connected to the other SMIF
  - The two remap regions are mapped to separate SMIFs
  - When a swap is required all that is needed is to swap their USE_SMIF[1:0] fields



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Dual channel interleaved FOTA

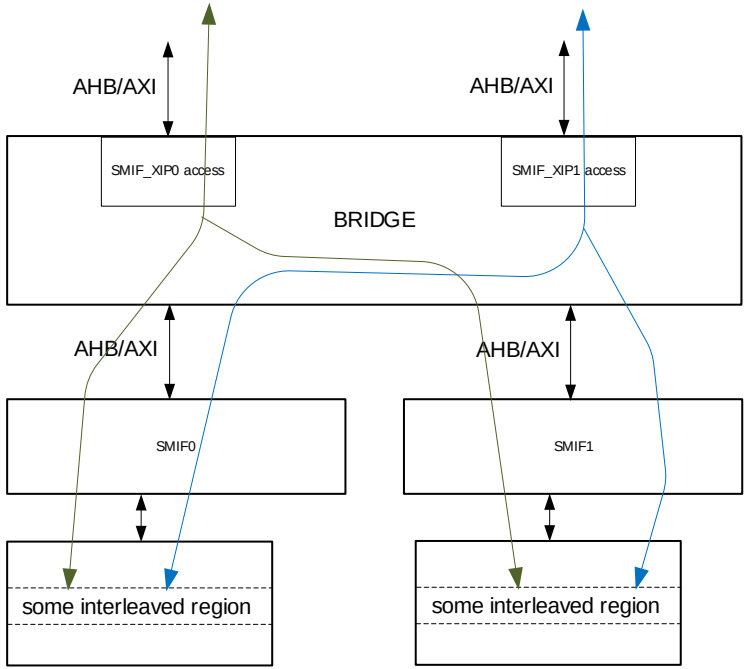
- Use case
  - The live region is interleaved across one memory connected to one SMIF and another memory connected to the other SMIF, and the dormant region is similarly interleaved (to the same memories as the live region if they are read-while-write capable memories)
  - Both the remap regions have their parameter USE_SMIF[1:0] set to b’11 indicating interleaving
  - When a swap is required, SMIF0_REMAP for the live region swaps with SMIF0_REMAP of the dormant region, and the same occurs for SMIF1_REMAP



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Aliased views

- Advantage
  - A single physical region in memory can be seen through either the SMIF0_XIP or SMIF1_XIP spaces (and thus by separate masters that may keep to one space or the other)
  - By setting up an aliased remap region, the interleaved region can be seen equally in either of the SMIFx_XIP spaces.



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Interleaving mode

- If USE_SMIF[1:0] = 11, then regardless of whether the access came in through the SMIF0_XIP port or the SMIF1_XIP port, the access is routed to both SMIF0 and SMIF1 in an interleaved manner
- Interleaving means access to ping-pong between the two SMIFs every INTLV_STEP_SIZE[2:0], which decodes as below:

INTLV_STEP_SIZE[2:0]	Byte
000	8 bytes
001	16 bytes
010	32 bytes
011	64 bytes
111	128 bytes

Hint Bar

Review TRM section 32.2.6 and 32.2.3.8 for additional details

Note:

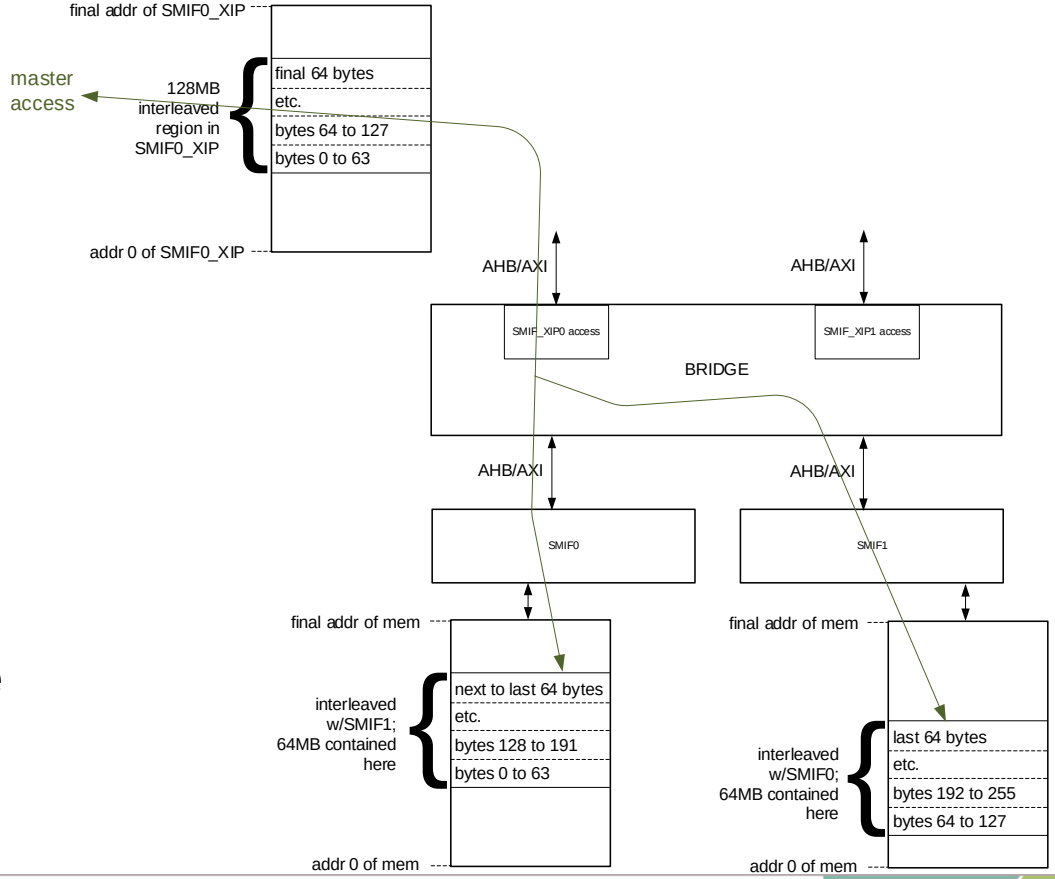
In TRAVEO™ T2G an AXI WRAP transfer only occurs when the CM7 fills a data or instruction cache line.

If the SMIF bridge features are required and the CM7 shall be able to access the SMIF XIP address space, user has to ensure that the corresponding address space does not have a cacheable memory attribute or disable caches globally.

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Interleaving mode use case

- Use case
  - Interleaving to arbitrary places in memories connected to SMIF0 and SMIF1
  - An arbitrary 128MB region in the SMIF0_XIP space (must be situated on a 128MB boundary), which divides into 64MB in each SMIF (must be situated on 64MB boundaries) using a step size of 64 bytes
- Advantage
  - Two SMIFs can keep the memories selected and accessible simultaneously, thus doubling the bandwidth to/from the master



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Delay-locked loop (DLL)

- DLL allows higher precision placement of clocks within data windows allowing for higher speed memories
- DLL-based memory interface supports the following protocols
  - HYPERBUS™, xSPI, and Octal SPI with DQS DDR
  - Octal SPI with DQS SDR
  - Normal SPI DDR
  - Normal SPI SDR
  - DLP SPI DDR
  - DLP SPI SDR
- DLL contains three main components:
  - One Master Delay Line (MDL)
  - Two Slave Delay Line (SDL)

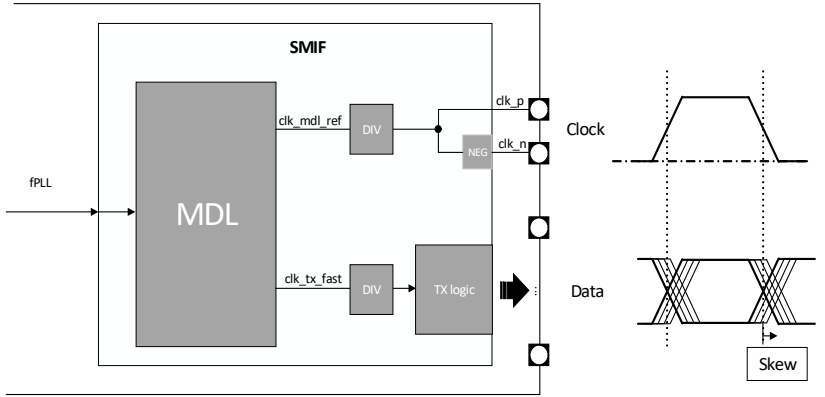
Hint Bar

Review TRM chapter 32.2.7 for additional details

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Master delay line (MDL)

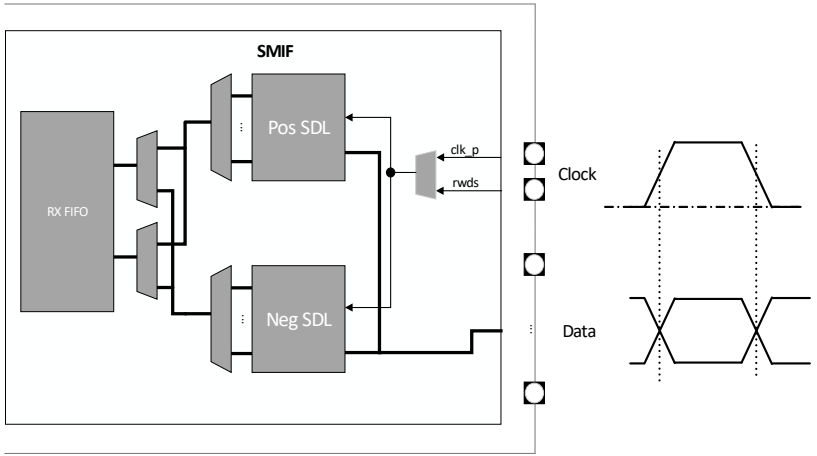
- Overview
  - MDL is a closed-loop DLL
  - It has16 taps that are nominally 391ps apart at 160 MHz.
  - It outputs the reference clock (taken just before the first tap stage) and a delayed version of that that is the result of a 16:1 mux of the tap stages as determined by the MMIO field CTL2.MDL_TAP_SEL.
  - The reference clock out becomes the basis for the clock to the memory, while the delayed clock out is used to clock the data out to the memory.
  - The proper delay is selected such that the data meets setup and hold to the memory clock.
- Use case
  - MDL is used for the transmit data path as well as for producing the clock to the memory



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Slave delay line (SDL)

- Overview
  - There are two SDLs, one for positive edge capture and the other for negative edge capture.
  - It has 16 tap stages like the MDL. However, the inbound clock is intermittent and thus cannot be reliably locked to. So instead the tap stages are tuned indirectly by the MDL which does have a free-running clock to lock to.
- Use case
  - SDLs are used for the receive data path to capture the incoming data



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Comparison of SMIF.3 and SMIF.4

Description	SMIF.3	SMIF.4
Supported xSPI/HYPERBUS™ Bus Speed Grade (DDR)	8-bit xSPI/HYPERBUS™ DDR up to 133 MHz	8-bit xSPI/HYPERBUS™ DDR up to 200 MHz[1]
Supported xSPI/HYPERBUS™ Bus Speed Grade (SDR)	8-bit xSPI SDR up to 133 MHz	8-bit xSPI SDR up to 166 MHz
Supported bus protocols and speed grades	Single/dual/quad/octal/dual-quad SPI up to 100 MHz SDR (133 MHz in 28HPL), 80 MHz DDR	Single/dual/quad/octal/dual-quad SPI up to 166 MHz SDR, 100 MHz DDR
AHB XIP interfaces	1 or 2 each with optional 4KB cache	- With bridge: 2 AHB and 2 AXI XIP interfaces - Without bridge: Either 2 AHB or 1 AHB and 1 AXI XIP (CM7) interfaces
AXI Buffer	0 or 1 AXI XIP interfaces with 512B buffer for up to 4 AXI transactions	512B AXI buffer per SMIF core for up to 4 AXI transactions
FOTA	Firmware update-Over-The-Air (FOTA) support allowing MMIO and XIP simultaneous access	Single-channel FOTA, plus dual-channel if bridge present
XIP-Space	Up to 4GB	- With bridge: 512MB for each port - Without bridge: up to 4GB

[1] Refer to the device-specific datasheet for maximum timing.

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Revision History

Revision	ECN	Submission Data	Description of Change
**	6399119	2018/12/03	Initial release
*A	6633414	2019/07/22	Change from mxsmif_ver2 to mxsmif_ver3 Updated slide 2, 6, 18, 19 Added slide 4, 17, 31
*B	7039074	2020/12/03	Updated slide 2, 3, 4
*C	7782972	2022/07/05	Updated 2, 4, 6, 15, 20, 22 to 26, 28 Added slide 7, 35 to 51.

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