MOTIX™ TLE986xQX family - BF, A, UH, and UI steps
MOTIX™ TLE987xQX family - BF, A, UH, and UI steps

Overview

This document lists the errata of the TLE986xQX family and the TLE987xQX family.

It is strongly recommended that the device behavior and possible proposed workarounds are considered for the application.

Referenced documents:

Table 1 Reference documents

Document type	Document reference	Issue date
Datasheet	See **Table 2**	
User manual	Infineon-TLE986x-UM-v01_92-EN.pdf	2025-09-15
User manual	Infineon-TLE987x-UM-v01_92-EN.pdf	2025-09-15
BootROM user manual	Infineon-TLE986x_TLE987x-BootROM-UM-v01_91-EN.pdf	2025-09-15

Affected products:

Table 2 List of affected products

Product name	Orderable part number (OPN)	Design step	Reference datasheet	Issue date
TLE9861QXA20	TLE9861QXA20XUMA2	BF	Infineon-TLE9861QXA20-DS-v02_11-EN.pdf	2024-04-08
	TLE9861QXA20XUMA3	UH		
	TLE9861QXA20XUMA4	UI		
TLE9862QXA40	TLE9862QXA40XUMA1	A	Infineon-TLE9862QXA40-DS-v01_10-EN.pdf	2023-10-23
TLE9867QXA20	TLE9867QXA20XUMA2	BF	Infineon-TLE9867QXA20-DS-v02_11-EN.pdf	2024-04-08
	TLE9867QXA20XUMA3	UH		
	TLE9867QXA20XUMA4	UI		
TLE9867QXA40	TLE9867QXA40XUMA2	BF	Infineon-TLE9867QXA40-DS-v02_11-EN.pdf	2024-04-08
	TLE9867QXA40XUMA3	UH		
	TLE9867QXA40XUMA4	UI		
TLE9867QXW20	TLE9867QXW20XUMA1	BF	Infineon-TLE9867QXW20-DS-v02_11-EN.pdf	2024-04-08
	TLE9867QXW20XUMA2	UH		
	TLE9867QXW20XUMA3	UI		
TLE9868QXB20	TLE9868QXB20XUMA2	BF	Infineon-TLE9868QXB20-DS-v02_20-EN.pdf	2025-09-15
	TLE9868QXB20XUMA4	UH		
	TLE9868QXB20XUMA5	UI		

Table 2 List of affected products (cont'd)

Product name	Orderable part number (OPN)	Design step	Reference datasheet	Issue date
TLE9869QXA20	TLE9869QXA20XUMA2	BF	Infineon-TLE9869QXA20-DS-v02_11-EN.pdf	2024-04-08
	TLE9869QXA20XUMA3	UH		
	TLE9869QXA20XUMA4	UI		
TLE9871QXA20	TLE9871QXA20XUMA2	BF	Infineon-TLE9871QXA20-DS-v02_20-EN.pdf	2025-09-15
	TLE9871QXA20XUMA3	UH		
	TLE9871QXA20XUMA4	UI		
TLE9872-2QTW40	TLE98722QTW40XUMA1	A	Infineon-TLE9872_2QTW40-DS-v01_10-EN.pdf	2023-10-23
TLE9872-2QXA40	TLE98722QXA40XUMA1	A	Infineon-TLE9872_2QXA40-DS-v01_10-EN.pdf	2023-10-23
TLE9872-2QXW40	TLE98722QXW40XUMA1	A	Infineon-TLE9872_2QXW40-DS-v01_10-EN.pdf	2023-10-23
TLE9872QTW40	TLE9872QTW40XUMA1	A	Infineon-TLE9872QTW40-DS-v01_10-EN.pdf	2023-10-23
TLE9872QXA40	TLE9872QXA40XUMA1	A	Infineon-TLE9872QXA40-DS-v01_10-EN.pdf	2023-10-23
TLE9873QXW40	TLE9873QXW40XUMA1	BF	Infineon-TLE9873QXW40-DS-v02_11-EN.pdf	2024-04-08
	TLE9873QXW40XUMA2	UH		
	TLE9873QXW40XUMA3	UI		
TLE9877QTW40	TLE9877QTW40XUMA1	BF	Infineon-TLE9877QTW40-DS-v01_10-EN.pdf	2023-10-23
TLE9877QXA40	TLE9877QXA40XUMA2	BF	Infineon-TLE9877QXA40-DS-v02_20-EN.pdf	2025-09-15
	TLE9877QXA40XUMA3	UH		
	TLE9877QXA40XUMA4	UI		
TLE9877QXW40	TLE9877QXW40XUMA1	BF	Infineon-TLE9877QXW40-DS-v02_11-EN.pdf	2024-04-08
	TLE9877QXW40XUMA2	UH		
	TLE9877QXW40XUMA3	UI		
TLE9879-2QXA40	TLE98792QXA40XUMA1	BF	Infineon-TLE9879_2QXA40-DS-v02_11-EN.pdf	2024-04-08
	TLE98792QXA40XUMA2	UH		
	TLE98792QXA40XUMA3	UI		
TLE9879QTW40	TLE9879QTW40XUMA1	BF	Infineon-TLE9879QTW40-DS-v01_10-EN.pdf	2023-10-23
TLE9879QXA40	TLE9879QXA40XUMA2	BF	Infineon-TLE9879QXA40-DS-v02_20-EN.pdf	2025-09-15
	TLE9879QXA40XUMA3	UH		
	TLE9879QXA40XUMA4	UI		
TLE9879QXW40	TLE9879QXW40XUMA1	BF	Infineon-TLE9879QXW40-DS-v02_11-EN.pdf	2024-04-08
	TLE9879QXW40XUMA2	UH		
	TLE9879QXW40XUMA3	UI		

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1 Product errata

This chapter lists the errata of the referenced products and documentation.

1.1 BootROM USER_ERASE_SECTOR, USER_ERASEPG, and USER_PROG (0000062134-25)

Scope

This erratum applies only to the UH step.

Implemented

The USER_ERASE_SECTOR, USER_ERASEPG, and USER_PROG routines make use of the RAM byte at 0x18000014. Any data being stored there is overwritten.

1.1.1 Workaround

The user code must not use the RAM location 0x18000014.

1.1.2 Planned fixes

Fix implemented in the UI step.

1.2 DMA requests from SSC2 not cleared (0000045882-2296)

Description of the behavior

If the SSC2 module is selected as a trigger for the DMA transfer request upon SSCx Transmit or SSCx Receive, the DMA transfer requests coming from the SSCx module are not cleared using the SSCTXC or SSCRXC bit field of the DMASRCCLR register (DMA Source Selection Clear Register).

Effect

If the SSC2 module is selected as trigger, the DMA transfer request cannot be cleared by the software, leading to undesired DMA transfers.

1.2.1 Workaround

In order to avoid the described erratum, the following workaround is recommended. This method can only be used to clear the DMA request after a DMA cycle is completed and the DMA controller is idle. In the following example, DMA CH2 and CH3 are used for DMA transfer with SSCx transmit and receive and with SSCx modules in master-slave communication.

```
001    void isr_Ch3_DMA_complete(void)
002      {
003        SCU->DMASRCCLR.bit.SSCTXC = 1;    /* SSC Transmit DMA Request cleared */      Not working, as
004        SCU->DMASRCCLR.bit.SSCRXC = 1;    /* SSC Receive DMA Request cleared */       described in this
                                                                                        erratum
005        DMA->CHNL_ENABLE_SET.reg |= ((uint32)1u << 2);
006        /* this clears the pending DMA request by acting as a  sort of dummy transfer request */
007        DMA_Reset_Channel(DMA_CH2, DMA_CH2_NoOfTrans);    /* DMA CH2 reset */
008        DMA_Reset_Channel(DMA_CH3, DMA_CH3_NoOfTrans);    /* DMA CH3 reset */
009      }
```

Figure 1 Code listing: recommended DMA complete function with workaround

1.2.2 Planned fixes

No design fix is planned.

2 Revision history

Revision	Date	Changes
Rev. 1.6	2025-09-15	Front cover • Revision numbers and dates updated for user manuals • Revision numbers and dates updated for datasheets with added package option “VQFN-48-37”: TLE9868QXB20, TLE9871QXA20, TLE9877QXA40, TLE9879QXA40
Rev. 1.51	2024-04-08	Front cover • Added an OPN number for the UI step • TLE9868QXB20: Changed BF step OPN number from “TLE9868QXB20XUMA3” to “TLE9868QXB20XUMA2”
Rev. 1.5	2023-10-23	Chapter “BootROM USER_ERASE_SECTOR, USER_ERASEPG, and USER_PROG (0000062134-25)”: Changed “Fix to be implemented in the next design step” to “Fix implemented in the UI step.” Obsolete: PORT2 CTRAP active level (0000057330-1) SCU->OSC_CON Bit5 (0000057330-3) RESET pin pull-up (0000057330-4) ADC1 accuracy (0000057330-8) ADC2 accuracy (0000057330-9) DC parameters of Port 0, Port 1, TMS and Reset (0000057330-11)
Rev. 1.4	2022-09-23	DMA requests from SSC2 not cleared (0000045882-2296) added
Rev. 1.3	2022-06-03	BootROM - USER_NVM_ECC_CHECK (0000048454-124) obsolete
		CPU->SHPR2 wrong address (0000057330-2) obsolete
		MON wake-up/monitoring threshold voltage (0000048438-7) obsolete
		SCU->OSC_CON Bit5 (0000057330-3) obsolete
		BootROM USER_ERASE_SECTOR, USER_ERASEPG, and USER_PROG (0000062134-25) added
		Operational amplifier (0000057330-10) obsolete
Rev. 1.2	2019-09-17	BootROM - USER_NVM_ECC_CHECK (0000048454-124) added
		PORT2 CTRAP active level (0000057330-1) added
		CPU->SHPR2 wrong address (0000057330-2) added
		MON wake-up/monitoring threshold voltage (0000048438-7) added
		SCU->OSC_CON Bit5 (0000057330-3) added
		RESET pin pull-up (0000057330-4) added
		Operation amplifier (0000057330-10) added
		DC parameters of Port 0, Port 1, TMS and Reset (0000057330-11) added
		ADC1 accuracy (0000057330-8) added
		ADC2 accuracy (0000057330-9) added

Revision history

Revision	Date	Changes
Rev. 1.1	2018-05-02	Errata obsolete
		ADC1 Accuracy Addendum
		ADC2 Accuracy Addendum
Rev. 1.0	2017-05-17	Errata obsolete

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Edition 2025-09-15
Published by
Infineon Technologies AG
81726 Munich, Germany

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