Silicon errata for the PSOC™ 4 HVMS 64K product family

2025-03-21

About this document

Scope and purpose

This document describes the errata for PSOC™ 4 HVMS 64K product family.

Intended audience

This document is intended for the users who plan to use for PSOC™ 4 HVMS 64K devices in an application.

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1 Errata

This document describes the errata for PSOC™ 4 HVMS 64K Family. Details include trigger conditions, scope of impact, available workarounds, and applicable silicon revisions.

For more details, contact Infineon support.

Part numbers affected

Table 1 Part numbers affected

Part number
CY8C4126LCE-HVSxxx
CY8C4146LCE-HVSxxx
CY8C4126LDE-HVSxxx
CY8C4146LDE-HVSxxx
CY8C4126LWE-HVSxxx
CY8C4146LWE-HVSxxx

PSOC™ 4 HVMS 64K family qualification status

Product status: Production samples

PSOC™ 4 HVMS 64K family errata summary

The following table defines the errata applicable to PSOC™ 4 HVMS 64K series of devices.

Note: In the following table, errata items are hyperlinked. Click on any item entry to jump to its description.

Items	Part numbers	Silicon revision	Fix status
[1]. Errata ID 1 LIN Break detection using SCB-based LIN	CY8C4126LCE-HVSxxx CY8C4146LCE-HVSxxx CY8C4126LDE-HVSxxx CY8C4146LDE-HVSxxx CY8C4126LWE-HVSxxx CY8C4146LWE-HVSxxx	Rev. B0	Will not fix, To resolve this issue, use the workaround.
[2]. Errata ID 2 Bulk Erase SROM API does not analyze the Flash Row Protection bits			Will not fix, To resolve this issue, use the workaround.
[3]. Errata ID 3 Undocumented copies of SFLASH image			Will not fix
[4]. Errata ID 10 LIN wakeup not gated by the LIN rising edge			Will not fix To resolve this issue, use the workaround.

Items	Part numbers	Silicon revision	Fix status
[5]. Errata ID 11 CMOD pins (P4.0, P4.1, P4.2, P4.3) cannot be repurposed as mutual cap RX sensors			Will not fix

1. LIN Break detection using SCB-based LIN	
Problem definition	SCB may trigger a false Break detection on 10-bits wide Break field while spec requirement is 11 bits
Parameters affected	Break detection flag
Trigger condition(s)	Any consecutive 10 bits of dominant state
Scope of impact	Impacts SCB-based LIN only. LIN block is not impacted
Workaround	Use the LIN block in place of SCB (already the preferred choice)
Fix status	Will not fix. To resolve this issue, use the workaround

2. Bulk Erase SROM API does not analyze the Flash Row Protection bits	
Problem definition	The data in protected rows can be erased with bulk erase, but cannot be rewritten until row protection is removed
Parameters affected	None
Trigger condition(s)	Bulk erase a macro with protected rows
Scope of impact	Impacts the Bulk Erase API only. Other APIs prevent the erase program of protected rows
Workaround	Check Flash Row Protection bits before calling the Bulk Erase API.
Fix status	Will not fix. To resolve this issue, use the workaround.

3. Undocumented copies of SFLASH image	
Problem definition	The total possible SFLASH region size is 0x2000. Of this, HVMS64K SFLASH uses 0x400. The image of the used SFLASH is repeated to fill the SFLASH region size. For example, reads of 0x0fffe100, 0x0fffe500, and 0xfffe900 all return the same value.
Parameters affected	Memory map
Trigger condition(s)	Reads of address region is above the documented SFLASH range
Scope of impact	Impacts reads only. Writes require the SROM API and are not impacted.
Workaround	None
Fix status	Will not fix

4. LIN wakeup not gated by the LIN rising edge	
Problem definition	The LIN Phy includes a wakeup counter that can trigger an interrupt to transition the part from the Deep Sleep mode. The interrupt is triggered by the counter overflow and is not gated by a rising edge of the LIN bus because it is required by the LIN standard.
Parameters affected	Wakeup timing from Deep Sleep to Active
Trigger condition(s)	LIN wakeup signal sent over the LIN bus
Scope of impact	By switching to Active mode before the LIN rising edge, more power will be consumed and any wakeup log will be incorrect.
Workaround	Configure VirtLinRxd (P2.0) to generate a rising edge triggered interrupt. This will wake up the part on a LIN rising edge. The interrupt handler can evaluate the state of the Wakeup counter and decide whether a valid wakeup pulse was provided. If not, reset the wakeup counter and go back to Sleep to wait for the next rising edge.
Fix status	Will not fix. To resolve this issue, use the workaround.

5. CMOD pins (P4.0, P4.1, P4.2, P4.3) cannot be repurposed as mutual cap RX sensors	
Problem definition	Mutual cap RX operation is not possible when CMOD pins are configured as sensors
Parameters affected	Raw count and CAPSENSE™ CSX operation
Trigger condition(s)	CMOD pins used as mutual cap RX electrodes
Scope of impact	Raw count saturation
Workaround	None but these pins must not be assigned as CSX RX pins
Fix status	Will not fix

Revision history

Document revision	Date	Description of changes
**	2025-03-21	Initial release.

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