CY7C132*G, CY7C133*G, CY7C134*G, CY7C135*G, CY7C138*D, CY7C138*DV25, CY7C137*D, CY7C137*DV25, CY7C148*, CY7C148*V25, CY7C147*, CY7C147*V25.

January 30, 2012

Silicon Errata Document for RAM9 (90-nm), 72-Mb (CY7C147*/*V25, CY7C148*/*V25), 18-Mb (CY7C137*D/*DV25, CY7C138*D/*DV25) & 4-Mb (CY7C132/3/4/5*G) Synchronous & NoBL™ SRAMs

This document describes the Ram9 Sync/NOBL ZZ pin, JTAG and Chip Enable issues. Details include trigger conditions, the devices affected, proposed workaround and silicon revision applicability. Please contact your local Cypress sales representative if you have further questions.

Part Numbers Affected

Density & Revision	Package Type	Operating Range
4Mb-Ram9 Synchronous SRAMs: CY7C132*G, CY7C133*G, CY7C134*G, 4Mb-Ram9 NoBL™ SRAMs: CY7C135*G	All packages	Commercial/ Industrial
18Mb-Ram9 Synchronous SRAMs: CY7C138*D, CY7C138*DV25, 18Mb-Ram9 NoBL SRAMs: CY7C137*D, CY7C137*DV25	All packages	Commercial/ Industrial
72Mb-Ram9 Synchronous SRAMs: CY7C148*, CY7C148*V25, 72Mb-Ram9 NoBL SRAMs: CY7C147*, CY7C147*V25	All packages	Commercial/ Industrial

Product Status

All of the devices in the Ram9 4Mb/18Mb/72Mb Sync/NoBL family are qualified and available in production quantities.

Ram9 Sync/NoBL ZZ Pin, JTAG & Chip Enable Issues Errata Summary

The following table defines the errata applicable to available Ram9 4Mb/18Mb/72Mb Sync/NoBL family devices.

Item	Issues	Description	Device	Fix Status
1.	ZZ Pin	When asserted HIGH, the ZZ pin places device in a “sleep” condition with data integrity preserved.The ZZ pin currently does not have an internal pull-down resistor and hence cannot be left floating externally by the user during normal mode of operation.	4M-Ram9 (90nm) 18M-Ram9 (90nm) 72M-Ram9 (90nm)	For the 72M Ram9 (90 nm) devices, this issue was fixed in the new revision. Please contact your local sales rep for availability. For the 4M/18M Ram9 (90 nm) devices, there is no plan to fix this issue.
2.	JTAG Functionality	During JTAG test mode, the Boundary scan circuitry does not perform as described in the datasheet.However, it is possible to perform the JTAG test with these devices in “BYPASS mode”.	18M-Ram9 (90nm)	This issue will be fixed in the new revision, which use the 65 nm technology. Please contact your local sales rep for availability.
3.	Chip Enable	The internal Chip Enable CE3# pad is floating instead of being tied to Ground. This floating input may cause unstable behavior of the device during normal mode of operation.	18M-Ram9 Synchronous SRAMs 119-ball BGA package option only (90nm)	This issue was fixed in the new revision of the device by a substrate change. Please contact your local sales rep for availability.

1. ZZ Pin Issue

PROBLEM DEFINITION

The problem occurs only when the device is operated in the normal mode with ZZ pin left floating. The ZZ pin on the SRAM device does not have an internal pull-down resistor. Switching noise in the system may cause the SRAM to recognize a HIGH on the ZZ input, which may cause the SRAM to enter sleep mode. This could result in incorrect or undesirable operation of the SRAM.

TRIGGER CONDITIONS

Device operated with ZZ pin left floating.

SCOPE OF IMPACT

When the ZZ pin is left floating, the device delivers incorrect data.

WORKAROUND

Tie the ZZ pin externally to ground.

FIX STATUS

Fix was done for the 72Mb RAM9 Synchronous SRAMs and 72M RAM9 NoBL SRAMs devices. Fixed devices have a new revision. The following table lists the devices affected and the new revision after the fix.

Table 1. List of Affected Devices and the new revision

Revision before the Fix	New Revision after the Fix
CY7C148*	CY7C148*B
CY7C148*V25	CY7C148*BV25
CY7C147*	CY7C147*B
CY7C147*V25	CY7C147*BV25

2. JTAG Functionality

PROBLEM DEFINITION

The problem occurs only when the device is operated in the JTAG test mode.During this mode, the JTAG circuitry can perform incorrectly by delivering the incorrect data or the incorrect scan chain length.

TRIGGER CONDITIONS

Several conditions can trigger this failure mode.

1. The device can deliver an incorrect length scan chain when operating in JTAG mode.
2. Some Byte Write inputs only recognize a logic HIGH level when in JTAG mode.
3. Incorrect JTAG data can be read from the device when the ZZ input is tied HIGH during JTAG operation.

SCOPE OF IMPACT

The device fails for JTAG test. This does not impact the normal functionality of the device.

WORKAROUND

1.Perform JTAG testing with these devices in “BYPASS mode”.

2.Do not use JTAG test.

3. Chip Enable Issue

PROBLEM DEFINITION

The die used for CY7C138*D and CY7C138*DV25 has three Chip Enables, CE1#, CE2 and CE3#. The devices having part numbers CY7C138*D and CY7C138*DV25 (with 119-ball BGA package option only) utilize a single Chip Enable (CE1#) signal. CE2 and CE3# signals which are unused should be internally connected to Vcc and Ground respectively to keep them in “enabled” state, thus allowing CE1# to have full control of the chip. The internal Chip Enable CE3# pad is floating instead of being tied to Ground. This state of CE3# signal can result in incorrect or undesirable operation of the SRAM.

TRIGGER CONDITIONS
There are no specific trigger conditions. The issue can occur at any time during the normal operation of the device.

SCOPE OF IMPACT
This issue affects the normal functionality, and can cause unstable operation of the device.

WORKAROUND
Use the fixed revision of the device.

FIX STATUS
Fix was done for all the devices having this issue and was involved re-design of the substrate in order to have CE2 and CE3# pads bonded to Vcc and Ground lines respectively in the substrate. Fixed devices have a new revision. The following table lists the devices affected and the new revision after the fix.

Table 2. List of Affected Devices and the new revision

Revision after the Fix	New Revision after the Fix
CY7C138*D (119-ball BGA package)	CY7C138*F (119-ball BGA package)
CY7C138*DV25 (119-ball BGA package)	CY7C138*FV25 (119-ball BGA package)

References

All Ram9(90-nm) 72M/18M/4M Sync/NoBL data sheets

[1] Document # 38-05281, CY7C1481V25/CY7C1483V25/CY7C1487V25 2 M × 36/4 M × 18/1 M × 72 FLOW-THROUGH SRAM

[2] Document # 38-05282, CY7C1480V25/CY7C1482V25/CY7C1486V25 72-MBIT (2 M × 36/4 M × 18/1 M × 72) PIPELINED SYNC RAM

[3] Document # 38-05283,CY7C1480V33/CY7C1482V33/CY7C1486V33 72-MBIT (2 M × 36/4 M × 18/1 M × 72) PIPELINED SRAM

[4] Document # 38-05284,CY7C1481V33/1483V33/1487V33 72-MBIT (2 M × 36/4 M × 18/1 M × 72) FLOW-THROUGH SRAM

[5] Document # 38-05285,CY7C1484V33/CYC1485V33 72-MBIT (2 M × 36/4 M × 18) PIPELINED DCD SYNC SRAM

[6] Document # 38-05286,CY7C1484V25/CY7C1485V25 72-MBIT (2 M × 36/4 M × 18) PIPELINED DCD SYNC SRAM

[7] Document # 38-05287,CY7C1471V25/73V25/75V25 72-MBIT (2 M × 36/4 M × 18/1 M × 72) FLOW-THROUGH SRAM WITH NOBL(TM) ARCHITECTURE

[8] Document # 38-05288, CY7C1471V33/73/75 72-MBIT (2 M × 36/4 M × 18/1 M × 72) FLOW-THROUGH SRAM WITH NOBL(TM) ARCHITECTURE

[9] Document # 38-05289,CY7C1470V33/CY7C1472V33/CY7C1474V33 72-MBIT (2 M × 36/4 M × 18/1 M × 72) PIPELINED SRAM WITH NOBL(TM) ARCHITECTURE.

[10] Document # 38-05290,CY7C1470V25/*72*/*74* 72-MB (2 M × 36/4 M × 18/1 M × 72) PIPELINED SRAM WITH NOBL(TM) ARCHITECTURE

[11] Document # 38-05543, CY7C1380D/CY7C1382D 18-MBIT (512 K × 36/1 M × 18) PIPELINED SRAM

[12] Document # 38-05544, CY7C1381D/CY7C1383D 18-MB (512 K × 36/1 M × 18) FLOW-THROUGH SRAM

[13] Document # 38-05545,CY7C1386D/CY7C1387D 18-MB (512 K × 36/1 M × 18) PIPELINED DCD SYNC SRAM

[14] Document # 38-05546,CY7C1380DV25/CY7C1382DV25 18-MB (512 K × 36/1 M × 18) PIPELINED SRAM

[15] Document # 38-05547,CY7C1381DV25/CY7C1383DV25 18-MB (512 K × 36/1 M × 18) FLOW-THROUGH SRAM

[16] Document # 38-05548,CY7C1386DV25/CY7C1387DV25 18-MB (512 K × 36/1 M × 18) PIPELINED DCD SYNC SRAM

[17] Document # 38-05555,CY7C1370D/CY7C1372D 18-MBIT (512 K × 36/1 M × 18) PIPELINED SRAM WITH NOBL ARCHITECTURE

[18] Document # 38-05556, CY7C1371D/CY7C1373D 18-MB (512 K × 36/1 M × 18) FLOW-THROUGH SRAM WITH NOBL(TM) ARCHITECTURE

[19] Document # 38-05557,CY7C1371DV25/CY7C1373DV25 18-MB (512 K × 36/1 M × 18) FLOW-THROUGH SRAM WITH NOBL(TM) ARCHITECTURE

[20] Document # 38-05558,CY7C1370DV25/CY7C1372DV25 512 K × 36/1 M × 18 PIPELINED SRAM WITH NOBL(TM) ARCHITECTURE

[21] Document # 38-05518,CY7C1325G 4-MBIT (256 K × 18) FLOW-THROUGH SYNC SRAM

[22] Document # 38-05519,CY7C1327G 4-MBIT (256 K × 18) PIPELINED SYNC SRAM

[23] Document # 38-05523,CY7C1328G 4MBIT (256 K × 18) PIPELINED DCD SYNC SRAM

[24] Document # 38-05521,CY7C1338G 4-MBIT (128 K × 32) FLOW-THROUGH SYNC SRAM

[25] Document # 38-05520, CY7C1339G 4-MBIT (128 K × 32) PIPELINED SYNC SRAM

[26] Document # 38-05522, CY7C1340G 4-MB (128 K × 32) PIPELINED DCD SYNC SRAM

[27] Document # 38-05517, CY7C1345G 4-MBIT (128 K × 36) FLOW-THROUGH SYNC SRAM

[28] Document # 38-05516, CY7C1347G 4-MBIT (128 K × 36) FLOW-THROUGH SYNC SRAM

[29] Document # 38-05608, CY7C1348G 4-MBIT (128 K × 36) PIPELINED DCD SYNC SRAM

[30] Document # 38-05524, CY7C1350G 4-MBIT (128 K × 36) PIPELINED SRAM WITH NOBL(TM) ARCHITECTURE

[31] Document # 38-05513, CY7C1351G 4-MBIT (128 K × 36) FLOW-THROUGH SRAM WITH NOBL(TM) ARCHITECTURE

[32 Document # 38-05514, CY7C1352G 4-MBIT (256 K × 18) PIPELINED SRAM WITH NOBL(TM) ARCHITECTURE

[33] Document # 38-05515, CY7C1353G 4-MBIT (256 K × 18) FLOW-THROUGH SRAM WITH NOBL(TM) ARCHITECTURE

Document History Page

Document Title: Silicon Errata document for RAM9 (90-nm) 72-Mb (CY7C147*/*V25, CY7C148*/*V25), 18-Mb (CY7C137*D/*DV25, CY7C138*D/*DV25) & 4-Mb (CY7C132/3/4/5*G) Synchronous & NoBL™ SRAMs Document Number: 001-05804				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	414573	See ECN	REF	New errata for Ram 9 72Mb/18Mb/4Mb Sync/NOBL SRAM.
*A	422336	See ECN	NJY	Added JTAG functionality issue, Item#2.
*B	472990	See ECN	NJY	Added a workaround for JTAG issue.
*C	743176	See ECN	TBE	Added a Chip Enable issue, Item #3.
*D	1828248	See ECN	TBE	Updated the ZZ Pin Issue, Item #1.
*E	2184207	See ECN	TBE	Update the fix status in the JTAG and the ZZ Pin issues.
*F	3287549	06/20/2011	OSN	Updated in new template.
*G	3512161	01/30/2011	PRIT	Upload to Cypress.com

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