TLE92104-xxxxx errata

Z8F80454798

About this document

Scope and purpose

This errata sheet describes the deviations of the TLE92104-232QX, TLE92104-131QX from the current datasheets and shows the workaround principles.

Table 1 Current datasheets

Device	Release date
Infineon-TLE92104-232QX-DataSheet-v01_00-EN	2020-09-21
Infineon-TLE92104-131QX-DataSheet-v01_00-EN	2020-09-21

Intended audience

Engineers developing applications with the TLE92104-232QX, TLE92104-131QX.

Table of contents

About this document 1

Table of contents 2

1 Errata 3

1.1 Possible low-side drain-source overvoltage reported before expiration of the drain-source overvoltage filter time in PWM operation 3

1.2 Possible high-side drain-source overvoltage reported before expiration of the drain-source overvoltage filter time in PWM operation 3

2 References 5

Revision history 6

Disclaimer 7

1 Errata

1.1 Possible low-side drain-source overvoltage reported before expiration of the drain-source overvoltage filter time in PWM operation

Expected behavior

When the low-side (LS) MOSFET is the active MOSFET, after the expiration of the blank time (t_{BLANK}), the device does not detect a drain-source overvoltage (VDSOV) for a LS if:

- a falling edge of the internal LS control signal is generated
- while the drain-source voltage of the LS (V_{DS_LS}) exceeds the configured threshold ($V_{VDSMONTHx}$) for a duration shorter than the configured filter time (t_{FVDS})

The internal LS control signal is a control signal derived from the synchronized PWM signal.

A falling edge of the internal LS control signal signalizes that the LS MOSFET starts to be turned off, due to the PWM operation.

Actual behavior

After the expiration of t_{BLANK}, a VDSOV is detected for a LS if:

- a falling edge of the internal LS control signal is generated
- while $V_{DS_LS} > V_{VDSMONTHx}$ for $t < t_{FVDS}$ (see the figure below)

The LS is latched off and the VDSOV status bit of the corresponding LS is set.

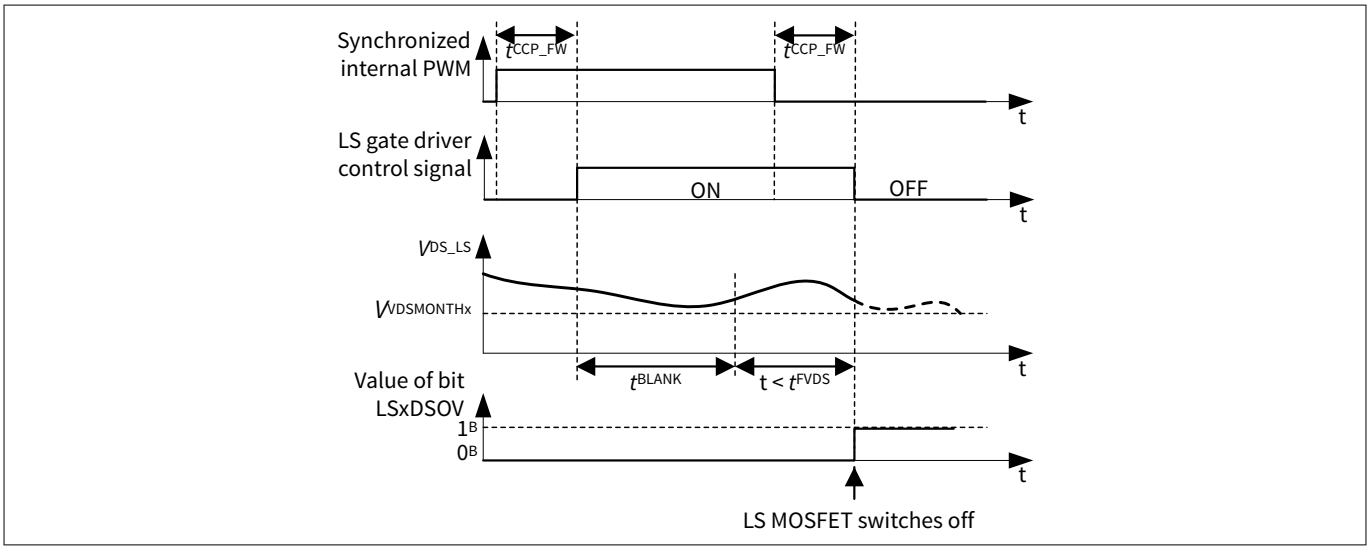


Figure 1 Falling edge of the internal LS control signal before the expiration of t_{FVDS}

Future action

Update the datasheets.

1.2 Possible high-side drain-source overvoltage reported before expiration of the drain-source overvoltage filter time in PWM operation

Expected behavior

When the HS MOSFET is the active MOSFET, after the expiration of t_{BLANK}, a VDSOV is not detected for a HS if:

1 Errata

- a falling edge of the internal HS control signal is generated
- while $V_{DS_HS} > V_{VDSMONTHx}$ for $t < t_{FVDS}$

V_{DS_HS} is the drain-source voltage of the high-side.

The internal HS control signal is a control signal derived from the synchronized PWM signal.

A falling edge of the internal HS control signal signalizes that the HS MOSFET starts to be turned off, due to the PWM operation.

Actual behavior

After the expiration of t_{BLANK}, a VDSOV is detected if:

- a falling edge of the internal HS control signal is generated
- while $V_{DS_HS} > V_{VDSMONTHx}$ for $t < t_{FVDS}$(see the figure below)

The device reaction is:

- the HS is latched off
- the VDSOV status bit of the HS is not set
- the VDSOV status bit of the LS from the same half-bridge is set

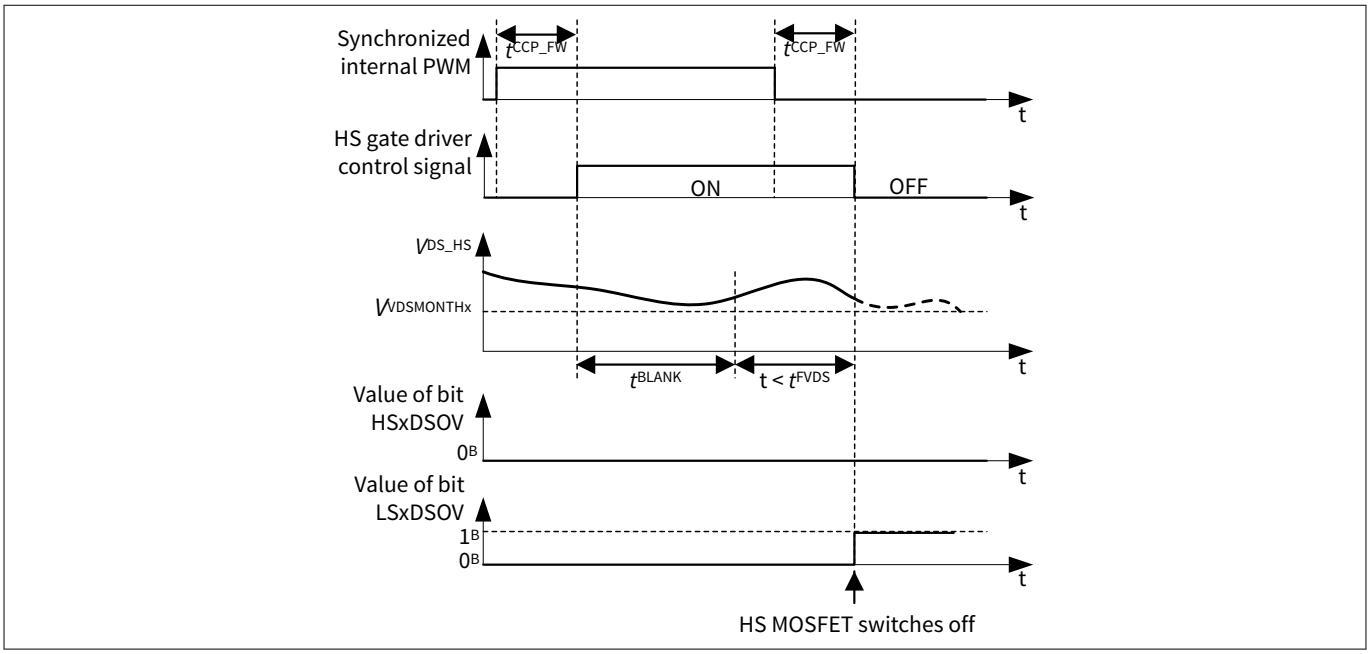


Figure 2 Falling edge of the internal HS control signal before the expiration of t_{FVDS}

Proposed workaround

Whenever a VDSOV is reported, perform an off-state diagnostic to confirm which MOSFET of the half-bridge is impacted.

Future action

Update the datasheets.

2 References

[1] TLE92104-232QX datasheet, Infineon-TLE92104-232QX-DataSheet-v01_00-EN, 2020-09-21

[2] TLE92104-131QX datasheet, Infineon-TLE92104-131QX-DataSheet-v01_00-EN, 2020-09-21

Revision history

Document version	Date of release	Description of changes
Rev. 2.00	2026-02-24	This errata is no longer applicable to TLE92108 devices following the release of its datasheet Revision 2.00.
Rev. 1.00	2023-05-01	First release

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