TRAVEO™ T2G CYT6BJ errata sheet

Marking/Step: Rev. B

32-bit single-chip microcontroller

About this document

Scope and purpose

This document describes the deviations of the device from the current user documentation, to support the assessment of the effects of these deviations on your custom hardware and software implementations.

Please take note of the following information:

- This errata sheet applies to all temperature and frequency versions and to all memory size variants, unless explicitly noted otherwise. For a derivative synopsis, see the latest datasheet or user manual
- Multiple device variants are covered in this one document. If an issue is related to a particular module, and this module is not specified for a specific device variant, then the issue does not apply to that device variant
- Devices marked with ES are engineering samples which may not be completely tested in all functional and electrical characteristics and are therefore only suitable for evaluation
- Some of the errata have workarounds which may be supported by the tool vendors. Some corresponding compiler switches may need to be set. Please refer to the respective documentation of your compiler
- To understand the effect of issues relating to the on-chip debug system, please refer to the respective debug tool vendor documentation

Current documentation

- TRAVEO™ T2G automotive MCU body controller high architecture reference manual
- TRAVEO™ T2G automotive MCU body controller high registers reference manual for CYT6BJ
- CYT6BJ datasheet TRAVEO™ T2G automotive MCU

Newer versions replace older versions, unless specifically stated otherwise.

Please always refer to the corresponding documentation for this device available in the category 'Documents' at www.infineon.com/TRAVEO™.

Conventions used in this document

Each erratum identifier follows the pattern [Number]:

- [Number] = ascending sequential number within the three

  ***Note**:* *[Number] As this sequence is used over several derivatives, including already solved deviations, gaps can occur inside this numbering sequence*

Table of contents

About this document . . . 1
Table of contents . . . 2
1 Errata overview . . . 3
2 Functional deviations . . . 5
Revision history of CYT6BJ errata sheet . . . 34
Disclaimer . . . 35

1 Errata overview

List of errata referenced in this document.

Table 1 Functional deviations

Issue title	Change	Page
[096] CAN FD RX FIFO top pointer feature does not function as expected		5
[097] CAN FD debug message handling state machine not get reset to Idle state when CANFD_CH_CCCR.INIT is set		5
[206] Hardfault may occur when the SROM APIs listed below while executing EraseSector or ProgramRow in non-blocking mode		6
[209] CAN FD sporadic data corruption (payload) in case acceptance filtering is not finished before reception of data R3 (DB7..DB4) is completed		7
[216]SMIF HSSPI (SDR/DDR) spec change for supported number of external memory devices		11
[218]Greater change of one Low voltage detection (LVD) level can issue an Over voltage detection (OVD) reset or another LVD interrupt		12
[229]System calls: improper usage of memory region end address in control logic		12
[234]Ethernet RGMII external mode issue		13
[237]CLK_HF5 cannot be configured as a separate, specific clock frequency for audio internal clock when CLK_HF4 is used for RGMII		14
[242]RTC busy status bit stuck issue		15
[243]System calls: ProgramWorkFlash and ProgramWorkFlash2 do not operate as expected except for the Work Flash address with 32 bits alignment		17
[244]WORK_INTERNAL_ERR bit can be set by a dummy read after work flash is erased/ programmed	changed	17
[245]CM7 power mode limitation		18
[250]SDHC: Wrong data written to external memory if system bus error occurs on last data beat during DMA transfer		19
[251]SDHC: Timeout error when BOOT ACK driven on all data lines in eMMC mode		20
[252]SDHC: AHB bus issue caused by insertion of wait cycles in a previous transfer		21
[253]SDHC: ADMA3 cannot be used		22
[254]SDHC: HW access flag for some registers is incorrect in Register TRM		23
[255]SDHC: Nst Timing of CMD12 STOP_TRANSMISSION command of SDHC is violated		23
[256]SDHC command response sampling failure when NCR equals 2 card clock cycles		24
[257]SDHC: Command queuing feature is not supported		25
[260]PLL may not be locked in certain scenarios		25
[261]Ethernet interrupt status flag description of SW/HW access in Register TRM is incorrect		27
[770]PLD might perform linefill to address that would generate a MemManage Fault (Arm® CM7 errata ID: 1013783)		28

(table continues...)

1 Errata overview

Table 1 (continued) Functional deviations

Issue title	Change	Page
[771]ECC error causes data corruption when the data cache error bank registers are locked (Arm® CM7 errata ID: 1267980)		29
[772]Data corruption for load following Store-Exclusive (Arm® CM7 errata ID: 1315869)		30
[773]TCM bandwidth sharing between AHBS writes and software stores might not function correctly when using TCM wait states (Arm® CM7 errata ID: 2328489)		31
[774]Cortex®-M7 can halt in an incorrect address when breakpoint and exception occurs simultaneously (Arm® CM7 errata ID: 3092511)		32

2 Functional deviations

2.1 [096] CAN FD RX FIFO top pointer feature does not function as expected

Description

RX FIFO top pointer function calculates the address for received messages in Message RAM by hardware. This address should be re-start back from the start address after reading all messages of RX FIFO n size (n: 0 or 1). However, the address does not re-start back from the start address when RX FIFO n size is set to 1 (CANFD_CH_RXFnC.FnS = 0x01). This results in CPU/DMA to read messages from the wrong address in Message RAM.

Parameters affected

N/A

Trigger condition(s)

RX FIFO top pointer function is used when RX FIFO n size set to 1 element (CANFD_CH_RXFnC.FnS = 0x01).

Scope of impact

Received message cannot be correctly read by using RX FIFO top pointer function, when RX FIFO n size set to 1 element.

Workaround

Any of the following

1. Set RX FIFO n size to 2 or more when using RX FIFO top pointer function.
2. Do not use RX FIFO top pointer function when RX FIFO n size set to 1 element. Instead of RX FIFO top pointer, read received messages from the Message RAM directly.

Fix status

No silicon fix planned. Use workaround.

2.2 [097] CAN FD debug message handling state machine not get reset to Idle state when CANFD_CH_CCCR.INIT is set

Description

If either CANFD_CH_CCCR.INIT bit is set by the Host or when the M_TTCAN module enters BusOff state, the debug message handling state machine stays in its current state instead of being reset to Idle state. Configuring the bit CANFD_CH_CCCR.CCE does not change CANFD_CH_RXF1S.DMS.

Parameters affected

N/A

Trigger condition(s)

Either CANFD_CH_CCCR.INIT bit is set by the Host or when the M_TTCAN module enters BusOff state.

Scope of impact

The errata is limited to the use case when the Debug on CAN functionality is active. Normal operation of CAN module is not affected, in which case the debug message handling state machine always remains in Idle state. In the described use case, the debug message handling state machine is stopped and remains in the current state signaled by the bit CANFD_CH_RXF1S.DMS. In case CANFD_CH_RXF1S.DMS is set to 0b11, DMA request remains active. Bosch classifies this as non-critical error with low severity, there is no fix for the IP, Bosch recommends the workaround listed also here.

Workaround

In case the debug message handling state machine has stopped while CANFD_CH_RXF1S.DMS is 0b01 or 0b10, it can be reset to Idle state by hardware reset or by reception of debug messages after CANFD_CH_CCCR.INIT is reset to zero.

Fix status

No silicon fix planned. Use workaround.

2.3 [206] Hardfault may occur when the SROM APIs listed below while executing EraseSector or ProgramRow in non-blocking mode

Description

The following SROM APIs read data from bank#0 (or bank#1 if dual bank mode with mapping B is used) in SFlash. While doing that the check for active non-blocking erase or program of bank#0 (or bank#1 if dual bank mode with mapping B is used) is not performed. Therefore, reading bank#0 (or bank#1 if dual bank mode with mapping B is used) while there is an active erase/program operation triggers a bus error. This results in a hardfault occurrence based on FLASHC_FLASH_CTL register settings.

Affected SROM APIs:

- ReadSWPU
- WriteSWPU
- GenerateHash
- Checksum[1)]
- ComputeBasicHash[1)]
- CheckFactoryHash
- ProgramWorkFlash[2)]
- SwitchOverRegulators (not for CYT2B6/7/9/L, CYT2CL)
- LoadRegulatorsTrims (not for CYT2B6/7/9/L, CYT2CL)

Parameters affected

N/A

Trigger condition(s)

Calling the affected SROM APIs while executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used).

1 Do not call it to calculate on the bank where programming/erasing is in progress
2 Do not use it during non-blocking operation

Scope of Impact

The affected SROM APIs cannot be used while executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used).

Workaround

Do not use the affected SROM APIs while executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used).

Fix status

No silicon fix planned.

The architecture technical reference manuals were updated:

- 002-19314 Rev. *J for body controller entry family
- 002-24401 Rev. *H for body controller high family
- 002-33175 Rev. *D for cluster entry family
- 002-25800 Rev. *F for cluster 2D family

Impact on Infineon software

Impact: Limitation

Related modules: S-LLD, HSM-Perf-Lib

Comment: While executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used), users must not do anything of following:

1. Call CySldProt_GetSwpuFlashStructCfg
2. Call CySldProt_VerifySecureDomainFlashWriteProtection if CySldProt_SwpuFlashStructGroupConfigurations is non-empty

2.4 [209] CAN FD sporadic data corruption (payload) in case acceptance filtering is not finished before reception of data R3 (DB7..DB4) is completed

Description

During frame reception the Rx Handler accesses the external Message RAM for acceptance filtering (read accesses) and for storing of the accepted messages (write accesses).

The time needed for acceptance filtering and for storing of a received message depends on

- the Host clock frequency
- the worst-case latency of the read and write accesses to the external Message RAM
- the number of configured filter elements
- the workload of the transmit message (Tx) handler in parallel to the receive message (Rx) handler

Received data bytes (DB0..DBm) from the CAN Core are buffered in the cache of the Rx Handler before they are written to the Message RAM (in words of 4 byte). Data words inside the Message RAM are numbered from R2 to Rn (n ≤ 17).

2 Functional deviations

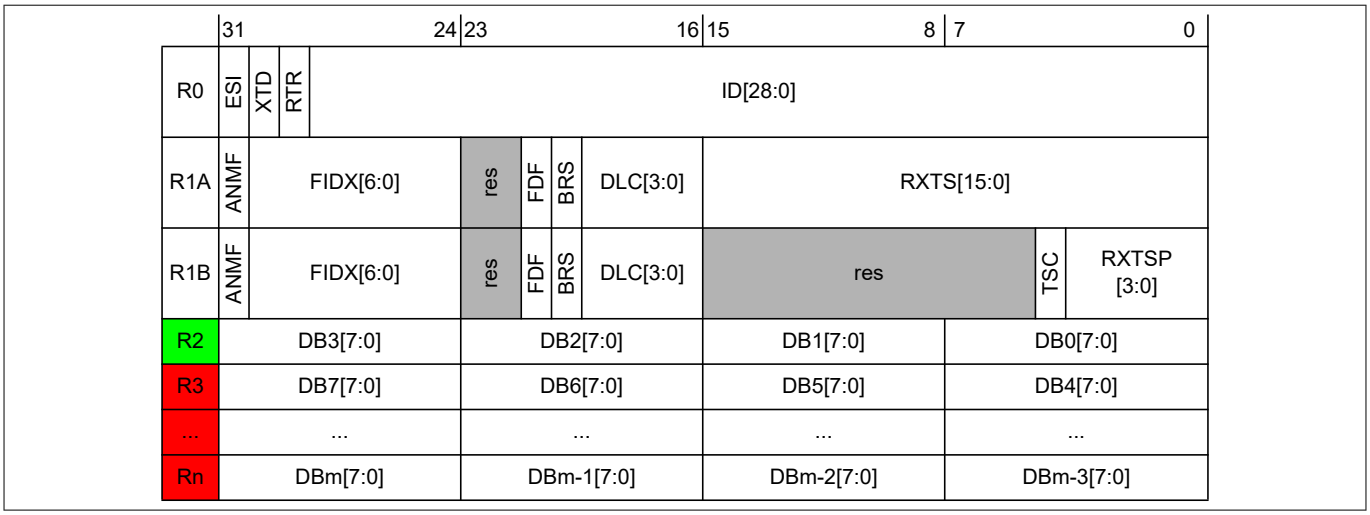

Figure 1 Rx Buffer and FIFO Element

Under the following conditions a received message will have corrupted data while the received message is signaled as valid to the host.

1. The data length code (DLC) of the received Message is greater than 4 (DLC > 4)
2. The storage of Ri of a received message into the Message RAM (after acceptance filtering is done) has not completed before R(i+1) is transferred from the CAN Core into the cache of the Rx Handler (where 2 ≤ i ≤ 5)
3. While condition 1 and 2 apply, a concurrent read of data word Ri from the cache and write of data word R(i+1) into the cache of the Rx handler happens

The data will be corrupted in a way, that in the Message RAM R(i+1) has the same content as Ri.

Despite the corrupted data, the M_TTCAN signals the storage of a valid frame in the Message RAM:

- Rx FIFO: FIFO put index RXFnS.FnPI is updated
- Dedicated Rx Buffer: New Data flag NDATn.NDxx is set
- Interrupt flag IR.MRAF is not set

The issue may occur in FD Frame Format as well as in Classic Frame Format.

Figure 2 shows how the available time for acceptance filtering and storage is reduced.

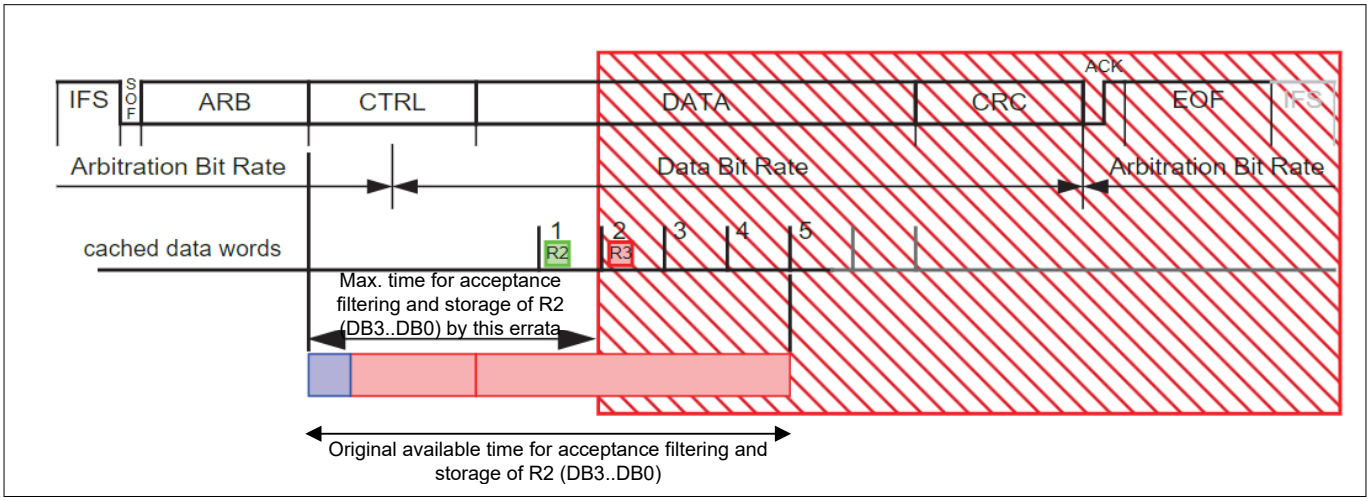

Figure 2 CAN frame with DLC > 4

2 Functional deviations

Table 2 TRAVEO™ T2G: Minimum host clock frequency for CAN FD when DLC = 5

Number of configured active filter element 11-bit IDs/29-bit IDs[1) 2)]	Number of active CAN channels in an instance[3)]	Arbitration bit rate = 0.5 Mbps				Arbitration bit rate = 1 Mbps			
		Data bit rate = 0.5 Mbps	Data bit rate = 1 Mbps	Data bit rate = 2 Mbps	Data bit rate = 4 Mbps	Data bit rate = 1 Mbps	Data bit rate = 2 Mbps	Data bit rate = 4 Mbps	Data bit rate = 5 Mbps
32/16	2	3.9 MHz	7.1 MHz	13.1 MHz	22.8 MHz	7.7 MHz	14.1 MHz	26.1 MHz	31.5 MHz
	3	5.4 MHz	9.9 MHz	18.3 MHz	31.8 MHz	10.7 MHz	19.7 MHz	36.5 MHz	44.0 MHz
	4	6.9 MHz	12.7 MHz	23.5 MHz	40.8 MHz	13.8 MHz	25.3 MHz	46.9 MHz	56.5 MHz
	5	8.4 MHz	15.5 MHz	28.6 MHz	49.9 MHz	16.8 MHz	30.9 MHz	57.2 MHz	69.0 MHz
64/32	2	7.4 MHz	13.5 MHz	24.9 MHz	43.4 MHz	14.7 MHz	26.9 MHz	49.8 MHz	60.0 MHz
	3	10.3 MHz	18.8 MHz	34.9 MHz	60.7 MHz	20.5 MHz	37.6 MHz	69.7 MHz	84.0 MHz[4)]
	4	13.2 MHz	24.2 MHz	44.8 MHz	78.0 MHz	26.3 MHz	48.4 MHz	89.5 MHz[4)]	107.9 MHz[5)]
	5	16.1 MHz	29.6 MHz	54.7 MHz	95.3 MHz[4)]	32.1 MHz	59.1 MHz	109.4 MHz[5)]	131.8 MHz[5)]
96/48	2	10. 8 MHz	19.9 MHz	36.8 MHz	64.0 MHz	21.6 MHz	39.7 MHz	73.5 MHz	88.6 MHz[4)]
	3	15.1 MHz	27.8 MHz	51.5 MHz	89.6 MHz[4)]	30.2 MHz	55.6 MHz	102.9 MHz[5)]	124.0 MHz[5)]
	4	19.4 MHz	35.7 MHz	66.1 MHz	115.1 MHz[5)]	38.8 MHz	71.4 MHz	132.2 MHz[5)]	159.3 MHz[5)]
	5	23.7 MHz	43.6 MHz	80.8 MHz[4)]	140.7 MHz[5)]	47.4 MHz	87.2 MHz[4)]	161.5 MHz[5)]	194.7 MHz[5)]
128/64	2	14.3 MHz	26.3 MHz	48.6 MHz	84.7 MHz[4)]	28.4 MHz	52.5 MHz	97.2 MHz[4)]	117.2 MHz[5)]
	3	20.0 MHz	36.8 MHz	68.0 MHz	118.5 MHz[5)]	40.0 MHz	73.5 MHz	136.0 MHz[5)]	164.0 MHz[5)]
	4	25.7 MHz	47.2 MHz	87.5 MHz[4)]	152.3 MHz[5)]	51.4 MHz	94.4 MHz[4)]	174.9 MHz[5)]	210.8 MHz[5)]
	5	31.4 MHz	57.7 MHz	106.9 MHz[5)]	186.1 MHz[5)]	62.7 MHz	115.4 MHz[5)]	213.7 MHz[5)]	257.5 MHz[5)]

1) M_TTCAN starts always at filter element #0 and proceeds through the filter list to find a matching element. Acceptance filtering stops at the first matching element and the following filter elements are not evaluated for this message. Therefore, the sequence of configured filter elements has a significant impact on the performance of the filtering process.
2) Acceptance filtering search for 11-bit IDs and 29-bit IDs filter element is running separately, only one configured filter setting should be considered. Searching for one 29-bit filter element requires approximately double cycles for one 11-bit filter element.
3) See the device datasheet for the supported number of channels
4) Frequency is not reachable since the maximum host clock frequency for M_TTCAN in CYT2B6 is 80 MHz
5) Frequency is not reachable since the maximum host clock frequency for M_TTCAN in all TRAVEO™ T2G is 100 MHz

2 Functional deviations

Parameters Affected

N/A

Trigger condition(s)

Under the following conditions a received message will have corrupted data while the received message is signaled as valid to the host.

1. The data length code (DLC) of the received Message is greater than 4 (DLC > 4)
2. The storage of Ri of a received message into the Message RAM (after acceptance filtering is done) has not completed before R(i+1) is transferred from the CAN Core into the cache of the Rx Handler (where 2 ≤ i ≤ 5)
3. While condition 1 and 2 apply, a concurrent read of data word Ri from the cache and write of data word R(i+1) into the cache of the Rx handler happens

Scope of impact

The erratum is limited to the case when the Host clock frequency used in the actual device is below the limit shown in Table 2.

Corrupted data is written to the Rx FIFO element respective the dedicated Rx Buffer.

The received frame is nevertheless signaled as valid.

Workaround

Check whether the minimum Host clock frequency, that is shown in Table 2, is below the Host clock frequency used in the actual device.

If yes, there is no problem with the selected configuration.

If no, use one of the following two workarounds.

<First workaround>

Try different configuration by changing the following parameters until the actual host clock frequency (CLK_GR5) is above the minimum host frequency shown in Table 2.

- Increase the CLK_GR5 frequency in the actual device
- Reduce the CAN-FD Data Bit rate
- Reduce the number of configured filter elements
- Reduce the number of active CAN channels in an instance

Also, use DLC>=8 instead of DLCs 5, 6, and 7 in the CAN Environment/System, as they place higher demands on the minimum Host clock frequency (the worst case is DLC=5) or restrict your CAN Environment/System to DLC 4.

Note: While changing the actual host clock frequency, CLK_GR5 must always be equal or higher than PCLK_CANFD[x]_CLOCK_CAN[y] for all configurations.

<Second workaround>

Due to condition 3 the issue occurs only sporadically. Use an end-to-end (E2E) protection (for example, checksum or CRC covering the data field) and add it to all messages in the CAN system, to detect data corruption in received frames.

Fix status

No silicon fix planned. Use workaround.

Impact on Infineon software

Impact: Limitation

Related modules: CAN, MCU

Comment: The user must evaluate the impact of the erratum for each CAN instance separately. A CAN instance is the entirety of CanControllers with the same CanControllerInstance value.

1. For the number of active CAN nodes: Use the maximum number of CanController configurations of a CAN instance that can be active (Autosar controller state STARTED or SLEEP) at a time
2. For the host clock frequency: In McuPeriGroupSettings locate the setting with McuPeriGroup=MCU_PERI_GROUP5_MMIO5 and take the value from McuPeriGroupClockFrequency
3. For the number of configured active filter element 11-bit IDs/29-bit IDs: Use the corresponding values from the “Message RAM (…) linking table” in the generated Can_PBcfg.h file. Note that each CanController has its separate table. Take the maximum values.
4. For the Arbitration bit rate: Use the maximum CanControllerBaudRate value of all the CanControllers
5. For the Data bit rate: Use the maximum CanControllerFdBaudRate value of all the CanControllers if configured. Otherwise use CanControllerBaudRate.

2.5 [216]SMIF HSSPI (SDR/DDR) spec change for supported number of external memory devices

Description

SMIF supports two external memories. However, CYT6BJ does not support the HSSPI (SDR/DDR) modes with two external memory devices because there is a glitch on the clock line during signal transitions and then functional failure of the protocol can happen. Therefore, the architecture reference manual has been updated to add a note that CYT6BJ does not support the HSSPI (SDR/DDR) modes with two external memories.

Parameter affected

N/A

Trigger condition(s)

Using the HSSPI (SDR/DDR) with two external memory devices in SMIF

Scope of impact

The number of supported external memory devices is changed to one from two.

Workaround

Do not use the HSSPI (SDR/DDR) with two external memory devices in SMIF.

Fix status

No silicon fixed planned.

Impact on Infineon software

Impact: No
Related modules: None
Comment: Software in scope does not support the SMIF.

2.6 [218]Greater change of one Low voltage detection (LVD) level can issue an Over voltage detection (OVD) reset or another LVD interrupt

Description

OVD and LVD1/2 share the common resistor ladder for reference voltages. Therefore, greater change of one LVD level can cause greater voltage fluctuation at OVD/another LVD reference voltage leading to OVD reset or another LVD interrupt.

Parameter affected

N/A

Trigger condition(s)

Change of LVD trip selection bits (PWR_LVD_CTL/2.HVLVD1/2_TRIPSEL_HT) by a step width of more than 1 at V_{DDD} > 4.5 V.

Scope of impact

Greater change of one LVD level can result in an OVD reset or another LVD interrupt.

Workaround

Any of the following

1. Do not change LVD trip selection bits (PWR_LVD_CTL/2.HVLVD1/2_TRIPSEL_HT) from default setting 0.
2. Increment LVD trip selection bits (PWR_LVD_CTL/2.HVLVD1/2_TRIPSEL_HT) by a step width of 1 per 10 µs. Change LVD1 or LVD2 independently, not at the same time.

Fix status

No silicon fix planned. Use workaround.

The architecture technical reference manuals were updated:

- 002-19314 Rev. *J for body controller entry family
- 002-24401 Rev. *H for body controller high family
- 002-33175 Rev. *D for cluster entry family
- 002-25800 Rev. *F for cluster 2D family

Impact on Infineon software

Impact: Limitation

Related modules: MCU

Comment: Workaround (2) was implemented in MCAL MCU driver version 1.24. Users of older versions can apply one of the suggested workarounds in following ways: Leave McuHvLvdThreshold at its default value of MCU_HVLVD_THRESHOLD_2_8V_TO_2_825V, or apply MCU configurations with changes of McuHvLvdThreshold in steps of 0.1V only.

2.7 [229]System calls: improper usage of memory region end address in control logic

Description

Erroneous system calls execution status will be returned when passing parameters to system calls via SRAM region at the end of available SRAM.

Parameters affected

N/A

Trigger condition(s)

When SRAM_SCRATCH_DATA_ADDR for the following system calls end in the last available SRAM word:

- ProgramRow
- ProgramRow2 (only for CYT6BJ)
- ProgramWorkFlash
- ProgramWorkFlash2 (only for CYT6BJ)

Scope of impact

0xF0000013 (invalid arguments location) will be returned when passing parameters to system calls via SRAM region at the end of available SRAM.

Workaround

Do not use the last word of available SRAM for passing SRAM_SCRATCH_DATA_ADDR for the following system calls:

- ProgramRow
- ProgramRow2 (only for CYT6BJ)
- ProgramWorkFlash
- ProgramWorkFlash2 (only for CYT6BJ)

Fix status

No silicon fix planned. Use workaround.

Impact on Infineon software

Impact: Limitation

Related modules: FLS

Comment: Users of MCAL FLS must make sure that Fls_WriteData is not located immediately below the highest SRAM address. You can use memory mapping via FLS_START_SEC_VAR_NO_INIT_UNSPECIFIED and/or linker configuration to modify the location of the affected object.

2.8 [234]Ethernet RGMII external mode issue

Description

Ethernet RGMII cannot be supported as external mode.

Parameter affected

SID385/B, SID386/B, SID385_1/4, SID385B_1

Trigger condition(s)

Using RGMII

Scope of impact

- The support mode for RGMII has been changed to internal mode from external mode.
- ECO accuracy must be within +/- 50 ppm.

- For CYT6BJ, CYT4EN Rev. B and CYT4FK devices, the internal mode requires that REF_CLK 125 MHz should be created by using the internal PLL clock frequency (PLL_OUT) 250 MHz with 2 dividing of OUTPUT_DIV and divided by 2 with the register ETHx_CTL.REFCLK_DIV = '1' setting.
- For CYT4BF device, no requirement for the internal PLL clock frequency (PLL_OUT) 250 MHz.
- For CYT4DN device, the internal mode requires that REF_CLK 125 MHz should be created by using the internal PLL clock frequency (PLL_OUT) 250 MHz with 2 dividing of OUTPUT_DIV and divided by 2 with the register CLK_ROOT_SELECT[x].ROOT_DIV = '1' setting.

Workaround

Use the RGMII internal mode instead of external mode.

Fix status

No silicon fixed planned. Use workaround. Datasheets will be updated accordingly.

Impact on Infineon software

Impact: No

Related modules: None

Comment: Software in scope does not support the Ethernet

2.9 [237]CLK_HF5 cannot be configured as a separate, specific clock frequency for audio internal clock when CLK_HF4 is used for RGMII

Description

CLK_HF5 cannot be configured as a separate, specific clock frequency for audio internal clock when CLK_HF4 is used for RGMII because there is only one PLL (PLL400#1), which is common to CLK_HF4 and CLK_HF5.

Parameter affected

SID748

Trigger condition(s)

Using both of CLK_HF4 and CLK_HF5

Scope of impact

CLK_HF5 cannot be configured as a separate, specific frequency like 196.608 MHz of SID748 when CLK_HF4 is used for RGMII.

Workaround

Any of following:

1. Use the audio subsystem with the external clock via AUDIOSSx_CLK_I2S_IF pin
2. Use the same PLL frequency for CLK_HF5 as for CLK_HF4. In this case, the following conditions must be met:
   - Use the audio subsystem as slave (MCLK must be generated by the external master)
   - Use the audio subsystem internal clock (MCLK_SOC) frequency is 8 times or more than the frequency of the input serial clock (MCLK)
   - For CYT6BJ Rev. B RGMII 1 Gbps, PLL400#1 250 MHz is required and then CLK_HF5 can be used at 125 MHz by dividing 250 MHz of PLL400#1 by 2 using pre-divider.
   - For CYT4BF RGMII 1Gbps, PLL400#1 125 MHz is required and then CLK_HF5 can be used at 125 MHz by dividing 125 MHz of PLL400#1 by 1 using pre-divider.

Fix status

No silicon fixed planned. Use workaround.

Impact on Infineon software

Impact: Limitation

Related modules: None

Comment:

1. Clock roots for Audio and Ethernet are configured in the McuClockRootSettings container of the MCAL MCU module. PLLs are configured in the McuPllSettings container of the MCAL MCU module
2. The configuration of the I2S clock selection is out of scope of the software in scope

2.10 [242]RTC busy status bit stuck issue

Description

RTC busy status flag (BACKUP_STATUS.RTC_BUSY register bit) is abnormally stuck at HIGH even after configuring the RTC user registers and BACKUP_RTC_RW.WRITE register bit is cleared by the software.

Parameter affected

N/A

Trigger condition(s)

RTC user register write operation randomly triggers this problem.

Scope of impact

RTC operation may not work as expected. If the software polls BACKUP_STATUS.RTC_BUSY flag before moving to any other tasks, it will be stuck there.

Workaround

Use the following software workaround:

1. If BACKUP_STATUS.RTC_BUSY flag is set, then run the following dummy write sequence
2. Start the sequence for maximum 8 retries (‘retryCount’) and start with 1
   - **a.** Write ‘1’ to BACKUP_RTC_RW.WRITE register for 'retryCount' times
   - **b.** Write ‘0’ to BACKIP_RTC_RW.WRITE register
   - **c.** Wait for 6 CLK_LF cycles (ILO0 or WCO)
   - **d.** If BACKUP_STATUS.RTC_BUSY flag is ‘0’, exit the loop
   - **e.** If ‘retryCount’ reaches to ‘8’, then handle this error according to user system requirement for failure case unrelated to this errata (e.g. write '1' to BACKUP_RESET.RESET register) else run dummy write sequence from “a”. Workaround for this errata needs to maximum 8 retries.

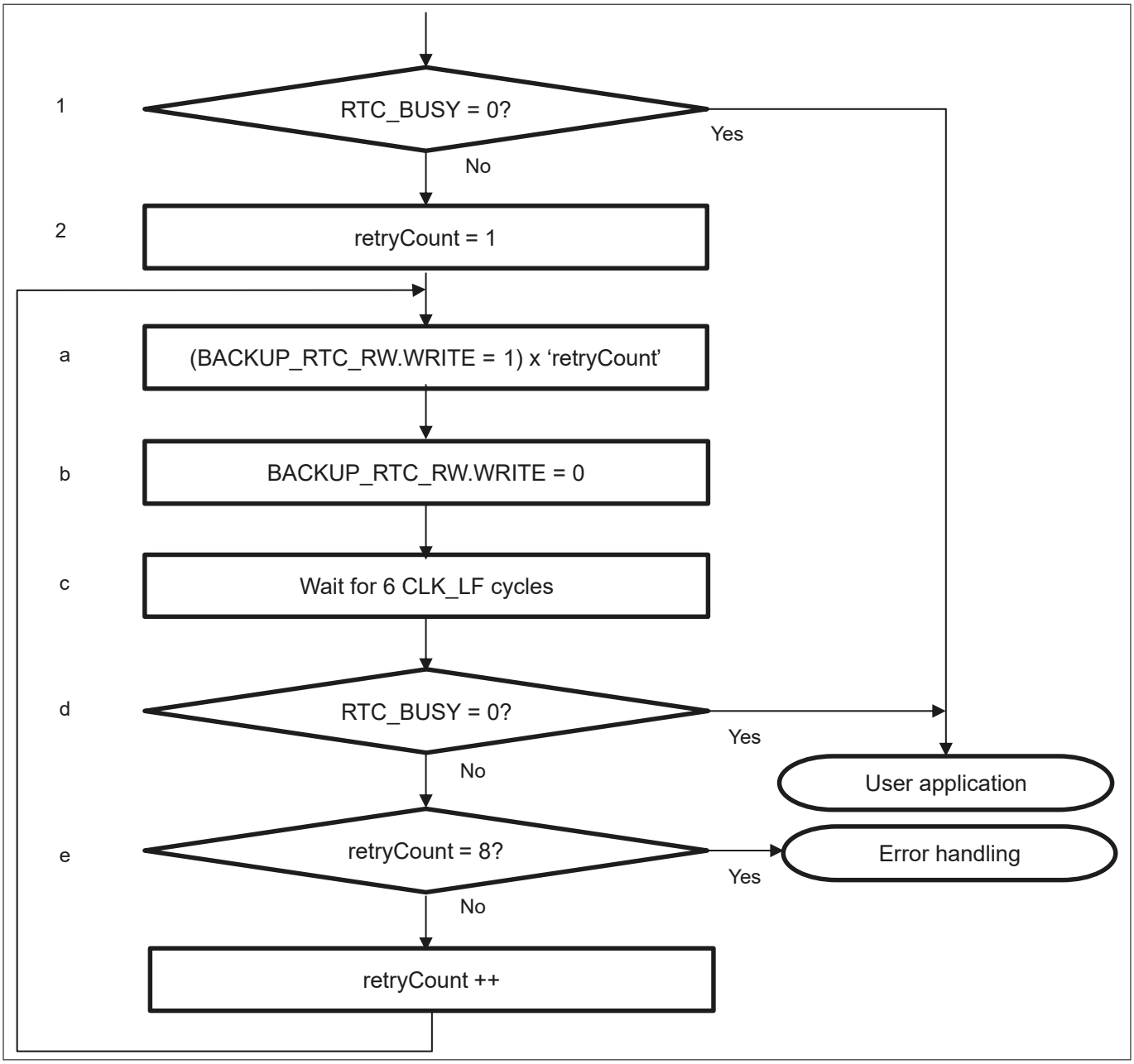

Figure 3 RTC software workaround

Fix status

No silicon fix planned. Use workaround.

Impact on Infineon software

Impact: None
Related modules: N/A
Comments: Software in scope does not access RTC registers.

2.11 [243]System calls: ProgramWorkFlash and ProgramWorkFlash2 do not operate as expected except for the Work Flash address with 32 bits alignment

Description

ProgramWorkFlash and ProgramWorkFlash2 (only for CYT6BJ) perform correct write operation only if the "Work flash address" argument passed to the ProgramWorkFlash/2 is aligned with "Data size" argument passed to the ProgramWorkFlash/2. Otherwise the ProgramWorkFlash/2 performs write operation to the unexpected Work flash area.

Parameters affected

N/A

Trigger condition(s)

If the "Work flash address" argument passed to the ProgramWorkFlash/2 is not aligned with "Data size" argument passed to the ProgramWorkFlash/2.

Scope of impact

This issue can perform write operation to the unexpected Work flash area.

Workaround

Use "Work flash address to be programmed" aligned with "Data size" argument.

[e.g., for Data size = 3 (64 bits) Work flash address must be aligned with 64 bits, for Data size = 4 (128 bits) Work flash address must be aligned with 128 bits, etc.]

For Data size = 2 (32 bits) the ProgramWorkFlash/2 works correct always.

Fix status

No silicon fix planned. Use workaround.

Impact on Infineon software

Impact: No

Related modules: MCAL FLS, FEE

Comment: FLS of MCAL uses ProgramRow, not ProgramWorkFlash or ProgramWorkFlash2. MCAL FLS in certain NRE services will use ProgramWorkFlash and contain a workaround for this erratum. FEE uses FLS to write to flash.

2.12 [244]WORK_INTERNAL_ERR bit can be set by a dummy read after work flash is erased/programmed

Description

1. When blocking mode is used for work flash erase/program, the dummy read is performed by the SROM API itself. However, the SROM API does not clear the WORK_INTERNAL_ERR bit in FLASHC_CM0_STATUS register or handle it even if it is set.
2. When non-blocking mode is used for work flash erase/program, the dummy read has to be done by user software. In this case, the WORK_INTERNAL_ERR bit can be set either on FLASHC_CM0_STATUS register or on FLASHC_CM4(or CM7_x)_STATUS register depending on which CPU first does the dummy read.

Parameter affected

N/A

Trigger condition(s)

A dummy read after work flash is erased/programmed

Scope of impact

WORK_INTERNAL_ERR bit handling needs to be done after a dummy read after work flash is erased/ programmed.

Workaround

- For problem 1, user software needs to clear the WORK_INTERNAL_ERR bit in FLASHC_CM0_STATUS register if it was set. If the first dummy read happened from CM4/CM7_x before the dummy read performed by the SROM API, then the WORK_INTERNAL_ERR bit may get set in FLASHC_CM4(or CM7_x)_STATUS register and user software needs to clear this bit.
- For problem 2, user software needs to clear the WORK_INTERNAL_ERR bit either on FLASHC_CM0_STATUS register or on FLASHC_CM4(or CM7_x)_STATUS register depending on which CPU first does the dummy read.

Fix status

No silicon fixed planned. Use workaround.

Impact on Infineon software

Impact: Limitation

Related modules: FLS

Comment: MCAL FLS clears the WORK_INTERNAL_ERR flag before activities that can cause the flag to indicate an error, and MCAL FLS checks and clears the flag after those activities. It may leave the flag active between API calls.

2.13 [245]CM7 power mode limitation

Description

When the power mode of CM7_x is changed to OFF, RESET, RETAINED by the CPUSS_CM7_x_PWR_CTL.PWR_MODE register, then the AXI infrastructure behavior can get undefined. This may corrupt transactions from CM7_x itself after its power mode is changed to ENABLED again, or transactions from other masters even while CM7_x is still in OFF, RESET, RETAINED power mode.

Parameter affected

N/A

Trigger condition(s)

Any of following:

1. Programming CPUSS_CM7_x_PWR_CTL.PWR_MODE register to RESET or OFF and not RETAINED while the CLK_MEM frequency is higher than 1/8 of the CLK_FAST_x frequency
2. Programming CPUSS_CM7_x_PWR_CTL.PWR_MODE register to RETAINED while the CLK_MEM frequency is higher than 1/12 of the CLK_FAST_x frequency

Scope of impact

This erratum affects all configurations of the Cortex®-M7 processor.

Workaround

1. In case of changing CPUSS_CM7_x_PWR_CTL.PWR_MODE = RESET or OFF and not RETAINED

   Before changing CPUSS_CM7_x_PWR_CTL.PWR_MODE = OFF | RESET, reduce the frequency of CLK_MEM to be lesser or equal to 1/8 of the frequency of CLK_FAST_x. Instead of directly writing the CPUSS_CM7_x_PWR_CTL register, the following sequence should be applied:

   a. Write CPUSS_MEM_CLOCK_CTL with a divider value to get 1/8 or less of the speed of CLK_FAST_x
   b. Set the desired power mode [OFF | RESET] in CPUSS_CM7_x_PWR_CTL.PWR_MODE
   c. Program original CPUSS_MEM_CLOCK_CTL settings, if desired
2. In case of changing CPUSS_CM7_x_PWR_CTL.PWR_MODE = RETAINED

   Before changing CPUSS_CM7_x_PWR_CTL.PWR_MODE = RETAINED, reduce the frequency of CLK_MEM to be lesser or equal to 1/12 of the frequency of CLK_FAST_x. Instead of directly writing the CPUSS_CM7_x_PWR_CTL register, the following sequence should be applied:

   a. Write CPUSS_MEM_CLOCK_CTL with a divider value to get 1/12 or less of the speed of CLK_FAST_x
   b. Set the desired power mode [RETAINED] in CPUSS_CM7_x_PWR_CTL.PWR_MODE
   c. Program original CPUSS_MEM_CLOCK_CTL settings, if desired

***Note**: If CPUSS_FAST_x_CLOCK_CTL.FRAC_DIV != 0, then the relevant divider for the CLK_FAST_x must be rounded up to the next higher integer. In this case, the CLK_FAST_x must be considered to be divided by (2+INT_DIV), since some clock periods may be 1 CLK_HFx cycle longer than other clock periods.*

Fix status

No silicon fix planned. Use workaround.

Impact on Infineon software

Impact: Limitation

Related modules: MCU

Comment: Users of the MCAL MCU module who turn off a powered-on CPU must implement the workaround. CPUs are powered off with McuMainCore0PowerMode ... McuMainCore3PowerMode set to MCU_POWERMODE_OFF. The memory clock divider value is configured with McuMemClockDivision.

2.14 [250]SDHC: Wrong data written to external memory if system bus error occurs on last data beat during DMA transfer

Description

In card write use cases, on occurrence of system bus error (AHB response error) it is expected that the data block is not sent to the device. However, in cases when error occurs at the last data beat of the transfer to the corresponding block, SDHC controller attempts to send this block to the device.

When the SDHC controller performs a card write operation using DMA (ADMA mode), data blocks are first fetched from system memory via the AHB master interface and buffered internally before being transmitted to the SD card or eMMC device.

If a system bus error response (AHB error) occurs exactly on the last data beat of the programmed transfer block, the controller may already have prefetched the corresponding block into its internal buffer and can start transmitting that block to the device. In this situation the controller simultaneously reports the transfer failure to software.

As a result, the SD card or eMMC device may receive a corrupted data block even though the controller signals an error condition.

Parameters affected

SDHC data integrity during write operations

Trigger condition(s)

The behavior can be reproduced when all of the following conditions are met:

- SDHC performs a write transfer to SD card or eMMC device using ADMA mode
- The system memory interface returns an AHB error response for the final data beat of the block transfer (for example byte 509-512 of a 512-byte block)
- The error is reported through SDHC0_CORE_ADMA_ERR_STAT_R and the transfer eventually terminates with an error interrupt indicated in SDHC0_CORE_NORMAL_INT_STAT_R / SDHC0_CORE_ERROR_INT_STAT_R

Software can detect the condition by observing that SDHC0_CORE_ADMA_ERR_STAT_R indicates a DMA error while the card has already accepted a write command for the affected block.

Scope of impact

Incorrect data may be written to the SD card or eMMC device even though the transfer ends with an error status reported by the controller.

Workaround

Implement the SD error recovery procedure when an ADMA error is detected:

- Monitor SDHC0_CORE_ADMA_ERR_STAT_R and SDHC0_CORE_ERROR_INT_STAT_R for DMA related errors
- If an ADMA error occurs during a write transfer, abort the transfer according to the SDHC error recovery sequence
- Retry the failed write command and associated data block

Executing the recovery sequence immediately after the error interrupt significantly reduces the possibility that the corrupted buffered block is transmitted to the device.

Fix status

No silicon fix planned. Use workaround.

Impact on Infineon software

Impact: No

Related modules: None

Comment: Software in scope does not support the SDHC

2.15 [251]SDHC: Timeout error when BOOT ACK driven on all data lines in eMMC mode

Description

In eMMC mode during Boot operation, when the device responds with BOOT ACK in all the data lines for 4/8 bit data widths, timeout/CRC error is reported by the controller because it erroneously detects the start bit of BOOT ACK as start bit of the BOOT Data.

Following consequences are possible:

- Unexpected event requiring software interrupt
- System benignly self-recovers
- Persistent data corruption/loss

Parameters affected

N/A

Trigger condition(s)

The issue can be happen under the following conditions:

- SDHC configured for eMMC mode
- eMMC Boot operation is initiated with BOOT ACK enabled:
  SDHC0_CORE_BOOT_CTRL_R.BOOT_ACK_ENABLE=1
- Bus width configured for 4-bit or 8-bit mode
  - SDHC0_CORE_HOST_CTRL1_R.DAT_XFER_WIDTH=1 or
    SDHC0_CORE_HOST_CTRL1_R.EXT_DAT_XFER=1
- The eMMC device drives BOOT ACK simultaneously on all active data lines (DAT[3:0] or DAT[7:0])

Scope of impact

eMMC Boot procedure is affected when BOOT ACK is used.

Normal command/data transfers in SD, SDIO, or eMMC modes outside the boot acknowledgement phase are not affected.

Workaround

Any of the following:

- Drive BOOT ACK on D0 only
- Disable the BOOT ACK feature when using eMMC Boot operation

Fix status

No silicon fix planned. Use workaround.

Impact on Infineon software

Impact: No

Related modules: None

Comment: Software in scope does not support the SDHC

2.16 [252]SDHC: AHB bus issue caused by insertion of wait cycles in a previous transfer

Description

SDHC AHB bus may hang or data might be corrupted when the SMIF AHB slave or Ethernet AHB slave is accessed while a burst read or write transfer to SHDC AHB bus in ongoing.

This issue only occurs in the PIO/slave mode where a continuous stream of data is accessed through the AHB interface.

Parameters affected

N/A

Trigger condition(s)

Continues stream of data accessed via AHB and AHB slaves (burst access) in same MMIO area (SMIF or Ethernet) inserts wait states in the AHB transfer.

***Note**: SDHC DMA modes are not affected.*

Scope of impact

- Wrong data read or written from/to SDHC
- AHB bus for SDHC, Ethernet, SMIF may hang

Workaround

SMIF and Ethernet must not be accessed while AHB read or write burst transfers to AHB slave interface of SDHC.

Fix status

No silicon fix planned. Use workaround.

Impact on Infineon software

Impact: No
Related modules: None
Comment: Software in scope does not support the SDHC, SMIF, and Ethernet.

2.17 [253]SDHC: ADMA3 cannot be used

Description

The ADMA3 has several functional limitation that make it unusable.

Parameters affected

N/A

Trigger condition(s)

Use of ADMA3

Scope of impact

ADMA3 cannot be used.

Workaround

Use SDMA and/or ADMA2.

Fix status

No silicon fix planned. Use workaround.

Impact on Infineon software

Impact: No
Related modules: None
Comment: Software in scope does not support the SDHC

2.18 [254]SDHC: HW access flag for some registers is incorrect in Register TRM

Description

The HW access flag for following register is set to “R” but should be “RW”.

- BOOT_CTRL bit [0]
- XFER_MODE_R bits [7:0]
- PWR_CTRL_R bit [0]

Parameters affected

Register TRM bit description of the registers

Trigger condition(s)

Using affected bits

Scope of impact

Register TRM does not describe the actual behavior of the bits.

Workaround

None

Fix status

No silicon fix planned. Register TRM will be updated.

Impact on Infineon software

Impact: No
Related modules: None
Comment: Software in scope does not support the SDHC

2.19 [255]SDHC: Nst Timing of CMD12 STOP_TRANSMISSION command of SDHC is violated

Description

According to the JEDEC specification, Nst timing should be two cycles (one data cycle and end bit cycle) after the end bit of stop transmission command (CMD12). However, the host controller stops the data traffic one cycle earlier than the protocol-mandated value of two cycles, due to which the end bit is missed.

Parameters affected

N/A

Trigger condition(s)

This issue is seen when CMD12 is issued by the controller to stop a data transfer.

Scope of impact

Non-Compliance with JEDEC specification for Nst timing.
Single-block transfers are not affected because CMD12 is not used.

Workaround

The user should use multiple block writes with a pre-defined block count rather than open-ended multiple block writes to avoid this issue. If an open-ended multiple block write is done, the Abort command (CMD12) must be sent after the traffic is completed, when NORMAL_INT_STAT_R.XFER_COMPLETE is asserted.

Fix status

No silicon fix planned. Use workaround.

Impact on Infineon software

Impact: No

Related modules: None

Comment: Software in scope does not support the SDHC

2.20 [256]SDHC command response sampling failure when NCR equals 2 card clock cycles

Description

The SDHC controller may fail to correctly sample the response start bit of the SD or eMMC device that returns a command response with the minimum allowed NCR timing of 2 card clock cycles. NCR is defined as the number of card clock cycles between the end bit of the command and the start bit of the response as defined in the SD/eMMC protocol. If the response start bit is driven exactly 2 card clock cycles after the command end bit, the controller sampling logic can miss or misalign the start bit detection. As a consequence, the response field may be captured with an incorrect phase. This results in error flags indicating a response framing mismatch.

Detection pattern observable by software:

- SDHCx_CORE_NORMAL_INT_STAT_R.ERR_INTERRUPT = 1
- SDHCx_CORE_ERROR_INT_STAT_R.CMD_END_BIT_ERR = 1 or SDHCx_CORE_ERROR_INT_STAT_R.CMD_CRC_ERR = 1

while the card response on the CMD line is valid.

Parameter affected

N/A

Trigger condition(s)

The faulty behavior can be reproduced under the following procedure:

1. An SD or eMMC command expecting a response (for example, CMD0 to CMD63 with response type R1/R3/R6)
2. The card drives the response start bit exactly 2 SD card clock cycles after the command end bit (NCR = 2)
3. The SDHC controller samples the CMD line during response start-bit detection

Scope of impact

Command/response transactions between the SDHC host controller and attached SD or eMMC devices.

Affected functionality:

- Command response reception
- Card identification and initialization sequences
- Any command requiring card response verification

If responses are consistently generated with NCR = 2, command execution may repeatedly fail due to false command error detection.

Workaround

No workaround

Fix status

No silicon fix planned.

Impact on Infineon software

Impact: No
Related modules: None
Comment: Software in scope does not support the SDHC

2.21 [257]SDHC: Command queuing feature is not supported

Description

The SDHC command queuing (CQ) feature is listed in the datasheet and technical reference manual, but it is not supported be the implemented IP.

Parameter affected

N/A

Trigger condition(s)

Use of SDHC

Scope of impact

Command queuing feature is not available.

Workaround

None

Fix status

No silicon fix planned. Datasheet will be updated.

Impact on Infineon software

Impact: No
Related modules: None
Comment: Software in scope does not support the SDHC

2.22 [260]PLL may not be locked in certain scenarios

Description

PLL may not be locked after wake-up from DeepSleep mode with trigger conditions.

Parameters affected

N/A

Trigger condition(s)

- Body High devices
  - Wakeup from DeepSleep with any of the following conditions
    - Using the external PMIC mode
      - The following conditions are met when entering DeepSleep mode
        - PLL is enabled
        - PWR_REGHC_CTL4.REGHC_PMIC_DPSLP = 0 & PWR_REGHC_CTL2.REGHC_EN = 1 (The power supply is switched to the internal regulator during DeepSleep, and PMIC control is handled by hardware)
        - PWR_REGHC_CTL.REGHC_PMIC_STATUS_WAIT register value > 00h
    - Using the external pass transistor mode
      - The following conditions are met entering DeepSleep mode
        - PLL is enabled
        - PWR_REGHC_CTL2.REGHC_EN = 1 (Pass transistor control is handled by hardware)
        - PWR_REGHC_CTL.REGHC_PMIC_STATUS_WAIT register value > 00h
- Cluster 2D or Graphic devices
  - Wakeup from DeepSleep with below conditions
    - Using the external PMIC mode
    - The following conditions are met when entering DeepSleep mode
      - PLL is enabled
      - PWR_PMIC_CTL4.PMIC_DPSLP = 0 & PWR_PMIC_CTL2.PMIC_EN = 1 (The power supply is switched to the internal regulator during DeepSleep, and PMIC control is handled by hardware)
      - PWR_PMIC_CTL.PMIC_STATUS_WAIT register value > 00h

Scope of impact

PLL may not be locked and the device works with reference clock of the PLL.

Workaround

Any of the following will work for all trigger conditions:

1. PWR_REGHC_CTL.REGHC_PMIC_STATUS_WAIT/PWR_PMIC_CTL.PMIC_STATUS_WAIT register value to be 00h

2. Restart PLL if PLL locked bit[3] remains 0 after wakeup

The sequence for restarting PLL is as follows:

a. Disable PLL by writing PLL enable bit[4] to 0

b. Wait at least 2 IMO cycles (≥ 250 ns)

c. Enable PLL by writing PLL enable bit[4] to 1

d. Wait till PLL locked bit[3] becomes 1

Fix status

No silicon fix planned. Use workaround.

Impact on Infineon software

Impact: None

Related modules: MCU

3 PLL200: CLK_PLL_STATUSx.LOCKED, PLL400: CLK_PLL400Mx_STATUS.LOCKED

4 PLL200: CLK_PLL_CONFIGx.ENABLE, PLL400: CLK_ PLL400Mx_CONFIG.ENABLE

Comment: PLL is enabled via the McuPllEnable configuration setting. PLL lock status can be retrieved with Mcu_GetPllStatus(). Current revisions of the software in scope do not support the REGHC and PMIC configuration. Revisions up to 1.19 of the MCU module supported the configuration of REGHC_PMIC_DPSLP/ PMIC_DPSLP and REGHC_EN/PMIC_EN via the McuRegHcEnable/McuPmicEnable and McuRegHcOnDeepSleepEnable/McuPmicOnDeepSleepEnable configuration settings, but did not modify REGHC_PMIC_STATUS_WAIT/PMIC_STATUS_WAIT.

2.23 [261]Ethernet interrupt status flag description of SW/HW access in Register TRM is incorrect

Description

The SW access and HW access flags of several Ethernet interrupt status registers are incorrect in the Register TRM.

Parameters affected

N/A

Trigger condition(s)

Use of following Interrupt status register flags:

- INT_STATUS [29], [27:18], [14:10], [7:0]
- INT_Q1_STATUS [11,7,6,5,2,1]
- INT_Q2_STATUS [11,7,6,5,2,1]
- RX_LPI [15:0]
- RX_LPI_TIME [23:0]
- TX_LPI [15:0]
- TX_LPI_TIME [23:0]

Scope of impact

Register TRM does not describe the actual behavior of these bits.
Register TRM will be updated as follows:

- SW access changed from W1C to RW1C for
  - INT_STATUS [29], [27:18], [14:10], [7]
- SW access changed from R to RW1C for
  - INT_Q1_STATUS [11,7,6,5,2,1]
  - INT_Q2_STATUS [11,7,6,5,2,1]
- HW access changed from R to RW for
  - RX_LPI [15:0]
  - RX_LPI_TIME [23:0]
  - TX_LPI [15:0]
  - TX_LPI_TIME [23:0]
- The description of following register has been corrected by removing 'Cleared on read'
  - INT_STATUS [26:18], [14:10], [7:0]

Workaround

None. Follow the updated Register TRM.

Fix status

No silicon fix planned. Register TRM will be updated.

Impact on Infineon software

Impact: No

Related modules: None

Comment: Software in scope does not support the Ethernet.

2.24 [770]PLD might perform linefill to address that would generate a MemManage Fault (Arm® CM7 errata ID: 1013783)

Description

If the MPU is present and enabled, then it can be programmed so that loads to certain addresses generate a MemManage Fault.

This could be because:

- The address is unmapped, that is, it is not in an enabled region and the default memory map is not being used
- The address cannot be accessed at the current privilege level
- The address cannot be accessed at any privilege level

Because of this erratum, a PLD to such an address might incorrectly cause a data cache linefill.

Parameters affected

N/A

Trigger condition(s)

1. The data cache is enabled and the MPU is enabled
2. A PLD is executed, and either:
   a. The PLD is to an address not mapped in the MPU, which requires that:
      1. The MPU is enabled
      2. The default memory map is not being used
      3. The default memory map is cacheable at that address
      4. The PLD does not hit an enabled MPU region
   b. The PLD is to a region that has permission requirements that the PLD does not meet, which requires that:
      1. The MPU is enabled
      2. The default memory map is not being used
      3. The region that the PLD hits is cacheable
      4. The region that the PLD hits would generate a MemManage fault for a load. This requires either:
         a. The region cannot be accessed by a read at any privilege level
         b. The region only has read access for privileged code and the PLD is unprivileged

Note that in rare cases, a PLD instruction can be speculatively executed in the shadow of a mispredicted branch. This can even theoretically be a literal value that decodes to a PLD.

Scope of impact

Processor execution is not affected by this erratum. The data returned from the linefill is not directly consumed by the PLD. Any subsequent load to that address can only access the data if it has permissions to do so. This erratum does not permit software to access data that it does not have permissions for.

The only implications of this erratum are the access itself which should not have been performed. This might have an impact on memory regions with side-effects on reads or on memory which never returns a response on the bus.

Workaround

Accesses to memory that is not mapped in the MPU can be avoided by using MPU region 0 to cover all unmapped memory and make this region execute-never and inaccessible.

That is, MPU_RASR0 should be programmed with:

- MPU_RASR0.ENABLE = 1 ; MPU region 0 enable
- MPU_RASR0.SIZE = b11111 ; MPU region 0 size = 2^32 bytes to cover entire memory
- MPU_RASR0.SRD = b00000000 ; All sub-regions enabled
- MPU_RASR0.XN = 1; Execute-never to prevent instruction fetch
- MPU_RASR0.AP = b000; No read or write access for any privilege level
- MPU_RASR0.TEX = b000 ; Attributes = Strongly-ordered
- MPU_RASR0.C = b0 ; Attributes = Strongly-ordered
- MPU_RASR0.B = b0 ; Attributes = Strongly-ordered

Accesses to memory that is mapped in the MPU, but should not be accessed at the current privilege level can be avoided by making the region non-cacheable.

That is, MPU_RASR0 should be programmed with:

- MPU_RASR0.TEX = b000 ; Attributes = Strongly-ordered
- MPU_RASR0.C = b0 ; Attributes = Strongly-ordered
- MPU_RASR0.B = b0 ; Attributes = Strongly-ordered

Fix status

No silicon fix planned. Use workaround.

Impact on Infineon software

Impact: None

Related modules: N/A

Comment: This erratum would only have noticeable effects if a PLD targeted the address of an MMIO with side-effects on reading. Conditions of the erratum are not met for such addresses: they are not cacheable in the default memory map (condition 2.a.3) and any meaningful MPU configuration (condition 2.b.3).

2.25 [771]ECC error causes data corruption when the data cache error bank registers are locked (Arm® CM7 errata ID: 1267980)

Description

The data cache contains two error bank registers, DEBR0 and DEBR1. These registers store the locations in the cache that Error Correcting Code (ECC) errors affect and prevent future allocations to those locations.

Software can lock each DEBR and this prevents the DEBR from being automatically updated when a data cache ECC error is detected.

Because of this erratum, if both DEBR0 and DEBR1 are locked and an ECC error is detected on a cacheable store, then the store data is written onto the bus but not written into the data cache. This might result in the data cache containing stale data.

Parameters affected

N/A

Trigger condition(s)

- DEBR0 and DEBR1 are locked
- The wanted address has been allocated to the cache
- A cacheable store to the wanted address looks up in the cache, and an ECC error is found in the cache set that the store addresses

Scope of impact

This erratum can cause data corruption in the data cache.

Workaround

Software must avoid locking both error bank registers.

Fix status

No silicon fix planned. Use workaround.

Impact on Infineon software

Impact: Limitation

Related modules: N/A

Comment: Software in scope does not use CM7_SCS_DEBR0 and CM7_SCS_DEBR1. Other software must not lock (set bit #1 of) the CM7_SCS_DEBR0 and CM7_SCS_DEBR1 registers at the same time.

2.26 [772]Data corruption for load following Store-Exclusive (Arm® CM7 errata ID: 1315869)

Description

A load that follows a Store-Exclusive to the same address might forward data from an earlier store, situated between the Load-Exclusive and the Store-Exclusive, and not the data from the Store-Exclusive.

Parameter affected

N/A

Trigger condition(s)

The following sequence is required for this erratum to occur:

1. A load exclusive sets the local monitor
2. A store to the wanted address
3. Any of the following instructions to the wanted address. This instruction must not fail either the local or global monitor check
   a. STREXB
   b. STREXH
   c. STREX
4. A load to the wanted address

There must be at most one instruction between the Store-Exclusive and the load. All accesses must be to Shareable memory.

Scope of impact

Data corruption occurs when the load returns data from the older store instead of the newer Store- Exclusive.

Stores between a Load-Exclusive and Store-Exclusive are not expected in real code because such stores can always clear the local monitor in some implementations.

Workaround

No workaround is necessary.

Fix status

No silicon fix planned.

Impact on Infineon software

Impact: None

Related modules: N/A

Comment: Software in scope does not use exclusive load and store. Other software, if using exclusive load and store, can be affected.

2.27 [773]TCM bandwidth sharing between AHBS writes and software stores might not function correctly when using TCM wait states (Arm® CM7 errata ID: 2328489)

Description

The TCM Control Unit (TCU) contains a Store Queue (SQ) FIFO that buffers Tightly Coupled Memory (TCM) writes. Software stores and AHBS writes both go through the SQ. A round-robin scheme is used to fairly share the SQ ingress bandwidth between software stores and AHBS writes when contention occurs. Due to this erratum, AHBS writes might take priority over 64-bit software stores, which can stall processor instruction execution while the AHBS writes are ongoing. Software stores take priority over AHBS writes and therefore this erratum does not occur when there is adequate TCM bandwidth available.

Parameters affected

N/A

Trigger condition(s)

This erratum can occur when either an STRD, STM, PUSH, VPUSH, VSTR.64, or VSTM instruction is executed targeting TCM during a long stream of back-to-back AHBS write transfers and TCM wait states are used.

Also, if a load instruction closely follows after a 64-bit store instruction to TCM that stalls the execution pipeline, then this will further exacerbate the issue. If the pipeline is stalled, the read will still go ahead but the data returned will be discarded. Hence, a TCM read will be repeated until the stall ends.

Scope of impact

This erratum only affects the performance of the Cortex®-M7 processor. It can cause the processor's execution pipeline to stall when executing a 64-bit store instruction while back-to-back AHBS writes are ongoing. When the AHBS back-to- back write stream ends, the 64-bit store will be accepted into the SQ and the pipeline will stop stalling.

Workaround

Do not modify CPUSS_CM7_x_CTL.ITCM_READ_WS and CPUSS_CM7_x_CTL.DTCM_READ_WS. By default, these registers are initialized to 0.

Fix status

No silicon fix planned. Use workaround.

Impact on Infineon software

Impact: Limitation

Related modules: N/A

Comment: The user must not modify CPUSS_CM7_x_CTL.ITCM_READ_WS and CPUSS_CM7_x_CTL.DTCM_READ_WS. By default, these registers are initialized to 0, so there are no TCM wait states and, hence, the erratum will not come into effect.

2.28 [774]Cortex®-M7 can halt in an incorrect address when breakpoint and exception occurs simultaneously (Arm® CM7 errata ID: 3092511)

Description

When an asynchronous exception occurs at the same time as a breakpoint event (either hardware breakpoint or software breakpoint), it is possible for the processor to halt at the beginning of the exception handler instead of the instruction address pointed by the breakpoint.

Parameters affected

N/A

Trigger condition(s)

The BKPT bit in Debug Fault Status Register (DFSR) is set, indicating that a breakpoint event has occurred. The return address of the exception is the breakpoint address. As a result, if the debugger clears the halting control bit in the processor at this point, the processor will reach the breakpoint again after servicing the exception.

The following conditions are required:

1. Halt mode debug is enabled and is permitted by debug authentication configuration
2. The processor reaches the breakpoint as the same time that the asynchronous exception is invoked

Scope of impact

A debugger connected to the Cortex®-M7 can detect the processor is halted after a breakpoint is hit, but might not be able to determine which breakpoint has triggered the halting.

Workaround

This issue only affect the debugger's operation. The debugger could report the halting reason as an unknown breakpoint, and optionally resume operation. If the processor's operation is resumed, it is likely to be halted again immediately after the interrupt is serviced and returns to the breakpoint address.

Fix status

No silicon fix planned.

Impact on Infineon software

Impact: None

2 Functional deviations

Related modules: N/A
Comment: This erratum only affects debugging.

Revision history of CYT6BJ errata sheet

Document version	Date of release	Description of changes
0.6	2025-05-12	Initial release
0.7	2025-09-30	Consolidated the description for all affected devices of errata ID 234. Added errata ID 242 and 770 to 774.
1.0	2026-04-22	Updated the description of errata ID 218. Added errata ID 243 to 245. Consolidated the description for all affected devices of errata ID 234.
1.1	2026-06-08	Added errata ID 250 to 257.
1.2	2026-07-16	Added errata ID 260, 261.
1.3	2026-07-28	Updated the workaround of errata ID 260 to change from 250 µs to 250 ns.
1.4	2026-08-27	Updated the "Impact on Infineon software" of errata ID 244.

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