TRAVEO™ T2G CYT4BF errata sheet

Marking/Step: Rev. D

32-bit single-chip microcontroller

About this document

Scope and purpose

This document describes the deviations of the device from the current user documentation, to support the assessment of the effects of these deviations on your custom hardware and software implementations.

Please take note of the following information:

- This errata sheet applies to all temperature and frequency versions and to all memory size variants, unless explicitly noted otherwise. For a derivative synopsis, see the latest datasheet or user manual
- Multiple device variants are covered in this one document. If an issue is related to a particular module, and this module is not specified for a specific device variant, then the issue does not apply to that device variant
- Devices marked with ES are engineering samples which may not be completely tested in all functional and electrical characteristics and are therefore only suitable for evaluation
- Some of the errata have workarounds which may be supported by the tool vendors. Some corresponding compiler switches may need to be set. Please refer to the respective documentation of your compiler
- To understand the effect of issues relating to the on-chip debug system, please refer to the respective debug tool vendor documentation

Current documentation

- TRAVEO™ T2G automotive MCU body controller high architecture technical reference manual
- TRAVEO™ T2G automotive MCU body controller high registers technical reference manual for CYT4BF
- CYT4BF datasheet TRAVEO™ T2G automotive MCU

Newer versions replace older versions, unless specifically stated otherwise.

Please always refer to the corresponding documentation for this device available in the category 'Documents' at www.infineon.com/TRAVEO™ and www.myInfineon.com.

Conventions used in this document

Each erratum identifier follows the pattern [Number]:

- [Number] = ascending sequential number within the three

  ***Note**:* *[Number] As this sequence is used over several derivatives, including already solved deviations, gaps can occur inside this numbering sequence*

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1 Errata overview

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2 Functional deviations

2.1 [096] CAN FD RX FIFO top pointer feature does not function as expected

Description

RX FIFO top pointer function calculates the address for received messages in Message RAM by hardware. This address should be re-start back from the start address after reading all messages of RX FIFO n size (n: 0 or 1). However, the address does not re-start back from the start address when RX FIFO n size is set to 1 (CANFD_CH_RXFnC.FnS = 0x01). This results in CPU/DMA to read messages from the wrong address in Message RAM.

Parameters affected

N/A

Trigger condition(s)

RX FIFO top pointer function is used when RX FIFO n size set to 1 element (CANFD_CH_RXFnC.FnS = 0x01).

Scope of impact

Received message cannot be correctly read by using RX FIFO top pointer function, when RX FIFO n size set to 1 element.

Workaround

Any of the following

1. Set RX FIFO n size to 2 or more when using RX FIFO top pointer function.
2. Do not use RX FIFO top pointer function when RX FIFO n size set to 1 element. Instead of RX FIFO top pointer, read received messages from the Message RAM directly.

Fix status

No silicon fix planned. Use workaround.

2.2 [097] CAN FD debug message handling state machine not get reset to Idle state when CANFD_CH_CCCR.INIT is set

Description

If either CANFD_CH_CCCR.INIT bit is set by the Host or when the M_TTCAN module enters BusOff state, the debug message handling state machine stays in its current state instead of being reset to Idle state. Configuring the bit CANFD_CH_CCCR.CCE does not change CANFD_CH_RXF1S.DMS.

Parameters affected

N/A

Trigger condition(s)

Either CANFD_CH_CCCR.INIT bit is set by the Host or when the M_TTCAN module enters BusOff state.

Scope of impact

The errata is limited to the use case when the Debug on CAN functionality is active. Normal operation of CAN module is not affected, in which case the debug message handling state machine always remains in Idle state. In the described use case, the debug message handling state machine is stopped and remains in the current state signaled by the bit CANFD_CH_RXF1S.DMS. In case CANFD_CH_RXF1S.DMS is set to 0b11, DMA request remains active. Bosch classifies this as non-critical error with low severity, there is no fix for the IP, Bosch recommends the workaround listed also here.

Workaround

In case the debug message handling state machine has stopped while CANFD_CH_RXF1S.DMS is 0b01 or 0b10, it can be reset to Idle state by hardware reset or by reception of debug messages after CANFD_CH_CCCR.INIT is reset to zero.

Fix status

No silicon fix planned. Use workaround.

2.3 [124]Limitation of the memory hole in SCB register space

Description

The memory hole [offset address: 0x1000 to 0xFFFF] inside SCB register space is not aligned to the below defined spec. The offset address bits [15:12] are ignored and treated as 4'b0000, so write/read access to offset address [0x1000 to 0xFFFF], will actually happen to [0x0000 to 0x0FFF].

- Access to address gaps in mapped memory space: writes are ignored and any read returns a zero.

Parameters affected

N/A

Trigger condition(s)

Access to the memory hole [offset address: 0x1000 to 0xFFFF] in SCB register space.

Scope of impact

The memory hole [offset address: 0x1000 to 0xFFFF] in SCB register space is not aligned to other IP registers.

Workaround

Do not access to the memory hole [offset address: 0x1000 to 0xFFFF] in SCB register space.

Fix status

No silicon fix planned. Use workaround.

2.4 [128]Limitation of the memory hole in Ethernet (ETH) register space

Description

The memory hole [offset address: 0x2000 to 0xFFFF] in ETH register space has the below mentioned original spec. However, when accessing to address gaps within [0x1000 to 0x1FFF], the offset address bits [15:13] are ignored and treated as 3'b000, so write/read access to offset address [0x3000 to 0x3FFF, 0x5000 to 0x5FFF, 0x7000 to 0x7FFF, 0x9000 to 0x9FFF, 0xB000 to 0xBFFF, 0xD000 to 0xDFFF, 0xF000 to 0xFFFF], will actually happen to [0x1000 to 0x1FFF].

- Access to address gaps within [0x0000 to 0x0FFF]: writes are ignored and any read returns a zero
- Access to address gaps within [0x1000 to 0x1FFF]: returns AHB ERROR

Parameters affected

N/A

Trigger condition(s)

Access to the memory hole [offset address: 0x3000 to 0x3FFF, 0x5000 to 0x5FFF, 0x7000 to 0x7FFF, 0x9000 to 0x9FFF, 0xB000 to 0xBFFF, 0xD000 to 0xDFFF, 0xF000 to 0xFFFF] in ETH register space.

Scope of impact

Write/read access to offset address [0x3000 to 0x3FFF, 0x5000 to 0x5FFF, 0x7000 to 0x7FFF, 0x9000 to 0x9FFF, 0xB000 to 0xBFFF, 0xD000 to 0xDFFF, 0xF000 to 0xFFFF], will actually happen to [0x1000 to 0x1FFF].

Workaround

Do not access to the memory hole [offset address: 0x3000 to 0x3FFF, 0x5000 to 0x5FFF, 0x7000 to 0x7FFF, 0x9000 to 0x9FFF, 0xB000 to 0xBFFF, 0xD000 to 0xDFFF, 0xF000 to 0xFFFF] in ETH register space.

Fix status

No silicon fix planned. Use workaround.

2.5 [133]RMA failure

Description

TransitionToRMA always fails due to hard fault resulting from access to protected memory (User SRAM except first 2 KB of SRAM0).

Parameter affected

N/A

Trigger condition(s)

When using TransitionToRMA

Scope of impact

TransitionToRMA always fails.

Workaround

None

Fix status

No silicon fix planned. Read and Write Access for PC1 shall be provided for the additional 2 KB of SRAM0 starting from SRAM0 + 2 KB. TRM was updated with this information.

2.6 [137]Limitation of work flash reading

Description

1. Work flash can be read via different CPU cores but only one CPU core is assigned for non-correctable ECC error handling
2. Reading 32 bits of work flash on AXI bus can result in ECC error (Only for CM7 core devices)

Parameter affected

N/A

Trigger condition(s)

1. Reading work flash via CPU core and ECC fault interrupt routed to two or more CPU cores
2. Reading 32 bits of work flash via CM7_0/1 or other AXI master and adjacent 32 bits of work flash is not initialized (Only for CM7 core devices)

Scope of impact

1. Only one CPU core can be assigned for non-correctable ECC error handling
2. Work flash should be accessed via AHB or AXI with 64-bit boundary (Only for CM7 core devices)

Workaround

Any of the following:

- Option A (Recommended solution)
  - Problem 1 and problem 2: Set each CPU core to use a separate AHB DMA (M-DMA or P-DMA) channel to read work flash. If non-correctable ECC error occurs, the DMA transaction get aborted and respective CPU core gets the interrupt to manage the non-correctable ECC error
- Option B
  - Problem 1[1]: Set non-correctable ECC error handling to reset. This way no one CPU core needs to manage the non-correctable ECC error handling
  - Problem 2: Limit work flash data size to 64 bits. Program work flash in units of aligned 64-bit double words and read it as 64-bit double words thru CM7_0/1 or another AXI master (Only for CM7 core devices)
- Option C
  - Problem 1[2]: Assign one CPU core for non-correctable ECC error handling and that core informs the error to the other core which caused the error, but it takes time
  - Problem 2: Use Option B

Fix status

No silicon fix planned. Use workaround. Infineon FLS and FEE driver were updated with workaround A. TRM was updated for this limitation.

2.7 [138]ROM boot code clears to zero last 2 KB of SRAM

Description

For TRAVEO™ T2G Body Entry devices, ROM boot code clears to zero last 2 KB of SRAM. This region is available to the user after boot. However, data retention across resets is not guaranteed in this area.

1 Not recommended to use for EEPROM emulation. EEPROM emulation needs to cope with aborted write/erase. In such a scenario, option B leads to deadlock in endless resets. However, option B can be used if work flash update is not intended in the field.
2 Not recommended to use with MCAL, since the inter-core communication is too slow.

For TRAVEO™ T2G Body High devices, ROM boot code clears to zero first word of last 2 KB of SRAM. This region is available to the user after boot. However, data retention across resets is not guaranteed in this area.

Paramater affected

N/A

Trigger condition(s)

After ROM boot

Scope of impact

For TRAVEO™ T2G Body Entry devices, data retention across resets is not guaranteed in last 2 KB of SRAM.
For TRAVEO™ T2G Body High devices, data retention across resets is not guaranteed in first word of last 2 KB of SRAM.

Workaround

For TRAVEO™ T2G Body Entry devices, do not use last 2 KB of SRAM for data retention.
For TRAVEO™ T2G Body High devices, do not use first word of last 2 KB of SRAM for data retention.

Scope

No silicon fix planned. Use workaround. TRM was updated for this limitation.

2.8 [139]Limitation of programming SFlash Normal Access Restrictions (row 13)

Description

CM0+ cache is not disabled when programming SFlash Normal Access Restrictions (row 13) by WriteRow SROM API. Occasionally, writing to SFlash Normal Access Restrictions (row 13) may return error status “0xF00000A4” (ProgramRow is invoked on unerased cells or blank check fails).

Parameter affected

N/A

Trigger condition(s)

WriteRow SROM API is called on Normal Access Restrictions (row 13)

Scope of impact

Error status – 0xF00000A4 “ProgramRow is invoked on unerased cells or blank check fails” is returned

Workaround

Disable CM0+ cache before call to WriteRow (to SFlash row 13) and enabling the cache back after the SROM API execution. Following sequence could be a recommended sequence:

1. FLASHC_CM0_CA_CTL0.CA_EN = 0; // Disable the CM0+ cache
2. Trigger WriteRow SROM API on NAR (row 13)
3. WriteRow successful
4. FLASHC_CM0_CA_CTL0.CA_EN = 1; // Enable the CM0+ cache

Fix status

No silicon fix planned. Use workaround. TRM was updated for this limitation.

2.9 [147]CAN FD controller message order inversion when transmitting from dedicated Tx Buffers configured with same Message ID

Description

Configuration:

Several Tx Buffers are configured with same Message ID. Transmission of these Tx Buffers is requested sequentially with a delay between the individual Tx requests.

Expected behavior:

When multiple Tx Buffers that are configured with the same Message ID have pending Tx requests, they shall be transmitted in ascending order of their Tx Buffer numbers. The Tx Buffer with lowest buffer number and pending Tx request is transmitted first.

Observed behavior:

It may happen, depending on the delay between the individual Tx requests, that in the case where multiple Tx Buffers are configured with the same Message ID the Tx Buffers are not transmitted in order of the Tx Buffer number (lowest number first).

Parameters affected

N/A

Trigger condition(s)

When multiple Tx Buffers that are configured with the same Message ID have pending Tx requests.

Scope of impact

In the case described it may happen, that Tx Buffers configured with the same Message ID and pending Tx request are not transmitted with lowest Tx Buffer number first (message order inversion).

Workaround

Any of the following:.

1. First write the group of Tx message with the same Message ID to the Message RAM and then afterwards request transmission of all these messages concurrently by a single write access to CANFDx_CHy_TXBAR. Before requesting a group of Tx messages with this Message ID ensure that no message with this Message ID has a pending Tx request.
2. Use the Tx FIFO instead of dedicated Tx Buffers for the transmission of several messages with the same Message ID in a specific order.

Applications not able to use workaround #1 or #2 can implement a counter within the data section of their messages sent with same ID in order to allow the recipients to determine the correct sending sequence.

Fix status

No silicon fix planned. Use workaround.

2.10 [167]CAN FD incomplete description of Dedicated Tx Buffers and Tx Queue related to transmission from multiple buffers configured with the same Message ID

Description

The following is the updated description in Section 3.5.2 Dedicated Tx Buffers and 3.5.4 Tx Queue of the Architecture TRM related to transmission from multiple buffers configured with the same Message ID.

3.5.2 Dedicated Tx Buffers

- Wording TRM: If multiple Tx Buffers are configured with the same Message ID, the Tx Buffer with the lowest buffer number is transmitted first.
- Enhancement: These Tx buffers shall be requested in ascending order with lowest buffer number first. Alternatively all Tx buffers configured with the same Message ID can be requested simultaneously by a single write access to CANFDx_CHy_TXBAR.

3.5.4 Tx Queue

- Wording TRM: If multiple queue buffers are configured with the same Message ID, the queue buffer with the lowest buffer number is transmitted first.
- Replacement: In case that multiple Tx Queue buffers are configured with the same Message ID, the transmission order depends on numbers of the buffers where the messages were stored for transmission. As these buffer numbers depend on the then current states of the PUT Index, a prediction of the transmission order is not possible.
- Wording TRM: An Add Request cyclically increments the Put Index to the next free Tx Buffer.
- Replacement: The PUT Index always points to that free buffer of the Tx Queue with the lowest number.

Parameters affected

N/A

Trigger condition(s)

Using multiple dedicated Tx Buffers or Tx Queue Buffers configured with the same Message ID

Scope of impact

In the case the dedicated Tx Buffers with the same Message ID are not requested in ascending order or at the same time or in case of multiple Tx Queue Buffers with the same Message ID, it cannot be guaranteed, that these messages are transmitted in ascending order with lowest buffer number first.

Workaround

In case a defined order of transmission is required the Tx FIFO shall be used for transmission of messages with the same Message ID. Alternatively dedicated Tx Buffers with the same Message ID shall be requested in ascending order with lowest buffer number first or by a single write access to CANFDx_CHy_TXBAR. Alternatively a single Tx Buffer can be used to transmit those messages one after the other.

Fix status

No silicon fix planned. Use workaround.

The architecture technical reference manuals were updated:

- 002-19314 Rev. *H for body controller entry family
- 002-24401 Rev. *F for body controller high family
- 002-33175 Rev. *A for cluster entry family
- 002-25800 Rev. *D for cluster 2D family

2.11 [175]Misleading status is returned for Flash and eFuse system calls if there are pending NC ECC faults in SRAM controller #0

Description

Flash and eFuse system calls will return misleading status of 0xf0000005 (“Page is write protected”) even for non-protected row or 0xf0000002 (“Invalid eFuse address”) for valid eFuse address in case of pending NC ECC faults in SRAM controller #0.

Parameters affected

Return status of Flash and eFuse system calls

Trigger condition(s)

NC ECC fault(s) pending in SRAM controller #0 and SWPUs are populated in the design.

Scope of impact

Flash and eFuse system calls will not work until the NC ECC fault(s) pending in SRAM controller #0 is properly handled.

Workaround

If the NC ECC fault(s) are not due to hardware malfunction (i.e. if the faults are due to usage of non-initialized SRAM or improper SRAM initialization), then clearing of these pending faults will resolve the issue.

Fix status

No silicon fix planned.
The architecture technical reference manuals were updated:

- 002-19314 Rev. *I for body controller entry family
- 002-24401 Rev. *G for body controller high family
- 002-33175 Rev. *A for cluster entry family
- 002-25800 Rev. *D for cluster 2D family

2.12 [176]WDT reset causes loss of SRAM retention

Description

Architecture TRM Table 19-1 shows WDT reset can retain SRAM if there is an orderly shutdown of the SRAM only during a warning interrupt. However, this is wrong. WDT reset causes loss of SRAM retention.

Parameters affected

N/A

Trigger condition(s)

WDT reset

Scope of impact

WDT reset causes loss of SRAM retention.

Workaround

None

Fix status

No silicon fix planned.
The architecture technical reference manuals were updated:

- 002-19314 Rev. *I for body controller entry family
- 002-24401 Rev. *G for body controller high family
- 002-33175 Rev. *A for cluster entry family
- 002-25800 Rev. *D for cluster 2D family

2.13 [177]RMII TX output maximum delay spec change for GPIO_STD

Description

RMII TX output maximum delay specification has been changed from 14 ns to 14.6 ns for GPIO_STD. The CYT4BF (272/320-BGA) HSIO_STD spec of 14ns is unchanged.

Parameters affected

SID393

Trigger condition(s)

Using GPIO_STD as RMII

Scope of impact

This spec change will cause that the PCB delay budget between MCU and PHY cut down to 1.4 ns from 2 ns.
[PCB delay budget = REF_CLK period (e.g. 20 ns) – SID393 (14.6 ns) – PHY RXD setup (e.g. 4 ns)]

Workaround

None

Fix status

No silicon fix planned. Datasheet was updated.

2.14 [185]Crypto ECC errors may be set after boot with application authentication

Description

Due to the improper initialization of the Crypto memory buffer, Crypto ECC errors may be set after boot with application authentication. In spite of the Crypto ECC errors, the result of the authentication is reliable.

Parameters affected

N/A

Trigger condition(s)

Boot device with application authentication

Scope of impact

Crypto ECC errors may be set after boot with application authentication.

Workaround

Clear or ignore Crypto ECC errors which generated during boot with application authentication.

Fix status

No silicon fix planned.
The architecture technical reference manuals were updated:

- 002-19314 Rev. *I for body controller entry family
- 002-24401 Rev. *G for body controller high family
- 002-33175 Rev. *A for cluster entry family
- 002-25800 Rev. *E for cluster 2D family

2.15 [198]Incomplete erase of Code Flash cells could happen Erase Suspend / Erase Resume is used along with Erase Sector operation in Non-Blocking mode

Description

Code Flash memory can be erased in “Non-Blocking” mode; a Non-Blocking mode supported option allow users to suspend an ongoing erase sector operation. When an ongoing erase operation is interrupted using “Erase Suspend” and “Erase Resume”, Flash cells may not have been erased completely, even after the erase operation complete is indicated by FLASHC_STATUS register. Only Code Flash is impacted by this issue, Work Flash and Supervisory Flash (SFlash) are not impacted.

Parameters affected

N/A

Trigger condition(s)

Using EraseSector System Call in Non-Blocking mode for CM0+ to erase Code Flash and the ongoing erase operation is interrupted using EraseSuspend and EraseResume System calls.

Scope of impact

When Code Flash sectors are erased in Non-Blocking mode and the ongoing erase operation is interrupted by Erase Suspend / Erase Resume, it cannot be guaranteed that the Code Flash cells are fully erased. Any read on the Code Flash area after the erase is complete or read on the programmed data after ProgramRow is complete can trigger ECC errors.

Workaround

Any of the following

1. User can use Non-Blocking mode for EraseSector, but users must not interrupt the erase operation using Erase Suspend / Erase Resume.
2. If a Code Flash sector erase operation is interrupted using Erase Suspend / Erase Resume, then erase the same sector again without Erase Suspend / Erase Resume before reading the sector or programming the sector.

Fix status

Fixed to update the Flash settings from the following date code

- CYT2B6/7/9: 304xxxxx
- CYT2BL: 312xxxxx

- CYT3BB/4BB: 240xxxxx
- CYT4BF: 312xxxxx
- CYT2CL: 312xxxxx
- CYT3DL: 312xxxxx
- CYT4DN: 312xxxxx

2.16 [199]Limitation for keeping the port state from peripheral IP after wakeup from DeepSleep

Description

The port state is not retained when the port selects peripheral IP (except for LIN or CAN FD) and MCU wakes up from DeepSleep.

Parameters affected

N/A

Trigger condition(s)

The port selects peripheral IP (except for LIN or CAN FD) and MCU wakes up from DeepSleep.

Scope of impact

Unexpected port output change might affect user system.

Workaround

If the port selects peripherals IP (except for LIN or CAN FD) and the port output value need to keep after wakeup from DeepSleep, set HSIOM_PRTx_PORT_SEL.IOy_SEL = 0 (GPIO) before DeepSleep and set the required output value in GPIO configuration registers. After wakeup, change HSIOM_PRTx_PORT_SEL.IOy_SEL back to the peripheral IP.

Fix status

No silicon fix planned.
The architecture technical reference manuals were updated:

- 002-19314 Rev. *I for body controller entry family
- 002-24401 Rev. *G for body controller high family
- 002-33175 Rev. *B for cluster entry family
- 002-25800 Rev. *E for cluster 2D family

2.17 [201]A part of the PWR_CTL2.BGREF_LPMODE description is lacked in the existing register TRM

Description

The following is lacked from the PWR_CTL2.BGREF_LPMODE description in the existing register TRM.
“This register will not set unless CLK_ILO0_CONFIG.ILO0_ENABLE==1. When changing back to continuous operation, keep ILO0 enabled for at least 5 ILO0 cycles after clearing this bit to allow for internal synchronization.”

Parameters affected

N/A

Trigger condition(s)

Using the PWR_CTL2.BGREF_LPMODE

Scope of impact

PWR_CTL2.BGREF_LPMODE may not be set or cleared.

Workaround

Use the PWR_CTL2.BGREF_LPMODE according to the following description.

“This register will not set unless CLK_ILO0_CONFIG.ILO0_ENABLE==1. When changing back to continuous operation, keep ILO0 enabled for at least 5 ILO0 cycles after clearing this bit to allow for internal synchronization.”

Fix status

No silicon fix planned. Register TRM was updated.

2.18 [202]Limitation of clock configuration before entering DeepSleep mode

Description

DeepSleep should not be entered while any FLL/PLL is enabled and using ECO as its reference clock. Since the unstable ECO clock after wakeup is outside the allowed reference clock limits for FLL/PLL, there is possibility of failing the DeepSleep wakeup.

Parameters affected

N/A

Trigger condition(s)

DeepSleep transition while any FLL/PLL is enabled and using ECO as its reference clock.

Scope of impact

There is possibility of failing the DeepSleep wakeup.

Workaround

If any FLL/PLL is operating with the ECO as its reference clock, change the clock to either ECO direct or IMO direct or IMO with FLL/PLL before entering DeepSleep.

Fix status

No silicon fix planned.

The architecture technical reference manuals were updated:

- 002-19314 Rev. *I for body controller entry family
- 002-24401 Rev. *G for body controller high family
- 002-33175 Rev. *B for cluster entry family
- 002-25800 Rev. *E for cluster 2D family

2.19 [203]Several data retention information in Register TRM are incorrect

Description

The following registers are described as 'Retained' in the Register TRM while it is not guaranteed that the value before entering DeepSleep mode is still readable from the register.

- SARADC: PASSx_SARy_CHz_RESULT
- SRSS: PWR_LVD_STATUS
- SRSS: PWR_LVD_STATUS2
- SRSS: CLK_CAL_CNT1
- SRSS: CLK_CAL_CNT2
- SRSS: CLK_FLL_STATUS
- SRSS: WDT_INTR
- SRSS: WDT_INTR_MASKED
- SRSS: CLK_PLL400Mx_STATUS (not for CYT2B6/7/9/L)
- MIXER: MIXER_DST_STRUCT_INTR_DST_MASKED (only for cluster devices)

Parameters affected

N/A

Trigger condition(s)

Use of the related function and wakeup from DeepSleep mode.

Scope of impact

The values before entering DeepSleep are not retained.

Workaround

For PASSx_SARy_CHz_RESULT, any of the following:

1. Store the conversion values at another memory location before entering DeepSleep mode
2. Restart the conversion after wakeup from DeepSleep mode

For the other registers:

- Rewrite the register value or read the status flags again after wakeup

Fix status

No silicon fix planned. Register TRM was updated.

2.20 [204]SCBx_INTR_TX.UNDERFLOW bit may be set unintentionally

Description

There is possibility of setting the SCBx_INTR_TX.UNDERFLOW bit even if the FIFO is not empty.

Parameters affected

N/A

Trigger condition(s)

Using the TX FIFO for SCB when the AHB-Lite interface clock (CLK_GR6) frequency of the AHB bus is greater than 3x the SCB functionality clock (PCLK_SCBx_CLOCK).

Scope of impact

SCBx_INTR_TX.UNDERFLOW bit may be set unintentionally.

Workaround

Ignore the SCBx_INTR_TX.UNDERFLOW bit if the FIFO is not empty.

Fix status

No silicon fix planned. Register TRM was updated.

2.21 [206] Hardfault may occur when the SROM APIs listed below while executing EraseSector or ProgramRow in non-blocking mode

Description

The following SROM APIs read data from bank#0 (or bank#1 if dual bank mode with mapping B is used) in SFlash. While doing that the check for active non-blocking erase or program of bank#0 (or bank#1 if dual bank mode with mapping B is used) is not performed. Therefore, reading bank#0 (or bank#1 if dual bank mode with mapping B is used) while there is an active erase/program operation triggers a bus error. This results in a hardfault occurrence based on FLASHC_FLASH_CTL register settings.

Affected SROM APIs:

- ReadSWPU
- WriteSWPU
- GenerateHash
- Checksum[3)]
- ComputeBasicHash[3)]
- CheckFactoryHash
- ProgramWorkFlash[4)]
- SwitchOverRegulators (not for CYT2B6/7/9/L, CYT2CL)
- LoadRegulatorsTrims (not for CYT2B6/7/9/L, CYT2CL)

Parameters affected

N/A

Trigger condition(s)

Calling the affected SROM APIs while executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used).

Scope of Impact

The affected SROM APIs cannot be used while executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used).

3 Do not call it to calculate on the bank where programming/erasing is in progress
4 Do not use it during non-blocking operation

Workaround

Do not use the affected SROM APIs while executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used).

Fix status

No silicon fix planned.

The architecture technical reference manuals were updated:

- 002-19314 Rev. *J for body controller entry family
- 002-24401 Rev. *H for body controller high family
- 002-33175 Rev. *D for cluster entry family
- 002-25800 Rev. *F for cluster 2D family

Impact on Infineon software

Impact: Limitation

Related modules: S-LLD, HSM-Perf-Lib

Comment: While executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used), users must not do anything of following:

1. Call CySldProt_GetSwpuFlashStructCfg
2. Call CySldProt_VerifySecureDomainFlashWriteProtection if CySldProt_SwpuFlashStructGroupConfigurations is non-empty

2.22 [209] CAN FD sporadic data corruption (payload) in case acceptance filtering is not finished before reception of data R3 (DB7..DB4) is completed

Description

During frame reception the Rx Handler accesses the external Message RAM for acceptance filtering (read accesses) and for storing of the accepted messages (write accesses).

The time needed for acceptance filtering and for storing of a received message depends on

- the Host clock frequency
- the worst-case latency of the read and write accesses to the external Message RAM
- the number of configured filter elements
- the workload of the transmit message (Tx) handler in parallel to the receive message (Rx) handler

Received data bytes (DB0..DBm) from the CAN Core are buffered in the cache of the Rx Handler before they are written to the Message RAM (in words of 4 byte). Data words inside the Message RAM are numbered from R2 to Rn (n ≤ 17).

2 Functional deviations

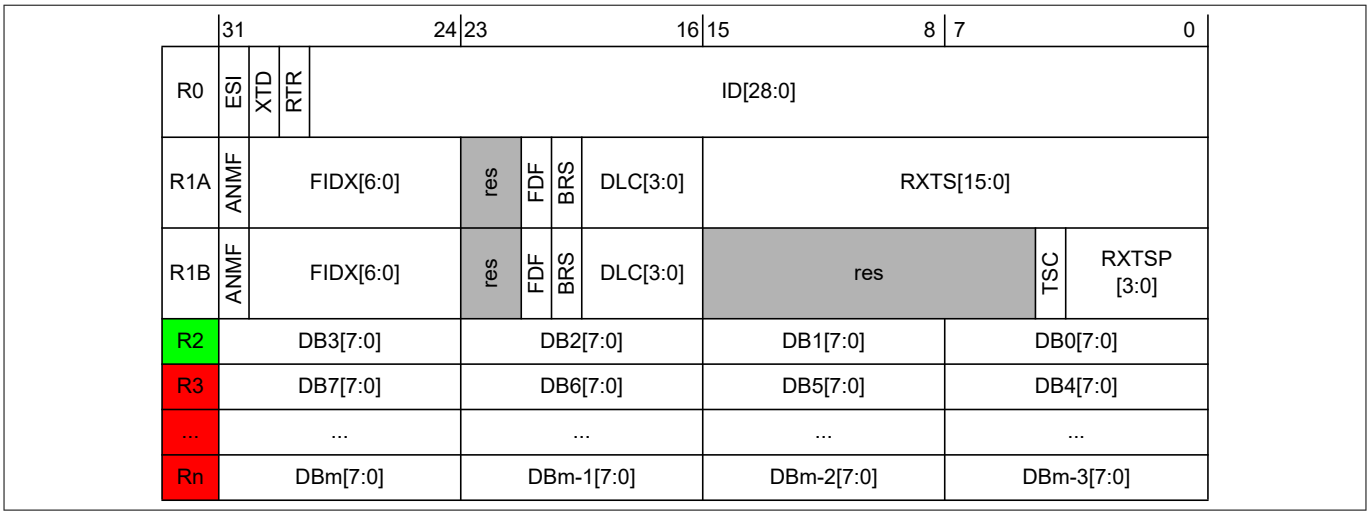


Figure 1 Rx Buffer and FIFO Element

Under the following conditions a received message will have corrupted data while the received message is signaled as valid to the host.

1. The data length code (DLC) of the received Message is greater than 4 (DLC > 4)
2. The storage of Ri of a received message into the Message RAM (after acceptance filtering is done) has not completed before R(i+1) is transferred from the CAN Core into the cache of the Rx Handler (where 2 ≤ i ≤ 5)
3. While condition 1 and 2 apply, a concurrent read of data word Ri from the cache and write of data word R(i+1) into the cache of the Rx handler happens

The data will be corrupted in a way, that in the Message RAM R(i+1) has the same content as Ri.

Despite the corrupted data, the M_TTCAN signals the storage of a valid frame in the Message RAM:

- Rx FIFO: FIFO put index RXFnS.FnPI is updated
- Dedicated Rx Buffer: New Data flag NDATn.NDxx is set
- Interrupt flag IR.MRAF is not set

The issue may occur in FD Frame Format as well as in Classic Frame Format.

Figure 2 shows how the available time for acceptance filtering and storage is reduced.

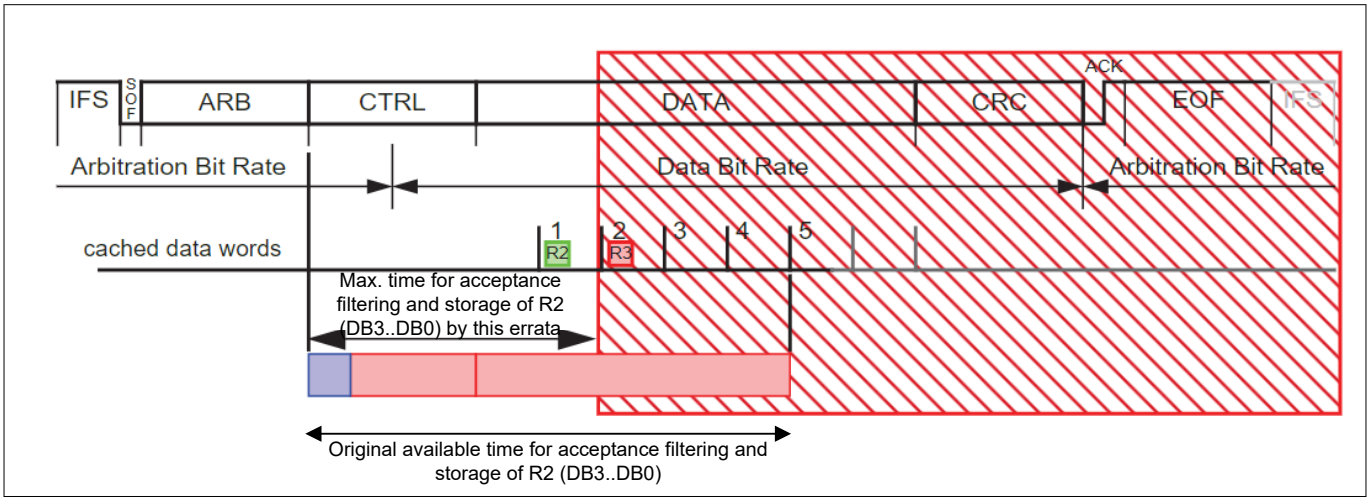


Figure 2 CAN frame with DLC > 4

Table 2 TRAVEO™ T2G: Minimum host clock frequency for CAN FD when DLC = 5

Number of configured active filter element 11-bit IDs/29-bit IDs[1) 2)]	Number of active CAN channels in an instance[3)]	Arbitration bit rate = 0.5 Mbps				Arbitration bit rate = 1 Mbps			
		Data bit rate = 0.5 Mbps	Data bit rate = 1 Mbps	Data bit rate = 2 Mbps	Data bit rate = 4 Mbps	Data bit rate = 1 Mbps	Data bit rate = 2 Mbps	Data bit rate = 4 Mbps	Data bit rate = 5 Mbps
32/16	2	3.9 MHz	7.1 MHz	13.1 MHz	22.8 MHz	7.7 MHz	14.1 MHz	26.1 MHz	31.5 MHz
	3	5.4 MHz	9.9 MHz	18.3 MHz	31.8 MHz	10.7 MHz	19.7 MHz	36.5 MHz	44.0 MHz
	4	6.9 MHz	12.7 MHz	23.5 MHz	40.8 MHz	13.8 MHz	25.3 MHz	46.9 MHz	56.5 MHz
	5	8.4 MHz	15.5 MHz	28.6 MHz	49.9 MHz	16.8 MHz	30.9 MHz	57.2 MHz	69.0 MHz
64/32	2	7.4 MHz	13.5 MHz	24.9 MHz	43.4 MHz	14.7 MHz	26.9 MHz	49.8 MHz	60.0 MHz
	3	10.3 MHz	18.8 MHz	34.9 MHz	60.7 MHz	20.5 MHz	37.6 MHz	69.7 MHz	84.0 MHz[4)]
	4	13.2 MHz	24.2 MHz	44.8 MHz	78.0 MHz	26.3 MHz	48.4 MHz	89.5 MHz[4)]	107.9 MHz[5)]
	5	16.1 MHz	29.6 MHz	54.7 MHz	95.3 MHz[4)]	32.1 MHz	59.1 MHz	109.4 MHz[5)]	131.8 MHz[5)]
96/48	2	10. 8 MHz	19.9 MHz	36.8 MHz	64.0 MHz	21.6 MHz	39.7 MHz	73.5 MHz	88.6 MHz[4)]
	3	15.1 MHz	27.8 MHz	51.5 MHz	89.6 MHz[4)]	30.2 MHz	55.6 MHz	102.9 MHz[5)]	124.0 MHz[5)]
	4	19.4 MHz	35.7 MHz	66.1 MHz	115.1 MHz[5)]	38.8 MHz	71.4 MHz	132.2 MHz[5)]	159.3 MHz[5)]
	5	23.7 MHz	43.6 MHz	80.8 MHz[4)]	140.7 MHz[5)]	47.4 MHz	87.2 MHz[4)]	161.5 MHz[5)]	194.7 MHz[5)]
128/64	2	14.3 MHz	26.3 MHz	48.6 MHz	84.7 MHz[4)]	28.4 MHz	52.5 MHz	97.2 MHz[4)]	117.2 MHz[5)]
	3	20.0 MHz	36.8 MHz	68.0 MHz	118.5 MHz[5)]	40.0 MHz	73.5 MHz	136.0 MHz[5)]	164.0 MHz[5)]
	4	25.7 MHz	47.2 MHz	87.5 MHz[4)]	152.3 MHz[5)]	51.4 MHz	94.4 MHz[4)]	174.9 MHz[5)]	210.8 MHz[5)]
	5	31.4 MHz	57.7 MHz	106.9 MHz[5)]	186.1 MHz[5)]	62.7 MHz	115.4 MHz[5)]	213.7 MHz[5)]	257.5 MHz[5)]

1) M_TTCAN starts always at filter element #0 and proceeds through the filter list to find a matching element. Acceptance filtering stops at the first matching element and the following filter elements are not evaluated for this message. Therefore, the sequence of configured filter elements has a significant impact on the performance of the filtering process.

2) Acceptance filtering search for 11-bit IDs and 29-bit IDs filter element is running separately, only one configured filter setting should be considered. Searching for one 29-bit filter element requires approximately double cycles for one 11-bit filter element.

3) See the device datasheet for the supported number of channels

4) Frequency is not reachable since the maximum host clock frequency for M_TTCAN in CYT2B6 is 80 MHz

5) Frequency is not reachable since the maximum host clock frequency for M_TTCAN in all TRAVEO™ T2G is 100 MHz

2 Functional deviations

Parameters Affected

N/A

Trigger condition(s)

Under the following conditions a received message will have corrupted data while the received message is signaled as valid to the host.

1. The data length code (DLC) of the received Message is greater than 4 (DLC > 4)
2. The storage of Ri of a received message into the Message RAM (after acceptance filtering is done) has not completed before R(i+1) is transferred from the CAN Core into the cache of the Rx Handler (where 2 ≤ i ≤ 5)
3. While condition 1 and 2 apply, a concurrent read of data word Ri from the cache and write of data word R(i+1) into the cache of the Rx handler happens

Scope of impact

The erratum is limited to the case when the Host clock frequency used in the actual device is below the limit shown in Table 2.

Corrupted data is written to the Rx FIFO element respective the dedicated Rx Buffer.

The received frame is nevertheless signaled as valid.

Workaround

Check whether the minimum Host clock frequency, that is shown in Table 2, is below the Host clock frequency used in the actual device.

If yes, there is no problem with the selected configuration.

If no, use one of the following two workarounds.

<First workaround>

Try different configuration by changing the following parameters until the actual host clock frequency (CLK_GR5) is above the minimum host frequency shown in Table 2.

- Increase the CLK_GR5 frequency in the actual device
- Reduce the CAN-FD Data Bit rate
- Reduce the number of configured filter elements
- Reduce the number of active CAN channels in an instance

Also, use DLC>=8 instead of DLCs 5, 6, and 7 in the CAN Environment/System, as they place higher demands on the minimum Host clock frequency (the worst case is DLC=5) or restrict your CAN Environment/System to DLC 4.

Note: While changing the actual host clock frequency, CLK_GR5 must always be equal or higher than PCLK_CANFD[x]_CLOCK_CAN[y] for all configurations.

<Second workaround>

Due to condition 3 the issue occurs only sporadically. Use an end-to-end (E2E) protection (for example, checksum or CRC covering the data field) and add it to all messages in the CAN system, to detect data corruption in received frames.

Fix status

No silicon fix planned. Use workaround.

Impact on Infineon software

Impact: Limitation

Related modules: CAN, MCU

Comment: The user must evaluate the impact of the erratum for each CAN instance separately. A CAN instance is the entirety of CanControllers with the same CanControllerInstance value.

1. For the number of active CAN nodes: Use the maximum number of CanController configurations of a CAN instance that can be active (Autosar controller state STARTED or SLEEP) at a time
2. For the host clock frequency: In McuPeriGroupSettings locate the setting with McuPeriGroup=MCU_PERI_GROUP5_MMIO5 and take the value from McuPeriGroupClockFrequency
3. For the number of configured active filter element 11-bit IDs/29-bit IDs: Use the corresponding values from the “Message RAM (…) linking table” in the generated Can_PBcfg.h file. Note that each CanController has its separate table. Take the maximum values.
4. For the Arbitration bit rate: Use the maximum CanControllerBaudRate value of all the CanControllers
5. For the Data bit rate: Use the maximum CanControllerFdBaudRate value of all the CanControllers if configured. Otherwise use CanControllerBaudRate.

2.23 [212] Description for PASS SARx to TCPWMx direct connect triggers one-to-one is incorrect in datasheet

Description

The body controller device's datasheet showed ‘trig=2’ in the description for PASS SARx to TCPWMx direct connect triggers one-to-one, which was incorrect as TCPWM’s input trigger selection (TR_IN_SEL) value. The correct value is ‘4’ as shown in the architecture TRM chapter 25 descriptions and table 25-2.

The cluster device's datasheet showed ‘trig=0’ in the description for PASS SARx to TCPWMx direct connect triggers one-to-one, which was incorrect as TCPWM’s input trigger selection (TR_IN_SEL) value. The correct value is ‘2’. Therefore, the correct description and table 25-2 in the architecture TRM chapter 25 are as follows.

Table 25-2 shows how the multiplexer should be handled for the input trigger event generation. The TRAVEO™ T2G Cluster MCU supports the following input triggers:

- Number of specific one-to-one trigger inputs: 1
- Number of general-purpose trigger inputs: 60

Table 3 Handling input trigger multiplexers for cluster devices

Input trigger selection	Input trigger	Input trigger source
0	Constant ‘0’	Constant ‘0’
1	Constant ‘1’	Constant ‘1’
2	HSIOM column ACT#2 or PASS (programmable analog subsystem), through 1:1 trigger mux #2	Refer to the "Alternate function pin assignments" or "Triggers one-to-one" section in the device datasheet
3	tr_all_cnt_in[0]	Refer to the trigger mux block in the device datasheet
:	:	:
62	tr_all_cnt_in[59]	Refer to the trigger mux block in the device datasheet

Parameters affected

N/A

Trigger condition(s)

Using the triggers one-to-one for PASS SARx to TCPWMx direct connect

Scope of impact

The triggers one-to-one for PASS SARx to TCPWMx direct connect cannot work if TCPWM's input trigger selection is not correct.

Workaround

For body devices, use '4' as TCPWM's input trigger selection (TR_IN_SEL) value for PASS SARx to TCPWMx direct connect.

For cluster devices, use '2' as TCPWM's input trigger selection (TR_IN_SEL) value for PASS SARx to TCPWMx direct connect.

Fix status

No silicon fix planned. Datasheet was updated.

Impact on Infineon Software

Impact: No

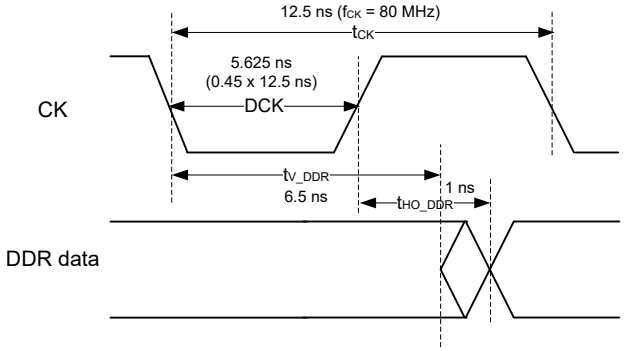
Related modules: PWM

Comment: MCAL PWM module does not support one-to-one triggers.

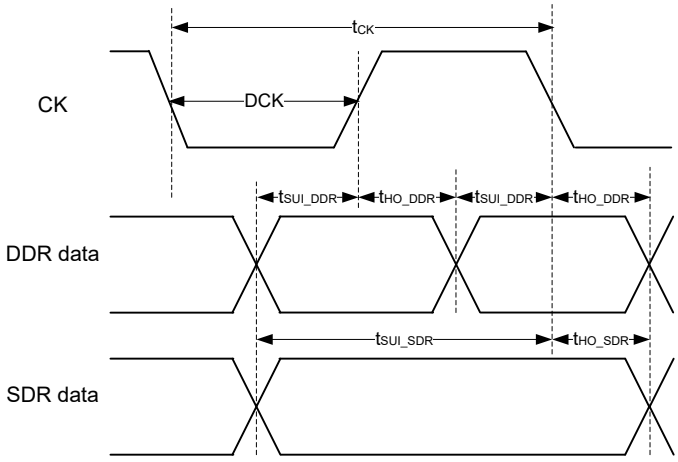
2.24 [215]SMIF HSSPI (SDR/DDR) spec change for read timing specification

Description

Existing read timing specification (data input) of SMIF HSSPI (SDR/DDR) has self-contradiction and required setup time for MCU is unclear. The example case (DDR for HSIO_STD) of this problem is shown below.



Therefore, we remove t_V spec (SID781/A/B/C) and add the setup time spec as below to avoid this problem.



Parameters affected

SID781, SID781A, SID781B, SID781C

Trigger condition(s)

Using the HSSPI (SDR/DDR) in SMIF.

Scope of impact

The read timings of SMIF HSSPI (SDR/DDR) specification are changed.

Workaround

We will add the following setup time spec (SID789/A/B/C) instead of removing the t_V spec (SID781/A/B/C).

Table 4 SMIF HSSPI (SDR/DDR) specification

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID789	$t_{SUI\_SDR\_HSIO}$	Input setup time	2	-	-	ns	SMIF_CTL.CLOCK_IF_RX_SEL=3, SMIF_CTL.DELAY_TAP_ENABLED=0
SID789A	$t_{SUI\_SDR\_GPIO}$	Input setup time	10	-	-	ns	SMIF_CTL.CLOCK_IF_RX_SEL=3, SMIF_CTL.DELAY_TAP_ENABLED=0
SID789B	$t_{SUI\_DDR\_HSIO}$	Input setup time	1.25	-	-	ns	SMIF_CTL.CLOCK_IF_RX_SEL=3, SMIF_CTL.DELAY_TAP_ENABLED=0
SID789C	$t_{SUI\_DDR\_GPIO}$	Input setup time	6	-	-	ns	SMIF_CTL.CLOCK_IF_RX_SEL=3, SMIF_CTL.DELAY_TAP_ENABLED=0

Fix status

No silicon fix planned. Datasheet was updated.

Impact on Infineon software

Impact: No
Related modules: None
Comment: Software in scope does not support the SMIF

2.25 [218]Greater change of Low voltage detection (LVD) level can issue an Over voltage detection (OVD) reset

Description

OVD and LVD share the common resistor ladder for reference voltages. Therefore, greater change of LVD level can cause greater voltage fluctuation at OVD reference voltage leading to OVD reset.

Parameter affected

N/A

Trigger condition(s)

Change of LVD trip selection bits (PWR_LVD_CTL/2.HVLVD1/2_TRIPSEL_HT) by a step width of more than 1 at V_{DDD} > 4.5 V.

Scope of impact

Greater change of LVD level can result in an OVD reset.

Workaround

Any of the following

1. Do not change LVD trip selection bits (PWR_LVD_CTL/2.HVLVD1/2_TRIPSEL_HT) from default setting 0.
2. Increment LVD trip selection bits (PWR_LVD_CTL/2.HVLVD1/2_TRIPSEL_HT) by a step width of 1 per 10 µs. Change LVD1 or LVD2 independently, not at the same time.

Fix status

No silicon fix planned. Use workaround.

The architecture technical reference manuals were updated:

- 002-19314 Rev. *J for body controller entry family
- 002-24401 Rev. *H for body controller high family
- 002-33175 Rev. *D for cluster entry family
- 002-25800 Rev. *F for cluster 2D family

Impact on Infineon software

Impact: Limitation

Related modules: MCU

Comment: Workaround (2) was implemented in MCAL MCU driver version 1.24. Users of older versions can apply one of the suggested workarounds in following ways: Leave McuHvLvdThreshold at its default value of MCU_HVLVD_THRESHOLD_2_8V_TO_2_825V, or apply MCU configurations with changes of McuHvLvdThreshold in steps of 0.1V only.

2.26 [229]System calls: improper usage of memory region end address in control logic

Description

Erroneous system calls execution status will be returned when passing parameters to system calls via SRAM region at the end of available SRAM.

Parameters affected

N/A

Trigger condition(s)

When SRAM_SCRATCH_DATA_ADDR for the following system calls end in the last available SRAM word:

- ProgramRow
- ProgramRow2 (only for CYT6BJ)
- ProgramWorkFlash
- ProgramWorkFlash2 (only for CYT6BJ)

Scope of impact

0xF0000013 (invalid arguments location) will be returned when passing parameters to system calls via SRAM region at the end of available SRAM.

Workaround

Do not use the last word of available SRAM for passing SRAM_SCRATCH_DATA_ADDR for the following system calls:

- ProgramRow
- ProgramRow2 (only for CYT6BJ)
- ProgramWorkFlash
- ProgramWorkFlash2 (only for CYT6BJ)

Fix status

No silicon fix planned. Use workaround.

Impact on Infineon software

Impact: Limitation

Related modules: FLS

Comment: Users of MCAL FLS must make sure that Fls_WriteData is not located immediately below the highest SRAM address. You can use memory mapping via FLS_START_SEC_VAR_NO_INIT_UNSPECIFIED and/or linker configuration to modify the location of the affected object.

2.27 [232]SDHC SD:DS mode spec change

Description

SDHC cannot meet the input setup/hold time in SD: DS mode. Therefore, the input setup/hold time (SID816/ SID818) and interface clock period (SID810) have been changed to meet the SD: DS mode specification.

Table 5 SDHC SD:DS timing specification

Spec ID	Description	Min	Typ	Max	Units	Details/ Conditions
SID810	Interface clock period	-	-	~~25~~ 16.7	MHz	~~40-ns period~~ 60-ns period

(table continues...)

Table 5 (continued) SDHC SD:DS timing specification

Spec ID	Description	Min	Typ	Max	Units	Details/ Conditions
SID816	Input setup time of CMD/DAT prior to CLK	~~24~~ 9	-	-	ns	
SID818	Input hold time of CMD/DAT after CLK	~~0~~ 2	-	-	ns	

Parameters affected

SID810, SID816, SID818

Trigger condition(s)

Using the SD: DS mode

Scope of impact

The maximum clock frequency (SID810) has been changed to 16.7 MHz to meet the input setup time (SID816) in SD: DS mode.

Workaround

Use the SD: DS mode with new parameters (SID810, SID816, SID818)

Fix status

No silicon fixed planned. Use workaround.

Impact on Infineon software

Impact: No
Related modules: None
Comment: Software in scope does not support the SDHC

2.28 [233]SDHC some modes are not supported

Description

CYT3BB/4BB/4BF do not support the eMMC: DDR mode. Therefore, the CYT3BB/4BB/4BF datasheet will be updated to remove the eMMC: DDR mode.

Parameter affected

SID896

Trigger condition(s)

Using the eMMC: DDR mode in CYT3BB/4BB/4BF.

Scope of impact

eMMC: DDR mode cannot be used in CYT3BB/4BB/4BF.

Workaround

Do not use the eMMC: DDR mode in CYT3BB/4BB/4BF.

FIx status

No silicon fixed planned.

Impact on Infineon software

Impact: No
Related modules: None
Comment: Software in scope does not support the SDHC

2.29 [234]Ethernet RGMII external mode issue

Description

Ethernet RGMII cannot be supported as external mode.

Parameter affected

SID385/B, SID386/B, SID385_1

Trigger condition(s)

Using RGMII

Scope of impact

- The support mode for RGMII has been changed to internal mode from external mode.
- ECO accuracy must be within +/- 50 ppm.
- For CYT6BJ device, the internal mode requires that REF_CLK 125 MHz should be created by using the internal PLL clock frequency (PLL_OUT) 250 MHz with 2 dividing of OUTPUT_DIV and divided by 2 with the register ETHx_CTL.REFCLK_DIV = ‘1’ setting.
- For CYT4BF device, no requirement for the internal PLL clock frequency (PLL_OUT) 250 MHz.
- For CYT4DN device, the internal mode requires that REF_CLK 125 MHz should be created by using the internal PLL clock frequency (PLL_OUT) 250 MHz with 2 dividing of OUTPUT_DIV and divided by 2 with the register CLK_ROOT_SELECT[x].ROOT_DIV = ‘1’ setting.

Workaround

Use the RGMII internal mode instead of external mode.

Fix status

No silicon fixed planned. Use workaround. Datasheets will be updated accordingly.

Impact on Infineon software

Impact: No
Related modules: None
Comment: Software in scope does not support the Ethernet

2.30 [235]Ethernet GMII is not supported

Description

Ethernet GMII is not supported. Therefore, datasheet and TRM will be updated to remove the GMII specifications.

Parameter affected

Ethernet GMII specifications (SID364B, SID365B, SID379 to SID384, SID389/A/B)

Trigger condition(s)

Using GMII

Scope of impact

Ethernet GMII cannot be used.

Workaround

Use RGMII instead of GMII

Fix status

No silicon fixed planned. Use workaround.

Impact on Infineon software

Impact: No
Related modules: None
Comment: Software in scope does not support the Ethernet

2.31 [237]CLK_HF5 cannot be configured as a separate, specific clock frequency for audio internal clock when CLK_HF4 is used for RGMII

Description

CLK_HF5 cannot be configured as a separate, specific clock frequency for audio internal clock when CLK_HF4 is used for RGMII because there is only one PLL (PLL400#1), which is common to CLK_HF4 and CLK_HF5.

Parameter affected

SID748

Trigger condition(s)

Using both of CLK_HF4 and CLK_HF5

Scope of impact

CLK_HF5 cannot be configured as a separate, specific frequency like 196.608 MHz of SID748 when CLK_HF4 is used for RGMII.

Workaround

Any of following:

1. Use the audio subsystem with the external clock via AUDIOSSx_CLK_I2S_IF pin
2. Use the same PLL frequency for CLK_HF5 as for CLK_HF4. In this case, the following conditions must be met:
   - Use the audio subsystem as slave (MCLK must be generated by the external master)
   - Use the audio subsystem internal clock (MCLK_SOC) frequency is 8 times or more than the frequency of the input serial clock (MCLK)
   - For CYT6BJ Rev. B RGMII 1 Gbps, PLL400#1 250 MHz is required and then CLK_HF5 can be used at 125 MHz by dividing 250 MHz of PLL400#1 by 2 using pre-divider.
   - For CYT4BF RGMII 1Gbps, PLL400#1 125 MHz is required and then CLK_HF5 can be used at 125 MHz by dividing 125 MHz of PLL400#1 by 1 using pre-divider.

Fix status

No silicon fixed planned. Use workaround.

Impact on Infineon software

Impact: Limitation

Related modules: None

Comment:

1. Clock roots for Audio and Ethernet are configured in the McuClockRootSettings container of the MCAL MCU module. PLLs are configured in the McuPllSettings container of the MCAL MCU module
2. The configuration of the I2S clock selection is out of scope of the software in scope

2.32 [242]RTC busy status bit stuck issue

Description

RTC busy status flag (BACKUP_STATUS.RTC_BUSY register bit) is abnormally stuck at HIGH even after configuring the RTC user registers and BACKUP_RTC_RW.WRITE register bit is cleared by the software.

Parameter affected

N/A

Trigger condition(s)

RTC user register write operation randomly triggers this problem.

Scope of impact

RTC operation may not work as expected. If the software polls BACKUP_STATUS.RTC_BUSY flag before moving to any other tasks, it will be stuck there.

Workaround

Use the following software workaround:

1. If BACKUP_STATUS.RTC_BUSY flag is set, then run the following dummy write sequence
2. Start the sequence for maximum 8 retries (‘retryCount’) and start with 1
   a. Write ‘1’ to BACKUP_RTC_RW.WRITE register for 'retryCount' times
   b. Write ‘0’ to BACKIP_RTC_RW.WRITE register
   c. Wait for 6 CLK_LF cycles (ILO0 or WCO)

d. If BACKUP_STATUS.RTC_BUSY flag is '0', exit the loop

e. If 'retryCount' reaches to '8', then handle this error according to user system requirement for failure case unrelated to this errata (e.g. write '1' to BACKUP_RESET.RESET register) else run dummy write sequence from "a". Workaround for this errata needs to maximum 8 retries.

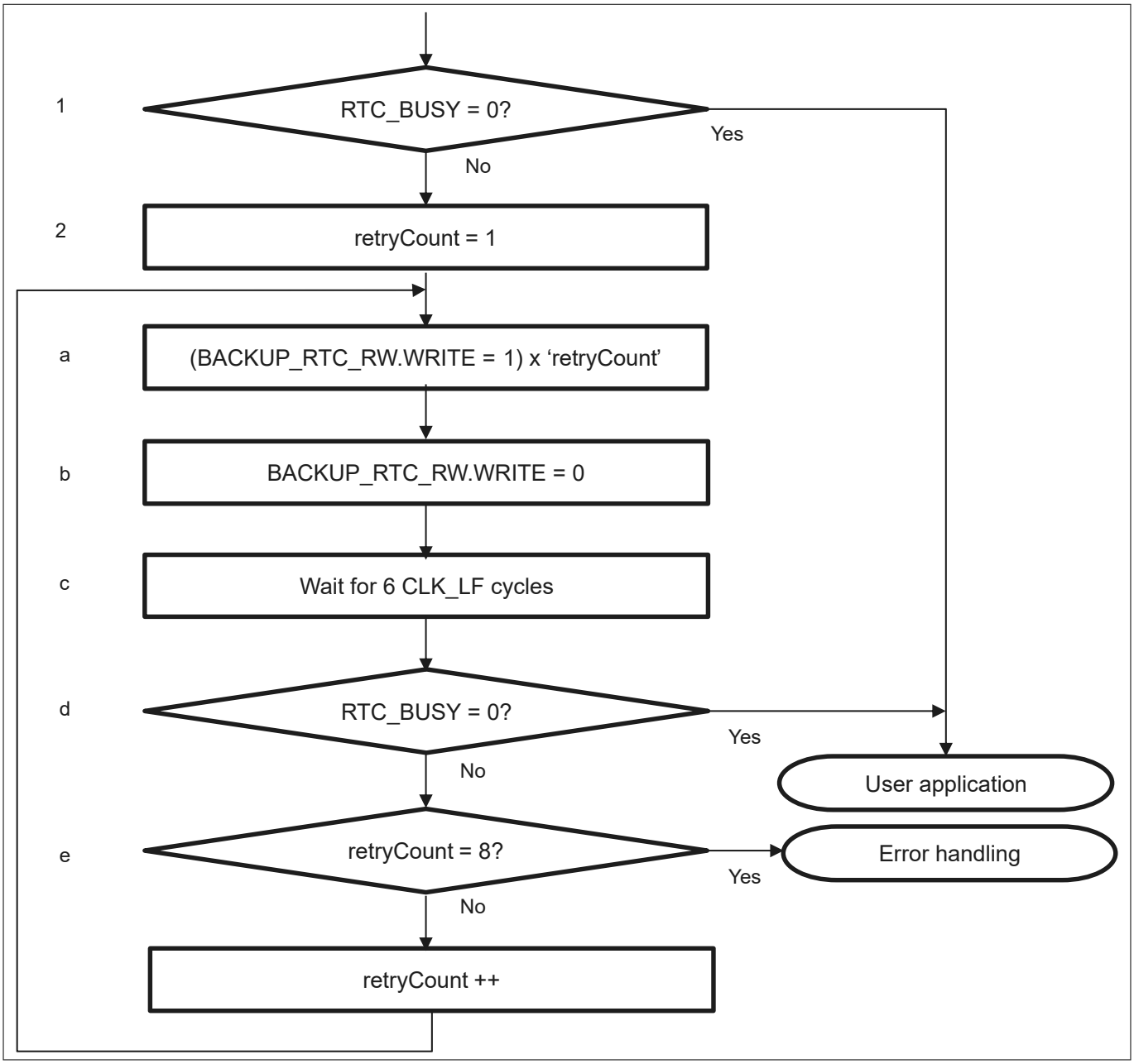


Figure 3 RTC software workaround

Fix status

No silicon fix planned. Use workaround.

Impact on Infineon software

Impact: None
Related modules: N/A
Comments: Software in scope does not access RTC registers.

2.33 [770]PLD might perform linefill to address that would generate a MemManage Fault (Arm® CM7 errata ID: 1013783)

Description

If the MPU is present and enabled, then it can be programmed so that loads to certain addresses generate a MemManage Fault.

This could be because:

- The address is unmapped, that is, it is not in an enabled region and the default memory map is not being used
- The address cannot be accessed at the current privilege level
- The address cannot be accessed at any privilege level

Because of this erratum, a PLD to such an address might incorrectly cause a data cache linefill.

Parameters affected

N/A

Trigger condition(s)

1. The data cache is enabled and the MPU is enabled
2. A PLD is executed, and either:
  a. The PLD is to an address not mapped in the MPU, which requires that:
    1. The MPU is enabled
    2. The default memory map is not being used
    3. The default memory map is cacheable at that address
    4. The PLD does not hit an enabled MPU region
  b. The PLD is to a region that has permission requirements that the PLD does not meet, which requires that:
    1. The MPU is enabled
    2. The default memory map is not being used
    3. The region that the PLD hits is cacheable
    4. The region that the PLD hits would generate a MemManage fault for a load. This requires either:
      a. The region cannot be accessed by a read at any privilege level
      b. The region only has read access for privileged code and the PLD is unprivileged

Note that in rare cases, a PLD instruction can be speculatively executed in the shadow of a mispredicted branch. This can even theoretically be a literal value that decodes to a PLD.

Scope of impact

Processor execution is not affected by this erratum. The data returned from the linefill is not directly consumed by the PLD. Any subsequent load to that address can only access the data if it has permissions to do so. This erratum does not permit software to access data that it does not have permissions for.

The only implications of this erratum are the access itself which should not have been performed. This might have an impact on memory regions with side-effects on reads or on memory which never returns a response on the bus.

Workaround

Accesses to memory that is not mapped in the MPU can be avoided by using MPU region 0 to cover all unmapped memory and make this region execute-never and inaccessible.

That is, MPU_RASR0 should be programmed with:

- MPU_RASR0.ENABLE = 1 ; MPU region 0 enable

- MPU_RASR0.SIZE = b11111 ; MPU region 0 size = 2^32 bytes to cover entire memory
- MPU_RASR0.SRD = b00000000 ; All sub-regions enabled
- MPU_RASR0.XN = 1; Execute-never to prevent instruction fetch
- MPU_RASR0.AP = b000; No read or write access for any privilege level
- MPU_RASR0.TEX = b000 ; Attributes = Strongly-ordered
- MPU_RASR0.C = b0 ; Attributes = Strongly-ordered
- MPU_RASR0.B = b0 ; Attributes = Strongly-ordered

Accesses to memory that is mapped in the MPU, but should not be accessed at the current privilege level can be avoided by making the region non-cacheable.

That is, MPU_RASR0 should be programmed with:

- MPU_RASR0.TEX = b000 ; Attributes = Strongly-ordered
- MPU_RASR0.C = b0 ; Attributes = Strongly-ordered
- MPU_RASR0.B = b0 ; Attributes = Strongly-ordered

Fix status

No silicon fix planned. Use workaround.

Impact on Infineon software

Impact: None

Related modules: N/A

Comment: This erratum would only have noticeable effects if a PLD targeted the address of an MMIO with side-effects on reading. Conditions of the erratum are not met for such addresses: they are not cacheable in the default memory map (condition 2.a.3) and any meaningful MPU configuration (condition 2.b.3).

2.34 [771]ECC error causes data corruption when the data cache error bank registers are locked (Arm® CM7 errata ID: 1267980)

Description

The data cache contains two error bank registers, DEBR0 and DEBR1. These registers store the locations in the cache that Error Correcting Code (ECC) errors affect and prevent future allocations to those locations.

Software can lock each DEBR and this prevents the DEBR from being automatically updated when a data cache ECC error is detected.

Because of this erratum, if both DEBR0 and DEBR1 are locked and an ECC error is detected on a cacheable store, then the store data is written onto the bus but not written into the data cache. This might result in the data cache containing stale data.

Parameters affected

N/A

Trigger condition(s)

- DEBR0 and DEBR1 are locked
- The wanted address has been allocated to the cache
- A cacheable store to the wanted address looks up in the cache, and an ECC error is found in the cache set that the store addresses

Scope of impact

This erratum can cause data corruption in the data cache.

Workaround

Software must avoid locking both error bank registers.

Fix status

No silicon fix planned. Use workaround.

Impact on Infineon software

Impact: Limitation

Related modules: N/A

Comment: Software in scope does not use CM7_SCS_DEBR0 and CM7_SCS_DEBR1. Other software must not lock (set bit #1 of) the CM7_SCS_DEBR0 and CM7_SCS_DEBR1 registers at the same time.

2.35 [772]Data corruption for load following Store-Exclusive (Arm® CM7 errata ID: 1315869)

Description

A load that follows a Store-Exclusive to the same address might forward data from an earlier store, situated between the Load-Exclusive and the Store-Exclusive, and not the data from the Store-Exclusive.

Parameter affected

N/A

Trigger condition(s)

The following sequence is required for this erratum to occur:

1. A load exclusive sets the local monitor
2. A store to the wanted address
3. Any of the following instructions to the wanted address. This instruction must not fail either the local or global monitor check
   a. STREXB
   b. STREXH
   c. STREX
4. A load to the wanted address

There must be at most one instruction between the Store-Exclusive and the load. All accesses must be to Shareable memory.

Scope of impact

Data corruption occurs when the load returns data from the older store instead of the newer Store- Exclusive.

Stores between a Load-Exclusive and Store-Exclusive are not expected in real code because such stores can always clear the local monitor in some implementations.

Workaround

No workaround is necessary.

Fix status

No silicon fix planned.

Impact on Infineon software

Impact: None

Related modules: N/A

Comment: Software in scope does not use exclusive load and store. Other software, if using exclusive load and store, can be affected.

2.36 [773]TCM bandwidth sharing between AHBS writes and software stores might not function correctly when using TCM wait states (Arm® CM7 errata ID: 2328489)

Description

The TCM Control Unit (TCU) contains a Store Queue (SQ) FIFO that buffers Tightly Coupled Memory (TCM) writes. Software stores and AHBS writes both go through the SQ. A round-robin scheme is used to fairly share the SQ ingress bandwidth between software stores and AHBS writes when contention occurs. Due to this erratum, AHBS writes might take priority over 64-bit software stores, which can stall processor instruction execution while the AHBS writes are ongoing. Software stores take priority over AHBS writes and therefore this erratum does not occur when there is adequate TCM bandwidth available.

Parameters affected

N/A

Trigger condition(s)

This erratum can occur when either an STRD, STM, PUSH, VPUSH, VSTR.64, or VSTM instruction is executed targeting TCM during a long stream of back-to-back AHBS write transfers and TCM wait states are used.

Also, if a load instruction closely follows after a 64-bit store instruction to TCM that stalls the execution pipeline, then this will further exacerbate the issue. If the pipeline is stalled, the read will still go ahead but the data returned will be discarded. Hence, a TCM read will be repeated until the stall ends.

Scope of impact

This erratum only affects the performance of the Cortex®-M7 processor. It can cause the processor's execution pipeline to stall when executing a 64-bit store instruction while back-to-back AHBS writes are ongoing. When the AHBS back-to- back write stream ends, the 64-bit store will be accepted into the SQ and the pipeline will stop stalling.

Workaround

Do not modify CPUSS_CM7_x_CTL.ITCM_READ_WS and CPUSS_CM7_x_CTL.DTCM_READ_WS. By default, these registers are initialized to 0.

Fix status

No silicon fix planned. Use workaround.

Impact on Infineon software

Impact: Limitation

Related modules: N/A

Comment: The user must not modify CPUSS_CM7_x_CTL.ITCM_READ_WS and CPUSS_CM7_x_CTL.DTCM_READ_WS. By default, these registers are initialized to 0, so there are no TCM wait states and, hence, the erratum will not come into effect.

2.37 [774]Cortex®-M7 can halt in an incorrect address when breakpoint and exception occurs simultaneously (Arm® CM7 errata ID: 3092511)

Description

When an asynchronous exception occurs at the same time as a breakpoint event (either hardware breakpoint or software breakpoint), it is possible for the processor to halt at the beginning of the exception handler instead of the instruction address pointed by the breakpoint.

Parameters affected

N/A

Trigger condition(s)

The BKPT bit in Debug Fault Status Register (DFSR) is set, indicating that a breakpoint event has occurred. The return address of the exception is the breakpoint address. As a result, if the debugger clears the halting control bit in the processor at this point, the processor will reach the breakpoint again after servicing the exception.

The following conditions are required:

1. Halt mode debug is enabled and is permitted by debug authentication configuration
2. The processor reaches the breakpoint as the same time that the asynchronous exception is invoked

Scope of impact

A debugger connected to the Cortex®-M7 can detect the processor is halted after a breakpoint is hit, but might not be able to determine which breakpoint has triggered the halting.

Workaround

This issue only affect the debugger's operation. The debugger could report the halting reason as an unknown breakpoint, and optionally resume operation. If the processor's operation is resumed, it is likely to be halted again immediately after the interrupt is serviced and returns to the breakpoint address.

Fix status

No silicon fix planned.

Impact on Infineon software

Impact: None

Related modules: N/A

Comment: This erratum only affects debugging.

Revision history of CYT4BF errata sheet

Document version	Date of release	Description of changes
1.0	2020-05-14	Initial release
1.1	2020-06-17	Added errata ID 133
1.2	2020-08-28	Updated "Fix status" in errata ID 133. Added errata ID 136 to 139.
1.3	2021-02-18	Added errata ID 147.
1.4	2021-06-29	Added errata ID 161, 163, 164.
1.5	2021-09-16	Updated "Workaround" of errata ID 147. Added errata ID 167, 168, 169.
1.6	2022-01-21	Added errata ID 175, 176, 177.
1.7	2022-07-04	Updated “Fixed status” of errata ID 169. Added errata ID 185.
1.8	2022-08-25	Updated “Description” of errata ID 185. Added errata ID 198, 199.
1.9	2022-12-02	Added errata ID 201, 202, 203, 204.
2.0	2023-02-08	Updated the description to 5 ILO0 cycles in errata ID 201. Updated "Description" of errata ID 203. Fixed the register name of errata ID 204. Added errata ID 206.
2.1	2023-06-15	Updated descriptions of errata ID 133. Updated errata ID 206 to add (or bank#1 if dual bank mode with mapping B is used). Added errata ID 209.
2.2	2023-10-17	Updated errata ID 206 to add the affected SROM APIs. Added errata ID 212.
2.3	2024-08-23	Added errata ID 215, 218.
2.4	2025-02-21	Added errata ID 299, 232 to 235, 237. Updated the “Impact on Infineon software” of errata ID 218. Removed errata ID 136, 161, 163, 164, 168, 169 because the datasheet was updated for errata ID 161, 163, 164, 168, 169, and errata ID 136 was fixed before official release.
2.5	2025-03-28	Migrated to Infineon errata template. Consolidated the description for all affected devices (each errata ID 137, 138, 198, 203, 206, 209, 212, 237).
2.6	2025-09-30	Removed "sometimes" from description of errata ID 229. Consolidated the description for all affected devices of errata ID 234. Added errata ID 242 and 770 to 774.

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Edition 2025-09-30

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about any aspect of this document?

Email: erratum@infineon.com

Document reference
IFX-zbf1724744550518

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