TRAVEO™ T2G CYT3DL errata sheet

Marking/Step: Rev. B

32-bit single-chip microcontroller

About this document

Scope and purpose

This document describes the deviations of the device from the current user documentation, to support the assessment of the effects of these deviations on your custom hardware and software implementations.

Please take note of the following information:

- This errata sheet applies to all temperature and frequency versions and to all memory size variants, unless explicitly noted otherwise. For a derivative synopsis, see the latest datasheet or user manual
- Multiple device variants are covered in this one document. If an issue is related to a particular module, and this module is not specified for a specific device variant, then the issue does not apply to that device variant
- Devices marked with ES are engineering samples which may not be completely tested in all functional and electrical characteristics and are therefore only suitable for evaluation
- Some of the errata have workarounds which may be supported by the tool vendors. Some corresponding compiler switches may need to be set. Please refer to the respective documentation of your compiler
- To understand the effect of issues relating to the on-chip debug system, please refer to the respective debug tool vendor documentation

Current documentation

- TRAVEO™ T2G automotive MCU cluster 2D architecture technical reference manual
- TRAVEO™ T2G automotive MCU cluster 2D registers technical reference manual for CYT3DL
- CYT3DL datasheet TRAVEO™ T2G automotive MCU

Newer versions replace older versions, unless specifically stated otherwise.

Please always refer to the corresponding documentation for this device available in the category 'Documents' at www.infineon.com/TRAVEO™.

Conventions used in this document

Each erratum identifier follows the pattern [Number]:

- [Number] = ascending sequential number within the three

  ***Note**:* *[Number] As this sequence is used over several derivatives, including already solved deviations, gaps can occur inside this numbering sequence*

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1 Errata overview

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1 Errata overview

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2 Functional deviations

2.1 [096] CAN FD RX FIFO top pointer feature does not function as expected

Description

RX FIFO top pointer function calculates the address for received messages in Message RAM by hardware. This address should be re-start back from the start address after reading all messages of RX FIFO n size (n: 0 or 1). However, the address does not re-start back from the start address when RX FIFO n size is set to 1 (CANFD_CH_RXFnC.FnS = 0x01). This results in CPU/DMA to read messages from the wrong address in Message RAM.

Parameters affected

N/A

Trigger condition(s)

RX FIFO top pointer function is used when RX FIFO n size set to 1 element (CANFD_CH_RXFnC.FnS = 0x01).

Scope of impact

Received message cannot be correctly read by using RX FIFO top pointer function, when RX FIFO n size set to 1 element.

Workaround

Any of the following

1. Set RX FIFO n size to 2 or more when using RX FIFO top pointer function.
2. Do not use RX FIFO top pointer function when RX FIFO n size set to 1 element. Instead of RX FIFO top pointer, read received messages from the Message RAM directly.

Fix status

No silicon fix planned. Use workaround.

2.2 [097] CAN FD debug message handling state machine not get reset to Idle state when CANFD_CH_CCCR.INIT is set

Description

If either CANFD_CH_CCCR.INIT bit is set by the Host or when the M_TTCAN module enters BusOff state, the debug message handling state machine stays in its current state instead of being reset to Idle state. Configuring the bit CANFD_CH_CCCR.CCE does not change CANFD_CH_RXF1S.DMS.

Parameters affected

N/A

Trigger condition(s)

Either CANFD_CH_CCCR.INIT bit is set by the Host or when the M_TTCAN module enters BusOff state.

Scope of impact

The errata is limited to the use case when the Debug on CAN functionality is active. Normal operation of CAN module is not affected, in which case the debug message handling state machine always remains in Idle state. In the described use case, the debug message handling state machine is stopped and remains in the current state signaled by the bit CANFD_CH_RXF1S.DMS. In case CANFD_CH_RXF1S.DMS is set to 0b11, DMA request remains active. Bosch classifies this as non-critical error with low severity, there is no fix for the IP, Bosch recommends the workaround listed also here.

Workaround

In case the debug message handling state machine has stopped while CANFD_CH_RXF1S.DMS is 0b01 or 0b10, it can be reset to Idle state by hardware reset or by reception of debug messages after CANFD_CH_CCCR.INIT is reset to zero.

Fix status

No silicon fix planned. Use workaround.

2.3 [137]Limitation of work flash reading

Description

1. Work flash can be read via different CPU cores but only one CPU core is assigned for non-correctable ECC error handling
2. Reading 32 bits of work flash on AXI bus can result in ECC error (Only for CM7 core devices)

Parameter affected

N/A

Trigger condition(s)

1. Reading work flash via CPU core and ECC fault interrupt routed to two or more CPU cores
2. Reading 32 bits of work flash via CM7_0/1 or other AXI master and adjacent 32 bits of work flash is not initialized (Only for CM7 core devices)

Scope of impact

1. Only one CPU core can be assigned for non-correctable ECC error handling
2. Work flash should be accessed via AHB or AXI with 64-bit boundary (Only for CM7 core devices)

Workaround

Any of the following:

- Option A (Recommended solution)
  - Problem 1 and problem 2: Set each CPU core to use a separate AHB DMA (M-DMA or P-DMA) channel to read work flash. If non-correctable ECC error occurs, the DMA transaction get aborted and respective CPU core gets the interrupt to manage the non-correctable ECC error

- Option B
  - Problem 1[1]: Set non-correctable ECC error handling to reset. This way no one CPU core needs to manage the non-correctable ECC error handling
  - Problem 2: Limit work flash data size to 64 bits. Program work flash in units of aligned 64-bit double words and read it as 64-bit double words thru CM7_0/1 or another AXI master (Only for CM7 core devices)
- Option C
  - Problem 1[2]: Assign one CPU core for non-correctable ECC error handling and that core informs the error to the other core which caused the error, but it takes time
  - Problem 2: Use Option B

Fix status

No silicon fix planned. Use workaround. Infineon FLS and FEE driver were updated with workaround A. TRM was updated for this limitation.

2.4 [146]Potential AXI interconnect hang-up when Graphics Subsystem is powered off

Description

When Graphics Subsystem is powered off while there are outstanding AXI transactions from CPU (and/or other sources) to VRAM, it would hang-up the system interconnect.

Parameter affected

N/A

Trigger condition(s)

Application software powering off the Graphics Subsystem while there are outstanding AXI transactions from CPU (and/or other sources) to VRAM.

Scope of impact

Powering off the Graphics Subsystem can hang-up the system interconnect.

Workaround

Before disabling the Graphics Subsystem, ensure that there are no outstanding AXI accesses from CPUSS to the VRAM:

- Confirm that M-DMA(AXI-DMA) and Ethernet MAC have completed their transfers to/from VRAM, and do not setup any new transfers to/from VRAM or with the descriptor in VRAM
- Ensure that CM7 is not executing code from VRAM
- Ensure that no VRAM addresses are cached in the CM7's caches, and that the VRAM address range is configured to non-cacheable
- Confirm that there are no outstanding transactions from the CM7 CPU to VRAM, e.g. by the following sequence:
  1. Read a certain address from the VRAM
  2. Write a different value to this VRAM address

1 Not recommended to use for EEPROM emulation. EEPROM emulation needs to cope with aborted write/erase. In such a scenario, option B leads to deadlock in endless resets. However, option B can be used if work flash update is not intended in the field.
2 Not recommended to use with MCAL, since the inter-core communication is too slow.

3. Read back this VRAM address and confirm that the written value is read
4. Do not perform any additional accesses to VRAM

Now it is safe to disable the Graphics Subsystem.

Fix status

There is no plan for any change of hardware or of the graphics driver.

2.5 [147]CAN FD controller message order inversion when transmitting from dedicated Tx Buffers configured with same Message ID

Description

Configuration:

Several Tx Buffers are configured with same Message ID. Transmission of these Tx Buffers is requested sequentially with a delay between the individual Tx requests.

Expected behavior:

When multiple Tx Buffers that are configured with the same Message ID have pending Tx requests, they shall be transmitted in ascending order of their Tx Buffer numbers. The Tx Buffer with lowest buffer number and pending Tx request is transmitted first.

Observed behavior:

It may happen, depending on the delay between the individual Tx requests, that in the case where multiple Tx Buffers are configured with the same Message ID the Tx Buffers are not transmitted in order of the Tx Buffer number (lowest number first).

Parameters affected

N/A

Trigger condition(s)

When multiple Tx Buffers that are configured with the same Message ID have pending Tx requests.

Scope of impact

In the case described it may happen, that Tx Buffers configured with the same Message ID and pending Tx request are not transmitted with lowest Tx Buffer number first (message order inversion).

Workaround

Any of the following:.

1. First write the group of Tx message with the same Message ID to the Message RAM and then afterwards request transmission of all these messages concurrently by a single write access to CANFDx_CHy_TXBAR. Before requesting a group of Tx messages with this Message ID ensure that no message with this Message ID has a pending Tx request.
2. Use the Tx FIFO instead of dedicated Tx Buffers for the transmission of several messages with the same Message ID in a specific order.

Applications not able to use workaround #1 or #2 can implement a counter within the data section of their messages sent with same ID in order to allow the recipients to determine the correct sending sequence.

Fix status

No silicon fix planned. Use workaround.

2.6 [153]No YUV422 allowed in Direct Capture Mode

Description

When VIDEOSS is operating in Direct Capture Mode (video input data goes directly to a display without frame buffer interaction) the YUV 4:2:2 to 4:4:4 up-sampling function is corrupting video in a way that prevents the display engine to properly synchronize.

Parameters affected

N/A

Trigger condition(s)

RASTERMODE = YUV422 in ExtScr4 when destination is ExtDst4 and not Store4 unit.

Scope of impact

YUV422 cannot be used as a color format for video sources in video feed-through applications.

Workaround

Use capture to display with frame buffers or use video source with RGB or YUV444 format.

Fix status

No silicon fix planned. Use workaround.

2.7 [167]CAN FD incomplete description of Dedicated Tx Buffers and Tx Queue related to transmission from multiple buffers configured with the same Message ID

Description

The following is the updated description in Section 3.5.2 Dedicated Tx Buffers and 3.5.4 Tx Queue of the Architecture TRM related to transmission from multiple buffers configured with the same Message ID.

3.5.2 Dedicated Tx Buffers

- Wording TRM: If multiple Tx Buffers are configured with the same Message ID, the Tx Buffer with the lowest buffer number is transmitted first.
- Enhancement: These Tx buffers shall be requested in ascending order with lowest buffer number first. Alternatively all Tx buffers configured with the same Message ID can be requested simultaneously by a single write access to CANFDx_CHy_TXBAR.

3.5.4 Tx Queue

- Wording TRM: If multiple queue buffers are configured with the same Message ID, the queue buffer with the lowest buffer number is transmitted first.
- Replacement: In case that multiple Tx Queue buffers are configured with the same Message ID, the transmission order depends on numbers of the buffers where the messages were stored for transmission. As these buffer numbers depend on the then current states of the PUT Index, a prediction of the transmission order is not possible.
- Wording TRM: An Add Request cyclically increments the Put Index to the next free Tx Buffer.
- Replacement: The PUT Index always points to that free buffer of the Tx Queue with the lowest number.

Parameters affected

N/A

Trigger condition(s)

Using multiple dedicated Tx Buffers or Tx Queue Buffers configured with the same Message ID

Scope of impact

In the case the dedicated Tx Buffers with the same Message ID are not requested in ascending order or at the same time or in case of multiple Tx Queue Buffers with the same Message ID, it cannot be guaranteed, that these messages are transmitted in ascending order with lowest buffer number first.

Workaround

In case a defined order of transmission is required the Tx FIFO shall be used for transmission of messages with the same Message ID. Alternatively dedicated Tx Buffers with the same Message ID shall be requested in ascending order with lowest buffer number first or by a single write access to CANFDx_CHy_TXBAR. Alternatively a single Tx Buffer can be used to transmit those messages one after the other.

Fix status

No silicon fix planned. Use workaround.

The architecture technical reference manuals were updated:

- 002-19314 Rev. *H for body controller entry family
- 002-24401 Rev. *F for body controller high family
- 002-33175 Rev. *A for cluster entry family
- 002-25800 Rev. *D for cluster 2D family

2.8 [172]SWRESET register field of VIDEOSS0_TCONx_SWRESET violates the spec

Description

1. Some devices might have wrong reset values upon reset.
2. The SWRESET field read as zero indicates TCON registers being at reset state. However, according to the spec, a value of one being read on SWRESET field should indicate the reset state
3. When TCON enters reset, not all registers are reset.

Parameters affected

N/A

Trigger condition(s)

On system reset and while writing to the SWRESET register

Scope of impact

No impact since the register is not used by the software for debug and not used in customer applications

Workaround

Write only zero to the SWRESET register field to not trigger the reset active state. This register should not be used at all since other register fields of this register are for miniLVDS and this feature is not supported.

Fix status

No silicon fix planned. Use workaround.

2.9 [175]Misleading status is returned for Flash and eFuse system calls if there are pending NC ECC faults in SRAM controller #0

Description

Flash and eFuse system calls will return misleading status of 0xf0000005 (“Page is write protected”) even for non-protected row or 0xf0000002 (“Invalid eFuse address”) for valid eFuse address in case of pending NC ECC faults in SRAM controller #0.

Parameters affected

Return status of Flash and eFuse system calls

Trigger condition(s)

NC ECC fault(s) pending in SRAM controller #0 and SWPUs are populated in the design.

Scope of impact

Flash and eFuse system calls will not work until the NC ECC fault(s) pending in SRAM controller #0 is properly handled.

Workaround

If the NC ECC fault(s) are not due to hardware malfunction (i.e. if the faults are due to usage of non-initialized SRAM or improper SRAM initialization), then clearing of these pending faults will resolve the issue.

Fix status

No silicon fix planned.
The architecture technical reference manuals were updated:

- 002-19314 Rev. *I for body controller entry family
- 002-24401 Rev. *G for body controller high family
- 002-33175 Rev. *A for cluster entry family
- 002-25800 Rev. *D for cluster 2D family

2.10 [176]WDT reset causes loss of SRAM retention

Description

Architecture TRM Table 19-1 shows WDT reset can retain SRAM if there is an orderly shutdown of the SRAM only during a warning interrupt. However, this is wrong. WDT reset causes loss of SRAM retention.

Parameters affected

N/A

Trigger condition(s)

WDT reset

Scope of impact

WDT reset causes loss of SRAM retention.

Workaround

None

Fix status

No silicon fix planned.
The architecture technical reference manuals were updated:

- 002-19314 Rev. *I for body controller entry family
- 002-24401 Rev. *G for body controller high family
- 002-33175 Rev. *A for cluster entry family
- 002-25800 Rev. *D for cluster 2D family

2.11 [185]Crypto ECC errors may be set after boot with application authentication

Description

Due to the improper initialization of the Crypto memory buffer, Crypto ECC errors may be set after boot with application authentication. In spite of the Crypto ECC errors, the result of the authentication is reliable.

Parameters affected

N/A

Trigger condition(s)

Boot device with application authentication

Scope of impact

Crypto ECC errors may be set after boot with application authentication.

Workaround

Clear or ignore Crypto ECC errors which generated during boot with application authentication.

Fix status

No silicon fix planned.
The architecture technical reference manuals were updated:

- 002-19314 Rev. *I for body controller entry family
- 002-24401 Rev. *G for body controller high family
- 002-33175 Rev. *A for cluster entry family
- 002-25800 Rev. *E for cluster 2D family

2.12 [198]Incomplete erase of Code Flash cells could happen Erase Suspend / Erase Resume is used along with Erase Sector operation in Non-Blocking mode

Description

Code Flash memory can be erased in “Non-Blocking” mode; a Non-Blocking mode supported option allow users to suspend an ongoing erase sector operation. When an ongoing erase operation is interrupted using “Erase Suspend” and “Erase Resume”, Flash cells may not have been erased completely, even after the erase operation complete is indicated by FLASHC_STATUS register. Only Code Flash is impacted by this issue, Work Flash and Supervisory Flash (SFlash) are not impacted.

Parameters affected

N/A

Trigger condition(s)

Using EraseSector System Call in Non-Blocking mode for CM0+ to erase Code Flash and the ongoing erase operation is interrupted using EraseSuspend and EraseResume System calls.

Scope of impact

When Code Flash sectors are erased in Non-Blocking mode and the ongoing erase operation is interrupted by Erase Suspend / Erase Resume, it cannot be guaranteed that the Code Flash cells are fully erased. Any read on the Code Flash area after the erase is complete or read on the programmed data after ProgramRow is complete can trigger ECC errors.

Workaround

Any of the following

1. User can use Non-Blocking mode for EraseSector, but users must not interrupt the erase operation using Erase Suspend / Erase Resume.
2. If a Code Flash sector erase operation is interrupted using Erase Suspend / Erase Resume, then erase the same sector again without Erase Suspend / Erase Resume before reading the sector or programming the sector.

Fix status

Fixed to update the Flash settings from the following date code

- CYT2B6/7/9: 304xxxxx
- CYT2BL: 312xxxxx
- CYT3BB/4BB: 240xxxxx
- CYT4BF: 312xxxxx
- CYT2CL: 312xxxxx
- CYT3DL: 312xxxxx
- CYT4DN: 312xxxxx

2.13 [199]Limitation for keeping the port state from peripheral IP after wakeup from DeepSleep

Description

The port state is not retained when the port selects peripheral IP (except for LIN or CAN FD) and MCU wakes up from DeepSleep.

Parameters affected

N/A

Trigger condition(s)

The port selects peripheral IP (except for LIN or CAN FD) and MCU wakes up from DeepSleep.

Scope of impact

Unexpected port output change might affect user system.

Workaround

If the port selects peripherals IP (except for LIN or CAN FD) and the port output value need to keep after wakeup from DeepSleep, set HSIOM_PRTx_PORT_SEL.IOy_SEL = 0 (GPIO) before DeepSleep and set the required output value in GPIO configuration registers. After wakeup, change HSIOM_PRTx_PORT_SEL.IOy_SEL back to the peripheral IP.

Fix status

No silicon fix planned.

The architecture technical reference manuals were updated:

- 002-19314 Rev. *I for body controller entry family
- 002-24401 Rev. *G for body controller high family
- 002-33175 Rev. *B for cluster entry family
- 002-25800 Rev. *E for cluster 2D family

2.14 [201]A part of the PWR_CTL2.BGREF_LPMODE description is lacked in the existing register TRM

Description

The following is lacked from the PWR_CTL2.BGREF_LPMODE description in the existing register TRM.

“This register will not set unless CLK_ILO0_CONFIG.ILO0_ENABLE==1. When changing back to continuous operation, keep ILO0 enabled for at least 5 ILO0 cycles after clearing this bit to allow for internal synchronization.”

Parameters affected

N/A

Trigger condition(s)

Using the PWR_CTL2.BGREF_LPMODE

Scope of impact

PWR_CTL2.BGREF_LPMODE may not be set or cleared.

Workaround

Use the PWR_CTL2.BGREF_LPMODE according to the following description.

“This register will not set unless CLK_ILO0_CONFIG.ILO0_ENABLE==1. When changing back to continuous operation, keep ILO0 enabled for at least 5 ILO0 cycles after clearing this bit to allow for internal synchronization.”

Fix status

No silicon fix planned. Register TRM was updated.

2.15 [202]Limitation of clock configuration before entering DeepSleep mode

Description

DeepSleep should not be entered while any FLL/PLL is enabled and using ECO as its reference clock. Since the unstable ECO clock after wakeup is outside the allowed reference clock limits for FLL/PLL, there is possibility of failing the DeepSleep wakeup.

Parameters affected

N/A

Trigger condition(s)

DeepSleep transition while any FLL/PLL is enabled and using ECO as its reference clock.

Scope of impact

There is possibility of failing the DeepSleep wakeup.

Workaround

If any FLL/PLL is operating with the ECO as its reference clock, change the clock to either ECO direct or IMO direct or IMO with FLL/PLL before entering DeepSleep.

Fix status

No silicon fix planned.
The architecture technical reference manuals were updated:

- 002-19314 Rev. *I for body controller entry family
- 002-24401 Rev. *G for body controller high family
- 002-33175 Rev. *B for cluster entry family
- 002-25800 Rev. *E for cluster 2D family

2.16 [203]Several data retention information in Register TRM are incorrect

Description

The following registers are described as ‘Retained’ in the Register TRM while it is not guaranteed that the value before entering DeepSleep mode is still readable from the register.

- SARADC: PASSx_SARy_CHz_RESULT
- SRSS: PWR_LVD_STATUS
- SRSS: PWR_LVD_STATUS2
- SRSS: CLK_CAL_CNT1
- SRSS: CLK_CAL_CNT2
- SRSS: CLK_FLL_STATUS
- SRSS: WDT_INTR
- SRSS: WDT_INTR_MASKED
- SRSS: CLK_PLL400Mx_STATUS (not for CYT2B6/7/9/L)
- MIXER: MIXER_DST_STRUCT_INTR_DST_MASKED (only for cluster devices)

Parameters affected

N/A

Trigger condition(s)

Use of the related function and wakeup from DeepSleep mode.

Scope of impact

The values before entering DeepSleep are not retained.

Workaround

For PASSx_SARy_CHz_RESULT, any of the following:

1. Store the conversion values at another memory location before entering DeepSleep mode
2. Restart the conversion after wakeup from DeepSleep mode

For the other registers:

- Rewrite the register value or read the status flags again after wakeup

Fix status

No silicon fix planned. Register TRM was updated.

2.17 [204]SCBx_INTR_TX.UNDERFLOW bit may be set unintentionally

Description

There is possibility of setting the SCBx_INTR_TX.UNDERFLOW bit even if the FIFO is not empty.

Parameters affected

N/A

Trigger condition(s)

Using the TX FIFO for SCB when the AHB-Lite interface clock (CLK_GR6) frequency of the AHB bus is greater than 3x the SCB functionality clock (PCLK_SCBx_CLOCK).

Scope of impact

SCBx_INTR_TX.UNDERFLOW bit may be set unintentionally.

Workaround

Ignore the SCBx_INTR_TX.UNDERFLOW bit if the FIFO is not empty.

Fix status

No silicon fix planned. Register TRM was updated.

2.18 [206] Hardfault may occur when the SROM APIs listed below while executing EraseSector or ProgramRow in non-blocking mode

Description

The following SROM APIs read data from bank#0 (or bank#1 if dual bank mode with mapping B is used) in SFlash. While doing that the check for active non-blocking erase or program of bank#0 (or bank#1 if dual bank mode with mapping B is used) is not performed. Therefore, reading bank#0 (or bank#1 if dual bank mode with mapping B is used) while there is an active erase/program operation triggers a bus error. This results in a hardfault occurrence based on FLASHC_FLASH_CTL register settings.

Affected SROM APIs:

- ReadSWPU
- WriteSWPU
- GenerateHash
- Checksum[3)]
- ComputeBasicHash[3)]
- CheckFactoryHash
- ProgramWorkFlash[4)]
- SwitchOverRegulators (not for CYT2B6/7/9/L, CYT2CL)
- LoadRegulatorsTrims (not for CYT2B6/7/9/L, CYT2CL)

Parameters affected

N/A

Trigger condition(s)

Calling the affected SROM APIs while executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used).

Scope of Impact

The affected SROM APIs cannot be used while executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used).

Workaround

Do not use the affected SROM APIs while executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used).

Fix status

No silicon fix planned.

The architecture technical reference manuals were updated:

- 002-19314 Rev. *J for body controller entry family
- 002-24401 Rev. *H for body controller high family
- 002-33175 Rev. *D for cluster entry family
- 002-25800 Rev. *F for cluster 2D family

Impact on Infineon software

Impact: Limitation

3 Do not call it to calculate on the bank where programming/erasing is in progress
4 Do not use it during non-blocking operation

Related modules: S-LLD, HSM-Perf-Lib

Comment: While executing EraseSector or ProgramRow in non-blocking mode on bank#0 (or bank#1 if dual bank mode with mapping B is used), users must not do anything of following:

1. Call CySldProt_GetSwpuFlashStructCfg
2. Call CySldProt_VerifySecureDomainFlashWriteProtection if CySldProt_SwpuFlashStructGroupConfigurations is non-empty

2.19 [208]FPD-Link shall be used only with PLL400#4 in integer mode and SSCG disabled

Description

FPD-Link timing parameters cannot be guaranteed if the used PLL400#4 is not set to integer mode.

Parameters affected

SID880 to SID922

Trigger condition(s)

Use of FPD-Link with PLL400#4.

Scope of impact

FPD-Link can only be used with PLL400#4 in integer mode

Workaround

Disable SSCG and fractional divider on PLL400#4 when FPD-Link is used as display output on Display#0 root clock (CLK_HF11) and/or Display#1 root clock (CLK_HF12).

***Note**: Other PLL400 instances cannot be used for Display root clocks.*

Fix status

No silicon fix planned. Datasheet was updated.

Impact on Infineon software

Customers of VGFX-DRV using display signal output via FPD-Link should apply the suggested workaround. The McuSscgPllModulationEnable and McuSscgPllFractionalDivisionEnable settings of the MCAL module can be used to disable SSCG and fractional divider.

2.20 [209] CAN FD sporadic data corruption (payload) in case acceptance filtering is not finished before reception of data R3 (DB7..DB4) is completed

Description

During frame reception the Rx Handler accesses the external Message RAM for acceptance filtering (read accesses) and for storing of the accepted messages (write accesses).

The time needed for acceptance filtering and for storing of a received message depends on

- the Host clock frequency
- the worst-case latency of the read and write accesses to the external Message RAM

2 Functional deviations

- the number of configured filter elements
- the workload of the transmit message (Tx) handler in parallel to the receive message (Rx) handler

Received data bytes (DB0..DBm) from the CAN Core are buffered in the cache of the Rx Handler before they are written to the Message RAM (in words of 4 byte). Data words inside the Message RAM are numbered from R2 to Rn (n ≤ 17).

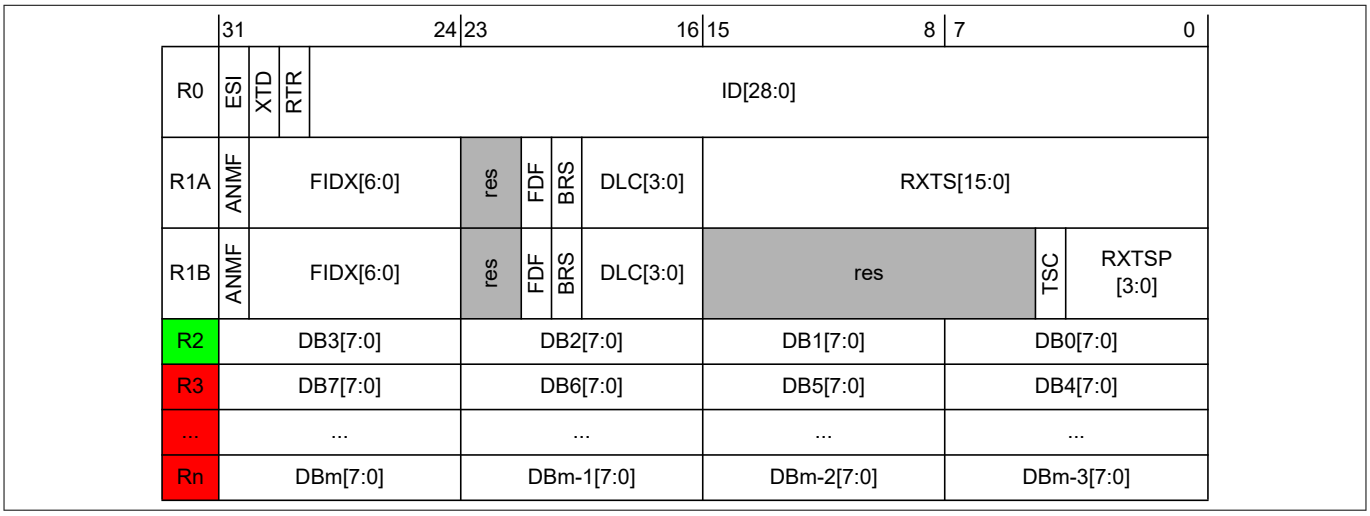


Figure 1 Rx Buffer and FIFO Element

Under the following conditions a received message will have corrupted data while the received message is signaled as valid to the host.

1. The data length code (DLC) of the received Message is greater than 4 (DLC > 4)
2. The storage of Ri of a received message into the Message RAM (after acceptance filtering is done) has not completed before R(i+1) is transferred from the CAN Core into the cache of the Rx Handler (where 2 ≤ i ≤ 5)
3. While condition 1 and 2 apply, a concurrent read of data word Ri from the cache and write of data word R(i+1) into the cache of the Rx handler happens

The data will be corrupted in a way, that in the Message RAM R(i+1) has the same content as Ri.

Despite the corrupted data, the M_TTCAN signals the storage of a valid frame in the Message RAM:

- Rx FIFO: FIFO put index RXFnS.FnPI is updated
- Dedicated Rx Buffer: New Data flag NDATn.NDxx is set
- Interrupt flag IR.MRAF is not set

The issue may occur in FD Frame Format as well as in Classic Frame Format.

Figure 2 shows how the available time for acceptance filtering and storage is reduced.

2 Functional deviations

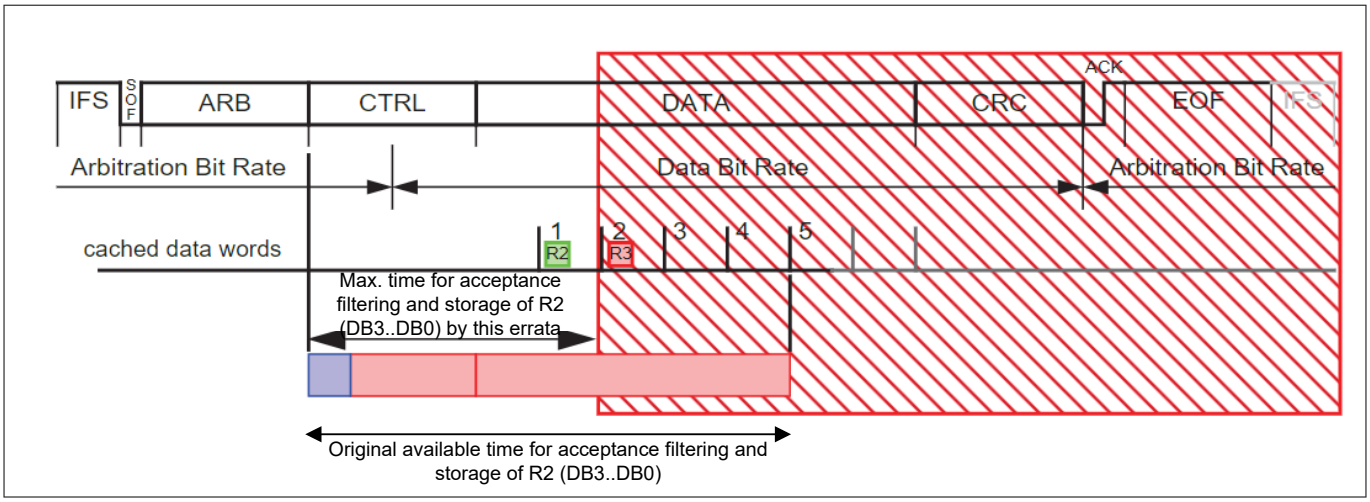


Figure 2 CAN frame with DLC > 4

Table 2 TRAVEO™ T2G: Minimum host clock frequency for CAN FD when DLC = 5

Number of configured active filter element 11-bit IDs/29-bit IDs[1) 2)]	Number of active CAN channels in an instance[3)]	Arbitration bit rate = 0.5 Mbps				Arbitration bit rate = 1 Mbps			
		Data bit rate = 0.5 Mbps	Data bit rate = 1 Mbps	Data bit rate = 2 Mbps	Data bit rate = 4 Mbps	Data bit rate = 1 Mbps	Data bit rate = 2 Mbps	Data bit rate = 4 Mbps	Data bit rate = 5 Mbps
32/16	2	3.9 MHz	7.1 MHz	13.1 MHz	22.8 MHz	7.7 MHz	14.1 MHz	26.1 MHz	31.5 MHz
	3	5.4 MHz	9.9 MHz	18.3 MHz	31.8 MHz	10.7 MHz	19.7 MHz	36.5 MHz	44.0 MHz
	4	6.9 MHz	12.7 MHz	23.5 MHz	40.8 MHz	13.8 MHz	25.3 MHz	46.9 MHz	56.5 MHz
	5	8.4 MHz	15.5 MHz	28.6 MHz	49.9 MHz	16.8 MHz	30.9 MHz	57.2 MHz	69.0 MHz
64/32	2	7.4 MHz	13.5 MHz	24.9 MHz	43.4 MHz	14.7 MHz	26.9 MHz	49.8 MHz	60.0 MHz
	3	10.3 MHz	18.8 MHz	34.9 MHz	60.7 MHz	20.5 MHz	37.6 MHz	69.7 MHz	84.0 MHz[4)]
	4	13.2 MHz	24.2 MHz	44.8 MHz	78.0 MHz	26.3 MHz	48.4 MHz	89.5 MHz[4)]	107.9 MHz[5)]
	5	16.1 MHz	29.6 MHz	54.7 MHz	95.3 MHz[4)]	32.1 MHz	59.1 MHz	109.4 MHz[5)]	131.8 MHz[5)]
96/48	2	10. 8 MHz	19.9 MHz	36.8 MHz	64.0 MHz	21.6 MHz	39.7 MHz	73.5 MHz	88.6 MHz[4)]
	3	15.1 MHz	27.8 MHz	51.5 MHz	89.6 MHz[4)]	30.2 MHz	55.6 MHz	102.9 MHz[5)]	124.0 MHz[5)]
	4	19.4 MHz	35.7 MHz	66.1 MHz	115.1 MHz[5)]	38.8 MHz	71.4 MHz	132.2 MHz[5)]	159.3 MHz[5)]
	5	23.7 MHz	43.6 MHz	80.8 MHz[4)]	140.7 MHz[5)]	47.4 MHz	87.2 MHz[4)]	161.5 MHz[5)]	194.7 MHz[5)]
128/64	2	14.3 MHz	26.3 MHz	48.6 MHz	84.7 MHz[4)]	28.4 MHz	52.5 MHz	97.2 MHz[4)]	117.2 MHz[5)]

(table continues...)

Table 2 (continued) TRAVEO™ T2G: Minimum host clock frequency for CAN FD when DLC = 5

Number of configured active filter element 11-bit IDs/29-bit IDs[1) 2)]	Number of active CAN channels in an instance [3)]	Arbitration bit rate = 0.5 Mbps				Arbitration bit rate = 1 Mbps			
		Data bit rate = 0.5 Mbps	Data bit rate = 1 Mbps	Data bit rate = 2 Mbps	Data bit rate = 4 Mbps	Data bit rate = 1 Mbps	Data bit rate = 2 Mbps	Data bit rate = 4 Mbps	Data bit rate = 5 Mbps
	3	20.0 MHz	36.8 MHz	68.0 MHz	118.5 MHz[5)]	40.0 MHz	73.5 MHz	136.0 MHz[5)]	164.0 MHz[5)]
	4	25.7 MHz	47.2 MHz	87.5 MHz[4)]	152.3 MHz[5)]	51.4 MHz	94.4 MHz[4)]	174.9 MHz[5)]	210.8 MHz[5)]
	5	31.4 MHz	57.7 MHz	106.9 MHz[5)]	186.1 MHz[5)]	62.7 MHz	115.4 MHz[5)]	213.7 MHz[5)]	257.5 MHz[5)]

1) M_TTCAN starts always at filter element #0 and proceeds through the filter list to find a matching element. Acceptance filtering stops at the first matching element and the following filter elements are not evaluated for this message. Therefore, the sequence of configured filter elements has a significant impact on the performance of the filtering process.
2) Acceptance filtering search for 11-bit IDs and 29-bit IDs filter element is running separately, only one configured filter setting should be considered. Searching for one 29-bit filter element requires approximately double cycles for one 11-bit filter element.
3) See the device datasheet for the supported number of channels
4) Frequency is not reachable since the maximum host clock frequency for M_TTCAN in CYT2B6 is 80 MHz
5) Frequency is not reachable since the maximum host clock frequency for M_TTCAN in all TRAVEO™ T2G is 100 MHz

Parameters Affected

N/A

Trigger condition(s)

Under the following conditions a received message will have corrupted data while the received message is signaled as valid to the host.

1. The data length code (DLC) of the received Message is greater than 4 (DLC > 4)
2. The storage of Ri of a received message into the Message RAM (after acceptance filtering is done) has not completed before R(i+1) is transferred from the CAN Core into the cache of the Rx Handler (where 2 ≤ i ≤ 5)
3. While condition 1 and 2 apply, a concurrent read of data word Ri from the cache and write of data word R(i+1) into the cache of the Rx handler happens

Scope of impact

The erratum is limited to the case when the Host clock frequency used in the actual device is below the limit shown in Table 2.

Corrupted data is written to the Rx FIFO element respective the dedicated Rx Buffer.

The received frame is nevertheless signaled as valid.

Workaround

Check whether the minimum Host clock frequency, that is shown in Table 2, is below the Host clock frequency used in the actual device.

If yes, there is no problem with the selected configuration.

If no, use one of the following two workarounds.

<First workaround>

Try different configuration by changing the following parameters until the actual host clock frequency (CLK_GR5) is above the minimum host frequency shown in Table 2.

- Increase the CLK_GR5 frequency in the actual device
- Reduce the CAN-FD Data Bit rate
- Reduce the number of configured filter elements
- Reduce the number of active CAN channels in an instance

Also, use DLC>=8 instead of DLCs 5, 6, and 7 in the CAN Environment/System, as they place higher demands on the minimum Host clock frequency (the worst case is DLC=5) or restrict your CAN Environment/System to DLC 4.

Note: While changing the actual host clock frequency, CLK_GR5 must always be equal or higher than PCLK_CANFD[x]_CLOCK_CAN[y] for all configurations.

<Second workaround>

Due to condition 3 the issue occurs only sporadically. Use an end-to-end (E2E) protection (for example, checksum or CRC covering the data field) and add it to all messages in the CAN system, to detect data corruption in received frames.

Fix status

No silicon fix planned. Use workaround.

Impact on Infineon software

Impact: Limitation

Related modules: CAN, MCU

Comment: The user must evaluate the impact of the erratum for each CAN instance separately. A CAN instance is the entirety of CanControllers with the same CanControllerInstance value.

1. For the number of active CAN nodes: Use the maximum number of CanController configurations of a CAN instance that can be active (Autosar controller state STARTED or SLEEP) at a time
2. For the host clock frequency: In McuPeriGroupSettings locate the setting with McuPeriGroup=MCU_PERI_GROUP5_MMIO5 and take the value from McuPeriGroupClockFrequency
3. For the number of configured active filter element 11-bit IDs/29-bit IDs: Use the corresponding values from the “Message RAM (…) linking table” in the generated Can_PBcfg.h file. Note that each CanController has its separate table. Take the maximum values.
4. For the Arbitration bit rate: Use the maximum CanControllerBaudRate value of all the CanControllers
5. For the Data bit rate: Use the maximum CanControllerFdBaudRate value of all the CanControllers if configured. Otherwise use CanControllerBaudRate.

2.21 [210]Added definition of minimum input slew rate for SPI-SDR and SPI-DDR of SMIF

Description

The minimum input slew rate of SPI-SDR and SPI-DDR mode of the serial memory interface were not defined which could cause malfunction of the transactions.

Parameters affected

Following parameters have been added:

- For CYT2CL
  - SPI-SDR: SID1614 = min 1.03 V/ns
  - SPI-DDR: SID1714 = min 1.03 V/ns

- For CYT3DL
  - SPI-SDR: SID1613 = min 0.7 V/ns
  - SPI-DDR: SID1713 = min 0.7 V/ns
- For CYT4DN and CYT4EN
  - SPI-SDR: SID1612 = min 1.125 V/ns
  - SPI-DDR: SID1712 = min 1.125 V/ns

Trigger condition(s)

Using SPI-SDR and SPI-DDR mode of the serial memory interface

Scope of impact

If the minimum input slew rate is not fulfilled, SMIF could cause malfunction of the transactions.

Workaround

The minimum input slew needs to be fulfilled for reliable operation.

Fix status

No silicon fix planned. Datasheet was updated.

Impact on Infineon software

Impact: No
Related modules: None
Comment: Software in scope does not support SMIF.

2.22 [211]Update of root and intermediate clocks table in datasheet

Description

Datasheet table 26-19 for root and intermediate clocks had some typos.

Parameters affected

Table 3 Root and intermediate clocks for CYT3DL

Root clock	Maximum permitted clock frequency (MHz)	Source	Maximum permitted clock frequency (MHz)					
			PLL/FLL Clock source: ECO/LPECO			PLL/FLL Clock source: IMO		
			Integer	SSCG	Fractional	Integer	SSCG	Fractional
CLK_HF8/ CLK_HF9	266	PLL400#1	200	~~196~~ N/A	~~198~~ N/A	191	~~187~~ N/A	~~189~~ N/A
		PLL400#2	266	~~260~~ N/A	~~263~~ N/A	254	~~249~~ N/A	~~252~~ N/A

Table 4 Root and intermediate clocks for CYT4DN

Root clock	Maximum permitted clock frequency (MHz)	Source	Maximum permitted clock frequency (MHz)					
			PLL/FLL Clock source: ECO/LPECO			PLL/FLL Clock source: IMO		
			Integer	SSCG	Fractional	Integer	SSCG	Fractional
CLK_HF8/ CLK_HF9	~~370~~ 333	PLL400#1	333	~~326~~ N/A	~~329~~ N/A	318	~~312~~ N/A	~~315~~ N/A
		PLL400#2	333	~~362~~ N/A	~~366~~ N/A	318	~~312~~ N/A	~~315~~ N/A

Table 5 Root and intermediate clocks for CYT4EN

Root clock	Maximum permitted clock frequency (MHz)	Source	Maximum permitted clock frequency (MHz)					
			PLL/FLL Clock source: ECO/LPECO			PLL/FLL Clock source: IMO		
			Integer	SSCG	Fractional	Integer	SSCG	Fractional
CLK_HF4	~~100~~ 50	FLL	~~100~~ 50	N/A	N/A	48	N/A	N/A
CLK_HF10	271	PLL400#3	271	266	~~366~~ 268	259	254	257
CLK_HF8/ CLK_HF9	~~370~~ 333	PLL400#1	~~370~~ 333	~~362~~ N/A	~~366~~ N/A	~~354~~ 318	~~347~~ N/A	~~350~~ N/A
		PLL400#2	~~370~~ 333	~~362~~ N/A	~~366~~ N/A	~~354~~ 318	~~347~~ N/A	~~350~~ N/A

Trigger condition(s)

Using these clocks and clock sources.

Scope of impact

Reduced frequency under these conditions

Workaround

Follow these maximum permitted clock frequencies

Fix status

No silicon fix planned. Datasheet was updated.

Impact on Infineon software

Impact: Limitation

Related modules: MCU

Comment: The user must verify that clock settings do not exceed the specified maximum. The value shown in McuClockRootSettings/McuClockRootFrequency must be less than or equal to the maximum permitted root clock. The value shown in McuClockPathSettings/McuClockPathFrequency must be less than or equal to the maximum permitted PLL/FLL clock. MCAL resource property files will be updated so that the validity check of McuClockRootFrequency works correctly.

2.23 [212] Description for PASS SARx to TCPWMx direct connect triggers one-to-one is incorrect in datasheet

Description

The body controller device's datasheet showed ‘trig=2’ in the description for PASS SARx to TCPWMx direct connect triggers one-to-one, which was incorrect as TCPWM’s input trigger selection (TR_IN_SEL) value. The correct value is ‘4’ as shown in the architecture TRM chapter 25 descriptions and table 25-2.

The cluster device's datasheet showed ‘trig=0’ in the description for PASS SARx to TCPWMx direct connect triggers one-to-one, which was incorrect as TCPWM’s input trigger selection (TR_IN_SEL) value. The correct value is ‘2’. Therefore, the correct description and table 25-2 in the architecture TRM chapter 25 are as follows.

Table 25-2 shows how the multiplexer should be handled for the input trigger event generation. The TRAVEO™ T2G Cluster MCU supports the following input triggers:

- Number of specific one-to-one trigger inputs: 1
- Number of general-purpose trigger inputs: 60

Table 6 Handling input trigger multiplexers for cluster devices

Input trigger selection	Input trigger	Input trigger source
0	Constant ‘0’	Constant ‘0’
1	Constant ‘1’	Constant ‘1’
2	HSIOM column ACT#2 or PASS (programmable analog subsystem), through 1:1 trigger mux #2	Refer to the "Alternate function pin assignments" or "Triggers one-to-one" section in the device datasheet
3	tr_all_cnt_in[0]	Refer to the trigger mux block in the device datasheet
:	:	:
62	tr_all_cnt_in[59]	Refer to the trigger mux block in the device datasheet

Parameters affected

N/A

Trigger condition(s)

Using the triggers one-to-one for PASS SARx to TCPWMx direct connect

Scope of impact

The triggers one-to-one for PASS SARx to TCPWMx direct connect cannot work if TCPWM’s input trigger selection is not correct.

Workaround

For body devices, use ‘4’ as TCPWM’s input trigger selection (TR_IN_SEL) value for PASS SARx to TCPWMx direct connect.

For cluster devices, use ‘2’ as TCPWM’s input trigger selection (TR_IN_SEL) value for PASS SARx to TCPWMx direct connect.

Fix status

No silicon fix planned. Datasheet was updated.

Impact on Infineon Software

Impact: No

Related modules: PWM

Comment: MCAL PWM module does not support one-to-one triggers.

2.24 [218]Greater change of one Low voltage detection (LVD) level can issue an Over voltage detection (OVD) reset or another LVD interrupt

Description

OVD and LVD1/2 share the common resistor ladder for reference voltages. Therefore, greater change of one LVD level can cause greater voltage fluctuation at OVD/another LVD reference voltage leading to OVD reset or another LVD interrupt.

Parameter affected

N/A

Trigger condition(s)

Change of LVD trip selection bits (PWR_LVD_CTL/2.HVLVD1/2_TRIPSEL_HT) by a step width of more than 1 at V_{DDD} > 4.5 V.

Scope of impact

Greater change of one LVD level can result in an OVD reset or another LVD interrupt.

Workaround

Any of the following

1. Do not change LVD trip selection bits (PWR_LVD_CTL/2.HVLVD1/2_TRIPSEL_HT) from default setting 0.
2. Increment LVD trip selection bits (PWR_LVD_CTL/2.HVLVD1/2_TRIPSEL_HT) by a step width of 1 per 10 µs. Change LVD1 or LVD2 independently, not at the same time.

Fix status

No silicon fix planned. Use workaround.

The architecture technical reference manuals were updated:

- 002-19314 Rev. *J for body controller entry family
- 002-24401 Rev. *H for body controller high family
- 002-33175 Rev. *D for cluster entry family
- 002-25800 Rev. *F for cluster 2D family

Impact on Infineon software

Impact: Limitation

Related modules: MCU

Comment: Workaround (2) was implemented in MCAL MCU driver version 1.24. Users of older versions can apply one of the suggested workarounds in following ways: Leave McuHvLvdThreshold at its default value of MCU_HVLVD_THRESHOLD_2_8V_TO_2_825V, or apply MCU configurations with changes of McuHvLvdThreshold in steps of 0.1V only.

2.25 [226]SCB transition times in SPI mode clarified

Description

SCB specification of transition time in SPI mode was meant to specify the input transition time only, but the description did not state this. The specified maximum transition time is not valid for signal output. The specification items have been split into input and output direction now.

Parameters affected

Following parameters have been updated:

Table 7 SCB transition timing

Spec ID	Description	Min	Typ	Max	Units	Details/ Conditions
SID129_2	SCB input transition in SPI mode	-	-	4	ns	
SID129_3	SCB output transition in SPI mode	-	-	10	ns	Valid for HSIO_STD(LN)
SID129_4	SCB output transition in SPI mode	-	-	20	ns	Valid for GPIO_STD, GPIO_ENH, GPIO_SMC

Trigger condition(s)

Use of SPI mode in SCB

Scope of impact

SCB specification of transition times in SPI mode has been split into input and output direction now..

Workaround

Use the SPI mode in SCB with these transition times.

Fix status

No silicon fix planned. Datasheet was updated.

Impact on Infineon software

Impact: No
Related modules: SPI
Comment: Transition time is a property of output signals which is not related to software

2.26 [229]System calls: improper usage of memory region end address in control logic

Description

Erroneous system calls execution status will be returned when passing parameters to system calls via SRAM region at the end of available SRAM.

Parameters affected

N/A

Trigger condition(s)

When SRAM_SCRATCH_DATA_ADDR for the following system calls end in the last available SRAM word:

- ProgramRow
- ProgramRow2 (only for CYT6BJ)
- ProgramWorkFlash
- ProgramWorkFlash2 (only for CYT6BJ)

Scope of impact

0xF0000013 (invalid arguments location) will be returned when passing parameters to system calls via SRAM region at the end of available SRAM.

Workaround

Do not use the last word of available SRAM for passing SRAM_SCRATCH_DATA_ADDR for the following system calls:

- ProgramRow
- ProgramRow2 (only for CYT6BJ)
- ProgramWorkFlash
- ProgramWorkFlash2 (only for CYT6BJ)

Fix status

No silicon fix planned. Use workaround.

Impact on Infineon software

Impact: Limitation

Related modules: FLS

Comment: Users of MCAL FLS must make sure that Fls_WriteData is not located immediately below the highest SRAM address. You can use memory mapping via FLS_START_SEC_VAR_NO_INIT_UNSPECIFIED and/or linker configuration to modify the location of the affected object.

2.27 [242]RTC busy status bit stuck issue

Description

RTC busy status flag (BACKUP_STATUS.RTC_BUSY register bit) is abnormally stuck at HIGH even after configuring the RTC user registers and BACKUP_RTC_RW.WRITE register bit is cleared by the software.

Parameter affected

N/A

Trigger condition(s)

RTC user register write operation randomly triggers this problem.

Scope of impact

RTC operation may not work as expected. If the software polls BACKUP_STATUS.RTC_BUSY flag before moving to any other tasks, it will be stuck there.

Workaround

Use the following software workaround:

1. If BACKUP_STATUS.RTC_BUSY flag is set, then run the following dummy write sequence
2. Start the sequence for maximum 8 retries (‘retryCount’) and start with 1
   - **a.** Write ‘1’ to BACKUP_RTC_RW.WRITE register for 'retryCount' times
   - **b.** Write ‘0’ to BACKIP_RTC_RW.WRITE register
   - **c.** Wait for 6 CLK_LF cycles (ILO0 or WCO)
   - **d.** If BACKUP_STATUS.RTC_BUSY flag is ‘0’, exit the loop
   - **e.** If ‘retryCount’ reaches to ‘8’, then handle this error according to user system requirement for failure case unrelated to this errata (e.g. write '1' to BACKUP_RESET.RESET register) else run dummy write sequence from “a”. Workaround for this errata needs to maximum 8 retries.

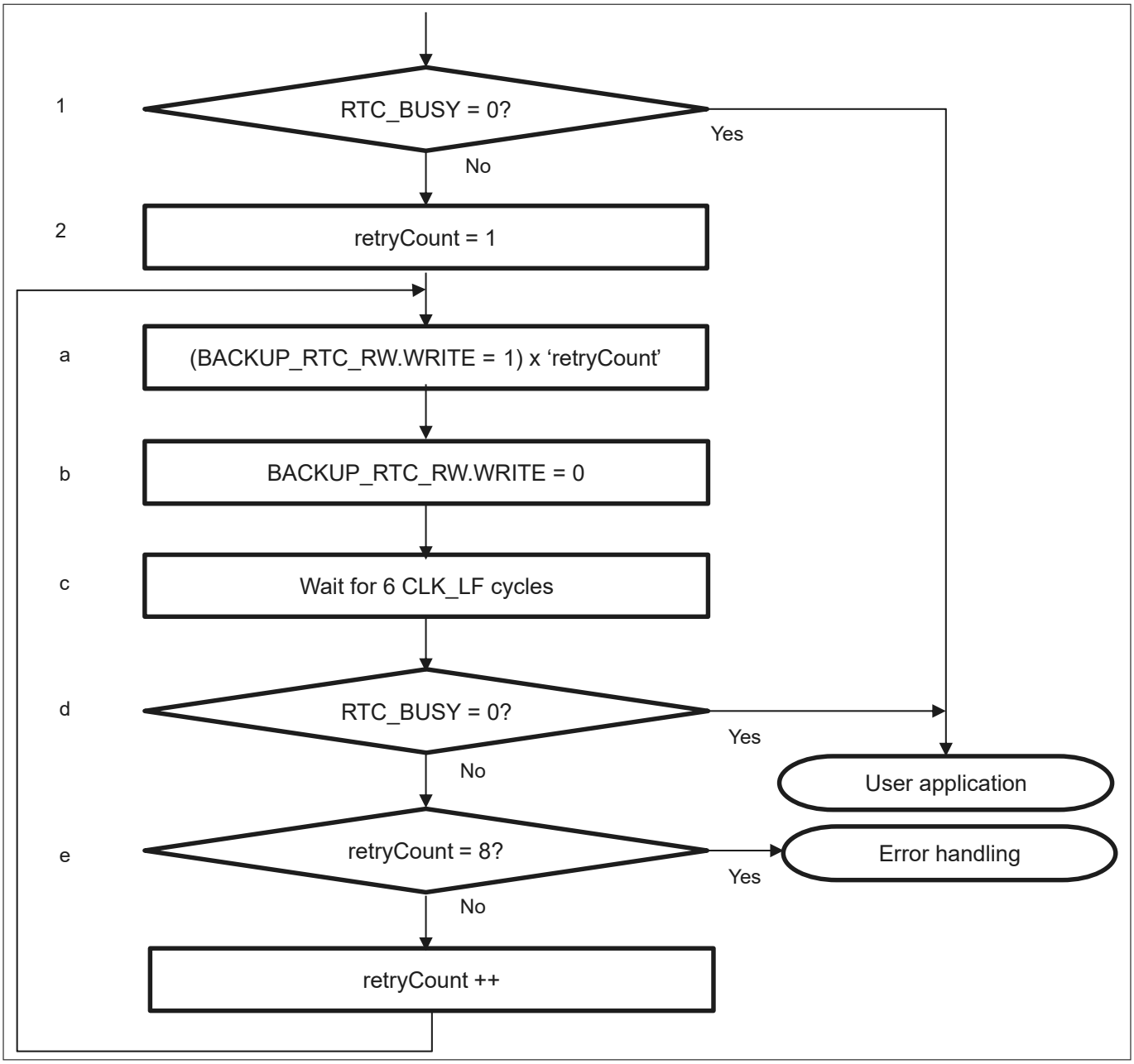


Figure 3 RTC software workaround

Fix status

No silicon fix planned. Use workaround.

Impact on Infineon software

Impact: None
Related modules: N/A
Comments: Software in scope does not access RTC registers.

2.28 [243]System calls: ProgramWorkFlash and ProgramWorkFlash2 do not operate as expected except for the Work Flash address with 32 bits alignment

Description

ProgramWorkFlash and ProgramWorkFlash2 (only for CYT6BJ) perform correct write operation only if the "Work flash address" argument passed to the ProgramWorkFlash/2 is aligned with "Data size" argument passed to the ProgramWorkFlash/2. Otherwise the ProgramWorkFlash/2 performs write operation to the unexpected Work flash area.

Parameters affected

N/A

Trigger condition(s)

If the "Work flash address" argument passed to the ProgramWorkFlash/2 is not aligned with "Data size" argument passed to the ProgramWorkFlash/2.

Scope of impact

This issue can perform write operation to the unexpected Work flash area.

Workaround

Use "Work flash address to be programmed" aligned with "Data size" argument.

[e.g., for Data size = 3 (64 bits) Work flash address must be aligned with 64 bits, for Data size = 4 (128 bits) Work flash address must be aligned with 128 bits, etc.]

For Data size = 2 (32 bits) the ProgramWorkFlash/2 works correct always.

Fix status

No silicon fix planned. Use workaround.

Impact on Infineon software

Impact: No

Related modules: MCAL FLS, FEE

Comment: FLS of MCAL uses ProgramRow, not ProgramWorkFlash or ProgramWorkFlash2. MCAL FLS in certain NRE services will use ProgramWorkFlash and contain a workaround for this erratum. FEE uses FLS to write to flash.

2.29 [244]WORK_INTERNAL_ERR bit can be set by a dummy read after work flash is erased/programmed

Description

1. When blocking mode is used for work flash erase/program, the dummy read is performed by the SROM API itself. However, the SROM API does not clear the WORK_INTERNAL_ERR bit in FLASHC_CM0_STATUS register or handle it even if it is set.
2. When non-blocking mode is used for work flash erase/program, the dummy read has to be done by user software. In this case, the WORK_INTERNAL_ERR bit can be set either on FLASHC_CM0_STATUS register or on FLASHC_CM4(or CM7_x)_STATUS register depending on which CPU first does the dummy read.

Parameter affected

N/A

Trigger condition(s)

A dummy read after work flash is erased/programmed

Scope of impact

WORK_INTERNAL_ERR bit handling needs to be done after a dummy read after work flash is erased/ programmed.

Workaround

- For problem 1, user software needs to clear the WORK_INTERNAL_ERR bit in FLASHC_CM0_STATUS register if it was set. If the first dummy read happened from CM4/CM7_x before the dummy read performed by the SROM API, then the WORK_INTERNAL_ERR bit may get set in FLASHC_CM4(or CM7_x)_STATUS register and user software needs to clear this bit.
- For problem 2, user software needs to clear the WORK_INTERNAL_ERR bit either on FLASHC_CM0_STATUS register or on FLASHC_CM4(or CM7_x)_STATUS register depending on which CPU first does the dummy read.

Fix status

No silicon fixed planned. Use workaround.

Impact on Infineon software

Impact: Limitation

Related modules: FLS

Comment: MCAL FLS clears the WORK_INTERNAL_ERR flag before activities that can cause the flag to indicate an error, and MCAL FLS checks and clears the flag after those activities. It may leave the flag active between API calls.

2.30 [245]CM7 power mode limitation

Description

When the power mode of CM7_x is changed to OFF, RESET, RETAINED by the CPUSS_CM7_x_PWR_CTL.PWR_MODE register, then the AXI infrastructure behavior can get undefined. This may corrupt transactions from CM7_x itself after its power mode is changed to ENABLED again, or transactions from other masters even while CM7_x is still in OFF, RESET, RETAINED power mode.

Parameter affected

N/A

Trigger condition(s)

Any of following:

1. Programming CPUSS_CM7_x_PWR_CTL.PWR_MODE register to RESET or OFF and not RETAINED while the CLK_MEM frequency is higher than 1/8 of the CLK_FAST_x frequency
2. Programming CPUSS_CM7_x_PWR_CTL.PWR_MODE register to RETAINED while the CLK_MEM frequency is higher than 1/12 of the CLK_FAST_x frequency

Scope of impact

This erratum affects all configurations of the Cortex®-M7 processor.

Workaround

1. In case of changing CPUSS_CM7_x_PWR_CTL.PWR_MODE = RESET or OFF and not RETAINED

   Before changing CPUSS_CM7_x_PWR_CTL.PWR_MODE = OFF | RESET, reduce the frequency of CLK_MEM to be lesser or equal to 1/8 of the frequency of CLK_FAST_x. Instead of directly writing the CPUSS_CM7_x_PWR_CTL register, the following sequence should be applied:

   a. Write CPUSS_MEM_CLOCK_CTL with a divider value to get 1/8 or less of the speed of CLK_FAST_x
   b. Set the desired power mode [OFF | RESET] in CPUSS_CM7_x_PWR_CTL.PWR_MODE
   c. Program original CPUSS_MEM_CLOCK_CTL settings, if desired
2. In case of changing CPUSS_CM7_x_PWR_CTL.PWR_MODE = RETAINED

   Before changing CPUSS_CM7_x_PWR_CTL.PWR_MODE = RETAINED, reduce the frequency of CLK_MEM to be lesser or equal to 1/12 of the frequency of CLK_FAST_x. Instead of directly writing the CPUSS_CM7_x_PWR_CTL register, the following sequence should be applied:

   a. Write CPUSS_MEM_CLOCK_CTL with a divider value to get 1/12 or less of the speed of CLK_FAST_x
   b. Set the desired power mode [RETAINED] in CPUSS_CM7_x_PWR_CTL.PWR_MODE
   c. Program original CPUSS_MEM_CLOCK_CTL settings, if desired

***Note**: If CPUSS_FAST_x_CLOCK_CTL.FRAC_DIV != 0, then the relevant divider for the CLK_FAST_x must be rounded up to the next higher integer. In this case, the CLK_FAST_x must be considered to be divided by (2+INT_DIV), since some clock periods may be 1 CLK_HFx cycle longer than other clock periods.*

Fix status

No silicon fix planned. Use workaround.

Impact on Infineon software

Impact: Limitation

Related modules: MCU

Comment: Users of the MCAL MCU module who turn off a powered-on CPU must implement the workaround. CPUs are powered off with McuMainCore0PowerMode ... McuMainCore3PowerMode set to MCU_POWERMODE_OFF. The memory clock divider value is configured with McuMemClockDivision.

2.31 [247]Open LVDS display interface (OpenLDI) non-standard balanced mode encoding

Description

OpenLDI balanced mode blanking signals (HSYNC/VSYNC) are not compliant with OpenLDI Spec v0.95.

Parameter affected

N/A

Trigger condition(s)

The Timing controller (TCON) of the Graphics subsystem is configured to drive the FPD-Link in OpenLDI balanced mode.

Specifically, the following register fields are set to these values:

- VIDEOSS0_TCON0/1_TCON_CTRL. ENLVDS = 1 (Enable LVDS , TTL and RSDS are disable, default value 0)

- VIDEOSS0_TCON0/1_TCON_CTRL. LVDSMODE = 0 (LVDS, default value 0)
- VIDEOSS0_TCON0/1_TCON_CTRL. LVDS_BALANCE = 1 (BALANCED, default value 1)

Scope of impact

Displays which require operation with OpenLDI balanced mode as well as explicit HSYNC and VSYNC framing does not work.

Workaround

Only OpenLDI unbalanced mode compatible displays can be used.

- VIDEOSS0_TCON0/1_TCON_CTRL. LVDS_BALANCE = 0 (UNBALANCED mode)

***Note**: Default value is 1 and needs to be changed to 0 by software*

Fix status

No silicon fix planned. Architecture TRM 002-25800 will be updated to mention that OpenLDI is only supported in unbalanced mode. Register TRMs will be updated to mark TCON_CTRL. LVDS_BALANCE=1 as not supported.

Impact on Infineon software

Impact: Limitation

Related modules: VGFX-DRV

Comment: TCON is configured via the CYGFX_DISP_TCON_PROPERTIES_S structure that is passed to CyGfx_DispOpenDisplay via the pTconProps element of the mode parameter.

2.32 [248]Potential failure of video capture stream

Description

Applications that use a video capture input from either MIPI or Parallel RGB capture may face undefined hardware state in very rare cases (e.g. hang-up of the capture control path) when certain features are used in combination.

Parameter affected

N/A

Trigger condition(s)

Following three conditions must be met to trigger the failure:

1. A cropping window with a non-zero size must be set (by CyGfx_CapSetCropWindow) for the capture input
2. The video processing block is dynamically enabled or bypassed
3. Internal condition must be hit, which depends on the clip window layout and memory access latency. This is not deterministic and cannot be controlled by the user.

The video processing block provides the features defined in cygfx_cm.h, including Filter, Scaler, CLUT, Color Matrix, and Histogram APIs. For Capture, the video processing block is bypassed by default. It is only enabled when the above features are required and the corresponding APIs are called. When these features are no longer needed, the block will be bypassed again.

Scope of impact

Usage for video capture input under specific conditions

Workaround

Application must avoid at least one of the two controllable trigger conditions by not using the related function.

Fix status

No silicon fix planned. A graphic driver update is planned for 2027 that implements a workaround.

Impact on Infineon software

Impact: Limitation

Related modules: VGFX-DRV

Comment: Cropping is configured with CyGfx_CapSetCropWindow. The Video Processing Block is dynamically enabled when the first of the features listed under Trigger Conditions is enabled after the start of capture. It is dynamically disabled when the last of these feature is disabled before the end of capture. This can be caused by a modification of the properties of the capture surface.

2.33 [260]PLL may not be locked in certain scenarios

Description

PLL may not be locked after wake-up from DeepSleep mode with trigger conditions.

Parameters affected

N/A

Trigger condition(s)

- Body High devices
  - Wakeup from DeepSleep with any of the following conditions
    - Using the external PMIC mode
      - The following conditions are met when entering DeepSleep mode
        - PLL is enabled
        - PWR_REGHC_CTL4.REGHC_PMIC_DPSLP = 0 & PWR_REGHC_CTL2.REGHC_EN = 1 (The power supply is switched to the internal regulator during DeepSleep, and PMIC control is handled by hardware)
        - PWR_REGHC_CTL.REGHC_PMIC_STATUS_WAIT register value > 00h
    - Using the external pass transistor mode
      - The following conditions are met entering DeepSleep mode
        - PLL is enabled
        - PWR_REGHC_CTL2.REGHC_EN = 1 (Pass transistor control is handled by hardware)
        - PWR_REGHC_CTL.REGHC_PMIC_STATUS_WAIT register value > 00h
- Cluster 2D or Graphic devices
  - Wakeup from DeepSleep with below conditions
    - Using the external PMIC mode
    - The following conditions are met when entering DeepSleep mode
      - PLL is enabled
      - PWR_PMIC_CTL4.PMIC_DPSLP = 0 & PWR_PMIC_CTL2.PMIC_EN = 1 (The power supply is switched to the internal regulator during DeepSleep, and PMIC control is handled by hardware)
      - PWR_PMIC_CTL.PMIC_STATUS_WAIT register value > 00h

Scope of impact

PLL may not be locked and the device works with reference clock of the PLL.

Workaround

Any of the following will work for all trigger conditions:

1. PWR_REGHC_CTL.REGHC_PMIC_STATUS_WAIT/PWR_PMIC_CTL.PMIC_STATUS_WAIT register value to be 00h
2. Restart PLL if PLL locked bit[5] remains 0 after wakeup

   The sequence for restarting PLL is as follows:

   a. Disable PLL by writing PLL enable bit[6] to 0
   b. Wait at least 2 IMO cycles (≥ 250 ns)
   c. Enable PLL by writing PLL enable bit[6] to 1
   d. Wait till PLL locked bit[5] becomes 1

Fix status

No silicon fix planned. Use workaround.

Impact on Infineon software

Impact: None

Related modules: MCU

Comment: PLL is enabled via the McuPllEnable configuration setting. PLL lock status can be retrieved with Mcu_GetPllStatus(). Current revisions of the software in scope do not support the REGHC and PMIC configuration. Revisions up to 1.19 of the MCU module supported the configuration of REGHC_PMIC_DPSLP/ PMIC_DPSLP and REGHC_EN/PMIC_EN via the McuRegHcEnable/McuPmicEnable and McuRegHcOnDeepSleepEnable/McuPmicOnDeepSleepEnable configuration settings, but did not modify REGHC_PMIC_STATUS_WAIT/PMIC_STATUS_WAIT.

2.34 [261]Ethernet interrupt status flag description of SW/HW access in Register TRM is incorrect

Description

The SW access and HW access flags of several Ethernet interrupt status registers are incorrect in the Register TRM.

Parameters affected

N/A

Trigger condition(s)

Use of following Interrupt status register flags:

- INT_STATUS [29], [27:18], [14:10], [7:0]
- INT_Q1_STATUS [11,7,6,5,2,1]
- INT_Q2_STATUS [11,7,6,5,2,1]
- RX_LPI [15:0]
- RX_LPI_TIME [23:0]

5 PLL200: CLK_PLL_STATUSx.LOCKED, PLL400: CLK_PLL400Mx_STATUS.LOCKED
6 PLL200: CLK_PLL_CONFIGx.ENABLE, PLL400: CLK_ PLL400Mx_CONFIG.ENABLE

- TX_LPI [15:0]
- TX_LPI_TIME [23:0]

Scope of impact

Register TRM does not describe the actual behavior of these bits.
Register TRM will be updated as follows:

- SW access changed from W1C to RW1C for
  - INT_STATUS [29], [27:18], [14:10], [7]
- SW access changed from R to RW1C for
  - INT_Q1_STATUS [11,7,6,5,2,1]
  - INT_Q2_STATUS [11,7,6,5,2,1]
- HW access changed from R to RW for
  - RX_LPI [15:0]
  - RX_LPI_TIME [23:0]
  - TX_LPI [15:0]
  - TX_LPI_TIME [23:0]
- The description of following register has been corrected by removing 'Cleared on read'
  - INT_STATUS [26:18], [14:10], [7:0]

Workaround

None. Follow the updated Register TRM.

Fix status

No silicon fix planned. Register TRM will be updated.

Impact on Infineon software

Impact: No
Related modules: None
Comment: Software in scope does not support the Ethernet.

2.35 [770]PLD might perform linefill to address that would generate a MemManage Fault (Arm® CM7 errata ID: 1013783)

Description

If the MPU is present and enabled, then it can be programmed so that loads to certain addresses generate a MemManage Fault.
This could be because:

- The address is unmapped, that is, it is not in an enabled region and the default memory map is not being used
- The address cannot be accessed at the current privilege level
- The address cannot be accessed at any privilege level

Because of this erratum, a PLD to such an address might incorrectly cause a data cache linefill.

Parameters affected

N/A

Trigger condition(s)

1. The data cache is enabled and the MPU is enabled
2. A PLD is executed, and either:
   a. The PLD is to an address not mapped in the MPU, which requires that:
      1. The MPU is enabled
      2. The default memory map is not being used
      3. The default memory map is cacheable at that address
      4. The PLD does not hit an enabled MPU region
   b. The PLD is to a region that has permission requirements that the PLD does not meet, which requires that:
      1. The MPU is enabled
      2. The default memory map is not being used
      3. The region that the PLD hits is cacheable
      4. The region that the PLD hits would generate a MemManage fault for a load. This requires either:
         a. The region cannot be accessed by a read at any privilege level
         b. The region only has read access for privileged code and the PLD is unprivileged

Note that in rare cases, a PLD instruction can be speculatively executed in the shadow of a mispredicted branch. This can even theoretically be a literal value that decodes to a PLD.

Scope of impact

Processor execution is not affected by this erratum. The data returned from the linefill is not directly consumed by the PLD. Any subsequent load to that address can only access the data if it has permissions to do so. This erratum does not permit software to access data that it does not have permissions for.

The only implications of this erratum are the access itself which should not have been performed. This might have an impact on memory regions with side-effects on reads or on memory which never returns a response on the bus.

Workaround

Accesses to memory that is not mapped in the MPU can be avoided by using MPU region 0 to cover all unmapped memory and make this region execute-never and inaccessible.

That is, MPU_RASR0 should be programmed with:

- MPU_RASR0.ENABLE = 1 ; MPU region 0 enable
- MPU_RASR0.SIZE = b11111 ; MPU region 0 size = 2^32 bytes to cover entire memory
- MPU_RASR0.SRD = b00000000 ; All sub-regions enabled
- MPU_RASR0.XN = 1; Execute-never to prevent instruction fetch
- MPU_RASR0.AP = b000; No read or write access for any privilege level
- MPU_RASR0.TEX = b000 ; Attributes = Strongly-ordered
- MPU_RASR0.C = b0 ; Attributes = Strongly-ordered
- MPU_RASR0.B = b0 ; Attributes = Strongly-ordered

Accesses to memory that is mapped in the MPU, but should not be accessed at the current privilege level can be avoided by making the region non-cacheable.

That is, MPU_RASR0 should be programmed with:

- MPU_RASR0.TEX = b000 ; Attributes = Strongly-ordered
- MPU_RASR0.C = b0 ; Attributes = Strongly-ordered
- MPU_RASR0.B = b0 ; Attributes = Strongly-ordered

Fix status

No silicon fix planned. Use workaround.

Impact on Infineon software

Impact: None

Related modules: N/A

Comment: This erratum would only have noticeable effects if a PLD targeted the address of an MMIO with side-effects on reading. Conditions of the erratum are not met for such addresses: they are not cacheable in the default memory map (condition 2.a.3) and any meaningful MPU configuration (condition 2.b.3).

2.36 [771]ECC error causes data corruption when the data cache error bank registers are locked (Arm® CM7 errata ID: 1267980)

Description

The data cache contains two error bank registers, DEBR0 and DEBR1. These registers store the locations in the cache that Error Correcting Code (ECC) errors affect and prevent future allocations to those locations.

Software can lock each DEBR and this prevents the DEBR from being automatically updated when a data cache ECC error is detected.

Because of this erratum, if both DEBR0 and DEBR1 are locked and an ECC error is detected on a cacheable store, then the store data is written onto the bus but not written into the data cache. This might result in the data cache containing stale data.

Parameters affected

N/A

Trigger condition(s)

- DEBR0 and DEBR1 are locked
- The wanted address has been allocated to the cache
- A cacheable store to the wanted address looks up in the cache, and an ECC error is found in the cache set that the store addresses

Scope of impact

This erratum can cause data corruption in the data cache.

Workaround

Software must avoid locking both error bank registers.

Fix status

No silicon fix planned. Use workaround.

Impact on Infineon software

Impact: Limitation

Related modules: N/A

Comment: Software in scope does not use CM7_SCS_DEBR0 and CM7_SCS_DEBR1. Other software must not lock (set bit #1 of) the CM7_SCS_DEBR0 and CM7_SCS_DEBR1 registers at the same time.

2.37 [772]Data corruption for load following Store-Exclusive (Arm® CM7 errata ID: 1315869)

Description

A load that follows a Store-Exclusive to the same address might forward data from an earlier store, situated between the Load-Exclusive and the Store-Exclusive, and not the data from the Store-Exclusive.

Parameter affected

N/A

Trigger condition(s)

The following sequence is required for this erratum to occur:

1. A load exclusive sets the local monitor
2. A store to the wanted address
3. Any of the following instructions to the wanted address. This instruction must not fail either the local or global monitor check
   a. STREXB
   b. STREXH
   c. STREX
4. A load to the wanted address

There must be at most one instruction between the Store-Exclusive and the load. All accesses must be to Shareable memory.

Scope of impact

Data corruption occurs when the load returns data from the older store instead of the newer Store- Exclusive.

Stores between a Load-Exclusive and Store-Exclusive are not expected in real code because such stores can always clear the local monitor in some implementations.

Workaround

No workaround is necessary.

Fix status

No silicon fix planned.

Impact on Infineon software

Impact: None

Related modules: N/A

Comment: Software in scope does not use exclusive load and store. Other software, if using exclusive load and store, can be affected.

2.38 [773]TCM bandwidth sharing between AHBS writes and software stores might not function correctly when using TCM wait states (Arm® CM7 errata ID: 2328489)

Description

The TCM Control Unit (TCU) contains a Store Queue (SQ) FIFO that buffers Tightly Coupled Memory (TCM) writes. Software stores and AHBS writes both go through the SQ. A round-robin scheme is used to fairly share

the SQ ingress bandwidth between software stores and AHBS writes when contention occurs. Due to this erratum, AHBS writes might take priority over 64-bit software stores, which can stall processor instruction execution while the AHBS writes are ongoing. Software stores take priority over AHBS writes and therefore this erratum does not occur when there is adequate TCM bandwidth available.

Parameters affected

N/A

Trigger condition(s)

This erratum can occur when either an STRD, STM, PUSH, VPUSH, VSTR.64, or VSTM instruction is executed targeting TCM during a long stream of back-to-back AHBS write transfers and TCM wait states are used.

Also, if a load instruction closely follows after a 64-bit store instruction to TCM that stalls the execution pipeline, then this will further exacerbate the issue. If the pipeline is stalled, the read will still go ahead but the data returned will be discarded. Hence, a TCM read will be repeated until the stall ends.

Scope of impact

This erratum only affects the performance of the Cortex®-M7 processor. It can cause the processor's execution pipeline to stall when executing a 64-bit store instruction while back-to-back AHBS writes are ongoing. When the AHBS back-to- back write stream ends, the 64-bit store will be accepted into the SQ and the pipeline will stop stalling.

Workaround

Do not modify CPUSS_CM7_x_CTL.ITCM_READ_WS and CPUSS_CM7_x_CTL.DTCM_READ_WS. By default, these registers are initialized to 0.

Fix status

No silicon fix planned. Use workaround.

Impact on Infineon software

Impact: Limitation

Related modules: N/A

Comment: The user must not modify CPUSS_CM7_x_CTL.ITCM_READ_WS and CPUSS_CM7_x_CTL.DTCM_READ_WS. By default, these registers are initialized to 0, so there are no TCM wait states and, hence, the erratum will not come into effect.

2.39 [774]Cortex®-M7 can halt in an incorrect address when breakpoint and exception occurs simultaneously (Arm® CM7 errata ID: 3092511)

Description

When an asynchronous exception occurs at the same time as a breakpoint event (either hardware breakpoint or software breakpoint), it is possible for the processor to halt at the beginning of the exception handler instead of the instruction address pointed by the breakpoint.

Parameters affected

N/A

Trigger condition(s)

The BKPT bit in Debug Fault Status Register (DFSR) is set, indicating that a breakpoint event has occurred. The return address of the exception is the breakpoint address. As a result, if the debugger clears the halting control bit in the processor at this point, the processor will reach the breakpoint again after servicing the exception.

The following conditions are required:

1. Halt mode debug is enabled and is permitted by debug authentication configuration
2. The processor reaches the breakpoint as the same time that the asynchronous exception is invoked

Scope of impact

A debugger connected to the Cortex®-M7 can detect the processor is halted after a breakpoint is hit, but might not be able to determine which breakpoint has triggered the halting.

Workaround

This issue only affect the debugger's operation. The debugger could report the halting reason as an unknown breakpoint, and optionally resume operation. If the processor's operation is resumed, it is likely to be halted again immediately after the interrupt is serviced and returns to the breakpoint address.

Fix status

No silicon fix planned.

Impact on Infineon software

Impact: None

Related modules: N/A

Comment: This erratum only affects debugging.

Revision history of CYT3DL errata sheet

Document version	Date of release	Description of changes
1.0	2021-07-13	Initial release
1.1	2021-07-20	Added errata ID 138, 139.
1.2	2021-09-16	Updated "Workaround" of errata ID 147. Added errata ID 167, 169.
1.3	2021-09-28	Updated the description of errata ID 158. Added errata ID 172.
1.4	2022-02-03	Updated “Fix Status” of errata ID 158, 164, 167, 169. Added errata ID 175, 176, 179.
1.5	2022-03-01	Added errata ID 183.
1.6	2022-06-15	Updated “Description” and “Fix Status” of errata ID 169. Updated “Description” and “Scope of Impact” of errata ID 179. Added errata ID 185, 186, 188 to 192, 196.
1.7	2022-07-15	Added errata ID 197.
1.8	2022-08-25	Updated "Description" of errata ID 185. Added errata ID 198, 199.
1.9	2022-12-07	Added errata ID 201, 202, 203, 204
2.0	2023-02-08	Updated "Description" of errata ID 203. Added errata ID 206.
2.1	2023-05-12	Updated errata ID 206 to add (or bank#1 if dual bank mode with mapping B is used). Added errata ID 208.
2.2	2023-06-15	Updated “Impact on Infineon Software” of errata ID 208. Added errata ID 209.
2.3	2023-10-17	Updated errata ID 206 to add the affected SROM APIs. Added errata ID 210, 211, 212.
2.4	2024-08-23	Added errata ID 218, 226.
2.5	2025-02-21	Added errata ID 229. Updated the “Impact on Infineon software” of errata ID 218. Removed errata ID 138, 139, 143, 145, 157, 158, 164, 169, 179, 183, 186, 188, 189, 190, 191, 192, 196, 197 because the datasheet was updated for errata ID 143, 145, 164, 169, 179, 183, 186, 188, 189, 190, 191, 192, 196, 197, and errata ID 138, 139, 157 and 158 were fixed before official release.
2.6	2025-03-28	Migrated to Infineon errata template. Consolidated the description for all affected devices (errata ID 137, 198, 203, 206, 209, 210, 211, 212).
2.7	2025-09-30	Removed "sometimes" from description of errata ID 229. Added errata ID 242 and 770 to 774.
2.8	2026-04-22	Updated the description of errata ID 218. Added errata ID 243 to 245. Consolidated the description for all affected devices (each errata ID 210, 211).
2.9	2026-06-08	Added errata ID 247, 248.
2.10	2026-07-16	Added errata ID 260, 261.
2.11	2026-07-28	Updated the workaround of errata ID 260 to change from 250 µs to 250 ns.
2.12	2026-08-27	Updated the "Impact on Infineon software" of errata ID 244.

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Edition 2026-08-27

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
IFX-gta1724911319557

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