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Chip Errata for the MB9DF120/MB9EF220 Series 32-bit ARM® Cortex®- R4 Microcontroller

This document describes the errata for the MB9DF120/MB9EF220 Series 32-bit ARM® Cortex® - R4 Microcontroller. Compare this document to the device's data sheet for a complete functional description.

Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number
MB9DF120/MB9EF220 Series

Description of Functional Limitation

The functional limitation was found with Flash memory implemented in the ARM® Cortex® R4 family. After issuing a Flash memory erase suspend command during Flash memory erase operation data of Flash memory may not be correctly readable even when the erase suspend state is reached. This functional limitation can only occur when erase suspend is used.

Affected Devices

ARM® Cortex ® - R4 family

Series	Product Name
MB9DF120 series	MB9DF125/F125E, MB9DF126
MB9EF220 series	MB9EF226

Conditions for Functional Limitation

The limitation may occur when all of following conditions are met:

- The sector erase suspend command is issued during sector erase.
- When a read command is issued to one of the sectors inside the Flash macro currently in sector erase suspend state.

Details of the Limitation

Data may not be read correctly irrespective of the large sectors or small sectors if the following operations are executed in sequence:

- The sector erase suspend command is issued to the flash memory during sector erase.
- After the state of the sector erase suspend is completed, the reading operation for the flash memory (instruction read or data read) is performed.

In this case the read data are undefined. After this read data will remain undefined until the sector erase resume command is issued. Combination of operating conditions for flash memories is the following table.

Table 1. Combination of operating conditions for Flash memories (ARM® Cortex® R4 family)

	Flash memory to which the sector erase suspend command is issued	Flash memory from which data is read	Read value of data in the sector erase suspend state
1	TC Flash-A	TC Flash-A	Undefined
2	TC Flash-B	TC Flash-B	Undefined
3	EE Flash	EE Flash	Undefined
4	TC Flash-A	TC Flash-B / EE Flash	Normal
5	TC Flash-B	TC Flash-A / EE	Normal
6	EE Flash	TC Flash-A / TC Flash-B	Normal

The cause of the limitation

The flash memory control circuit consists of the following two circuits:

- The circuit to control automatic algorithm execution for sector erase operation.
- The circuit, which receives the sector erase suspend command from the above mentioned circuit, to stop the automatic algorithm execution and to switch to the state where the read operation is enabled.

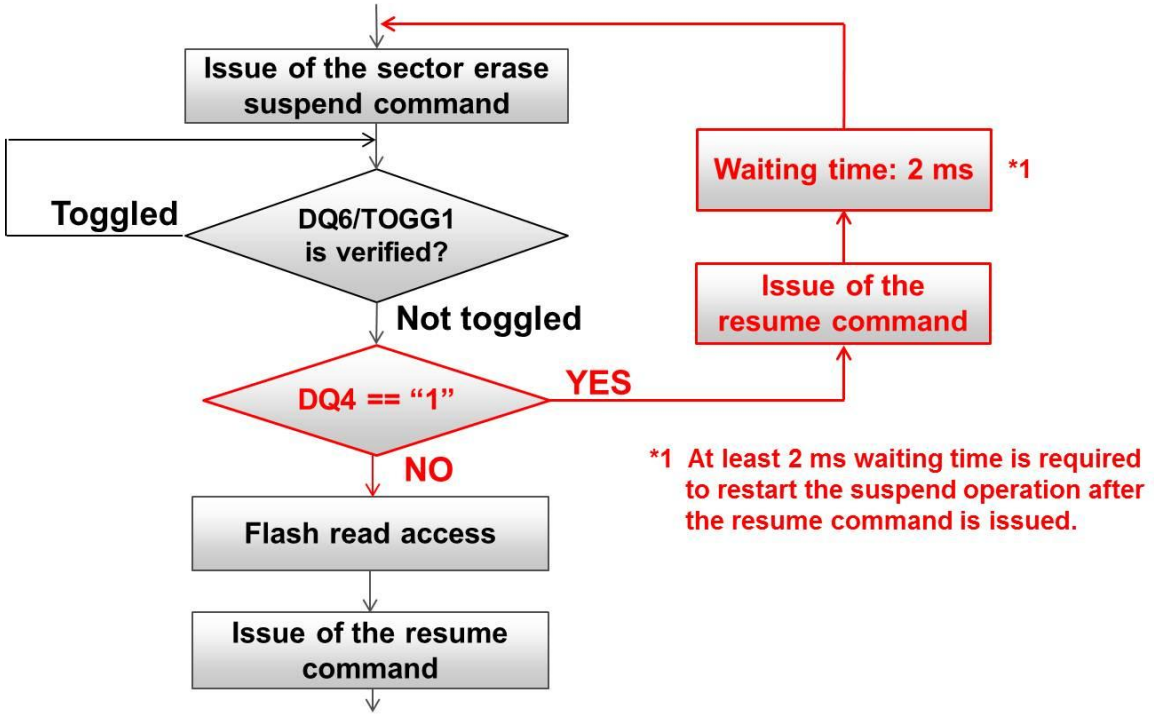
The limitation is caused by the circuitry changing the erase state to erase suspend state not allowing normal data read.

Workaround

To avoid this limitation, the following workaround by software is recommended.

After the flash sector erase suspend operation (issue of the suspend command + verification of DQ6/TOGG1 bit) is finished, check the hardware sequence flag DQ4 bit indicating the specific internal state which can read flash or not (see Figure 1).
If the value of DQ4 bit is "1"then issue the sector erase resume command and restart the sector erase suspend operation after the waiting time.

Figure 1. Workaround by software



Please note the following factors of internal circuit when using the software workaround:

- At least 2 ms waiting time is required to restart the sector erase suspend operation after the resume command is issued by DQ4 == "1" (see *1 in Figure 1).
- Approximately a maximum of 10 ms would be required for DQ4 to become "0" after the suspend command is issued first.

Though DQ4 is an undefined bit on the hardware manual, it can be used to read the internal sequence state. If DQ4 ==”0”, it indicates the internal state allowing data read/instruction fetch from flash. But if DQ4 ==”1”, internal circuit have not changed to the state allowing data read/instruction fetch. See the following table and figure representing bit assignment of DQ4 bit for FCR4 family and FR5 family, respectively.

Table 2. Bit assignment of hardware sequence flags (ARM® Cortex® R4 family)

Read data bit no.	7	6	5	4	3	2	1	0
Hardware sequence flag	DQ7	DQ6	DQ5	**DQ4**	DQ3	DQ2	-	-
Read data bit no.	15	14	13	12	11	10	9	8
Hardware sequence flag	DQ15	DQ14	DQ13	-	DQ11	DQ10	-	-

Note

The following software products (all releases) are not affected by this limitation, because they do not use erase suspend:

- FCR4MCAL(SW-MCAL31-DRV-FCR4-E01, SW-MCAL31-DRV-FCR4-E02, SW-MCAL40-DRV-FCR4-E01),
- FCR4 FEE/FLS (SW-FEEFLS-DRV-FCR4-E01, SW-FEE40-DRV-FCR4-E01)

Document History Page

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Rev.	**ECN No.**	**Orig. of Change**	**Description of Change**
**	_	NOFL	Initial release
*A	5229319	NOFL	Migrated to Cypress format

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