Errata Sheet

V1.0, 2007-09

Device	**C504-2E**
Marking/Step	**Step CC**
Package	**P-MQFP-44**

This Errata Sheet describes the deviations from the current user documentation.

The module oriented classification and numbering system uses an ascending sequence over several derivatives, including already solved deviations. So gaps inside this enumeration can occur.

Current Documentation

- C504 User's Manual 10.97
- C504 Data Sheet May 2000
- Instruction Set Manual 07.2000

Note: Devices marked with EES- or ES are engineering samples which may not be completely tested in all functional and electrical characteristics, therefore they should be used for evaluation only.

The specific test conditions for EES and ES are documented in a separate Status Sheet.

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1 History List/Change Summary

(since last CPU Step ES-CB/CB, previous Errata Sheet V1.3)

Table 1 Functional Deviations

Functional Deviation	Short Description	Fixed in Step	Change
EH.1	Emulation Mode not supported		
RST.1	Figure in User's Manual and Data Sheet regarding the Reset Circuitries is incorrect		
WDT.1	Watchdog Timer is not halted in the Idle Mode		
WDT.2	To refresh the Watchdog Timer, the WDT and SWDT bits in WDCON Register can not be set by using Immediate Addressing Mode instruction		
OTP.1	ROM Verification Mode 2 and verification error signaling at Port 3.5		

Table 2 AC/DC Deviations

AC/DC Deviation	Short Description	Fixed in Step	Change
AC.1	Minimum Oscillator Clock Frequency		
DC.1	± 4 LSB Total Unadjusted Error (TUE) of A/D Converter		
DC.3	Maximum value of -70 µA for the logic 0 input current (Ports 1,2,3)		
DC.5	Output low voltage (V_{OL}) of the output pin COUT3		
DC.6	± 6 LSB Total Unadjusted Error (TUE) of A/D Converter at 40 MHz		
DC.7	V_{DD} is valid for a smaller range than specified on documents		
DC.8	Minimum value of -3 µA for the logic 0 input current (Ports 1, 2, 3)		
DC.9	Maximum limit values of the power supply current (I_{DD})for Active Mode		

Table 2 AC/DC Deviations (cont'd)

AC/DC Deviation	Short Description	Fixed in Step	Change
DC.10	Maximum limit values of the power supply current (I_{DD})for Idle Mode		

Table 3 Application Hints

Application Hint	Short Description	Fixed in Step	Change
None.			

2 Functional Deviations

EH.1: Emulation Mode not supported

The “Enhanced Hooks Technology” Emulation Mode is not supported by the C504-2E.

Workaround:

None.

RST.1: Figure in User’s Manual and Data Sheet regarding the Reset Circuitries is incorrect

Figure 5-1 in User’s Manual and Figure 6 in Data Sheet show incorrectly that the RESET pin has an internal pullup resistor connected to the V_{DD}. Instead, at the RESET pin, an internal pulldown resistor is connected to the V_{SS}. The correct implementation is illustrated in **Figure 1**.

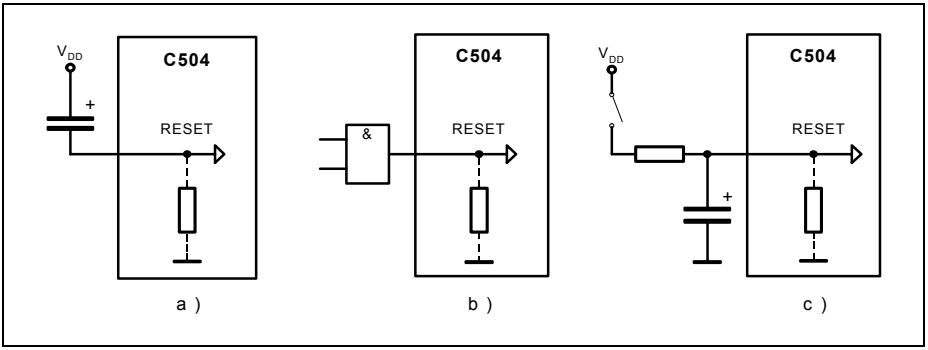

Figure 1 Reset Circuitries

This correction will be updated to the future versions of the User’s Manual and Data Sheet.

Workaround:

Not applicable

WDT.1: Watchdog Timer is not halted in Idle Mode

The Watchdog Timer (WDT) is not halted in the Idle Mode as defined. However, during the Idle Mode, an overflow condition of the WDT does not initiate an internal reset. In such a case, the WDT starts a new count sequence.

Workaround:

1. Do not use the Watchdog Timer function in combination with the Idle Mode
2. In case of WDT is running before entry into idle mode, to avoid a WDT initiated reset upon exit of the Idle Mode, the following methods can be used.

   a) The WDT is refreshed immediately upon exit from Idle Mode.
   b) A timed interrupt can be used to exit the Idle Mode before the WDT reaches the counter state 7FFCh. This can be achieved by using Timer 0, 1 or 2. This timer can be programmed to generate an interrupt at a WDT counter state prior to overflow, for e.g., at 7F00h. Prior to entering Idle Mode, the WDT can be refreshed and Timer 0, 1or 2 can be started immediately to synchronize the WDT. In the interrupt service routine of Timer 0, 1 or 2, the WDT must be refreshed. If required, Idle Mode could be entered again.

WDT.2: Setting WDT and SWDT bits in WDCON Register by using Immediate Addressing Mode instruction may not refresh the Watchdog Timer.

To initiate a refresh of the Watchdog Timer, the WDT bit should be set directly before the SWDT bit in WDCON register (WDCON.1 and WDCON.0). However, using the Immediate Addressing Mode instruction to set the WDT and SWDT bits may not refresh the Watchdog Timer, the Watchdog Timer may keep counting until overflow and reset the device.

For example:

```
MOV   WDCON, #02h
MOV   WDCON, #01h
```

These instructions will not refresh the Watchdog Timer.

Workaround:

Use the Bit Manipulation Instruction to set the WDT and SWDT bits.

For example:

```
SETB   WDCON.1
SETB   WDCON.0
```

OTP.1: ROM Verification Mode 2 and verification error signaling at Port 3.5

The last block of 16 bytes will always return verification error in the ROM Verification Mode 2.

Workaround:

None.

3 Deviations from Electrical- and Timing Specification

AC.1: Minimum Oscillator Clock Frequency

The minimum oscillator clock frequency $1/t_{CLCL}$ is increased to 4 MHz (instead of 3.5 MHz).

Workaround:

None.

DC.1: ± 4 LSB Total Unadjusted Error (TUE) of A/D Converter

The total unadjusted error of the A/D Converter does not meet the specified value of the DC characteristics. The value for TUE is limited as follows:

$TUE = \pm 4$ LSB in the V_{IN} range: $V_{SS} < V_{IN} < V_{CC}$

Workaround:

None.

DC.3: Maximum value of - 70 µA for the logic 0 input current (Ports 1, 2, 3)

The maximum value of the logic 0 input current for ports 1, 2, and 3 is higher than the specified value:

I_{IL} max = - 70 µA (instead of - 50 µA)

Workaround:

None.

DC.5: Output low voltage (V_{OL}) of the output pin COUT3

The maximum output low voltage of the output pin COUT3 (pin #28) is increased:

V_{OL}(max) = 0.7 V (instead of 0.45 V)

Workaround:

None.

DC.6: ± 6 LSB Total Unadjusted Error (TUE) of A/D Converter at 40 MHz

The total unadjusted error of the A/D Converter at 40 MHz operating frequency does not meet the specified value of the DC characteristics. The value for TUE is limited as follows:

TUE = ± 6 LSB in the V_{IN} range: $V_{SS} < V_{IN} < V_{CC}$ at 40 MHz

Workaround:

None.

DC.7: V_{DD} is valid for a smaller range than specified on documents

V_{DD} is valid in the range from 4.5 V to 5.5 V at all specified temperatures, instead of 4.25 V to 5.5 V as specified on the documents. This smaller range is effective on devices with step code starting from CB.

Workaround:

None.

DC.8: Minimum value of - 3 µA for the logic 0 input current (Ports 1, 2, 3)

The minimum value of the logic 0 input current for ports 1, 2, and 3 is lower than the specified value:

I_{IL} min. = - 3 µA (instead of - 10 µA)

Workaround:

None.

DC.9: Maximum limit values of the power supply current (I_{DD}) for Active Mode

The maximum limit values of the power supply current (I_{DD}) for Active Mode are shown in the table below, instead of the specified values stated in the Data Sheet.

Power Supply Current

Parameter			Symbol	Maximum Limit Values	Unit
Active Mode	C504-2E	24 MHz	I_{DD}	32.11	mA
		40 MHz	I_{DD}	49.87	mA

Workaround:

None.

DC.10: Maximum limit values of the power supply current (I_{DD}) for Idle Mode

The maximum limit values of the power supply current (I_{DD}) for Idle Mode are shown in the table below, instead of the specified values stated in the Data Sheet.

Power Supply Current

Parameter			Symbol	Maximum Limit Values	Unit
Idle Mode	C504-2E	24 MHz	I_{DD}	19.02	mA
		40 MHz	I_{DD}	27.79	mA

Workaround:

None.

4 Application Hints

No application hints for this step.