Power filter options for the FPD-Link interfaces in TRAVEO™ T2G family

Associated part family

- CYT3D series
- CYT4D series

About this document

Scope and purpose

A number of Infineon TRAVEO™ T2G cluster 2D series microcontrollers include a flat panel display link (FPD-Link) interface to drive LCD or similar flat-panel displays. To ensure that the interface meets its stringent timing and jitter requirements, power supplies for the associated LVDS drivers and PLL supply must be isolated and properly conditioned. This application note describes various conditioning options based on a mix of use cases.

Intended audience

This document is intended for anyone using TRAVEO™ T2G family CYT3D/CYT4D series MCUs.

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1 Introduction

TRAVEO™ T2G cluster 2D series of automotive MCUs contain integrated graphics controllers for driving flat-panel displays. One of the supported display interfaces, known as FPD-Link, sends the digital display data serially across three or four low-voltage differential signaling (LVDS) communication links, along with a separate LVDS clock signal (TXCLK±).

To ensure interoperability with a wide range of LCD and other flat-panel displays, this FPD-Link interface must meet stringent limits on the jitter present in the output clock. This application note documents different use cases and associated filter options to limit the propagation of noise from the external LVDS driver and PLL power supplies to the differential signals of the FPD-Link interface.

2 FPD-Link power domains

The FPD-Link interface for TRAVEO™ T2G cluster MCUs spans pins 79 (83) through 104 (108) in the TEQFP 208 (TEQFP-216) packages. Within **Figure 1**, those pins shown with signal names are where the FPD-Link power, ground, and differential signals are present. This interface has three power domains:

- VDDHA_FPD0 and VSSA_FPD0: Power and ground for FPD-Link line drivers
- VDDA_FPD0 and VSSA_FPD0: Power and ground for FPD-Link core supply
- VDDPLL_FPD0 and VSSPLL_FPD0: Power and ground for FPD-Link PLLs

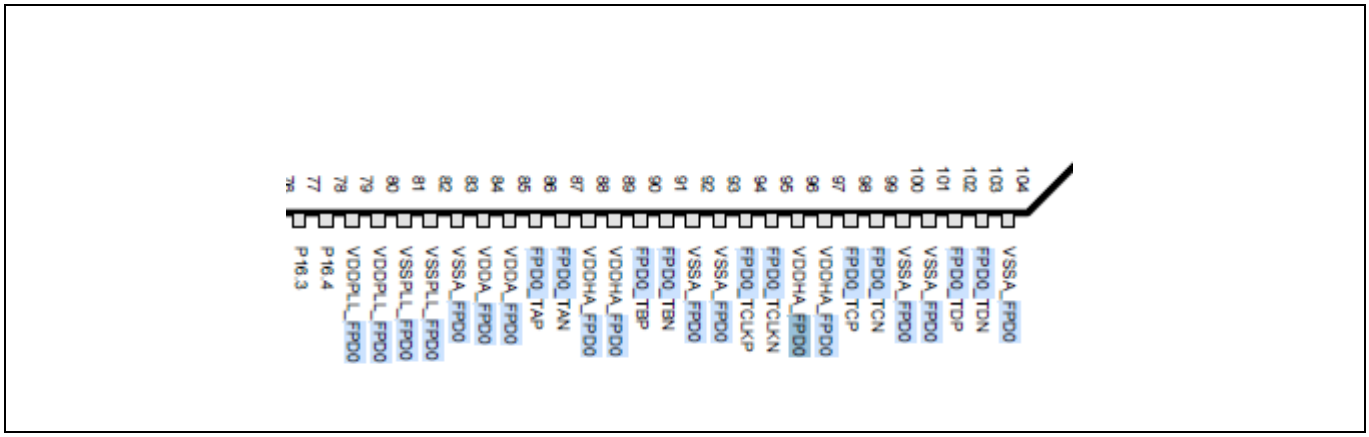


Figure 1 TRAVEO™ T2G cluster series (TEQFP 208) FPD-Link pins

All pins with a named “VSS” in **Figure 1** are device ground (VSS) which must be shorted together, preferably through short connections to a low-impedance ground plane.

The supply for the PLL (used to serialize the video data and clock signal) connects to pins 79 and 80 in **Figure 1**. While both the FPD-Link core supply and serializer PLL supplies are specified to operate over the same 1.15 V, they must not be directly shorted together and connected to the same power source. If they are, the switching noise on the LVDS driver supply couples into the PLL supply causing increased jitter. Likewise, it is recommended to keep the PLL supply separate from that of any attached display to prevent display-induced noise from coupling into the circuits.

The FPD-Link interface was created in 1996 by National Semiconductor for transport of high-speed digital video and dot-clock across parallel ANSI/TIA/EIA-644A standard LVDS links. To reduce the number of signal pairs and lane-to-lane timing constraints, the FPD-Link-II interface was introduced in 2006 that replaces the multiple LVDS links with a single current-mode logic (CML) differential serial bit-stream carrying the same video data with an embedded clock. The interface was enhanced again in 2010, creating the FPD-Link-III interface, via addition of an embedded bidirectional communications channel for control signaling.

3 FPD-Link use cases

The FPD-Link video interface connects to a display with either an integrated FPD-Link receiver or a parallel RGB interface. The components used to implement this connection play a critical part in determining applicable noise reduction methods for the PLL supply.

There are two general use cases for the FPD-Link interface in TRAVEO™ T2G cluster series MCUs:

- DIRECT: FPD-Link TX => FPD-Link RX => Display
- CONVERTED: FPD-Link TX => FPD-Link RX => FPD-Link-II/III TX => FPD-Link-II/III RX => Display

A pair of examples of direct FPD-Link connections is shown in **Figure 2**. The upper diagram shows a direct connection to a display with an integrated FPD-Link receiver. Such a link may also contain a separate cable carrying the LVDS signals between the FPD-Link transmitter in the TRAVEO™ T2G cluster MCU and the FPD-Link receiver integrated into the display.

The lower diagram in **Figure 2** shows a direct connection to a display with a native parallel RGB interface. Video data is transported between the TRAVEO™ T2G cluster MCU and the display through an FPD-Link interface, but is converted to parallel RGB using a separate device external to the display module.

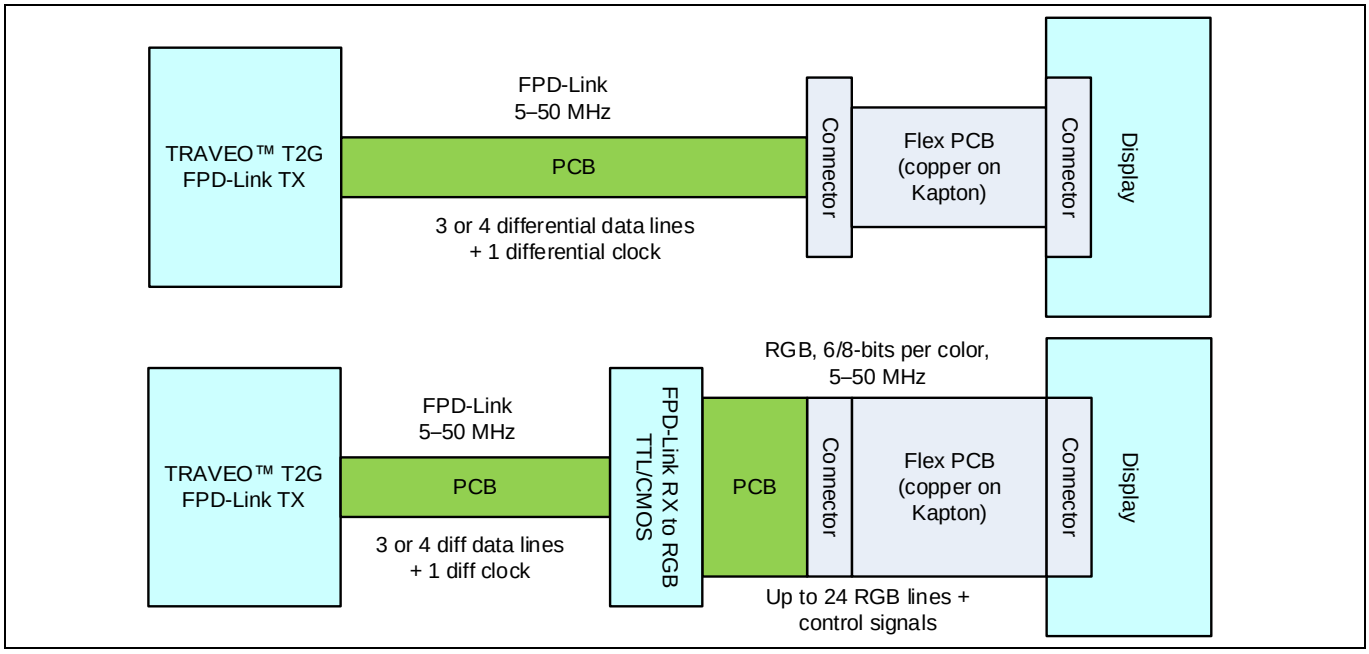


Figure 2 FPD-Link direct to display examples

Examples of a converted FPD-Link connection are shown in **Figure 3**. These are similar to the direct connections in **Figure 2**, but include the hardware to convert from the multi-lane FPD-Link interface to a single serial-stream FPD-Link-II interface. While the protocol and content of the data sent by the TRAVEO™ T2G cluster series MCU and accepted by the display do not change, the physical transport layer between them is now a single balanced transmission line with no constraints for lane-to-lane skew.

Because an FPD-Link-II interface carries four times as much data as each of the LVDS lanes in an FPD-Link interface, the jitter present on the TXCLK± signal must be much lower than that of the direct connections in **Figure 2**. This requires significantly lower noise at the PLL supply input to the TRAVEO™ T2G cluster series MCU.

FPD-Link use cases

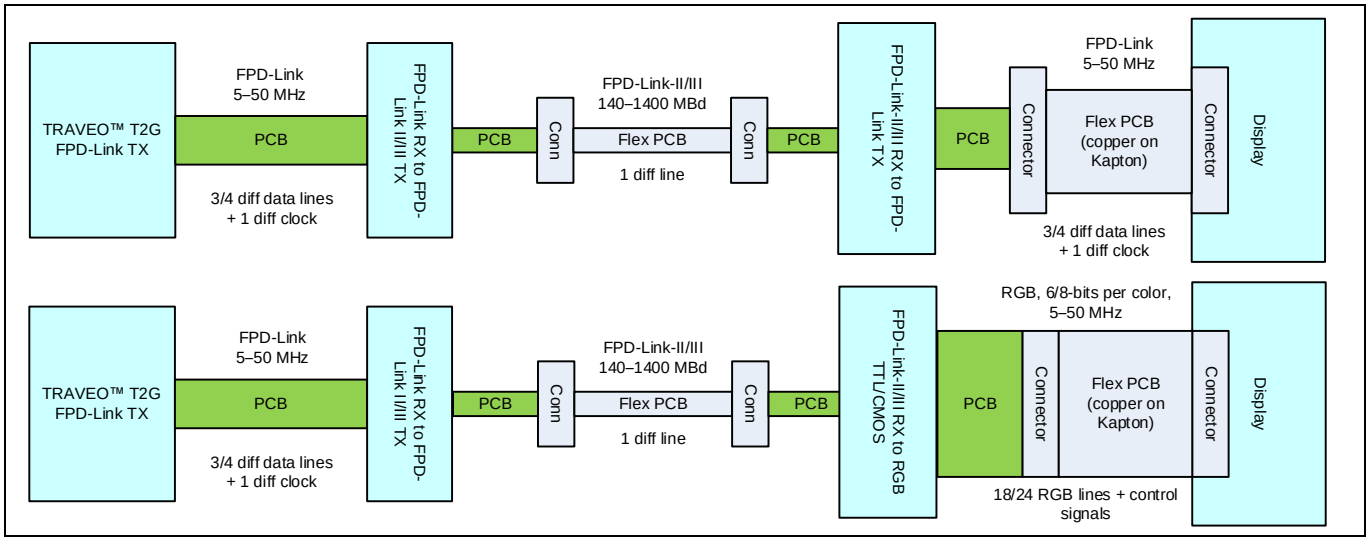


Figure 3 FPD-Link through an FPD-Link-II converter example

4 PLL supply filter options

While it would be simple to provide a one-size-fits-all power-filter solution for the PLL supply, that solution may not be cost-optimal for all applications. For example, if the interface is only used for direct connections (like those in **Figure 2**), the additional filtering required for transport through an FPD-Link-II interface is not required. **Table 1** provides a list of power filter options that ensure that the FPD-Link interface meets its performance requirements for the given conditions. These filter options include an LDO regulator, RC low-pass filter, or LC low-pass filter.

Table 1 FPD-Link PLL supply filter options

Case #	PLL supply voltage	Supply noise	TXCLK frequency (MHz)	Connection type	Filter [1]
1	>3.6 V	–	–	–	LDO
2	3.3 V ≤ S ≤ 3.6 V	> 100 mV pp	–	–	LDO
3	3.0 V ≤ S ≤ 3.6 V	≤ 100 mV pp	≥ 24	Direct	RC
4			< 24		None (decouple) [2]
5			–	Converted	LC
6		≤ 20 mV pp	–	Direct	None (decouple) [2]
7			–	Converted	LC
8		≤ 7 mV pp	–	–	None (decouple)[2]

4.1 LDO filter

A low drop-out (LDO) regulator is a linear regulator IC that blocks most noise on an external power supply while regulating to a lower supply level. For Case 1 in **Table 1**, an external regulator is required because the available external supply exceeds the maximum allowed operating range for the FPD-Link PLL supply. An example LDO regulator meeting the requirements of the PLL supply is shown in **Figure 4**.

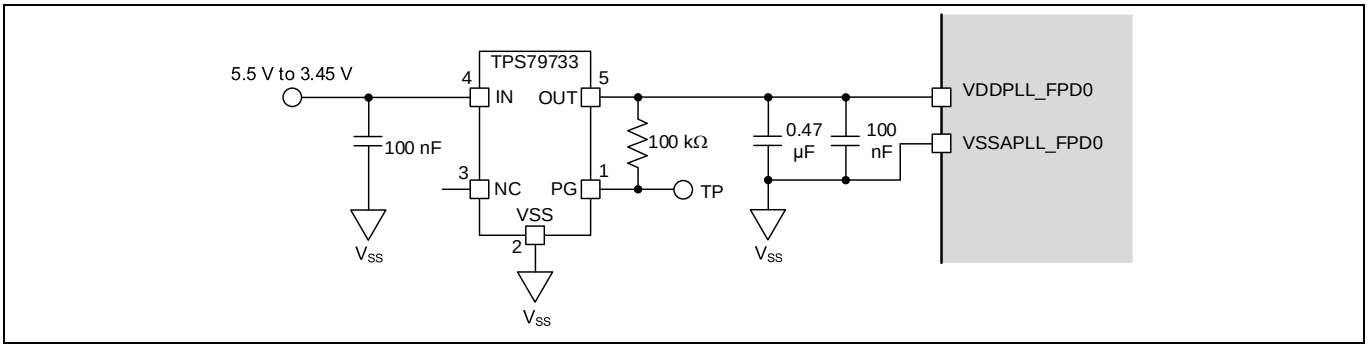


Figure 4 LDO example for supplies >3.45 V

[1] The cutoff frequency of the passive filters specified in this application note assumes spectral noise commonly found in high-frequency buck switching regulators; i.e., >100 kHz. For environments where the PLL supply noise frequencies are lower than this, it may be necessary to select alternative reactive components to lower the corner frequency of the filter, change the filter type, or program the on-die PLL loop-filter bandwidth to a higher frequency to allow the PLL to reject more of the supply noise.

[2] While in these cases a PLL supply filter is not required to limit the noise from the power supply, one may still be required to provide isolation between the LVDS driver (VDDA_FPD0) and serializer PLL (VDDPLL_FPD0) power domains, or to filter the noise injected into the VDDAPLL_FPD0 supply by other sources.

TPS79733 is a low-current regulator (10 mA) with a fixed 3.3-V output. To ensure stability, the regulator needs a load capacitor of at least 0.47 µF. This regulator requires very low headroom (110 mV) and supports supplies up to 5.5 V.

The LDO filter circuit in **Figure 4** can also support the lower supply range in Case 2 by replacing the TPS79733 regulator with a TPS79730. This alternative regulator provides a lower 3.0-V output, but because this is effectively free of noise, it still meets the minimum voltage requirement of the FPD-Link PLL.

4.2 RC low-pass filter

For environments that provide a normally conditioned supply (1.15 V, 100-mV pp noise), where the use case is for a direct FPD-Link connection (see **Figure 2**), a simple RC low-pass filter like that in **Figure 5** is generally sufficient for operation at all TXCLK frequencies.

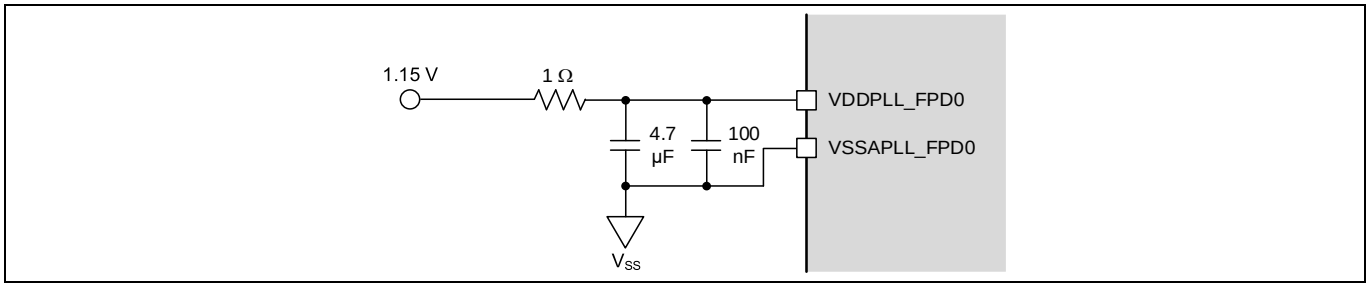


Figure 5 RC low-pass filter example

*Note: The smaller 100-nF capacitor in **Figure 5** provides a dynamic charge to the PLL. While this theoretically can be provided by the 4.7-µF capacitor of the RC filter, its higher equivalent series resistance (ESR) limits its effectiveness for high-frequency charge delivery.*

The cutoff frequency (–3 dB power point; 20 log V_{OUT}/V_{IN}) for a single-pole RC filter is determined by **Equation 1**. For the filter components shown in **Figure 5**, this provides a corner frequency of ~34 kHz. Spectral content in the supply above this frequency gets attenuated by 20 dB/decade (6 dB/octave).

$$fc = \frac{1}{2\pi RC} \quad \textbf{Equation 1}$$

As noted in **Table 1**, an RC low-pass filter is not required in all use cases of direct connections. When the TXCLK frequency is low enough (Case 4), or the source supply noise is low enough (cases 6 and 8), all that is required is a power supply decoupling capacitor (see Section **4.4**) to handle the dynamic charge needs of the serializer PLL.

4.3 RLC low-pass filter

For environments that provide a normally conditioned supply (1.15 V, 100-mV pp noise), where the use case is for an FPD-Link connection through an FPD-Link-II converter (see **Figure 3**), an LC low-pass filter like that in **Figure 6** is sufficient for operation at all TXCLK frequencies.

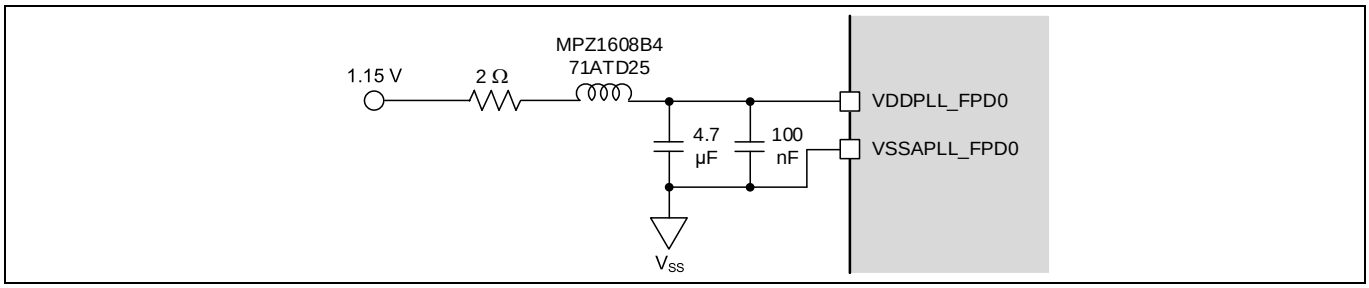


Figure 6 LC low-pass filter example

The cutoff frequency (–3 dB power point; 20 log VOUT/VIN) for a single-pole LC filter is determined by **Equation 2**. For the filter components shown in **Figure 6**, this provides a corner frequency of ~25 kHz. Due to the presence of two reactive components in this LC filter, instead of just the single capacitor in the RC filter, spectral content in the supply above this frequency gets attenuated by 40 dB/decade (12 dB/octave).

$$fc = \frac{1}{2\pi\sqrt{LC}} \quad \textbf{Equation 2}$$

The inductor shown in **Figure 6** is really a ferrite bead designed for automotive power-line filtering. While shown in **Figure 6** as an inductor, its main equivalent internal components consist of an 8.6-µH inductor in parallel (shunted) with a 470-Ω resistor. This means that the 40-dB/decade attenuation slope only holds for spectral content below around 5 MHz, and slowly transitions to a 20-dB/decade rate for frequencies over 10 MHz (XL = XR at 8.7 MHz). Because the primary area of noise concern are for those frequencies around the loop bandwidth of the PLL (<< 2 MHz), this transition to an alternate slope at higher frequencies has no impact on the jitter performance of the PLL.

There is no requirement to use the specific ferrite bead shown in **Figure 6**. Alternative ferrite beads from other manufacturers, or passives designed specifically as inductors (i.e., without the internal shunt resistor), may provide the same or better spectral filtering as long as they have equivalent or greater inductance. When selecting the reactive elements, it is strongly recommended to simulate the resulting filter network to ensure that there is no significant gain (peaking) around the resonance point of the LC filter. The 2-Ω resistor in **Figure 6** is selected for the listed ferrite, and is there specifically to dampen any potential oscillations (damping factor $\zeta \geq 1$), and varies based on the Q of the components in the filter.

As noted in **Table 1**, an LC low-pass filter is not required in all use cases of converted connections. When the source supply noise is low enough (Case 8), all that is required is a power supply decoupling capacitor (see Section **4.4**) to handle the dynamic charge needs of the serializer PLL.

4.4 Non-filtered

While **Table 1** lists a number of FPD-Link PLL supply filter options that do not require an external filter, the associated use cases must be evaluated and implemented with care. For Case 4 (normal supply range, normal supply noise, direct FPD-Link connection, operated below 24 MHz), the PLL should be able to meet its cycle-to-cycle jitter requirement due to the larger unit interval (UI) at the slower clock rates. However, this is only possible if the noise source is from the external supply and within a similar spectral range. If a secondary noise source is also coupled into the PLL supply, the TXCLK output jitter may exceed its datasheet limits.

The directly adjacent LVDS driver supply is the most common source for this secondary noise. When the FPD-Link interface is operating, up to five differential drivers (10 output pins) can be switching at exactly the same time. These switching events have a nominal duration of ~400 ps, and during each transition, current on the LVDS driver supply can exceed 300 mA. This is considerably more than the < 10 mA needs of the PLL supply. These LVDS driver switching events can couple noise into a shared supply.

PLL supply filter options

For cases where the serializer PLL supply is sourced from a different regulator than that of the LVDS drivers, a local decoupling capacitor like that in **Figure 7** is all that is required.

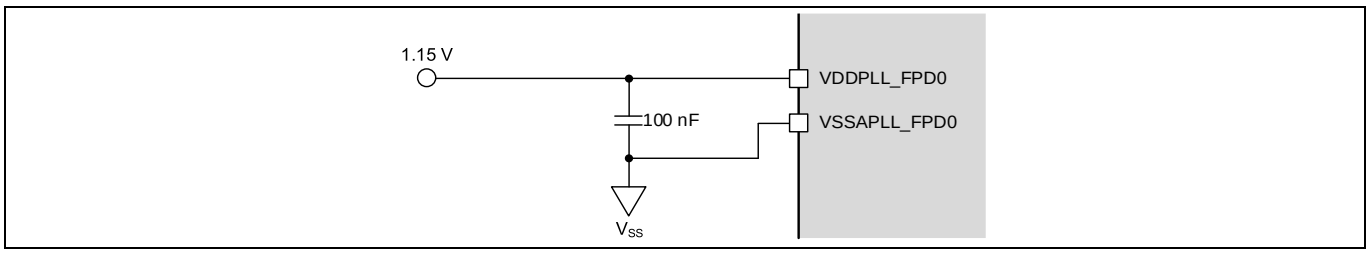


Figure 7 Non-filtered decoupling only

4.5 Shared driver/PLL supply

Unfortunately, the reality of cost-effective system design seldom provides a large array of independent regulated sources. Far more common is a single supply that provides power to multiple domains operating at the same voltage. Because both the LVDS driver (VDDA_FPD0) and serializer PLL (VDDPLL_FPD0) operate over the same 1.15-V range, they are usually powered from the same source. To prevent the LVDS driver supply from becoming an aggressor and coupling noise into the serializer PLL supply, the PLL supply must be filtered.

As noted in Section **4.1**, an LDO regulator can allow the operation of the PLL supply from a source in the allowed operating range, but only when the minimum supply remains above the dropout voltage of the regulator, and the regulator output is ≥3.0 V.

Implementations for passive filters for use with a shared driver/PLL supply are shown in **Figure 8**. These take the same filters shown in **Figure 5** and **Figure 6** and add local decoupling capacitors for the LVDS drivers supply pins.

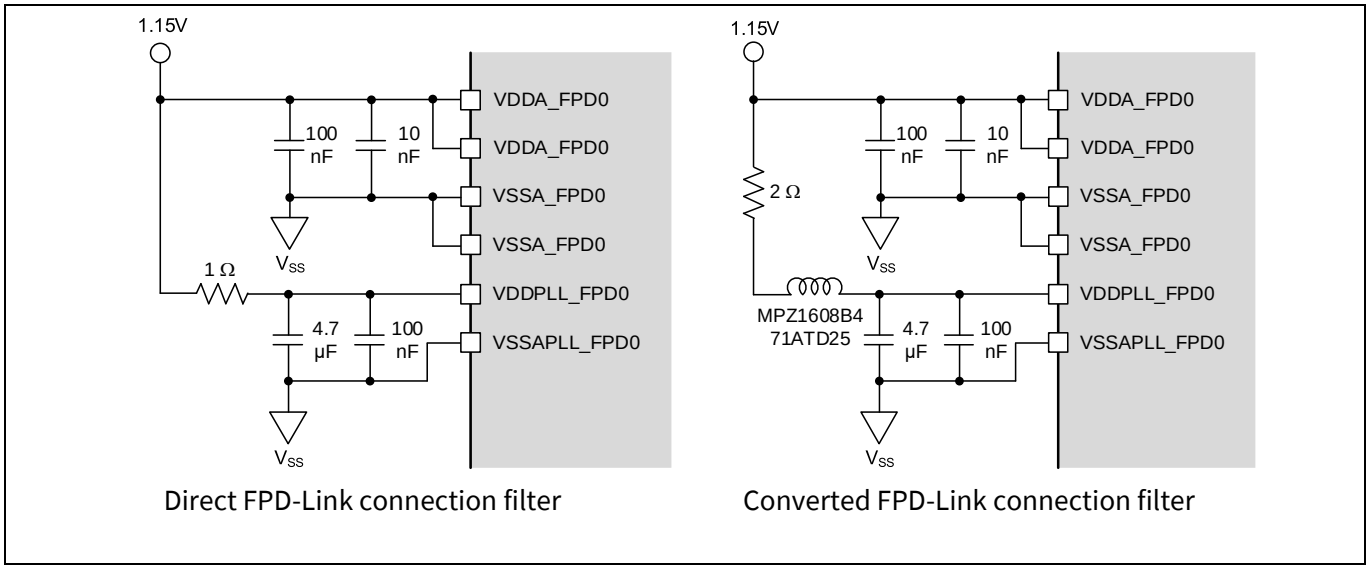


Figure 8 Shared driver/PLL supply filters

5 Voltage coefficient of capacitors

When selecting a capacitor to implement the RC or LC filter, the standard specifications of temperature coefficient and breakdown/operating voltage are not sufficient to ensure that the filter performs as needed. This is because the base capacitance of most ceramic capacitors is specified only at 0-V DC. As the DC potential across the capacitor increases, the actual capacitance tends to drop such that a part with a datasheet capacitance of 4.7 µF often has much less under bias.

Figure 9 shows plots of the capacitance versus applied DC voltage for two capacitors from a top-rated manufacturer. Both capacitors have identical specifications of 4.7-µF capacitance, X7R dielectric, 10% tolerance, 10-VDC rated, and 0805 (2012M) package size.

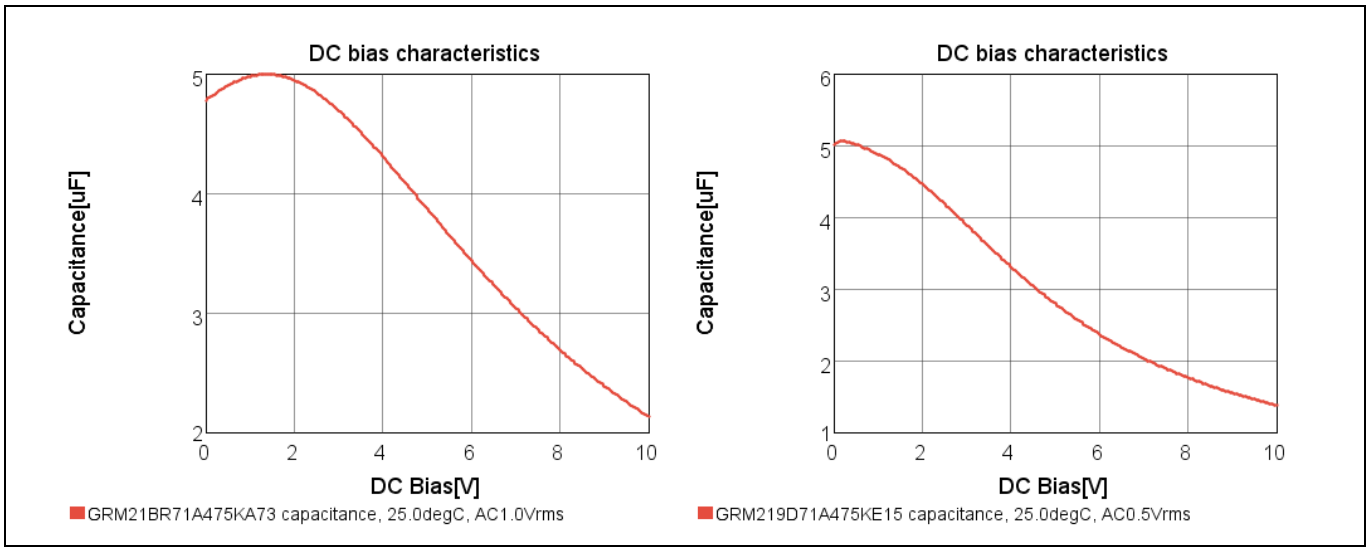


Figure 9 Voltage coefficient comparison

While both are excellent 4.7-µF capacitors, a GRM21BR71A475KA73 capacitor (left graph in **Figure 9**) provides 4.6-µF of capacitance with 3.3-V DC across it, while a GRM219D71A475KE15 capacitor (right graph in **Figure 9**) provides only 3.7 µF (–22%) under the same conditions.

If the 4.7-µF capacitor on the left in **Figure 9** is used to implement our RC filter, the –3 dB cutoff frequency would be at ~35 kHz. Using the capacitor on the right would move this corner frequency to ~43 kHz, and allow more noise into the PLL power supply.

A simple alternative to finding a capacitor with a flat voltage coefficient is to select one that provides the necessary capacitance under the given operating conditions. For example, the next larger standard size capacitor would be 6.8 µF. A 6.8-µF capacitor with the same voltage coefficient profile as that on the right in **Figure 9** would provide a 5.3-µF capacitance when biased to 3.3 V, and provide a ~30-kHz cutoff.

6 Summary

This application note provides recommended active and passive power-domain filters to ensure low clock jitter and error-free data transfer through the FPD-Link video interface of TRAVEO™ T2G cluster MCUs.

7 Abbreviations

Abbreviation	Description
GPIO	general-purpose I/O
LDO regulator	low-dropout regulator
MCU	microcontroller Unit
PCB	printed circuit board
PG	power good output signal from PMIC
PFM	pulse frequency modulation
PMIC	power management integrated circuit
PWM	pulse width modulation
POR	power-on-reset

8 Related documents

The following are the TRAVEO™ T2G family series datasheets and technical reference manuals. Contact **Technical Support** to obtain these documents.

- Device datasheets
  - CYT3DL datasheet 32-bit Arm® Cortex®-M7 microcontroller TRAVEO™ T2G family (Doc No. 002-27763)
  - CYT4DN datasheet 32-bit Arm® Cortex®-M7 microcontroller TRAVEO™ T2G family (Doc No. 002-24601)
- Architecture technical reference manual (TRM)
  - TRAVEO™ T2G automotive cluster 2D family architecture technical reference manual (TRM) (Doc No. 002-25800)
- Registers technical reference manual (TRM)
  - CYT3 series: TRAVEO™ T2G automotive cluster 2D registers technical reference manual (TRM) for CYT3DL (Doc No. 002-29854)
  - CYT4 series: TRAVEO™ T2G automotive cluster 2D registers technical reference manual (TRM) for CYT4DN (Doc No. 002-25923)
- **AN211139** – FPD-Link PCB guidelines for the TRAVEO™ T1G family S6J3200 series MCUs

Revision history

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**	2021-10-04	New application note.

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