# Short errata sheet - power-up behavior and flyback condition

## EiceDRIVER™ 1EDI3050AS, 1EDI3051AS

Z8F80578229

## About this document

### Scope and purpose

This document provides information on the power-up behavior of the gate driver. The term gate driver is hereby referring to the products mentioned in Chapter 1.1.

### Intended audience

This document is intended for engineers who develop and integrate applications using the 1EDI3050AS, 1EDI3051AS gate drivers.

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# 1 Errata

## 1.1 References

The following table provides the list of related devices and reference documents for this errata.

**Table 1 Related devices**

| Type | Design step<br>Primary die | Package | Marking |
|---|---|---|---|
| 1EDI3050AS | U5887B | PG-DSO-36 | 1EDI3050AS |
| 1EDI3051AS | | | 1EDI3051AS |

**Table 2 Reference documents**

| # | Document title | Document version | Release date | Infineon internal unique ID |
|---|---|---|---|---|
| 1 | EiceDRIVER™gate driver 1EDI3050AS datasheet | Rev 1.0 | 2023-05-15 | Z8F69662782 |
| 2 | EiceDRIVER™ gate driver 1EDI3051AS datasheet | Rev 1.0 | 2023-05-15 | Z8F69199023 |
| 3 | EiceDRIVER™ 1EDI305x safety manual | Rev 1.0 | 2022-12-12 | Z8F80224682 |
| 4 | Safety analysis summary report 1EDI305xAS | Rev 1.0 | 2022-12-16 | Z8F80318654 |

## 1.2 Possible output stage turn-on during secondary side power-up

Figure 1 shows a simplified block level representation of the gate driver output stage. It is used for further explanation in Chapter 1.2.1.

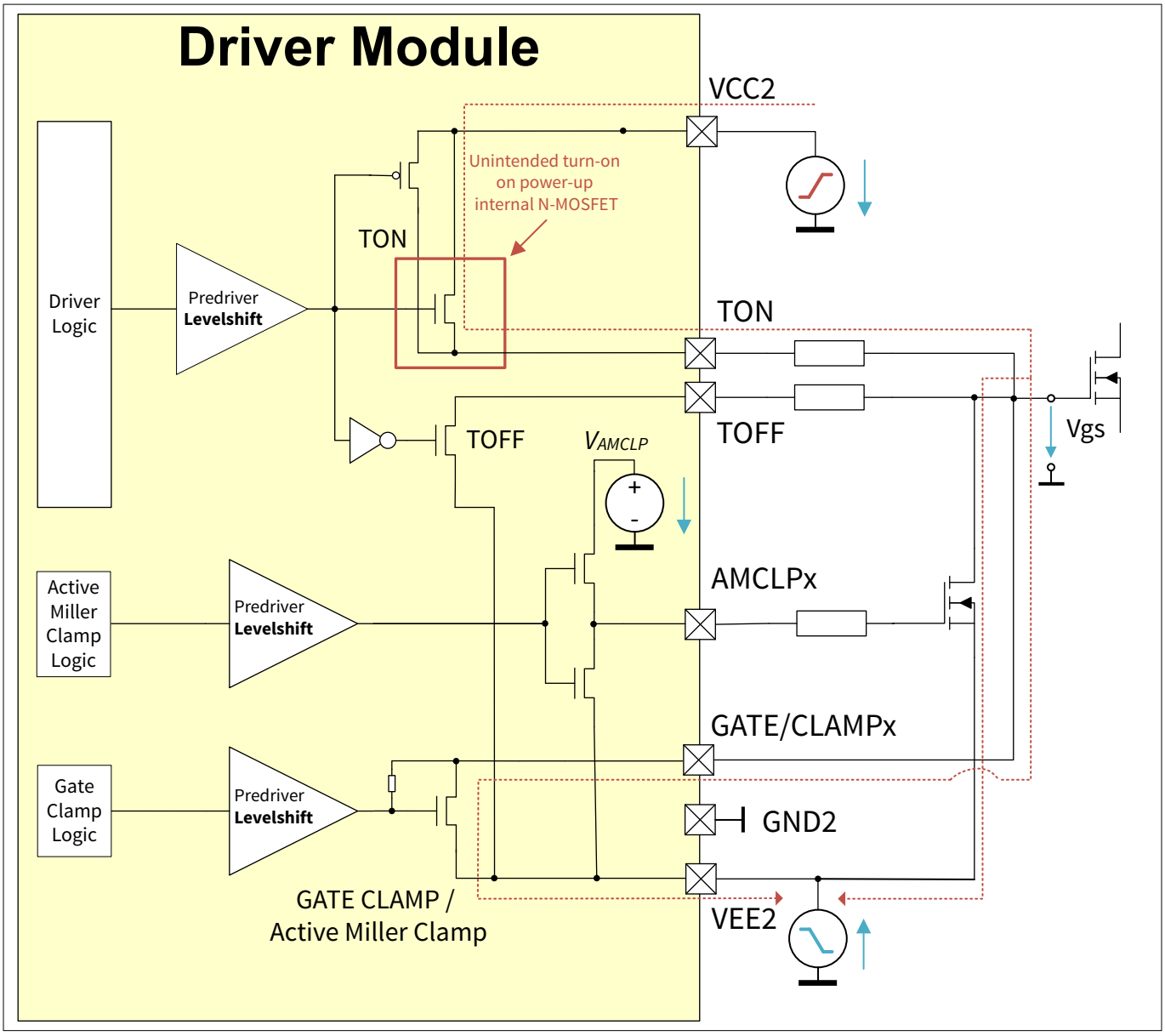



**Figure 1 Driver module unintended turn-on**

### 1.2.1 Description of behavior

In this errata, secondary side power-up is referring to the ramp of the secondary side supply voltages VCC2 and VEE2 from any level, where the VCC2 voltage is initially smaller or equal to 6 V.

#### Occurrence

Upon secondary side power-up an unintended activation of the internal N-MOSFET in the high-side of the gate driver output stage may occur as shown in Figure 1.

The unintended activation is more likely to occur when the gate driver operating temperature is low.

The unintended activation occurs typically in a voltage range of 3 V ≤ VCC2 ≤ 6 V outside the gate driver functional range. During this unintended activation the gate clamp/internal active Miller clamp or external

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active Miller clamp feature can be either active or inactive resulting in the two scenarios hereafter explained in “Impact”.

Once VCC2 is actively driven beyond typically 6 V the unintended activation stops and the gate driver continues to power-up, entering normal operation.

### Impact

Scenario 1 – unintended activation of the internal N-MOSFET while gate clamp/internal active Miller clamp or external active Miller clamp is active (example waveform shown in Figure 2)

- During unintended output stage activation, the N-MOSFET drives the TON pin to VCC2
- The gate clamp/internal active Miller clamp or external active Miller clamp is simultaneously driving the Vgs voltage down to VEE2 either through the internal clamp MOSFET or the external Miller clamp MOSFET
- A cross current starts to flow from VCC2 to VEE2 as depicted in Figure 1
- The cross current and resulting Vgs voltage are given by the voltage divider formed by Rds-on of the unintendedly activated N-MOSFET (PRQ-683), the external gate resistor, the Rds-on of the gate clamp/ internal active Miller clamp (PRQ-99) and the Rds-on of the external active Miller clamp MOSFET
- If the system supply concept is not capable to supply the resulting cross current to the gate driver, the power-up timing may change and cause a prolongation of the unintended activation of the internal N-MOSFET depending on the system power supply characteristic

Scenario 2 – unintended activation of the internal N-MOSFET while gate clamp/internal active Miller clamp or external active Miller clamp is inactive

- During unintended output stage activation, the N-MOSFET drives the TOUT pin to VCC2
- The gate clamp/internal active Miller clamp or external active Miller clamp are not active
- No cross current flows from VCC2 to VEE2
- The resulting Vgs voltage is given by the supply voltage VCC2
- The duration of the unintended activation of the internal N-MOSFET depends on the system supply characteristic

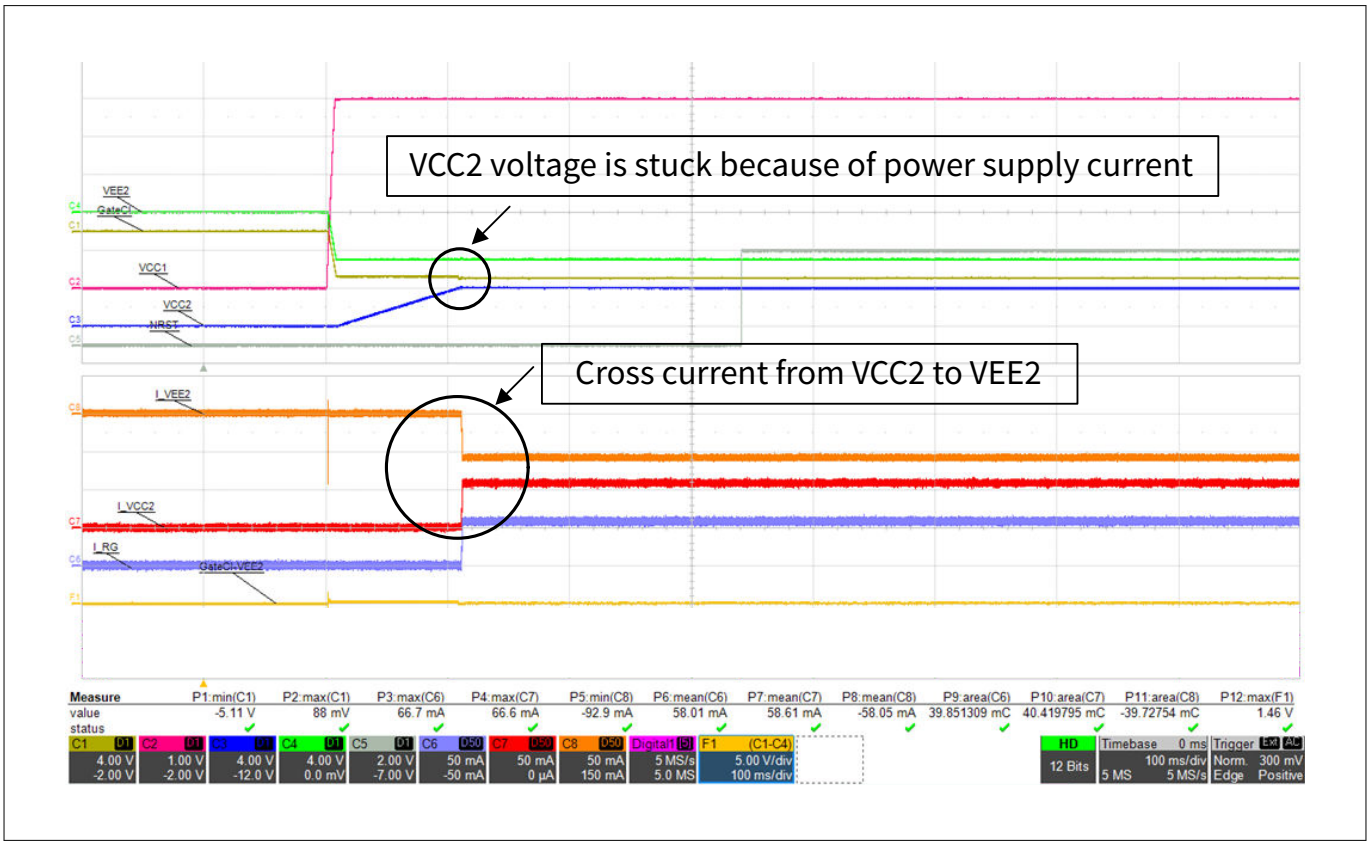



**Figure 2 Scenario 1 power-up example with cross current**

### 1.2.2 Mitigation measure in application

Mitigation measures on application level are possible. Please contact your Infineon sales representative for information on mitigation measures on application level.

#### 1.2.2.1 Containment action

The root cause of the behavior described in this erratum has been determined and the failure mechanisms are identified. A screening method is put into place for all productive devices (datecode > March 2023) to screen for both unintended behaviors (scenario 1 and scenario 2) detailed in Chapter 1.2.1.

For more detailed information, please get in touch with our technical service center.

#### 1.2.2.2 Corrective action

The root cause of the behavior described in this section of the erratum has been determined and the failure mechanisms are identified. A redesign of the 1EDI305xAS gate drivers is planned to remove both of the unintended behaviors detailed in Chapter 1.2.1. See Chapter 1.4 for timeline information.

This redesign will incorporate the learnings from the preceding redesign of 1EDI302x/3xAS (x=0,1,3).

## 1.3 Additional flyback condition on SRDY status

After the secondary side power up an additional criteria exists that must be met for the gate driver to transition from Error_Mode to Ready_Mode. The voltage on level on VCC2 needs to rise above the "flyback threshold, high" $V_{FBth,high}$ voltage (PRQ-837) only once after power up. When this criteria is met and there is no other active error, then the gate driver will transition to Ready_Mode after a rising edge is detected on the NRST input pin.

For any following transition from Error_Mode to Ready_Mode the flyback voltage condition no longer applies. The condition will only be active again after a new power up of the secondary side of the gate driver. See Figure 3 (also figure 3 in the datasheet) for details. The criteria applies regardless of the flyback enable state bit FLYBENA in the FLYBACKC1 register.

- The transition from Error_Mode to ASCP_Mode is not affected
- Secondary side active short circuit function ASCS is not affected

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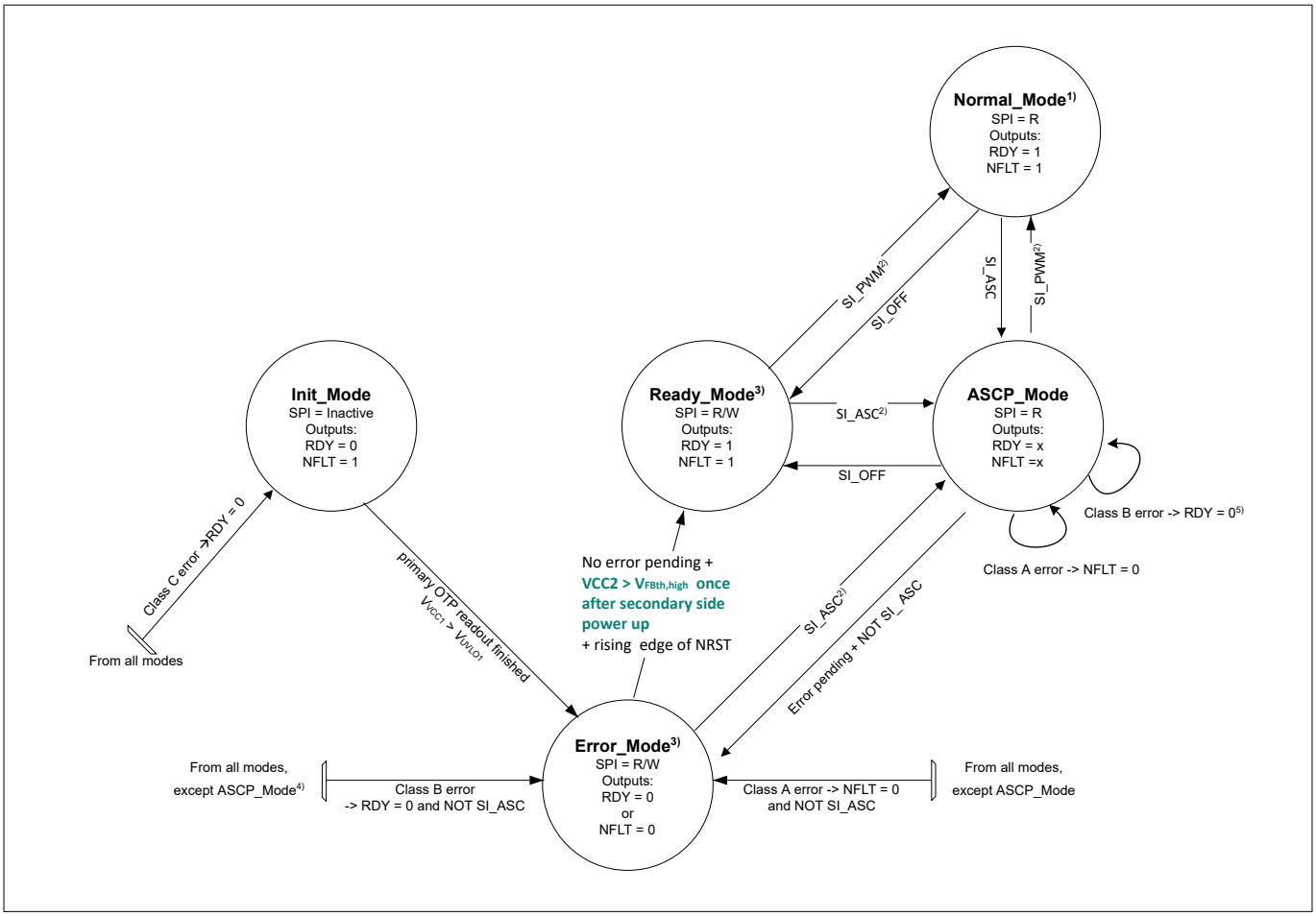



**Figure 3 Updated operating modes diagram**

Furthermore the RDY signal activation list in the datasheet (table 51 in 1EDI3050AS datasheet, table 50 in 1EDI3051AS datasheet)) is expanded to reflect the impact of the additional VCC2 voltage criteria on the RDY signal as shown in Table 3.

**Table 3 RDY signal activation list extension**

| Event | SPI diagnosis | TON/TOFF | Configurable | SPI config register | SI1, SI2 |
|---|---|---|---|---|---|
| $V_{FBth,high}$ not met on VCC2 after power-up | DIAGS | turn-off | Yes | SPSML | Active |

### Impact

Depending on the applied VCC2 supply voltage level after power up and the programmed $V_{FBth,high}$ the gate driver may not transition into Ready_Mode despite a rising edge is detected on NRST and RDY stays low. This means that the gate driver output remains off. PWM switching is not possible. The SRDY bit in the STATUSP register and in the 8 bit in frame status response is not set.

## 1.3.1 Mitigation measure in application

The "flyback threshold, high" $V_{FBth,high}$ reflects the maximum detection threshold of the programmed flyback output voltage set level. When the flyback is enabled and used to supply the secondary VCC2 voltage $V_{FBth,high}$ will be automatically reached due to the flyback feedback loop and regulation. A transition into Ready_Mode is

then possible by applying a rising edge on NRST in case of no other pending error condition. When the flyback is disabled through the bit FLYBENA in FLYBACKC1 register and VCC2 is externally supplied, two scenarios have to be considered in the application as shown in Chapter 1.3.1.1 and Chapter 1.3.1.2.

### 1.3.1.1 VCC2 voltage higher than default flyback threshold high voltage

In this scenario the flyback is disabled and the VCC2 voltage is externally supplied. The external supply voltage settles above $V_{FBth,high}$, which is given by the default value of the VCC2VL setting in the SPSML register. Prior to applying a rising edge on NRST no further action is required to transition the gate driver to Ready_Mode.

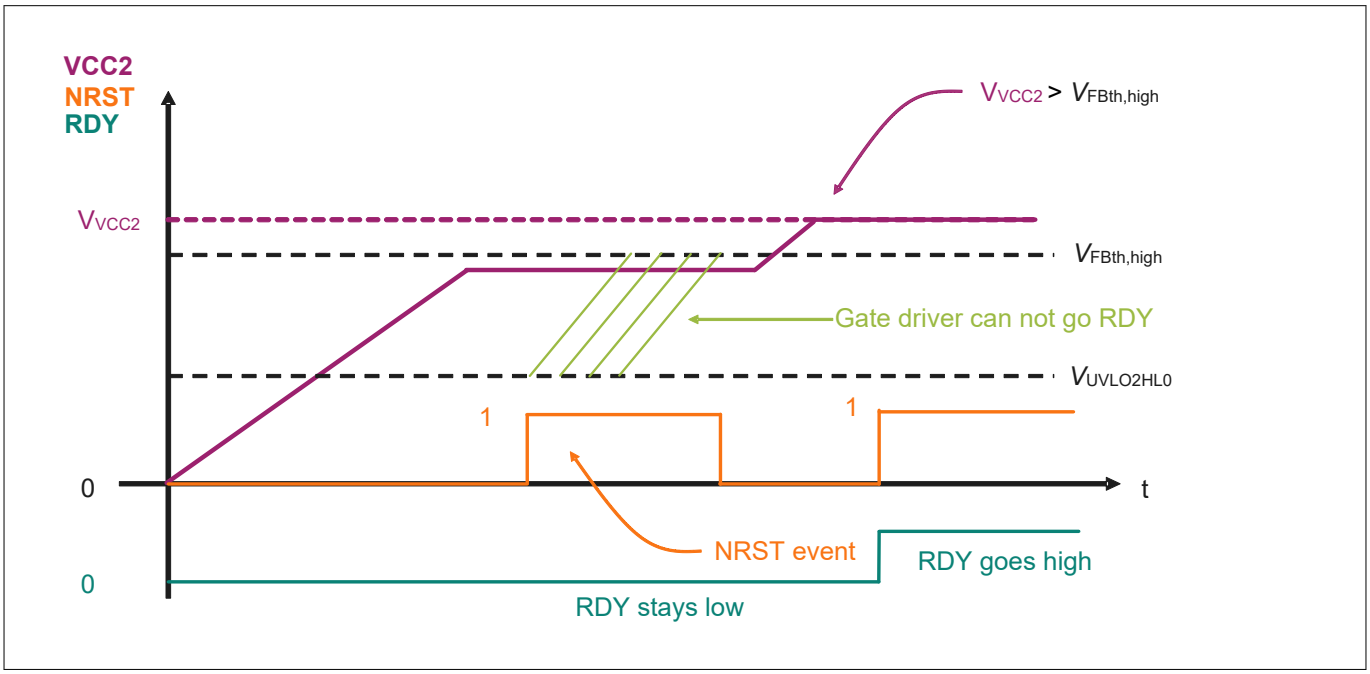



**Figure 4 Scenario 1 example - no reprogramming required**

### 1.3.1.2 VCC2 voltage lower than default flyback threshold high voltage

In this scenario the flyback is disabled and the VCC2 voltage is externally supplied. The external supply voltage settles below $V_{FBth,high}$, which is given by the default value of the VCC2VL setting in the SPSML register. The gate driver will not transition into Ready_Mode after applying a rising edge on NRST. A transition into Ready_Mode is only possible after reprogramming the VCC2VL setting in the SPSML register to a lower voltage value than the default value. This scenario is especially important for IGBT applications, where VCC2 is usually supplied to be 15 V, while the default VCC2VL setting is also 15 V. As a consequence a transition to Ready_Mode is not possible unless VCC2VL is reprogrammed to a lower setting. Note that the lowest VCC2VL setting is 14 V.

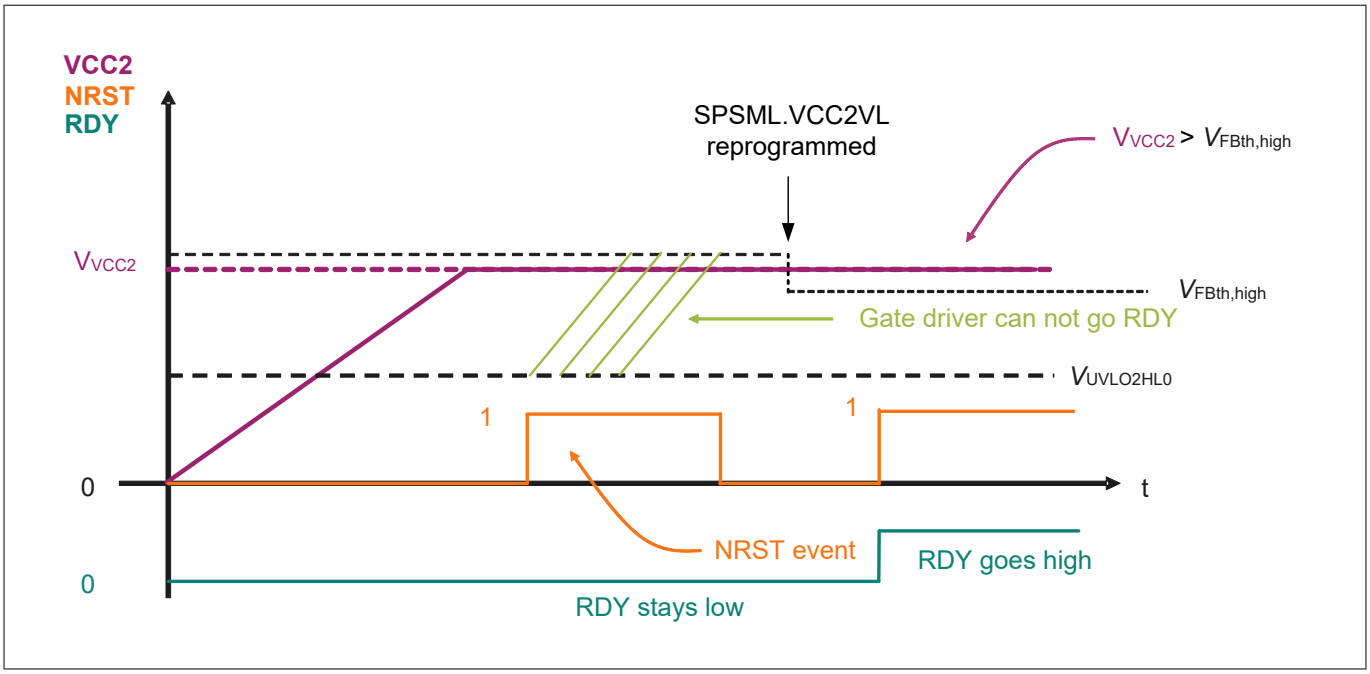



**Figure 5 Scenario 2 example - reprogramming through SPI required**

### 1.3.1.3 Containment action

A containment for the described behavior is not possible, since the root cause is a systematic implementation in the secondary chip digital design. Therefore every part is affected.

### 1.3.1.4 Corrective action

The root cause of the behavior described in this section of the erratum has been determined and the resulting behavior has been described. A redesign of the 1EDI305xAS gate drivers is planned to remove the additional flyback condition of Chapter 1.3 that is applied on power-up. See Chapter 1.4 for timeline information.

## 1.4 Redesign timeline

For more detailed information on redesign timeline, please get in touch with our technical service center.

# Revision history

| Document version | Date of release | Description of changes |
|---|---|---|
| 1.0 | 2024-03-18 | Initial release |

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