SIEMENS

Microcomputer Components
Technical Support Group Munich
HL MCB PD 8

Errata Sheet

July 7, 1997 / Release 1.0

Device : **C509-L**

Marking : **DB**

These parts of the SAB-C509-L/SAF-C509-L can be identified by the letters "DB" below the part number. The parts are mounted in a Plastic Metric Quad Flat Pack (P-MQFP-100-2) package.

This errata sheet describes both the functional problems (see part 1) and the deviations from the electrical and timing specifications (see part 2) known in this step.

If a problem was already introduced with an errata sheet of an earlier step, its initial number is still retained in this errata sheet. Thus, the numerical order of the problems described in the following may contain gaps.

At the end of this document, you will find two history tables showing the problems found in the C509-L up to now. Changes to the last revision are shaded light grey in the history tables.

1) Functional Problems

The following malfunctions are known in this step:

Problem 7 : MDU-Error Flag Mechanism

The error flag mechanism in the MDU is not functional in this step and therefore the error flag MDEF (ARCON.7) should not be used.

Workaround :

The multiplication, division, normalize or shift left/right operations will work correctly if a once started operation was not disturbed by any read/write operation to the registers MD0, MD1, MD2, MD3, MD4, MD5, or ARCON before it was terminated (e.g. by a interrupt routine).

Problem 16 : Slow Down Mode

The Slow-Down Mode is not tested in this step.

Problem 21 : Normalizing with the MDU

Conditions:

The Multiplication/Division Unit (MDU) performs a normalize operation and the overflow flag MDOV in SFR ARCON (EF_H) is used for detection of the MSB MD3.7 in SFR MD3 (EC_H).

Failure:

When performing a normalizing operation with the MSB MD3.7 set in SFR MD3 (EC_H), the overflow flag MDOV in SFR ARCON (EF_H) might be not set erroneously by the HW.

Workaround:

If MD3.7 bit in SFR MD3 (EC_H) is set before the normalize operation, the overflow flag MDOV has to be set by the corrective SW after having finished the normalize operation by the MDU.

Problem 26 : Timer 0/1 in operating mode 3

When timer 0 operates in mode 3 there are some restrictions for the prescaler ratios of timer 0 and timer 1. Dependent on the selected mode for the low-byte of the timer 0 register (SFR TL0 at address 8AH) - timer or counter mode - some restrictions concerning the prescaler ratio settings have to be regarded.
While TL0 operates as counter, the timer clock of the high-byte of the timer 0 register (SFR TH0 at address 8CH) is fixed at fosc/6 and cannot be changed by setting another prescaler ratio for timer 0 in SFR PRSC (B4H). In counter mode, the divider ratios of prescaler 0 and 1 have to be set to 1÷1. Otherwise the interrupt generation by bit TF1 (timer 1 overflow bit) located in SFR TCON (88H) might be erroneously disturbed.
While TL0 operates as timer, both prescalers have to be set to the same divider ratio values (1÷1, 1÷2, 1÷4 or 1÷8) for proper timer 1 interrupt generation.

Counter mode:
For correct timer 1 interrupt generation in counter mode, the following prescaler ratio initialization is recommended:

```
MOV    PRSC,#XXXX0000B     ;timer 0 and timer 1 prescaler are set to ratio 1÷1
                           ;as result the timer 0/1 clock is fixed at fosc/6
```

Timer mode:
For correct timer 1 interrupt generation in timer mode, prescalers 0 and 1 have to be set to the same divider ratio; e.g.:

```
MOV    PRSC,#XXXX1010B     ;timer 0 and timer 1 prescaler are set to the same ratio
                           ;in this example 1÷4 which results in timer 0/1 clock of fosc/24
```

Note: The abbreviation „X“ means don’t care.

2) Electrical- and Timing-Spec. Deviations

The following deviations of electrical and timing parameters from the specification are known in this step:

Problem 1: **Restricted Duty Cycle of the External Clock Drive XTAL2**

The specified duty cycle variation of the oscillator clock from 0.4 to 0.6 at CPU clock = 16 MHz is not met. The duty cycle of the external clock drive XTAL2 for this step is restricted from 0.45 to 0.55 at CPU clock = 16 MHz.

Problem 3 : **Restricted Voltage Supply Vcc**

The specified voltage supply range of Vcc = 5V +10%, - 15% is restricted for this step to Vcc = 5V +10%, - 5% (4.75V ≤ Vcc ≤ 5.5V).

Problem 1 and 3 above will be fixed in future revisions of the Data Sheet and User's Manual. The actual valid revisions are 09.96 for the Data Sheet and 07.96 for the User's Manual.

Functional Problem No.	Marking	Description	Remarks
1	ES-AA	XRAM access via SFR XPAGE/P2	fixed in ES-AB and later
2	ES-AA, ES-AB	External access to Data Memory	fixed in ES-BB and later
3	ES-AA	Baudrate Generator of Serial Interface 0	fixed in ES-AB and later
4	ES-AA, ES-AB	Reset Value of SFR EICC1	fixed in ES-BB and later
5	ES-AA	Pin PRGEN	fixed in ES-AB and later
6	ES-AA, ES-AB, ES-BB, BB; ES-CA	Oscillator Watchdog (replaces HWPD-Reset)	fixed in DB
7	ES-AA, ES-AB, ES-BB, BB; ES-CA, DB	MDU-Error Flag Mechanism	
8	ES-AA, ES-AB	Bootstrap-Loader SW-Problem	fixed in ES-BB and later
9	ES-AA	Emulation Mode	fixed in ES-AB and later
10	ES-AA, ES-AB	Serial Interface 0 (USART) in 9-bit modes 2 and 3 - Incorrect RB80 reception	fixed in ES-BB and later
11	ES-AA, ES-AB	Serial Interface 0 (USART) in 8-bit mode 1 - Incorrect RB80 reception	fixed in ES-BB and later
12	ES-AA, ES-AB	Serial Interface 1 (USART) in 9-bit mode A or 8-bit mode B - Incorrect RB81 reception	fixed in ES-BB and later
13	ES-AA, ES-AB, ES-BB, BB; ES-CA	Write to SFR DIR2	fixed in DB
14	ES-AA, ES-AB, ES-BB, BB; ES-CA	Undefined Reset Values of Datapointers 1-7	fixed in DB
15	ES-AA, ES-AB, ES-BB, BB; ES-CA	Bidirectional Port Structure at Port 0 during external memory access	fixed in DB
16	ES-AA, ES-AB, ES-BB, BB; ES-CA, DB	Slow-Down Mode	

Functional Problem No.	Marking	Description	Remarks
17	ES-AA, ES-AB, ES-BB, BB; ES-CA	Reset Values at A/D Converter SFR´s	fixed in DB
18	ES-AA, ES-AB, ES-BB, BB; ES-CA	Timer 0/1 Overflow Bits TF0/TF1	fixed in DB
19	ES-AA, ES-AB, ES-BB, BB; ES-CA	Start of Compare Timer 1	fixed in DB
20	ES-AA, ES-AB, ES-BB, BB; ES-CA	Modulation Range in CM0 with the Compare Timers 0/1	fixed in DB
21	ES-AA, ES-AB, ES-BB, BB; ES-CA, DB	Normalizing with the MDU	
22	ES-AA, ES-AB, ES-BB, BB; ES-CA	Timer 2 - Compare Mode 2	fixed in DB
23	ES-AA, ES-AB, ES-BB, BB; ES-CA	Reset Values at Timer 2 SFR´s	fixed in DB
24	ES-AA, ES-AB, ES-BB, BB; ES-CA	Port 0 write instructions during external program execution	fixed in DB
25	ES-AA, ES-AB, ES-BB, BB; ES-CA	Wrong destination address at AJMP and ACALL instructions	fixed in DB
26	ES-AA, ES-AB, ES-BB, BB; ES-CA DB	Timer 0/1 in operating mode 3	

Table 1: History of Functional Problems

Electrical- / Timing-Problem No.	Marking	Description	Remarks
1	ES-AA, ES-AB, ES-BB, BB; ES-CA	Restricted Duty Cycle of the External Clock Drive XTAL2	
2	ES-AA, ES-AB, ES-BB, BB; ES-CA	Restricted Accuracy of the AD-Converter	fixed in DB
3	ES-AA, ES-AB, ES-BB, BB; ES-CA	Restricted Supply Voltage Vcc	
4	ES-AA, ES-AB, ES-BB, BB	Restricted Capacity Load Conditions	fixed in CA
5	ES-AA, ES-AB, ES-BB, BB; ES-CA	Input Hysteresis for CMOS Ports	fixed in DB

Table 2: History of Electrical- and Timing-Spec. Deviations