Errata Sheet

V 1.1, 2003-12

Device	**C868-1RR/RG**
Marking/Step	**Step ES-CA, CA**
Package	**P-TSSOP-38,**
	P-DSO-28

This Errata Sheet describes the deviations from the current user documentation.

The module oriented classification and numbering system uses an ascending sequence over several derivatives, including already solved deviations. So gaps inside this enumeration can occur.

Current Documentation

- C868 User's Manual V1.0 January 2003
- C868 Data Sheet V1.0 May 2003
- Instruction Set Manual 07.2000

Note: Devices marked with EES- or ES are engineering samples which may not be completely tested in all functional and electrical characteristics, therefore they should be used for evaluation only.

The specific test conditions for EES and ES are documented in a separate Status Sheet.

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1 History List/Change Summary

(since last CPU Step ES-BA, previous Errata Sheet V1.0)

Table 1 Functional Deviations

Functional Deviation	Short Description	Fixed in Step	Change
CCU.2	T12 Shadow Transfer for Phase Delay Function.		
ADC.1	Selection of ADC conversion by hardware by just writing a '1' to 'CCU_ADEX' bit does not work.		
SYS.2	Brownout (BO) threshold level is too low		New

Table 2 AC/DC Deviations

AC/DC Deviation	Short Description	Fixed in Step	Change
None			

Table 3 Application Hints

Application Hint	Short Description	Fixed in Step	Change
PD.H1	After wakeup from power down PLL might unlock if oscillator startup is long.		Updated

2 Functional Deviations

CCU.2: T12 Shadow Transfer for Phase Delay Function

In Hall mode (T12MSELx = '1001'), T12 never reaches its period value in normal operation because a detected hall event on CCPOSx captures the actual T12 count value to CC60R (speed reference) and **resets T12**. But this period event is needed to trigger the shadow transfer of T12 register, i.e. an update of the timer registers (e.g. CC61R as variable phase delay) is not possible. The shadow transfer should be triggered together with the reset event of T12.

Workaround:

The shadow registers of T12 are transparent if the timer is stopped and if the shadow transfer is enabled (STE12=1). Therefore it is possible to write the new value to the shadow registers by enabling the shadow transfer, stopping T12 and starting T12 again. This is equivalent to a hardware triggered shadow transfer event. Inevitably, some clocks for the capture/compare events are lost in between the stop / start operation. It has to be noted that bit STE12 is cleared by hardware after a shadow transfer event.

ADC.1: Selection of A/D conversion by hardware by just writing a ‘1’ to CCU_ADEX bit does not work.

Selection of A/D conversion by hardware by just writing a ‘1’ to CCU_ADEX does not work. The analog input channel selection can only be latched when ‘ADST’ bit is set. So during hardware trigger mode, ‘ADST’ needs to be ‘1’ to select the input channel and ‘CCU_ADEX’ needs to be ‘1’ to select the conversion to be started by T13 period match event. Please note that when ‘ADST’ and ‘CCU_ADEX’ are both set at the same time (in one instruction), conversion is started by hardware. In case ‘ADST’ is set before ‘CCU_ADEX’, conversion is started immediately by software.

Workaround:

In software, set ‘ADST’, ‘CCU_ADEX’ at the same time together with the desired input channel selection to enable conversion triggered by T13PM. For example,

```
MOV ADCON0, #8CH     ; enable hardware triggered conversion for channel 4
```

SYS.2: Brownout (BO) threshold level is too low

The brownout (BO) threshold level is too low for a safe operation. It cannot be guaranteed that the device is working correctly down to such a low voltage. Thus the use of this feature is not encouraged. It must be kept disabled at all time by ensuring that bit SFR PMCON0.4 (EBO bit) is written with 0 only.

The brownout detection section will be removed from future documentations.

Workaround:

None.

3 Deviations from Electrical- and Timing Specification

No deviations from the Electrical- and Timing Specification are known for this step.

4 Application Hints

PD.H1: After wakeup from power down PLL might unlock if oscillator startup is long.

In the User's Manual, it is stated that there will a period of start-up phase before PLL starts locking. Conversely, PLL starts to lock even during the start-up phase. And once the lock detection circuit has output an 'OK' signal, the program will start running. However, due to instability of start-up phase and inadequate lock detection period of 4096 clocks (153 us @ 10.67 MHz), PLL might unlock and generate a PLL-reset. This will cause a rebooting if BSL mode is enabled and therefore the wakeup process is corrupted.

Note: This application hint is renamed as PD.H1

Workaround:

Use a ceramic resonator instead of a crystal with a fast oscillator startup phase.

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