Microcontrollers

Errata Sheet

11 June 2001 / Release 1.3

Device:	**C508-4R**
Stepping Code / Marking:	**ES-AA**
	AA
Package:	**P-MQFP-64**
	P-SDIP-64

This Errata Sheet describes the deviations from the current user documentation. The classification and numbering system is module oriented in a continual ascending sequence over several derivatives, as well already solved deviations are included. So gaps inside this enumeration could occur.

The current documentation is: Data Sheet 08.00
User's Manual 11.99
Instruction Set Manual 05.98

Note: ***Devices marked with EES- or ES are engineering samples which may not be completely tested in all functional and electrical characteristics, therefore they should be used for evaluation only.***

The specific test conditions for EES and ES are documented in a separate Status Sheet.

Change summary to the last Errata Sheet Rel. 1.2:

- New items ADC.1 and ADC.2.

Functional Problems:

ADC.1: The upper limit for f_{ADC} is increased from 2MHz to 5MHz

The ADC conversion clock f_{ADC} is to be adjusted such that the resulting f_{ADC} is less than or equal to 5MHz, instead of 2MHz as currently specified.

Workaround:

None. This new upper limit will be included in future documentation updates.

ADC.2: A/D Converter Clock Prescaler Ratio is not as defined in documentation

The prescaler ratio for the A/D conversion clock is not as defined on the User's Manual page 6-118. The effective prescaler ratio is as follows:

ADCL1	ADCL0	Prescaler Ratio
0	0	Divide by 4
0	1	Divide by 4
1	0	Divide by 8
1	1	Divide by 8

Workaround:

None.

EH.2: In Emulation Mode, PLL may be bypassed when P5.7 goes low

When P5.7 goes low due to an instruction or is being pulled low on entry into and during the emulation mode on an emulator, the PLL operation may be bypassed resulting in the system clock being the same as the applied input at XTAL1. This is instead of the expected doubled system clock frequency. In this case, the micro-controller and its peripheral units are running at half the frequency intended, such as the ALE frequency is halved.

Workaround:

Pin P5.7 and its alternate function as INT7 must not be used during emulation. The pin must always be held at high throughout emulation.

WDT.2: Typing Error on the Reset Value of Watchdog Timer

In the User's Manual, on page 3-14 and page 8-2, the reset value for the High Byte of Watchdog Timer (WDTH) should be $X0000000_B$ (in binary form).

Workaround:

None. This will be updated in the next versions of the documentation.

CCU.5: The Phase Delay Timer is no longer a feature of the Capture/Compare Unit of the C508

The phase delay timer of the CCU is no longer a feature of the C508. Previous items relating to the phase delay timer are to be ignored. The C508 User's Manual and Data Sheet will be updated and excludes the phase delay timer. Bit 6 of SFR COTRAP is now a reserved bit and must remain cleared always. Writing a '1' to this bit is prohibited.

Workaround:

None.

Deviation from Electrical- and Timing Specification:

DC.1: Increased the Input High voltage, V_{IH}, for Port 4

Port 4 is the input port to the A/D converter and can be used for digital input. For using as digital input port, the input high voltage (V_{IH}) should be higher than 4.5V in order to be recognized as an input logic high level.

It should be noted that this would not affect the A/D converter function at Port 4.

Workaround:

Use driving buffer at the port input pins for digital input.

DC.2: ± 3 LSB total unadjusted error (TUE) of A/D converter

The total unadjusted error of the A/D converter does not meet the specified value of the DC characteristics. The value for TUE is limited as follows:

$$TUE = \pm 3 \text{ LSB} \quad \text{in the } V_{IN} \text{ range :} \quad V_{SS} < V_{IN} < V_{CC}$$

Workaround:

None.

DC.3: The Test Condition for I_{TL} Parameter is not as Specified in Documentation

The test condition for I_{TL} is at V_{IN}=2.2V, instead of 2V as specified in the documentation.

Workaround:

None.

DC.4: The Minimum Limit of the Input High Voltage V_{IH} Parameter is Higher

The minimum limit of the Input high voltage V_{IH} parameter is higher than specified in the documentation. The value for the minimum limit is:

$$V_{IH} = 0.2\ V_{DD} + 1.1$$

Item DC.1 above is still valid.

Workaround:

None.

History List (since CPU Step ES-AA)

Functional Problems

Functional Problem	Short Description	Fixed
ADC.1	The upper limit for f_{ADC} is increased from 2MHz to 5MHz	
ADC.2	A/D Converter Clock Prescaler Ratio is not as defined in documentation	
EH.2	In Emulation Mode, PLL may be bypassed when P5.7 goes low	
WDT.2	Typing Error on the Reset Value of Watchdog Timer	
CCU.5	The Phase Delay Timer is no longer a feature of the Capture/Compare Unit of the C508	

AC/DC Deviations

AC/DC Deviation	Short Description	Fixed
DC.1	Increased the Input High voltage, V_{IH} , for Port 4	
DC.2	$\pm$ 3 LSB total unadjusted error (TUE) of A/D converter	
DC.3	The Test Condition for I_{TL} Parameter is not as Specified in Documentations	
DC.4	The Minimum Limit of the Input High Voltage V_{IH} Parameter is Higher	

Application Support Group, Singapore