Microcontrollers

Errata Sheet

29 June 2001 / Release 1.8

Device:	**C508-4E**
Stepping Code / Marking:	**ES-AA**
	AA
Package:	**P-MQFP-64**
	P-SDIP-64

This Errata Sheet describes the deviations from the current user documentation. The classification and numbering system is module oriented in a continual ascending sequence over several derivatives, as well already solved deviations are included. So gaps inside this enumeration could occur.

The current documentation is: Data Sheet 08.00
User's Manual 11.99
Instruction Set Manual 05.98

Note: ***Devices marked with EES- or ES are engineering samples which may not be completely tested in all functional and electrical characteristics, therefore they should be used for evaluation only.***

The specific test conditions for EES and ES are documented in a separate Status Sheet.

Change summary to last Errata Sheet Rel. 1.7:

- New item numbered OTP.1.

Functional Problems:

ADC.1: The upper limit for f_{ADC} is increased from 2MHz to 5MHz

The ADC conversion clock f_{ADC} is to be adjusted such that the resulting f_{ADC} is less than or equal to 5MHz, instead of 2MHz as currently specified.

Workaround:

None. This new upper limit will be included in future documentation updates.

ADC.2: A/D Converter Clock Prescaler Ratio is not as defined in documentation

The prescaler ratio for the A/D conversion clock is not as defined on the User's Manual page 6-118. The effective prescaler ratio is as follows:

ADCL1	ADCL0	Prescaler Ratio
0	0	Divide by 4
0	1	Divide by 4
1	0	Divide by 8
1	1	Divide by 8

Workaround:

None.

INT.1: Contents of SFR EINT cannot be read correctly

Reading of SFR EINT (address FBH) causes data corruption in the register. It is not recommended to read the contents of EINT register.

Workaround:

SFR EINT holds the interrupt edge flags and the rising/falling edge control flags for external interrupts 7 to 9. If it is necessary for the application to read this register, then the application software can declare a shadow register to SFR EINT. This shadow register must be updated each time SFR EINT is written. To retrieve the contents of SFR EINT, the shadow register is read instead.

INT.2: SFR EINT does not support all addressing modes

Writing data to SFR EINT (address FBH) can only be done by using Immediate Addressing mode or Register Addressing mode.

Workaround:

In order to set the interrupt rising/falling edge control flags of SFR EINT for external interrupts 7 to 9, the Immediate Addressing mode or Register Addressing mode should be used.

For example:
Using Immediate Addressing Mode,

```
MOV   EINT, #data
```

Using Register Addressing Mode,

```
MOV   A, #data
MOV   EINT, A
```

If Direct Addressing Mode has to be used, it is suggested as below:

```
MOV   direct, #data     ; where 'direct' is the memory address
MOV   A, direct
MOV   EINT, A
```

WDT.1: Watchdog Timer is not halted in Idle Mode

The Watchdog Timer (WDT) is not halted in the idle mode as defined. However, during the idle mode, an overflow condition of the WDT does not initiate an internal reset. In such a case the WDT starts a new count sequence.

Workaround:

1. Do not use the Watchdog Timer function in combination with the idle mode.
2. In case of WDT is running before entry into idle mode, to avoid a WDT initiated reset upon exit of the idle mode, the following methods can be used.

(A) The WDT is refreshed immediately upon exit from idle mode.

(B) A timed interrupt can be used to exit the idle mode before the WDT reaches the counter state 7FFCh. This can be achieved by using Timer 0, 1 or 2. This timer can be programmed to generate an interrupt at a WDT counter state prior to overflow, for e.g., at 7F00h. Prior to entering idle mode, the WDT can be refreshed and the timer 0, 1or 2 can be started immediately to synchronize the WDT. In the interrupt service routine of the Timer 0, 1 or 2, the WDT must be refreshed. If required, idle mode could be entered once again.

WDT.2: Typing Error on the Reset Value of Watchdog Timer

In the User's Manual, on page 3-14 and page 8-2, the reset value for the High Byte of Watchdog Timer (WDTH) should be $X0000000_B$ (in binary form).

Workaround:

None. This will be updated in the next versions of the documentation.

CCU.1: The PWM is Output on CCx pins instead of COUTx during the Rotate Left 0° Phase Shift mode

In the Block Commutation mode, the Rotate Left at 0° Phase Shift mode (user's manual page 6-88) can be selected by the three control bits (BCM1=1, BCM0=0 and BCTSEL=1). During this 0° phase shift mode, the PWM signal is output on CCx pins instead of COUTx pins if the modulation mode is selected.

Workaround:

None.

CCU.2: The CT1 output signal inversion in burst and block commutation is also controlled by the initial value of COUT3

The function description for the control bit COUTXI in SFR COINI (on page 6-69 of User's Manual) is true only if the initial value of COUT3 is set to 1. The complete function description should be:

Bit	Function
COUTXI	**Compare Timer 1 output signal inversion in burst and block commutation** Initial value of COUT3 = 1: When COUTXI is set, the output signal of Compare Timer 2 which is wired to the compare outputs COUTx (x = 0-2) in burst or block commutation mode is inverted. When COUTXI is cleared, no inversion at the compare outputs. Initial value of COUT3 = 0: When COUTXI is set, no inversion at the compare outputs. When COUTXI is cleared, the output signal of Compare Timer 2 which is wired to the compare outputs COUTx (x = 0-2) in burst or block commutation mode is inverted.

Workaround:

None.

CCU.3, CCU.4: The Phase Delay Timer is no longer a feature of the Capture/Compare Unit of the C508

The phase delay timer of the CCU is no longer a feature of the C508. Previous items relating to the phase delay timer are to be ignored. The C508 User's Manual and Data Sheet will be updated and excludes the phase delay timer. Bit 6 of SFR COTRAP is now a reserved bit and must remain cleared always. Writing a '1' to this bit is prohibited.

Workaround:

None.

EH.1: In Emulation Mode, the device may not work properly with the Emulator at the crystal frequency higher than 8 MHz.

In Emulation Mode, the device may not work properly with Emulator for the crystal frequency range greater than 8MHz. This commonly results to missing some interrupt responses from the Emulator.

It should be noted that this would not affect the functions of C508 device for full speed (10MHz) operation in normal mode.

Workaround:

Use crystal frequency less than or equal to 8MHz for Emulation Mode.

OTP.1: OTP module may fail under special conditions, leading to undefined operation

The OTP module may malfunction, causing the chip to enter an undefined state with unsteady operation, if there is a remaining voltage at the V_{DD} pin before powering up. The critical remaining voltage is approximately 100-400mV. The undefined state can only be left by a complete power off (V_{DD}=0V) and not by any RESET-source (e.g. hardware reset, WDT-reset). The problem is due to variation in technology and manufacturing parameters.

Workaround:

The device should always be powered up from V_{DD}=0V, ensuring that there is no voltage at any pins which leads to a remaining voltage level at V_{DD} pin (coupling over the ESD-structure).

Deviation from Electrical- and Timing Specification:

None.

History List (since last CPU Step ES-AA)

Functional Problems

Functional Problem	Short Description	Fixed
ADC.1	The upper limit for f_{ADC} is increased from 2MHz to 5MHz	
ADC.2	A/D Converter Clock Prescaler Ratio is not as defined in documentation	
INT.1	Contents of SFR EINT cannot be read correctly	
INT.2	SFR EINT does not support all addressing modes	
WDT.1	Watchdog Timer is not halted in Idle Mode	
CCU.1	The PWM is Output on CCx pins instead of COUTx during the Rotate Left 0° Phase Shift mode	
CCU.2	The CT1 output signal inversion in burst and block commutation is also controlled by the initial value of COUT3	
CCU.3, CCU.4	The Phase Delay Timer is no longer a feature of the Capture/Compare Unit of the C508	
EH.1	In Emulation Mode, the device may not work properly with the Emulator at the crystal frequency higher than 8 MHz.	
OTP.1	OTP module may fail under special conditions, leading to undefined operation	

AC/DC Deviations

AC/DC Deviation	Short Description	Fixed
	None	

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