SIEMENS

Microcomputer Components
Technical Support Group Munich
HL MCB AT1

Errata Sheet

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Device : **SAB 80C517A**

Marking : **BE**

These parts of the SAB 80C517A can be identified by the letters "BE" below the part number. The parts are mounted in Plastic Leaded Chip Carrier (P-LCC-84) or in a Plastic Metric Quad Flat Pack (P-MQFP-100-2) package.

This errata sheet describes both the *functional problems* (see part 1) and the *deviations from the electrical and timing specifications* (see part 2) known in this step.

If a problem was already introduced with an errata sheet of an earlier step, its initial number is still retained in this errata sheet. Thus, the numerical order of the problems described in the following may contain gaps.

At the end of this document, you will find two history tables showing the problems found in the SAB 80C517A up to now. Changes to the last revision are shaded light grey in the history tables.

1) Functional Problems

The following malfunctions are known in this step:

Problem 8: Oscillator Watchdog

The problem might occur only at external clock rates below 10 MHz (2.5 MHz ≤ fosc < 10 MHz). For all other specified clock rates (10 MHz ≤ fosc ≤ 18 MHz) this problem cannot occur.

Conditions:

The oscillator watchdog is enabled by OWE = 1. The Oscillator Watchdog is activated by

- a fast internal reset after power on or
- a restart from hardware- or software power down mode or
- a short drop of the external clock source below the specified minimum clock rate of fosc = 2.5 MHz (e.g. in case of a short lost connection of the crystal).

The part then enters the specified reset state until the external clock source becomes stable.

Failure:

In the moment when the clock system switches over from the internal RC-oscillator to the external clock source, a spike at the internal clock system might occur. This might create an undefinded behaviour of the controller when starting up program execution (e.g. the program execution will not start at the defined reset address 0000H).

Note: A **hardware activated** watchdog timer (PE#/SWD = 1) can reset the system when missing the corresponding refresh-sequence and therefore restart the system correctly.

Problem 9: ROM Verification Mode 1

In this step the ROM Verification Mode 1 is not stable at the specified voltage range from 5V ± 5% at T = 25^{O}C ± 5^{O}C and therefore should not be used.

Workarounds:

1. Reading out by MOVC instructions in the upper code space

ROM data can be read by an external executed MOVC instruction. The program sequence has to be located in the upper code space (PC ≥ 8000H, EA# = 1).

For example a possible scheme of generating a ROM verification software could be:

- set EA# pin to logic low level (external code memory is accessed).
- start external program execution at address 0000H by releasing the RESET signal.
- execute a LJMP instruction to external code address higher than 8000H.
- set EA# pin to logic high level (internal ROM can be accessed now).
- use MOVC instruction to read ROM data in address area 0000H - 7FFFH.

2.) Using ROM Verification Mode 2

ROM data can be verified by using the ROM Verification Mode 2 as specified

2) Electrical- and Timing-Spec. Deviations

The following deviations of electrical and timing parameters from the specification are known in this step:

Problem 8: f_{OSC}, Minimum Limit Value

If internal oscillator watchdog is enabled (OWE = 1), the minimum oscillator frequency is restricted to 2.5 MHz (2.5 MHz ≤ f_{OSC} ≤ 18 MHz).

Note:

When using an external oscillator circuit with 1MHz ≤ f_{OSC} ≤ 2.5 MHz, the enabled internal ocillator watchdog might initiate an internal reset.

Functional Problem No.	Marking	Description	Remarks
9	BE, ES-BE, BD	ROM Verification Mode 1	
8	BE, ES-BE, BD	Oscillator Watchdog	
7	BD	Entering the Hardware Power Down Mode	fixed in ES-BE and later
6	BD, ES-BD	Start of Watchdog-Timer	fixed in ES-BE and later
5	BC	Port0/Port2, XRAM Access Using DPTR	fixed in ES-BD and later
4	BC	Set/Reset-Mode with Timer 2 and Port 5	fixed in ES-BD and later
3	BC	CMx Registers Assigned to Timer 2 - Compare Mode 1	fixed in ES-BD and later
2	ES-BB	ADC, Prescaler Bit Problem	fixed in ES-BC and later
1	ES-BB	ADC, Busy-Bit/IADC-Bit Problem	fixed in ES-BC and later

Table 1: History of Functional Problems

Electrical- / Timing-Problem No.	Marking	Description	Remarks
8	BE, ES-BE, BD, ES-BD	f_{OSC}, Minimum Limit Value	
7	BC	Power Supply Current in Hardware Power Down Mode	fixed in ES-BD and later
6	BD, ES-BD, BC, ES-BC, ES-BB	Input Low Current PE#/SWD, OWE, IIL4	changed in Data Sheet 11.92
5	BD, ES-BD, BC, ES-BC, ES-BB	Input Low Current XTAL2, IIL3	changed in Data Sheet 11.92
4	BD, ES-BD, BC, ES-BC, ES-BB	Logic 0 Input Current, IIL	changed in Data Sheet 11.92
3	ES-BB	Input High Level at analog/digit. Inputs	fixed in ES-BC and later
2	ES-BA	Hardware Power Down Mode	fixed in ES-BC and later
1	ES-BA	Restricted Operating Conditions	fixed in ES-BC and later

Table 2: History of Electrical- and Timing-Spec. Deviations