SIEMENS

Microcomputer Components
Technical Support Group Munich
HL MCB AT1

# Errata Sheet

December 05, 1995 / Release 1.5

**Device :** **SAB-C509-L**

**Marking :** **BB**

These parts of the SAB-C509-L can be identified by the letters "BB" below the part number. The SAB-C509-L, BB is mounted in a Plastic Metric Quad Flat Pack (P-MQFP-100-2) package.

This errata sheet describes both the *functional problems* (see part 1) and the *deviations from the electrical and timing specifications* (see part 2) known in this step.

If a problem was already introduced with an errata sheet of an earlier step, its initial number is still retained in this errata sheet. Thus, the numerical order of the problems described in the following may contain gaps.

At the end of this document, you will find two history tables showing the problems found in the SAB-C509 up to now. Changes to the last revision are shaded light grey in the history tables.

# 1) Functional Problems

The following malfunctions are known in this step:

### Problem 6: Oscillator Watchdog

When leaving an activated oscillator watchdog reset the following problem might occur:

**Conditions:**

If the oscillator watchdog is enabled by OWE = 1, the oscillator watchdog reset can be activated by:

a.) a "fast internal reset" after power on

b.) a restart from hardware power down mode

c.) a restart from software power down mode

d.) a short drop of the external clock source below the specified minimum clock rate of fosc = 2.5 MHz (e.g. in case of a short lost connection of the crystal)

The part then enters the oscillator watchdog reset until the external clock source becomes stable.

**Failure:**

When the clock system switches from the internal RC-oscillator to the external clock source, a spike at the internal clock system might occur. This spike creates an undefinded behaviour of the controller when starting program execution (e.g. the program execution will not start at the defined reset address 0000H).

**Workaround:**

a.) Using the "fast internal reset after power on" feature:

The external reset signal needs to be delayed to a stable Vcc for a minimum period of 10 ms. In this case the external oscillator gets enough time for an stable oscillation and when releasing the external reset signal, the internal clock spike cannot occur.

b.) Termination of the Hardware Power Down Mode (HWPD):

A termination of the HWPD-mode without the possibility of the generation of a clock spike can only be avoided by activating the external reset signal for a minimum period of 10 ms. During this time, the HWPD-signal has to be deactivated to prevent a new entering of the HWPD-mode after releasing the reset signal.

c.) Termination of Software Power Down Mode (SWPD):

see a.).

d.) A short drop of the external clock source:

No workaround possible

## Problem 7: MDU-Error Flag Mechanism

The error flag mechanism in the MDU is not functional in this step and therefore the error flag MDEF (ARCON.7) should not be used.

**Workaround:**

The multiplication, division, normalize or shift left/right operations will work correctly if a once started operation was not disturbed by any read/write operation to the registers MD0, MD1, MD2, MD3, MD4, MD5, or ARCON before it was terminated (e.g. by a interupt routine).

## Problem 13: Write to SFR DIR2

Any write access to SFR DIR2 (A0H) causes a simultaneous write access to SFR XPAGE (91H)

**Workaround:**

After each write to SFR DIR2, the SFR XPAGE has to be rewritten with the former page address.

## Problem 14: Undefined Reset Values of Datapointers 1-7

For this step the reset values in the datapointer registers DPL1 - DPL7 (82H) and DPH1 - DPH7 (83H) are undefined. The datapointer registers DPL0 and DPH0 are not affected (specified reset values are 00H).

**Workaround:**

Before using the datapointer registers DPL1 - DPL7 and DPH1 - DPH7 this registers has to be inialized with the user specified values.

## Problem 15: Bidirectional Port Structure at Port 0 during external memory access

**Conditions:** - the bidirectional portstructure is selected by bit PMOD =1 (SYSCON.6) and the direction register DIR0 of Port 0 is set to the output mode (DIR0 = 00H).

When performing an external access to the program or data memory (EA# = 0), the driven address low output voltage level at port 0 by FET n1 is influenced by the simultaneously switched-on FETs p2 and p3. Therefore the address low output voltage level at port 0 is typically above 1V.

**Workaround:**

When setting the DIR0 register to FFH (reset value) into the input mode in the bidirectional portstructure, the problem will not occur.

## Problem 16: Slow-Down Mode

The Slow-Down Mode is not tested in this step and therefore should not be used.

## Problem 17: Reset-Values at A/D Converter SFR´s

**Failure:**

The four A/D Converter SFR´s ADCON0 (D8H), ADCON1 (DCH), ADDATH (D9H) and ADDATL (DAH) might not be set to their predefined reset values after a reset.

**Workaround:**

After a reset the four SFR´s should be initialized by SW with their specified reset values (ADCON0 (D8H), ADDATH (D9H) and ADDATL (DAH) = 00H; ADCON1 (DCH) = 01000000B).

## Problem 18: Timer 0/1 Overflow Bits TF0/TF1

**Conditions:**

Timer 0/1 operate in timer mode (C/T-bits are not set in SFR TMOD ($89_H$)).

**Failure:**

When the overflow bits TF0 and TF1 are used for interrupt generation, it might happen that the corresponding interrupt flag TF0/TF1 will not be cleared by hardware when the interrupt routine is entered. In this cases, the interrupt routine might be executed several times.

**Workaround:**

Additionally clearing the overflow bits TF0 and TF1 by software in the corresponding timer0/1 interrupt service routine (but not as the first instruction) will solve the problem.

e.g.: CSEG AT TIMER0 ($0B_H$)

```
        NOP         ; this is the first instruction in the timer 0 overflow interrupt service routine
                    ; instead of NOP this can be the first instruction of the customer SW
        CLR TF0     ; clear overflow bit TF0 in the SFR TCON (88H)
        ...         ; customer specified SW
        RETI        ; return from interrupt
```

## Problem 19: Start of Compare Timer 1

When starting the Compare Timer 1 by an initial write instruction to the mapped SFR reload register CT1RELL ($DE_H$), the SFR IRCON2 ($BF_H$) might be erroneously influenced.

**Workaround:**

Before starting the Compare Timer 1 the compare/capture event interrupt should be disabled by clearing bit ECC1 in SFR IEN3 ($BE_H$) . After starting the Compare Timer 1 the SFR IRCON2 ($BF_H$) should be written with its reset value $00_H$. Further, the compare/capture event interrupt is enabled by setting the bit ECC1 in SFR IEN3 (BEH).

## Problem 20: Modulation Range in CM0 with the Compare Timers 0/1

**Conditions:**

The compare timers (0/1) are used in a Compare Mode 0 (CM0) configuration. The corresponding compare registers CMx are equal to the compare timer reload registers.

**Failure:**

In this configuration the corresponding compare output(s) might not be set permanently to a constant high level but show a low level for maximum 1 compare timer clock period. Therefore, a maximum modulation range up to 100% cannot be achieved as specified.

## Problem 21: Normalizing with the MDU

**Conditions:**

The Multiplication/Division Unit (MDU) performs a normalize operation and the overflow flag MDOV in SFR ARCON ($EF_H$) is used for detection of the MSB MD3.7 in SFR MD3 ($EC_H$).

**Failure:**

When performing a normalizing operation with the MSB MD3.7 set in SFR MD3 ($EC_H$), the overflow flag MDOV in SFR ARCON ($EF_H$) might be not set erroneously by the HW.

**Workaround:**

If MD3.7 bit in SFR MD3 ($EC_H$) is set before the normalize operation, the overflow flag MDOV has to be set by the corrective SW after having finished the normalize operation by the MDU.

## Problem 22: Timer 2 - Compare Mode 2

**Conditions:**

The Compare/Capture Unit is used for the concurrent compare output at P5 in compare mode 2 with timer 2. The SFR registers COMSETL ($0A1_H$) / COMSETH ($0A2_H$) and COMCLRL ($0A3_H$) / COMCLRH ($0A4_H$) are set to identical values.

**Failure:**

If a set and reset request occurs at the same time (identical values in SFR´s COMSET and COMCLR), it might happen that a low spike occurs at port 5 although the set operation should take precedence in this case.

**Note:**

Do not use identical values for the SFR´s COMSET / COMCLR while using the compare mode 2.

## Problem 23: Reset-Values at Timer 2 SFR´s

**Failure:**

The timer 2 module related SFR´s might not be set to their predefined reset values after a reset. The following SFR´s are concerned:
CCEN, CC4EN, CCH1 ... CCH4, CCL1 ... CCL4, CMEN, CMH0 ... CMH7, CML0 ... CML7, CMSEL, CRCH, CRCL, COMSETL, COMSETH, COMCLRL, COMCLRH , SETMSK, CLRMSK, CTCON, CTRELH, CTRELL, TH2, TL2, T2CON.

**Workaround:**

After a reset the above listed SFR´s should be initialized by SW with their specified reset values.

## Problem 24: Port 0 write instructions during external program execution

**Description:**

When an instruction is used during external program memory execution which has port 0 as destination (e.g. MOV P0,A), wrong program code can be executed.

**Workaround :**

No usage of instructions which write data to port 0.

## 2) Electrical- and Timing-Spec. Deviations

The following deviations of electrical and timing parameters from the specification are known in this step:

### Problem 1: Restricted Duty Cycle of the External Clock Drive XTAL2

The specified duty cycle variation of the oscillator clock from 0.4 to 0.6 at CPU clock = 16 MHz is not met. The duty cycle of the external clock drive XTAL2 for this step is restricted from 0.45 to 0.55 at CPU clock = 16 MHz.

### Problem 2: Restricted Accuracy of AD-Converter

The specified Total Unadjusted Error (TUE $\leq \pm$ 2 LSB) for the AD-converter is not met. The TUE for this step is restricted to TUE $\leq \pm$ 2,5 LSB.

### Problem 3: Restricted Voltage Supply Vcc

The specified voltage supply range of Vcc = 5V +10%, - 15% is restricted for this step to Vcc = 5V +10%, - 5% (4.75V $\leq$ Vcc $\leq$ 5.5V).

### Problem 4: Restricted Capacity Load Conditions

The capacity load conditions in the AC characteristics are restricted for this step to $C_L$ = 30 pF for port 0, ALE, PSEN# and all other outputs.

**Note:**

When using the specified capacity load conditions $C_L$ for port 0, ALE , PSEN# = 100 pF and $C_L$ for all other outputs = 80 pF, the following program memory characteristics has to be modified:

- ALE to valid instruction in: $t_{LLIV}$ = 2CLP - 70 ns
- PSEN#/RDF# to valid instruction in: $t_{PLIV}$ = CLP + $TCL_{Hmin}$ - 70 ns
- Address to valid instruction in: $t_{AVIV}$ = 2CLP + $TCL_{Hmin}$ - 75 ns

### Problem 5: Input Hysteresis for CMOS Ports

The input hysteresis for the CMOS ports 1, 3, 4, 5, 6, 7, 8, and 9 of minimum 0.1 V is not met for this step.

| Functional Problem No. | Marking | Description | Remarks |
|---|---|---|---|
| 1 | ES-AA | XRAM access via SFR XPAGE/P2 | fixed in ES-AB and later |
| 2 | ES-AA, ES-AB | External access to Data Memory | fixed in ES-BB and later |
| 3 | ES-AA | Baudrate Generator of Serial Interface 0 | fixed in ES-AB and later |
| 4 | ES-AA, ES-AB | Reset Value of SFR EICC1 | fixed in ES-BB and later |
| 5 | ES-AA | Pin PRGEN | fixed in ES-AB and later |
| 6 | ES-AA, ES-AB, ES-BB, BB | Oscillator Watchdog<br>(replaces HWPD-Reset) | |
| 7 | ES-AA, ES-AB, ES-BB, BB | MDU-Error Flag Mechanism | |
| 8 | ES-AA, ES-AB | Bootstrap-Loader SW-Problem | fixed in ES-BB and later |
| 9 | ES-AA | Emulation Mode | fixed in ES-AB and later |
| 10 | ES-AA, ES-AB | Serial Interface 0 (USART) in 9-bit modes 2 and 3 - Incorrect RB80 reception | fixed in ES-BB and later |
| 11 | ES-AA, ES-AB | Serial Interface 0 (USART) in 8-bit mode 1 - Incorrect RB80 reception | fixed in ES-BB and later |
| 12 | ES-AA, ES-AB | Serial Interface 1 (USART) in 9-bit mode A or 8-bit mode B - Incorrect RB81 reception | fixed in ES-BB and later |
| 13 | ES-AA, ES-AB, ES-BB, BB | Write to SFR DIR2 | |
| 14 | ES-AA, ES-AB, ES-BB, BB | Undefined Reset Values of Datapointers 1-7 | |
| 15 | ES-AA, ES-AB, ES-BB, BB | Bidirectional Port Structure at Port 0 during external memory access | |
| 16 | ES-AA, ES-AB, ES-BB, BB | Slow-Down Mode | |
| 17 | ES-AA, ES-AB, ES-BB, BB | Reset Values at A/D Converter SFR´s | |

| | | | |
|---|---|---|---|
| 18 | ES-AA, ES-AB, ES-BB, BB | Timer 0/1 Overflow Bits TF0/TF1 | |
| 19 | ES-AA, ES-AB, ES-BB, BB | Start of Compare Timer 1 | |
| 20 | ES-AA, ES-AB, ES-BB, BB | Modulation Range in CM0 with the Compare Timers 0/1 | |
| 21 | ES-AA, ES-AB, ES-BB, BB | Normalizing with the MDU | |
| 22 | ES-AA, ES-AB, ES-BB, BB | Timer 2 - Compare Mode 2 | |
| 23 | ES-AA, ES-AB, ES-BB, BB | Reset Values at Timer 2 SFR´s | |
| 24 | ES-AA, ES-AB, ES-BB, BB | Port 0 write instructions during external program execution | |

Table 1: History of Functional Problems

| Electrical- / Timing-Problem No. | Marking | Description | Remarks |
|---|---|---|---|
| 1 | ES-AA, ES-AB, ES-BB, BB | Restricted Duty Cycle of the External Clock Drive XTAL2 | |
| 2 | ES-AA, ES-AB, ES-BB, BB | Restricted Accuracy of the AD-Converter | |
| 3 | ES-AA, ES-AB, ES-BB, BB | Restricted Supply Voltage Vcc | |
| 4 | ES-AA, ES-AB, ES-BB, BB | Restricted Capacity Load Conditions | |
| 5 | ES-AA, ES-AB, ES-BB, BB | Input Hysteresis for CMOS Ports | |

Table 2: History of Electrical- and Timing-Spec. Deviations