Introduction to the simulation model PSpice

LITIX™ BASIC+ TLD1173-1ET

About this document

Scope and purpose

This document outlines the main features of LITIX™ BASIC+ TLD1173-1ET by means of its digital twin. The digital twin is the simulation model. In typical application setups, the simulation model aims to be an easy, time-efficient, and cost-effective solution for exploring device capabilities and integration into complex applications.

Intended audience

This application note, along with the simulation model itself, offers an interactive solution targeted at anybody who aims to explore the functionality and “what-if” scenarios for the LITIX™ BASIC+ TLD1173-1ET.

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1 Details of the delivery package

The package contains a complete setup for PSpice using the transient spice model for the Infineon TLD1173-1ET:

- `TLD1173-1ET_encrypted.lib`: Code source file (the model library is encrypted to protect Infineon IP)
- `TLD1173-1ET.olb`: Device symbol view for schematic graphical user interface
- Application test bench(es):
  - PWM_SC: This setup shows the short-circuit protection during ON and OFF states of a PWM signal applied on EN/DEN
- Additional files included in the package:
  - `LS_LR_E6xF_TRS.lib`: Red LED model library from Osram
  - `LS_LR_E6xF_TRS.olb`: Symbol view for schematic graphical user interface for red LED from Osram
  - `Infineon-PSpice-GettingStarted-AN-v01_00-EN.pdf`: This document provides more information on the simulation environment

***Note**: All model libraries are already configured, and the project is ready for use.*

2 Simulation model features

The simulation model enables you to:

- Perform transient simulations to observe and analyze the device's response to different stimuli with no limit on the number of stimuli and probes
- Measure the device's electrical parameters under typical conditions with increased precision at small resolution (for example, 100 ns/1 µV/1 µA)
- Integrate the simulation model into a complex application and explore new possibilities
- Obtain results quickly and accurately, without incurring any errors or damaging physical components. The simulation can also be run by anyone, including engineers and students, without risk of damage
- The simulation model allows you to explore the key features of the real device, including,
  - Power stage and regulation
  - Fault management
  - Thermal behavior including self-heating
- Simulate thermal behavior of real device, including accurate measurement of junction temperature and interactions between power transistors for multichannel devices. For more information, refer to Thermal behavior

To maintain the balance between usability and simulation speed, the simulation model does not cover all features of the real device. The following features are not included:

- Current consumption of the IC (a realistic power efficiency calculation is not possible)
- Electrostatic discharge simulation
- Electromagnetic compatibility simulation
- AC and DC simulation
- Monte Carlo analysis

***Note**: Convergence issues may occur when using the DC sources, steep ramps, or high-frequency sources within the setup.*

2.1 Thermal behavior

The simulation model contains two junction-to-ambient thermal networks associated with 2s2p and 1s0p footprint of PCB JEDEC standards (Figure 1). Optionally (on request), One junction-to-package thermal network that allows an external heat sink connection (Figure 2 and Figure 3) to be used for custom PCB cooling.

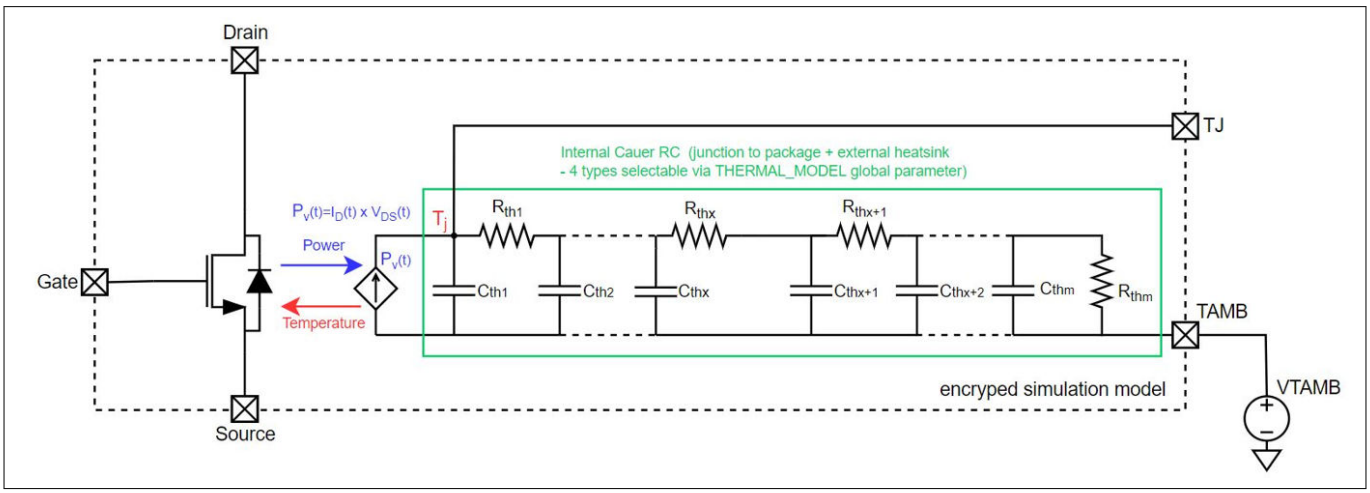

Figure 1 Junction-to-ambient thermal network concept schematic

2 Simulation model features

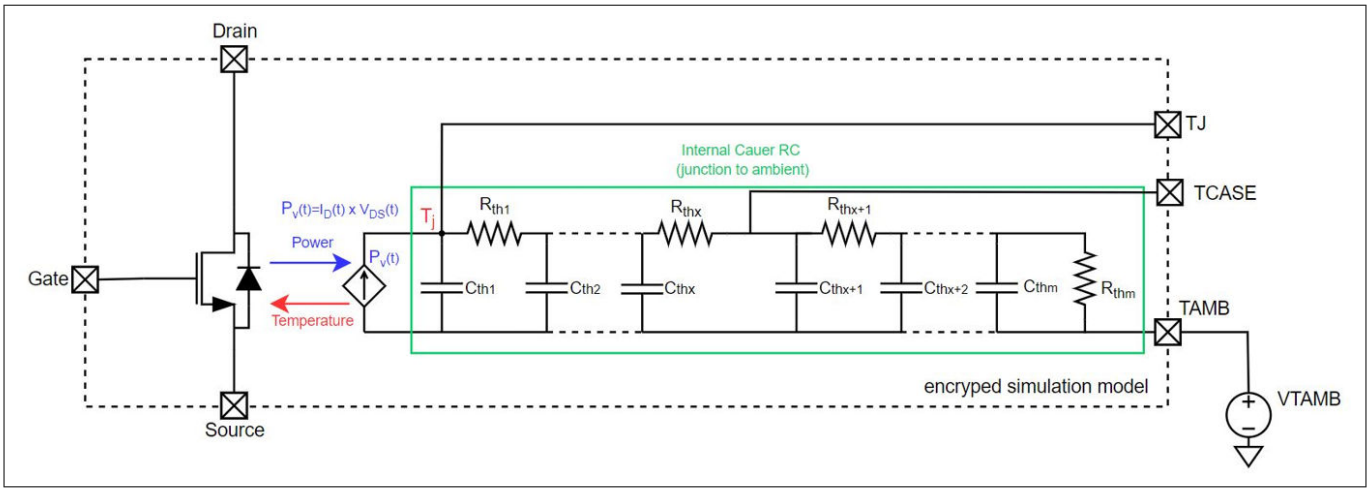

Figure 2 Junction-to-ambient thermal network with TCASE[1)] concept schematic (optional)

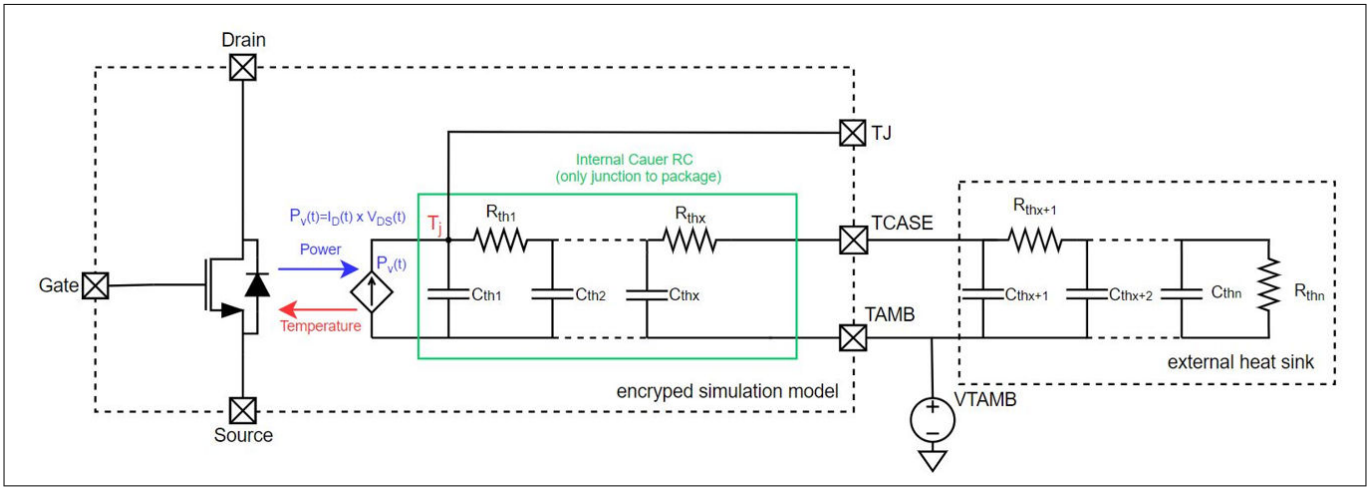

Figure 3 Junction-to-package thermal network concept schematic (optional)

To choose a PCB type, change the value of the THERMAL_MODEL parameter located next to the symbol of the device (refer to thermal model parameters) as follows:

- THERMAL_MODEL = 1: P = 1.5 W; T = 85°C; PCB type: 2s2p
- THERMAL_MODEL = 2: P = 1.5 W; T = 85°C; PCB type: 1s0p footprint
- THERMAL_MODEL = 0: P = 0 W; self-heating disabled, temperature control possible from TAMB only
- Optional[1)]: THERMAL_MODEL = 5: P = 1 W; T = 85°C; For junction-to-case thermal model, connect an external heat sink between TCASE and TAMB

Where,

P = Dissipated power on power transistor

T = Ambient temperature

For more information on global/local parameters, refer to the Getting Started file for the specific simulator included in the package.

1 Not applicable for all product simulation models

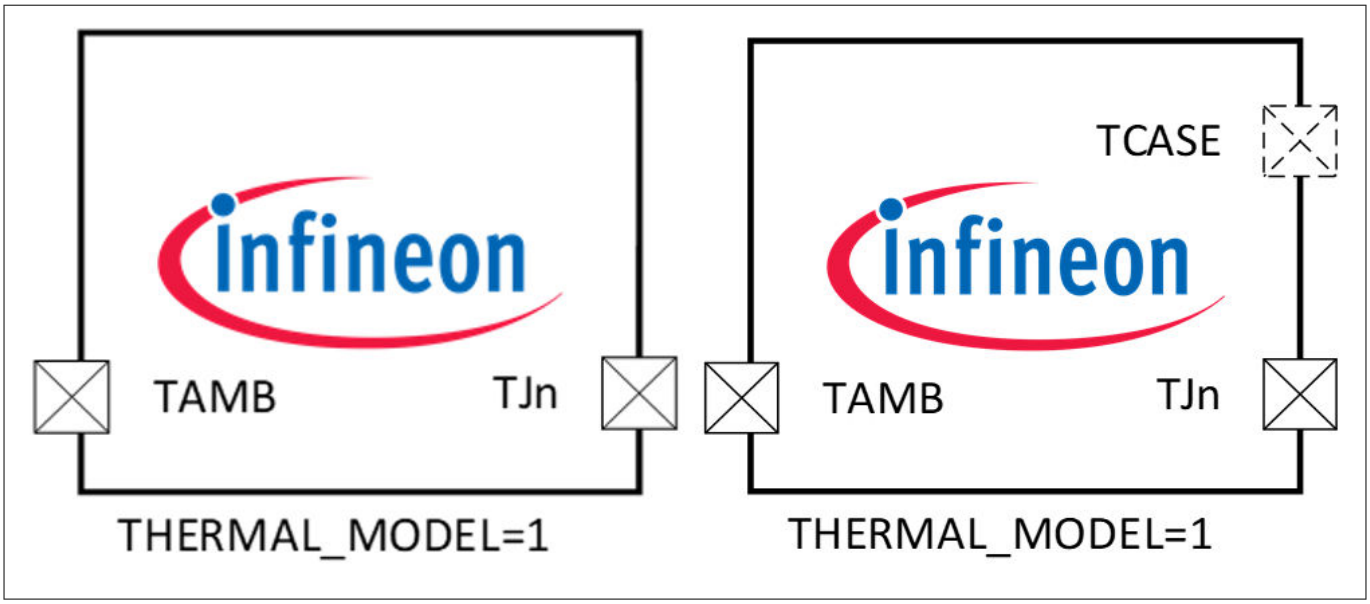

Figure 4 Thermal model parameter

The ambient temperature of the entire chip can be set by connecting a voltage source to the TAMB input pin. Note that modifying the simulation temperature via the TNOM parameter of the simulator does not influence in any way the provided simulation model.

The absolute temperature junction (T_{Ji}) is emulated as the sum of the ambient temperature (T_{AMB}), the temperature due to self-heating of the power stage (T_{PS}), and the influences of all the other channels in the case of multichannel devices (T_{CH}).

$$T_{Ji} = T_{AMB} + T_{PSi} + \sum_{x \neq i}^{n} T_{CHx} \quad (1)$$

Infineon recommends that you leave the TJ pin open (no external connection). The thermal electrical convention is: 1 V = 1°C.

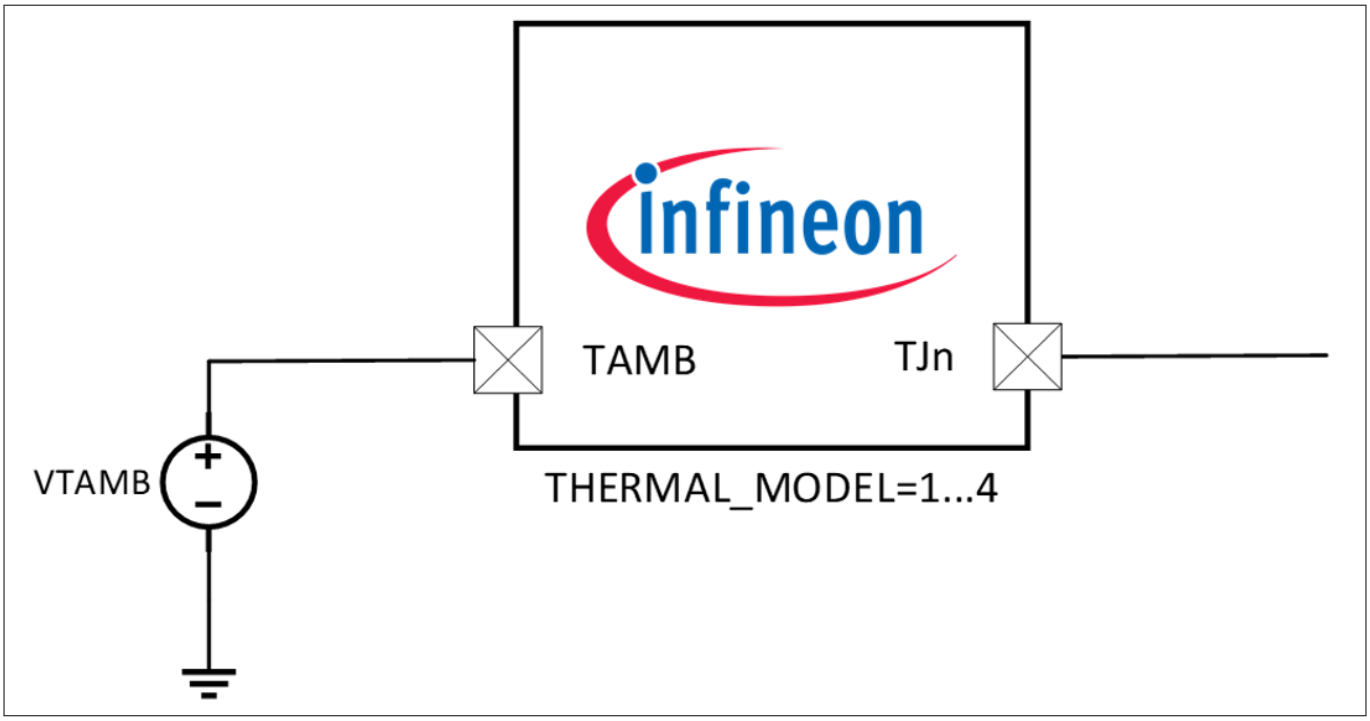

Figure 5 **Configuration of TAMB and TJ pins for THERMAL_MODEL = 1...4**

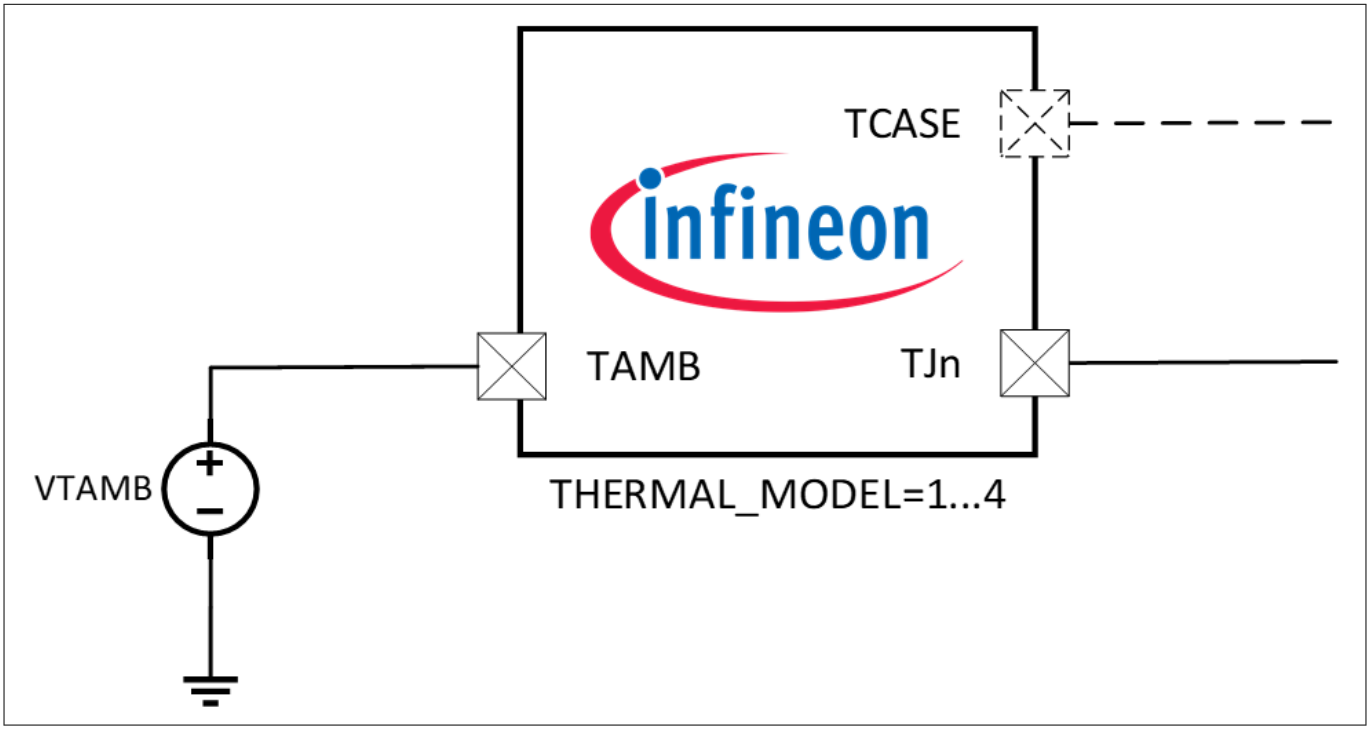

Figure 6 **Configuration of TAMB, TCASE[1)] (optional) and TJ pins for THERMAL_MODEL = 1...4**

[1] Not applicable for all product simulation models

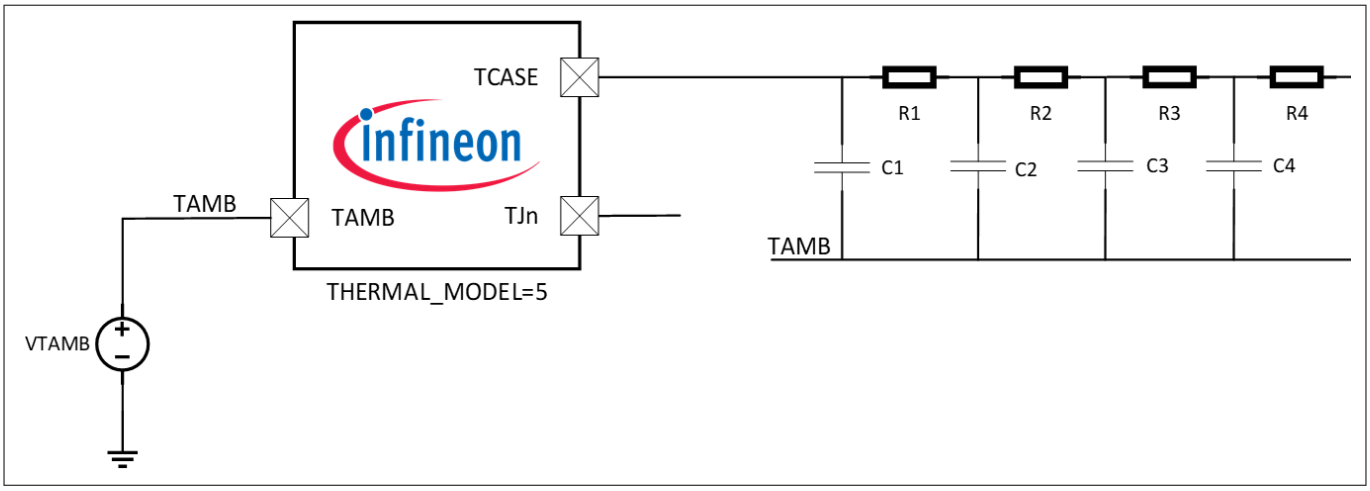

Figure 7 Configuration of TAMB, TCASE and TJ pins for THERMAL_MODEL = 5 (optional)[1)]

[1] Not applicable for all product simulation models

3 Model performance

3.1 Short circuit during PWM and diagnosis disable from ERRN/DEN – Transient

This setup shows the short-circuit protection during both ON and OFF states of a PWM signal applied on EN/DEN. If the fault occurs during an ON pulse, it is detected assuming that the EN/DEN stays high for at least the tFAULT filter duration. If the fault occurs during an OFF phase, the fault management responds as soon as EN/DEN returns to the high state. Once detected, the fault is latched until it clears. The setup also shows how to avoid open-load fault detection when the supply on VS is ramped down below output forward voltage. By connecting the ERRN/DEN pin to a resistor divider and properly dimensioning the value of resistors, fault detection can be disabled before the open-load condition occurs. In this example, at 8 V of supply voltage at VS, the diagnosis is disabled to avoid false open-load conditions, which typically occur when the supply voltage is close to total load voltage drop.

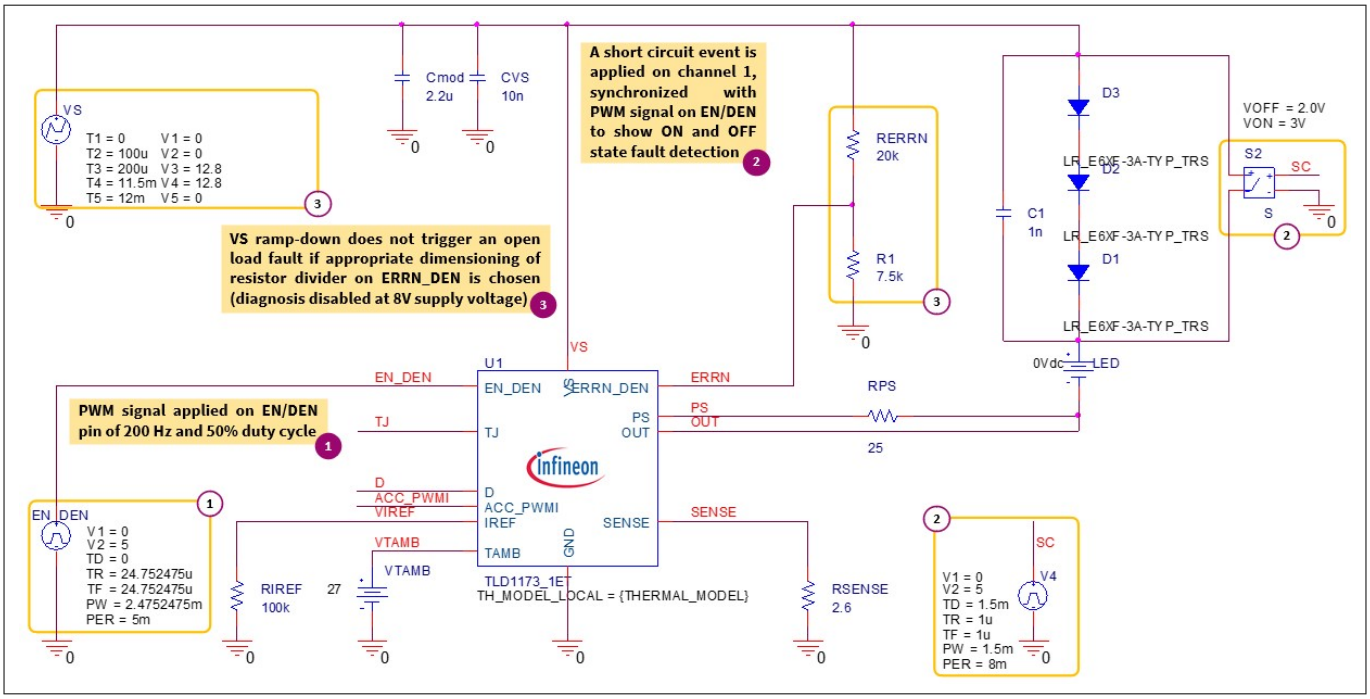

Figure 8 Test setup PWM SC

3 Model performance

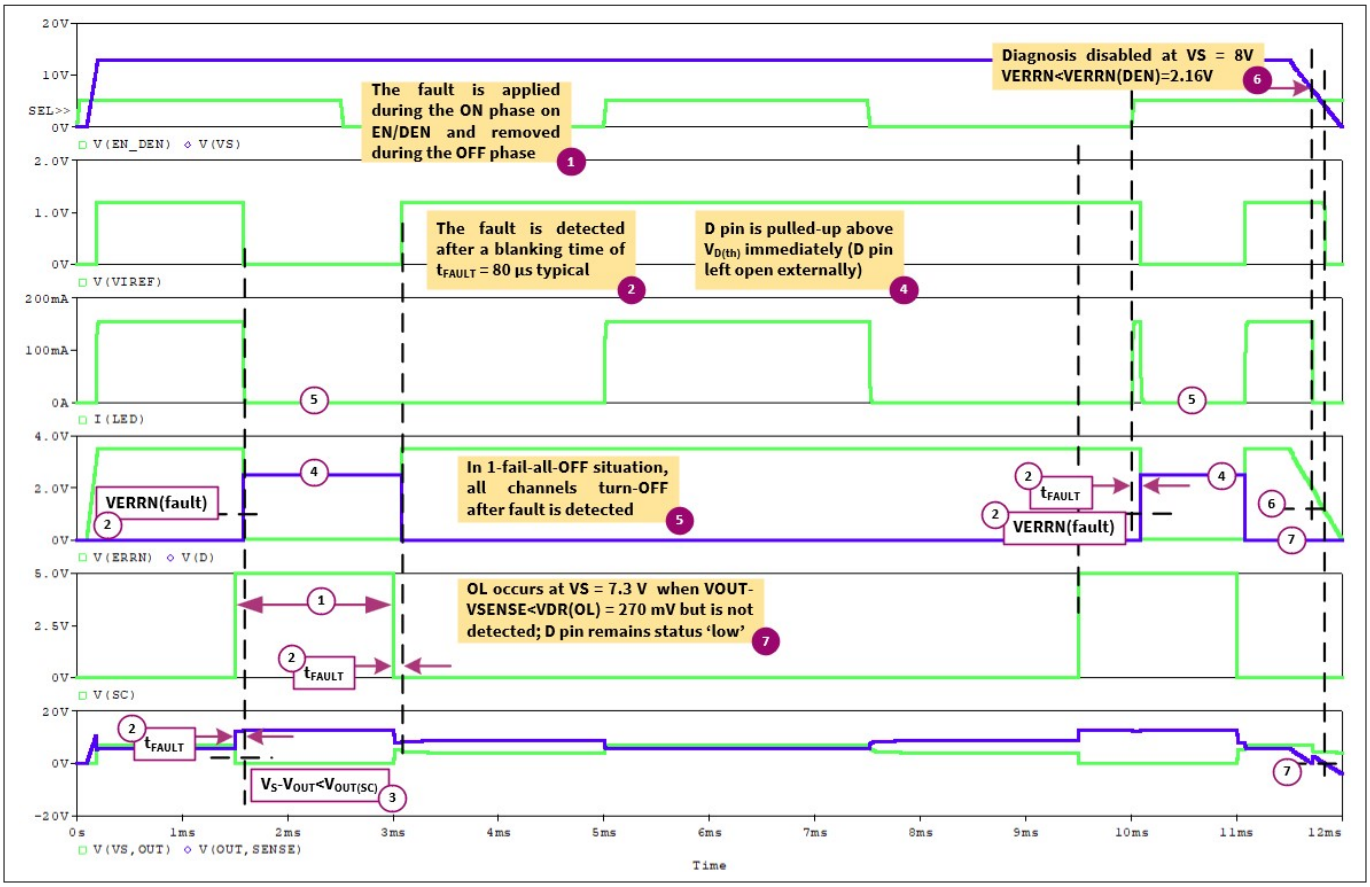

Figure 9 Simulation results PWM SC

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Revision history

Document revision	Date	Description of changes
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