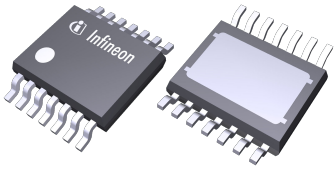
OPTIREG™ switcher TLS5112C0EPV

48 V synchronous step down regulator

AEC Qualified RoHS

Features



- Input voltage range 20 V to 65 V
- Compliant with ISO 21780 standard electrical requirements and tests
- Adjustable output voltage (9 V to 16 V) ±2% accuracy
- 1.2 A step-down regulator
- Enable and programmable undervoltage lockout
- Low quiescent current: 50 µA at no load condition
- Ultra low shutdown current consumption in disabled state: typically 3 µA
- Integrated high-side and low-side power MOSFETs
- Integrated compensation network
- Current mode *PWM* and *PFM* regulation
- Light load PFM mode with improved efficiency
- Switching frequency 320 kHz to 400 kHz
- Synchronization input
- Spread spectrum for improved *EMI* performance
- Adjustable soft start function
- Overvoltage monitoring (power good)
- Output discharge function in disabled state
- Overcurrent protection and overload protection
- Wide temperature range: T_j = -40°C to 150°C
- Green Product (RoHS compliant)

Potential applications

- 48 V applications that require a voltage conversion from high voltage (for example 48 V board net) to an intermediate voltage (for example 12 V)

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The OPTIREG™ switcher TLS5112C0EPV is a synchronous standalone step-down DC/DC-converter especially designed for automotive applications. The device has a current capability of 1.2 A, adjustable output voltage in a range of 9 V to 16 V and a feedback voltage precision of ±2%. The integrated power-stages, a soft start feature and compensation reduce the required amount of external components and thus system cost and board space. The wide input voltage range supports a wide range of use cases for automotive systems (for example 48 V board net). The switching frequency can synchronize to an external clock signal. Optional spread spectrum improves the *electromagnetic interference (EMI)* performance in *pulse-width modulation (PWM)* operation. The device offers optimized efficiency due to low current consumption in *pulse-frequency modulation (PFM)* mode at light loads. In disabled mode the current consumption is reduced to typically 3 µA and an undervoltage lockout

threshold can be programmed via the EN/*undervoltage (UV)*-pin. The device can detect an overvoltage condition at the output and indicate this at the power good output pin. Overcurrent protection and overload protection avoid excessive current in short circuit conditions at the buck converter output. The integrated thermal shutdown feature protects the device from overheating. The enhanced PG-TSDSO-14 exposed-pad package offers enhanced thermal performance in the application.

Type	Package	Marking
TLS5112C0EPV	PG-TSDSO-14	5112C0V

Table of contents

Features . . . 1
Potential applications . . . 1
Product validation . . . 1
Description . . . 1
Table of contents . . . 3
1 Block diagram . . . 5
2 Pin configuration . . . 6
2.1 Pin assignment . . . 6
2.2 Pin definitions and functions . . . 6
3 General product characteristics . . . 8
3.1 Absolute maximum ratings . . . 8
3.2 Functional range . . . 9
3.3 Thermal resistance . . . 9
4 Buck regulator . . . 11
4.1 Functional description buck regulator . . . 11
4.1.1 Regulation loop and operation modes . . . 11
4.1.1.1 PWM (pulse width modulation) mode . . . 11
4.1.1.2 PFM (pulse frequency modulation) mode . . . 12
4.1.2 Adjustable output voltage . . . 12
4.1.3 Power management . . . 12
4.1.3.1 Soft start feature . . . 12
4.1.3.2 Active output discharge . . . 13
4.1.4 Protection features . . . 14
4.1.4.1 Overcurrent protection . . . 14
4.1.4.2 Overtemperature shutdown . . . 14
4.2 Electrical characteristics buck regulator . . . 14
4.3 Typical performance characteristics buck regulator . . . 16
5 Oscillator . . . 20
5.1 Functional description oscillator . . . 20
5.1.1 Synchronization input . . . 20
5.1.2 Spread spectrum . . . 20
5.2 Electrical characteristics oscillator . . . 20
5.3 Typical performance characteristics oscillator . . . 22
6 Enable, undervoltage lockout and current consumption . . . 23
6.1 Functional description enable, undervoltage lockout and current consumption . . . 23
6.2 Electrical characteristics enable, undervoltage lockout and current consumption . . . 23

Table of contents

7 Power good 25
7.1 Functional description power good 25
7.2 Electrical characteristics power good 26
8 Application information 28
8.1 Enable, undervoltage lockout for controlled startup and power-down 29
8.2 Feedforward capacitor 29
8.3 Layout recommendations 30
8.4 Additional information 31
9 Package information 32
Glossary 33
Revision history 34
Disclaimer 35

1 Block diagram

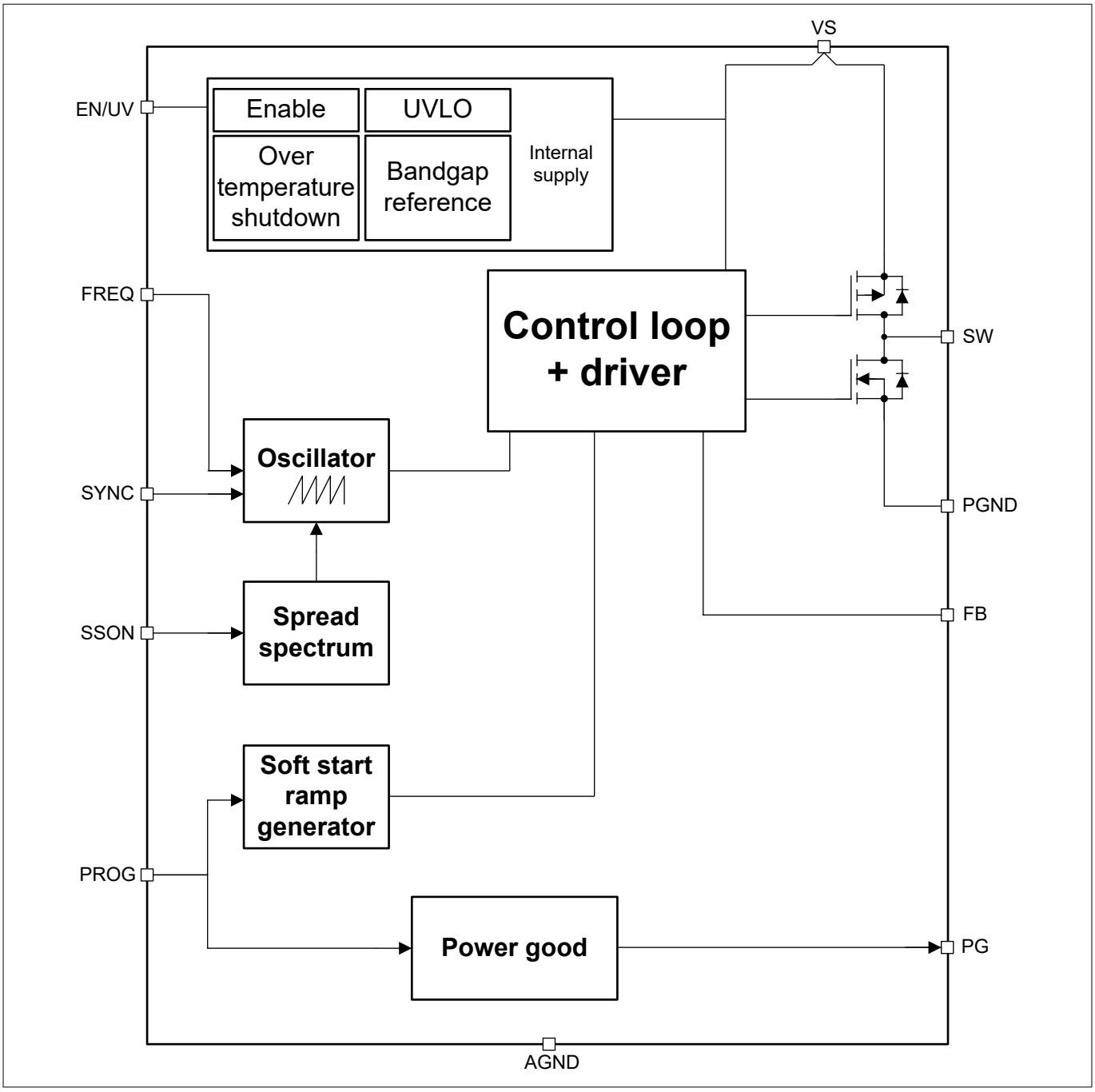


Figure 1 Block diagram

2 Pin configuration

2.1 Pin assignment

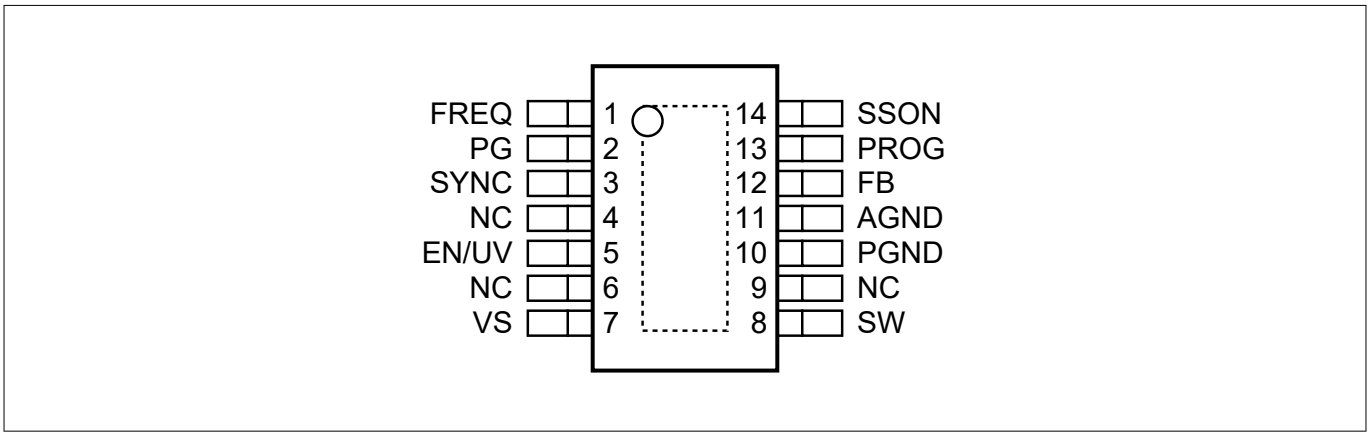


Figure 2 Pin configuration

2.2 Pin definitions and functions

Pin	Symbol	Function
1	FREQ	Frequency selection input: Connect this pin to GND directly to set the default switching frequency. Connect this pin to GND via a resistor for frequency selection.
2	PG	Power good output: Provides the power good output signal. If overvoltage monitoring is used, then connect this pin to a voltage rail below 5.2 V via a resistor. If overvoltage monitoring is not used, then leave this pin open. This pin has an open drain output.
3	SYNC	Synchronization input: If synchronization of the switching frequency is not used, then connect this pin to GND. Connect this pin to an external clock signal to synchronize the switching frequency. In *PFM* mode synchronization is disabled. Do not leave this pin open.
4	N.C.	Not connected: No internal connection. Leave this pin open.
5	EN/*UV*	Enable input, undervoltage lockout: Connect this pin to "high" to enable the device. Connect this pin to "low" to disable the device. Connect this pin to the resistor divider tap to set the undervoltage lockout threshold. This pin has an integrated pull-down resistor.
6	N.C.	Not connected: No internal connection. Leave this pin open.

2 Pin configuration

Pin	Symbol	Function
7	VS	Supply voltage input: Connect this pin to input supply voltage.
8	SW	Buck switch output: Connect this pin directly to the buck converter power inductance.
9	N.C.	Not connected: No internal connection. Leave this pin open.
10	PGND	Power ground: Connect this pin directly to GND via a low inductive and broad trace. Do not leave this pin open.
11	AGND	Analog ground: Connect this pin directly to GND via a low inductive and broad trace. Do not leave this pin open.
12	FB	Feedback input: Connect this pin to the feedback resistor divider tap.
13	PROG	Programming function input: Programming function for • power good overvoltage threshold level • soft start timing Connect this pin to GND via a resistor for programming.
14	SSON	Spread spectrum enable input: Connect this pin to "high" to enable spread spectrum. Connect this pin to "low" or leave it open to disable spread spectrum. This pin has an integrated pull-down resistor.
–	Exposed pad	Connect to heatsink area and to GND by low inductance wiring.

3 General product characteristics

3.1 Absolute maximum ratings

Table 1 Absolute maximum ratings[1)]

T_j = -40°C to 150°C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Voltages							
Supply voltage input voltage	V_{VS}	-0.3	–	70	V	–	P_3.1.22
Supply voltage input voltage	$V_{VS,dyn}$	-0.3	–	85	V	2) Transients present on this pin	P_3.1.10
Enable input, undervoltage lockout	$V_{EN/UV}$	-0.3	–	70	V	–	P_3.1.1
Enable input, undervoltage lockout	$V_{EN/UV,dyn}$	-0.3	–	85	V	2) Transients present on this pin	P_3.1.6
Synchronization input voltage	V_{SYNC}	-0.3	–	6	V	–	P_3.1.2
Spread spectrum selection voltage	V_{SSON}	-0.3	–	6	V	–	P_3.1.5
Frequency selection input voltage	V_{FREQ}	-0.3	–	6	V	–	P_3.1.3
Power good output voltage	V_{PG}	-0.3	–	6	V	–	P_3.1.4
Programming pin voltage	V_{PROG}	-0.3	–	6	V	–	P_3.1.7
Feedback input voltage	V_{FB}	-0.3	–	1.5	V	–	P_3.1.15
Buck switch output voltage	V_{SW}	-0.3	–	V_{VS} + 0.3	V	Minimum -2.0 V in transient condition (single event < 15 ns)	P_3.1.16
Power GND voltage	V_{PGND}	-0.3	–	0.3	V	–	P_3.1.24
Analog GND voltage	V_{AGND}	-0.3	–	0.3	V	–	P_3.1.25
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_3.1.26
Storage temperature	T_{stg}	-55	–	150	°C	–	P_3.1.27
ESD susceptibility							
ESD susceptibility to GND	V_{ESD}	-2	–	2	kV	3) *HBM*	P_3.1.28
ESD susceptibility to GND	V_{ESD}	-500	–	500	V	4) *CDM*	P_3.1.29
ESD susceptibility pins 1, 7, 8, 14 (corner pins) to GND	$V_{ESD1,7,8,14}$	-750	–	750	V	4) CDM	P_3.1.30

1) Not subject to production test, specified by design.
2) Transients between 70 V and 85 V can be tolerated for single events of a duration ≤ 1 µs.
3) Human body model (HBM) robustness according to AEC-Q100-002.

4) Charged device model (CDM) robustness according to AEC-Q100-011; voltage level refers to test condition (TC) mentioned in the standard.

***Notes**:*

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as outside the normal operating range. Protection functions are not designed for continuous repetitive operation.*

3.2 Functional range

Table 2 Functional range

T_j = -40°C to 150°C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Supply voltage	V_{VS}	20	–	65	V	–	P_3.2.1
Enable input, undervoltage lockout	$V_{EN/UV}$	0	–	65	V	–	P_3.2.17
Output voltage adjust range	V_{CC}	9.0	–	16.0	V	Nominal output voltage range	P_3.2.5
SYNC input voltage	V_{SYNC}	0	–	5.2	V	–	P_3.2.7
Spread spectrum selection voltage	V_{SSON}	0	–	5.2	V	–	P_3.2.3
Power good output voltage	V_{PG}	0	–	5.2	V	1)	P_3.2.8
Output current	I_{CC}	0	–	1.2	A	–	P_3.2.4
Junction temperature	T_j	-40	–	150	°C	–	P_3.2.16

1) Allowed external pull-up voltage applied via pull-up resistor to PG pin.

***Note**:* *Within the functional range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the electrical characteristics table.*

3.3 Thermal resistance

Table 3 Thermal resistance[1)]

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	4.2	–	K/W	–	P_3.3.1
Junction to ambient	R_{thJA}	–	36	–	K/W	2) 2s2p	P_3.3.2
Junction to ambient	R_{thJA}	–	48	–	K/W	3) 1s0p + 600 mm²	P_3.3.3
Junction to ambient	R_{thJA}	–	58	–	K/W	3) 1s0p + 300 mm²	P_3.3.4

(table continues...)

Table 3 (continued) Thermal resistance[1)]

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Junction to ambient	R_{thJA}	–	129	–	K/W	[3)] 1s0p, footprint	P_3.3.5

1) Not subject to production test, specified by design.
2) Specified R_{thJA} value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with two inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable, a thermal via array next to the package contacted the first inner copper layer.
3) Specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with 1 copper layer (1 x 70µm Cu).

***Note**: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information refer to www.jedec.org.*

4 Buck regulator

4.1 Functional description buck regulator

The TLS5112C0EPV is a monolithic current mode step-down converter with selectable switching frequency f_{OSC}. The device can operate in *PWM* mode or in *PFM* mode and move automatically between both modes on changes of load and input voltage.

4.1.1 Regulation loop and operation modes

Figure 3 shows the regulation loop. An external resistor divider is required between V_{CC} and the AGND pin, see Figure 6. The error amplifier processes the difference between scaled output voltage feedback voltage and internal reference voltage to provide a reference current for the *PWM* comparator. The device compares the reference current with a scaled version of the inductor current in order to define the PWM duty cycle.

The control logic supervises the transitions between the operation modes and triggers the drivers of the high side PMOS power stage (connected between pin VS and SW) and the low side NMOS power stage (connected between pin SW and PGND) accordingly. See PWM (pulse width modulation) mode and PFM (pulse frequency modulation) mode.

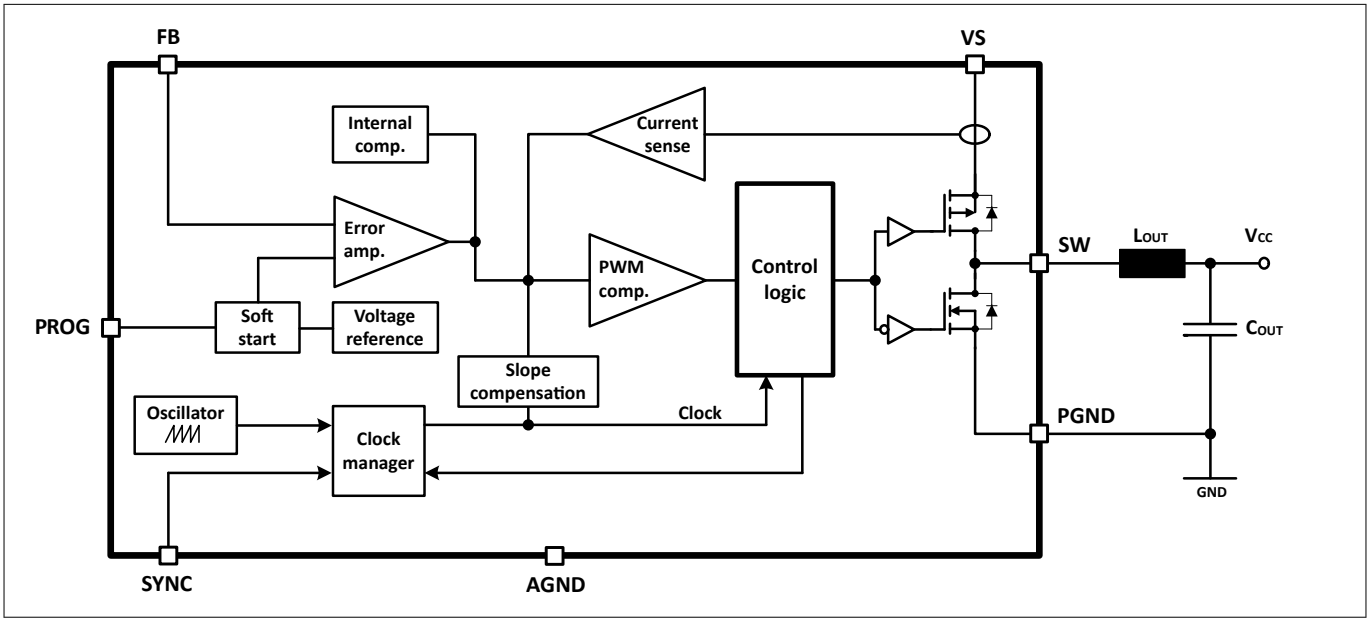


Figure 3 Functional block diagram buck regulator

4.1.1.1 PWM (pulse width modulation) mode

At high load the TLS5112C0EPV operates with the configured switching frequency f_{OSC} in *PWM* mode. In this mode the device modulates the duty cycle in order to regulate the output voltage. The nominal switching frequency can be controlled in one of the following ways (see Oscillator):

- via an external resistor connected at the FREQ pin
- via a synchronization signal applied at pin SYNC

Pulse width modulation is based on peak current mode detection to achieve fast reaction time and optimized feedback voltage accuracy. The PWM comparator processes the current signal detected at the high side PMOS power stage as well as the current signals of the slope compensation and the error amplifier in order to regulate the output voltage by adjusting the switching duty cycle accordingly. The slope compensation ensures system stability for a duty cycle above 50%. This is achieved by avoidance of sub harmonic oscillations of the output inductor current.

Due to a current sense signal inaccuracy at the beginning of the high side switch conduction time during each cycle, a short blanking time is required to mask the output of the current sense, before processing it. The blanking time defines the minimum allowed on-time $t_{on,min}$ of the high side PMOS power stage and therefore the transition from PWM to *PFM* operation.

4.1.1.2 PFM (pulse frequency modulation) mode

The system can operate at constant high side on-time $t_{on,min}$ to achieve a stable output voltage regulation at light load as well as with high input voltage. In *PFM* mode the on-time remains constant while switching frequency is reduced with respect to *PWM* and properly modulated to maintain a stable and regulated output voltage.

In PFM mode at light loads the device offers optimized efficiency due to reduced current consumption of the internal circuitry.

4.1.2 Adjustable output voltage

The output voltage of the TLS5112C0EPV can be adjusted by a voltage divider connected to the FB pin. To achieve high output voltage accuracy, it is recommended to choose a voltage divider cross current above 8 µA:

$$R_{FB2} \leq \frac{0.8\,V}{8\,\mu A} = 100\,k\Omega$$

Equation 1

Neglecting the current flowing into the FB pin, the desired resistance R_{FB1} can be calculated from the required nominal output voltage V_{CC}:

$$R_{FB1} = R_{FB2}\left(\frac{V_{CC}}{V_{FB}} - 1\right)$$

Equation 2

See also Application information.

4.1.3 Power management

The soft start feature and active output discharge control the power on and power off of the device.

4.1.3.1 Soft start feature

The TLS5112C0EPV provides a soft start feature in order to control the ramp-up of the output voltage with a defined timing t_{start} during startup. The soft start timing can be configured via an external resistor R_{PROG} connected between the PROG pin and GND. A valid "high" signal at pin EN/*UV* initiates the start up procedure with the selected soft start timing.

During initialization, the internal supply establishes a stable state and the device initializes the selected configuration for the switching frequency, the overvoltage power good threshold and the soft start timing. When the initialization phase is completed, the regulator starts to increase the output voltage V_{cc}. The device controls the rising output voltage by ramping up the internal voltage reference connected to the error amplifier.

Table 4 Configuration of soft start time

R_{PROG} [kΩ][1]	t_{SS} [ms][2]
6.8	8
10	8
15	8
22	8
33	16
47	16
68	16
>200 (or leave open/floating)	16

1) Resistor tolerance ≤ 5%.
2) Typical soft start time.

4.1.3.2 Active output discharge

The active output discharge function of the device controls the ramp-down of the output voltage during power-down, see Figure 4.

As soon as the device detects a valid "low" signal at the EN/*UV* pin, it actively discharges the device output. In this condition an integrated discharge transistor connected to the SW pin is switched on to discharge the output capacitor C_{OUT} via the output inductor L_{OUT}. The typical on-resistance R_{dc} of the discharge transistor is 200 Ω. The time required to discharge the output capacitor through the switching node depends on:

- R_{dc}
- Load current I_{CC}
- Output capacitance C_{OUT}
- Output inductor L_{OUT}
- Supply voltage V_{VS}

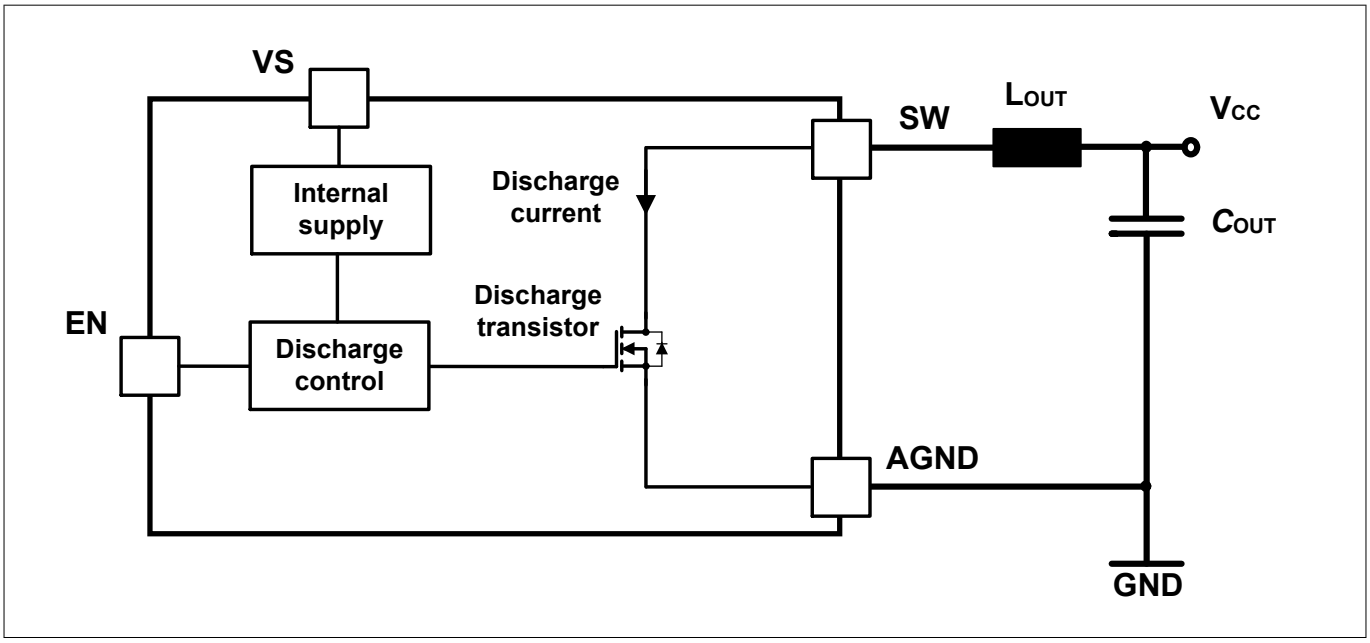


Figure 4 Active output discharge

4.1.4 Protection features

The device is equipped with certain protection features against fault events such as overcurrent, overload and overtemperature.

4.1.4.1 Overcurrent protection

If the sensed current through the high side PMOS power stage exceeds the buck peak overcurrent limit I_{BUOC}, then the device turns off the high side power stage. The current limitation operates as a cycle-by-cycle limitation. For each individual cycle, the device switches off the high side PMOS power stage as soon as it detects exceedance of the current limit after the blanking time of the current sense. The activated current limitation can lead to a reduced output voltage level.

The current sensor of the high side PMOS power stage can also detect overload conditions, such as a short to GND condition at the output voltage node. If the overload limit I_{BUOL} is exceeded, then the device shuts down and restarts with a soft start, after a waiting time of typically 1 s, in order to protect itself from overheating. The overload threshold level lies above the overcurrent threshold level.

4.1.4.2 Overtemperature shutdown

The integrated overtemperature protection turns off the device in case of excessive junction temperature. The typical junction thermal shutdown temperature $T_{j,sd}$ is 175°C. After the device cools down by the amount of the junction temperature hysteresis (T_{j,sd_hyst}) and an additional waiting time of typically 1 s, the device automatically restarts with a soft start to resume normal operation. The thermal shutdown is designed to prevent immediate destruction of the device during fault conditions. However, a junction temperature above 150°C is outside of the maximum ratings and reduces the life time of the device.

4.2 Electrical characteristics buck regulator

Table 5 Electrical characteristics buck regulator

V_S = 20 V to 65 V; T_j = -40°C to 150°C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
FB voltage	V_{FB}	–	0.8	–	V	–	P_4.2.1
FB voltage precision	V_{FB}	-2.0	–	+2.0	%	–	P_4.2.2
MOSFETs							
High side *MOSFET* on-resistance	$R_{on,hs}$	500	900	1700	mΩ	tested at I_{CC} = 100 mA	P_4.2.4
Low side MOSFET on-resistance	$R_{on,ls}$	200	380	740	mΩ	tested at I_{CC} = 100 mA	P_4.2.5
Regulation loop							
Buck peak overcurrent limit	I_{BUOC}	1.5	1.75	2.1	A	–	P_4.2.6
Overload current limit	I_{BUOL}	2.0	2.3	2.7	A	–	P_4.2.7
Minimum switch on-time	$t_{on,min}$	200	250	310	ns	I_{CC} = 0.7 A	P_4.2.13
Soft start							
Soft start time 8 ms	$t_{start,8}$	6.4	8.0	9.6	ms	V_{CC} rising from 5% to 95% of nominal V_{CC} level	P_4.2.18

(table continues...)

Table 5 (continued) Electrical characteristics buck regulator

V_S = 20 V to 65 V; T_j = -40°C to 150°C; all voltages with respect to ground (unless otherwise specified)

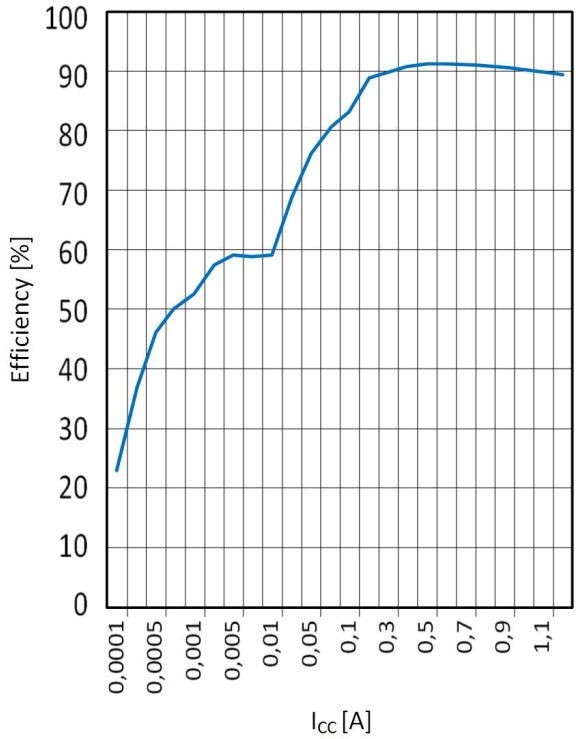
Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Soft start time 16 ms	$t_{start,16}$	12.8	16.0	19.2	ms	V_{CC} rising from 5% to 95% of nominal V_{CC} level	P_4.2.19
Overtemperature protection							
Overtemperature shutdown	$T_{j,sd}$	–	175	–	°C	1)	P_4.2.24
Overtemperature shutdown hysteresis	T_{j,sd_hyst}	8	10	20	K	1)	P_4.2.28

1) Not subject to production test, specified by design.

4.3 Typical performance characteristics buck regulator

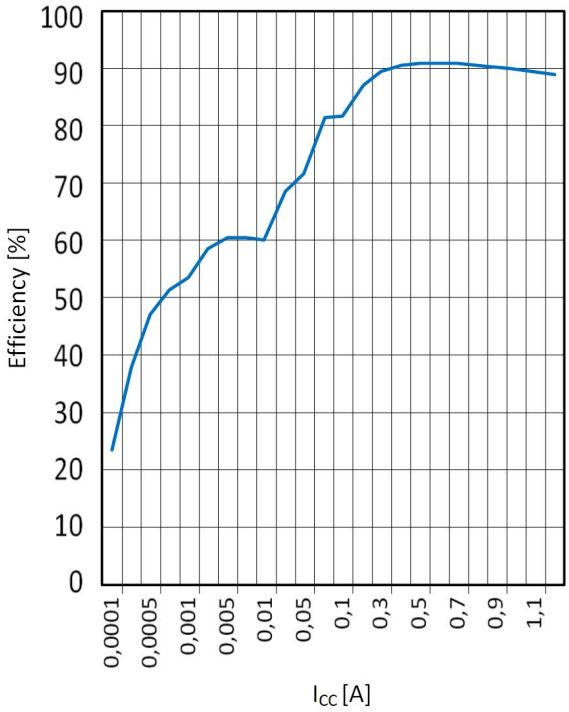
Efficiency

V_{VS} = 48 V; V_{CC} = 12 V; f_{OSC} = 320 kHz; T_{amb} = 25°C



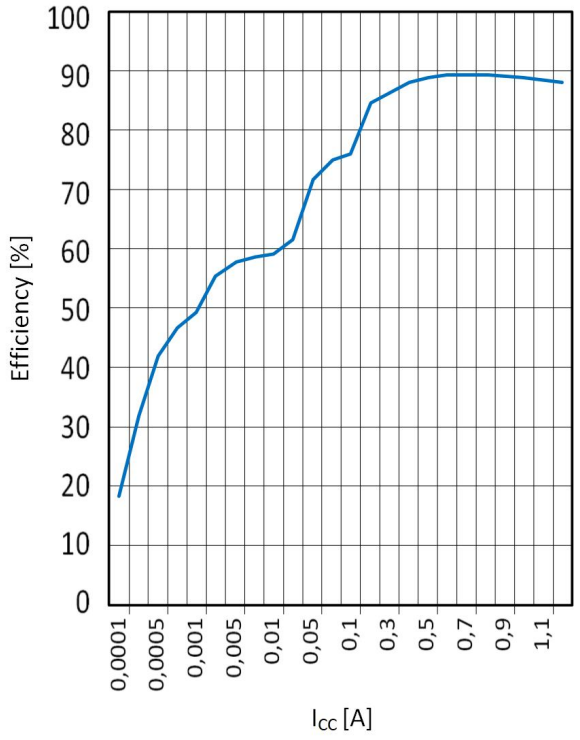
Efficiency

V_{VS} = 48 V; V_{CC} = 12 V; f_{OSC} = 400 kHz; T_{amb} = 25°C



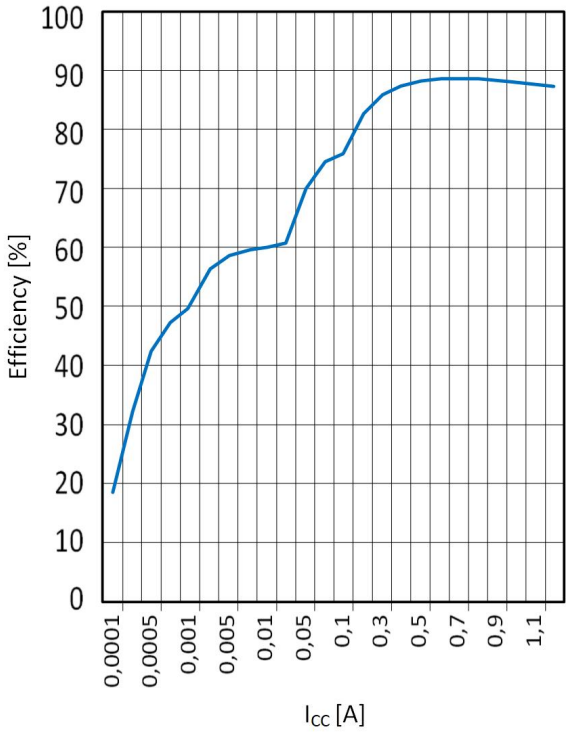
Efficiency

V_{VS} = 65 V; V_{CC} = 12 V; f_{OSC} = 320 kHz; T_{amb} = 25°C



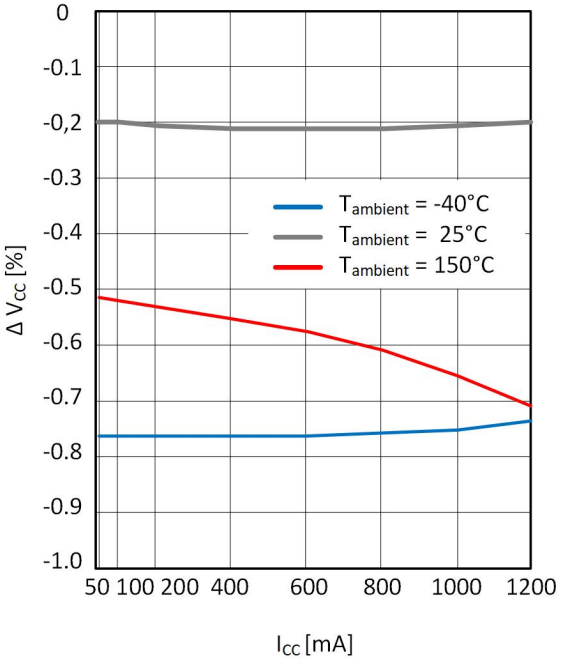
Efficiency

V_{VS} = 65 V; V_{CC} = 12 V; f_{OSC} = 400 kHz; T_{amb} = 25°C



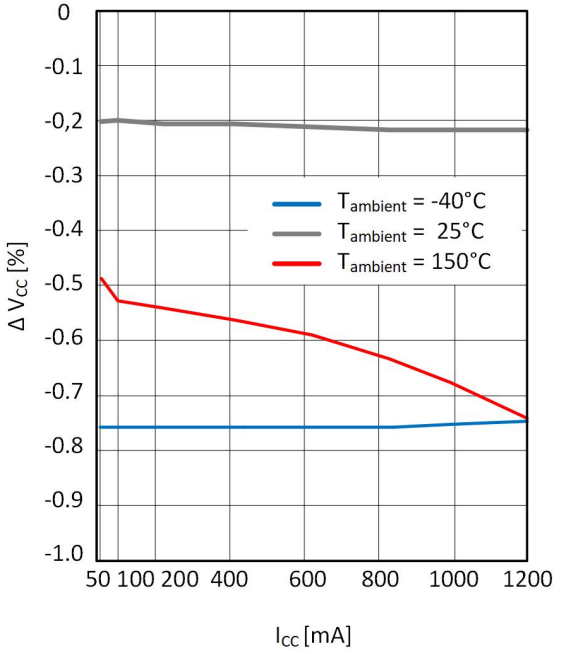
Load regulation

f_{OSC} = 400 kHz; V_{VS} = 20 V; V_{CC} = 12 V



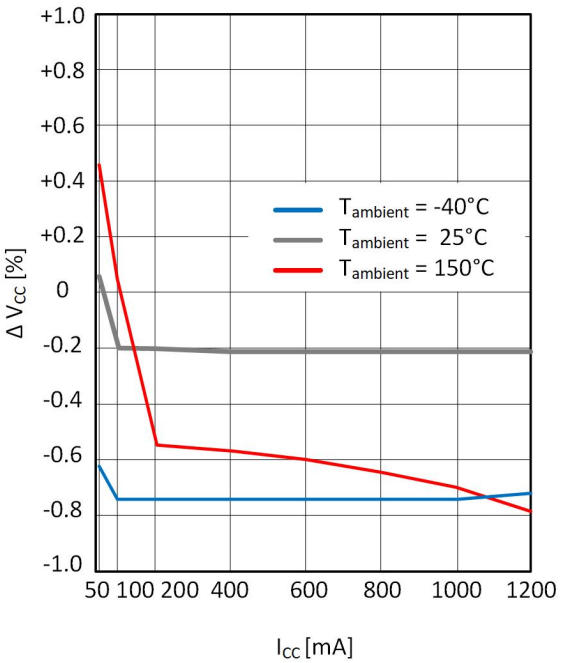
Load regulation

f_{OSC} = 400 kHz; V_{VS} = 48 V; V_{CC} = 12 V



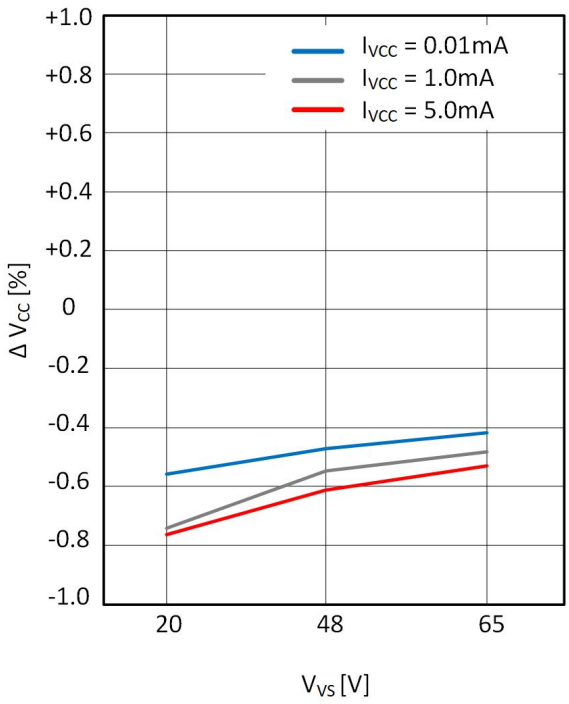
Load regulation

f_{OSC} = 400 kHz; V_{VS} = 65 V; V_{CC} = 12 V



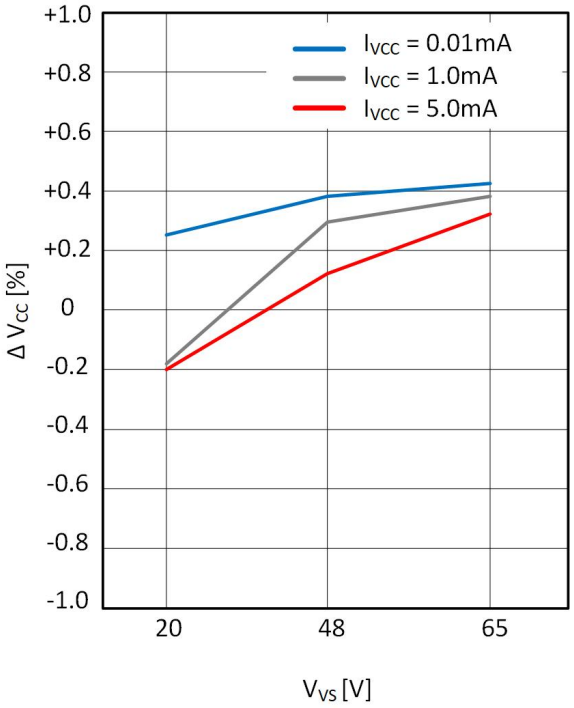
Line regulation

f_{OSC} = 400 kHz; T_{amb} = -40°C



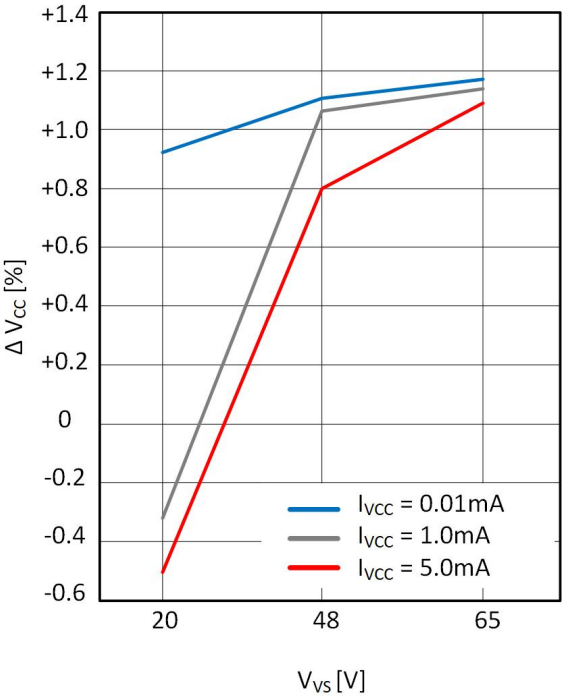
Line regulation

f_{OSC} = 400 kHz; T_{amb} = 25°C



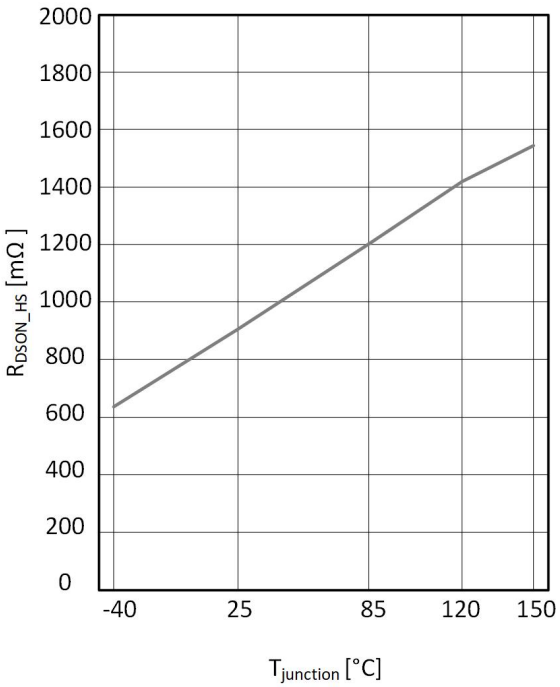
Line regulation

f_{OSC} = 400 kHz; T_{amb} = 150°C



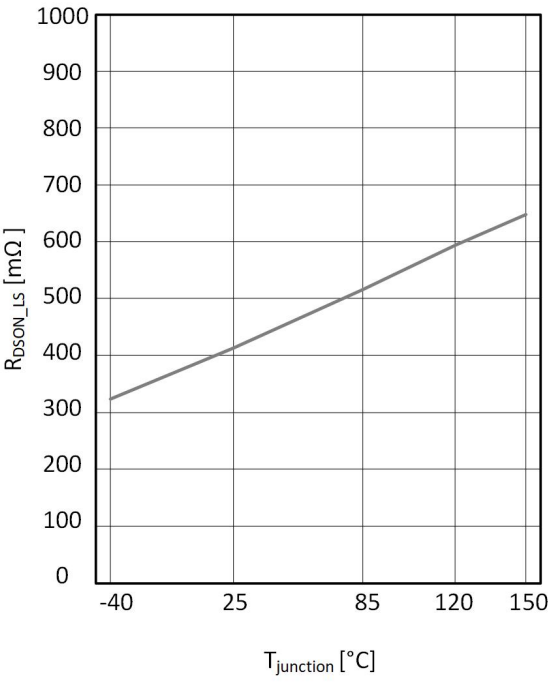
High-side MOSFET ON-resistance

V_{VS} = 48 V;



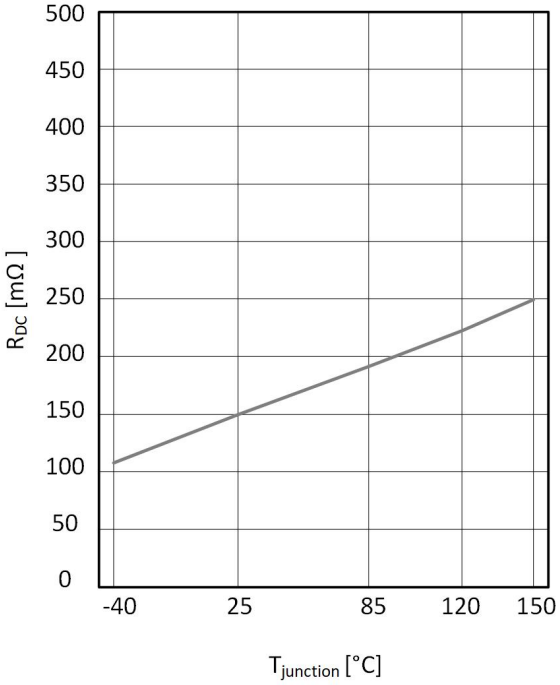
Low-side MOSFET ON-resistance

V_{VS} = 48 V;



Active output discharge resistor

V_{VS} = 48 V;



5 Oscillator

5.1 Functional description oscillator

The integrated clock provides a constant frequency to the regulation loop. In *PWM* mode the device switches on and off the high side and low side power transistors at the oscillator frequency f_{OSC}.

The oscillator frequency can be configured externally via a resistor R_{FREQ} connected between pin FREQ and GND. The device sets the selected switching frequency during startup.

Table 6 Oscillator frequency selection

R_{FREQ} [kΩ][1]	f_{osc} [kHz][2]
2.2	320
3.3	360
≤ 1.0 (or connect FREQ pin directly to GND)	400[3]

1) Resistor tolerance ≤ 5%.
2) Typical oscillator frequency.
3) Default low oscillator frequency.

5.1.1 Synchronization input

In *PWM* mode the switching frequency can synchronize to an external clock signal connected to pin SYNC. Synchronization is enabled when startup is completed and the external clock signal at pin SYNC is accepted.

5.1.2 Spread spectrum

In *PWM* mode, when used without an external clock at the SYNC pin, the device can apply spread spectrum in order to optimize *EMI* performance. The device modulates the switching frequency up and down by a triangle wave of typically 8.3 kHz within a range of typically ±7.5% of the selected oscillator frequency. The logical signal on the SSON pin switches spread spectrum on or off.

5.2 Electrical characteristics oscillator

Table 7 Electrical characteristics oscillator

V_S = 20 V to 65 V; T_j = -40°C to 150°C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Frequency setting							
Oscillator frequency	$f_{osc,320}$	288	320	352	kHz	R_{FREQ} = 2.2 kΩ	P_5.2.1
Oscillator frequency	$f_{osc,360}$	324	360	396	kHz	R_{FREQ} = 3.3 kΩ	P_5.2.2
Default oscillator low frequency	$f_{osc,400}$	360	400	440	kHz	R_{FREQ} ≤ 1.0 kΩ; or connect FREQ pin to GND	P_5.2.3

(table continues...)

Table 7 (continued) Electrical characteristics oscillator

V_S = 20 V to 65 V; T_j = -40°C to 150°C; all voltages with respect to ground (unless otherwise specified)

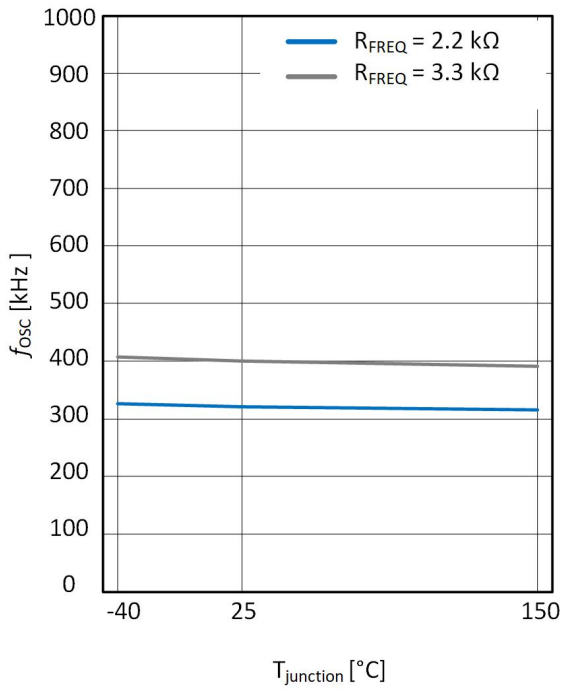
Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Synchronization input							
Synchronization capture frequency range	$f_{SYNC,lo}$	320	–	400	kHz	–	P_5.2.8
SYNC valid "high" voltage	$V_{SYNC,hi}$	3.4	–	–	V	1)	P_5.2.9
SYNC valid "low" voltage	$V_{SYNC,lo}$	–	–	0.8	V	1)	P_5.2.10
SYNC voltage hysteresis	$V_{SYNC,hyst}$	45	255	600	mV	1)	P_5.2.11
SYNC "high" input current	$I_{SYNC,hi}$	–	0.1	2	µA	V_{SYNC} = 5 V	P_5.2.12
SYNC "low" input current	$I_{SYNC,lo}$	-1	-0.1	–	µA	V_{SYNC} = 0 V	P_5.2.13
SYNC signal duty cycle	D_{SYNC}	10	–	90	%	2)	P_5.2.15
Spread spectrum							
SSON valid "high" voltage	$V_{SSON,hi}$	2.0	–	–	V	Enables spread spectrum	P_5.2.17
SSON valid "low" voltage	$V_{SSON,lo}$	–	–	0.8	V	Disables spread spectrum	P_5.2.18
SSON voltage hysteresis	$V_{SSON,hyst}$	100	250	1000	mV	–	P_5.2.19
SSON "high" input current	$I_{SSON,hi}$	0.7	1	1.25	µA	V_{SSON} = 5.0 V	P_5.2.20
SSON modulation frequency	$f_{SSON,mod}$	7.5	8.3	10	kHz	Spread spectrum is enabled	P_5.2.21
SSON modulation frequency range	$f_{SSON,range}$	-11	±7.5	12	%	Spread spectrum is enabled	P_5.2.22

1) Synchronization of *PWM*-on signal to falling edge.
2) Not subject to production test.

5.3 Typical performance characteristics oscillator

Oscillator frequency

V_{VS} = 48 V



6 Enable, undervoltage lockout and current consumption

6.1 Functional description enable, undervoltage lockout and current consumption

A valid "high" signal ($V_{EN/UV} \geq V_{EN/UV,thres}$) at the EN/*UV* pin turns on the regulator. A valid "low" signal ($V_{EN/UV} \leq V_{EN/UV,sd}$) turns off the device. In off state the current consumption of the device is typically 3 µA. If the EN/UV pin is left open, then an integrated pull-down resistor $R_{EN/UV,int}$ at the EN/UV pin ensures that the device turns off.

An undervoltage lockout threshold can be programmed precisely via a voltage divider between VS pin and GND, where the tap is connected to EN/UV pin, see Equation 3 and Figure 6. If the lockout feature is not used, then the EN/UV pin can be tied to the VS pin. Alternatively a logic signal can drive the EN/UV pin as an enable input.

$$V_{VS,\,EN/UV(rising)} = V_{EN,\,UV,\,thres}\left(\frac{R_{EN/UV1}}{R_{EN/UV2}} + 1\right)$$

Equation 3

6.2 Electrical characteristics enable, undervoltage lockout and current consumption

Table 8 Electrical characteristics enable undervoltage lockout and current consumption

V_S = 20 V to 65 V; T_j = -40°C to 150°C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Current consumption							
Current consumption, shutdown mode	$I_{VS,off}$	–	3	15	µA	$V_{EN/UV} \leq V_{EN/UV,sd}$; T_j < 85°C; V_{VS} = 48 V	P_7.2.1
Current consumption, *PFM* mode	I_{VS}	–	50	87	µA	$V_{EN/UV} \geq V_{EN/UV,thres}$; V_{FB} = 0.9 V V_{VS} = 48 V T_j < 85°C	P_7.2.3
Enable undervoltage lockout							
Enable undervoltage shutdown threshold	$V_{EN/UV,sd}$	0.3	0.4	–	V	for lowest shutdown current $I_{VS,off}$; $V_{EN/UV}$ rising	P_7.2.4
Enable undervoltage lockout threshold	$V_{EN/UV,thres}$	1.16	1.21	1.3	V	$V_{EN/UV}$ rising	P_7.2.5
Enable undervoltage lockout hysteresis	$V_{EN/UV,hyst}$	75	100	135	mV	–	P_7.2.6
Enable undervoltage lockout current	$I_{EN/UV,hi1.5}$	–	0.15	0.5	µA	$V_{EN/UV}$ = 1.5 V	P_7.2.7

(table continues...)

Table 8 (continued) Electrical characteristics enable undervoltage lockout and current consumption

V_S = 20 V to 65 V; T_j = -40°C to 150°C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Enable undervoltage lockout current	$I_{EN/UV,hi48}$	–	0.4	1.5	µA	$V_{EN/UV}$ = 48 V	P_7.2.8
Enable undervoltage internal pull down resistor	$R_{EN/UV,int}$	7	10	13	MΩ	$V_{EN/UV}$ = 1.2 V	P_7.2.9

7 Power good

7.1 Functional description power good

The power good function supervises the regulator output voltage V_{CC} by monitoring the feedback voltage V_{FB} and indicates the power good status at pin PG. A "high" level at pin PG confirms that the output voltage V_{CC} is within the desired power good thresholds. A "low" level at pin PG is a warning, that the output voltage V_{CC} is outside the desired power good thresholds.

Power good output

The power good output pin PG is an open drain structure and requires an external pull-up resistor to a voltage level below 5.2 V. The external resistor R_{PG} must match the specified maximum power good output "low" sink current, see Power good output PG .

As long as the device operates within the specified range in Table 1 and Table 2, the power good feature is functional. After the device ramps up and the soft start time expires, the power good function is active. If the device is switched off or a protection function is active, such as thermal shut down event or overload condition, then it disables the power good feature.

Power good operation

If the output voltage V_{CC} rises above the output overvoltage power good threshold $V_{PG,OVthres}$ for more than the blanking time $t_{PG,blank}$, then the device indicates power good by setting the PG pin "low". The blanking time is implemented to avoid incorrect triggering of power good due to short glitches at the output voltage V_{CC}. If the output voltage V_{CC} recovers and drops below the output overvoltage power good recovery threshold $V_{PG,OVrecover}$, then the device sets the PG pin "high" after the blanking time $t_{PG,blank}$ expires, see Figure 5.

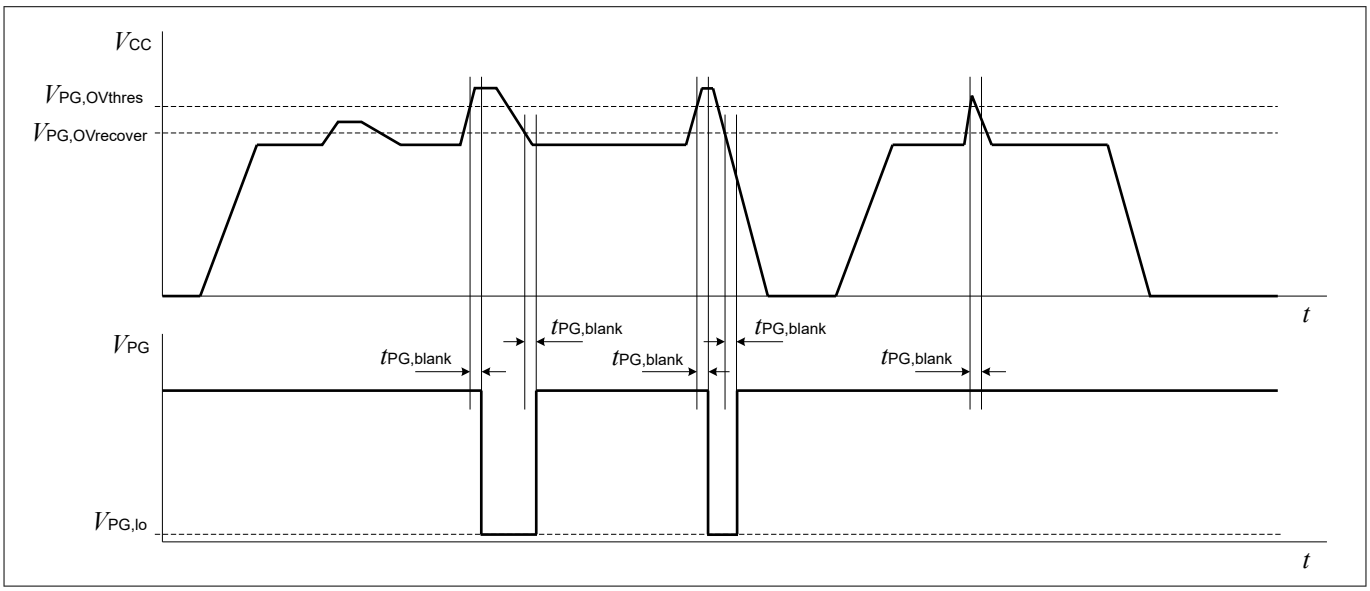


Figure 5 Power good timing diagram

Power good thresholds

The overvoltage power good threshold $V_{PG,OVthres}$ can be configured according to the application's need via an external resistor R_{PROG} connected to the PROG pin. It's resistance sets the overvoltage power good threshold according to Table 9.

Table 9 PROG: configuration of overvoltage power good threshold

R_{PROG} [kΩ][1]	$V_{PG,OVthres}$ [% of V_{FB}][2]
6.8	+35
10	+25
15	+15
22	+8
33	+25
47	+15
68	+8
> 200 (or leave PROG pin open)	+35

1) Resistor tolerance ≤ 5 %.
2) Typical overvoltage power good threshold.

7.2 Electrical characteristics power good

Table 10 Electrical characteristics power good

V_S = 20 V to 65 V; T_j = -40°C to 150°C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Power good output PG							
PG "low" voltage	$V_{PG,lo}$	–	–	0.4	V	$V_{FB} \geq V_{PG,OVthres}$; $V_{EN/UV} \geq V_{EN/UV,thres}$; $I_{PG} \leq 1.5$ mA	P_8.2.1
PG "low" sink current	$I_{PG,lo}$	–	–	1.5	mA	$V_{FB} \geq V_{PG,OVthres}$; $V_{EN/UV} \geq V_{EN/UV,thres}$; $V_{PG} \leq 0.4$ V	P_8.2.2
PG leakage current	$I_{PG,L}$	–	–	1	µA	Power good not active $V_{FB} < V_{PG,OVthres}$	P_8.2.3
Output overvoltage power good threshold							
Output overvoltage power good threshold increasing	$V_{PG,OVthres8}$	6	8	10	%	percentage of V_{FB}; see also PROG configuration in Table 9	P_8.2.4
Output overvoltage power good threshold increasing	$V_{PG,OVthres15}$	13	15	17	%	percentage of V_{FB}; see also PROG configuration in Table 9	P_8.2.5
Output overvoltage power good threshold increasing	$V_{PG,OVthres25}$	23	25	27	%	percentage of V_{FB}; see also PROG configuration in Table 9	P_8.2.6

(table continues...)

Table 10 (continued) Electrical characteristics power good

V_S = 20 V to 65 V; T_j = -40°C to 150°C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Output overvoltage power good threshold increasing	$V_{PG,OVthres35}$	33	35	37	%	percentage of V_{FB}; see also PROG configuration in Table 9	P_8.2.7
Output overvoltage power good recovery threshold	$V_{PG,OVrecover}$	2	4	6	%	percentage of V_{FB}; V_{FB} decreasing	P_8.2.8
Power good timing							
Power good blanking time	$t_{PG,blank}$	2	5	20	µs	Output voltage spikes filtered by blanking time	P_8.2.9

8 Application information

***Note**: The information provided in this chapter is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition, or quality of the device. The function must be verified in the real application. For sizing and dimensioning of external components, refer to additional technical documentation or contact our technical support team for assistance.*

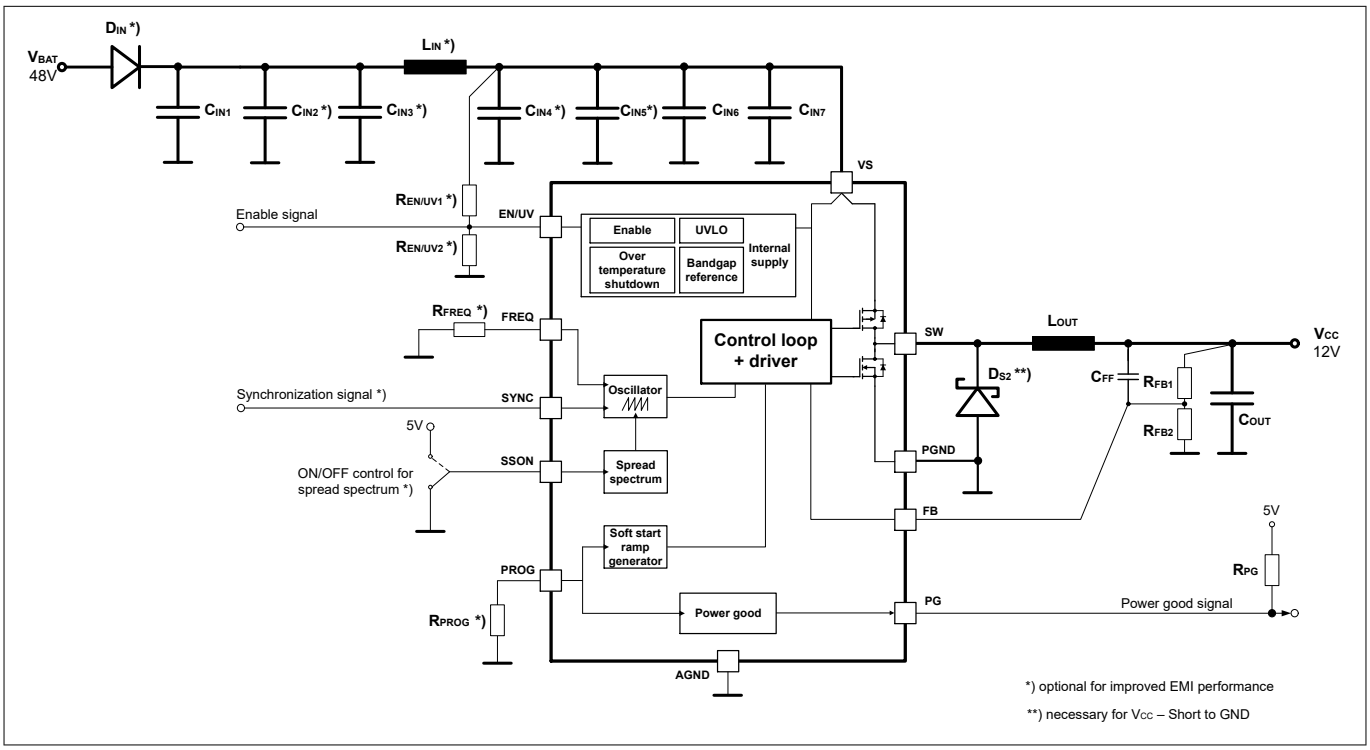


Figure 6 Application diagram

Table 11 Recommended values for parts in application diagram

Name	Value[1)]	Remarks
C_{IN1}	100 µF/100 V	No π-filter used
C_{IN6}	4.7 µF/100 V	No π-filter used
C_{IN7}	100 nF/100 V	No π-filter used
C_{IN1}	4.7 µF/100 V	Optional, for improved *EMI* performance
C_{IN2}	4.7 µF/100 V	Optional, for improved EMI performance
C_{IN3}	100 nF/100 V	Optional, for improved EMI performance
C_{IN4}	4.7 µF/100 V	Optional, for improved EMI performance
C_{IN5}	33 µF/100 V	Optional, for improved EMI performance
C_{IN6}	4.7 µF/100 V	Optional, for improved EMI performance
C_{IN7}	1 µF/100 V	Optional, for improved EMI performance
L_{IN}	15 µH	Optional, for improved EMI performance
L_{OUT}	68 µH	Use low DC-resistance inductor for high efficiency

(table continues...)

Table 11 (continued) Recommended values for parts in application diagram

Name	Value[1)]	Remarks
C_{OUT}	66 µF	Ceramic capacitor
R_{FB1}	453 kΩ (1%)	For an output voltage of typically 12 V
R_{FB2}	32.4 kΩ (1%)	For an output voltage of typically 12 V
R_{PG}	10 kΩ (1%)	–
$R_{EN/UV1}$	460.1 kΩ (1%)	For a $V_{VS,EN/UV(rising)}$ threshold of about 19.83 V
$R_{EN/UV2}$	30 kΩ (1%)	For a $V_{VS,EN/UV(rising)}$ threshold of about 19.83 V
R_{FREQ}	0 Ω	For an oscillator frequency of typically 400 kHz
R_{PROG}	6.8 kΩ	For a soft start time of typically 8 ms and an overvoltage power good threshold of typically +35% (of V_{FB})
D_{S2}	Schottky 100 V / 5 A	Necessary to protect the device from V_{CC} short to GND

1) Typical conditions.

For stable low-frequency operation (320 kHz ≤ f_{SW} ≤ 400 kHz), the output LC filter must be selected as described below.

Table 12 Output LC filter

Description	Symbol	Min.	Typ.	Max.	Unit
Output inductor	L_{OUT}	54.4 (-20%)	68	81.6 (+20%)	µH
Output inductor series resistance	DCR_{LOUT}	1	–	250	mΩ
Output capacitor (ceramic), effective value	C_{OUT}	43.2 (-34.5%)	66	85.8 (+30%)	µF
Output capacitor (ceramic) equivalent series resistance at 100 kHz	$ESR_{C_{OUT}}$	1	–	50	mΩ

8.1 Enable, undervoltage lockout for controlled startup and power-down

For a controlled startup and power down, the use of a voltage divider between VS and GND with the tap connected to EN/*UV* pin is recommended, see Figure 6. With this configuration an undervoltage threshold can be programmed via a voltage divider to specify when the device starts up or shuts down.

8.2 Feedforward capacitor

An additional feedforward capacitor C_{FF} between the output voltage node V_{CC} and the feedback pin FB is required for stable operation, see Figure 6. The value of this capacitance depends on the feedback resistors selected and therefore on the output voltage.

Use the following formula to obtain the value of this capacitance:

$$C_{FF} = 0.75 \times \frac{16 \times 10^{-6}}{R_{FB1}}$$

Equation 4

Table 13 Feedforward capacitor

Output voltage	C_{FF}	R_{FB1}	R_{FB2}
9 V	33 pF	332.1 kΩ	32.4 kΩ
12 V	22 pF	453.6 kΩ	32.4 kΩ
16 V	18 pF	615.6 kΩ	32.4 kΩ

8.3 Layout recommendations

Introduction

A switch mode step down converter is a potential source of electromagnetic disturbances which may affect the application environment as well as the device itself. This can lead to sporadic malfunction such as regulator instability or irreversible damage depending on the amount of generated noise.

Types of electromagnetic disturbances:

- Radiated magnetic fields caused by circulating currents, which occur mostly in accordance with the switching frequencies and their respective harmonics
- Radiated electric fields, mostly caused by voltage oscillations
- Conducted disturbances, which are voltage oscillations or noise mainly present at the input and the output

Radiated magnetic fields

Radiated magnetic fields are caused by circulating currents occurring in so called current windows, which are defined by the area of the corresponding circulating current. These alternating currents (or current ripples) are induced by the switching activities through the power stage MOSFETs and cause magnetic field emission depending on the amplitude of the current and the size of the current window.

Mainly contributing current windows:

- Input current window:
  path consisting of C_{IN1}, C_{IN2}, L_{OUT} and C_{OUT}
- Output current window:
  path consisting of L_{OUT} and C_{OUT}

The areas of these windows must be kept as small as possible and with the related elements placed next to each other as close as possible. Additionally it is highly recommended to use additional ground planes as shielding against radiated magnetic fields.

Radiated electric fields

Radiated electric fields are caused by voltage oscillations on parasitic inductances and capacitances between the SW pin and the output capacitor C_{OUT}. This effect depends also on the commutation of the current from the high side to the low side power stage. The effect needs to be mitigated as good as possible using short, but wide enough connections and by arranging the related parts together as close as possible to reduce the effect of parasitic elements of traces and connections. During the switching action the parasitic capacitance at the SW pin is charged and discharged by short current spikes. Therefore especially the SW node area between the SW pin and the output inductor L_{OUT} should be kept as small as possible.

Conducted disturbances

Conducted disturbances occur permanently or by occasion at the regulator input or output connection. Similar to the radiated electric fields, conducted disturbances are caused by voltage oscillations. Their frequencies can exceed 100 MHz and they are superimposed to the input voltage V_{VS} and output voltage V_{CC}. This might disturb other components of the application. Countermeasures against conducted disturbances are similar to the ones against radiated electric fields. It is recommended to use short and wide traces between the converter components and all parts should be mounted close together. Additionally, well connected small ceramic filter capacitors (1 nF to 220 nF) with low *equivalent series resistance (ESR)* can be connected in parallel to the input capacitors close to the input pin VS and in parallel to the output capacitor C_{OUT} close to the output inductor L_{OUT}. In order to reduce the noise injected into the battery supply line, a π-filter could be necessary (for example consisting of C_{IN1}, C_{IN2}, C_{IN3} and L_{IN}), which requires additional capacitors and an inductor.

8.4 Additional information

Please contact Infineon:

- for information regarding the pin behavioral assessment
- for application notes with more detailed information about this device
- for any further information visit https://www.infineon.com/

9 Package information

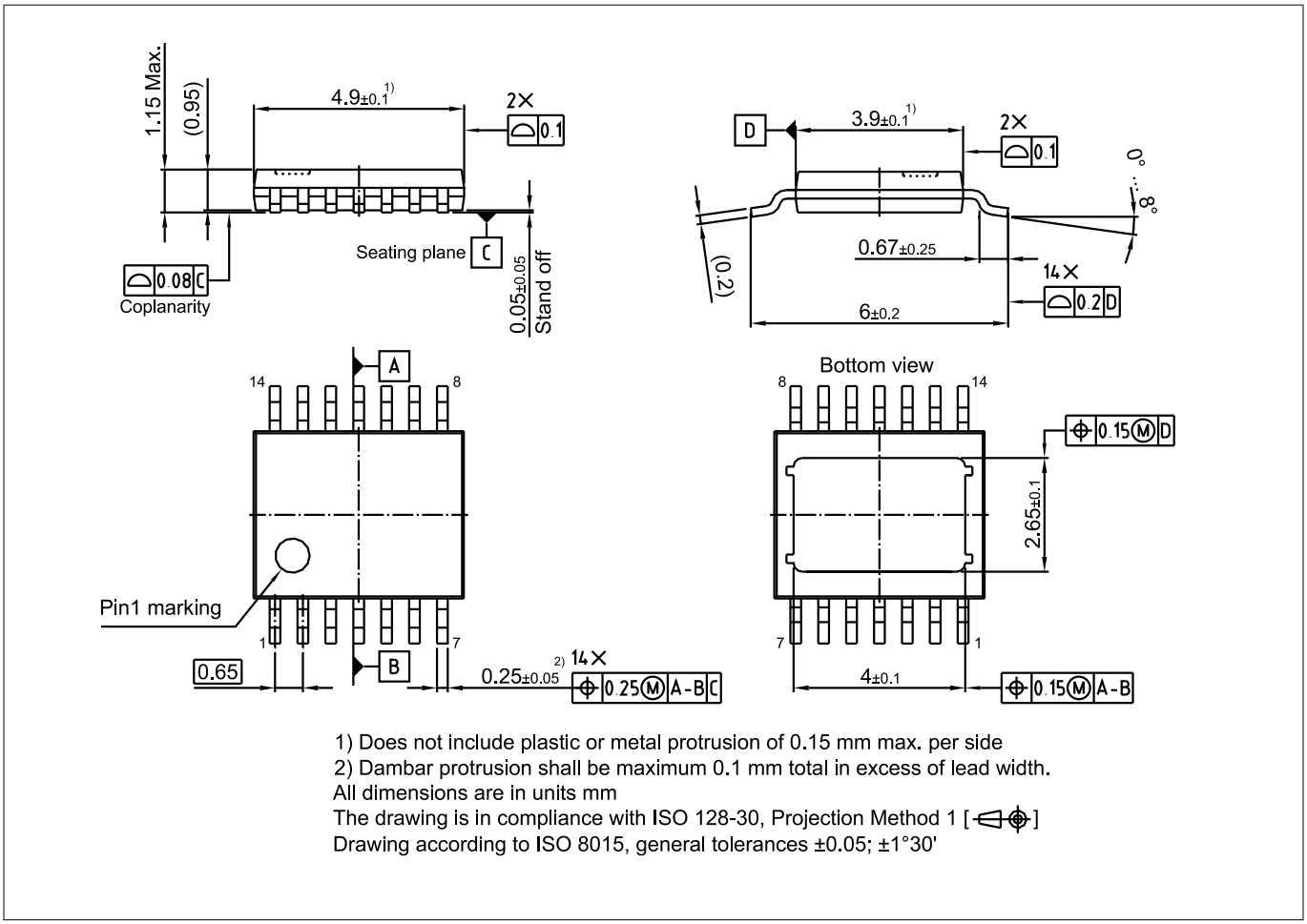


Figure 7 PG-TSDSO-14

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations, the device is available as a Green Product. Green Products are RoHS compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Information on packages

For more information on packages, such as recommendations on assembly, refer to www.infineon.com/packages.

Glossary

CDM

charged device model (CDM)

A model for characterizing the susceptibility of an electronic device to damage from electrostatic discharge (ESD).

EMI

electromagnetic interference (EMI)

A disturbance generated by an external source that affects an electrical circuit by electromagnetic induction, electrostatic coupling, or conduction.

ESR

equivalent series resistance (ESR)

A value representing the loss of useful energy in a simple electronic circuit consisting of a resistor and an ideal capacitor or inductor.

HBM

human body model (HBM)

A model for characterizing the susceptibility of an electronic device to damage from electrostatic discharge (ESD) based on a human body.

MOSFET

metal-oxide-semiconductor field-effect transistor (MOSFET)

PFM

pulse-frequency modulation (PFM)

A modulation method for representing an analog signal using only two levels (1 and 0). PFM fixes the width of square pulses while varying the frequency.

PWM

pulse-width modulation (PWM)

A technique to encode an analog value into the duty cycle of a pulsing signal with arbitrary amplitude.

UV

undervoltage (UV)

Revision history

Revision	Date	Changes
1.10	2026-11-03	Datasheet updated Typical performance characteristics buck regulator added Typical performance characteristics oscillator added
1.00	2026-09-09	Datasheet created

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