OPTIREG™ PMIC TLF4D985QKV02R1

Multi-rail power management IC for systems up to ASIL D

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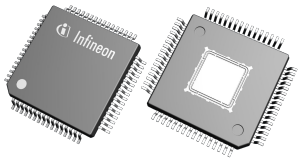
AEC Qualified | RoHS | ISO 26262 compliant

Features



- AEC-Q100 Grade 0 for high temperature mission profiles
- Wide input voltage range 3.8 V to 60 V
- 3.3 V, 30 mA low drop voltage regulator for standby supply
- 5.5 V, 4.0 V, 10 A pre-regulator
- 7 A multiphase synchronous buck converter for microcontroller supply, configurable from 0.7 V to 1.1 V in 12.5 mV steps
- 3.3 V, 1.2 A buck post-regulator for high-speed communication interface
- 3.3 V, 600 mA low drop regulator for microcontroller IO supply
- 5.0 V, 600 mA low drop regulator for low speed communication supply
- 5.0 V ±1%, 150 mA voltage reference for ADC supply
- Control circuit for external MOSFETs for safety switch and reverse battery
- Voltage monitoring with reset and interrupt functions, built-in self-test
- Input voltage monitoring with overvoltage shutdown
- Two safe state control outputs, configurable functional watchdog and window watchdog
- Internal state machine with support for CPU and system virtualization
- 32 bit SPI with CRC
- ISO 26262 Safety Element out of Context (SEooC) for safety requirements up to ASIL D
- Infineon automotive quality
- Green Product (RoHS compliant)

Potential applications

- Car powertrain and transmission applications: inverter, engine management
- Truck applications, CAV applications
- Sensor fusion
- Domain controller, zone controller
- Connected gateway

Product validation

Qualified for automotive applications with higher temperature requirements. Product validation according to AEC-Q100, Grade 0.

Description

The OPTIREG™ PMIC TLF4D985QKV02R1 is a highly efficient Functional Safety PMIC (Power management integrated circuit).

Type	Package	Marking (Line 1 / Line 2)
TLF4D985QKV02R1	PG-LQFP-64	TLF4D985 V02R1

Table of contents

Features . . . 1
Potential applications . . . 1
Product validation . . . 1
Description . . . 2
Table of contents . . . 3
1 Block diagram . . . 11
2 Pin configuration . . . 12
2.1 Pin assignment . . . 12
2.2 Pin definitions and functions . . . 12
3 General product characteristics . . . 16
3.1 Absolute maximum ratings . . . 16
3.2 Functional range . . . 19
3.2.1 Functional range description . . . 19
3.2.2 Electrical characteristics functional range . . . 19
3.3 Thermal resistance . . . 21
4 DCDC Switching frequency generation and clock synchronization . . . 22
4.1 Functional description . . . 22
4.1.1 EMC features . . . 23
5 Power supply function . . . 24
5.1 BUCK PREREG (buck pre-regulator) . . . 24
5.1.1 Functional description BUCK PREREG . . . 24
5.1.2 Electrical characteristics BUCK PREREG . . . 25
5.2 BUCK CORE (buck core regulator) . . . 28
5.2.1 Functional description BUCK CORE . . . 29
5.2.2 Electrical characteristics BUCK CORE . . . 30
5.3 BUCK IF (interface regulator) . . . 35
5.3.1 Functional description BUCK IF . . . 36
5.3.2 Electrical characteristics BUCK IF . . . 37
5.4 BOOST (boost regulator) . . . 40
5.4.1 Functional description BOOST . . . 41
5.4.2 Electrical characteristics BOOST . . . 42
5.5 Communication LDO (QCO) . . . 43
5.5.1 Functional description communication LDO (QCO) . . . 44
5.5.2 Electrical characteristics communication LDO (QCO) . . . 44
5.6 Reference LDO (QVR) . . . 45
5.6.1 Functional description reference LDO (QVR) . . . 45
5.6.2 Electrical characteristics reference LDO (QVR) . . . 46

Table of contents

5.7 MCU-LDO (QUC) 46
5.7.1 Functional description MCU-LDO (QUC) 47
5.7.2 Electrical characteristics MCU-LDO (QUC) 47
5.8 Standby LDO (QST) 48
5.8.1 Functional descriptions standby LDO (QST) 48
5.8.2 Electrical characteristics standby LDO (QST) 49
5.9 Active discharge 50

6 Safety switch (SSW) 51
6.1 Functional description safety switch (SSW) 51
6.2 Electrical characteristics safety switch (SSW) 52

7 Wakeup functions 54
7.1 Introduction 54
7.2 Enable (ENA) 54
7.2.1 Functional description enable (ENA) 55
7.2.2 Electrical characteristics enable (ENA) 55
7.3 Wake (WAK) 56
7.3.1 Functional description wake (WAK) 56
7.3.2 Electrical characteristics wake (WAK) 57
7.4 Wake-up timer (WUT) 57
7.4.1 Functional description wake-up timer (WUT) 57
7.4.2 Electrical characteristic wake-up timer 58
7.5 Wake-up via SPI frame 58

8 Hardware configuration (HWCFG) 59
8.1 Functional description 59

9 State machine (FSM) 61
9.1 Functional description state machine (FSM) 61
9.1.1 Description of the states 62
9.1.1.1 POWERDOWN state 62
9.1.1.2 INIT state 63
9.1.1.3 NORMAL state 65
9.1.1.4 WAKE state 66
9.1.1.5 REDUCED OPERATION state 68
9.1.1.6 FAILSAFE state 69
9.1.1.7 SLEEP state 70
9.1.1.8 STANDBY state 72
9.1.2 INIT timer function 73
9.1.3 State transition 76
9.1.3.1 State transition table 76
9.1.3.2 Programmable transition delay time 78
9.1.3.3 Automated wake-up from FAILSAFE 79
9.1.4 Power sequencing 79

Table of contents

9.1.4.1 Power up sequence schema A . . . 80
9.1.4.2 Power up sequence schema B . . . 81
9.1.4.3 Power down sequencing . . . 82
9.2 Electrical characteristics state machine (FSM) . . . 84

10 Monitoring functions . . . 103
10.1 Watchdog functions (WD) . . . 103
10.1.1 Introduction watchdog functions (WD) . . . 103
10.1.2 Window watchdog (WWD) . . . 104
10.1.2.1 Functional description window watchdog (WWD) . . . 104
10.1.2.1.1 Valid triggering of the window watchdog . . . 104
10.1.2.1.2 Invalid triggering due to missing trigger during open window . . . 105
10.1.2.1.3 Invalid triggering due to trigger during closed window . . . 106
10.1.2.1.4 Watchdog startup behavior (enable and reset) . . . 107
10.1.2.1.5 Windows watchdog error counter . . . 108
10.1.2.1.6 Timing constraints and behavior after configuring the watchdog . . . 108
10.1.2.2 Electrical characteristics window watchdog (WWD) . . . 109
10.1.3 Functional watchdog (FWD) . . . 110
10.1.3.1 Functional description functional watchdog (FWD) . . . 110
10.1.3.1.1 Functional watchdog service . . . 110
10.1.3.1.2 Functional watchdog error counter overflow . . . 116
10.2 Error monitoring (ERR MON) . . . 117
10.2.1 Introduction . . . 117
10.2.2 Functional description error monitoring (ERR MON) . . . 118
10.2.2.1 Error monitoring initialization . . . 118
10.2.2.2 Error monitoring configuration . . . 119
10.2.2.3 Error monitoring recovery timers . . . 121
10.2.2.4 Invalid error toggling . . . 121
10.2.3 Electrical characteristics error monitoring (ERR MON) . . . 123
10.3 Voltage monitoring . . . 124
10.3.1 Introduction . . . 124
10.3.2 Battery voltage monitoring . . . 125
10.3.3 Internal voltage monitoring . . . 125
10.3.4 Electrical characteristics monitoring functions . . . 128
10.3.5 Ext. monitoring channels (VMON) . . . 131
10.3.5.1 Functional description ext. monitoring channels (VMON) . . . 132
10.3.5.2 Electrical characteristics ext. monitoring channels (VMON) . . . 133
10.4 Overcurrent and overtemperature monitoring . . . 134
10.4.1 Introduction . . . 134
10.4.2 Functional description overtemperature monitoring . . . 136
10.4.3 Functional description current monitoring . . . 136
10.4.4 Electrical characteristics overtemperature monitoring . . . 137
10.5 Safe state control (SSOx) . . . 137

Table of contents

10.5.1 Introduction . . . 137
10.5.2 Functional descriptions shutdown path (SSOx) . . . 138
10.5.2.1 Delay times and reaction on detected faults . . . 138
10.5.3 Electrical characteristics shutdown path (SSOx) . . . 140
10.6 Reaction on faults . . . 140
10.6.1 Reaction on detected fault . . . 140
10.7 Analog built-in self test (ABIST) . . . 156
10.7.1 Analog built-in self test (ABIST) - overview . . . 156
10.7.2 ABIST - comparators only . . . 157
10.7.3 ABIST - full path . . . 157
10.7.4 ABIST - configuration and execution . . . 159
10.7.5 ABIST - testing the secondary shutdown path logic . . . 159

11 Interrupt function (INT) . . . 161
11.1 Introduction . . . 161
11.2 Interrupt activation . . . 162
11.3 Interrupt deactivation . . . 162
11.4 Electrical characteristics interrupt (INT) . . . 165

12 Reset function (RESOUT) . . . 166
12.1 Functional description reset function (RESOUT) . . . 166
12.1.1 Introduction . . . 166
12.1.2 Application Reset (REDUCED OPERATION ENABLE) . . . 168
12.1.2.1 Activation . . . 168
12.1.3 System Reset . . . 170
12.1.3.1 Activation . . . 170
12.1.3.2 Hard and Soft reset . . . 171
12.2 Electrical characteristics reset function (RESOUT) . . . 173

13 Microcontroller programming support (MPS) . . . 174

14 SPI . . . 175
14.1 Functional description SPI . . . 175
14.1.1 SPI data transfer . . . 176
14.1.2 SPI frame format . . . 176
14.1.2.1 SPI transfer . . . 176
14.1.2.2 SPI service . . . 177
14.1.2.3 SPI read service . . . 177
14.1.2.4 SPI write service . . . 178
14.1.2.5 CRC field . . . 178
14.1.2.5.1 CRC microcontroller handling . . . 179
14.1.2.5.2 CRC device handling . . . 180
14.1.2.6 Status field . . . 182
14.1.2.6.1 Last frame OK (LFOK) . . . 182
14.1.2.7 Error mechanism . . . 183

Table of contents

14.1.2.8 SPI response with MPS ON . . . 183
14.2 Electrical characteristics SPI . . . 184

15 Reset classes . . . 186
15.1 R0 - Reset class . . . 186
15.2 R1 - Reset class . . . 186
15.3 R2 - Reset class . . . 186
15.4 R3 - Reset class . . . 186
15.5 R3_C1 - Reset class . . . 186
15.6 R3_C2 - Reset class . . . 187

16 Collection registers, error reporting and clearance of bitfields . . . 188
16.1 Error reporting generating an interrupt . . . 188
16.2 Error reporting causing a move to INIT or REDUCED OPERATION . . . 195
16.3 Error reporting causing a move to FAILSAFE . . . 198
16.4 Status reporting - Miscellaneous registers . . . 203

17 Protected registers - Protected write and reflected status registers . . . 204
17.1 Unlock/lock sequence . . . 204

18 Registers description . . . 205
18.1 Registers overview - OTHERSR2 (ascending offset address) . . . 205
18.2 Registers overview - ERR (ascending offset address) . . . 206
18.3 Registers overview - OTHERSR0 (ascending offset address) . . . 206
18.4 Registers overview - OTHERSR1 (ascending offset address) . . . 206
18.5 Registers overview - WATCHDOG (ascending offset address) . . . 207
18.6 Register overview - MISC (ascending offset address) . . . 208
18.7 Registers overview - DEVICEID (ascending offset address) . . . 209
18.8 Device configuration 4 *R2) . . . 210
18.9 Reduced operation reflected status configuration 2 register - *R2) . . . 212
18.10 Protection configuration register - *R2) . . . 213
18.11 Device reflected status configuration Register *R2) . . . 214
18.12 Wake up timer LSB Value (*R2) . . . 216
18.13 Wake up timer MSB Value (*R2) . . . 217
18.14 Wakeup status flags for Application 1 *R2) . . . 218
18.15 Wakeup status flags for Application 2 *R2) . . . 219
18.16 INIT and REDUCED OPERATION Error Status flags for Application 1 *R2) . . . 220
18.17 INIT and REDUCED OPERATION Error Status flags for Application 2 *R2) . . . 222
18.18 Interrupt flags for Application 1 that trigger INT1 *R2) . . . 224
18.19 Interrupt flags for Application 2 that trigger INT2 *R2) . . . 226
18.20 System status flags for Application 1 that trigger INT1 *R2) . . . 228
18.21 System status flags for Application 2 that trigger INT2 *R2) . . . 230
18.22 SPI failure status flags that triggers INT1 *R2) . . . 232
18.23 SPI status flags for Application 2 that trigger INT2 *R2) . . . 233
18.24 Monitor status flags register 2 for Application 1 *R2) . . . 234

Table of contents

18.25 Monitor status flags register 2 for Application 2 *R2) 236
18.26 Over temperature warning and over current status flags *R2) 238
18.27 Over temperature warning /Over current status flags for Application 2 *R2) 240
18.28 Voltage monitor status *R2) 242
18.29 Device status register *R2) 244
18.30 DC-DC switching frequency change *R2) 246
18.31 DC-DC Frequency spread-spectrum control register *R2) 248
18.32 ABIST control 0 *R2) 250
18.33 ABIST control 1 *R2) 251
18.34 ABIST select 0 *R2) 252
18.35 ABIST select 1 *R2) 254
18.36 ABIST select 2 *R2) 256
18.37 Global testmode *R2) 258
18.38 Reduced operation reflected status configuration 1 register - *R2) 259
18.39 ERR0 protection write configuration register *R2) 261
18.40 ERR0 reflected status configuration register *R3) 262
18.41 ERR1 protection write configuration register *R2) 263
18.42 ERR1 reflected status configuration register *R3_C1) 264
18.43 ERR2 protection write configuration register *R2) 265
18.44 ERR2 reflected status configuration register *R3_C2) 266
18.45 Device configuration 1 register *R0) 267
18.46 Device protected write configuration 2 register *R0) 269
18.47 Device reflected status configuration 2 register *R0) 270
18.48 System failure status register for application 1 *R1) 271
18.49 System failure status flags for application 2 *R1) 273
18.50 Short to ground status register for application 1 *R1) 275
18.51 Short to ground status register for application 2 *R1) 277
18.52 Overvoltage status register for application 1 *R1) 279
18.53 Overvoltage status register for application 2 *R1) 281
18.54 Internal supply status register for application 1 *R1) 283
18.55 Internal supply status register for application 2 *R1) 284
18.56 Over temperature status register for application 1 *R1) 285
18.57 Over temperature status register for application 2 *R1) 286
18.58 Protection status *R1) 287
18.59 Reduced operation protected write configuration 1 register - *R1) 288
18.60 Reduced operation protected write configuration 2 register - *R1) 290
18.61 Device protected write configuration 3 register *R1) 291
18.62 Watchdog 1 protected write configuration 0 register *R2) 293
18.63 Watchdog 1 reflected status configuration 0 register - *R3_C1 294
18.64 Watchdog 1 protected write configuration 1 register *R2) 295
18.65 Watchdog 1 reflected status configuration 1 register- *R3_C1 296
18.66 Functional watchdog 1 protected write heart beat timer period configuration register - *R2) . . 297

Table of contents

18.67 Functional watchdog 1 reflected status heart beat timer period configuration register *R3_C1 298
18.68 Window watchdog 1 protected write closed window configuration register - *R2) 299
18.69 Window watchdog 1 reflected status closed window configuration register *R3_C1) 300
18.70 Window watchdog 1 protected write open window configuration register - *R2) 301
18.71 Window watchdog 1 reflected status open window configuration register - *R3_C1) 302
18.72 Window watchdog 1 trigger- *R2) 303
18.73 Functional watchdog 1 response register - *R2) 304
18.74 Functional watchdog 1 response register with synchronization of the heartbeat timer - *R2) . . 305
18.75 Functional watchdog 1 status register - *R3_C1) 306
18.76 Window watchdog 1 error counter status register - *R3_C1) 307
18.77 Watchdog 2 protected write configuration 0 register - *R2) 308
18.78 Watchdog 2 reflected status configuration 0 register- *R3_C2) 309
18.79 Watchdog 2 protected write configuration 1 - *R2) 310
18.80 Watchdog 2 reflected status configuration 1 register - *R3_C2) 311
18.81 Functional watchdog 2 protected write heart beat timer period configuration register - *R2) . . 312
18.82 Functional watchdog 2 reflected status heart beat timer period configuration register *R3_C2) 313
18.83 Window watchdog 2 protected write closed window configuration register - *R2) 314
18.84 Window watchdog 2 reflected status closed window configuration register *R3_C2) 315
18.85 Window watchdog 2 protected write open window configuration register - *R2) 316
18.86 Window watchdog 2 reflected status open window configuration register *R3_C2) 317
18.87 Window watchdog 2 service - *R2) 318
18.88 Functional watchdog 2 response register - *R2) 319
18.89 Functional watchdog 2 response register with synchronization - *R2) 320
18.90 Functional watchdog 2 status register - *R3_C2) 321
18.91 Window watchdog 2 status register - *R3_C2) 322
18.92 Safety switch diagnostics, *R1) 323
18.93 BUCK CORE protected write voltage selection register *R1) 324
18.94 BUCK CORE reflected status voltage selection register *R2) 325
18.95 Buck core voltage selection stat, *R2) 326
18.96 Buck core voltage selection monitors stat, *R2) 327
18.97 Wake Up Timer value after exiting from STANDBY or SLEEP (lower 16 bits) 328
18.98 Wake Up Timer value after exiting from STANDBY or SLEEP (upper 8 bits) 329
18.99 Chip product identifier 330
18.100 Chip product version and revision 331
18.101 Manufacturer ID 332

19 Application information 333
19.1 Application diagram 333
19.2 BOM recommendation 334

20 Package information 341

21 Revision history 342

Table of contents

Disclaimer 343

1 Block diagram

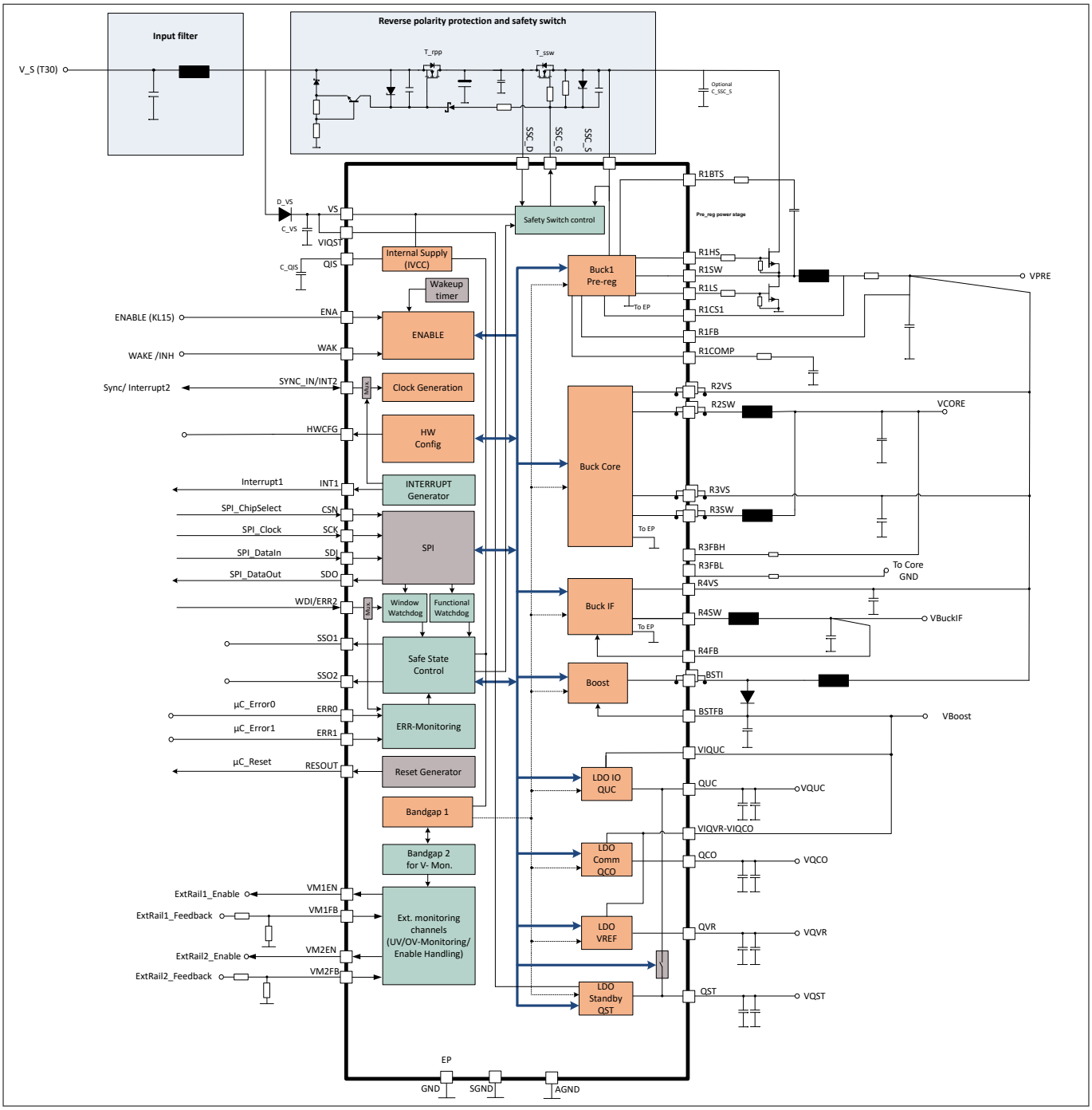


Figure 1 Block diagram

2 Pin configuration

2.1 Pin assignment

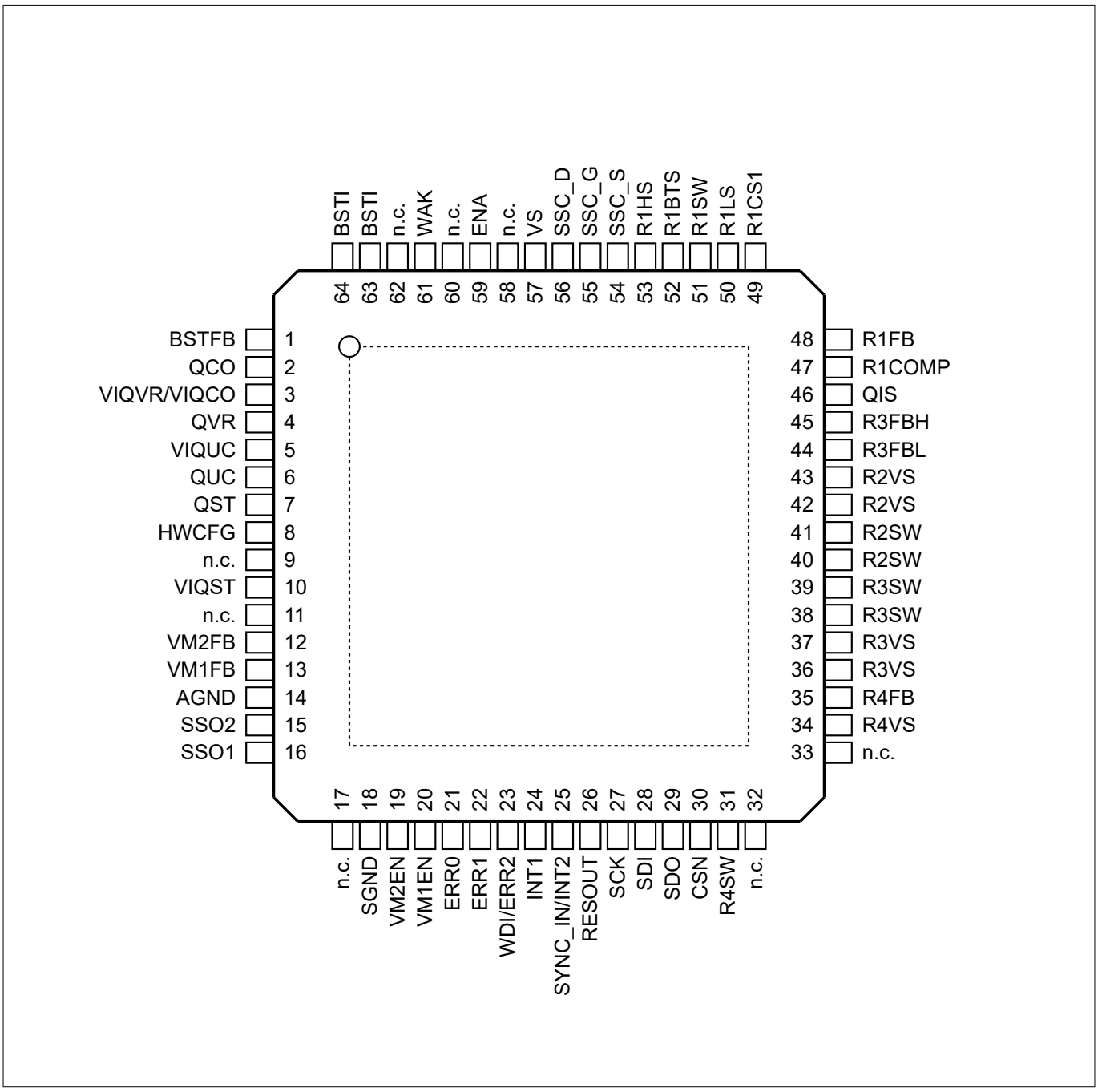


Figure 2 Pin assignment PG-LQFP-64 package

2.2 Pin definitions and functions

Table 1 Pin definitions and functions

Pin	Name	Type	Function

(table continues...)

Table 1 (continued) Pin definitions and functions

1	BSTFB	AI	Boost voltage feedback (connect to R1FB if BOOST not used)
2	QCO	SO	Communication supply voltage
3	VIQVR - VIQCO	SI	Input voltage for voltage reference regulator (QVR) and communication supply regulator (QCO)
4	QVR	SO	ADC reference supply voltage
5	VIQUC	SI	Input voltage for microcontroller IO regulator
6	QUC	SO	Microcontroller IO supply voltage
7	QST	SO	Standby regulator output voltage
8	HWCFG	AO	Hardware configuration setting
9	n.c.	–	Not connected - do not connect to any potential and leave floating
10	VIQST	SI	Input voltage for standby regulator and internal peripherals
11	n.c.	–	Not connected - do not connect to any potential and leave floating
12	VM2FB	AI	Feedback for external voltage monitoring 2
13	VM1FB	AI	Feedback for external voltage monitoring 1
14	AGND	GND	Analog ground connection
15	SSO2	AO	Safe state control output 2
16	SSO1	AO	Safe state control output 1
17	n.c.	–	Not connected - do not connect to any potential and leave floating
18	SGND	GND	Safety ground connection (ground for safety corner SSO1 and SSO2)
19	VM2EN	DIO	Enable for external voltage monitoring 2
20	VM1EN	DIO	Enable for external voltage monitoring 1
21	ERR0	DI	Error monitoring 0 input
22	ERR1	DI	Error monitoring 1 input
23	WDI/ ERR2	DI	Watchdog input/ Error monitoring 2 input WDI option is the default function If REDUCED OPERATION is enabled the integrator must ensure to use the functionality correctly and exclusively use WDI/ERR2 for either one of the watchdogs or ERR2
24	INT1	DO	Interrupt 1 output
25	SYNC_IN/ INT2	DIO	Synchronization input/ Interrupt 2 output
26	RESOUT	DO	Reset output
27	SCK	DI	SPI clock input
28	SDI	DI	SPI data input
29	SDO	DO	SPI data output

(table continues...)

Table 1 (continued) Pin definitions and functions

30	CSN	DI	SPI chip select input
31	R4SW	AO	Switching node buck interface
32	n.c.	–	Not connected - do not connect to any potential and leave floating
33	n.c.	–	Not connected - do not connect to any potential and leave floating
34	R4VS	SI	Input voltage buck interface
35	R4FB	AI	Feedback voltage buck interface regulator
36	R3VS	SI	Input voltage buck core regulator
37	R3VS	SI	Input voltage buck core regulator
38	R3SW	AO	Switching node buck core
39	R3SW	AO	Switching node buck core
40	R2SW	AO	Switching node buck core
41	R2SW	AO	Switching node buck core
42	R2VS	SI	Input voltage buck core regulator
43	R2VS	SI	Input voltage buck core regulator
44	R3FBL	AI	Feedback BUCKCORE regulator: Remote ground GND
45	R3FBH	AI	Feedback buck core regulator
46	QIS	SO	Buffer capacitor for internal supply
47	R1COMP	AO	Buck pre-regulator compensation
48	R1FB	AI	Feedback voltage buck pre-regulator
49	R1CS1	AI	Current feedback shunt positive
50	R1LS	AO	Gate external low side FET for buck pre-regulator
51	R1SW	AI	Switch node pre-regulator
52	R1BTS	SI	Bootstrap input voltage
53	R1HS	AO	Gate external high side FET for buck pre-regulator
54	SSC_S	AI	Safety switch source (If the safety switch is not used, connect to the input of PREREG)
55	SSC_G	AO	Safety switch gate (If the safety switch is not used, connect to the input of PREREG)
56	SSC_D	SI	Safety switch drain (If the safety switch is not used, connect to GND)
57	VS	SI	Main supply voltage
58	n.c.	–	Not connected - do not connect to any potential and leave floating
59	ENA	AI	Enable - edge sensitive
60	n.c.	–	Not connected - do not connect to any potential and leave floating
61	WAK	AI	Wake - level sensitive

(table continues...)

Table 1 (continued) Pin definitions and functions

62	n.c.	–	Not connected - do not connect to any potential and leave floating
63	BSTI	AO	Switch node boost regulator (connect to GND if BOOST not used)
64	BSTI	AO	Switch node boost regulator (connect to GND if BOOST not used)
–	Exposed pad	–	Connect the exposed pad to GND. It is recommended to connect the exposed pad to a heat sink.

Notes:
AI: Analog input
AO: Analog output
AIO: Analog input output
SI: Supply input
SO: Supply output
DI: Digital input
DO: Digital output
DIO: Digital input output

3 General product characteristics

***Note**:*

- *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
- *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as outside the normal operating range. Protection functions are not designed for continuous repetitive operation.*

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings

T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)
1)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Pins							
Input voltage for standby regulator QST	V_{VIQST}	-0.3	–	60	V	–	DS-1661
Safety switch drain	V_{SSC_D}	-0.3	–	60	V	–	DS-1662
Safety switch gate	V_{SSC_G}	-0.3	–	60	V	–	DS-1663
Safety switch source	V_{SSC_S}	-0.3	–	60	V	–	DS-1664
Main supply voltage	V_{VS}	-0.3	–	60	V	–	DS-1665
Enable	V_{ENA}	-0.3	–	60	V	–	DS-1666
Wake	V_{WAK}	-0.3	–	60	V	–	DS-1667
Switch node BUCK PREREG	V_{R1SW}	-2	–	60	V	–	DS-1668
Bootstrap input voltage	V_{R1BTS}	-0.3	–	60	V	–	DS-1669
Gate external high-side FET for BUCK PREREG	V_{R1HS}	-0.3	–	60	V	–	DS-1670
Switch node BOOST regulator	V_{BSTI}	-0.3	–	7	V	–	DS-1671
Current feedback shunt positive	V_{R1CS1}	-0.3	–	7	V	–	DS-1672
Feedback voltage BUCK PREREG	V_{R1FB}	-0.3	–	7	V	–	DS-1673
Input voltage BUCK IF regulator	V_{R4VS}	-0.3	–	7	V	–	DS-1674
Feedback for BUCK IF regulator	V_{R4FB}	-0.3	–	7	V	–	DS-1675
Input voltage BUCK CORE 2 regulator	V_{R3VS}	-0.3	–	7	V	–	DS-1676

(table continues...)

Table 2 (continued) Absolute maximum ratings

T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)
1)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Switch node BUCK CORE 2 regulator	V_{R3SW}	-0.3	–	7	V	–	DS-1677
Switch node BUCK CORE 1 regulator	V_{R2SW}	-0.3	–	7	V	–	DS-1678
Input voltage BUCK CORE 1 regulator	V_{R2VS}	-0.3	–	7	V	–	DS-1679
Compensation	V_{R1COMP}	-0.3	–	7	V	–	DS-1680
Buffer capacitor for internal supply	V_{QIS}	-0.3	–	7	V	–	DS-1681
Feedback BUCK CORE 2 regulator	V_{R3FBH}	-0.3	–	7	V	–	DS-1682
Switch node BUCK IF regulator	V_{R4SW}	-0.3	–	7	V	–	DS-1683
SPI chip select input	V_{CSN}	-0.3	–	6	V	–	DS-1684
Feedback for external voltage monitoring 2	V_{VM2FB}	-0.3	–	60	V	–	DS-1685
Feedback for external voltage monitoring 1	V_{VM1FB}	-0.3	–	6	V	–	DS-1686
SPI data output	V_{SDO}	-0.3	–	6	V	–	DS-1687
SPI data input	V_{SDI}	-0.3	–	6	V	–	DS-1688
SPI clock input	V_{SCK}	-0.3	–	6	V	–	DS-1689
Hardware configuration setting	V_{HWCFG}	-0.3	–	60	V	–	DS-1690
Output voltage for standby regulator QST	V_{QST}	-0.3	–	6	V	Max value increases to 7 V if QUC is OFF and QST is ON	DS-1691
Microcontroller IO supply voltage	V_{QUC}	-0.3	–	6	V	–	DS-1692
Input voltage for microcontroller IO regulator	V_{VIQUC}	-0.3	–	7	V	–	DS-1693
ADC reference supply voltage	V_{QVR}	-0.3	–	6	V	–	DS-1694
Input voltage reference and communication regulator	$V_{VIQVR-VIQCO}$	-0.3	–	7	V	–	DS-1695
Communication supply voltage	V_{QCO}	-0.3	–	6	V	–	DS-1696

(table continues...)

Table 2 (continued) Absolute maximum ratings

T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)
1)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Boost voltage feedback	V_{BSTFB}	-0.3	–	7	V	–	DS-1697
Safe state control output 1	V_{SSO1}	-0.3	–	60	V	–	DS-1698
Safe state control output 2	V_{SSO2}	-0.3	–	60	V	–	DS-1699
Reset output	V_{RESOUT}	-0.3	–	6	V	–	DS-1700
Synchronization input / interrupt output 2	$V_{SYNC\_IN/INT2}$	-0.3	–	6	V	–	DS-1701
Interrupt output 1	V_{INT1}	-0.3	–	6	V	–	DS-1702
Watchdog input / error input 2	$V_{WDI/ERR2}$	-0.3	–	6	V	–	DS-1703
Error input 0	V_{ERR0}	-0.3	–	6	V	–	DS-1704
Error input 1	V_{ERR1}	-0.3	–	6	V	–	DS-1705
Enable for external voltage monitoring 1	V_{VM1EN}	-0.3	–	6	V	–	DS-1706
Enable for external voltage monitoring 2	V_{VM2EN}	-0.3	–	6	V	–	DS-1707
Safety ground connection	V_{SGND}	-0.3	–	0.3	V	AGND, SGND and EP are internally connected	DS-1708
Power ground - exposed pad	V_{EP}	-0.3	–	0.3	V	AGND, SGND and EP are internally connected	DS-1709
Analog ground connection	V_{AGND}	-0.3	–	0.3	V	AGND, SGND and EP are internally connected	DS-1710
Connection to buck core ground	V_{R3FBL}	-0.3	–	0.3	V	Respect to AGND	DS-1711
Gate external low-side FET for BUCK PREREG	V_{R1LS}	-0.3	–	7	V	Respect to AGND	DS-1712
ESD robustness							
ESD voltage HBM parameter	V_{ESD_HBM}	-2	–	2	kV	2) HBM	DS-1732
ESD robustness not corner pins (CDM)	V_{ESD_CDM}	-500	–	500	V	3) CDM	DS-1733
ESD robustness corner pins (CDM)	$V_{ESD\_CDM\_Corner}$	- 750	–	750	V	3) CDM	DS-1734
Differential parameters							
Differential voltage between R1BTS - R1SW	$\Delta V_{R1BTS-R1SW}$	-0.3	–	7	V	$\Delta V_{R1BTS-R1SW} = V_{R1BTS} - V_{R1SW}$	DS-2060

(table continues...)

Table 2 (continued) Absolute maximum ratings

T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)
1)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Differential voltage between R1HS- R1SW	$\Delta V_{R1HS-R1SW}$	-0.3	–	7	V	$\Delta V_{R1HS-R1SW} = V_{R1HS} - V_{R1SW}$	DS-2061
Differential voltage between SSC_G - SSC_S	$\Delta V_{SSC\_G-SSC\_S}$	-0.3	–	7	V	$\Delta V_{SSC\_G-SSC\_S\_max} = V_{SSC\_G} - V_{SSC\_S}$	DS-2062

1) Not subject to production test, specified by design.
2) Human Body Model (HBM) according to JEDEC HBM Human Body Model ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF).
3) Charged Device Model (CDM) according to ESDA STM5.3.1 or ANSI/ESD S.5.3.1.

3.2 Functional range

3.2.1 Functional range description

***Note**: Within the functional or operating range, the device operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.*

3.2.2 Electrical characteristics functional range

Table 3 Functional range

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply voltage for normal operation of internal blocks with BOOST	V_S	3.8	–	36	V	For V_{VS} < 6 V, max temp is 105°C; Same voltage applied to VS and VIQST pins; Device must already be operating *1)*	DS-2143
Supply voltage for normal operation of internal blocks without BOOST	V_S	6	–	36	V	Same voltage applied to VS and VIQST pins *1)*	DS-1932

(table continues...)

Table 3 (continued) Functional range

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Device start-up time	t_{start_up}	–	–	11	ms	From first battery connection to release of microcontroller reset RESOUT; Default reset delay time t_{RD} = 2ms; V_{SSC_S} < 1V at startup; Capacitance at SSC_S pin = 1uF[Max] *1)*	DS-2084
Supply voltage range, load dump	V_{VS_LD}			V_{VS_OV}	V	Load dump condition, device transitions to FAILSAFE mode if severe overvoltage is detected on VS pin; Same voltage applied to VS and VIQST pins; *1)*	DS-2132
PREREG input voltage with boost	V_{SSC_S}	3.8	–	36	V	For V_{SSC_S} ≤ 6.5 V: T_j = -40°C to 25°C; BOOST max load: 650 mA; PREREG max load: 3.5 A (including BOOST load); dV_{SSC_S}/dt ≤ 8 V/ms; PREREG efficiency >= 88% *1)*	DS-2070
PREREG input voltage with boost, high temp	V_{SSC_S}	4.3	–	36	V	For V_{SSC_S} ≤ 6.5 V: T_j = -40°C to 105°C; BOOST max load: 650 mA; PREREG max load: 3.5 A (including BOOST load); dV_{SSC_S}/dt ≤ 8 V/ms; PREREG efficiency >= 88% *1)*	DS-2157
PREREG input voltage without boost	$V_{SSC\_S\_PREREG\_noBOOST}$	6.6	–	36	V	V_{SSC_S} > 6.6V needed for startup without boost; *1)*	DS-2157

(table continues...)

Table 3 (continued) Functional range

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Temperatures							
Junction temperature	T_j	-40	–	175	°C	Continuous operation; 1)	DS-1931
Storage temperature	T_{stg}	-55	–	175	°C	1)	DS-2069

1) Not subject to production test, specified by design

3.3 Thermal resistance

Table 4 Thermal resistance

V_{VS} = 6.0 V to 40 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	4.8	–	K/W	Fixed temperature for bottom 1)	DS-2018
Junction to top	R_{thJTop}	–	16.9	–	K/W	Fixed temperature for top side 1)	DS-2020
Junction to ambient - 2s2p	R_{thJA_2s2p}	–	24.4	–	K/W	JEDEC 2s2p PCB 1) 2)	DS-2022
Junction to ambient - 2s4p	R_{thJA_2s4p}	–	19.3	–	K/W	2s4p PCB 1) 3)	DS-2024

1) Not subject to production test, specified by design
2) Specified R_{thJA} value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with two outside signal Cu traces (2x70µm) and two inner copper layers (2×35µm). Where applicable, a thermal via array next to the package contacted the first inner copper layer.
3) Specified R_{thJA} value is according to internal application board at a natural convection on FR4 2s4p board; the product (chip and package) was simulated on a 74.2 × 74.2 × 1.688 mm^3 board with two outside copper layers (2x53µm) and four inner copper layers (4 × 33 µm Cu). Thermal via array contacted the second and third inner copper layer.

4 DCDC Switching frequency generation and clock synchronization

Table 5 Electrical characteristics DCDC Switching frequency generation and clock synchronization

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
DCDC switching frequency default	f_{DCDC}	2.2 + f_{DCDC_acc}[MIN]	2.2	2.2 + f_{DCDC_acc}[MAX]	MHz	–	DS-1719
DCDC switching frequency accuracy	f_{DCDC_acc}	-10	–	+10	%	–	DS-1720

4.1 Functional description

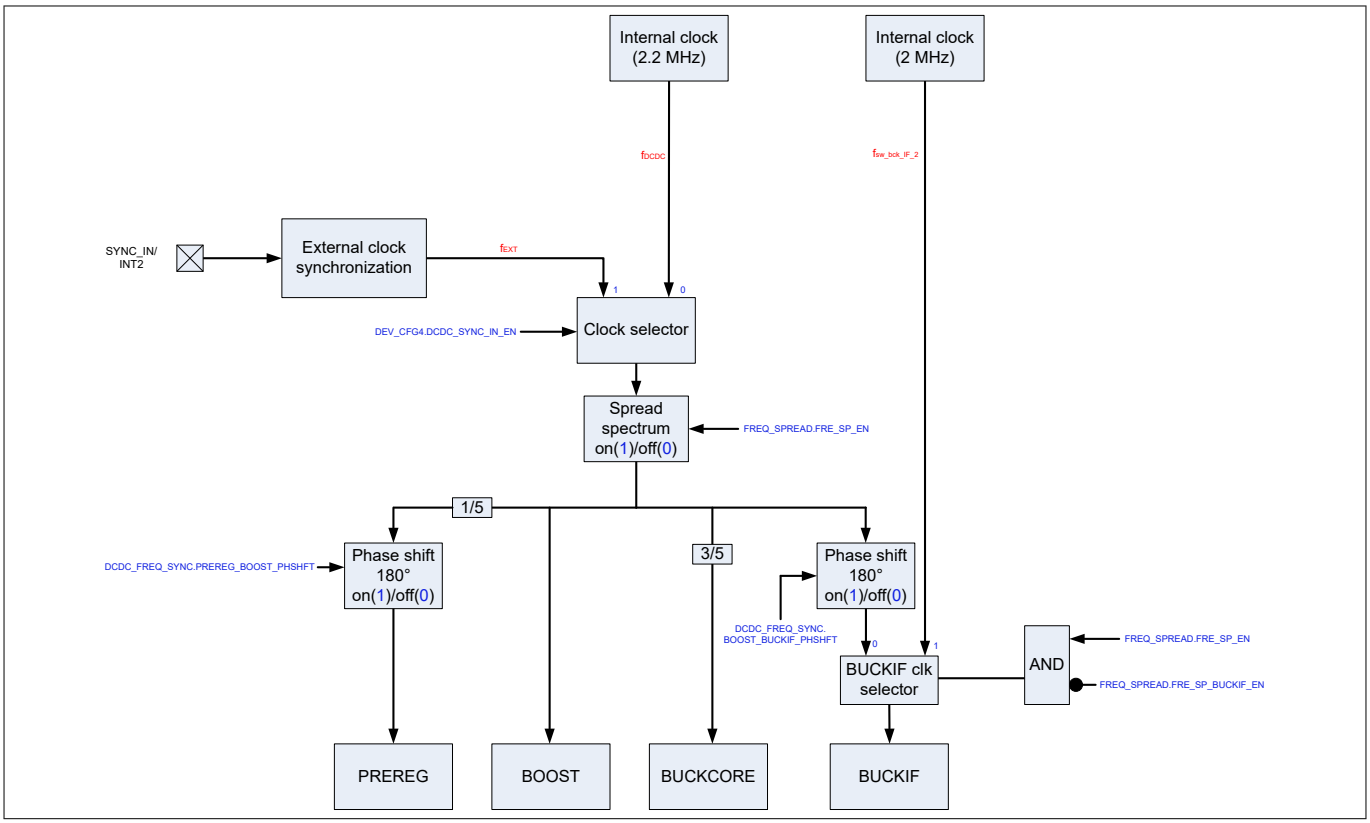


Figure 3 DCDC clock generation and clock manager

The switching frequencies for the different integrated DCDC converters are generated by an integrated clock generator or an external synchronization frequency signal.

The main switching frequency (f_{DCDC}) is adjustable via SPI bitfield **DCDC_FREQ_SYNC.DCDC_FREQSEL,** in the range of 1.8 MHz to 2.4 MHz with 100 kHz step resolution.

External clock synchronization

The device provides an external synchronization of the DC-DC switching frequency f_{DCDC} to an external clock source within the range 1.6 MHz to 2.6 MHz at the SYNC_IN/INT2 pin, to improve the EMC/EMI performance and reduce the cross-talk to the loads.

Synchronization can be enabled or disabled via SPI bit DEV_CFG4.DCDC_SYNC_IN_EN, default is disabled (DEV_CFG4.DCDC_SYNC_IN_EN = 0).

The device handles a change of 100 kHz in the external clock source frequency with a settling time of 50 µs on the switching frequency.

4.1.1 EMC features

Spread spectrum

The device incorporates spread-spectrum modulation to improve EMC/EMI performance. The spread spectrum modulation is applied to the main clock source, hence affects all power converters.

The spread spectrum modulation is disabled by default and can be enabled via SPI bit **FREQ_SPREAD.FRE_SP_EN.**

After enabling the spread spectrum (**FREQ_SPREAD.FRE_SP_EN = 1)**, the device allows to configure the spread spectrum functionality to be applied also to the Buck IF regulator via SPI bit **FREQ_SPREAD.FRE_SP_BUCKIF_EN.**

The configuration of the spread spectrum modulation method, modulation frequency and amplitude can be selected via SPI register **FREQ_SPREAD.**

Phase shift

To further improve the EMC performance, the device allows to configure phase relationship between BUCK PREREG and BOOST regulator and between BUCK IF and BOOST regulator via SPI:

- The device enables 180° phase shift between BOOST and BUCK IF if SPI **DCDC_FREQ_SYNC.BOOST_BUCKIF_PHSHFT** is set to 1.
- The device enables 180° phase shift between BOOST and PREREG if SPI **DCDC_FREQ_SYNC.PREREG_BOOST_PHSHFT** is set to 1.

Slew rate control

Device also provides configurability of switching slew rate for all power converters via SPI register **DCDC_FREQ_SYNC**

5 Power supply function

5.1 BUCK PREREG (buck pre-regulator)

5.1.1 Functional description BUCK PREREG

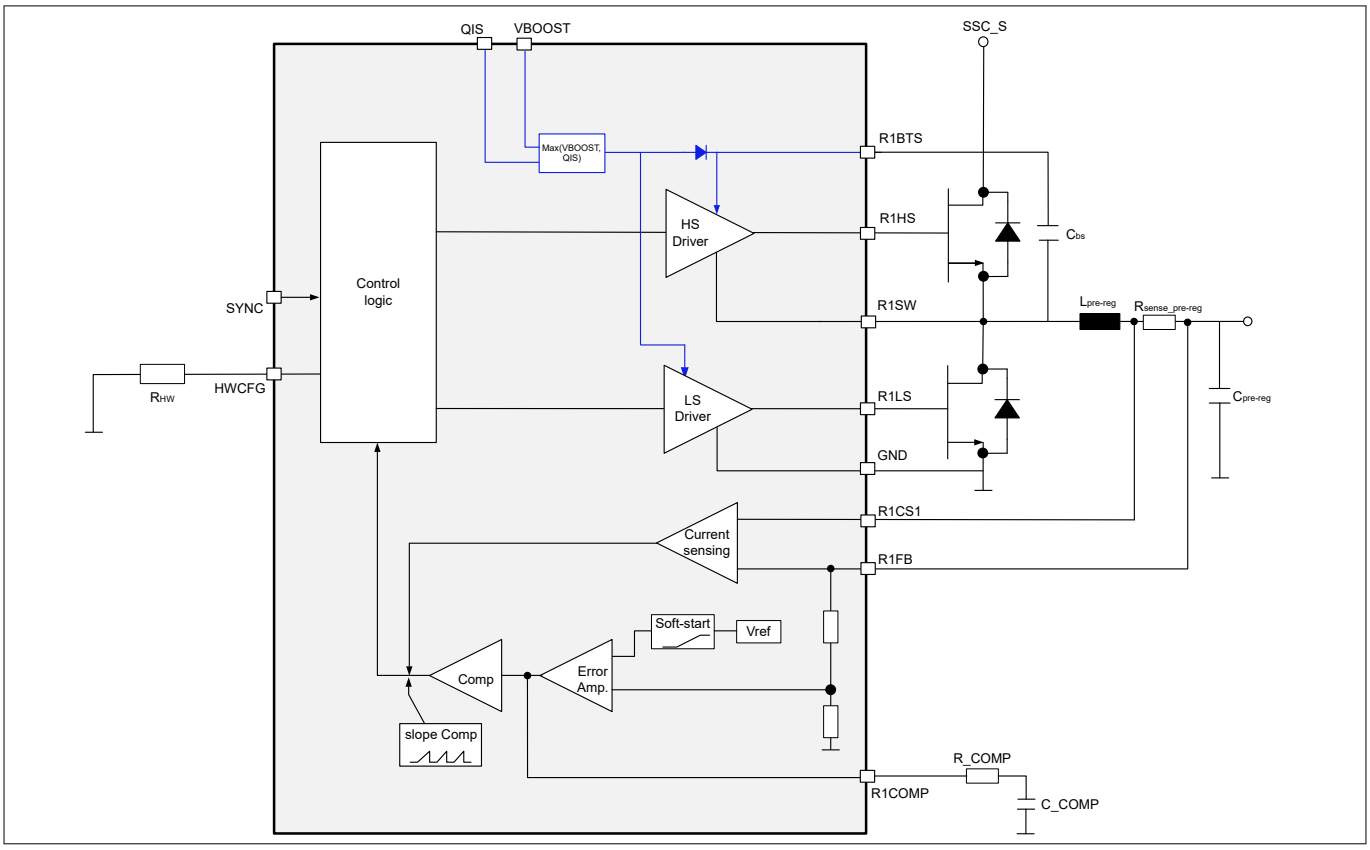


Figure 4 Block diagram PREREG

The pre-regulator is a synchronous buck controller with two external power switches (NMOS, enhanced type) to supply internal circuitry, buck, boost, LDOs and other external loads.

The pre-regulator converts the input voltage at pin SSC_S to an output voltage V_{R1FB} with I_{bck_prereg} output current.

The output voltage of the pre-regulator is configurable by hardware.

Depending on the value of the external resistor on pin HWCFG, the output voltage $V_{R1FB} = V_{R1FB\_4V0}$ or $V_{R1FB} = V_{R1FB\_5V5}$.

The pre-regulator operates in PWM mode with peak current control and outer voltage control loop.

The output current is sensed via an external shunt resistor (R_{sense}) in series with the inductor and the maximum current capability is defined by the external components (NMOS gate charge, inductor, shunt resistor), the gate driver current capability and the switching frequency. An overcurrent detection is implemented to protect the external MOSFETs. If an overcurrent is detected after the HS minimum TON time, the HS is turned OFF and will be turned ON again at the next rising edge of the switching clock. The overcurrent induces a duty cycle reduction that could lead to the output voltage gradually dropping.

The BUCK PREREQ operates with external compensation for external component-references according to the table given below:

Table 6 External filter component buck pre-regulator

1)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
External inductor	L_{PR}	-20 %	6.8	20%	µH	–	DS-1890
External inductor series resistance	$DCRL_{PR}$	–	8	10	mΩ	Max value to guarantee the efficiency	DS-1891
External capacitor	C_{PR}	-20 %	66	20%	µF	–	DS-1892
External capacitor series resistance	R_{C_PR}	–	10	20	mΩ	Max value to guarantee the efficiency and the stability	DS-1893
External bootstrap capacitor	C_{R1BTS}	-20 %	100	20%	nF	–	DS-1894
External bootstrap capacitor resistance	R_{C_R1BTS}	–	50	–	mΩ	–	DS-1895
External sense resistor	R_{sense}	-1%	10	+1%	mΩ	For 10 A current capability	DS-1896
External sense resistor	R_{sense}	-1%	20	+1%	mΩ	For 5 A current capability	DS-1897
External compensation capacitor	C_{comp}	-20 %	1.5	+20 %	nF	For 5 A current capability	DS-1898
External compensation capacitor	C_{comp}	-20 %	2.7	+20 %	nF	For 10 A current capability	DS-1899
External compensation resistance	R_{comp}	-1%	25	+1%	kΩ	For 5 A current capability	DS-1900
External compensation resistance	R_{comp}	-1%	12	+1%	kΩ	For 10 A current capability	DS-1901

1) Not subject to production test

5.1.2 Electrical characteristics BUCK PREREG

Table 7 Electrical characteristics BUCK PREREG

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
4.0 V output voltage	V_{R1FB_4V0}	3.6	4	4.4	V	$V_{SSC\_S} \geq 5.5$ V; dI/dt ≤ 390 A/ms; Output voltage is set to 4 V by HWCFG	DS-1407

(table continues...)

Table 7 (continued) Electrical characteristics BUCK PREREG

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
4.0 V output voltage accuracy	$V_{R1FB\_4V0\_acc}$	3.88	–	4.08	V	Static; $V_{SSC\_S} \geq 5.5$ V	DS-2151
5.5 V output voltage	V_{R1FB_5V5}	4.95	5.5	6.05	V	$V_{SSC\_S} \geq 6.5$ V; dI/dt ≤ 390 A/ms; Output voltage is set to 5V5 by HWCFG	DS-2154
5.5 V output voltage accuracy	$V_{R1FB\_5V5\_acc}$	5.34	–	5.61	V	Static; $V_{SSC_S} \geq 6.5$V	DS-2152
Maximum output current	I_{bck_prereg}	5	–	10	A	Max = 10 A with R_{sense} = 10 mΩ; Max = 5 A with R_{sense} = 20 mΩ; I_{bck_prereg} < 5 A if $V_{SSC_S} \leq 8$V	DS-2155
Sense input current high side	I_{R1CS1}			100	µA	V_{SSC_S} > 3.6 V; I_{bck_prereg} = 0 *1)*	DS-1410
Sense input current low-side	I_{R1FB}			100	µA	V_{SSC_S} > 3.6 V; I_{bck_prereg} = 0 *1)*	DS-1411
Overcurrent peak detection threshold	$V_{shunt\_R1FB\_OC}$	120	150	180	mV	Overcurrent case not including R_{sense} tolerance	DS-1412
Switching frequency	$f_{sw\_bck\_prereg}$	f_{DCDC} [MIN]/5	f_{DCDC} /5	f_{DCDC} [MAX]/5	MHz	$f_{sw\_bck\_prereg} = f_{DCDC}/5$	DS-1413
Soft-start time	$t_{ss\_bck\_prereg}$	–	400	715	us	Voltage at pin V_{R1FB} ramps up from 10% to 90% of V_{R1FB}	DS-1414
Maximum duty cycle	$D_{max\_bck\_prereg}$			98	%		DS-1415
High-side peak sourcing current	I_{R1HS_SRC}	200 * x	–	850 * x	mA	V_{R1HS} - V_{R1SW} from 1 V to 4 V V_{QIS} = 5.5 V I_{R1HS_SRC} is programmable by SPI in DCDC_FREQ_SYNC.PREREG_DRIVER_CONFIG; x:1,2/3,1/3; Default value: 1; *1)*	DS-2087

(table continues...)

Table 7 (continued) Electrical characteristics BUCK PREREG

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
High-side peak sinking current	I_{R1HS_SNK}	200 * x		850 * x	mA	V_{R1HS} - V_{R1SW} from 4 V to 1 V; V_{QIS} = 5.5 V I_{R1HS_SNK} is programmable by SPI in DCDC_FREQ_SYNC.PREREG_DRIVER_CONFIG; x:1,2/3,1/3; Default value: 1; 1)	DS-2088
Low-side peak sourcing current	I_{R1LS_SRC}	200 * x	-	850 * x	mA	V_{R1LS} from 1 V to 4 V; V_{QIS} = 5.5 V; I_{R1LS_SRC} is programmable by SPI in DCDC_FREQ_SYNC.PREREG_DRIVER_CONFIG; x:1,2/3,1/3; Default value: 1; 1)	DS-2089
Low-side peak sinking current	I_{R1LS_SNK}	200 * x		850 * x	mA	V_{R1LS} from 4 V to 1 V; V_{QIS} = 5.5 V I_{R1LS_SNK} is programmable by SPI in DCDC_FREQ_SYNC.PREREG_DRIVER_CONFIG; x:1,2/3,1/3; Default value: 1; 1)	DS-2090
Low-side high level gate output voltage vs. source	ΔV_{R1LS}	3.5	4.5	6	V	$\Delta V_{R1LS} = V_{R1LS} - V_{GND}$; $V_{VS} = V_{VIQST} > 6$ V 1)	DS-1514
High-side high level gate output voltage vs. source	$\Delta V_{HS\_R1HS\_R1SW}$	3.5	4.5	6	V	$\Delta V_{HS\_R1HS\_R1SW} = V_{R1HS} - V_{R1SW}$; $V_{VS} = V_{VQST} > 6$ V 1)	DS-1515
High-side gate rise time	t_{R1HS_r}	23	–	55	ns	V_{R1HS} from 10% to 90%; C_{R1HS} = 3 nF 1)	DS-1516
High-side gate fall time	t_{R1HS_f}	24	–	51	ns	V_{R1HS} from 90% to 10%; C_{R1HS} = 3 nF 1)	DS-1517

(table continues...)

Table 7 (continued) Electrical characteristics BUCK PREREG

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Low-side gate rise time	t_{R1LS_r}	23	–	55	ns	V_{R1LS} from 10% to 90%; C_{R1LS} = 3 nF 1)	DS-1518
Low-side gate fall time	t_{R1LS_f}	24	–	51	ns	V_{R1LS} from 90% to 10%; C_{R1LS} = 3 nF 1)	DS-1519

1) Not subject to production test, specified by design

5.2 BUCK CORE (buck core regulator)

5.2.1 Functional description BUCK CORE

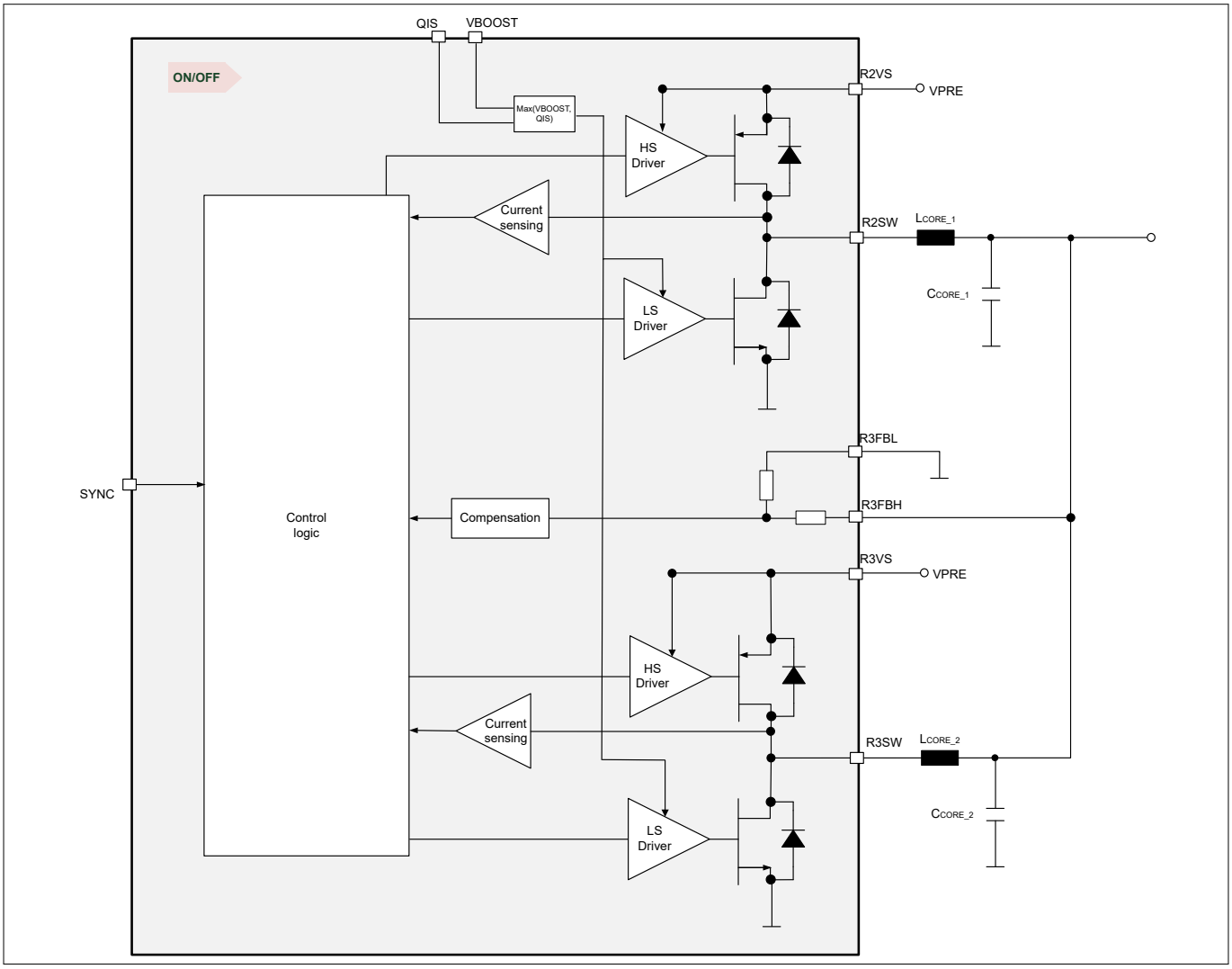


Figure 5 Block diagram BUCK CORE regulator

The device provides a dual phases buck regulator, which generates an output voltage between V_{R3FBH} and V_{R3FBL} with I_{bck_core} output current to supply the microcontroller core.

The default output voltage of the buck core can be read in the SPI register bitfield **VCORESTAT.VOUT.**

The output voltage of the buck core can be adjusted via SPI register bitfield **BUCK_CORE_PW_VSEL.VSEL.**

The device provides voltage scaling based on the request from the SPI interface in the range of V_{R3FBH_rg} with the unit step of V_{R3FBHL_step}. When starting up or recovering from a R1 reset class event (see Reset classes) the regulator starts up with its default value of 1.025 V.

Further default OTP (One Time Programmable) values are available as default options:

0.7 V, 0.8 V, 0.9 V, 0.95 V, 0.9625 V, 0.975 V, 0.9875 V, 1.0 V, 1.0125 V, 1.025 V, 1.0375 V, 1.05 V, 1.15 V

***Note**: The reset value of the respective registers for configuring the output voltage of BUCKCORE (BUCK_CORE_PW_VSEL,BUCK_CORE_RS_VSEL,VCORESTAT,VCOREMONSTAT) does not correspond with the value a user will read upon the device's start-up or recovering from reset event. During the start-up, this register is overwritten with the pre-set default value.*

The undervoltage and overvoltage monitoring thresholds of the buck core are adjusted according to the chosen regulator set point during static voltage scaling.

An overcurrent protection of maximum $I_{OC\_bck\_core}$ in cycle-by-cycle limitation mode is implemented.

The buck core regulator is implemented with an overload protection in the low-side MOSFET with $I_{OL\_bck\_core}$ limit in source-drain direction.

The buck core regulator operates with internal compensation for external component-references according to the table given below:

Table 8 External filter component (BOM) buck core regulator

1)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
External inductor 1	$L_{buck\_core\_1}$	-20 %	1	20%	µH	–	DS-1902
External inductor series resistance 1	$DCR_{L\_buck\_core\_1}$	–	30	37	mΩ	–	DS-1903
External inductor 2	$L_{buck\_core\_2}$	-20 %	1	20%	µH	–	DS-1904
External inductor series resistance 2	$DCR_{L\_buck\_core\_2}$	–	30	37	mΩ	–	DS-1905
External capacitor 1	$C_{buck\_core\_1}$	-20 %	47	20%	µF	–	DS-1906
External capacitor series resistance 1	$ESR_{C\_buck\_core\_1}$	–	–	5	mΩ	–	DS-1907
External capacitor 2	$C_{buck\_core\_2}$	-20 %	47	20%	µF	–	DS-1908
External capacitor series resistance 2	$ESR_{C\_buck\_core\_2}$	–	–	5	mΩ	–	DS-1909

1) Not subject to production test

5.2.2 Electrical characteristics BUCK CORE

Table 9 Electrical characteristics BUCK CORE

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Input voltage	V_{R*VS}	V_{R1FB_4V0}	–	V_{R1FB_5V5}	V	$V_{R*VS} = V_{R2VS} = V_{R3VS}$	DS-1418
Default output voltage	V_{R3FBH}	–	1.025	–	V	–	DS-2085
Maximum output current	$I_{bck\_core\_ph}$	–	–	3.5	A	Per phase	DS-1421

(table continues...)

Table 9 (continued) Electrical characteristics BUCK CORE

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Minimum output current	$I_{bck\_core\_min}$	1	–	–	mA	1)	DS-1428
Overcurrent limitation	$I_{OC\_bck\_core\_ph}$	4.3	–	5.3	A	Per phase	DS-1423
Overload limitation	$I_{OL\ bck\ core\ ph}$	4.3	–	5.3	A	Per phase	DS-1529
Static voltage range	V_{R3FBH_rg}	0.7	–	1.1	V	V_{R3FBH_rg} is programmable (6 bits) between 0.7V and 1.1V via SPI with a default value V_{R3FBH} From 0.7V to 0.8875V: V_{R2VS} = V_{R3VS} = V_{R1FB_4V0}	DS-1419
Static voltage steps	V_{R3FBH_step}	–	12.5	–	mV	–	DS-1530
Switching frequency	$f_{sw\_bck\_core}$	(f_{DCDC}[MIN]/5) × 3	(f_{DCDC}/5) × 3	(f_{DCDC}[MAX]/5) × 3	MHz	–	DS-1531
Static tolerance including ripple	dV_{R3FBHL_stat}	-2	–	+2	%	Under static output load.	DS-1420
Response time for static voltage scaling	$T_{R\_TO\_SVS}$	0.9 * $T_{R\_TO\_SVS}$[typ]	20 + 50 * ((V_{R3FBH_end} - V_{R3FBH_start}) / dV_{R3FBH_step}) + 20	1.1 * $T_{R\_TO\_SVS}$[typ]	us	V_{R3FBH_end} is the target V_{R3FBH} output voltage; V_{R3FBH_start} is the starting V_{R3FBH} output voltage; I_{bck_core} ≥ 200 mA to guarantee the BUCK_CORE response time for static voltage scaling 1)	DS-1422

(table continues...)

Table 9 (continued) Electrical characteristics BUCK CORE

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Peak efficiency	$P_{eff\_bck\_core}$	83	87	–	%	50% of max load (I_{bck_core}/2) including typical external components and excluding board parasitics at RT 1)	DS-1424
Soft-start time	$t_{ss\_bck\_core}$	–	0.5	–	ms	Voltage at pin V_{R3FBH} ramps up from 10% to 90% of V_{R3FBH}	DS-1425
Load step response for high load	dV_{R3FBH_HL}	-0.04 *V_{R3FBH}	–	0.04 *V_{R3FBH}	mV	(1) 0.7 V ≤ V_{R3FBH} ≤ 0.9 V; V_{R2VS} = V_{R3VS} = 4 V; (2) 0.9 V < V_{R3FBH} ≤ 1.1 V; V_{R2VS} = V_{R3VS} = 5.5 V or V_{R2VS} = V_{R3VS} = 4 V; dI_{buck_core} < 1200 mA; 100 mA ≤ I_{bck_core} ≤ 5000 mA; load step rise/fall time = 100 ns; $t_{settling}$ = 10 µs dI_{buck_core} > -1200 mA; 2100mA ≤ I_{bck_core} ≤ 7000mA; load step rise/fall time = 100 ns; $t_{settling}$ = 10 µs series resistance 10mOhm between R3FBH and load (VDD supply pin MCU); series resistance 5 mΩ between R3FBL and load ground (supply ground pin of MCU); Including static output voltage accuracy 1)	DS-2147

(table continues...)

Table 9 (continued) Electrical characteristics BUCK CORE

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Load step response for medium load	dV_{R3FBH_ML}	-0.035*V_{R3FBH}	–	0.035*V_{R3FBH}	mV	(1) 0.7 ≤ V_{R3FBH} ≤ 0.9; V_{R3VS} = 4V (2) 0.9 < V_{R3FBH} ≤ 1.1V; V_{R3VS} = 5.5V or V_{R3VS} = 4V dI_{buck_core} < 500mA; 100mA ≤ I_{bck_core} ≤ 6500mA; load step rise/fall time = 100ns; $t_{settling}$=10µs dI_{buck_core} > -500mA; 600mA ≤ I_{bck_core} ≤ 7000mA; load step rise/fall time = 100ns; $t_{settling}$=10µs series resistance 10mOhm between R3FBH and load (VDD supply pin MCU); series resistance 5mOhm between R3FBL and load ground (supply ground pin of MCU); Including static output voltage accuracy [1)]	DS-2148
Line step response	dV_{R3FBH_line}	-0.015*V_{R3FBH}	–	0.015*V_{R3FBH}	mV	(1) Maximum load: dV/dT = 50 V/ms; step on V_{R2VS} = V_{R3VS} from 3.6 V to 4.4 V if V_{R1FB} = V_{R1FB_4V0}; 100 mA ≤ I_{bck_core} ≤ 7000 mA (2) Maximum load: dV/dT = 50 V/ms; step on V_{R2VS} = V_{R3VS} from 4.95 V to 6.05 V if V_{R1FB} = V_{R1FB_5V5}; 100 mA ≤ I_{bck_core} ≤ 7000 mA [1)]	DS-1429
Internal pull-down resistor	R_{R3FBH_PD}	2.5	–	8.5	Ω	V_{R3FBH} = 1 V	DS-1532
BUCKCORE high side on-resistance (4V0)	$R_{DS(on)\_HS\_BUCKCORE\_4V0}$	–	67	118	mΩ	V_{R1FB} = V_{R1FB_4V0} [1)]	DS-2053
BUCKCORE high side on-resistance (5V5)	$R_{DS(on)\_HS\_BUCKCORE\_5V5}$	–	58	101	mΩ	V_{R1FB} = V_{R1FB_5V5}	DS-2063
BUCKCORE low side on-resistance	$R_{DS(on)\_LS\_BUCKCORE}$	–	33	63	mΩ	–	DS-2146

(table continues...)

Table 9 (continued) Electrical characteristics BUCK CORE

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Switching output slew rate	$SR_{bck\_core\_5V5}$	4.2	–	6.3	V/ns	$V_{R2VS} = V_{R3VS}$ = 5.5 V $SR_{bck\_core\_5V5}$ = 0.8 * V_{R2VS} / trise, where trise is the rise time measured between 10% and 90%. DCDC_FREQ_SYNC.BUCKCORE_DRIVER_CONFIG = 00_b 1)	DS-2094
Switching output slew rate	$SR_{bck\_core\_5V5}$	2.8		5.9	V/ns	$V_{R2VS} = V_{R3VS}$ = 5.5 V $SR_{bck\_core\_5V5}$ = 0.8 * V_{R2VS} / trise, where trise is the rise time measured between 10% and 90%. DCDC_FREQ_SYNC.BUCKCORE_DRIVER_CONFIG = 01_b 1)	DS-2099
Switching output slew rate	$SR_{bck\_core\_5V5}$	1.1	–	3.6	V/ns	$V_{R2VS} = V_{R3VS}$ = 5.5 V $SR_{bck\_core\_5V5}$ = 0.8 * V_{R2VS} / trise, where trise is the rise time measured between 10% and 90%. DCDC_FREQ_SYNC.BUCKCORE_DRIVER_CONFIG = 10_b 1)	DS-2098
Switching output slew rate	$SR_{bck\_core\_4V}$	2.8	–	4.9	V/ns	$V_{R2VS} = V_{R3VS}$ = 4 V $SR_{bck\_core\_4V}$ = 0.8 * V_{R2VS} / trise, where trise is the rise time measured between 10% and 90% DCDC_FREQ_SYNC.BUCKCORE_DRIVER_CONFIG = 00_b 1)	DS-2097

(table continues...)

Table 9 (continued) Electrical characteristics BUCK CORE

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Switching output slew rate	$SR_{bck\_core\_4V}$	1		4.4	V/ns	$V_{R2VS} = V_{R3VS}$ = 4 V $SR_{bck\_core\_4V} = 0.8 * V_{R2VS}$ / trise, where trise is the rise time measured between 10% and 90% DCDC_FREQ_SYNC.BUCKCORE_DRIVER_CONFIG = 01_b 1)	DS-2096
Switching output slew rate	$SR_{bck\_core\_4V}$	0.38	–	1.3	V/ns	$V_{R2VS} = V_{R3VS}$ = 4 V $SR_{bck\_core\_4V} = 0.8 * V_{R2VS}$ / trise, where trise is the rise time measured between 10% and 90% DCDC_FREQ_SYNC.BUCKCORE_DRIVER_CONFIG = 10_b 1)	DS-2095

1) Not subject to production test, specified by design

5.3 BUCK IF (interface regulator)

5.3.1 Functional description BUCK IF

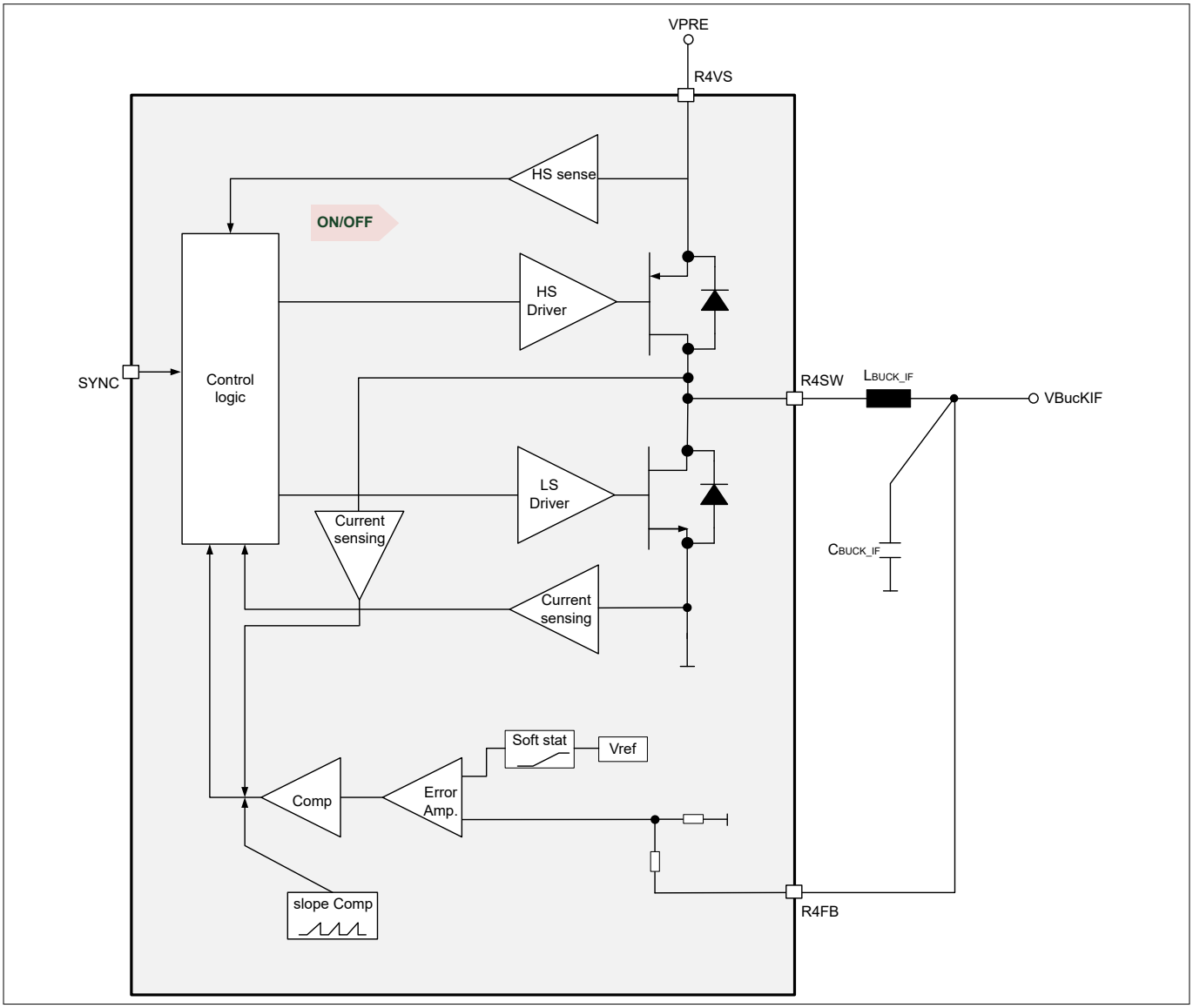


Figure 6 Block diagram BUCKIF

The device provides buck interface regulator which steps down the PREREG output voltage VPRE to an output voltage V_{BUCKIF} with I_{bck_if} output current at pin R4FB.

***Note**: This voltage can be used to supply the high speed interfaces.*

The BUCK IF regulator is implemented with an overcurrent protection of maximum $I_{OC\_bck\_if}$ in cycle-by-cycle limitation mode.

The BUCK IF regulator is implemented with an overload protection in the low-side MOSFET with $I_{OL\ bck\ if}$ limit in source-drain direction.

The device provides an auto detection during start-up if the BUCK IF regulator is used within the application. If not used the pins of BUCKIF must be connected according to the following configuration:

- R4VS: connect to GND
- R4FB: leave open
- R4SW: leave open

***Note**: BUCK IF is excluded from the power sequencing if not used.*

The BUCK IF regulator operates with internal compensation for external component-references according to the table given below:

Table 10 External filter component (BOM) BUCK IF

1)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
External inductor	L_{BUCK_IF}	-20 %	2.2	20%	µH	–	DS-1910
External inductor series resistance	$D_{CRL\_BUCK\_IF}$		20	80	mΩ	Max value to guarantee the efficiency	DS-1911
External capacitor	C_{BUCK_IF}	25	47	(+20 %)	µF	–	DS-1912
External capacitor series resistance	$ESR_{C\_BUCK\_IF}$		8	15	mΩ	Max value to guarantee the efficiency	DS-1913

1) Not subject to production test

5.3.2 Electrical characteristics BUCK IF

Table 11 Electrical characteristics BUCK IF

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Input voltage	V_{R4VS}	V_{R1FB_4V0}	–	V_{R1FB_5V5}	V	–	DS-1431
Output voltage excluding ripple	V_{R4FB}	3.234	3.3	3.366	V	Static output voltage excluding ripple minimum load: $I_{bck\_if} \geq 20mA$ *1)*	DS-1432
Maximum output current	I_{bck_if}	–	–	1.2	A	*1)*	DS-1434
Minimum output current	$I_{buck\_if\_min}$	200	–	–	µA	*1)*	DS-2042
Overcurrent limitation	$I_{OC\_bck\_if}$	1.5	–	2.6	A	–	DS-1435
Peak efficiency	$P_{eff\_bck\_if}$	80	88	–	%	I_{buck_if} from 0.2 A up to 1 A, including typical external components at RT *1)*	DS-1436

(table continues...)

Table 11 (continued) Electrical characteristics BUCK IF

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Switching frequency	$f_{sw\_bck\_IF}$	f_{DCDC} [MIN]	f_{DCDC}	f_{DCDC} [MAX]	MHz	–	DS-1523
Switching frequency 2	$f_{sw\_bck\_IF\_2}$	0.9 * $f_{sw\_bck\_IF\_2}$[typ]	2	1.1 * $f_{sw\_bck\_IF\_2}$[typ]	MHz	Only applicable if: FREQ_SPREAD.FRE_SP_EN = 1 AND FREQ_SPREAD.FRE_SP_BUCKIF_EN = 0	DS-2050
Soft-start time	$t_{ss\_bck\_if}$	–	430	800	µs	Voltage at pin V_{R4FB} ramps up from 10% to 90% of V_{R4FB} 5 mA < I_{R4FB} < 500 mA	DS-2167
Load step response	ΔV_{R4FB_load}	-82	–	82	mV	ΔI_{bck_if} < 500 mA; 20 mA ≤ I_{bck_if} ≤ 500 mA; load step rise/fall time = 100 ns; ΔI_{bck_if} > -500 mA; 520 mA ≤ I_{bck_if} ≤ 1000 mA; load step rise/fall time = 100 ns 1)	DS-1438
Load step response max dynamic range	$\Delta V_{R4FB\_mdr\_load}$	-116	–	116	mV	ΔI_{bck_if} > -700 mA; I_{bck_if} =1000 mA; load step rise/fall time = 100 ns; $t_{settling}$ = 10 µs 1)	DS-1440
Line step response	ΔV_{R4FB_line}	-116	–	116	mV	Step on V_{R4VS} from 3.88 V to 3.66 V in 10 us and from 3.66 V to 3.88 V in 10 us if V_{R1FB} = V_{R1FB_4V0}; Step on V_{R4VS} from 5.61 V to 5.97 V in 10 us and from 5.97 V to 5.61 V in 10 us if V_{R1FB} = V_{R1FB_5V5}; 20mA ≤ I_{bck_if} ≤ 1000mA	DS-1442
Overload limitation	$I_{OL\ bck\ if}$	1.5	–	2.1	A	–	DS-1522
Internal pull-down resistor	R_{R4FB_PD}	3.2	–	21	Ω	–	DS-1524
BUCKIF high side on-resistance (4V0)	$R_{DS(on)\_HS\_BUCKIF\_4V0}$	–	214	372	mΩ	V_{R1FB} = V_{R1FB_4V0} 1)	DS-2055

(table continues...)

Table 11 (continued) Electrical characteristics BUCK IF

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
BUCKIF high side on-resistance (5V5)	$R_{DS(on)\_HS\_BUCKIF\_5V5}$	–	181	309	mΩ	$V_{R1FB} = V_{R1FB\_5V5}$	DS-2065
BUCKIF low side on-resistance (4V0)	$R_{DS(on)\_LS\_BUCKIF\_4V0}$	–	92	158	mΩ	$V_{R1FB} = V_{R1FB\_4V0}$ 1)	DS-2056
BUCKIF low side on-resistance (5V5)	$R_{DS(on)\_LS\_BUCKIF\_5V5}$	–	82	139	mΩ	$R_{DS(on)\_HS\_BUCKIF\_5V5}$	DS-2066
Switching output slew rate	$SR_{bck\_if\_5V5}$	1.8	–	3.5	V/ns	V_{R4VS} = 5.5 V $SR_{bck\_if\_5V5}$ = 0.8 * V_{R4VS} / trise, where trise is the rise time measured between 10% and 90% DCDC_FREQ_SYNC.BUCKIF_DRIVER_CONFIG = 00_b 1)	DS-2100
Switching output slew rate	$SR_{bck\_if\_5V5}$	1.8	–	3.5	V/ns	V_{R4VS} = 5.5 V $SR_{bck\_if\_5V5}$ = 0.8 * V_{R4VS} / trise, where trise is the rise time measured between 10% and 90% DCDC_FREQ_SYNC.BUCKIF_DRIVER_CONFIG = 01_b 1)	DS-2101
Switching output slew rate	$SR_{bck\_if\_5V5}$	1.8	–	3.5	V/ns	V_{R4VS} = 5.5 V $SR_{bck\_if\_5V5}$ = 0.8 * V_{R4VS} / trise, where trise is the rise time measured between 10% and 90% DCDC_FREQ_SYNC.BUCKIF_DRIVER_CONFIG = 10_b 1)	DS-2102

(table continues...)

Table 11 (continued) Electrical characteristics BUCK IF

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Switching output slew rate	$SR_{bck\_if\_4V}$	1.3	–	2.6	V/ns	V_{R4VS} = 4V $SR_{bck\_if\_4V}$ = 0.8 * V_{R4VS} / trise, where trise is the rise time measured between 10% and 90% DCDC_FREQ_SYNC.BUCKIF_DRIVER_CONFIG = 00_b *1)*	DS-2103
Switching output slew rate	$SR_{bck\_if\_4V}$	1.3	–	2.6	V/ns	V_{R4VS} = 4V $SR_{bck\_if\_4V}$ = 0.8 * V_{R4VS} / trise, where trise is the rise time measured between 10% and 90% DCDC_FREQ_SYNC.BUCKIF_DRIVER_CONFIG = 01_b *1)*	DS-2104
Switching output slew rate	$SR_{bck\_if\_4V}$	1.1	–	2.1	V/ns	V_{R4VS} = 4V $SR_{bck\_if\_4V}$ = 0.8 * V_{R4VS} / trise, where trise is the rise time measured between 10% and 90% DCDC_FREQ_SYNC.BUCKIF_DRIVER_CONFIG = 10_b *1)*	DS-2105

1) Not subject to production test, specified by design

5.4 BOOST (boost regulator)

5.4.1 Functional description BOOST

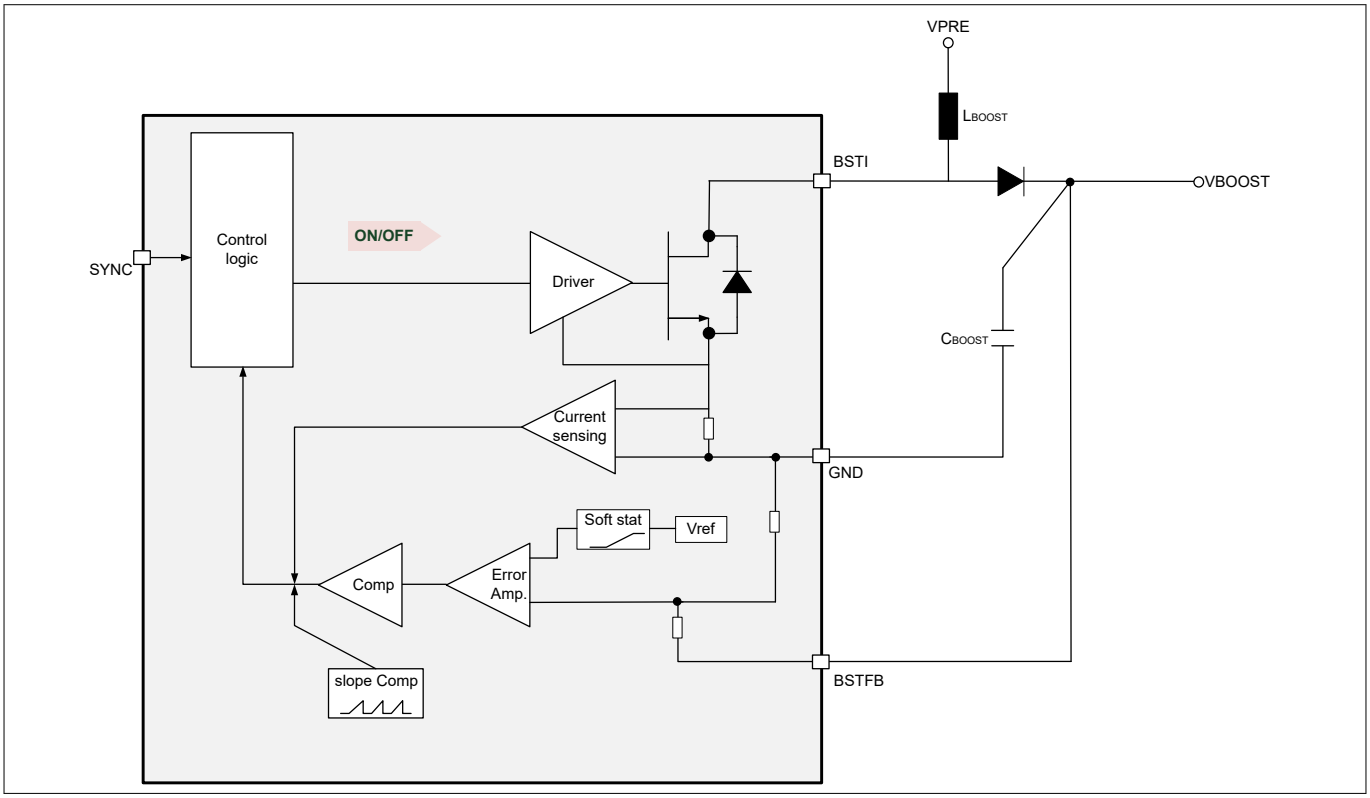


Figure 7 Block diagram BOOST

The device provides a boost regulator which steps up the PREREG output voltage VPRE to an output voltage VBOOST with an external diode to ensure post power blocks.

The device provides an auto detection during start-up if the boost regulator is used within the application. If the BOOST is not used in the application make sure that the following connections of pins BSTI and BSTFB are made:

- BSTI: connect to GND
- BSTFB: connect to R1FB

The boost regulator operates with internal compensation for external component-references according to the table given below:

Table 12 External filter component BOOST

1)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
External inductor	L_{bst}	-20 %	3.3	20%	µH	–	DS-1914
External inductor series resistance	DCR_{L_bst}	–	20	50	mΩ	–	DS-1915
External capacitor	C_{bst}	-20 %	10	20%	µF	–	DS-1916

(table continues...)

Table 12 (continued) External filter component BOOST

1)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
External capacitor series resistance	ESR_{C_bst}	–	10	20	mΩ	–	DS-1917
External Schottky diode forward voltage	V_{Dbst}	–	0.4	0.52	V	@I_{D_boost} =1 A	DS-1951

1) Not subject to production test

5.4.2 Electrical characteristics BOOST

Table 13 Electrical characteristics BOOST

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Input voltage	V_{in_boost}	2.7	–	5.61	V	*1)*	DS-2150
Output voltage	V_{BSTFB}	5.63	5.8	5.97	V	I_{LOAD_BOOST} < 1A: 3.9 V ≤ V_{R1FB_4V0} ≤ 4.1 V, 5.33V ≤ V_{R1FB_5V5} ≤ 5.61 V; I_{LOAD_BOOST} < 0.650 A; 2.59 V ≤ V_{R1FB} ≤ 2.71 V	DS-1447
Load current	I_{LOAD_BOOST}	–	–	1	A	Total load (internal and external load)	DS-1509
Switching frequency	f_{sw_bst}	f_{DCDC} [MIN]	f_{DCDC}	f_{DCDC} [MAX]	MHz	–	DS-1526
Overcurrent limitation	I_{OC_BSTI}	3.5	4	4.5	A	–	DS-1448
Efficiency	P_{eff_bst}	81	85	–	%	Including typical BOM; @27°C; 150mA ≤ I_{LOAD_BOOST} ≤ 950mA *1)*	DS-1449
Soft-start time	t_{ss_boost}	–	650	1000	µs	Voltage at pin V_{BSTFB} ramps up from 10% to 90% of V_{BSTFB}	DS-1450
Pull-down resistor	R_{BSTFB_PD}	12	–	76	Ω	–	DS-1527
BOOST low side on-resistance	$R_{DS(on)\_LS\_BOOST}$	–	114	221	mΩ	–	DS-2057

(table continues...)

Table 13 (continued) Electrical characteristics BOOST

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Switching output slew rate	SR_{bst}	0.50		2.2	V/ns	SR_{bst} = 0.8 * V_{BSTI} / tfall, where tfall is the fall time measured between 10% and 90%. 100mA < I_{bst} < 1A DCDC_FREQ_SYNC.BOOST_DRIVER_CONFIG = 00_b *1)*	DS-2091
Switching output slew rate	SR_{bst}	0.4		1.5	V/ns	S_{R_bst} = 0.8 * V_{BSTI} / tfall, where tfall is the fall time measured between 10% and 90%. 100mA < I_{bst} < 1A DCDC_FREQ_SYNC.BOOST_DRIVER_CONFIG = 01_b *1)*	DS-2092
Switching output slew rate	SR_{bst}	0.15		0.8	V/ns	S_{R_bst} = 0.8 * V_{BSTI} / tfall, where tfall is the fall time measured between 10% and 90%. 100mA < I_{bst} < 1A DCDC_FREQ_SYNC.BOOST_DRIVER_CONFIG = 10_b *1)*	DS-2093

1) Not subject to production test, specified by design

5.5 Communication LDO (QCO)

5.5.1 Functional description communication LDO (QCO)

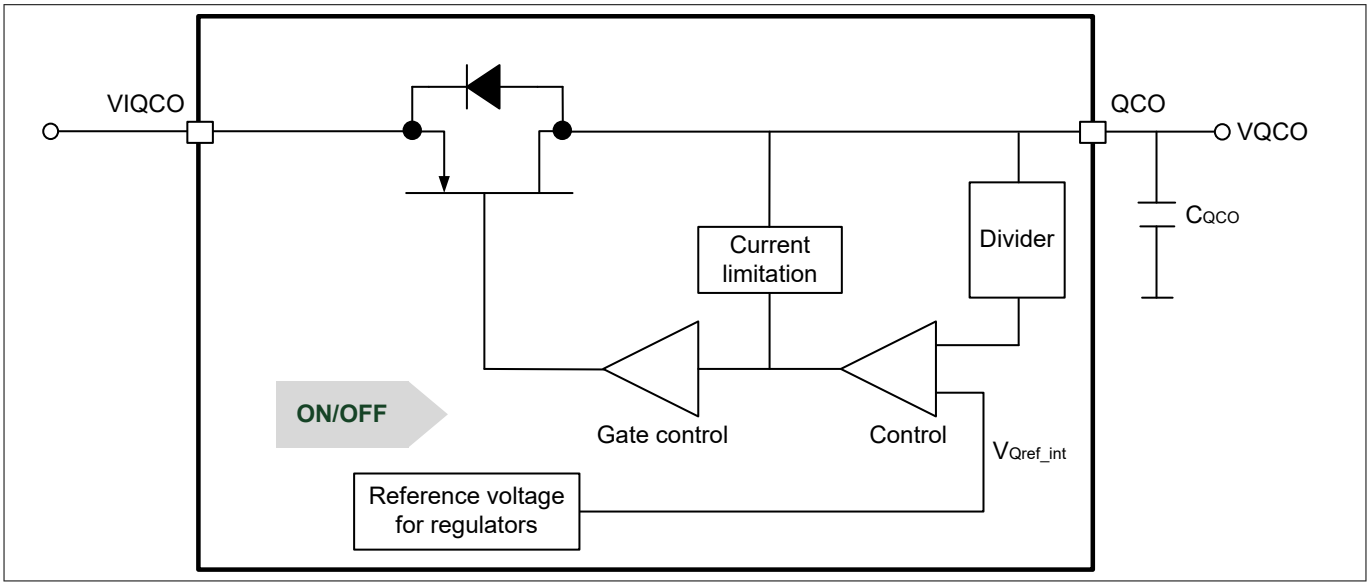


Figure 8 Block diagram LDO-QCO

The device provides a low-dropout-regulator LDO-QCO which generates a regulated output voltage V_{QCO} with I_{QCO} output current to supply the microcontroller. The regulator is supplied from the boost regulator output. As a configuration option, the regulator can also be supplied directly from the pre-regulator output.

The stability of the control loop depends on the load current, the characteristics of the output capacitor and the chip junction temperature. A stable operation is ensured by the output capacitance chosen according to the specified electrical characteristics table below (capacitance value C_{QCO} and equivalent series resistance ESR_{C_QCO}). The output capacitance is either one capacitor or a set of capacitors following the capacitance range as a whole.

***Note**: This voltage can be used to supply the communication device, e.g. CAN transceiver.*

To protect the communication supply from overstress the current limitation limits the output current I_{QCO} to the specified limit I_{QCO_max}.

5.5.2 Electrical characteristics communication LDO (QCO)

Table 14 Electrical characteristics communication LDO (QCO)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output voltage	V_{QCO}	4.9	5	5.1	V	0 mA < I_{QCO} < 600 mA	DS-1453
Output current	I_{QCO}	0	–	600	mA	–	DS-1454
Output current limitation	I_{QCO_max}	650	–	1100	mA	–	DS-1455

(table continues...)

Table 14 (continued) Electrical characteristics communication LDO (QCO)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Drop voltage	V_{dr_QCO}	–	–	500	mV	I_{QCO} < 600 mA	DS-1456
Power supply ripple rejection	$PSRR_{QCO}$	26	–	–	dB	V_{VIQVR_VIQCO} = 5.8V with 100mVpp at 2.2 MHz and Iload ≤ I_{QCO} ESR_{C_QCO} ≤ 50mΩ 1)	DS-1457
Load regulation	ΔV_{QCO}	–	40	70	mV	100 µA < I_{QCO} < 600 mA	DS-1458
Output capacitor	C_{QCO}	1	–	47	µF	1)	DS-1459
Output capacitor equivalent series resistance	ESR_{C_QCO}	–	–	100	mΩ	1)	DS-1460
Soft-start time	t_{ss_QCO}	–	290	500	µs	Voltage at pin QCO ramps up from 10% to 90% of V_{QCO}; -60 mA < I_{QCO} < -5 mA; C_{QCO} = 4.7 µF	DS-2046

1) Not subject to production test, specified by design

5.6 Reference LDO (QVR)

5.6.1 Functional description reference LDO (QVR)

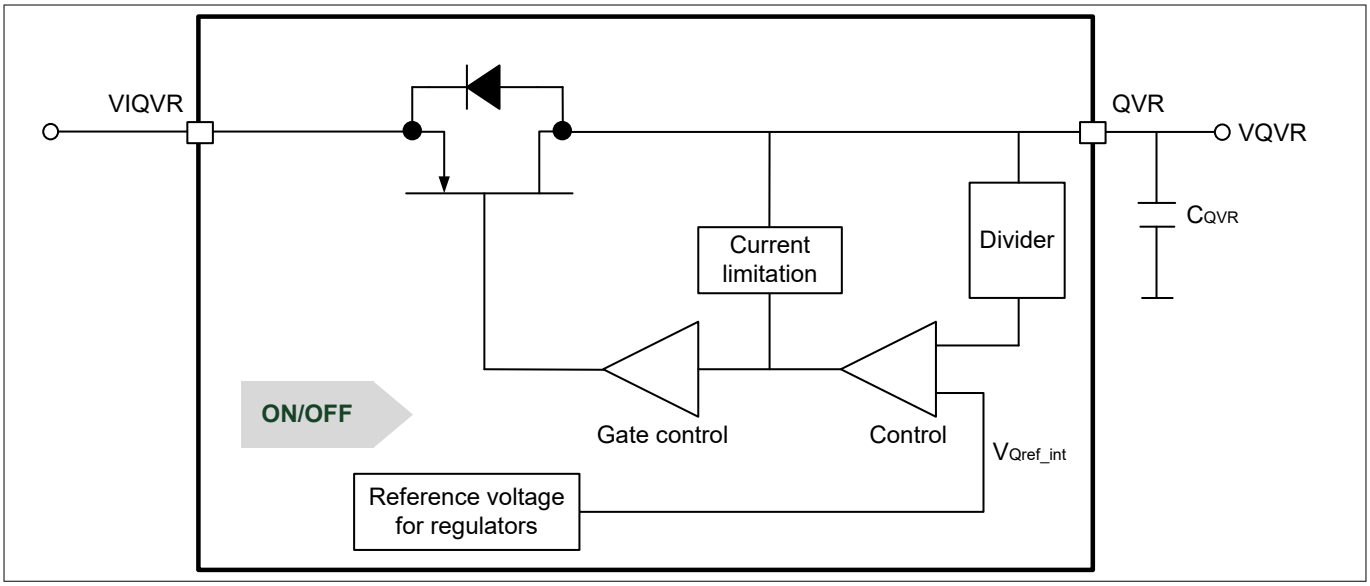


Figure 9 Block diagram LDO-QVR

The device provides a low dropout regulator LDO-VREF which generates a regulated output voltage V_{QVR} with I_{QVR} output current to supply the microcontroller. The regulator is supplied from the boost regulator output. As a configuration option, the regulator can also be supplied directly from the pre-regulator output.

The stability of the control loop depends on the load current, the characteristics of the output capacitor and the chip junction temperature. A stable operation is ensured by the output capacitance chosen according to the specified electrical characteristics table below (capacitance value C_{VREF} and equivalent series resistance ESR_{C_QVR}). The output capacitance is either one capacitor or a set of capacitors following as a whole the capacitance range.

***Note**: This voltage can be used as reference voltage for the ADC in the microcontroller.*

To protect the communication supply from overstress the current limitation limits the output current I_{QVR} to the specified limit I_{QVR_max}.

The status of OC fault can be read via register and can be cleared on write command via SPI once the OC fault is expired.

5.6.2 Electrical characteristics reference LDO (QVR)

Table 15 Electrical characteristics reference LDO (QVR)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output voltage	V_{QVR}	4.95	5	5.05	V	0 mA < I_{QVR} < 150 mA	DS-1462
Output current	I_{QVR}	0	–	150	mA	–	DS-1463
Output current limitation	I_{QVR_max}	170	–	345	mA	–	DS-1464
Drop voltage	V_{dr_QVR}	–	–	400	mV	I_{QVR} < 150 mA	DS-1465
Load regulation	ΔV_{QVR}	–	4.5	9	mV	100 µA < I_{QVR}< 150 mA	DS-1466
Power supply ripple rejection	$PSRR_{QVR}$	26	–	–	dB	V_{IQVR_VIQCO} = 5.8V with 100mVpp at 2.2 MHz and Iload ≤ I_{QVR} ESR_{C_QVR} ≤ 50mΩ *1)*	DS-1467
Output capacitor	C_{QVR}	1	–	10	µF	*1)*	DS-1468
Output capacitor equivalent series resistance	ESR_{C_QVR}	–	–	100	mΩ	*1)*	DS-1469
Soft-start time	t_{ss_QVR}	–	280	520	µs	Voltage at pin QVR ramps up from 10% to 90% of V_{QVR}; -15 mA < I_{QVR} < -5 mA; C_{QVR} = 4.7 µF	DS-2048

1) Not subject to production test, specified by design

5.7 MCU-LDO (QUC)

5.7.1 Functional description MCU-LDO (QUC)

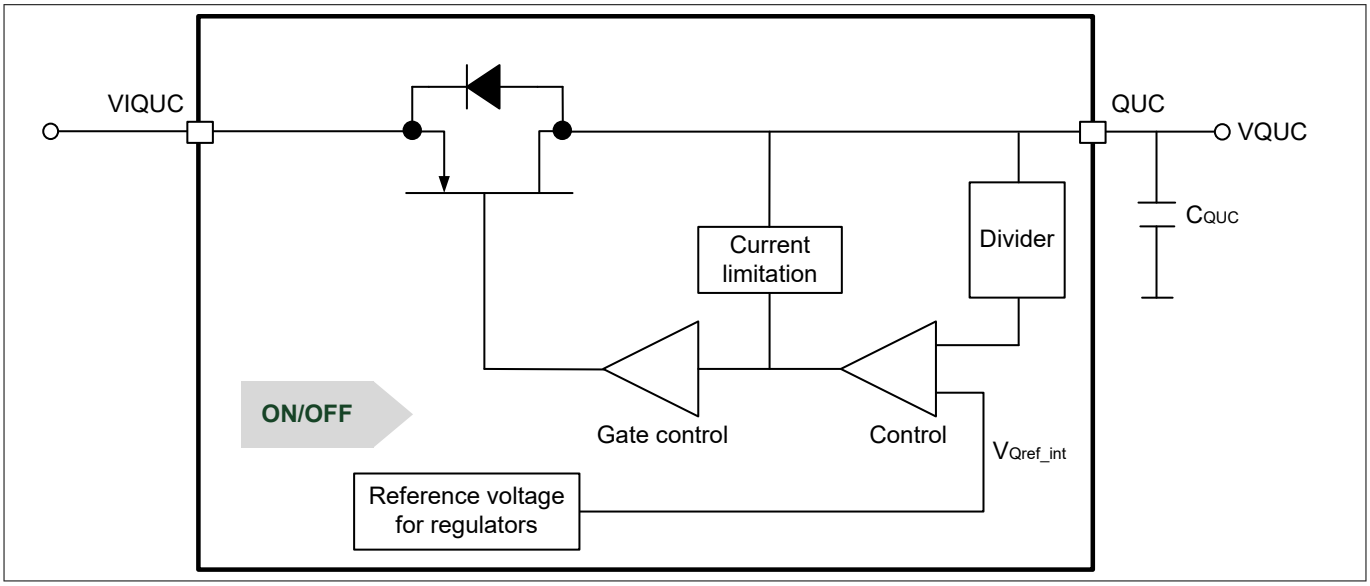


Figure 10 Block diagram LDO-QUC

The device provides a low drop out regulator LDO-QUC which generates a regulated output voltage V_{QUC} with I_{QUC} output current to supply the microcontroller. The regulator is supplied from the boost regulator output. As a configuration option, the regulator can also be supplied directly from the pre-regulator output.

The stability of the control loop depends on the load current, the characteristics of the output capacitor and the chip junction temperature. A stable operation is ensured by the output capacitance chosen according to the specified electrical characteristics table below (capacitance value C_{QUC} and equivalent series resistance ESR_{C_QUC}). The output capacitance is either one capacitor or a set of capacitors following the capacitance range as a whole.

To protect the QUC supply from overstress the current limitation limits the output current I_{QUC} to the specified limit I_{QUC_max}.

***Note**: When the current, sunk from the output pin QUC, is limited, the output voltage V_{QUC} will decrease.*

5.7.2 Electrical characteristics MCU-LDO (QUC)

Table 16 Electrical characteristics MCU-LDO (QUC)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output voltage	V_{QUC}	3.23	3.3	3.37	V	0 mA < I_{QUC}< 600 mA	DS-1472
Output current	I_{QUC}	0	–	600	mA	–	DS-1473
Output current limitation	I_{QUC_max}	650	–	1100	mA	–	DS-1474
Drop voltage	ΔV_{QUC}	–	–	500	mV	I_{QUC} < 600 mA	DS-1476
Load regulation	ΔV_{QUC_load}	–	40	60	mV	100 µA < I_{QUC} < 600 mA	DS-1478

(table continues...)

Table 16 (continued) Electrical characteristics MCU-LDO (QUC)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output capacitor	C_{QUC}	2.2	4.7	22	µF	1)	DS-1479
Output capacitor equivalent series resistance	ESR_{C_QUC}	–	–	100	mΩ	1)	DS-1480
Power supply ripple rejection	$PSRR_{QUC}$	26	–	–	dB	V_{IQUC} = 5.8 V with 100 mVpp at 2.2 MHz and Iload ≤ I_{QUC} ESR_{C_QUC} ≤ 50 mΩ 1)	DS-1481
Soft-start time	t_{ss_QUC}	–	290	500	µs	Voltage at pin QUC ramps up from 10% to 90% of V_{QUC}; -60 mA < I_{QUC} < -5 mA; C_{QUC} = 4.7 µF 1)	DS-2047

1) Not subject to production test, specified by design

5.8 Standby LDO (QST)

5.8.1 Functional descriptions standby LDO (QST)

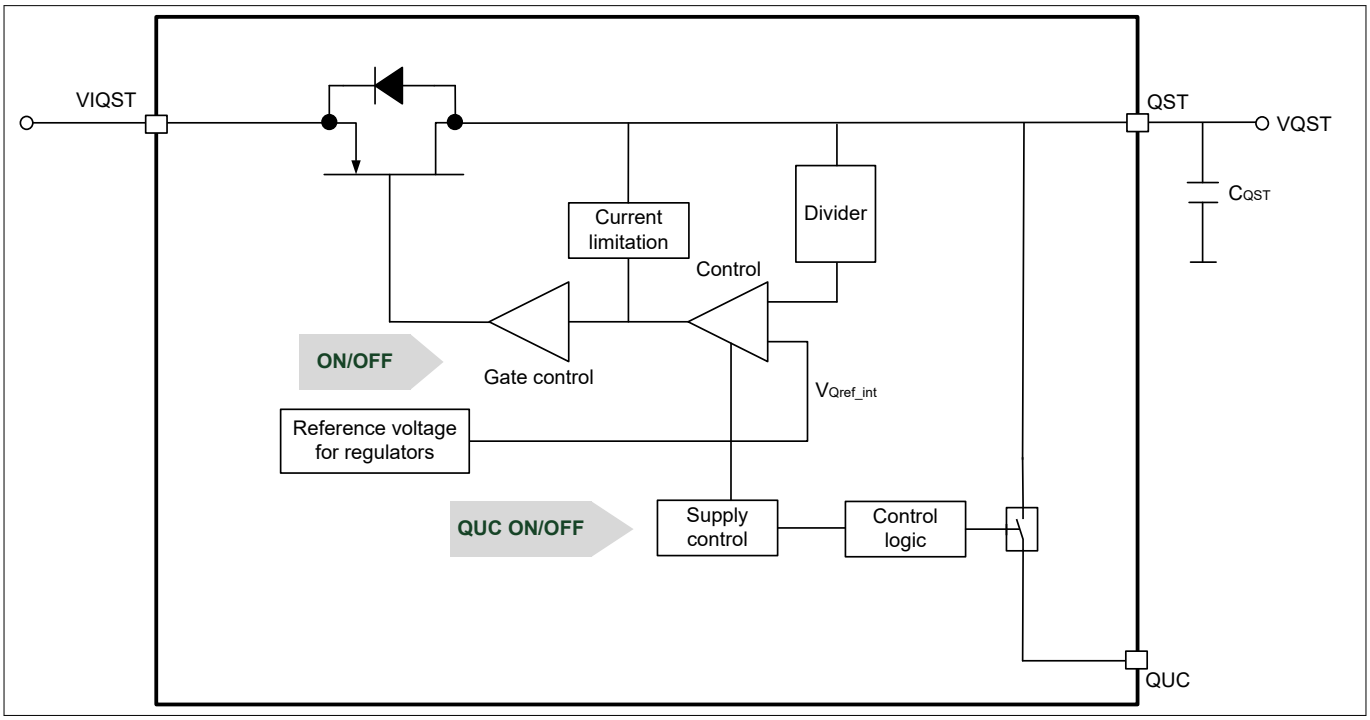


Figure 11 Block diagram LDO QST

The device provides a linear low dropout regulator LDO-QST witch generated a regulated output voltage V_{QST} with I_{QST} output current.

The output voltage V_{QST} at pin QST is generated from the input voltage V_{IQST} after starting up the device.
In case LDO-QUC is enabled, the output voltage V_{QST} is supplied from the input voltage V_{QUC} at pin QUC to optimize the supply topology for higher efficiency.

The stability of the control loop depends on the load current, the characteristics of the output capacitor and the chip junction temperature. A stable operation is ensured by the output capacitance chosen according to the specified electrical characteristics table below (capacitance value C_{QST} and equivalent series resistance ESR_{C_QST}). The output capacitance is either one capacitor or a set of capacitors following as a whole the capacitance range.

The QST regulator can be enabled or disabled by protected SPI communication.
To protect the standby supply from overstress the current limitation limits the output current I_{QST} to the specified limit I_{QST_max}.
The status of OC fault can be read via register and can be cleared on write command via SPI once the OC fault is expired.

***Note**: When the current sunk from the output pin QST is limited, the output voltage V_{QST} will decrease.*

5.8.2 Electrical characteristics standby LDO (QST)

Table 17 Electrical characteristics standby LDO (QST)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output voltage	V_{QST}	3.17	3.3	3.43	V	0 mA < I_{QST} < 30 mA	DS-1487
Output current	I_{QST}	0	–	30	mA	QUC OFF	DS-1498
Output current limitation	I_{QST_max}	40	60	90	mA	QUC OFF	DS-1488
Soft-start time	$t_{ss\_QST.}$	–	255	–	µs	Voltage at pin QST ramps up from 10% to 90% of V_{QST}; -5 mA < I_{QST} < -1 mA; C_{QUC} = 4.7 µF	DS-1497
Transient line regulation 1	$\Delta V_{QST\_tr\_line}$	–	–	70	mV	I_{QST} < 30 mA; V_{IQST} from 10 V to 14 V voltage step in Δt = 30 µs; QUC OFF	DS-1490
Transient line regulation 2	$\Delta V_{QST\_tr\_line2}$	–	–	140	mV	I_{QST} < 30 mA; V_{IQST} from 6 V to 14 V voltage step in Δt = 500 µs; QUC OFF	DS-1491
Load regulation	ΔV_{QST_load}	–	20	40	mV	100 µA < I_{QST} < 15 mA; QUC OFF	DS-1493

(table continues...)

Table 17 (continued) Electrical characteristics standby LDO (QST)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Power supply ripple rejection	$PSRR_{QST}$	30	–	–	dB	Vbatt = 13.5 V, 100 mVpp, ESR <= 50 mOhm, f = 100 Hz and f = 100 kHz 1)	DS-1496
Output capacitor	C_{QST}	0.47	–	10	µF	1)	DS-1494
Output capacitor equivalent series resistance	ESR_{C_QST}	–	–	200	mΩ	1)	DS-1495
Drop voltage RT	ΔV_{QST_RT}	–	–	380	mV	I_{QST} < 30 mA; at T_j = 27°C	DS-1721
Drop voltage HT	ΔV_{QST_HT}	–	–	600	mV	I_{QST} < 30 mA; at T_j = 155°C	DS-1489
Dropout voltage when QUC ON	ΔV_{QUC_QST}	–	–	300	mV	I_{QST} = 30 mA	DS-2003

1) Not subject to production test, specified by design

5.9 Active discharge

Each of the output rails generated by one of the device's regulators, incorporate an active discharge function. This discharge function consists of an internal pull-down resistor. Whenever a regulator is disabled via SPI or switched off due to reaction on detected faults (this also includes state transitions into FAILSAFE), the discharge path is activated and discharges the corresponding output rail. Except for Boost regulator, this discharge feature remains also active while being in SLEEP or STANDBY state if a regulator is not used during this time.

6 Safety switch (SSW)

6.1 Functional description safety switch (SSW)

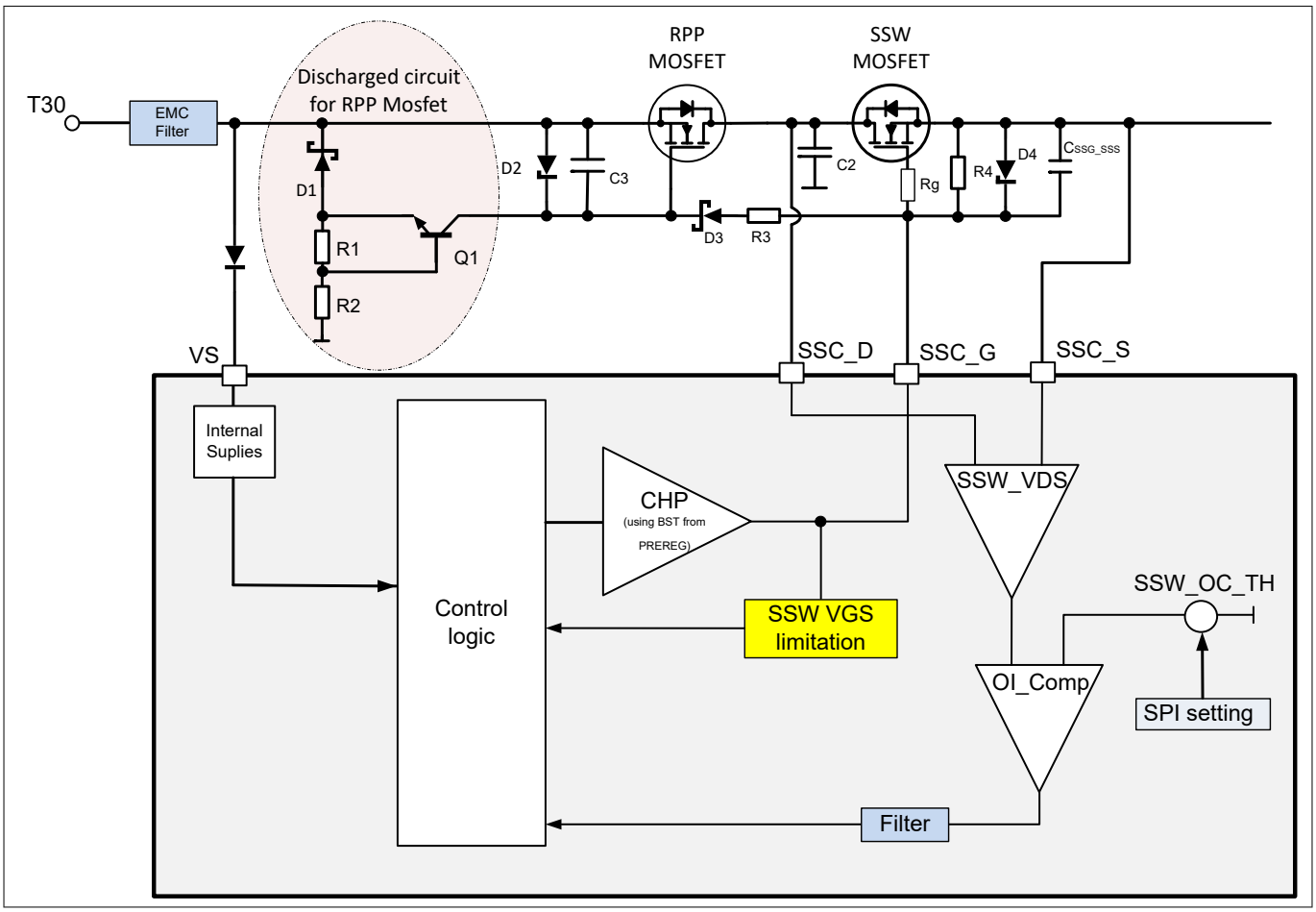


Figure 12 Block diagram SSW & RPP

The device provides a driver to control the external n-channel power MOSFETs (the reverse polarity protection (RPP) MOSFET and the safety switch (SSW) MOSFET).

The gate of both MOSFETs is connected to SSC_G.

The activation of the external power MOSFET is driven according to the failure reaction table and the operation mode.

In case of reverse battery, the Gate of the RPP MOSFET is discharged through the external circuitry.

The source of the SSW MOSFET is connected to pin SSC_S and the drain is connected to SSC_D pin.

The driver circuit includes an over current detection on the SSW MOSFET (Sensing the voltage drop between source and drain).

The threshold for the over current detection is programmable via SPI register bitfield **DEV_PW_CFG2.SSW_OC_TH**.

The overcurrent is detected if the drain source voltage exceeds the detection threshold (SSW_{OC_TH}) for a time longer than the over current detection time (t_{fil_OC}).

The device autodetects at start-up the usage of the input side safety switch protection MOSFET and store the autodetection result into a status register. If the safety switch is not used the corresponding pins must be connected according to the following configuration:

- SSC_D: connect to GND

- SSC_G: connect to input of PREREG
- SSC_S: connect to input of PREREG

6.2 Electrical characteristics safety switch (SSW)

Table 18 Electrical characteristics safety switch

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
High level gate output voltage vs. source	ΔV_{SSG_SSS}	4	4.5	–	V	$\Delta V_{SSG\_SSS} = V_{SSC\_G} - V_{SSC\_S}$; $C_{BTS} > 20 \times C_{SSG\_SSS}$; BUCK PREREG in CCM; $I_{bck\_prereg} \geq 1$ A 1)	DS-1500
[SSW] High level Gate output voltage vs. Source (light load)	ΔV_{SSG_SSS}	3.4	4.5	–	V	$\Delta V_{SSG\_SSS} = V_{SSC\_G} - V_{SSC\_S}$; $C_{BTS} > 20 * C_{SSG\_SSS}$; BUCK PREREG in CCM; $I_{bck\_prereg} < 1$ A 1)	DS-2041
Gate rise time	$t_{SSC\_G\_r}$	–	–	320	µs	ΔV_{SSG_SSS} from 0 V to 4 V $V_{VS} > V_{VS}$[MIN] C_{SSG_SSS} = 3 nF From R1SW rising edge 1)	DS-1501
Gate fall time	$t_{SSC\_G\_f}$	–	–	3	µs	$\Delta V_{SSG\_SSS} = V_{SSC\_G} - V_{SSC\_S}$; ΔV_{SSG_SSS} from 4.0V to 0.7V C_{SSG_SSS} = 1nF $V_{VS} > V_{VS}$ [MIN] 1)	DS-2141
Over current detection threshold for SSW	SSW_{OC_TH}	x * 0.63	x	x * 1.73	V	SSW_{OC_TH} is programmable by SPI; x: 0.755 V, 0.944 V, 1.04 V, 1.22 V; Default value: 0.755V; $V_{SSC_D} \geq 5$V, for x: 0.755V $V_{SSC_D} \geq 6.5$V, for x: 0.944V, 1.04V, 1.22V $V_{VS} > V_{VS}$[MIN]	DS-2136
Filter time for over current detection	t_{fil_OC}	-	60	-	ns	$V_{VS} > V_{VS}$[MIN] 1)	DS-1947

(table continues...)

Table 18 (continued) Electrical characteristics safety switch

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SSW over current detection and reaction time	$t_{SSW\_OC\_SD}$	-	500	-	ns	V_{SSG_SSS} is off $V_{VS} > V_{VS}$[MIN] 1)	DS-1948

1) Not subject to production test, specified by design

7 Wakeup functions

7.1 Introduction

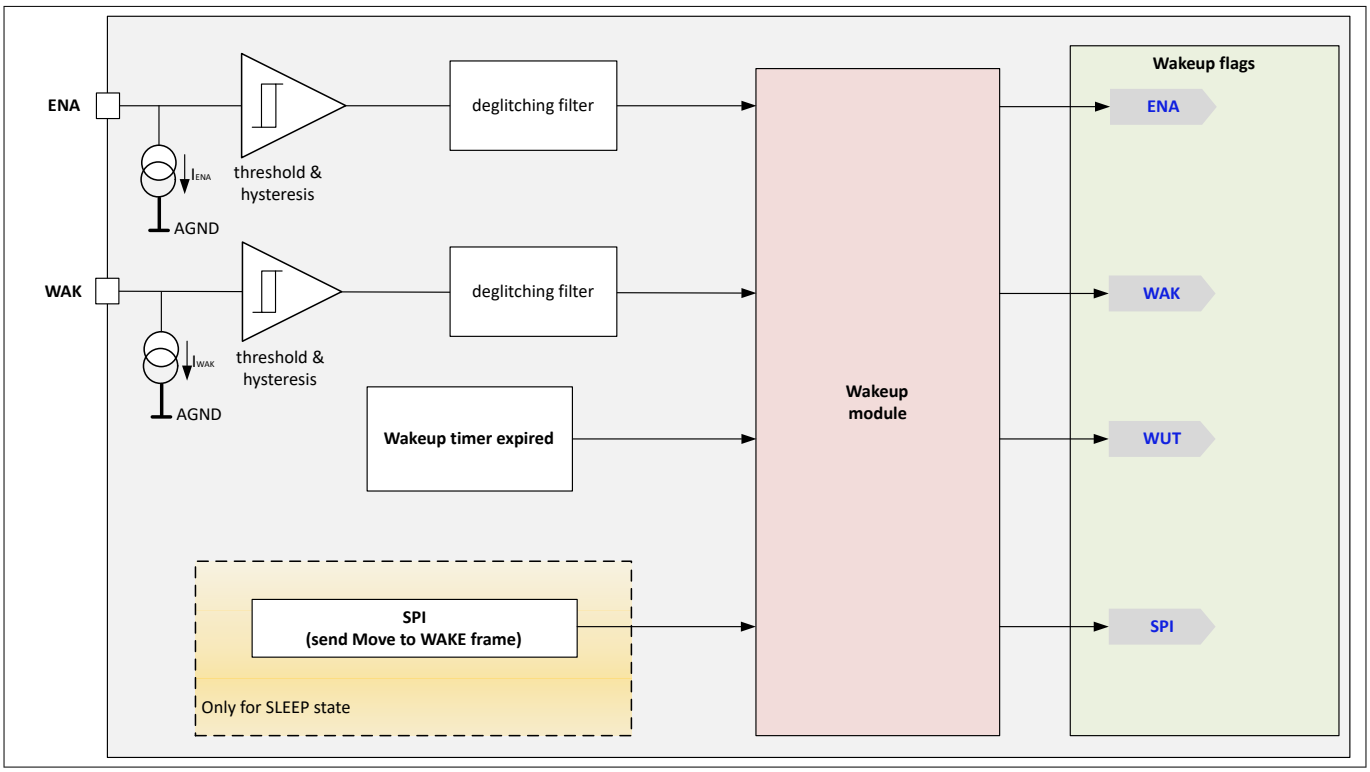


Figure 13 Functional block diagram wakeup functions

The module provides the following wakeup sources:

- ENA pin (edge sensitive input)
- WAK pin (level sensitive input)
- Internal wakeup timer (WUT)
- SPI

To determine which wake-up event caused the device to start-up, the registers **WAKE_STAT_APP1/2** store the following wakeup events:

- ENA
- WAK
- WUT
- SPI

Any wakeup event may trigger a state transition and an interrupt event, see Chapter 9 and interrupt [AutoNumbering].

The ENA wakeup signal is typically a signal from the vehicle ignition switch. The WAK wakeup signal is typically a signal from a transceiver.

7.2 Enable (ENA)

7.2.1 Functional description enable (ENA)

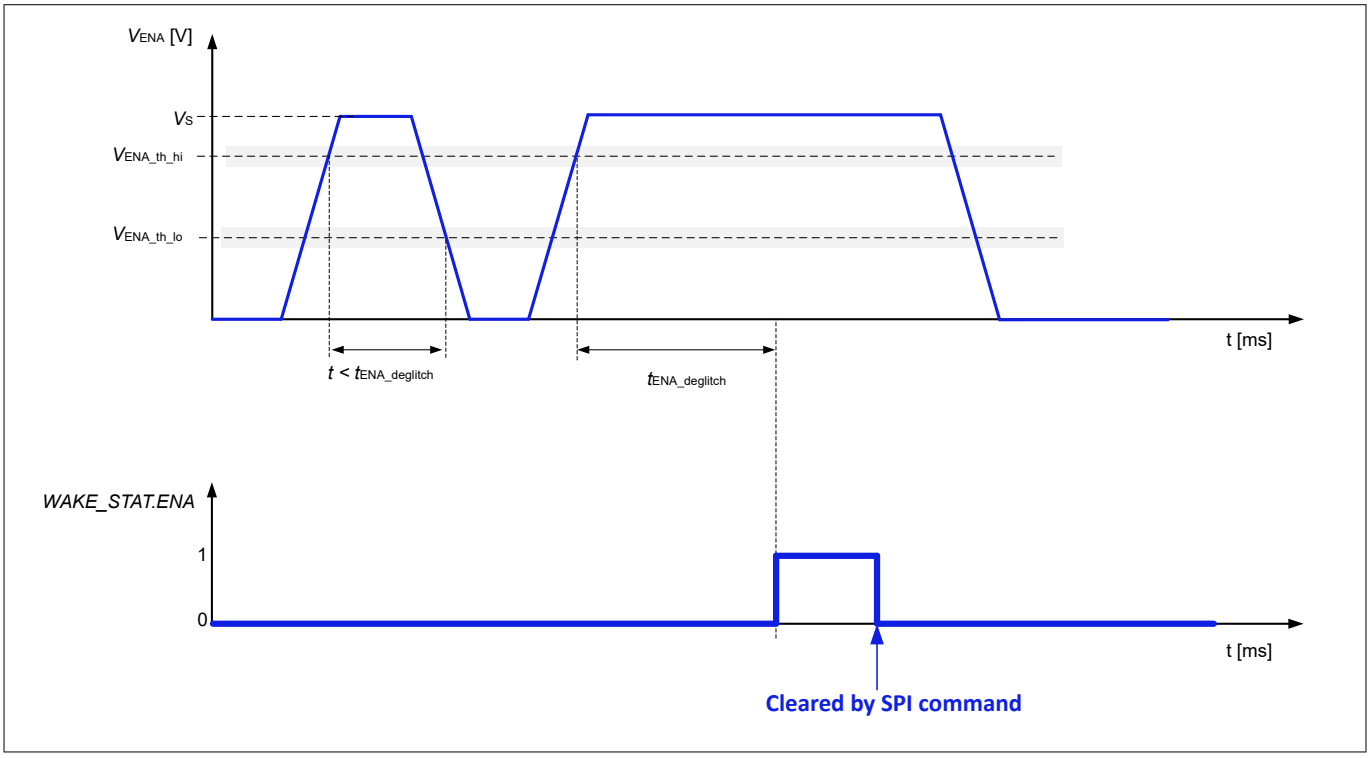


Figure 14 Enable (ENA) signal diagram

The ENA pin is edge sensitive.

Rising edge detection

If the voltage at the ENA pin exceeds the threshold $V_{ENA\_th\_lo}$ and it also exceeds the threshold $V_{ENA\_th\_hi}$ for longer than the deglitch filter time $t_{ENA\_deglitch}$, then the device detects a rising edge.

ENA bit setting

The device sets the **WAKE_STAT_APPx.ENA** bit if an FSM state transition is caused by a rising edge detection at the ENA pin.

The **WAKE_STAT_APPx.ENA** bit can be cleared via SPI, independently of the voltage level at the ENA pin.

7.2.2 Electrical characteristics enable (ENA)

Table 19 Electrical characteristics enable (ENA)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ENA threshold "high" voltage	$V_{ENA\_th\_hi}$	1.3	1.65	2.0	V	V_{ENA} increasing; $V_S \geq 6$ V	DS-1971
ENA threshold "low" voltage	$V_{ENA\_th\_lo}$	1	1.2	1.4	V	V_{ENA} decreasing; $V_S \geq 6$ V	DS-1972

(table continues...)

Table 19 (continued) Electrical characteristics enable (ENA)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ENA deglitch filter time	$t_{ENA\_deglitch}$	20	30	40	µs	$V_S \geq 6$ V	DS-1973
ENA pin "high" input current	I_{ENA_hi}	–	–	5	µA	$V_{ENA} \geq 2$ V	DS-1974
ENA pin "low" input current	I_{ENA_lo}	–	0.1	2	µA	$V_{ENA} \leq 1$ V	DS-1975
ENA threshold hysteresis	V_{ENA_HYST}	200	400	550	mV	$V_S \geq 6$ V	DS-1976

7.3 Wake (WAK)

7.3.1 Functional description wake (WAK)

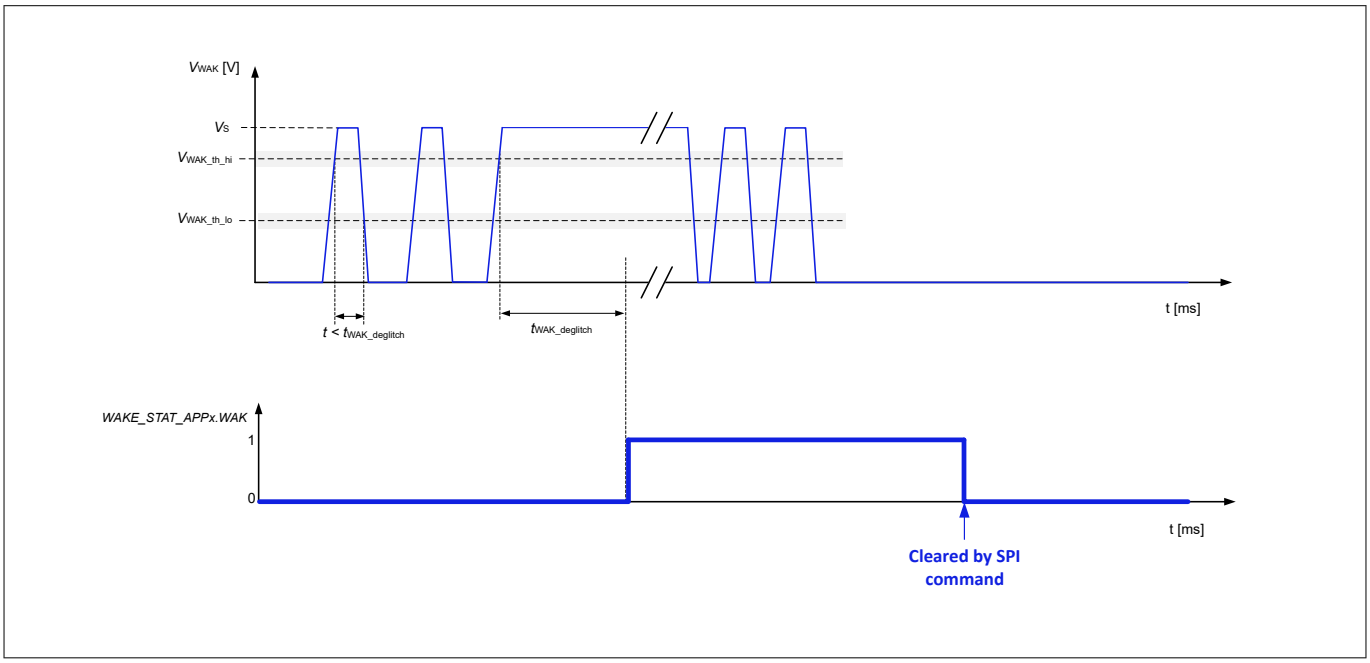


Figure 15 Wake(WAK) signal diagram

The WAK pin is level sensitive.

Level definition

If the voltage level at the WAK pin is below the threshold $V_{WAK\_th\_lo}$ for longer than the deglitch filter time $t_{WAK\_deglitch}$, then it detects a valid "low" signal.

If the voltage level at the WAK pin is above the threshold $V_{WAK\_th\_hi}$ for longer than the deglitch filter time $t_{WAK\_deglitch}$, then it detects a valid "high" signal.

WAK bit setting

The device sets an **WAKE_STAT_APPx.WAK** bit if a wake-up is caused by a valid "high" level detection at the WAK pin

The **WAKE_STAT_APPx.WAK** bit can be cleared via SPI.

7.3.2 Electrical characteristics wake (WAK)

Table 20 Electrical characteristics wake (WAK)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
WAK threshold "high" voltage	$V_{WAK\_th\_hi}$	1.3	1.65	2.0	V	V_{WAK} increasing; $V_S \geq 6$ V	DS-1977
WAK threshold "low" voltage	$V_{WAK\_th\_lo}$	1.0	1.2	1.4	V	V_{WAK} decreasing; $V_S \geq 6$ V	DS-1978
WAK deglitch filter time	$t_{WAK\_deglitch}$	20	30	40	µs	$V_S \geq 6$ V	DS-1979
WAK pin "high" input current	I_{WAK_hi}	–	–	5	µA	$V_{WAK} \geq 2$ V	DS-1980
WAK pin "low" input current	I_{WAK_lo}	–	0.1	2	µA	$V_{WAK} \leq 1$ V	DS-1981
WAK threshold hysteresis	V_{WAK_HYST}	200	400	550	mV	$V_S \geq 6$ V	DS-1982

7.4 Wake-up timer (WUT)

7.4.1 Functional description wake-up timer (WUT)

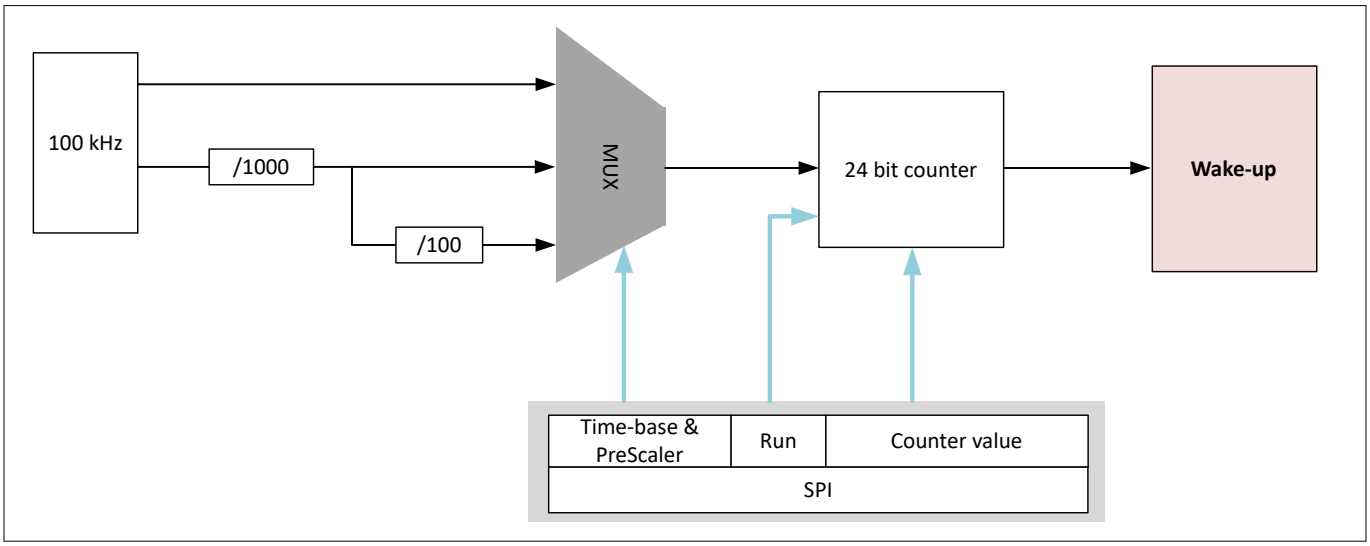


Figure 16 Functional block diagram wake-up timer

Wake-up timer configuration

The wake-up timer value can be configured via SPI in the 24-bit wide wake-up timer registers **WUT_CFG0** and **WUT_CFG1** and the time base can be configured via **DEV_CFG4** register.

The wake-up timer is a 24-bit counter, which operates at a selectable clock frequency of 100 kHz, 1 kHz, 100 Hz or 1 Hz (timebase).

Table 21 Wake-up timer configuration

Timebase		Clock	Timer resolution	Timer range (timebase resolution × timer value)
WUT_CYC	WUT_PRESC			
0	0	100 kHz	10 µs	10 µs to 168 s
0	1	1 kHz	1 ms	1 ms to 4.6 h
1	0	100Hz	10 ms	10 ms to 1.9 days
1	1	1 Hz	1 s	1 s to 194 days

The device allows enabling and disabling the wake-up timer via **DEV_CFG4.WUT_EN**.

Wake-up timer start and stop

On entering STANDBY state or SLEEP state with DEV_CFG4.WUT_EN=1, the counter is loaded with the value of the wake-up timer register and starts decrementing.

The device stops the timer under any of the following conditions:

- The wake-up timer expires
- The device exits SLEEP state or STANDBY state. The remaining timer value can be read back via SPI in order to evaluate the theoretical time left and the corresponding time elapsed (**WUT_STAT0.TIMVALL**, **WUT_STAT1.TIMVALH**, **WUT_STAT1.PRESC**, **WUT_STAT1.CYC**)

Wake-up timer bit

If the wake-up timer expires, the device sets the wake-up timer bit **WAKE_STAT_APPx.WUT = 1**.

The WUT bit can be cleared via SPI.

7.4.2 Electrical characteristic wake-up timer

Table 22 Electrical characteristic wake-up timer

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Wake-up timer accuracy	d_{acc_WUT}	-10	–	10	%	–	DS-2059

7.5 Wake-up via SPI frame

A wake-up via SPI is only available if the device is in SLEEP state and BUCKCORE and QUC are enabled. Only then the device can be woken up by sending a state transition request to WAKE state by writing **DEV_PW_CFG3.FSM_STATEREQ = WAKE** accordingly. Writing any other register that is not involved in a state transition request does not result in a wake-up of the device.

8 Hardware configuration (HWCFG)

Table 23 Electrical characteristics hardware configuration resistor

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
External resistor accuracy	R_{HWCFG_acc}	-5	-	+5	%	1)	DS-2017

1) Not subject to production test, specified by design

8.1 Functional description

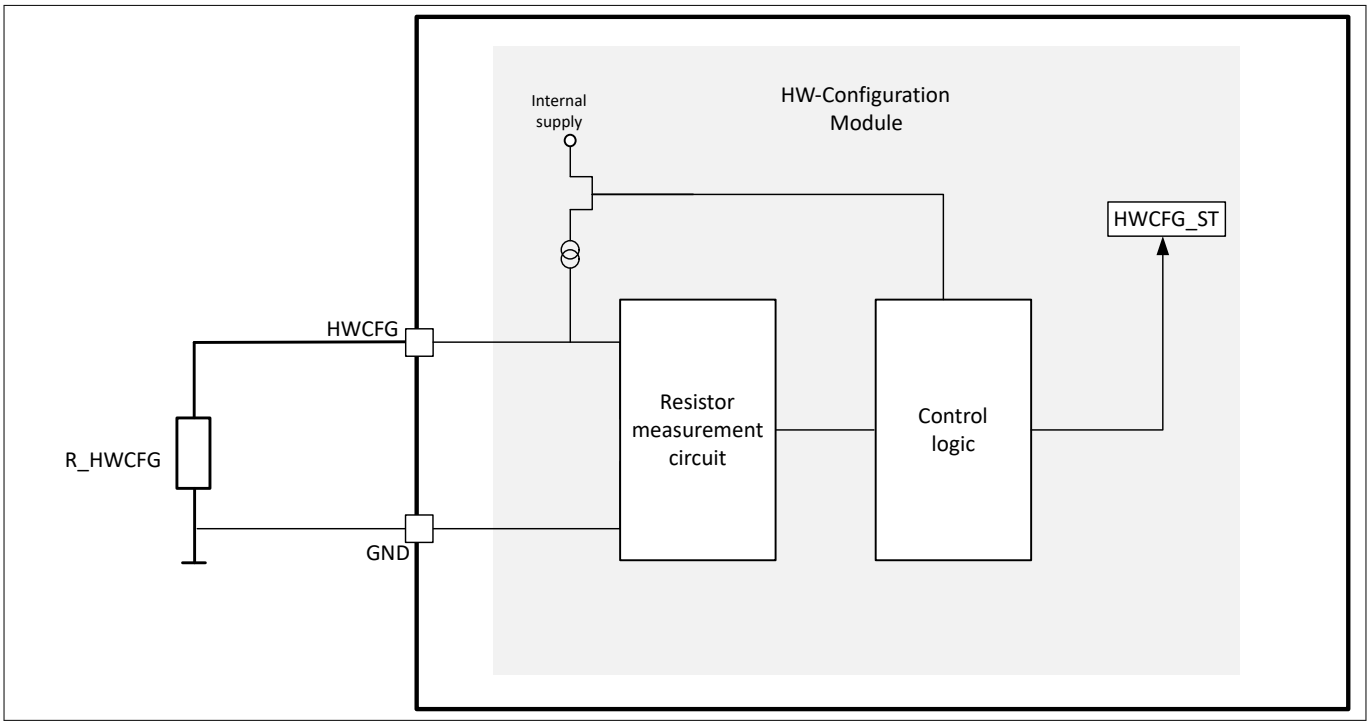


Figure 17 Hardware configuration blockdiagramm

The device provides a hardware configuration module. The external resistor (R_HWCFG) connected on pin (HWCFG) is used to:

- Define the start-up sequence of the internal regulators
- Define the pre-regulator output voltage
- Define the default value of the reset delay time
- Activate the MPS mode

According to the table below.

Table 24 Hardware configuration (HWCFG)

HWCFG resistor setting kΩ, 5% tolerance	RESOUT start-up delay	Pre-regulator output voltage (VPRE)	Start-up sequence of the regulator	MPS mode activation	SPI bits readout DEV_CFG1.HWCFG_STAT
	2 ms/10 ms (TBD)	4V/5V5	Schema (A)/ Schema (B)	ON/OFF	
< 1.0 or GND	10 ms	4V	A	OFF	0000
2.2	2 ms	4V	A	OFF	0001
3.3	2 ms	4V	B	OFF	0010
4.7	10 ms	4V	B	OFF	0011
6.8	2 ms	5V5	A	OFF	0100
10	10 ms	5V5	A	OFF	0101
15	2 ms	5V5	B	OFF	0110
22	2 ms	5V5	B	ON	1001
33	2 ms	5V5	A	ON	1010
47	10 ms	4V	B	ON	1011
68	2 ms	4V	B	ON	1100
100	2 ms	4V	A	ON	1101
150	10 ms	4V	A	ON	1110
> 200 or open	10 ms	4V	A	OFF	1111

After starting up the device, microcontroller can verify the selected setting by reading the SPI status register **DEV_CFG1.HWCFG_STAT** where the HWCFG resistor value is stored

9 State machine (FSM)

9.1 Functional description state machine (FSM)

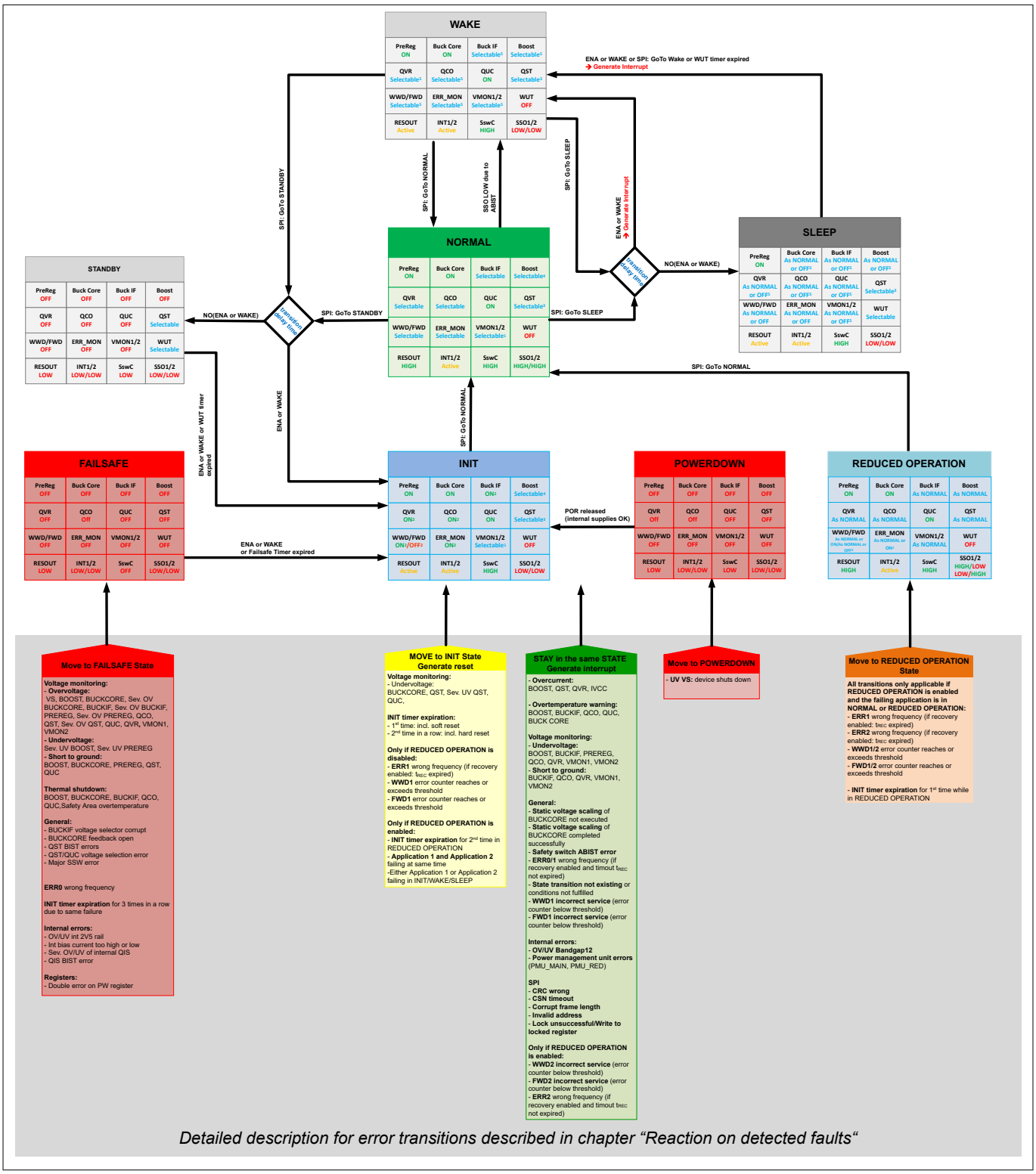


Figure 18 State machine flow diagram

(1): Selectable function during the start-up via VMxEN; can be switched off via SPI. Restarts on entering INIT

(2): Switched ON or OFF at entering the INIT or the REDUCED OPERATION state, then configurable via SPI.

(3): QST supply is on or off, can be configured by SPI when QST_MODE is configured as USER_MODE else QST is on independently of QST_EN when QST_MODE is configured as PMIC_MODE (Default)

(4): Selectable with start-up autodetect only if VPREREG=5V5 nominal. Otherwise it is ON

(5): WD: Can be configured to remain active in SLEEP; all other modules have to be disabled within the same SPI frame that contains the move to SLEEP command; Upon wake-up the modules are restored to the states as they were before the move to SLEEP

9.1.1 Description of the states

The device provides the following states:

- INITIALIZATION states:
  - INIT
  - WAKE
- OPERATIONAL state:
  - NORMAL
- LOW QUIESCENT states:
  - SLEEP
  - STANDBY
- ERROR states
  - FAILSAFE
  - REDUCED OPERATION

9.1.1.1 POWERDOWN state

The POWERDOWN state represents the unpowered condition of the device. The voltage at VS pin is not available.

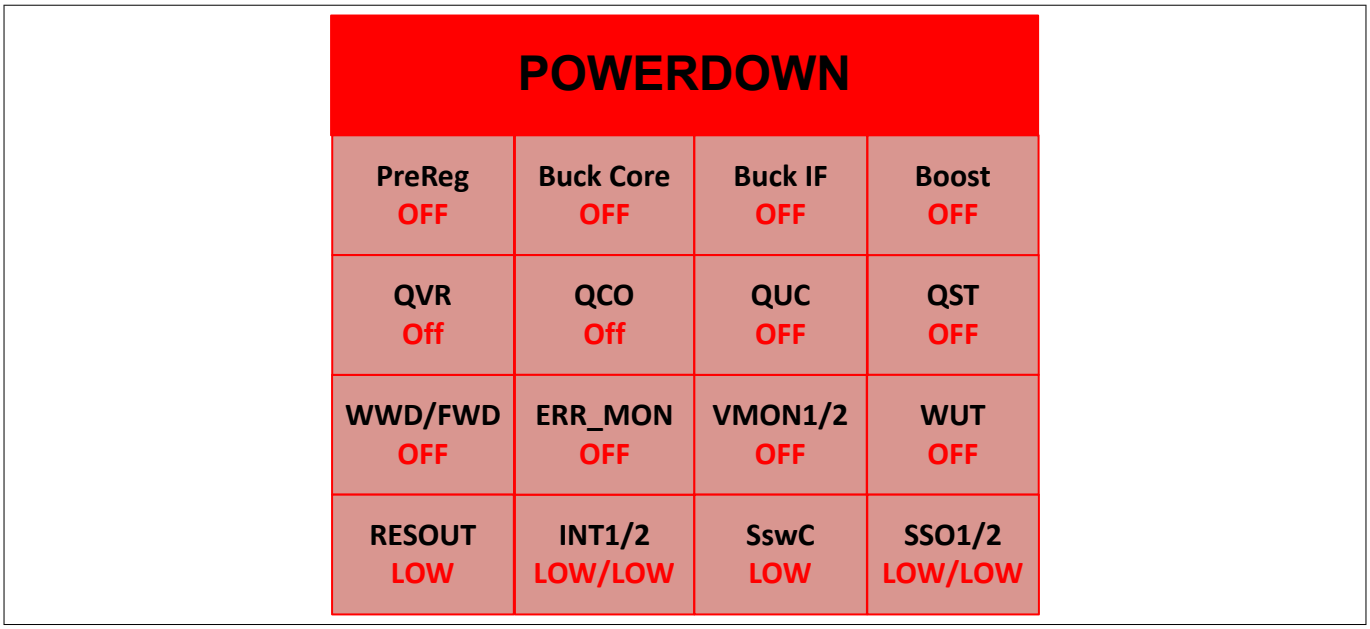


Figure 19 POWERDOWN state

Table 25 POWERDOWN state

Part/Function	Value	Description
PreReg	OFF	Pre-regulator is off
Buck Core	OFF	Core supply is off
Buck IF	OFF	Buck regulator for interface supply is off
Boost	OFF	Boost regulator is off
QVR	OFF	Voltage reference is off
QCO	OFF	Communication supply is off
QUC	OFF	Microcontroller supply is off
QST	OFF	Standby supply is off
WWD/FWD	OFF	Watchdog is off
ERR_MON	OFF	Error monitoring function ERR MON is off
VMON1/2	OFF	External voltage monitoring VMON1/2 is off
WUT	OFF	Wake up timer (WUT) is off
RESOUT	LOW	RESOUT output is low
INT1/2	LOW	Interrupt outputs are low
SswC	LOW	External safety switch is off
SSO1/2	LOW	Safe state outputs are low

9.1.1.2 INIT state

In INIT state the device starts up its internal supplies, as well as the external voltage rails as configured. Upon every entry RESOUT will be pulled low for tRD_2ms/tRD_10ms or to its configured value and released again after the power-up sequence was executed. If rails are still at their nominal voltage upon entry, they are skipped in the power-up sequence. Internal checks are being performed and the device waits for successful initialization by the microcontroller before the INIT timer t_{INIT} expires.

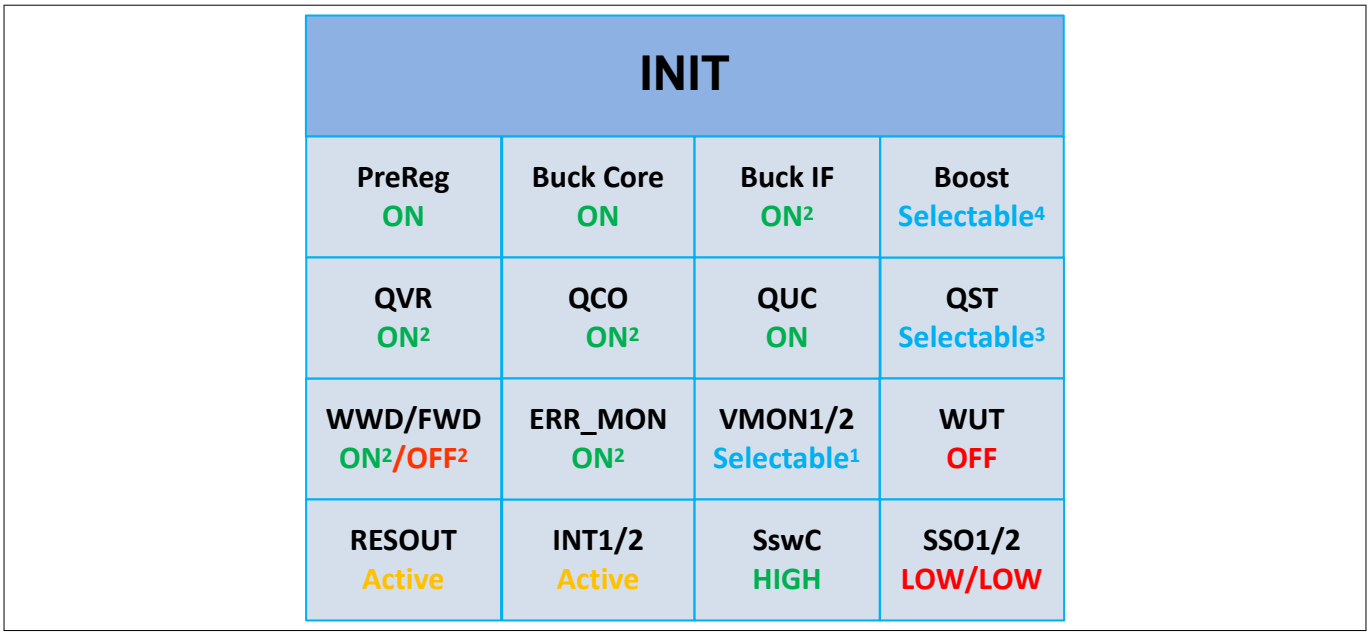


Figure 20 INIT state

Table 26 INIT state

Part/Function	Value	Description
PreReg	ON	Pre-regulator is on
Buck Core	ON	Core supply is on
Buck IF	ON	Buck regulator for interface supply is on, if automated use-detection identified the usage; then configurable via SPI
Boost	Selectable	Boost regulator is selectable with start-up autodetect only if V_{OUT_PreReg} = 5V5 nominal otherwise, it is on.
QVR	ON	Voltage reference is on; then configurable via SPI
QCO	ON	Communication supply is on; then configurable via SPI
QUC	ON	Microcontroller supply is on
QST	Selectable	Standby supply is selectable when QST_MODE is configured as USER_MODE otherwise, it is on when QST_MODE is configured as PMIC_MODE (default)
WWD	ON	Window watchdog is on; then configurable via SPI
FWD	OFF	Functional Watchdog is off; then configurable via SPI
ERR_MON	ON	Error monitoring function ERR MON is on; then configurable via SPI
VMON1/2	Selectable	External voltage monitoring VMON1/2 is on, if automated use-detection identified the usage; can be switched off by SPI
WUT	OFF	Wake-up timer (WUT) is off
RESOUT	Active	RESOUT output released ("high") after power-up sequence has finished and reset delay time has expired

(table continues...)

Table 26 (continued) INIT state

Part/Function	Value	Description
INT1/2	Active	Interrupt outputs are active (INT2 only active if "REDUCED OPERATION" is enabled)
SswC	High	External safety switch is on
SSO1/2	LOW	Safe state outputs are low

***Note**:*

The Move to NORMAL SPI command is not executed:

- *900µs after move to INIT because of execution of auto detection*
- *Until all enabled voltage rails are in regulation (above UV threshold). Note: all regulators are switched on again at move to INIT (if disabled before)*

In general the application is not exposed to this limitation due to RESOUT at low level but with the following exceptions:

- *with low tRD values (<1ms)*
- *in case MPS is ON (the RESOUT stays high for WDs/ERRs monitoring faults and therefore the application can be exposed to such limitation).*

9.1.1.3 NORMAL state

Device has a NORMAL state and the only state where safe state outputs (SSO1/2) are high.

***Note**: In this state the device is suppling the microcontroller and the peripheral blocks in the application.*

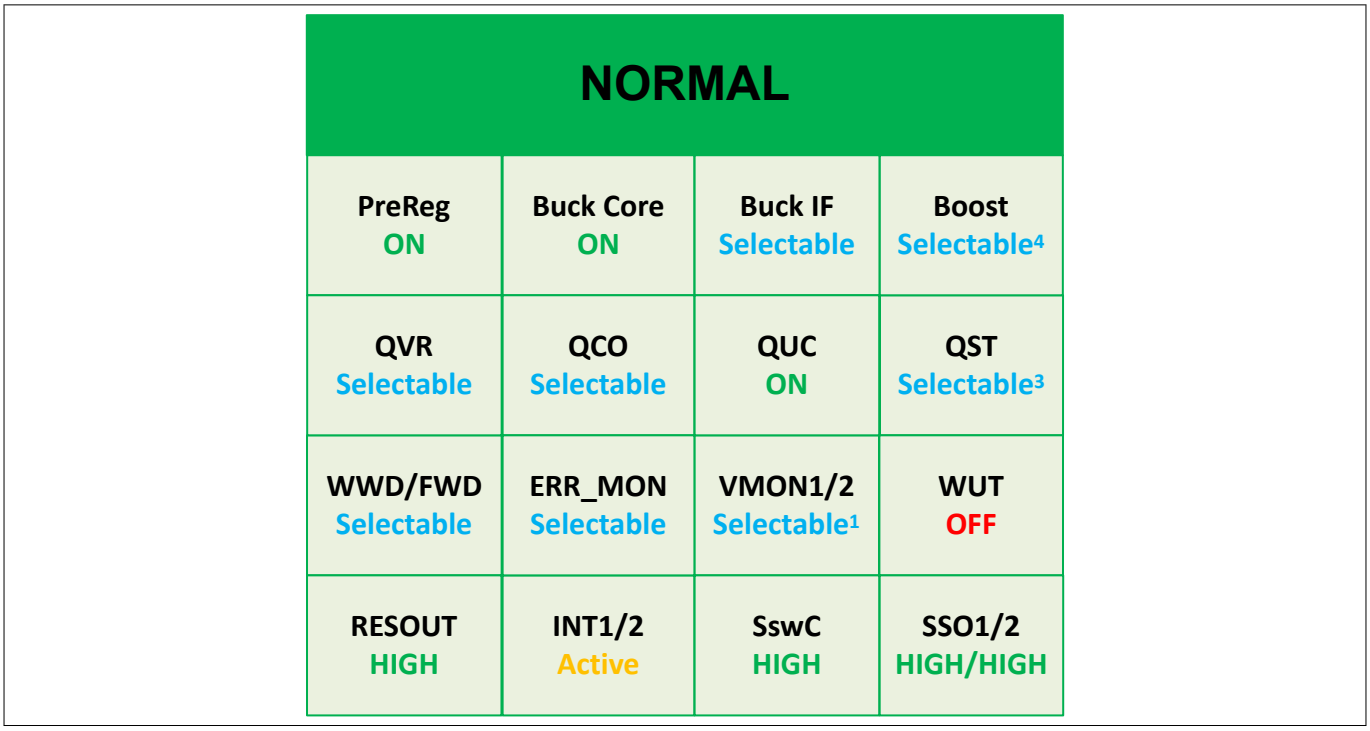


Figure 21 NORMAL state

Table 27 NORMAL state

Part/Function	Value	Description
PreReg	ON	Pre-regulator is on
Buck Core	ON	Core supply is on
Buck IF	Selectable	Buck regulator for interface supply can be switched on or off, if it has been detected via automated use detection during start-up
Boost	Selectable	Boost regulator is selectable with start-up autodetect only if V_{R1FB} = 5V5 nominal. Otherwise it is on
QVR	Selectable	Voltage reference can be selected by SPI to be on or off
QCO	Selectable	Communication supply can be selected by SPI to be on or off
QUC	ON	Microcontroller supply is on
QST	Selectable	Standby supply is selectable when QST_MODE is configured as USER_MODE otherwise, it is on when QST_MODE is configured as PMIC_MODE (default)
WWD/FWD	Selectable	Watchdog can be selected by SPI to be on or off
ERR_MON	Selectable	Error monitoring function ERR MON can be selected by SPI to be on or off
VMON1/2	Selectable	External voltage monitoring VMON1/2 is on, if automated use-detection identified the usage; can be switched off by SPI
WUT	OFF	Wake-up timer (WUT) is off
RESOUT	High	RESOUT output is high
INT1/2	Active	Interrupt outputs are active (INT2 only active if "REDUCED OPERATION" is enabled)
SswC	High	External safety switch is on
SSO1/2	High/High	Safe state outputs are high

9.1.1.4 WAKE state

When the device enters WAKE from SLEEP, the modules are restored to the states as they were before the move to SLEEP. If in SLEEP RESOUT was low, in WAKE state the device waits for successful initialization by the microcontroller before the INIT timer tINIT expires.

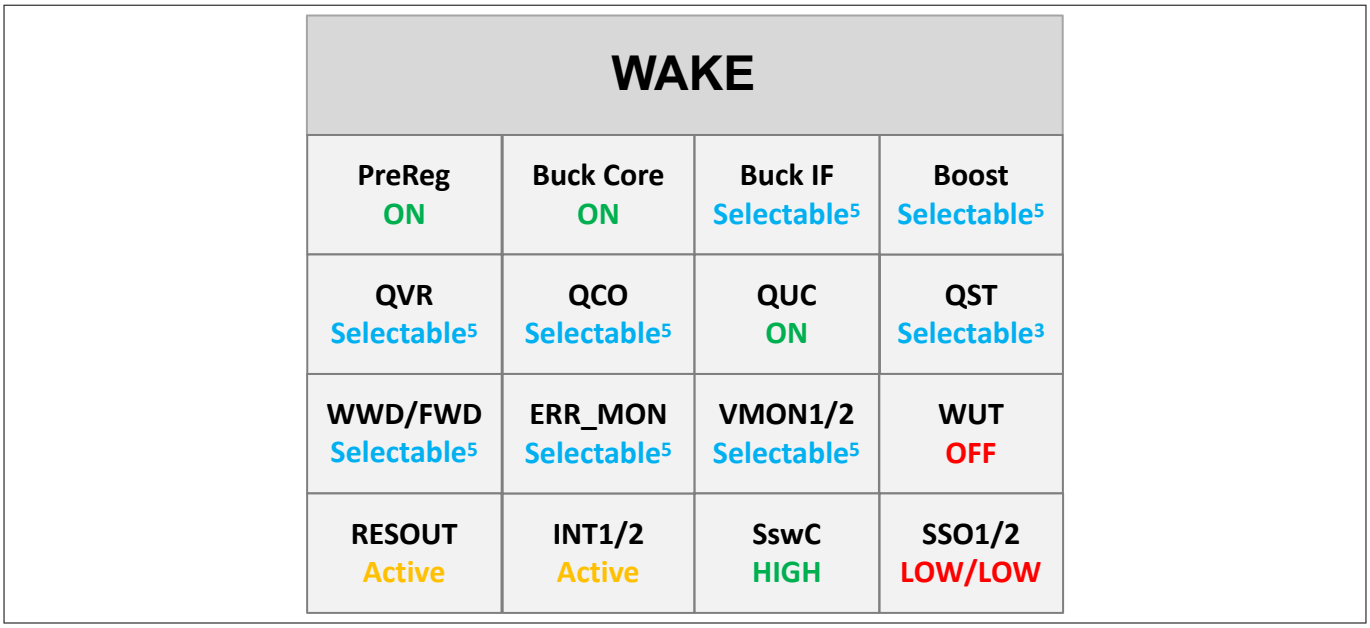


Figure 22 WAKE state

Table 28 WAKE state

Part/Function	Value	Description
PreReg	ON	Pre-regulator is on
Buck Core	ON	Core supply is on
Buck IF	Selectable	Buck regulator for interface supply is configurable, if it has been detected via automated use detection during start-up
Boost	Selectable	Boost regulator is configurable with start-up autodetect only if VR1FB =5V5 nominal otherwise, it is on
QVR	Selectable	Voltage reference is configurable via SPI
QCO	Selectable	Communication supply is configurable via SPI
QUC	ON	Microcontroller supply is on
QST	Selectable	Standby supply is selectable when QST_MODE is configured as USER_MODE otherwise, it is on when QST_MODE is configured as PMIC_MODE (default)
WWD/FWD	Selectable	Watchdog is configurable via SPI
ERR_MON	Selectable	Error monitoring function ERR MON is configurable via SPI
VMON1/2	Selectable	External voltage monitoring VMON1/2 is on, if automated use-detection identified the usage; can be switched off by SPI
WUT	OFF	Wake-up timer (WUT) is off
RESOUT	Active	RESOUT output is active
INT1/2	Active	Interrupt outputs are active
SswC	HIGH	External safety switch is on
SSO1/2	LOW	Safe state outputs are low

9.1.1.5 REDUCED OPERATION state

The device provides a REDUCED OPERATION state to allow severe safety reactions only on sub-parts of the application, when the device is either in NORMAL state or REDUCED OPERATION state itself. In addition, a successful initialization by the microcontroller must be done before the INIT timer t_{INIT} expires. If REDUCED OPERATION is enabled (**REDOP_RS_CFG1.EN = 1**) the device shows a differentiated reaction to specific events. In particular an additional Application Reset function is introduced. This Application Reset differs in its configurable pulse width compared to a normal reset and it is issued at the outputs INT1/2 accordingly (**REDOP_RS_CFG2.REDOP_RESOUT_APP1_DUR**, **REDOP_RS_CFG2.REDOP_RESOUT_APP2_DUR**). By enabling this state ERR2 and WD2 are automatically enabled, too. Events that are detected at ERR1 or WD1 are reported with an Application Reset at INT1 and events that are detected at ERR2 and WD2 are reported with an Application Reset at INT2. In addition a normal interrupt is issued at INT1 if ERR2 or WD2 report an error and vice versa at INT2 if ERR1 or WD1 report an error. This cross application notification however can be disabled by using the configuration in **REDOP_RS_CFG1.INT1_DIS** and **REDOP_RS_CFG1.INT2_DIS**. For further information on initialization in REDUCED OPERATION, failure reaction, interrupt generation and Application Reset the following chapter provide more details:

- INIT timer function
- Reaction on faults
- Interrupt function (INT)
- Application Reset (REDUCED OPERATION ENABLE)

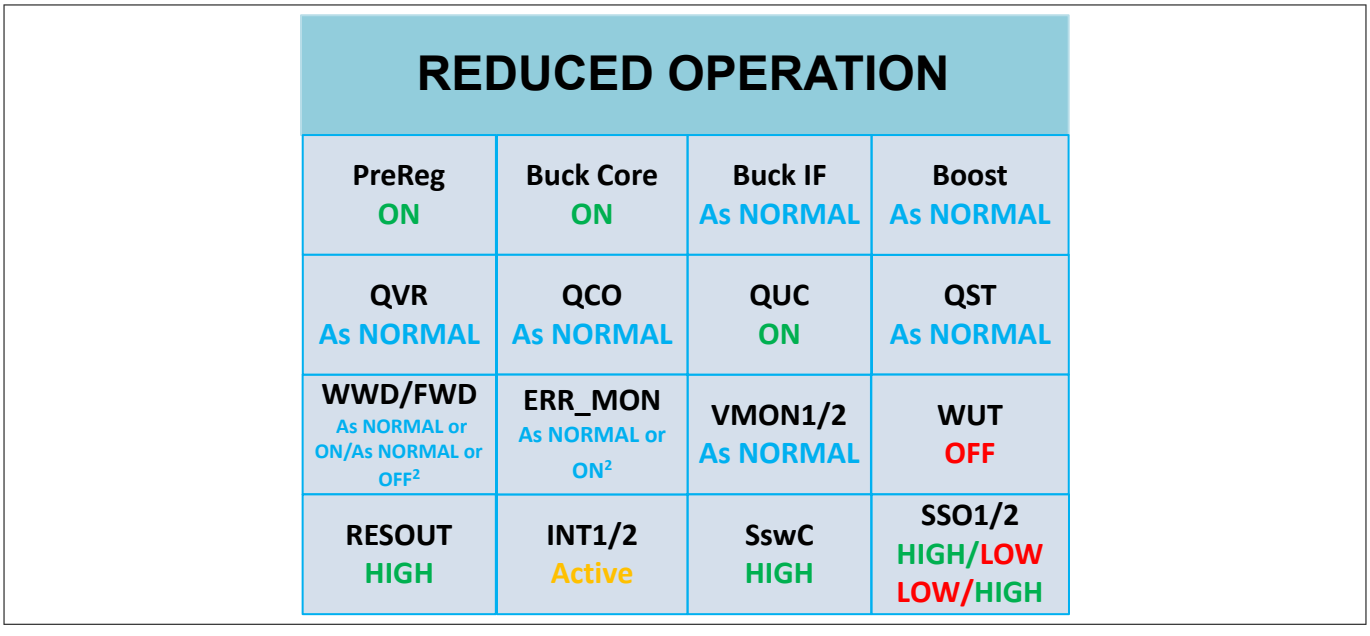


Figure 23 REDUCED OPERATION state

Table 29 REDUCED OPERATION state

Part/Function	Value	Description
PreReg	ON	Pre-regulator is on
Buck Core	ON	Core supply is on
Buck IF	As NORMAL	Buck regulator for interface supply has same configuration as in NORMAL state
Boost	As NORMAL	Boost regulator has the same configuration as in NORMAL
QVR	As NORMAL	Voltage reference has same configuration as in NORMAL state
QCO	As NORMAL	Communication supply has same configuration as in NORMAL state

(table continues...)

Table 29 (continued) REDUCED OPERATION state

Part/Function	Value	Description
QUC	ON	Microcontroller supply is on
QST	As NORMAL	Standby supply has same configuration as in NORMAL state
WWD	Failing application: ON Configuration registers reset Non failing application: As NORMAL	Failing application: Configuration registers reset and remains ON. Waits for trigger and/or configuration via SPI. Non failing application: Keeps configuration as for NORMAL state and needs to be serviced as in NORMAL state.
FWD	Failing application: OFF Configuration registers reset Non failing application: As NORMAL	Failing application: Configuration registers reset and OFF. Non failing application: Keeps configuration and stays ON as in NORMAL. Trigger must be done accordingly.
ERR_MON	Failing application: ON Configuration registers reset Non failing application: As NORMAL	Failing application: Configuration registers reset and remains ON. Waits for correct ERR pin signal and/or configuration via SPI. Non failing application: Keeps configuration as for NORMAL state and needs to be serviced as in NORMAL state.
VMON1/2	As NORMAL	External voltage monitoring VMON1/2 have same configuration as in NORMAL state
WUT	OFF	Wake-up timer (WUT) is off
RESOUT	High	RESOUT output is high
INT1/2	Active	Interrupt outputs are active
SswC	High	External safety switch is on
SSO1/2	High/Low or Low/High	Safe state outputs are low or high depending on the failing cluster/ application

***Note**: While being in REDUCED OPERATION state it must be ensured by the integrator, that except for triggering the watchdog and reconfiguring the application specific monitoring ERR1/2 or WD1/2, no other configuration of the device is being made, like disabling or enabling voltage rails. This could interfere with the internal monitoring of the device and cause incorrect error reporting while being in REDUCED OPERATION. In addition it must be mentioned, that upon the release of the related INTx, the corresponding WWDx and ERRx function is re-enabled, whereas the FWD is disabled.*

9.1.1.6 FAILSAFE state

In FAILSAFE sate all generated voltage rails are being switched off.

The failsafe timer is started when entering the FAILSAFE state.

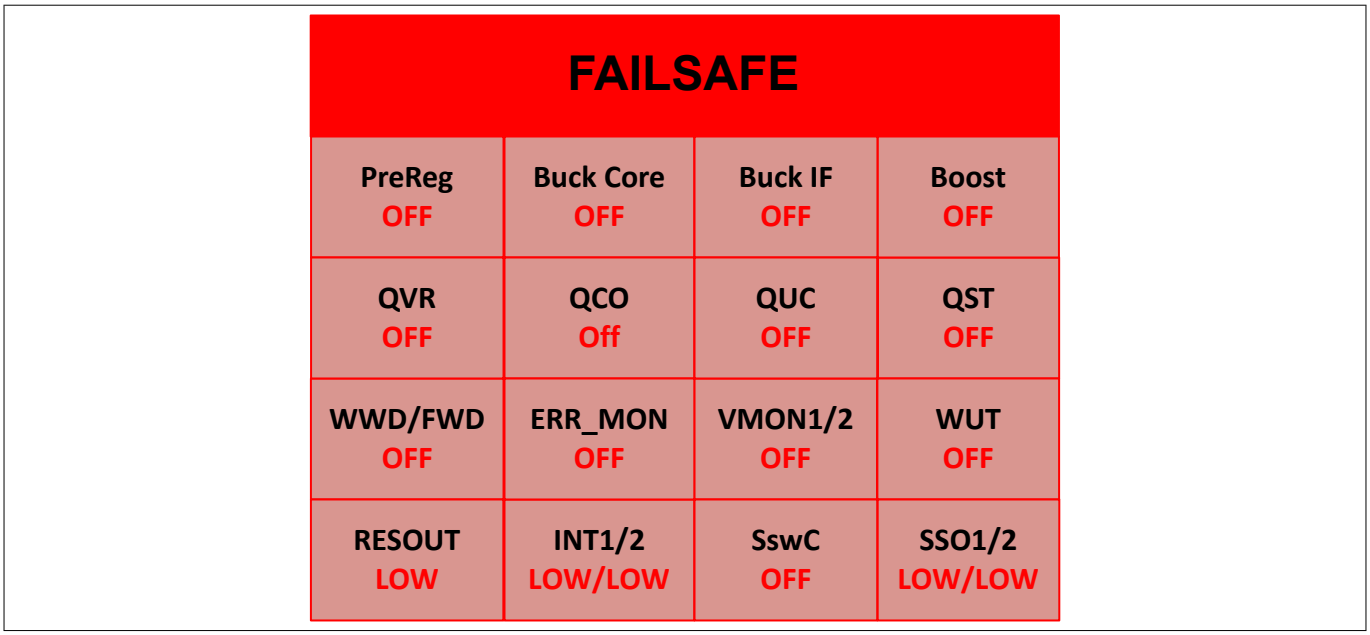


Figure 24 FAILSAFE state

Table 30 FAILSAFE state

Part/Function	Value	Description
PreReg	OFF	Pre-regulator is off
Buck Core	OFF	Core supply is off
Buck IF	OFF	Buck regulator for interface supply is off
Boost	OFF	Boost regulator is off
QVR	OFF	Voltage reference is off
QCO	OFF	Communication supply is off
QUC	OFF	Microcontroller supply is off
QST	OFF	Standby supply is off
WWD/FWD	OFF	Watchdog is off
ERR_MON	OFF	Error monitoring function ERR MON block is off
VMON1/2	OFF	External voltage monitoring VMON1/2 are off
WUT	OFF	Wake-up timer (WUT) is off
RESOUT	LOW	RESOUT output is low
INT1/2	LOW	Interrupt outputs are low
SswC	LOW	External safety switch is off
SSO1/2	LOW	Safe state outputs are low

9.1.1.7 SLEEP state

For minimized operation constraints in the application the device can be moved into a SLEEP state which provides a configuration to only operate selected modules of the device. This enables a state for reduced function sets while consuming less energy in the application compared to the NORMAL state.

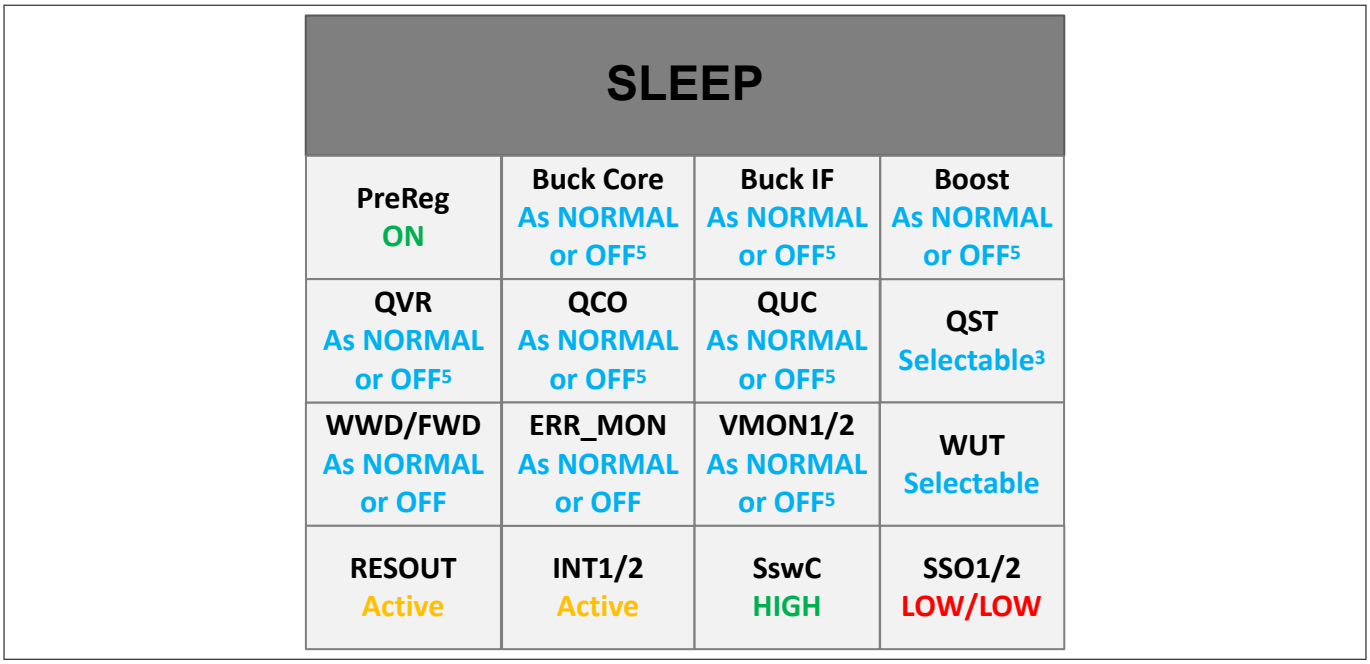


Figure 25 SLEEP state

Table 31 SLEEP state

Part/Function	Value	Description
PreReg	ON	Pre-regulator is on
Buck Core	As NORMAL or OFF	Buck core regulator has same configuration as in NORMAL state or is off if configured
Buck IF	As NORMAL or OFF	Buck regulator for interface supply has same configuration as in NORMAL state or is off if configured
Boost	As NORMAL or OFF	Boost regulator has same configuration as in NORMAL state or is off if configured
QVR	As NORMAL or OFF	Voltage reference has same configuration as in NORMAL state or is off if configured
QCO	As NORMAL or OFF	Communication supply has same configuration as in NORMAL state or is off if configured
QUC	As NORMAL or OFF	Microcontroller supply has same configuration as in NORMAL state or is off if configured
QST	Selectable	Standby supply is selectable when QST_MODE is configured as USER_MODE otherwise, it is on when QST_MODE is configured as PMIC_MODE (default)
WWD/FWD	As NORMAL or OFF	Watchdog has same configuration as in NORMAL state or is off if configured
ERR_MON	As NORMAL or OFF	Error monitoring function ERR MON has same configuration as in NORMAL state or is off if configured
VMON1/2	As NORMAL or OFF	External voltage monitoring VMON1/2 have same configuration as in NORMAL state or they are off if configured

(table continues...)

Table 31 (continued) SLEEP state

Part/Function	Value	Description
WUT	Selectable	Wake-up timer (WUT) is selectable to be on or off
RESOUT	Active	RESOUT output is active (LOW if either BUCKCORE or QUC are OFF)
INT1/2	Active	Interrupt outputs are active (LOW if QUC is OFF)
SswC	HIGH	External safety switch is on
SSO1/2	LOW	SSO1 and SSO2 are low

***Note**: While being in SLEEP state it must be ensured by the integrator, that except for servicing the watchdog no other configuration of the device is being made, like disabling or enabling voltage rails or changing the configuration of WD1/2 or ERR1/2. This could interfere with the internal monitoring of the device and cause incorrect error reporting while being in SLEEP.*

9.1.1.8 STANDBY state

The STANDBY state represents the low current mode of the device.

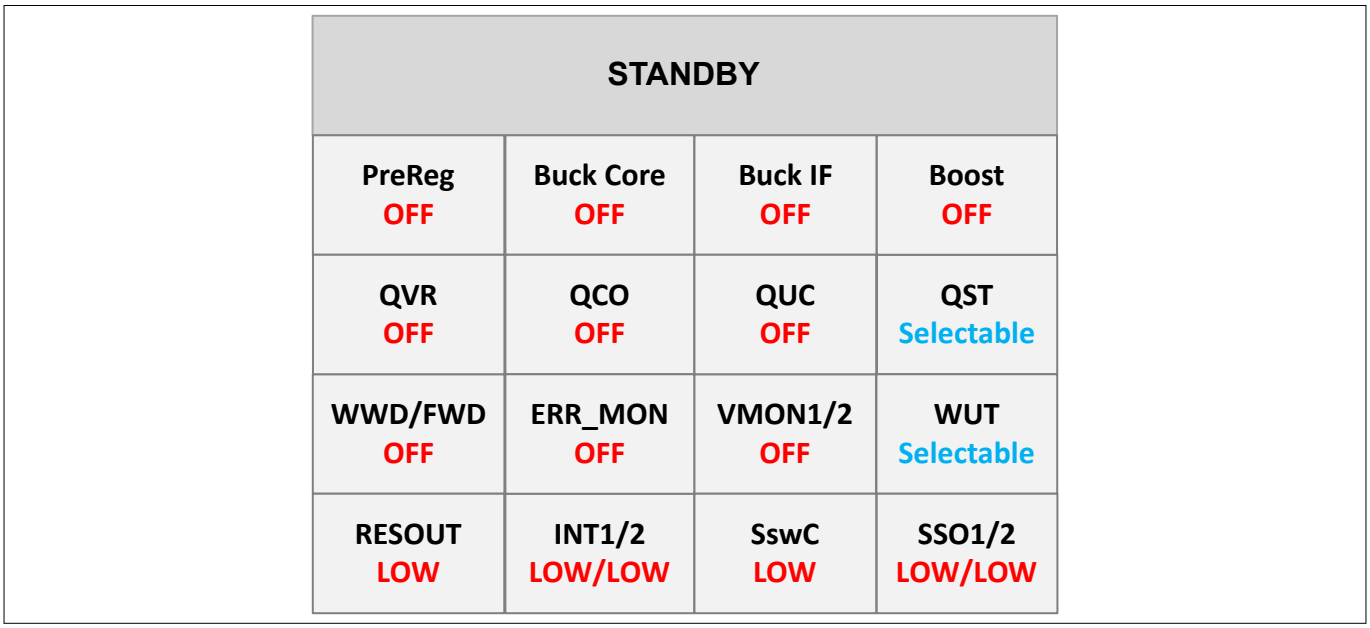


Figure 26 STANDBY state

Table 32 STANDBY state

Part/Function	Value	Description
PreReg	OFF	Pre-regulator is off
Buck Core	OFF	Core supply is off
Buck IF	OFF	Buck regulator for interface supply is off
Boost	OFF	Boost regulator is off
QVR	OFF	Voltage reference is off
QCO	OFF	Communication supply is off

(table continues...)

Table 32 (continued) STANDBY state

Part/Function	Value	Description
QUC	OFF	Microcontroller supply is off
QST	Selectable	Standby supply is on or off, can be configurable by SPI
WWD/FWD	OFF	Watchdog interface is off
ERR_MON	OFF	Error monitoring block is off
VMON1/2	OFF	Monitoring blocks are off
WUT	Selectable	Wake block is selected to be on or off
RESOUT	LOW	Control reset output is low
INT1/2	LOW	Interrupt outputs are low
SswC	LOW	External safety switch is off
SSO1/2	LOW	Safe state outputs are low

***Note**: Lowest quiescent current can only be reached if WUT and QST are both OFF. This allows the device to switch off all internal voltage rails that are not required.*

9.1.2 INIT timer function

The INIT timer provides an extended time window for the microcontroller to properly start-up and synchronize itself with the PMIC. Upon release of the reset output elementary supervision functions have be established or disabled before t_{INIT} expires. The following paragraphs refine the general operation of the INIT timer.

Start INIT timer

- The INIT timer starts on the rising edge of the application reset pulse of the corresponding INT1/2 pin if the device is in REDUCED OPERATION state.
- The INIT timer starts on the rising edge of RESOUT pin if the device is in INIT or in WAKE state.

STOP INIT timer

The device stops the INIT timer and resets its expiration counter if all of the following conditions are fulfilled:

- WD1/2 is properly triggered or is disabled via SPI, see Watchdog functions.
- ERRMON0/1/2 signal is applied correctly or is disabled via SPI, see Error monitoring

INIT TIMER FAULT

The device detects an INIT_TIMER_FAULT if the INIT timer is not successfully stopped before it expires.

***Note**: WD2 and ERR2 only need to be initialized if REDUCED OPERATION is enabled (**REDOP_RS_CFG1.EN = 1**).*

If the INIT timer elapses **once** in INIT state, the device:

- generates an INIT_TIMER_FAULT,
- activates a soft reset
- stores the fault
- resets registers belonging to the reset class R3
- moves to INIT state, see state machine

If the INIT timer elapses **twice** in INIT state, the device

- generates an INIT_TIMER_FAULT
- activates a hard reset
- stores the fault

- resets registers belonging to the reset class R3
- performs configured power-down sequence
- restarts configured power sequence
- moves to INIT state, see state machine

If the INIT timer elapses **a third time** in INIT state, the device

- stores the fault
- resets registers belonging to the reset class R2
- moves to FAILSAFE state, see state machine

If the INIT timer elapses **once** in REDUCED OPERATION state, the device:

- generates an INIT_TIMER_FAULT
- activates a new application reset corresponding to the application that has failed
- sets the bit **INIT_ERR_APPx.REDOP_RES1**

If the INIT timer elapses **twice** in REDUCED OPERATION state, the device

- generates an INIT_TIMER_FAULT,
- activates a soft reset
- sets the error bit **INIT_ERR_APPx.REDOP_RES2**
- moves to INIT state, see state machine

If the INIT timer elapses **once** in WAKE state, the device

- generates an INIT_TIMER_FAULT,
- activates a soft reset
- stores the fault
- resets registers belonging to the reset class R3
- moves to INIT state, see state machine

Note: *The first expiration in WAKE already counts as first as if it had happened in INIT.*

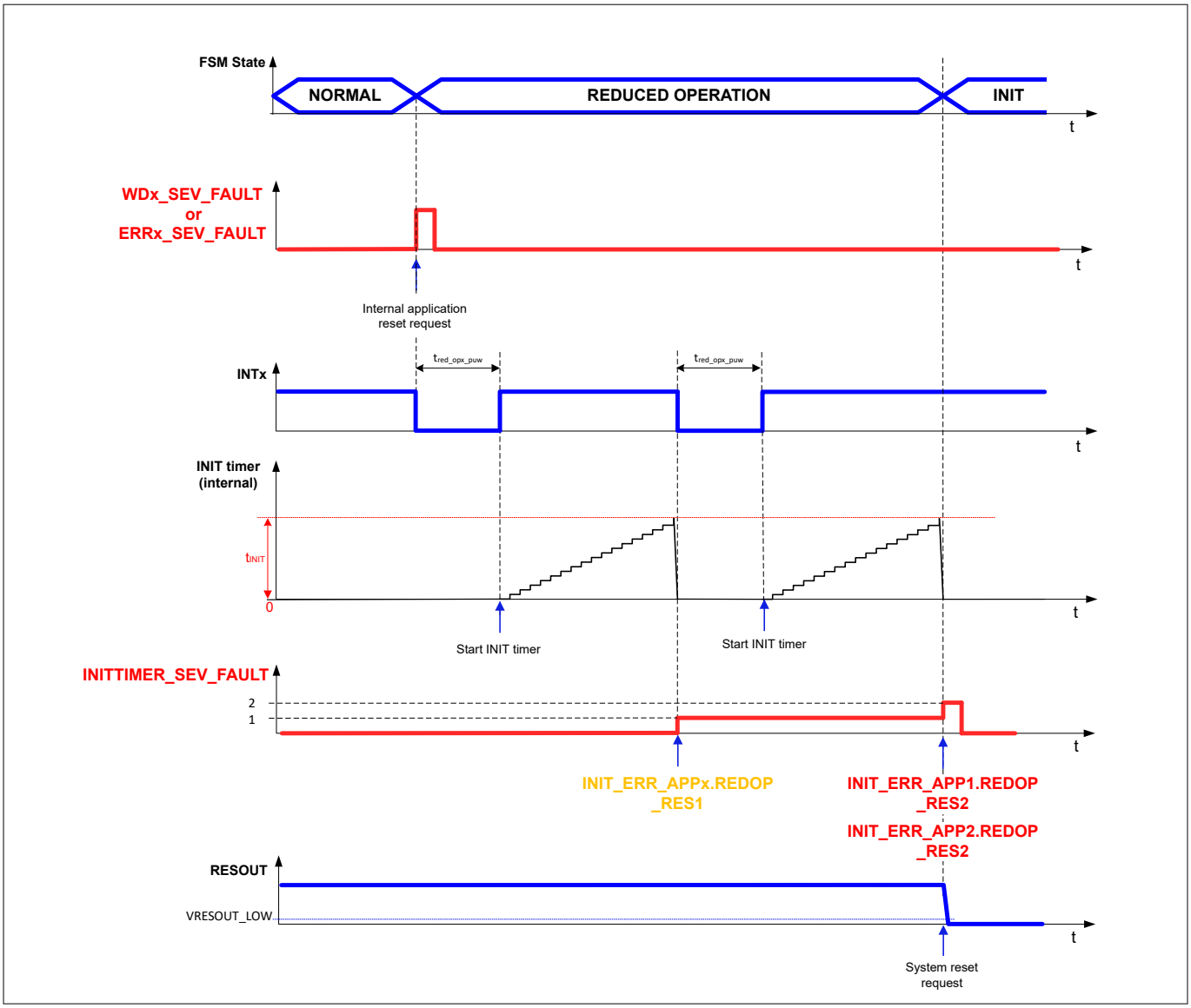


Figure 27 Signal diagram system reset activation in REDUCED OPERATION state

x = 1, 2

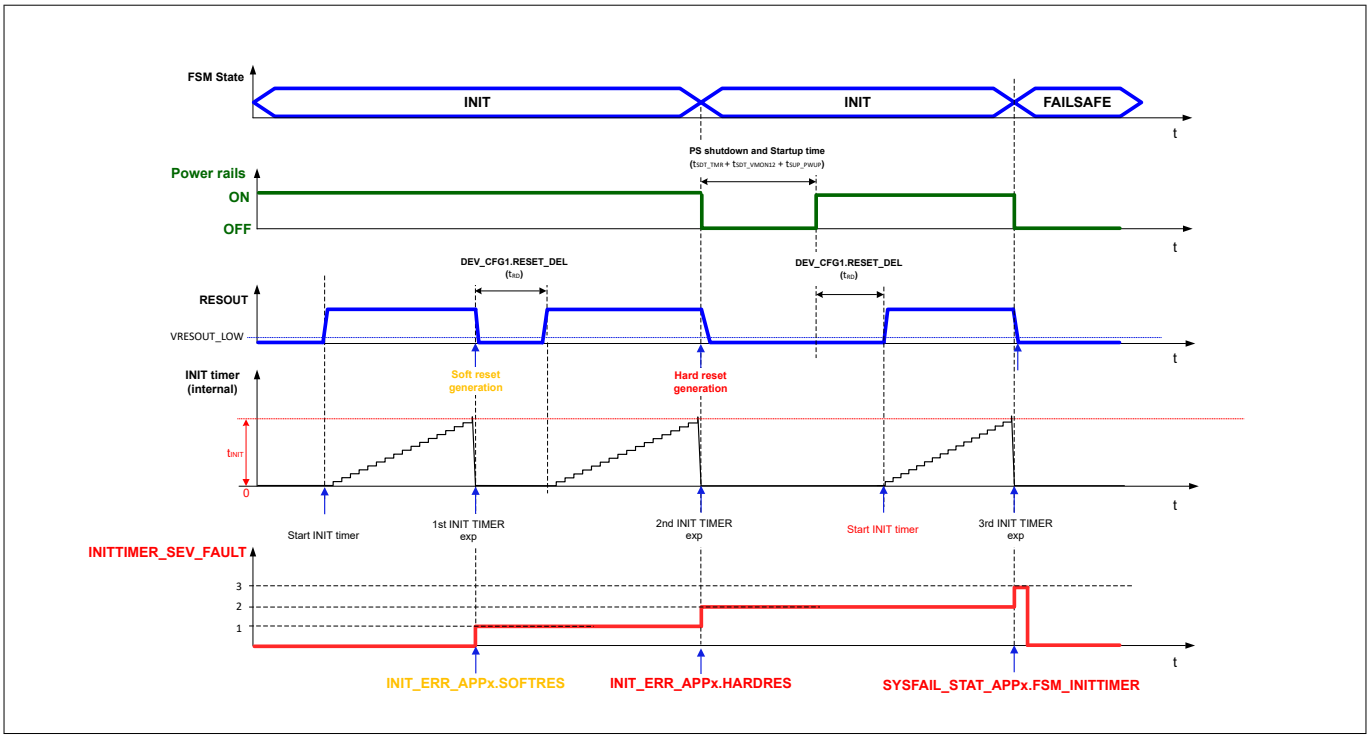


Figure 28 Signal diagram system shutdown due to 3xINIT timer elapse in INIT state

x = 1, 2

9.1.3 State transition

A state transition is requested by writing the bitfield **DEV_PW_CFG3.FSM_STATEREQ**. Made changes will take effect upon successful completion of the SPI communication and locking the protected write registers again. This happens upon release of CSN after **PROT_CFG.KEY** has been written with the lock key. If a state transition originated in NORMAL is requested, the release of CSN after writing the lock key also marks the moment when the outputs SSOx will be pulled low. Possible configured delay times between SSO1 and SSO2 will still be respected.

If a state request is received while the device executes a power-up or power-down sequence, the state transition is rejected and the bit **SYS_STAT_APP1.FSM_NOOP** is set while at the same time an interrupt is issued (if REDUCED OPERATION is enabled, also **SYS_STAT_APP2.FSM_NOOP** is set). The same reaction also takes place if a state transition is requested which is not listed in the state transition table (invalid state transition request). If a valid state transition is requested while already being in a transition delay into SLEEP or STANDBY, the current delay will be aborted and a transition takes place as if ENA or WAK signal would have been detected instead. Transitions from one state into itself are allowed.

In case a WAK, ENA takes places after the delay time has expired, the already started power-down sequence will be finished and a wake-up takes place directly afterwards.

(x = 1,2)

9.1.3.1 State transition table

Old State	New state	Conditions	Comments
POWERDOWN	INIT	Internal POR (internal supplies OK)	The configured power sequencing is applied, see Hardware configuration (HWCFG)

INIT	NORMAL	(SPI command: Move to NORMAL) AND (Disable or successful service within t_{INIT}: - WWD1/2 - FWD1/2 - ERR0/1/2 pin monitoring)	–
NORMAL	SLEEP	(SPI command: Move to SLEEP) AND (No ENA) AND (No WAK)	- If a move to SLEEP is unsuccessful an interrupt is issued and the device moves into WAKE - The configured power sequencing is applied, see Hardware configuration (HWCFG)
NORMAL	STANDBY	(SPI command: Move to STANDBY) AND (No ENA) AND (No WAK)	- If a move to STANDBY is unsuccessful an interrupt is issued and the device moves into INIT - The configured power sequencing is applied, see Hardware configuration (HWCFG)
SLEEP	WAKE	ENA OR WAK OR WUT timer expired OR (SPI command: Move to WAKE)	- Upon wake-up from SLEEP an interrupt is issued, if QUC was on in SLEEP - The wake-up information is stored - Restores regulator configuration as it has been before entering SLEEP, following the power-up sequence and skipping the respective regulators, see Hardware configuration (HWCFG)
WAKE	NORMAL	(SPI command: Move to NORMAL) AND (Disable or successful service within t_{INIT}: - WWD1/2 - FWD1/2 - ERR0/1/2 pin monitoring)	–

WAKE	SLEEP	(SPI command: Move to SLEEP) AND (No ENA) AND (No WAK)	- If a move to SLEEP is unsuccessful an interrupt is issued and the device moves into WAKE - The configured power sequencing is applied, see Hardware configuration (HWCFG)
WAKE	STANDBY	(SPI command: Move to STANDBY) AND (No ENA) AND (No WAK)	- If a move to STANDBY is unsuccessful an interrupt is issued and the device moves into INIT - The configured power sequencing is applied, see Hardware configuration (HWCFG)
STANDBY	INIT	ENA OR WAK OR WUT timer expired	The configured power sequencing is applied
FAILSAFE	INIT	ENA OR WAK OR Failsafe Timer expired	- The automated wake-up from FAILSAFE upon expiration of the failsafe timer only works if FAILSAFE has not been entered three times consecutively caused by the same failure - The configured power sequencing is applied
REDUCED OPERATION	NORMAL	(SPI command: Move to NORMAL) AND (Disable or successful service within t_{INIT}: - WWD1/2 - FWD1/2 - ERR0/1/2 pin monitoring)	–

***Note**: When requesting a state transition into SLEEP or STANDBY, all configurations of the destination state must be done before sending the state transition request.*

9.1.3.2 Programmable transition delay time

For the transitions from NORMAL to SLEEP, from NORMAL to STANDBY, from WAKE to SLEEP and from WAKE to STANDBY a configurable transition delay time exists. Once one of the mentioned state transitions have been requested by the microcontroller, the transition takes place after the expiration of the transition delay time

t_{TR_DEL}.The transition is unsuccessful and moves to INIT or WAKE respectively, if a state request is received within the transition delay time.

The configuration is done in **DEV_CFG4.FSM_TRDEL**.

9.1.3.3 Automated wake-up from FAILSAFE

Upon entering FAILSAFE the device remains in it for $t_{FAILSAFE\_min}$*. Afterwards it runs an automated restart attempt unless FAILSAFE was entered 3 times consecutively caused by the same error source, in which case the device remains in FAILSAFE and waits for ENA or WAK to run another restart attempt. In case it is unsuccessful, the device follows the same sequence as above.

*) If an overtemperature event was the cause for entering FAILSAFE the device remains in it for t_{TSD_min}.

9.1.4 Power sequencing

BUCK PREREG and QST are the first regulators to ramp up when the internal power on reset (POR) was released. However QST output voltage level has no impact on the power sequencing and is not gating for other rails to start up. Also the UV events for a regulator is masked until the output has exceeded its undervoltage threshold.

If a regulator does not succeed to establish a voltage above its undervoltage threshold before t_{StG} expires, one of the following scenarios apply:

1. Move to FAILSAFE:
   - BUCK PREREG
   - BOOST (if usage detected)
   - QUC
   - BUCK CORE
   - QST
2. Skipps the start-up of the respective regulator and disables it. Issues an interrupt according to the reaction on detected faults for short to GND detection in Reaction on faults (non-blocking for power sequence)
   - BUCK IF (if usage detected)
   - VMON1 (if usage detected)
   - QVR
   - QCO
   - VMON2 (if usage detected)

The initial reset release (RESOUT going "high") after a power-up sequence has taken place, occurs when QUC, QST and BUCKCORE have surpassed their undervoltage thresholds. Further details for the reset function see Reset function (RESOUT)

.

PREREG starts switching after the input voltage at the pins VS and VIQST is above $V_{PWD\_TH\_H}$ and the time t_{SUP_PWUP} has passed.

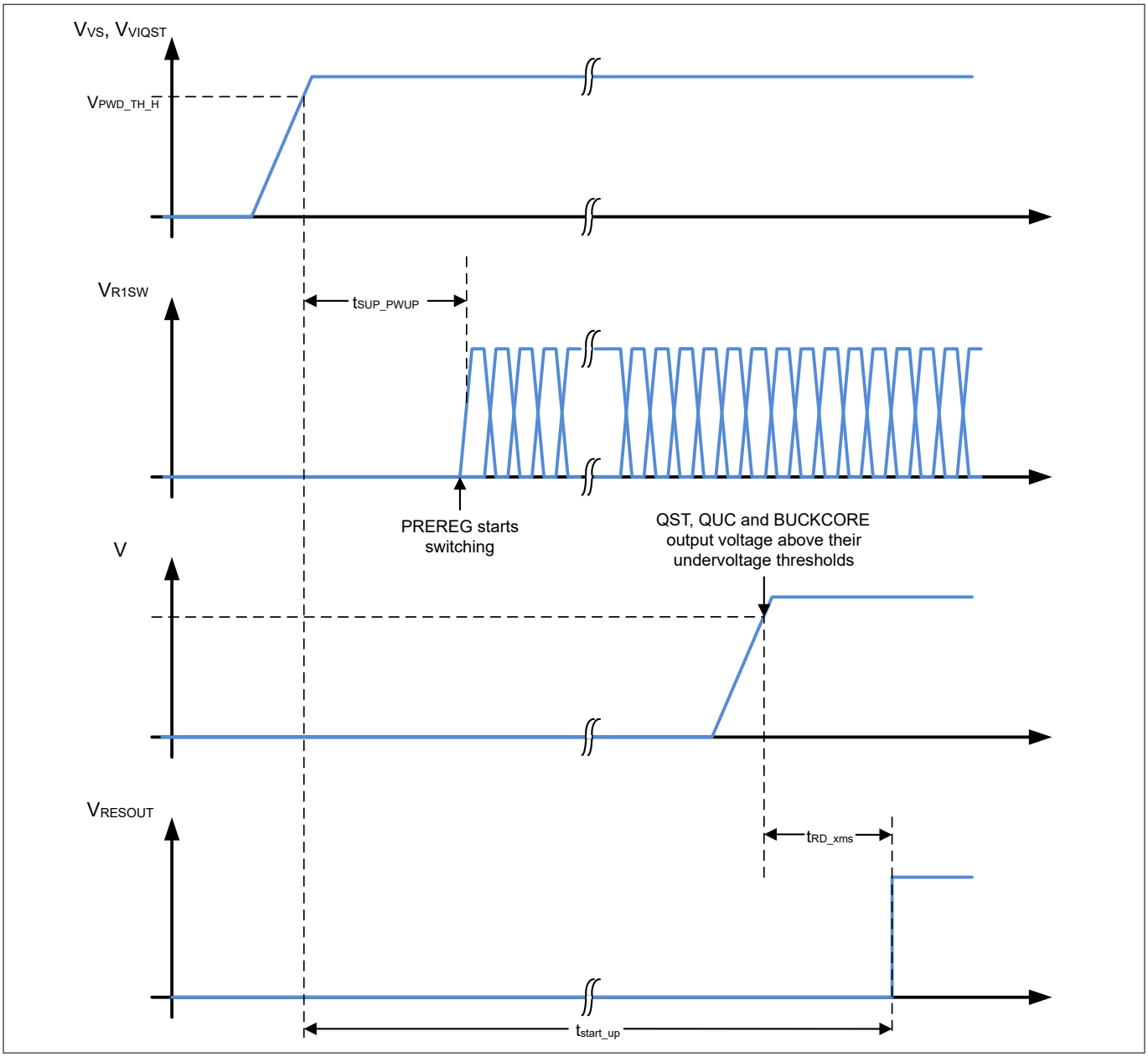


Figure 29 System start-up timings

If a state transition request is placed while the device performs a power-down or power-up sequence the following points apply:

- The command is ignored
- An interrupt is triggered
- The fault is stored in a dedicated register

The device provides status information for static configurations (active regulators) via register status flags in DEV_STAT.

9.1.4.1 Power up sequence schema A

The hardware configuration (HWCFG) determines the start up sequence to be either schema A or schema B.

If the power up sequence schema A is selected, the sequence as described below is executed. Thereby the next voltage rail is only ramped up if the previous output voltage rail has exceeded its undervoltage threshold. QST starts up independently from the other voltage regulators and is not a precondition for another regulator.

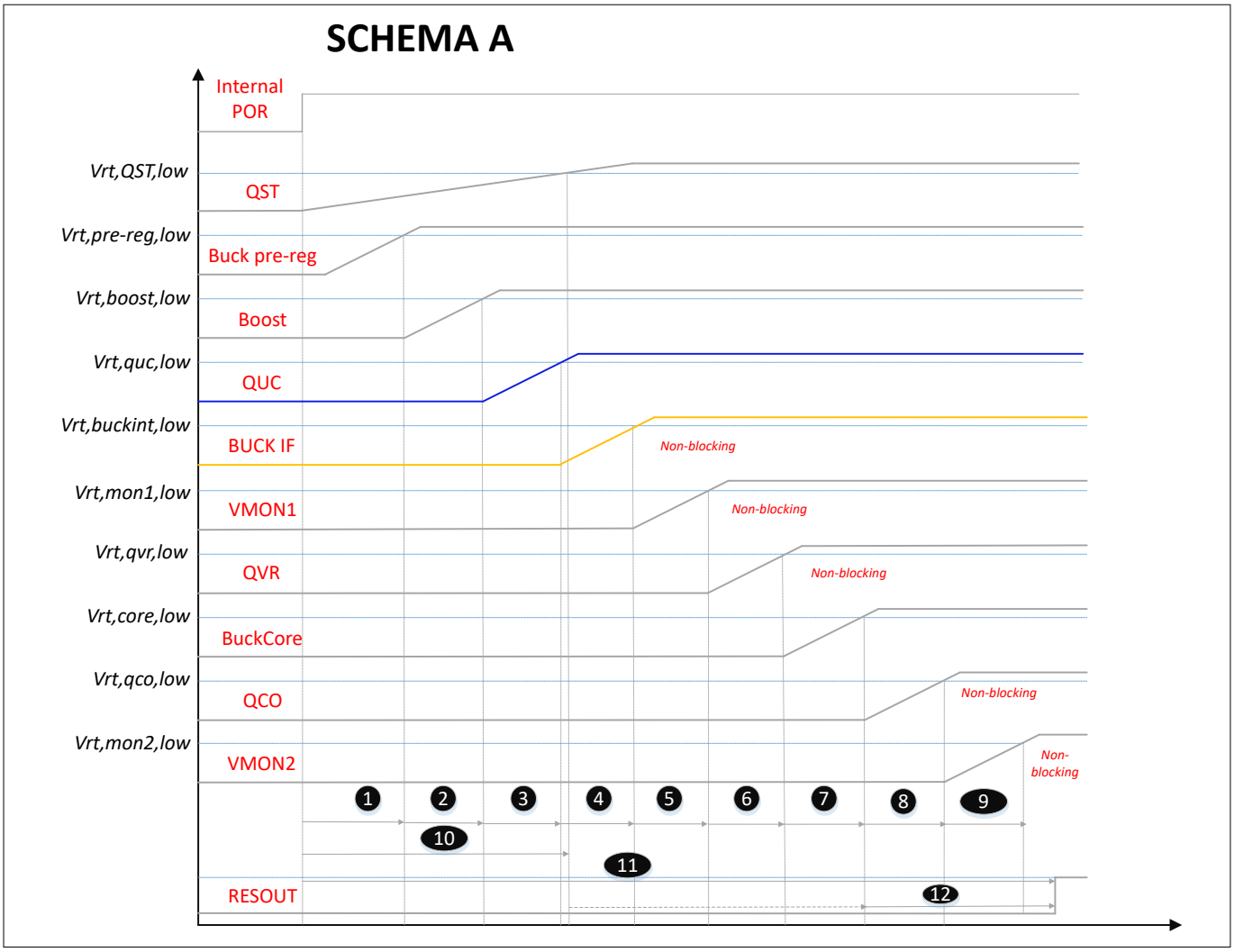


Figure 30 Power-up sequencing schema A

1 -> PREREG starts up
2 -> BOOST starts up (only if autodetected)
3 -> QUC starts up
4 -> BUCKIF starts up (only if autodetected during first power up sequence)
5 -> VMON1 starts up (only if autodetected during first power up sequence)
6 -> QVR starts up
7 -> BUCK CORE starts up
8 -> QCO starts up
9 -> VMON2 starts up(only if autodetected during first power up sequence)
10 -> QST starts up
11 -> Duration of complete start-up: t_{start_up}
12 -> RESOUT delay time (further information in Reset function (RESOUT)

9.1.4.2 Power up sequence schema B

If the power up sequence schema B is selected, the sequence as described below is executed. Thereby the next voltage rail is only ramped up if the previous output voltage rail has exceeded its undervoltage threshold. QST starts up independently from the other voltage regulators and is not a precondition for another regulator.

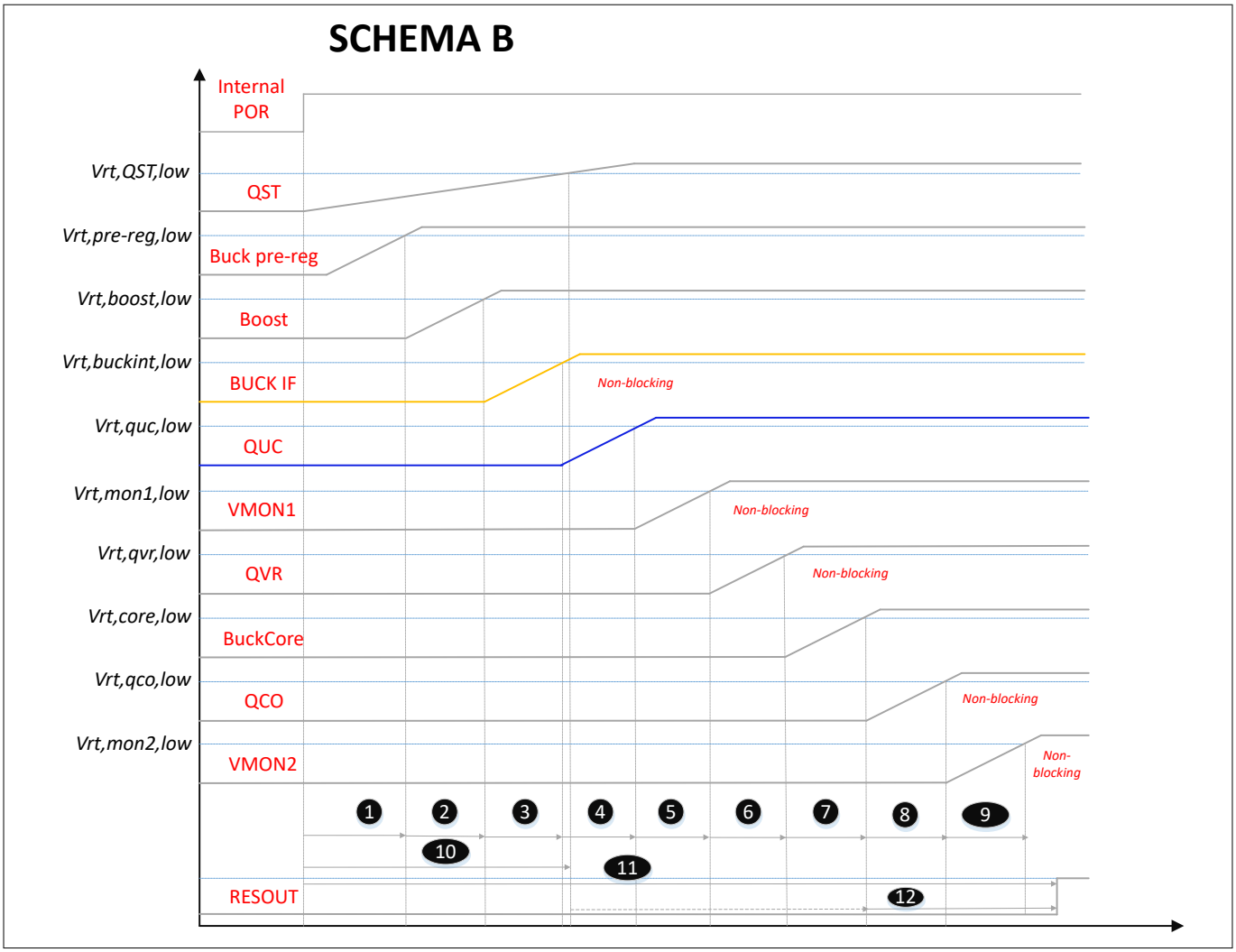


Figure 31 Power sequencing schema B

1 -> PREREG starts up
2 -> BOOST starts up (only if autodetected)
3 -> BUCKIF starts up (only if autodetected during first power up sequence)
4 -> QUC starts up
5 -> VMON1 starts up (only if autodetected during first power up sequence)
6 -> QVR starts up
7 -> BUCK CORE starts up
8 -> QCO starts up
9 -> VMON2 (only if autodetected during first power up sequence)
10 -> QST starts up
11 -> Duration of complete start-up: t_{start_up}
12 -> RESOUT delay time (further information in Reset function (RESOUT)

9.1.4.3 Power down sequencing

The device disables the output voltage rail(s) following the corresponding power down sequences if it transitions into STANDBY or SLEEP. When transitioning into SLEEP the sequence will leave out the rails and the associated delays, that are configured to stay on.

If power up sequence schema A was selected

1. disable VMON2
2. wait for t_{SDT_VMON12}
3. disable QCO
4. wait for t_{SDT_TMR}
5. disable BUCK CORE
6. wait for t_{SDT_TMR}
7. disable QVR
8. wait for t_{SDT_TMR}
9. disable VMON1
10. wait for t_{SDT_VMON12}
11. disable BUCK IF
12. wait for t_{SDT_TMR}
13. disable QUC
14. wait for t_{SDT_TMR}
15. disable BOOST
16. wait for t_{SDT_TMR}
17. disable BUCK PREREG
18. wait for t_{SDT_TMR}

If power up sequence schema B was selected

1. disable VMON2
2. wait for t_{SDT_VMON12}
3. disable QCO
4. wait for t_{SDT_TMR}
5. disable BUCK CORE
6. wait for t_{SDT_TMR}
7. disable QVR
8. wait for t_{SDT_TMR}
9. disable VMON1
10. wait for t_{SDT_VMON12}
11. disable QUC
12. wait for t_{SDT_TMR}
13. disable BUCK IF
14. wait for t_{SDT_TMR}
15. disable BOOST
16. wait for t_{SDT_TMR}
17. disable BUCK PREREG
18. wait for t_{SDT_TMR}

The device disables the output voltage rail(s) following the corresponding power down sequencing.

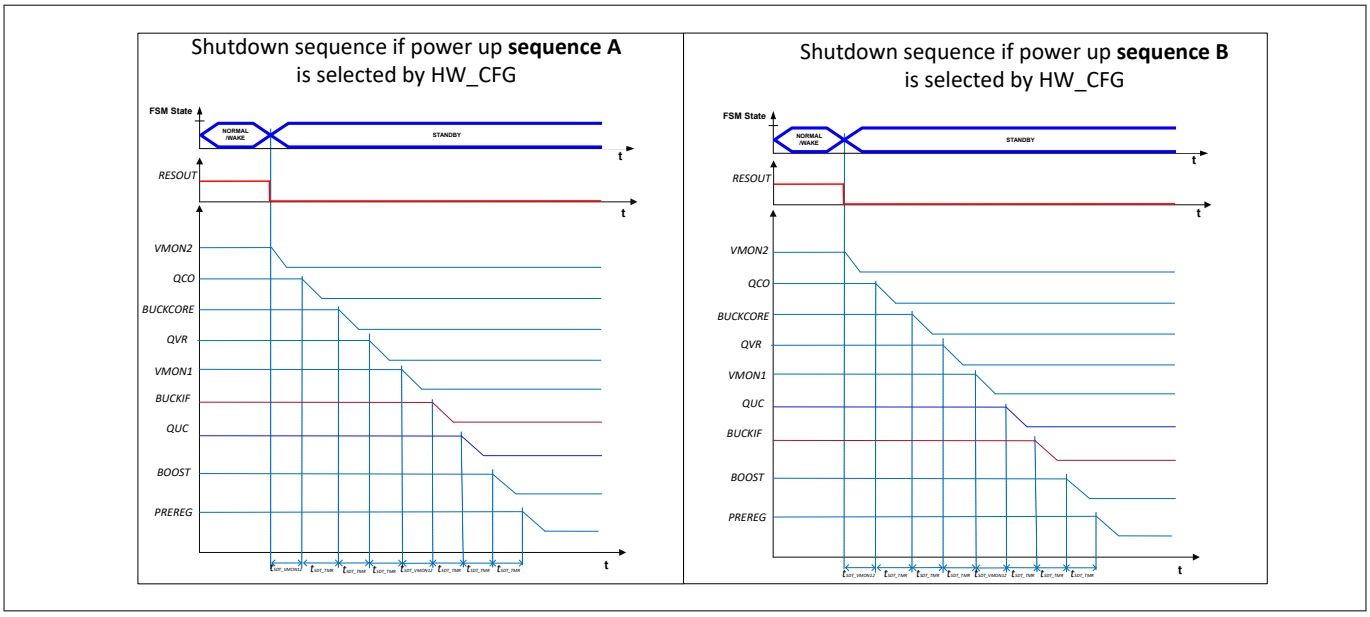


Figure 32 Power down sequencing

***Note**: The parameter t_{SDT_TMR} and t_{SDT_VMON12} represent an internal delay and is not gated by external conditions.*

9.2 Electrical characteristics state machine (FSM)

Table 33 Electrical characteristics state machine (FSM)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supplies start-up time	t_{SUP_PWUP}	–	4	6	ms	• V_{VS} and $V_{VIQST} \geq V_{PWD\_TH\_H}$ (V_S and V_{IQST} pins assumed to be connected together externally) • V_{SSC_S} < 1V at startup • Max. Capacitance at SSC_S pin is 1uF	DS-2083
Power up threshold	$V_{PWD\_TH\_H}$	–	–	6	V	V_{VS} increasing	DS-2156
Power down threshold low	$V_{PWD\_TH\_L}$	2.5	–	5.5	V	V_{VS} decreasing BOOST not used	DS-1555
System shutdown time	t_{SDT}	–	–	15	ms	–	DS-1536
Thermal shutdown time	t_{TSD_min}	0.9	1	1.1	s	–	DS-1548

(table continues...)

Table 33 (continued) Electrical characteristics state machine (FSM)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Internal voltage rails shutdown delay	t_{SDT_TMR}	0.9*t_{SDT_TMR}	t_{SDT_TMR}	1.1*t_{SDT_TMR}	µs	t_{SDT_TMR}: Programmable via SPI in DEV_CFG4.FSM_SDT_TMR	DS-1936
VMON1/2 shutdown time	t_{SDT_VMON12}	0.9*t_{SDT_VMON12}	t_{SDT_VMON12}	1.1*t_{SDT_VMON12}	µs	t_{SDT_VMON12}: Programmable via SPI in DEV_CFG4.FSM_SDT_VMON12	DS-1937
Short to ground detection time for internal regulators except QST	t_{STG}	0.9	1	1.1	ms	–	DS-1538
Short to ground detection time for QST regulator	t_{STG_QST}	1.8	2	2.2	ms	–	DS-1537
FAILSAFE time	$t_{FAILSAFE\_min}$	18	20	22	ms	–	DS-1547
INIT timer	t_{INIT}	540	600	660	ms	–	DS-1549
Low power state transition time	t_{TR_DEL}	100	–	1600	µs	t_{TR_DEL} is programmable between 100 µs and 1.6 ms via SPI The default value is set to 900 µs	DS-1503
Accuracy for low power state transition time	$t_{TR\_DEL\_ACC}$	-20	–	20	%	–	DS-1550
State transition time	t_{TR}	–	–	200	µs	–	DS-1551
State transition time to Initialization state	t_{TR_INIT}	–	–	3	ms	Transition from STANDBY/ FAILSAFE to INIT state: Measured from rising edge of ENA/WAKE to R1SW rising edge; Move to INIT faults: Measured from RESOUT falling edge to QVR enable or R1SW rising edge	DS-1552

(table continues...)

Table 33 (continued) Electrical characteristics state machine (FSM)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Current consumption							
SLEEP state current consumption	I_{q_SLEEP}	–	12.9	20	mA	Current consumptions are measured from V_S(T30) without load current applied to post regulators: • BUCK PREREG, QUC, BUCK IF, QCO and QST are enabled • BUCK CORE and QVR are switched off; • BOOST is not populated; • $V_{R1FB} = V_{R1FB\_5V5}$; • f_{DCDC} = 2.2 MHz; • VMON1 and VMON2 are disabled; • Error pin monitoring and all watchdog channels are disabled; • wakeup timer is disabled; • V_{VS}/V_{VIQST} = 13.5 V; • MOSFET IPG20N06S2L-35A for SSW, MOSFET IPG20N06S4L-26A for PREREG Half-bridge • BUCK CORE Load = 1mA, BUCK IF Load = 200uA • $T_j \leq 85°C$	DS-2128

(table continues...)

Table 33 (continued) Electrical characteristics state machine (FSM)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SLEEP state current consumption	I_{q_SLEEP}	–	7.9	12.3	mA	Current consumptions are measured from V_S(T30) : • BUCK PREREG enabled • BOOST, BUCK CORE, QUC, BUCK IF, QCO and QST and QVR are switched off; • $V_{R1FB} = V_{R1FB\_4V}$; • f_{DCDC} = 2.2 MHz; • VMON1 and VMON2 are disabled; • Error pin monitoring and all watchdog channels are disabled; • wakeup timer is disabled; • V_{VS}/V_{VIQST} = 13.5 V; • MOSFET IPG20N06S2L-35A for SSW, MOSFET IPG20N06S4L-26A for PREREG Half-bridge • BUCK CORE Load = 1mA, BUCK IF Load = 200uA • $T_j \leq 85°C$	DS-2107

(table continues...)

Table 33 (continued) Electrical characteristics state machine (FSM)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SLEEP state current consumption	I_{q_SLEEP}	–	6	9.3	mA	Current consumptions are measured from V_S(T30) : • BUCK PREREG and BOOST are enabled • BUCK CORE, QUC, BUCK IF, QCO and QST and QVR are switched off; • $V_{R1FB} = V_{R1FB\_4V}$; • f_{DCDC} = 2.2 MHz; • VMON1 and VMON2 are disabled; • Error pin monitoring and all watchdog channels are disabled; • wakeup timer is disabled; • V_{VS}/V_{VIQST} = 13.5 V; • MOSFET IPG20N06S2L-35A for SSW, MOSFET IPG20N06S4L-26A for PREREG Half-bridge • BUCK CORE Load = 1mA, BUCK IF Load = 200uA • $T_j \leq 85°C$	DS-2109

(table continues...)

Table 33 (continued) Electrical characteristics state machine (FSM)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SLEEP state current consumption	I_{q_SLEEP}	–	6.9	10.7	mA	Current consumptions are measured from V_S(T30) : • BUCK PREREG, BOOST and QUC are enabled • BUCK CORE, BUCK IF, QCO and QST and QVR are switched off; • $V_{R1FB} = V_{R1FB\_4V}$; • f_{DCDC} = 2.2 MHz; • VMON1 and VMON2 are disabled; • Error pin monitoring and all watchdog channels are disabled; • wakeup timer is disabled; • V_{VS}/V_{VIQST} = 13.5 V; • MOSFET IPG20N06S2L-35A for SSW, MOSFET IPG20N06S4L-26A for PREREG Half-bridge • BUCK CORE Load = 1mA, BUCK IF Load = 200uA • $T_j \leq 85°C$	DS-2111

(table continues...)

Table 33 (continued) Electrical characteristics state machine (FSM)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SLEEP state current consumption	I_{q_SLEEP}	–	10.4	16.2	mA	Current consumptions are measured from V_S(T30) : • BUCK PREREG, BOOST, BUCK IF and QUC are enabled • BUCK CORE, QCO, QST and QVR are switched off; • $V_{R1FB} = V_{R1FB\_4V}$; • f_{DCDC} = 2.2 MHz; • VMON1 and VMON2 are disabled; • Error pin monitoring and all watchdog channels are disabled; • wakeup timer is disabled; • V_{VS}/V_{VIQST} = 13.5 V; • MOSFET IPG20N06S2L-35A for SSW, MOSFET IPG20N06S4L-26A for PREREG Half-bridge • BUCK CORE Load = 1mA, BUCK IF Load = 200uA • $T_j \leq 85°C$	DS-2113

(table continues...)

Table 33 (continued) Electrical characteristics state machine (FSM)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SLEEP state current consumption	I_{q_SLEEP}	–	11.4	17.7	mA	Current consumptions are measured from V_S(T30) : • BUCK PREREG, BOOST, BUCK IF, QVR and QUC are enabled • BUCK CORE, QCO, QST are switched off; • $V_{R1FB} = V_{R1FB\_4V}$; • f_{DCDC} = 2.2 MHz; • VMON1 and VMON2 are disabled; • Error pin monitoring and all watchdog channels are disabled; • wakeup timer is disabled; • V_{VS}/V_{VIQST} = 13.5 V; • MOSFET IPG20N06S2L-35A for SSW, MOSFET IPG20N06S4L-26A for PREREG Half-bridge • BUCK CORE Load = 1mA, BUCK IF Load = 200uA • $T_j \leq 85°C$	DS-2115

(table continues...)

Table 33 (continued) Electrical characteristics state machine (FSM)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SLEEP state current consumption	I_{q_SLEEP}	–	12.9	20	mA	Current consumptions are measured from V_S(T30) : • BUCK PREREG, BOOST, BUCK IF, QVR, BUCK CORE, QCO and QUC are enabled • QST is switched off; • $V_{R1FB} = V_{R1FB\_4V}$; • f_{DCDC} = 2.2 MHz; • VMON1 and VMON2 are disabled; • Error pin monitoring and all watchdog channels are disabled; • wakeup timer is disabled; • V_{VS}/V_{VIQST} = 13.5 V; • MOSFET IPG20N06S2L-35A for SSW, MOSFET IPG20N06S4L-26A for PREREG Half-bridge • BUCK CORE Load = 1mA, BUCK IF Load = 200uA • $T_j \leq 85°C$	DS-2117

(table continues...)

Table 33 (continued) Electrical characteristics state machine (FSM)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SLEEP state current consumption	I_{q_SLEEP}	–	6	9.3	mA	Current consumptions are measured from V_S(T30) : • BUCK PREREG is enabled • BUCK IF, QVR, BUCK CORE, QCO, QUC and QST are switched off; • BOOST is not populated; • $V_{R1FB} = V_{R1FB\_5V5}$; • f_{DCDC} = 2.2 MHz; • VMON1 and VMON2 are disabled; • Error pin monitoring and all watchdog channels are disabled; • wakeup timer is disabled; • V_{VS}/V_{VIQST} = 13.5 V; • MOSFET IPG20N06S2L-35A for SSW, MOSFET IPG20N06S4L-26A for PREREG Half-bridge • BUCK CORE Load = 1mA, BUCK IF Load = 200uA • $T_j \leq 85°C$	DS-2119

(table continues...)

Table 33 (continued) Electrical characteristics state machine (FSM)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SLEEP state current consumption	I_{q_SLEEP}	–	6.1	9.5	mA	Current consumptions are measured from V_S(T30) : • BUCK PREREG and QUC are enabled • BUCK IF, QVR, BUCK CORE, QCO and QST are switched off; • BOOST is not populated; • $V_{R1FB} = V_{R1FB\_5V5}$; • f_{DCDC} = 2.2 MHz; • VMON1 and VMON2 are disabled; • Error pin monitoring and all watchdog channels are disabled; • wakeup timer is disabled; • V_{VS}/V_{VIQST} = 13.5 V; • MOSFET IPG20N06S2L-35A for SSW, MOSFET IPG20N06S4L-26A for PREREG Half-bridge • BUCK CORE Load = 1mA, BUCK IF Load = 200uA • $T_j \leq 85°C$	DS-2121

(table continues...)

Table 33 (continued) Electrical characteristics state machine (FSM)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SLEEP state current consumption	I_{q_SLEEP}	–	13.4	20.8	mA	Current consumptions are measured from V_S(T30) : • BUCK PREREG, BUCK IF and QUC are enabled • QVR, BUCK CORE, QCO and QST are switched off; • BOOST is not populated; • $V_{R1FB} = V_{R1FB\_5V5}$; • f_{DCDC} = 2.2 MHz; • VMON1 and VMON2 are disabled; • Error pin monitoring and all watchdog channels are disabled; • wakeup timer is disabled; • V_{VS}/V_{VIQST} = 13.5 V; • MOSFET IPG20N06S2L-35A for SSW, MOSFET IPG20N06S4L-26A for PREREG Half-bridge • BUCK CORE Load = 1mA, BUCK IF Load = 200uA • $T_j \leq 85°C$	DS-2123

(table continues...)

Table 33 (continued) Electrical characteristics state machine (FSM)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SLEEP state current consumption	I_{q_SLEEP}	–	14	21.7	mA	Current consumptions are measured from V_S(T30) : • BUCK PREREG, BUCK IF, QVR and QUC are enabled • BUCK CORE, QCO and QST are switched off; • BOOST is not populated; • $V_{R1FB} = V_{R1FB\_5V5}$; • f_{DCDC} = 2.2 MHz; • VMON1 and VMON2 are disabled; • Error pin monitoring and all watchdog channels are disabled; • wakeup timer is disabled; • V_{VS}/V_{VIQST} = 13.5 V; • MOSFET IPG20N06S2L-35A for SSW, MOSFET IPG20N06S4L-26A for PREREG Half-bridge • BUCK CORE Load = 1mA, BUCK IF Load = 200uA • $T_j \leq 85°C$	DS-2125

(table continues...)

Table 33 (continued) Electrical characteristics state machine (FSM)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SLEEP state current consumption	I_{q_SLEEP}	–	15.2	23.6	mA	Current consumptions are measured from V_S(T30) : • BUCK PREREG, BUCK IF, QVR, BUCK CORE, QCO and QUC are enabled • QST is switched off; • BOOST is not populated; • $V_{R1FB} = V_{R1FB\_5V5}$; • f_{DCDC} = 2.2 MHz; • VMON1 and VMON2 are disabled; • Error pin monitoring and all watchdog channels are disabled; • wakeup timer is disabled; • V_{VS}/V_{VIQST} = 13.5 V; • MOSFET IPG20N06S2L-35A for SSW, MOSFET IPG20N06S4L-26A for PREREG Half-bridge • BUCK CORE Load = 1mA, BUCK IF Load = 200uA • $T_j \leq 85°C$	DS-2127

(table continues...)

Table 33 (continued) Electrical characteristics state machine (FSM)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
STANDBY state current consumption	$I_{q\_STANDBY\ OFF}$	–	20	24	µA	Current consumptions are measured from V_S(T30): • All output voltage rails (BUCK PREREG, BUCK CORE, BUCK IF, BOOST, QUC, QVR, QST, QCO) are switched off • VMON1 and VMON2 are disabled • Error pin monitoring and all watchdog channels are disabled • Wakeup timer is disabled • Pin ENA and pin WAK are monitored for wakeup events • 10 V ≤ V_{VS}/V_{VIQST} ≤ 28 V • T_j ≤ 85°C • Quiescent current also depending on the leakage of diode D3	DS-2079

(table continues...)

Table 33 (continued) Electrical characteristics state machine (FSM)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
STANDBY state current consumption with QST ON	$I_{q\_STANDBY\_ON}$	–	54	70	µA	Current consumptions are measured from V_S(T30): • QST is switched ON • All output voltage rails (BUCK PREREG, BUCK CORE, BUCK IF, BOOST, QUC, QVR, QCO) are switched off • ERRx pin monitoring, WWD and F WD are disabled • VMON1 and VMON2 are disabled • Wakeup timer is disabled • Pin ENA and pin WAK are monitored for wakeup events • 10 V ≤ V_{VS}/V_{VIQST} ≤ 28 V • T_j ≤ 85°C • Quiescent current also depending on the leakage of diode D3	DS-1544

(table continues...)

Table 33 (continued) Electrical characteristics state machine (FSM)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
STANDBY state current consumption with WUT ON	$I_{q\_WUT\_ON}$	–	–	50	µA	Current consumptions are measured from V_S(T30): • QST is switched OFF • All output voltage rails (BUCK PREREG, BUCK CORE, BUCK IF, BOOST, QUC, QVR, QCO) are switched off • ERRx pin monitoring, WWD and F WD are disabled • VMON1 and VMON2 are disabled • Wakeup timer is enabled • Pin ENA and pin WAK are monitored for wakeup events • 10 V ≤ V_{VS}/V_{VIQST} ≤ 28 V • T_j ≤ 85°C • Quiescent current also depending on the leakage of diode D3	DS-2052

(table continues...)

Table 33 (continued) Electrical characteristics state machine (FSM)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
STANDBY state current consumption with QST and WUT ON	$I_{q\_STANDBY\_WUT\_ON}$	–	–	70	µA	Current consumptions are measured from V_S(T30): • QST is switched ON • All output voltage rails (BUCK PREREG, BUCK CORE, BUCK IF, BOOST, QUC, QVR, QCO) are switched off • ERRx pin monitoring, WWD and F WD are disabled • VMON1 and VMON2 are disabled • Wakeup timer is enabled • Pin ENA and pin WAK are monitored for wakeup events • 10 V ≤ V_{VS}/V_{VIQST} ≤ 28 V • T_j ≤ 85°C • Quiescent current also depending on the leakage of diode D3	DS-2051
Operational state current consumption	$I_{q\_Operational}$	–	20	30	mA	Current consumptions are measured from V_S(T30) without load current applied to post regulators: • All output voltage rails (BUCK PREREG, BUCK CORE, BUCK IF, BOOST, QUC, QTS, QVR, QCO) are switched on • ERRx pin monitoring, WWD and F WD are disabled • VMON1 and VMON2 are disabled • Wakeup timer is disabled • f_{DCDC} = 2.2 MHz • 10 V ≤ V_{VS}/V_{VIQST} ≤ 28 V • T_j ≤ 85°C	DS-2080

(table continues...)

Table 33 (continued) Electrical characteristics state machine (FSM)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
FAILSAFE state current consumption	$I_{q\_FAILSAFE}$	–	120	200	µA	Current consumptions are measured from V_S(T30): • All output voltage rails (BUCK PREREG, BUCK CORE, BUCK IF, BOOST, QUC, QVR, QST, QCO) are switched off • ERRx pin monitoring, WWD and FWD are disabled • VMON1 and VMON2 are disabled • Wakeup timer is disabled • Pin ENA and pin WAK are monitored for wakeup events • 10 V ≤ V_{VS}/V_{VIQST} ≤ 18 V • T_j ≤ 40°C • $t_{FAILSAFE}$ > $t_{FAILSAFE\_min}$ • Quiescent current also depending on the leakage of diode D3	DS-1546

1) Not subject to production test, specified by design

10 Monitoring functions

10.1 Watchdog functions (WD)

10.1.1 Introduction watchdog functions (WD)

The purpose of a watchdog is to provide a monitoring mechanism for the application microcontroller by means of temporal and logical program sequence monitoring. A watchdog may detect defective MCU program sequence, where individual program elements (e.g. software modules, subprograms, or commands) are processed in the wrong sequence or period of time, or if the clock of the processor is faulty.

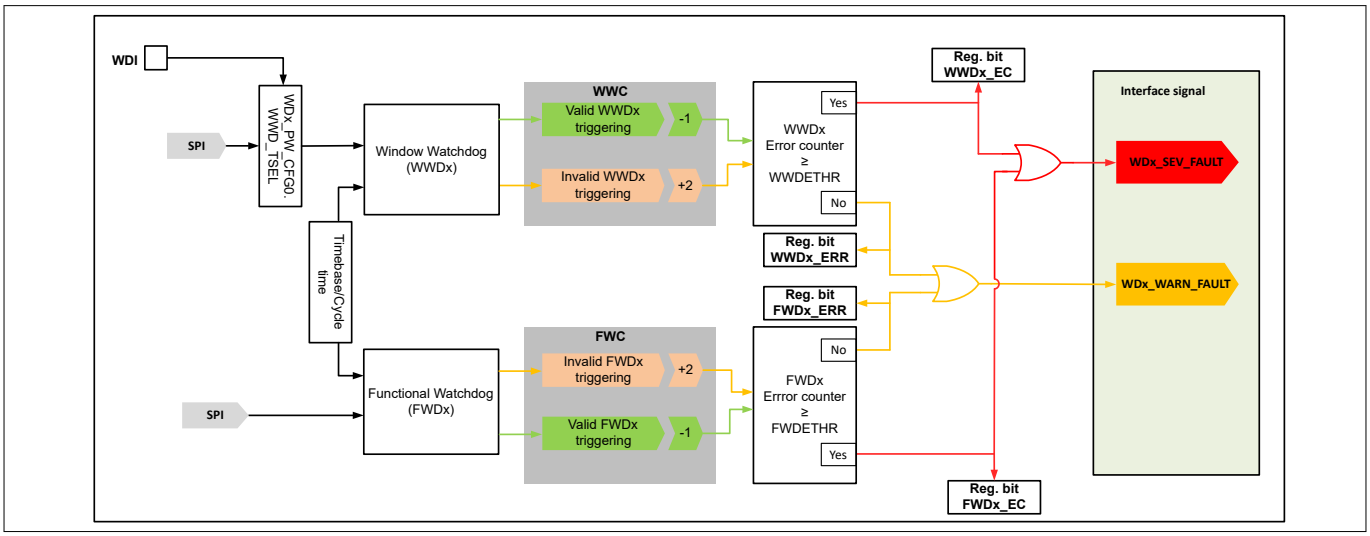


Figure 33 Functional block diagram watchdog functions

(x = 1; 2)

The device incorporates two independent watchdog instances(WD). Each of them consisting of one window watchdog module (WWD) and one functional watchdog module (FWD):

- WD1: Consisting of WWD1 and FWD1
- WD2: Consisting of WWD2 and FWD2

***Note**: Watchdog instance 2 can only be used if REDUCED OPERATION is enabled (**REDOP_RS_CFG1.EN = 1**).*

The watchdog modules differentiate between the following services:

- "Valid WWDx triggering" or "Invalid WWDx triggering"
- "Valid FWDx triggering" or "Invalid FWDx triggering"

Each WWD module and each FWD module has its own error counters assigned and monitors the watchdog triggers. This allows an operation of a WWD and FWD in parallel. A WWDx shares the same time base with its corresponding FWDx.

The basic time base configuration is done with the register bit WDx_PW_CFG0.CYC. For shortening the time base even further an additional divider by 10 can be enabled which results in a time base as depicted:

$$time\ \ base\ \ = \frac{WDx\_RS\_CFG0\,.\,CYC}{WDx\_RS\_CFG1\,.\,CYC\_DIV}\ \text{(interpreted value)}$$

Equation 1

Configuration

Each watchdog module can be activated and deactivated independently in the register bits **WDx_PW_CFG0.WWD_EN** and **WDx_PW_CFG0.FWD_EN**.

Automatic deactivation of the watchdogs on entering SLEEP state can be configured in the register bits **WDx_PW_CFG1.SLP_EN.**

10.1.2 Window watchdog (WWD)

10.1.2.1 Functional description window watchdog (WWD)

The window watchdogs (WWDx) can be configured in **WDx_PW_CFG0.WWD_TSEL** to be triggered by one of the following events:

- Falling edge at the digital input pin WDI
- Writing WWD1_TRIG.TRIG via SPI. In order to trigger the watchdog:
  - Read the last internal service value (**WWDx_TRIG.TRIG_STAT**) received via SPI
  - Write the inverted value of the (**WWDx_TRIG.TRIG_STAT**) to the **WWDx_TRIG.TRIG** bitfield

If the trigger event occurs during the open window period (OW), then the device detects a **"valid WWDx triggering".** The open window is closed immediately and the closed window starts.

If no trigger event occurs during the open window period or if the trigger event occurs during the closed window period (CW), then the device detects an **"invalid WWDx triggering"**.

The duration of the open window t_{OW} and the closed window t_{CW} can be calculated with the following formulas:

$$t_{OW} = (\text{WWDx\_PW\_OW\_CFG.OW} + 1) \times 50 \times time\ base$$

Equation 2

$$t_{CW} = (\text{WWDx\_PW\_CW\_CFG.CW} + 1) \times 50 \times time\ base$$

Equation 3

The duration of the closed window of the window watchdog is also configurable to be set to 0. If this setting is used (**WWDx_PW_CW_CFG.CW_DIS** = 1), a successful trigger within the open window will immediately initialize a new open window again.

10.1.2.1.1 Valid triggering of the window watchdog

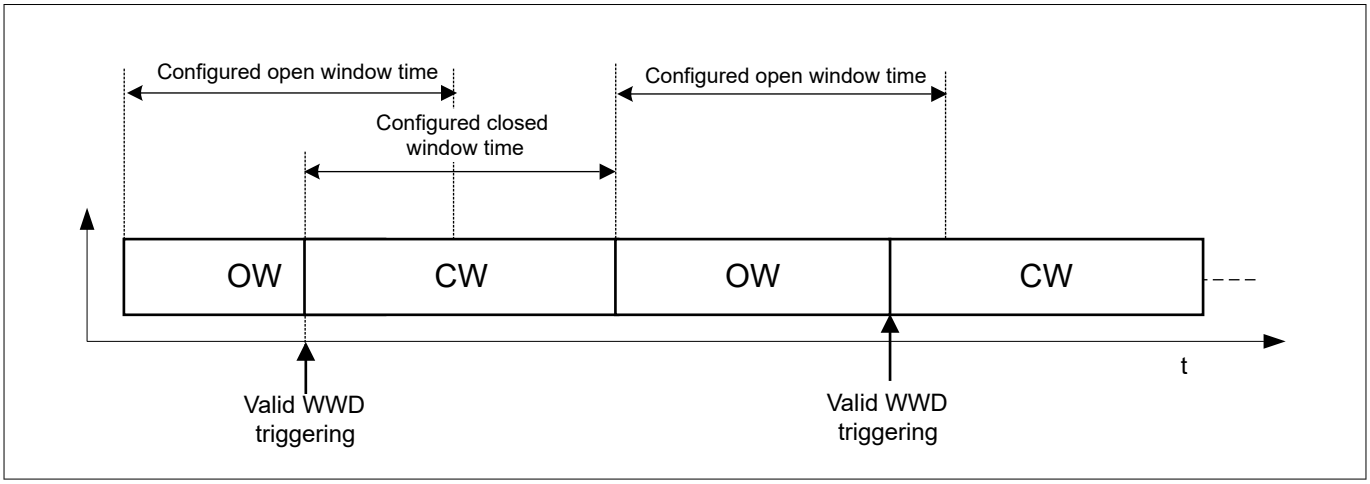


Figure 34 Valid triggering of the window watchdog

Initially the window watchdog starts with an open window. If successfully triggered, the open window closes immediately and a closed window is started. After the closed window was active for the configured time, an open window is started again. After reconfiguration the window watchdog starts with the configured open window and its corresponding error counter is reset.

10.1.2.1.2 Invalid triggering due to missing trigger during open window

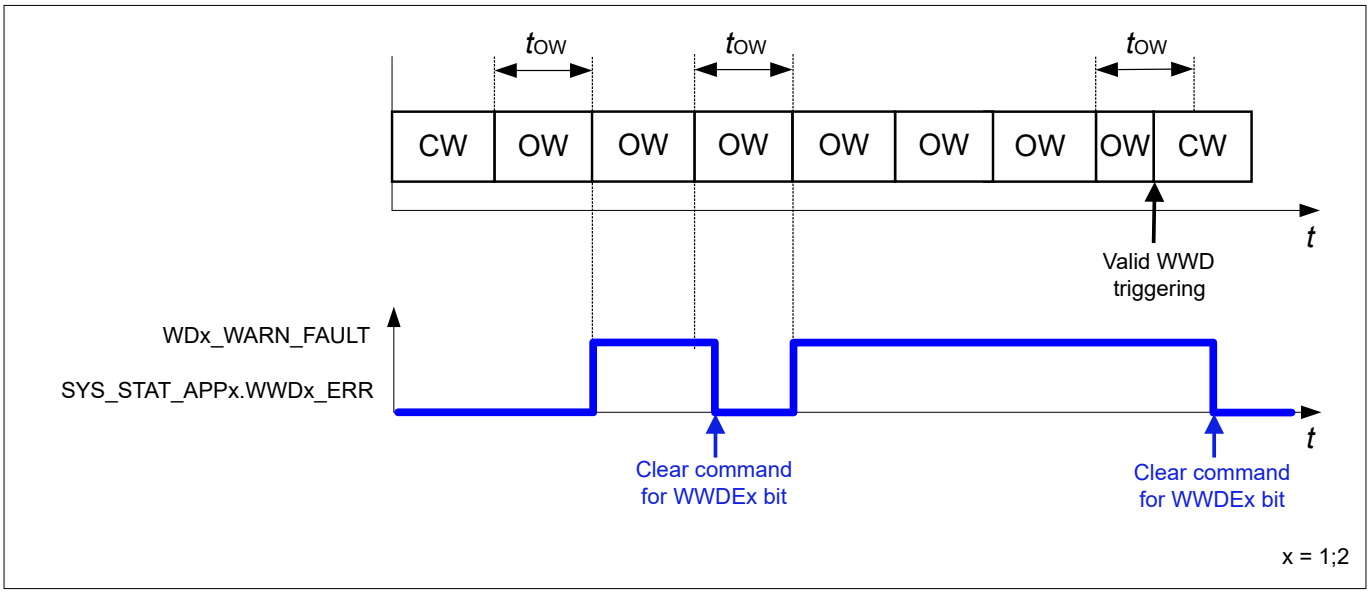


Figure 35 Invalid service due to missing trigger during open window assuming error counter remains smaller than threshold

If the open window expires without any trigger, then the watchdog starts a new timing sequence with an open window and the device performs the following actions:

1. Increment the corresponding error counter value by 2, see Chapter 10.1.2.1.5
2. If the error counter remains below the configured threshold:
   - then:
     - Generate a watchdog warning fault WDx_WARN_FAULT
     - Set the corresponding error bit **SYS_STAT_APPx.WWDx_ERR**, which can be cleared via SPI
   - else:
     - Generate a watchdog severe fault WDx_SEV_FAULT

(x = 1; 2)

10.1.2.1.3 Invalid triggering due to trigger during closed window

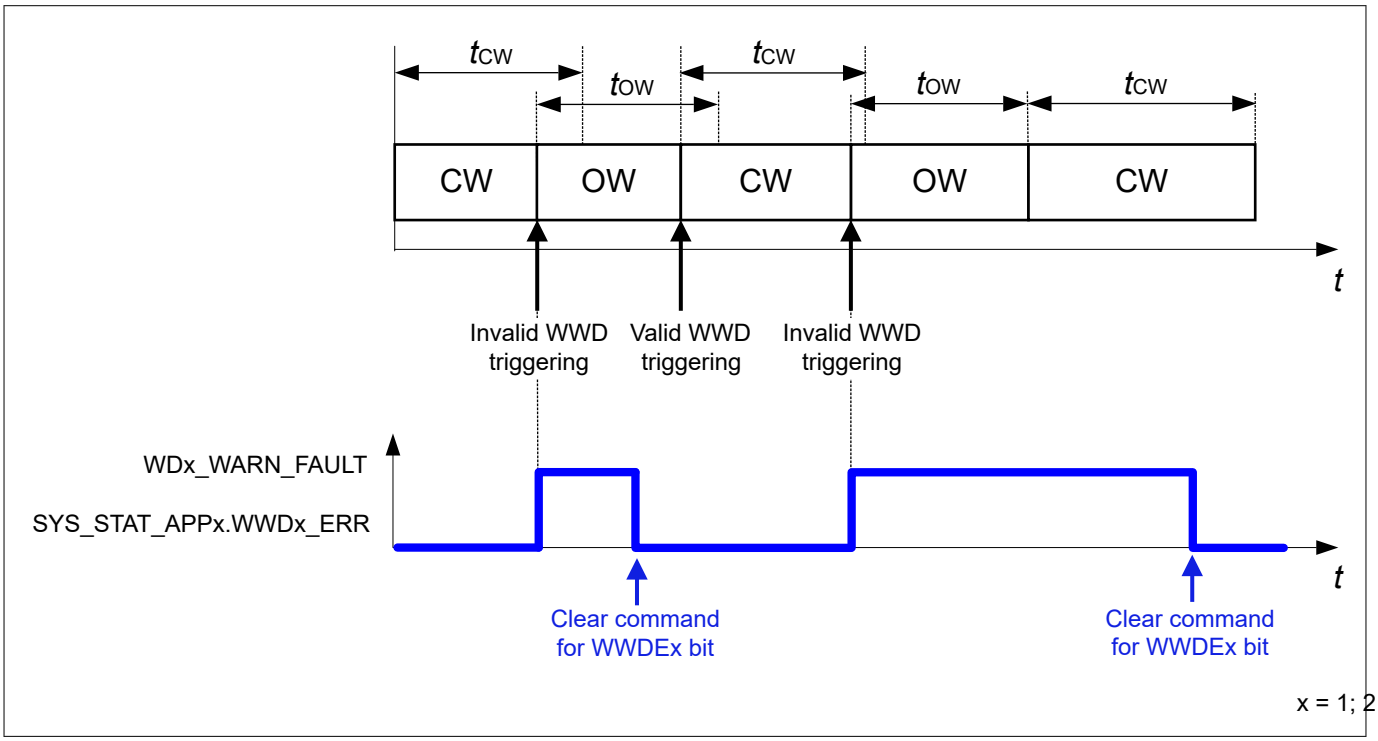


Figure 36 Invalid triggering due to trigger during closed window assuming error counter remains smaller than threshold

If the watchdog is triggered during the closed window, then it starts a new watchdog timing sequence with an open window and the device performs the following actions:

1. Increment the corresponding error counter value by 2, see Chapter 10.1.2.1.5
2. If the error counter remains below the configured threshold:
   - then:
     - Generate a watchdog warning fault WDx_WARN_FAULT
     - Set the corresponding error bit **SYS_STAT_APPx.WWDx_ERR**, which can be cleared via SPI
   - else:
     - Generate a watchdog severe fault WDx_SEV_FAULT

(x = 1; 2)

10.1.2.1.4 Watchdog startup behavior (enable and reset)

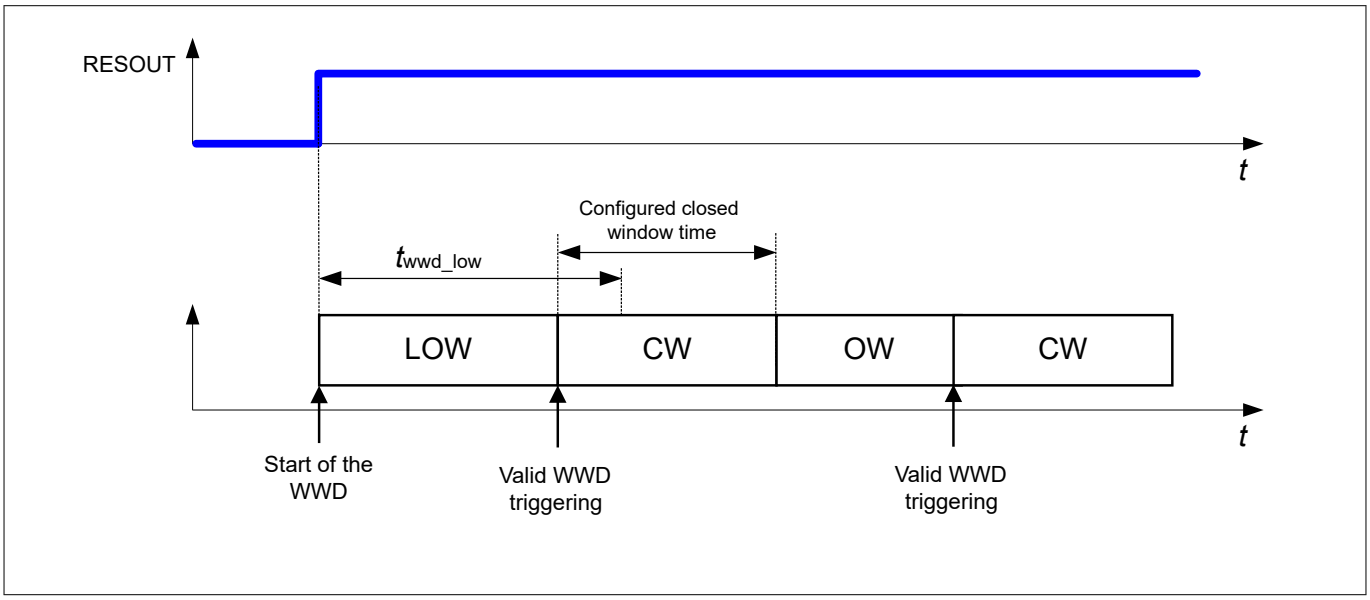


Figure 37 Watchdog initialization phase

Whenever INIT state is entered and RESOUT was released (pin RESOUT goes "high"), the watchdog is enabled and starts the first watchdog timing window sequence with a long open window. The long open window time t_{WWD_LOW} matches the INIT timer duration t_{INIT}. If a valid trigger is provided within t_{WWD_LOW} the WWD starts operating as described in this chapter, else the watchdog long open window expires together with the INIT timer and an INIT_TIMER_FAULT is generated.

10.1.2.1.5 Windows watchdog error counter

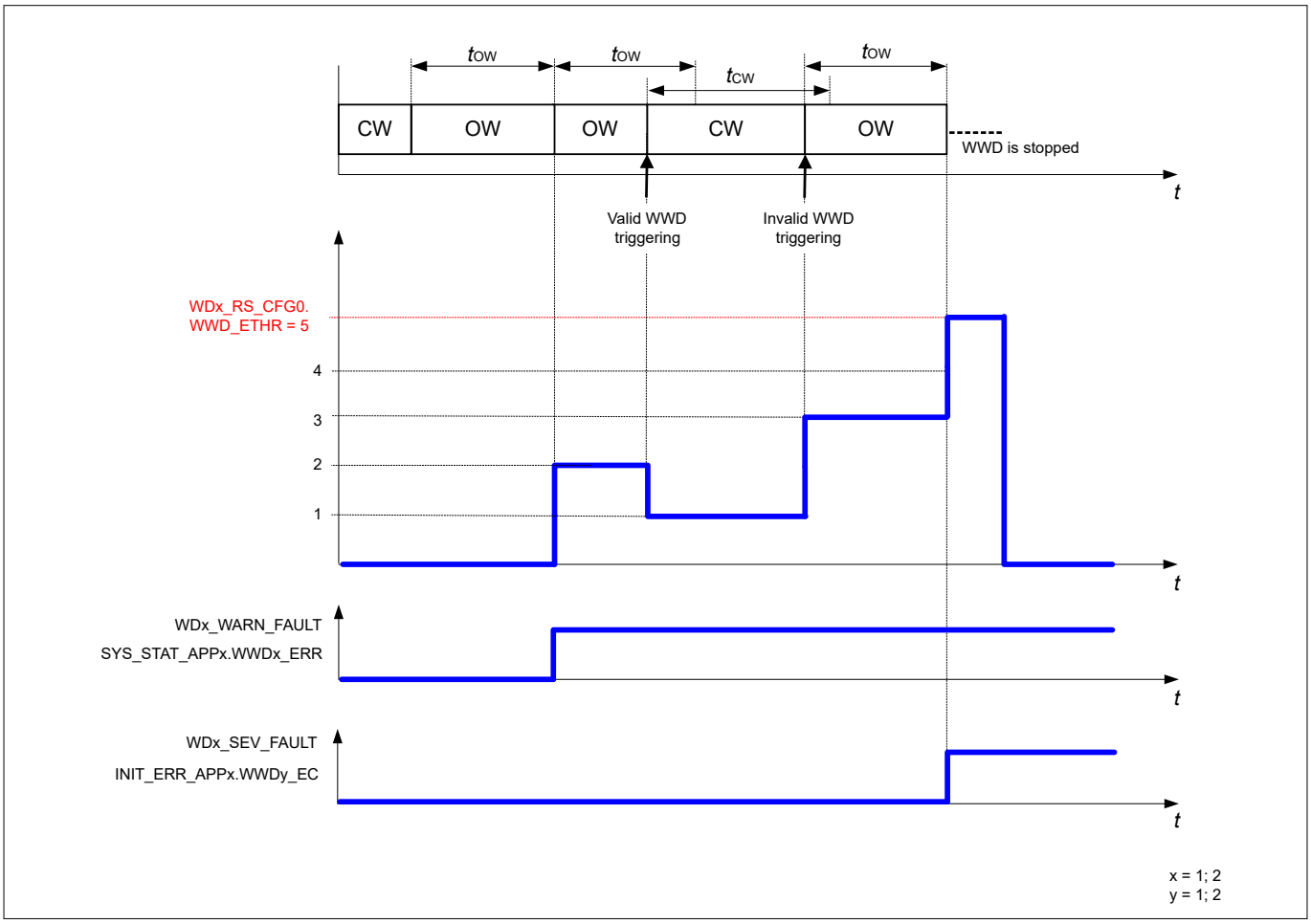


Figure 38 Window watchdog error counter

If the device detects an invalid triggering, it increments the value of **WWDx_ECNT_STAT.ECNT** by 2.

If the device detects a valid triggering, it decrements **WWDx_ECNT_STAT.ECNT** by 1.

If the value of the ECNT bitfield reaches the value of the configured WWD error counter threshold **WDx_RS_CFG0.WWD_ETHR**, the device performs the following actions:

- Generate a watchdog severe fault WDx_SEV_FAULT
- Set the corresponding error bit **INIT_ERR_APPx.WWDy_EC**, which can be cleared via SPI
- Clear the error counter

10.1.2.1.6 Timing constraints and behavior after configuring the watchdog

After configuring the watchdog and before first service there is a timing constraint, which needs to be respected. New configurations of the watchdog, such as open/closed window time, made by the microcontroller can take up to $t_{config\_delay\_wd}$ before they become active.. Because the watchdog configuration registers belong to the protected registers, an unlock and lock command must be sent. Only upon successfully receiving the lock command changes, made to the watchdog configuration, are mirrored to the corresponding reflected status registers and hereby made available for the PMICs modules. Hence the lock command marks the start of the timing before a first trigger can be received via SPI and applied to the new configuration. This timing limitation does however not apply to a trigger via WDI pin, since the combination of sample time t_{WDI_spl} and filter criteria will always be longer than $t_{config\_delay\_wd}$.

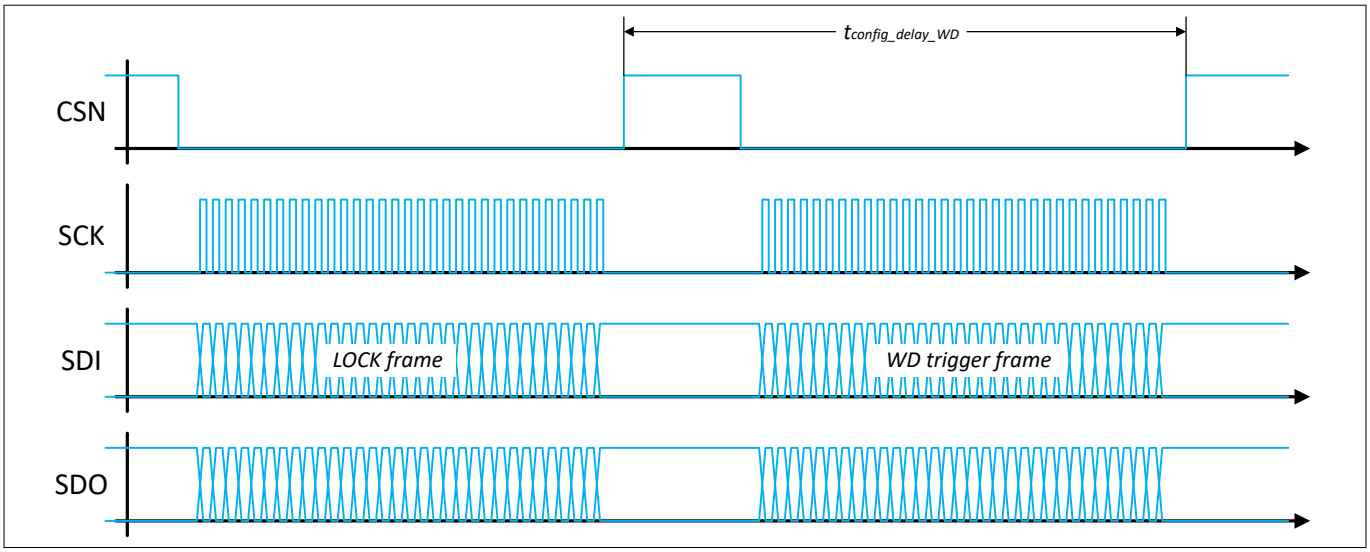


Figure 39 Watchdog trigger delay after configuration of watchdog module

10.1.2.2 Electrical characteristics window watchdog (WWD)

Table 34 Electrical characteristics window watchdog (WWD)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Cycle time	$t_{wwd\_cycle\_0}$	90	100	110	µs	Selectable via SPI	DS-1660
Cycle time, default	$t_{wwd\_cycle\_1}$	900	1000	1100	µs	Selectable via SPI	DS-1659
Long open window time	t_{wwd_low}	540	600	660	ms	Used for the initial WWD activation, or after each WWD restart due to recovery from a fault condition	DS-1653
WDI sample time	t_{WDI_spl}	45	50	55	µs	2) 1)	DS-2166
WD configuration-trigger delay	$t_{config\_delay\_wd}$	–	–	22	µs	2)	DS-2068

1) Since ERR2 and WDI share the same pin, they also share the electrical characteristic for voltage levels, hysteresis and current specification. Therefore it is being referred to table
Electrical characteristics error monitoring (ERR MON) [EC-Table-P]
.

2) Not subject to production test, specified by design

10.1.3 Functional watchdog (FWD)

10.1.3.1 Functional description functional watchdog (FWD)

The functional watchdog (FWD, also called question/answer watchdog) generates a question taken from a table and starts the heartbeat counter from zero. To trigger the functional watchdog correctly, the correct response bytes to each question must be written to an answer register, in a specific order, within the heartbeat period.

The heartbeat timer increments until it reaches its configured heart beat timer period. This period is configured via the register **FWDx_PW_HBTP_CFG.HBTP.** The length of the period follows the following formula for the heart beat timer:

$$heartbeat\quad time = (\mathrm{FWD}x\_\mathrm{RS\_HBTP\_CFG}\,.\,\mathrm{HBTP} \quad + \quad 1) \times 50 \times time\quad base \qquad (\text{interpreted} \quad \text{value})$$

Equation 4

10.1.3.1.1 Functional watchdog service

Upon enabling or reconfiguration of the FWD its corresponding HBT starts running. It waits for 4 bytes being written to FWDx_RSP.RSP or FWDx_RSP_SYNC.RSP_SYNC consecutively. The response bytes have to match the question which is read from FWDx_STAT.QUEST. If all bytes are written correctly before the HBT expires, the service was successful, which decrements the error counter and starts a new sequence with the next question in FWDx_STAT.QUEST. After having received the 4th response byte, the received byte is checked for correctness. If the response was incorrect and the last byte was written to FWDx_RSP_SYNC.RSP_SYNC the error counter of FWDx is incremented. Also, if the HBT expires the corresponding error counter is incremented. Status register FWDx_STAT is reset upon reconfiguration of the FWD.

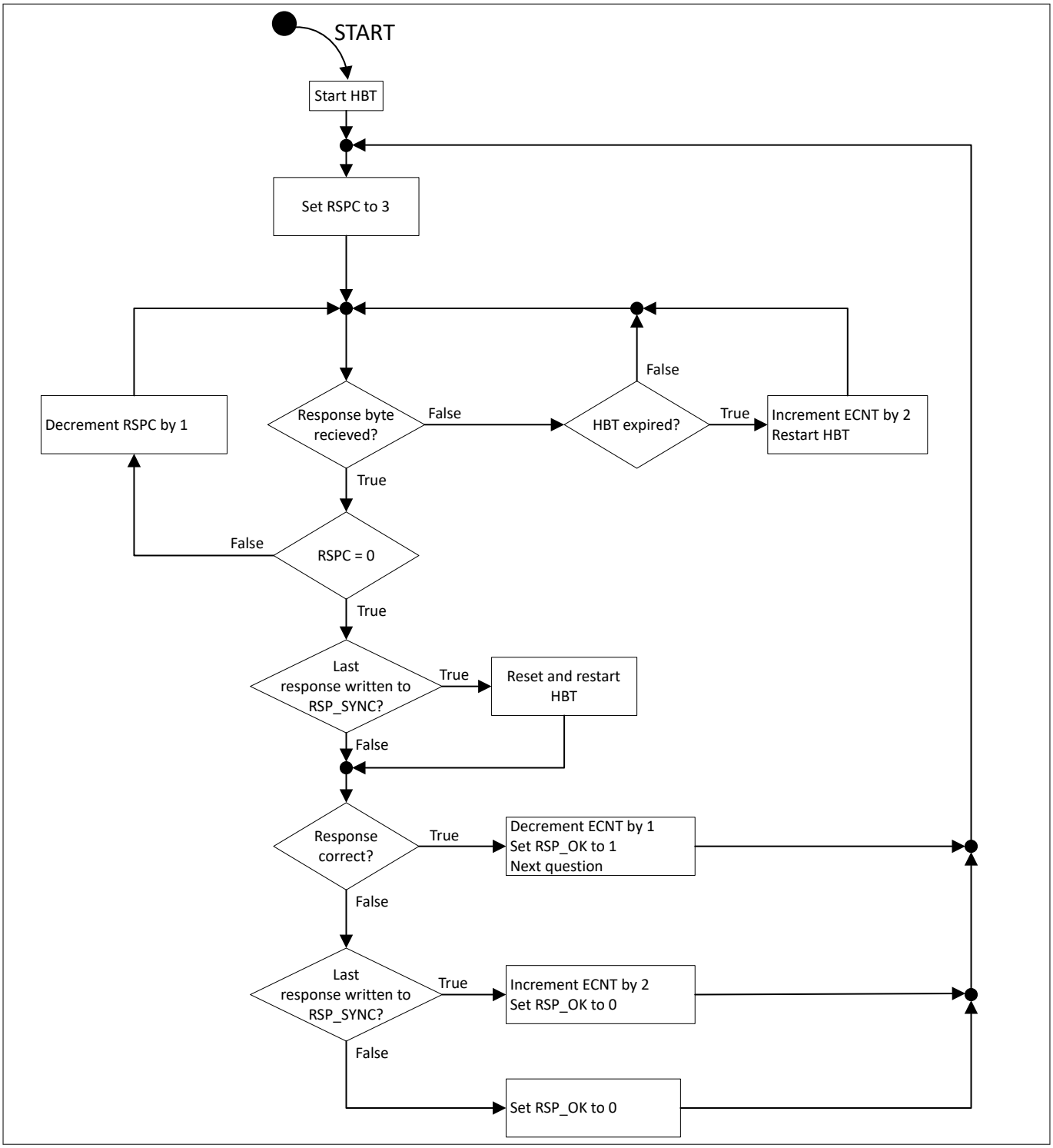


Figure 40 FWD flow chart

Valid triggering of the functional watchdog

The question consists of 4 bits, the corresponding answer consists of four consecutive response bytes.

The answer to each question in the register **FWDx_STAT.QUEST** needs to be written to the response register **FWDx_RSP.RSP** or **FWDx_RSP_SYNC.RSP_SYNC**.

Table 35 Functional watchdog questions and responses

QUEST[3:0]	RESP3	RESP2	RESP1	RESP0
0	FF	0F	F0	00
1	B0	40	BF	4F
2	E9	19	E6	16
3	A6	56	A9	59
4	75	85	7A	8A
5	3A	CA	35	C5
6	63	93	6C	9C
7	2C	DC	23	D3
8	D2	22	DD	2D
9	9D	6D	92	62
A	C4	34	CB	3B
B	8B	7B	84	74
C	58	A8	57	A7
D	17	E7	18	E8
E	4E	BE	41	B1
F	01	F1	0E	FE

If all of the following conditions are fulfilled for a question, the FWD is triggered correctly (valid trigger):

- The four response bytes are in the correct order from RESP3 to RESP0
- All four responses are correctly written to the response registers

To reset the heartbeat counter, the last response (RESP0) must be written to the synchronization response register **FWDx_RSP_SYNC.RSP_SYNC**.

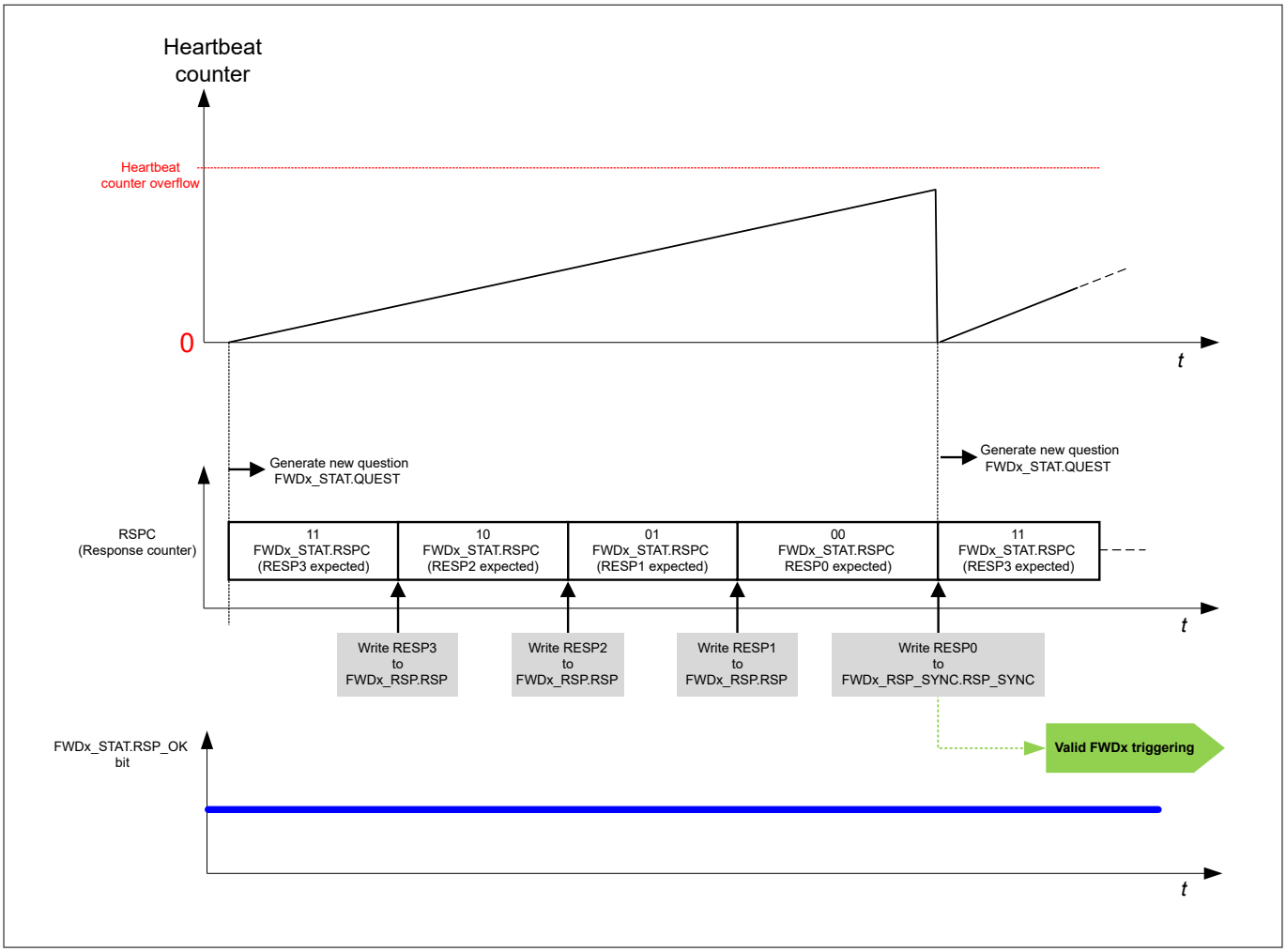


Figure 41 Example FWD: Possible valid triggering

Upon detection of a valid triggering, the device performs the following actions:

- Generate a new question
- Resets the response counter RSPC to 3
- Decrements the corresponding error counter value by 1 if not already at 0, see Chapter 10.1.2.1.5
- Sets the corresponding status bit of the response bytes **FWDx_STAT.RSP_OK** to 1
- If the last byte has been written to **FWDx_RSP_SYNC.RSP_SYNC** also the HBT periode is reset and restarted

Invalid triggering of the functional watchdog

If any of the following conditions is fulfilled, the FWD is triggered incorrectly (invalid trigger):

- Wrong order or content of the four response bytes
- Heartbeat period expires (heartbeat counter overflow)

Upon detection of an invalid trigger, the device performs the following actions:

- HBT expiration:
  - Increment error counter **FWDx_STAT.ECNT** by 2, see Chapter 10.1.3.1.2
  - Reset and restart HBT
- If the 4th byte was written to **FWDx_RSP_SYNC.RSP_SYNC**:
  - Reset and restart HBT

- Set the status bit **FWDx_STAT.RSP_OK** to 0
- Increment the error counter **FWDx_STAT.ECNT** by 2, see Chapter 10.1.3.1.2

- If the 4th byte was written to **FWDx_RSP.RSP**:
  - Set the status bit **FWDx_STAT.RSP_OK** to 0
- If error counter **FWDx_STAT.ECNT** was incremented (see Reaction on faults):
  - Generate a watchdog warning fault WDx_WARN_FAULT if error counter is still below configured error threshold, see Chapter 9
  - Sets the corresponding error bit **SYS_STAT_APPx.FWDx_ERR**, which can be cleared via SPI

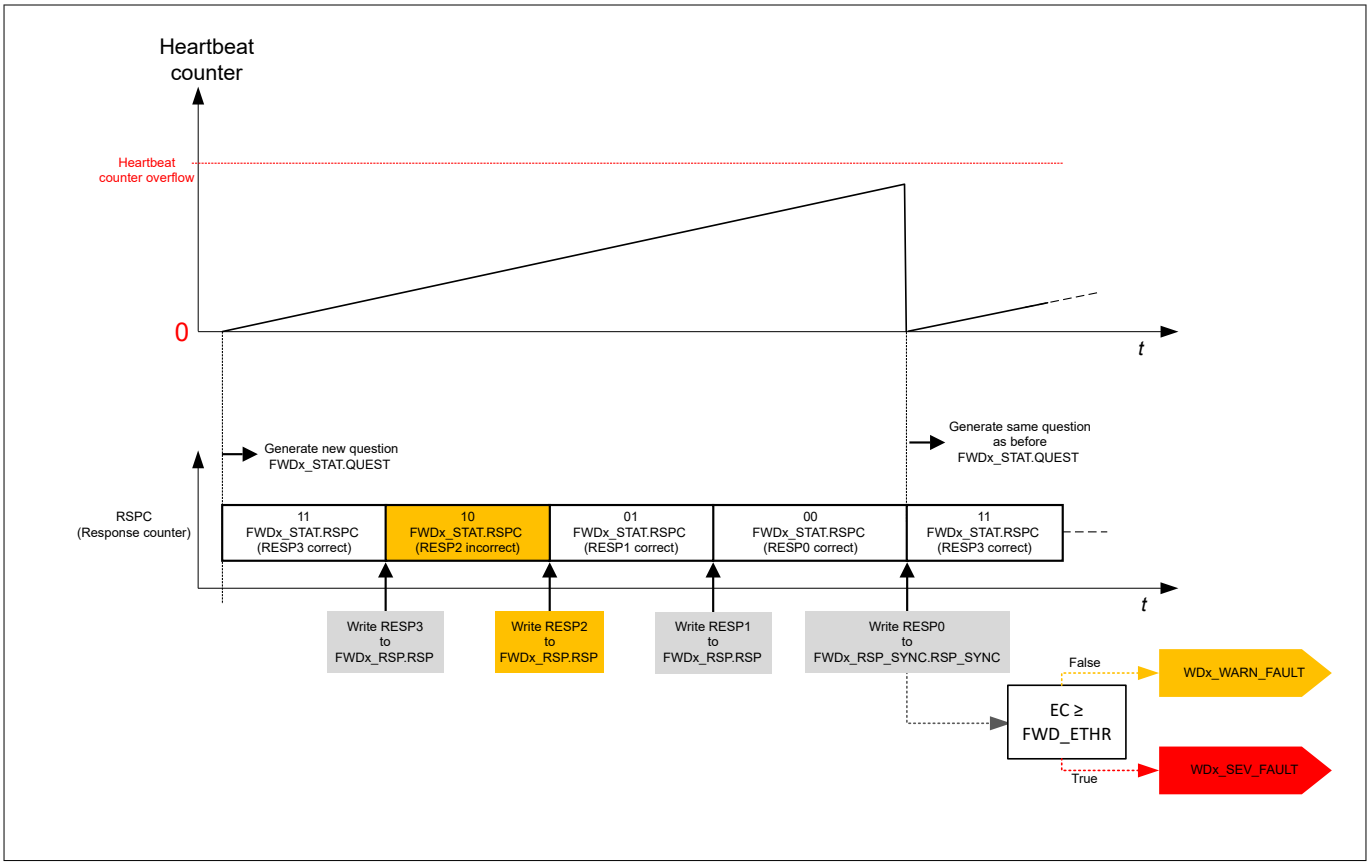


Figure 42 FWD: Wrong response (RESP2) timing diagram

(x = 1, 2)

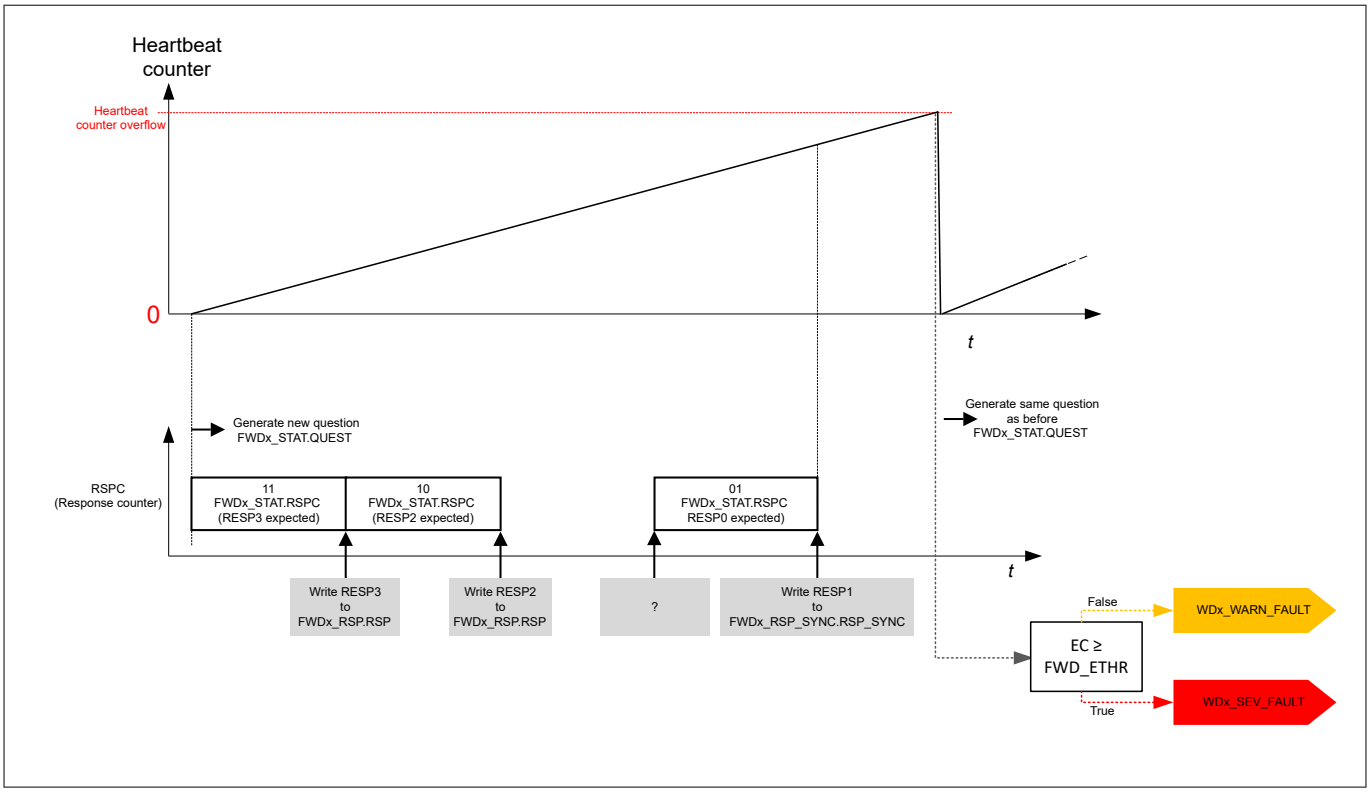


Figure 43 Missing response timing diagram

(x = 1, 2)

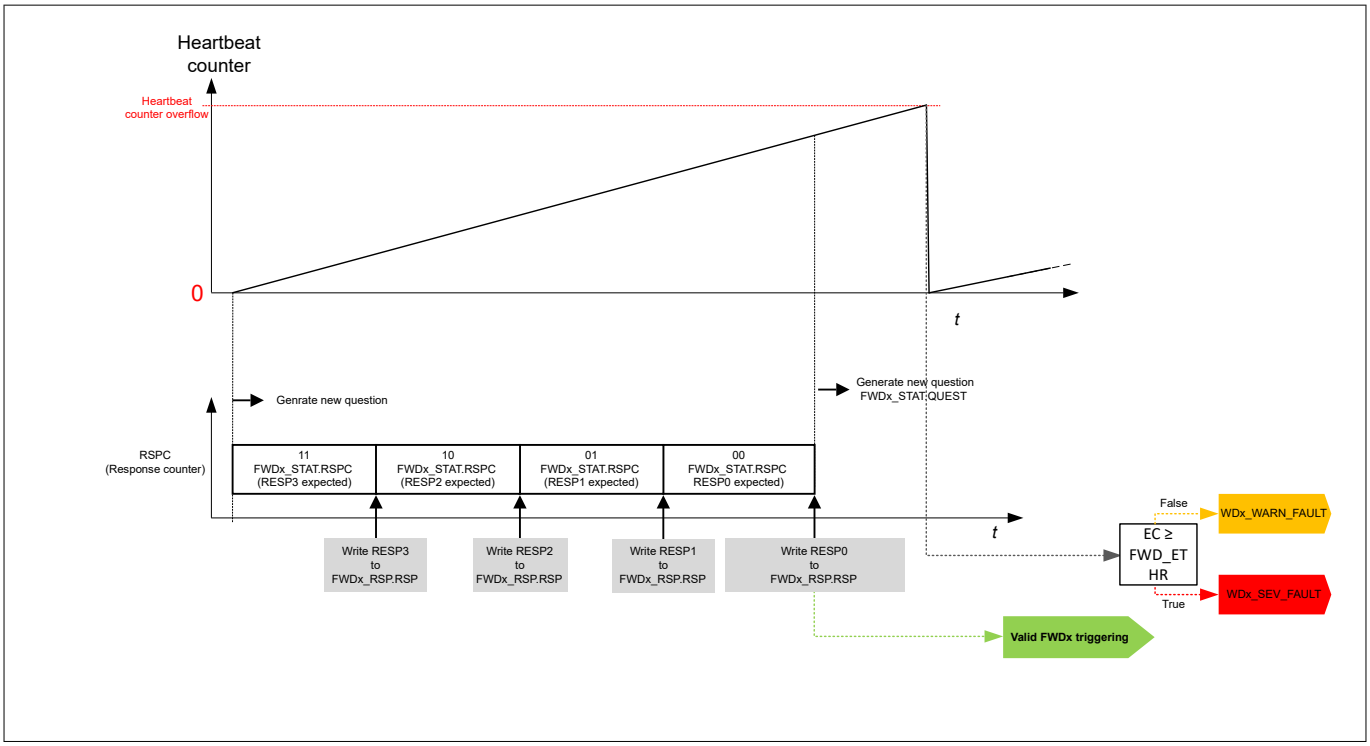


Figure 44 Missing synchronization timing diagram

(x = 1, 2)

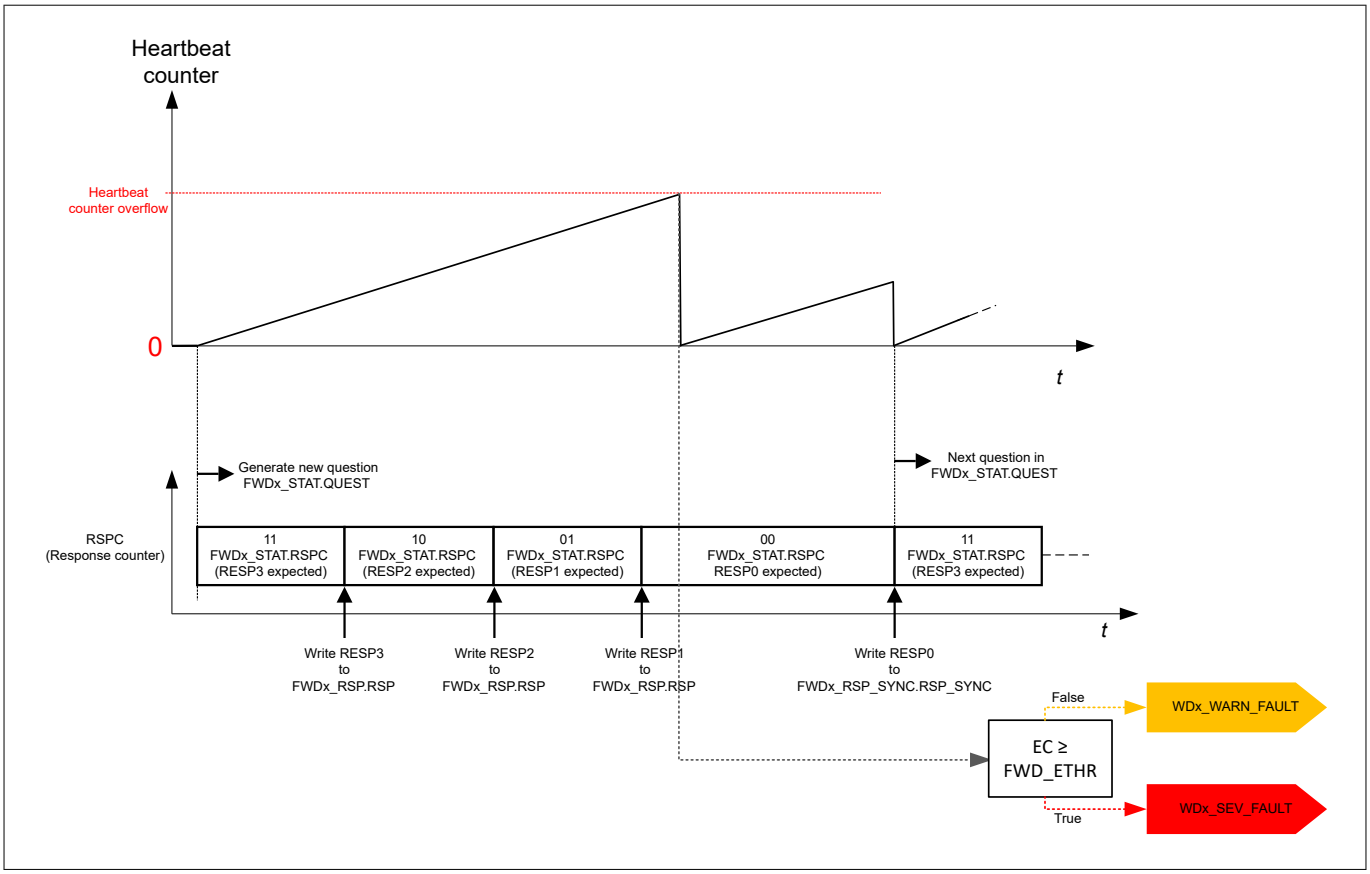


Figure 45 Heartbeat counter overflow

(x = 1, 2)

10.1.3.1.2 Functional watchdog error counter overflow

If the device detects valid FWDx triggering, then it decrements the value of the ECNT bitfield in the **FWDx_STAT** register by 1 if greater than 0.

If the device detects invalid FWDx triggering, then it increments the value of the ECNT bitfield in the **FWDx_STAT** register by 2.

If the value of the ECNT bitfield reaches or exceeds the value of the configured FWD error counter threshold **WDx_PW_CFG1.FWD_ETHR**, the device performs the following actions (see Reaction on faults):

- Generate a watchdog severe fault WDx_SEV_FAULT, see Chapter 9
- Set the corresponding failure bit (register **INIT_ERR_APPx.FWDy_EC**), which can be cleared via SPI
- Clear the FWD error counter

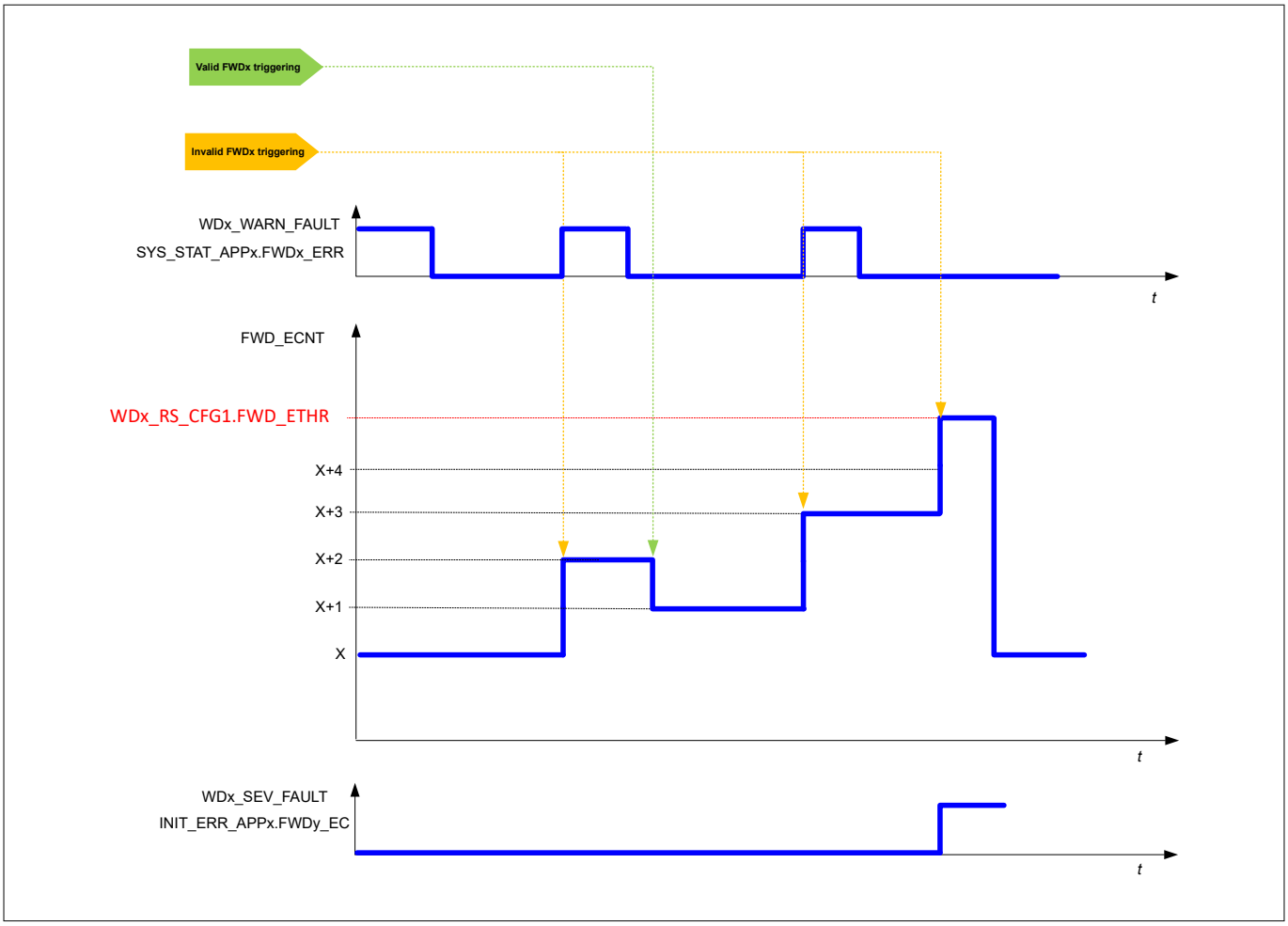


Figure 46 Error counter (ECNT) overflow timing diagram

(x = 1, 2)
(y = 1, 2)

10.2 Error monitoring (ERR MON)

10.2.1 Introduction

The error monitoring (ERR MON) function is a safety mechanism that supervises the safety management unit (SMU) of the application's microcontroller. There are three independent ERRx inputs. If one of the error monitors detects a signal frequency at its input which is outside of the valid frequency range, the device reacts accordingly (see Reaction on faults).

(x=0, 1, 2)

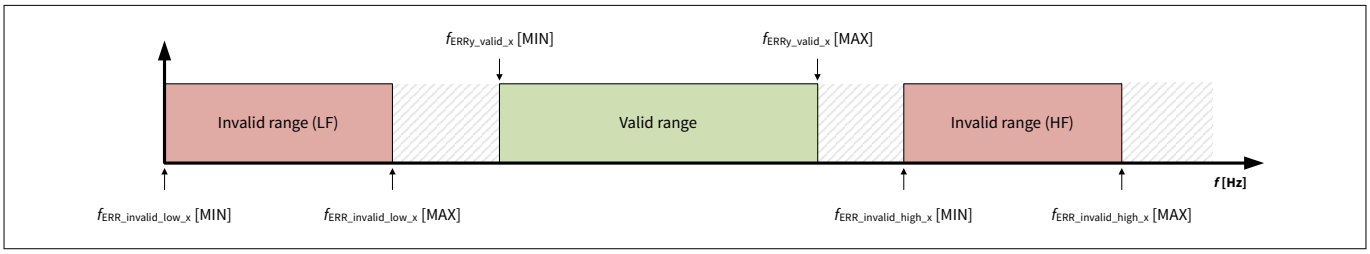


Figure 47 Toggling frequency signal applied on ERRy monitoring inputs

(x = LF; HF)

(y = 0; 1; 2)

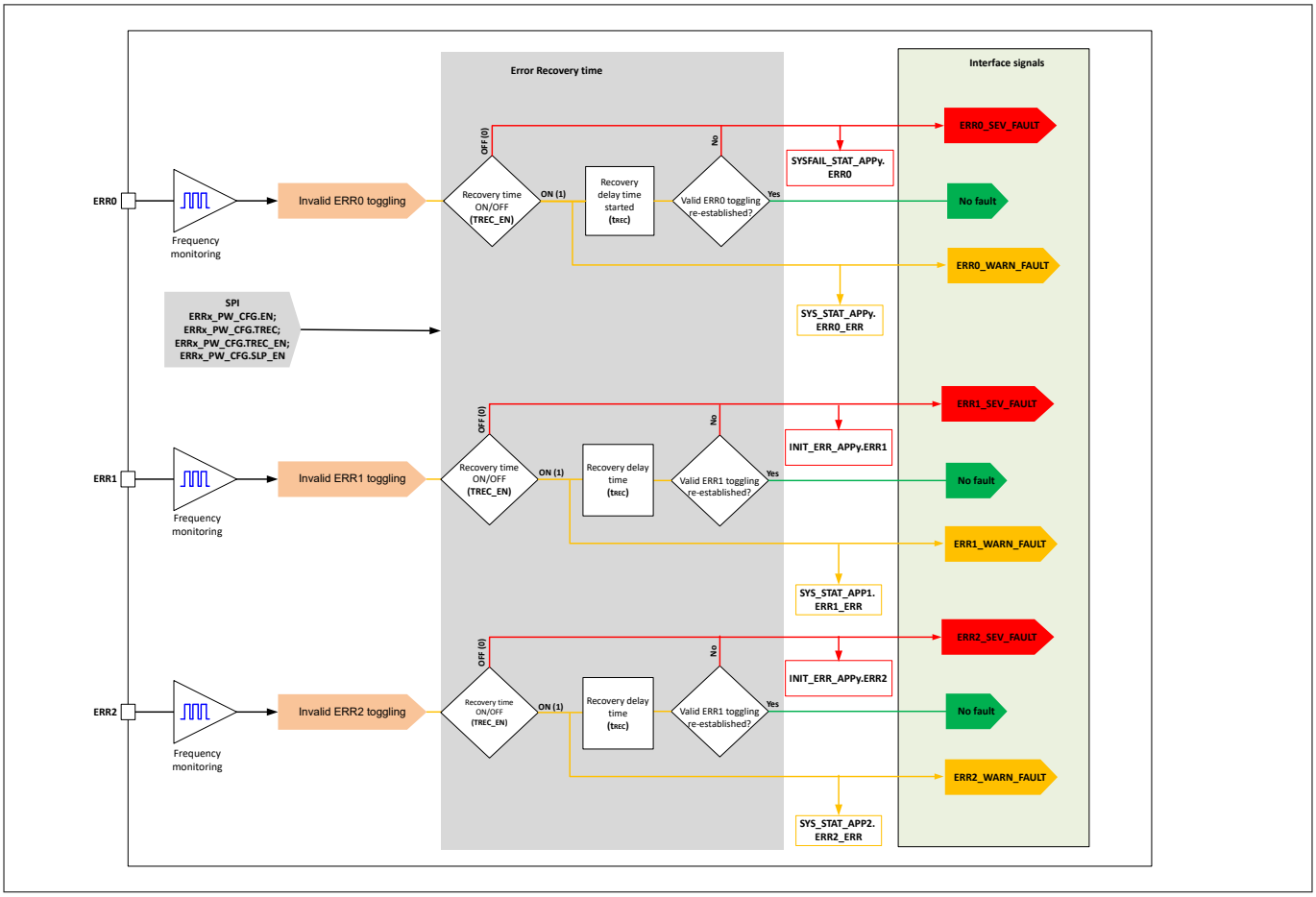


Figure 48 Functional block diagram error monitoring functions

(x = 1, 2, 3; y = 1, 2)

The device provides the following error monitoring channels:

- ERR MON0 for the ERR0 pin
- ERR MON1 for the ERR1 pin
- ERR MON2 for the ERR2 pin

10.2.2 Functional description error monitoring (ERR MON)

10.2.2.1 Error monitoring initialization

The error monitoring module can be properly triggered either using a low or a high frequency:

- Valid input signal frequency low ($f_{ERRx\_valid\_LOW}$)
- Valid input signal frequency high ($f_{ERRx\_valid\_HIGH}$)

Upon applying the error monitoring signal at ERRx, the device ignores the first six edges of the signal to allow stabilization of the external signal. Next the device automatically detects the frequency range among the allowed ranges. If no correct frequency range can be detected, it reacts accordingly (see Reaction on faults). While operating, the ERRx module continuously monitors the applied signal. This procedure is always executed whenever the ERRx module experiences a reset condition and reinitialization is required. Reset conditions are:

- RESOUT showed a reset
- Starting from POWERDOWN
- Recovering from FAILSAFE, STANDBY or SLEEP with QUC or BUCKCORE disabled
- Exiting form SLEEP with **ERRx_RS_CFG.EN** = 1 and **ERRx_RS_CFG.SLP_EN** = 0

(x = 0; 1; 2)

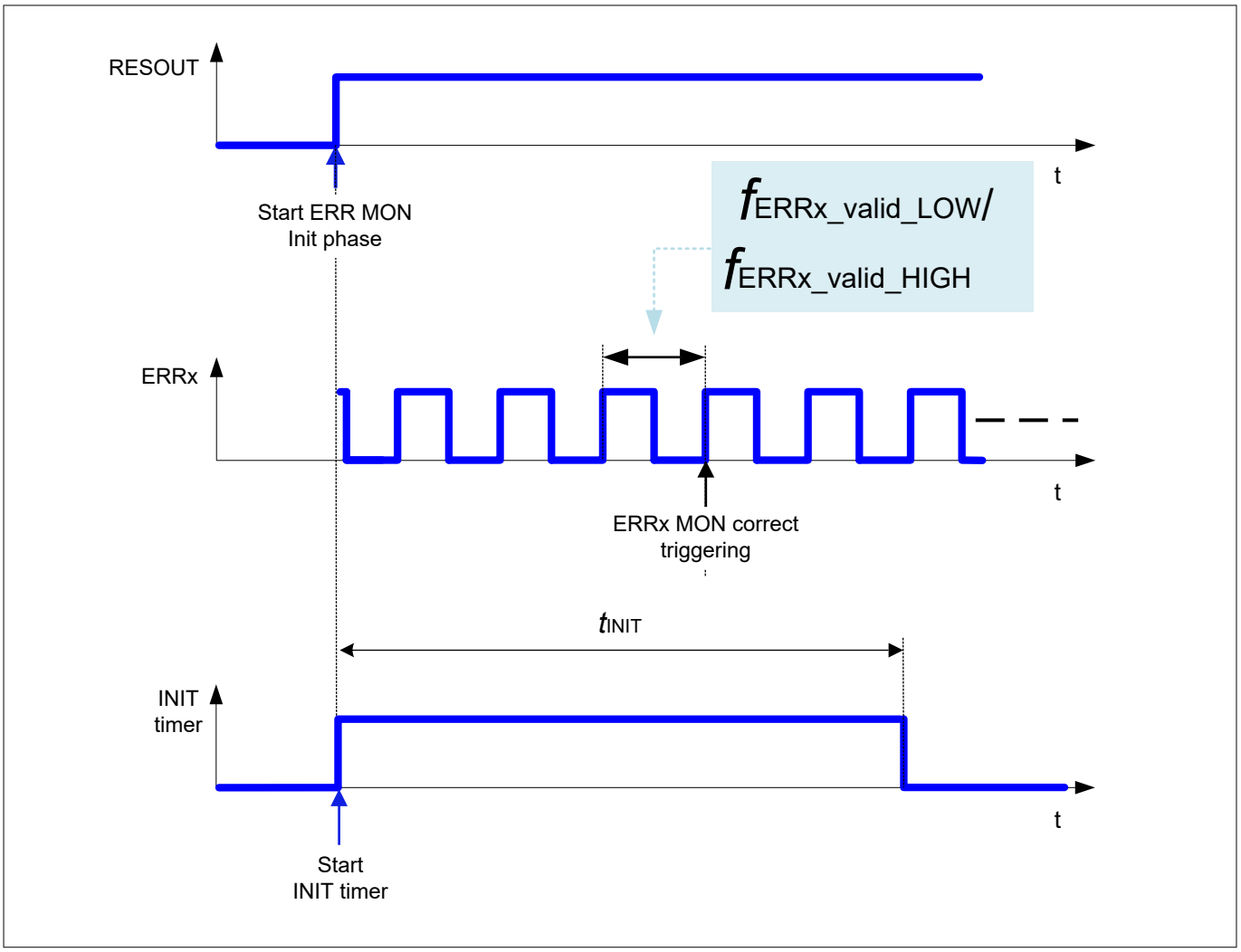


Figure 49 Error monitoring correct triggering

(x = 0; 1; 2)

10.2.2.2 Error monitoring configuration

Each error monitoring channel can be activated or deactivated independently in the register bit **ERRx_PW_CFG.EN**.

On reactivating the error monitoring channel via SPI, the device starts the reactivation timeout after reenabling $t_{ERR\_to\_ren}$. When the device detects an edge on the ERRx pin, it stops $t_{ERR\_to\_ren}$. If $t_{ERR\_to\_ren}$ expires without detecting an edge, a severe fault is thrown.

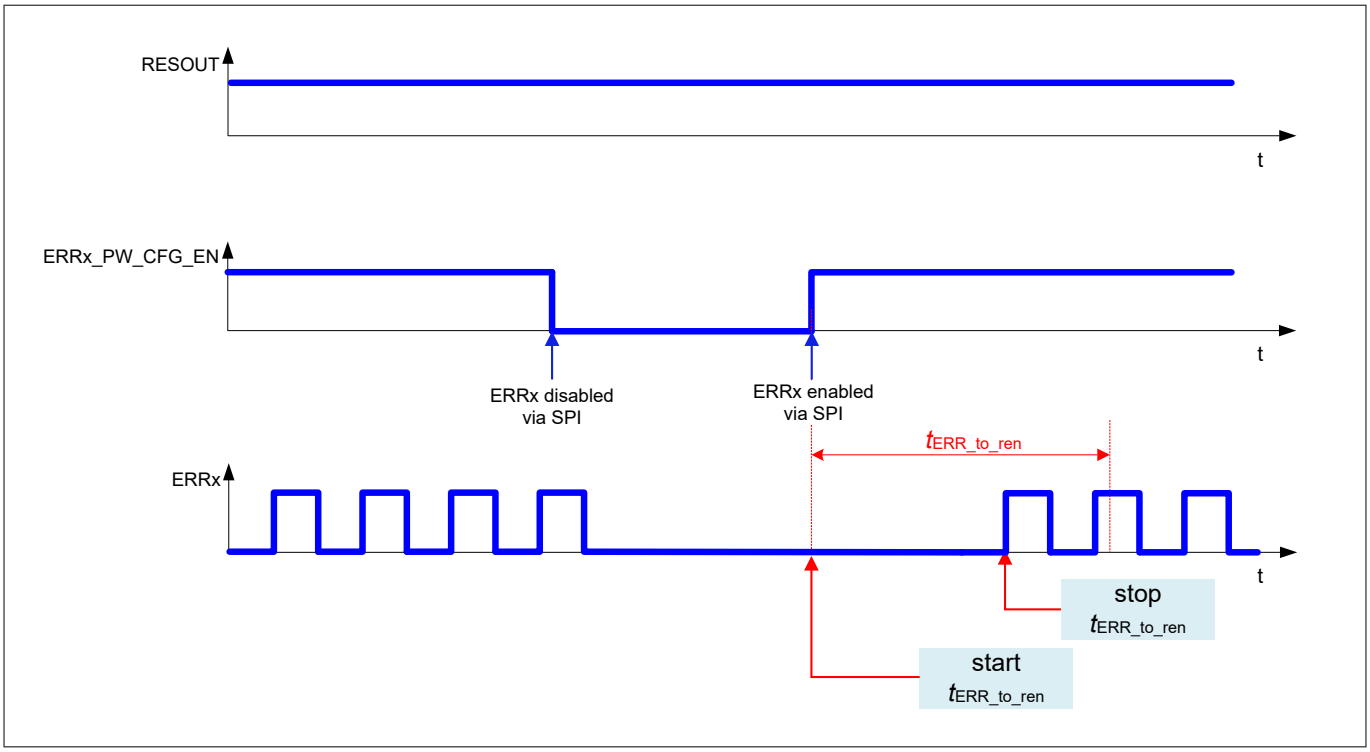


Figure 50 ERRx reactivation timeout

(x = 0; 1; 2)

The error monitoring channels can be enabled and disabled independently from each other by writing the respective **ERRx_PW_CFG.EN** bit. In addition each error monitoring channel can be configured to remain active while being in SLEEP state with the respective bit **ERRx_PW_CFG.SLP_EN**. If the error monitoring has not been configured to remain active while being in SLEEP state and it has already been running before entering SLEEP state, the function will re-enable upon transition into WAKE state and starts the reactivation timeout t_{ERR_to}. This provides an additional time budget to apply an error monitoring signal again or disable the function. If no error monitoring is applied within t_{ERR_to} an ERRx_SEV_FAULT is issued (see Interrupt function (INT) and Reset function (RESOUT)). The ERR timeout is a global timer and is only stopped, if either all ERRx channels are disabled or all enabled ERRx channels are properly serviced within t_{ERR_to}.

***Note**: ERR2 can only be used if REDUCED OPERATION is enabled (**REDOP_RS_CFG1.EN = 1**).*

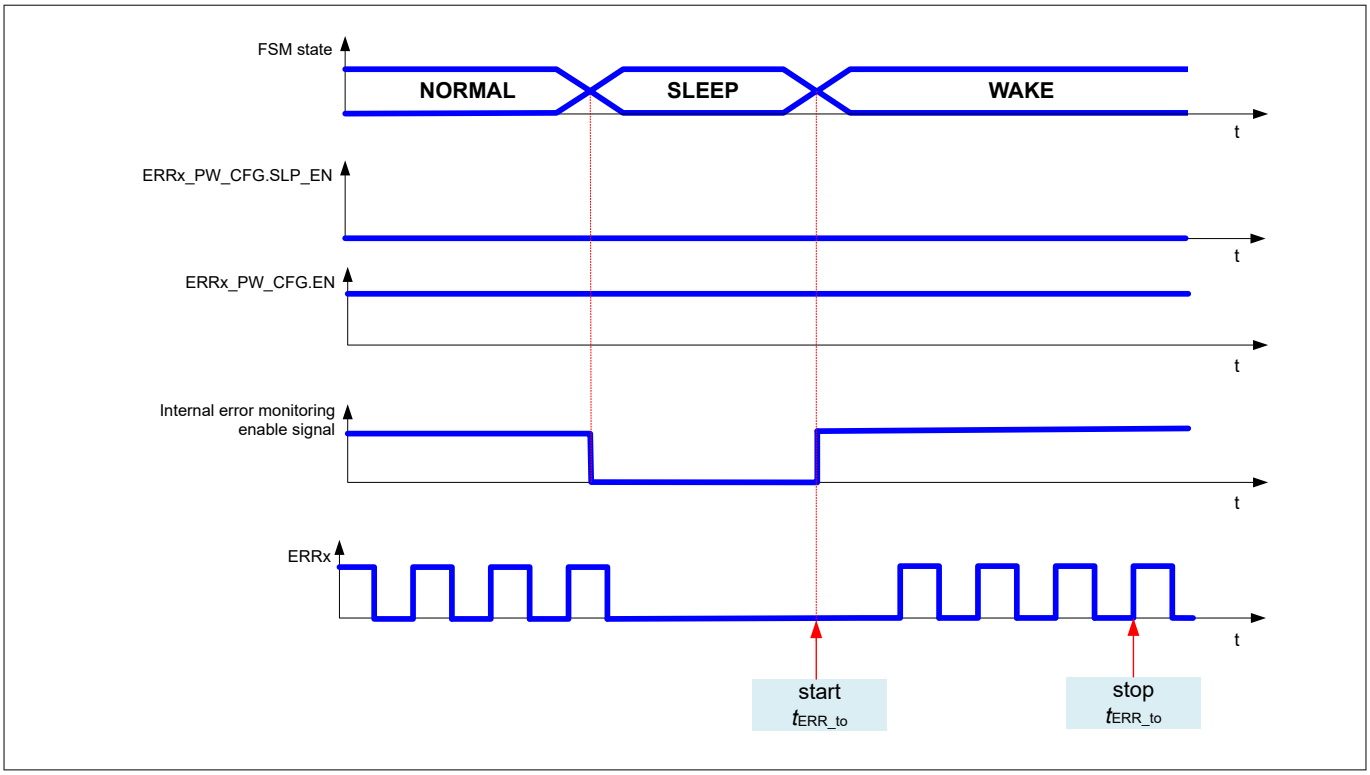


Figure 51 ERRx reactivation timeout from SLEEP state

(x = 0; 1; 2;
y = 1; 2)

10.2.2.3 Error monitoring recovery timers

Each error monitoring channel provides a recovery timer. On detection of an invalid ERRx toggling signal period, the corresponding recovery timer grants the application some time to recover and to resume valid error frequency generation.

The recovery timer of each error monitoring channel can be activated or deactivated independently in the register bit **ERRx_PW_CFG.TREC_EN**.

For an activated recovery timer, the duration of the recovery time t_{REC} can be configured in the bitfield **ERRx_PW_CFG.TREC**.

10.2.2.4 Invalid error toggling

If any of the following conditions is fulfilled, then the device detects "**invalid ERRx toggling**":

- The ERR signal stops toggling and remains "low" or "high"
- The ERR signal starts toggling with a too high frequency ($f_{ERR\_invalid\_high\_x}$)
- The ERR signal starts toggling with a too low frequency ($f_{ERR\_invalid\_low\_x}$)

(x = LF; HF)

Recovery time disabled

On detection of an invalid ERRx triggering, the device performs the following actions:

- Generate an error monitoring severe fault ERRx_SEV_FAULT, see Reaction on faults
- Set the corresponding failure bit (**SYSFAIL_STAT_APPy.ERR0, INIT_ERR_APPy.ERRx**)

Recovery time enabled

On detection of invalid ERRx triggering, the device performs the following actions:

- Generate an error monitoring warning fault ERRx_WARN_FAULT, see Reaction on faults
- Set the corresponding failure bits (**SYS_STAT_APPy.ERRx_ERR)**, which can be cleared via SPI

- Start the recovery timer
- If correct signal has been re-established before t_{REC} has expired, timer is stopped and no further actions take place
- Generate an error monitoring severe fault ERRx_SEV_FAULT after the recovery time t_{REC} has expired and no valid error signal has been re-established in time, see Reaction on faults
- Set the corresponding failure bit (**SYSFAIL_STAT_APPy.ERR0, INIT_ERR_APPy.ERRx**), which can be cleared via SPI

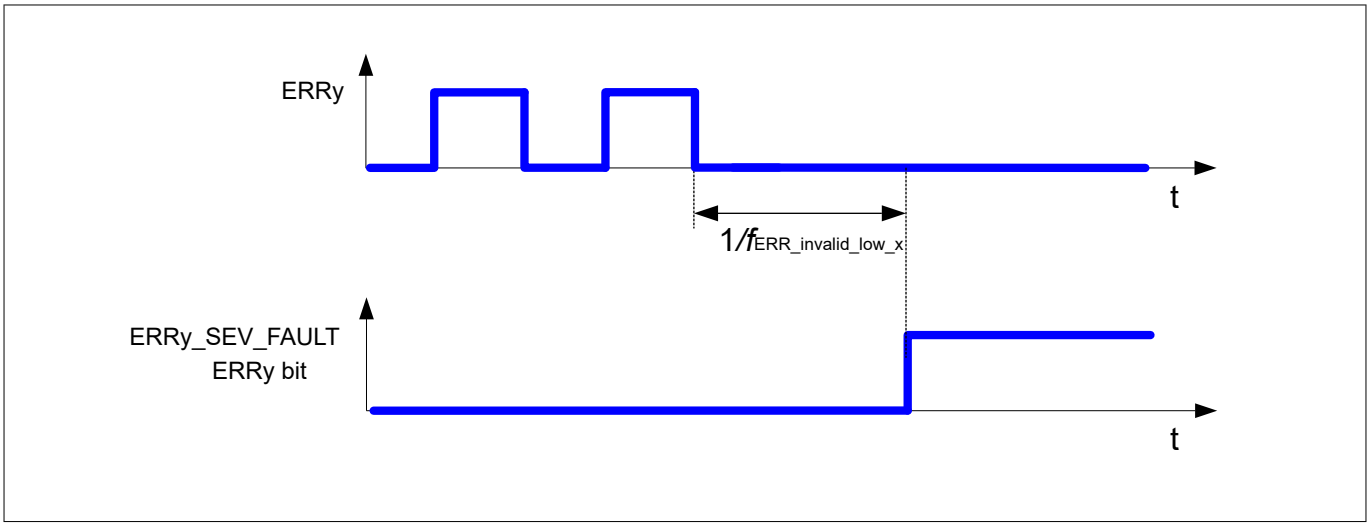


Figure 52 ERRy capture with too low frequency or stops toggling (recovery time disabled)

(x = LF; HF)
(y = 0; 1; 2)

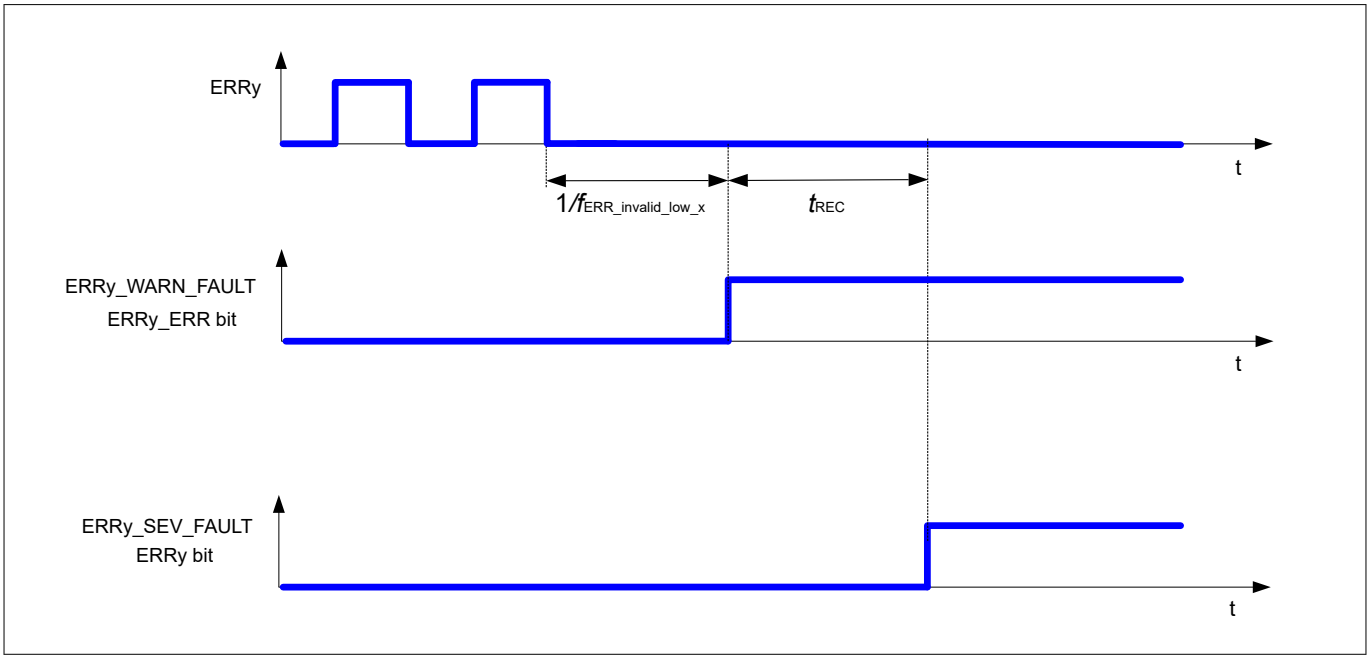


Figure 53 ERRy capture with too low frequency or stops toggling (recovery time enabled)

(x = LF; HF)
(y = 0; 1; 2)

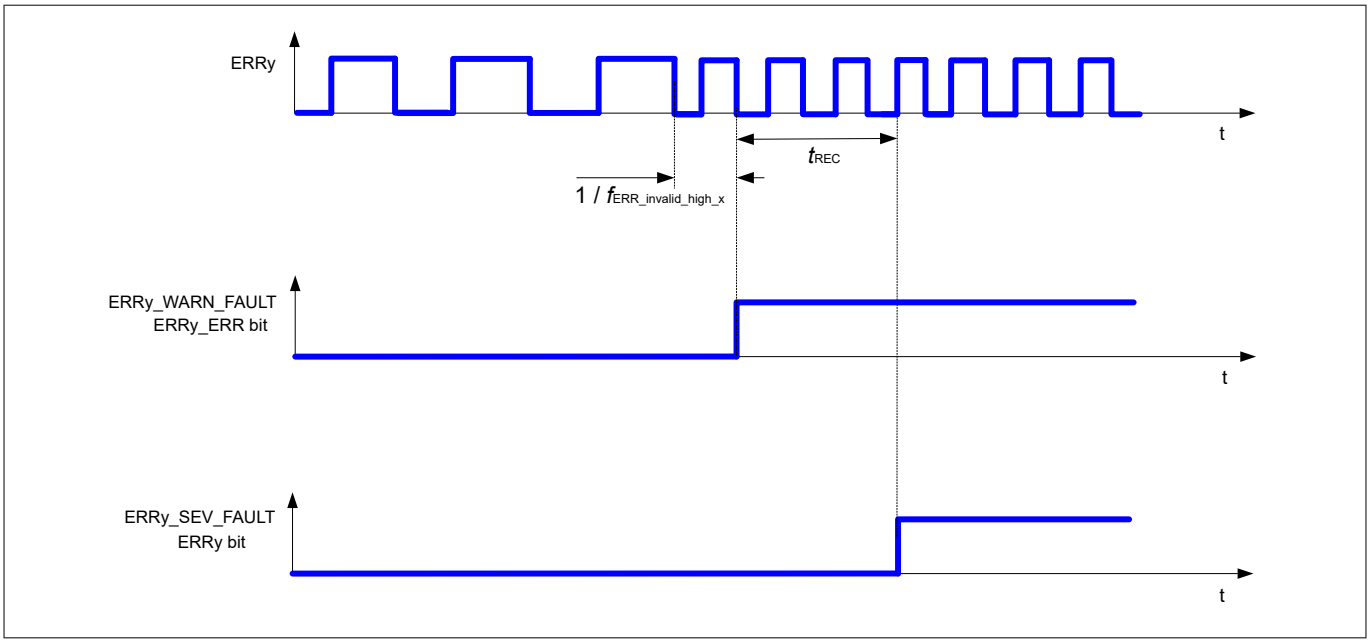


Figure 54 ERRy capture with too high frequency (recovery time enabled)

(x = LF; HF)
(y = 0; 1; 2)

10.2.3 Electrical characteristics error monitoring (ERR MON)

Table 36 Electrical characteristics error monitoring (ERR MON)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ERRx pin valid "high" voltage	V_{ERRx_HIGH}	2	–	V_{QUC}	V	V_{ERRx} increasing; $V_{QUC} \geq V_{QUC}$[Min.]	DS-1624
ERRx pin valid "low" voltage	V_{ERRx_LOW}	0	–	0.8	V	V_{ERRx} decreasing	DS-1625
ERRx pin hysteresis	V_{ERRx_HYST}	–	200	–	mV	$V_{QUC} = V_{QUC}$[Typ.]	DS-1627
ERRx pin pull-down current	I_{ERRx}	–	135	330	µA	$V_{ERRx} = V_{QUC}$	DS-1628
ERRx pin input capacitance	C_{ERRx}	–	4	15	pF	1)	DS-1629
Valid ERRx input signal frequency low	$f_{ERRx\_valid\_LOW}$	10	–	45	kHz	–	DS-1630
Valid ERRx input signal frequency high	$f_{ERRx\_valid\_HIGH}$	1000	–	2000	kHz	–	DS-1631
ERRx invalid input signal - too low frequency LF	$f_{ERR\_invalid\_low\_LF}$	0	–	5	kHz	1)	DS-1632
ERRx invalid input signal - too high frequency LF	$f_{ERR\_invalid\_high\_LF}$	96.2	–	10000	kHz	1)	DS-1633

(table continues...)

Table 36 (continued) Electrical characteristics error monitoring (ERR MON)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ERRx invalid input signal - too low frequency HF	$f_{ERR\_invalid\_low\_HF}$	0	–	0.5	MHz	1)	DS-1634
ERRx invalid input signal - too high frequency HF	$f_{ERR\_invalid\_high\_HF}$	4	–	10	MHz	1)	DS-1635
Reactivation timeout	t_{ERR_to}	9	–	11	ms	After SLEEP with RESOUT=1 and ERRx_RS_CFG.EN=1 and ERRx_RS_CFG.SLP_EN=0 1)	DS-1636
Reactivation timeout after reenabling	$t_{ERR\_to\_ren}$	90	100	110	µs	After reenabling via SPI 1)	DS-1637
ERRx recovery time	t_{REC}	0.9 · t	t	1.1 · t	ms	t configurable to be 1 ms, 2.5 ms, 5 ms, 10 ms; Configuration done via SPI 1)	DS-1998

1) Not subject to production test, specified by design

10.3 Voltage monitoring

10.3.1 Introduction

The voltage monitoring (VMON) function is a safety mechanism that supervises the internal and external supply rails. If the monitoring voltage rail is outside of the defined operational range, then the device reacts accordingly.

The voltage monitoring module provides following voltage monitoring channels:

- The Battery voltage monitoring
- The internal voltage monitoring for each internal regulator or supply rail
- Two external voltage monitoring channels

The voltage monitoring for the corresponding voltage rail is active whenever the regulator is enabled.

Only when a regulator is being ramped up, an undervoltage is ignored until the output voltage is within the monitoring range defined by his undervoltage and overvoltage thresholds.

A short to ground detection remains active while being ramped up.

The device integrates also internal voltage supplies and bias currents necessary to operate all functions, including regulators, monitoring and digital logic. These internal supplies are monitored to ensure proper device functionality.

The following internal supplies are monitored in the device:

- internal supply voltages
- bias currents
- bandgap to bandgap variation

Note: These voltages and current sources are not directly available externally to the device

10.3.2 Battery voltage monitoring

The voltage on Vs pin is monitored to protect the device for unexpected overvoltage.

If the voltage (V_{VS}) on Vs pin exceeds the overvoltage threshold V_{VS_OV}, the device performs the following actions:

- Generate an VBAT monitoring severe fault VBAT_SEV_FAULT, see Chapter 9
- Set the corresponding failure bit INTSUP_STAT_APPx.VBAT_OV, which can be cleared via SPI.

10.3.3 Internal voltage monitoring

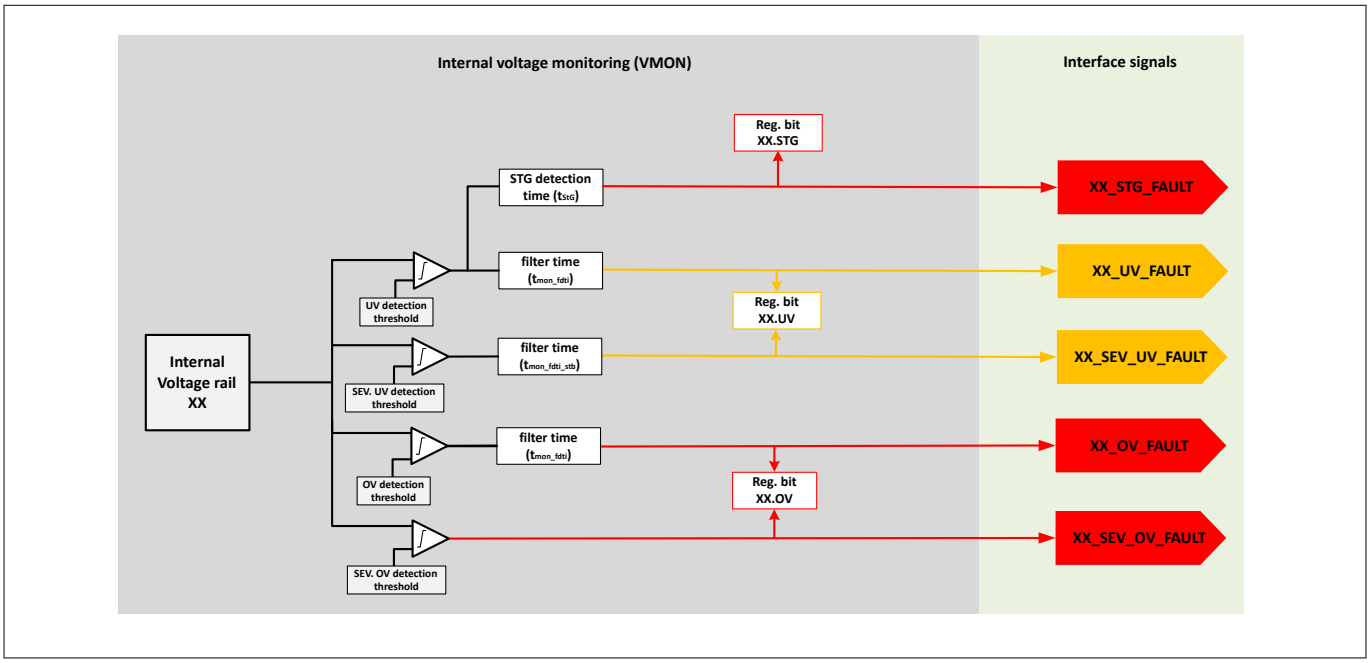


Figure 55 Functional block diagram internal voltage monitoring

The table below shows the corresponding monitoring type for each regulator rail (XX)

Monitoring rail (XX)	severe OV detection	OV detection	UV detection	severe UV Detection	Short to Ground
BUCK PREREG	x	x	x	x (BOOST not used) *	x
BUCKIF	x	x	x		x
BUCKCORE	x	x	x		x
BOOST		x	x	x (BOOST used) *	x
QUC		x	x		x
QCO		x	x		x
QVR		x	x		x
QST	x	x	x		x
QST (STANDBY)	x			x	x
Int. Supply	x	x	x		x
BG12		x	x		

** Severe undervoltage monitoring is performed at BSTFB pin with following cases:*

- *If BOOST is mounted and switched on, it is considered as BOOST severe undervoltage and it is indicated in the SPI bitfield STG_STAT_APPx.BOOST*
- *If BOOST is not mounted or switched off in Sleep state, it is considered as BUCK PREREG severe undervoltage and is indicated in the SPI bitfield STG_STAT_APPx.PREREG*

Overvoltage detection:

If the output voltage of internal supply rail XX exceeds the defined overvoltage threshold V_{XX_OV} for a timer longer than the monitoring reaction time of t_{mon_fdti}, the device performs the following actions:

- Generate an internal overvoltage fault XX_OV_FAULT (see Reaction on detected fault)
- Set the corresponding failure bits (register **OV_STAT_APPx.XX**), which can only be cleared via SPI after the voltage returns to normal operation range.

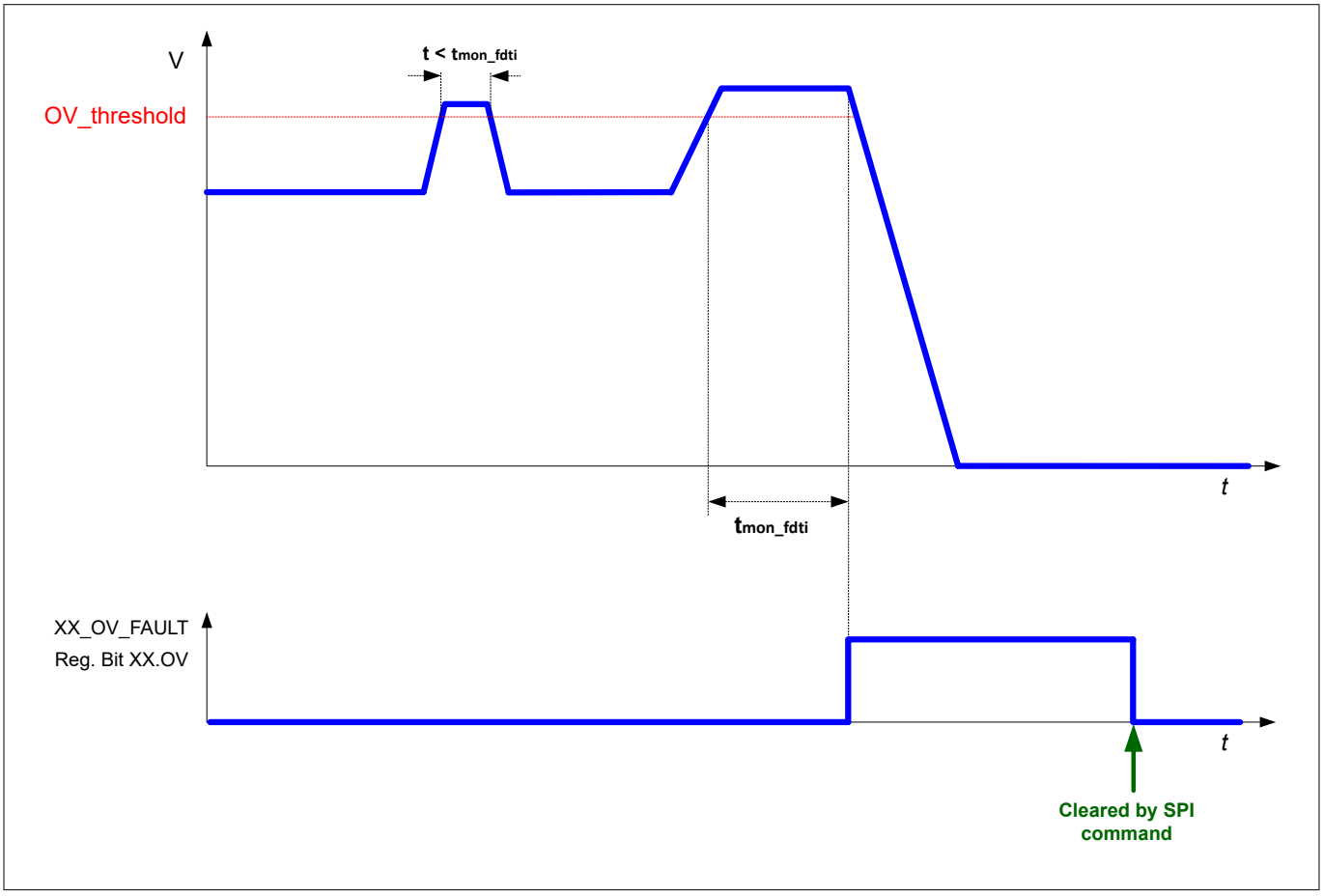


Figure 56 Timing diagram overvoltage detection

Severe overvoltage detection:

If the output voltage of internal supply rail XX rapidly increases and reach the severe overvoltage threshold $V_{XX\_SEV\_OV}$,
the device immediately switches off the correspondent regulator. In general the severe overvoltage reaction is the same as for the overvoltage detection with the difference, that the threshold is set higher compared to the overvoltage and the filter time is not applied.

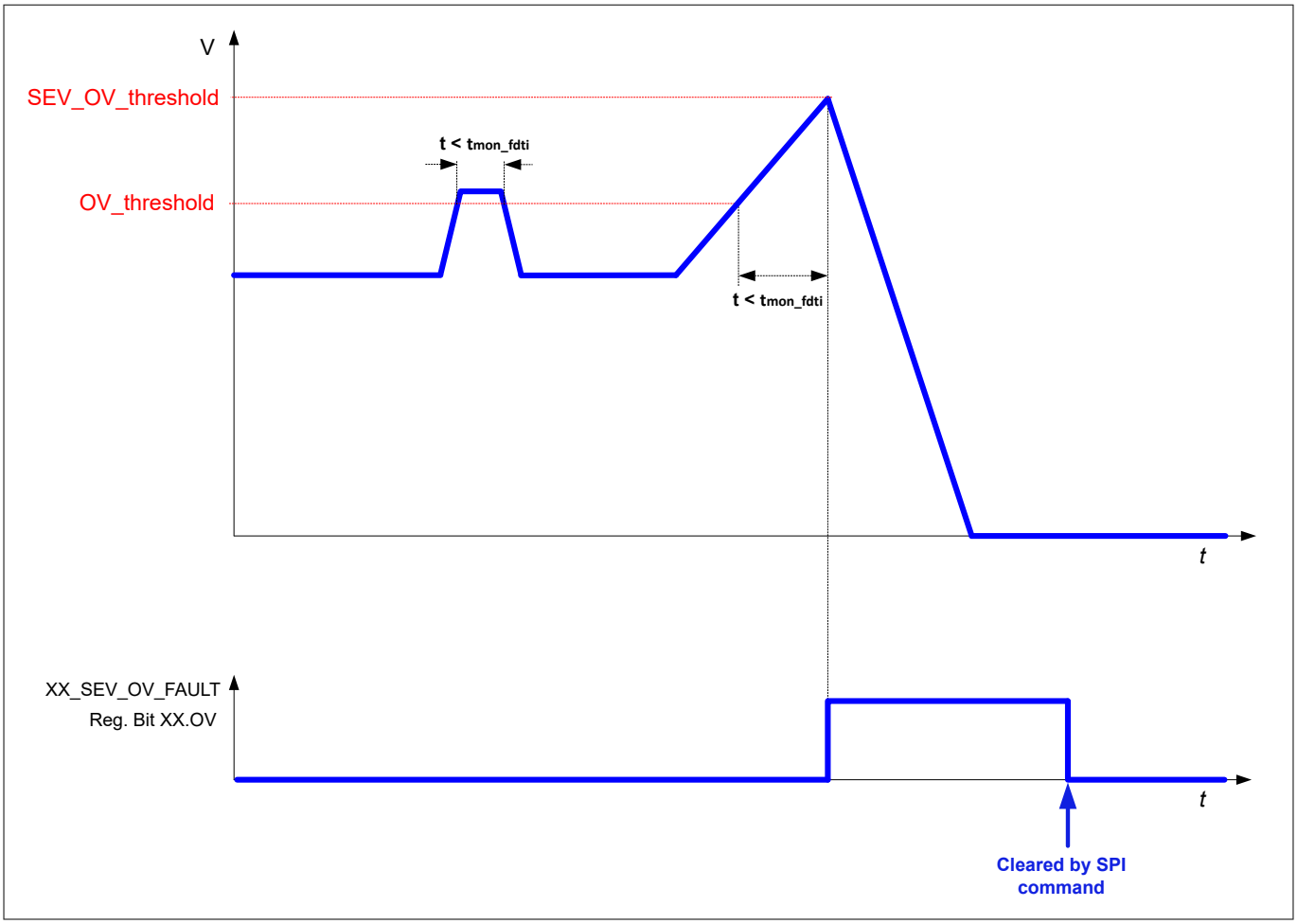


Figure 57 Timing diagram severe overvoltage detection

If the device enters STANDBY state and the output voltage of the standby regulator (QST) drops below the severe undervoltage threshold $V_{QST\_SEV\_UV}$ for a timer longer than the monitoring reaction time in standby $t_{mon\_fdti\_stb}$,
the device performs the following actions:

- Generate an internal undervoltage fault QST_SEV_UV_FAULT (see Reaction on detected fault)
- Set the corresponding failure bits (register **UV_STAT_APPx.XX**), which can only be cleared via SPI after the voltage returns to normal operation range.

Short to Ground detection:

If the output voltage of the internal supply rail XX drops below the defined undervoltage threshold V_{XX_UV} for a timer longer than the short to ground detection time of t_{STG},
the device performs the following actions:

- Generate an internal short to ground fault XX_STG_FAULT, see Chapter 9
- Set the corresponding failure bit (register **STG_STAT_APPx.XX**), which can only be cleared via SPI after the voltage returns to normal operation range.

The device detects a short to ground (StG) on the BOOST regulator switched node, if the voltage at pin V_{BSTI} does not recover above the threshold V_{BSTI_UV} between the switching cycles.

The device detects an short to ground (StG) at pin QST if the voltage V_{QST} drops below the undervoltage threshold V_{QST_UV} for a timer longer than the QST short to ground detection time t_{StG_QST}.

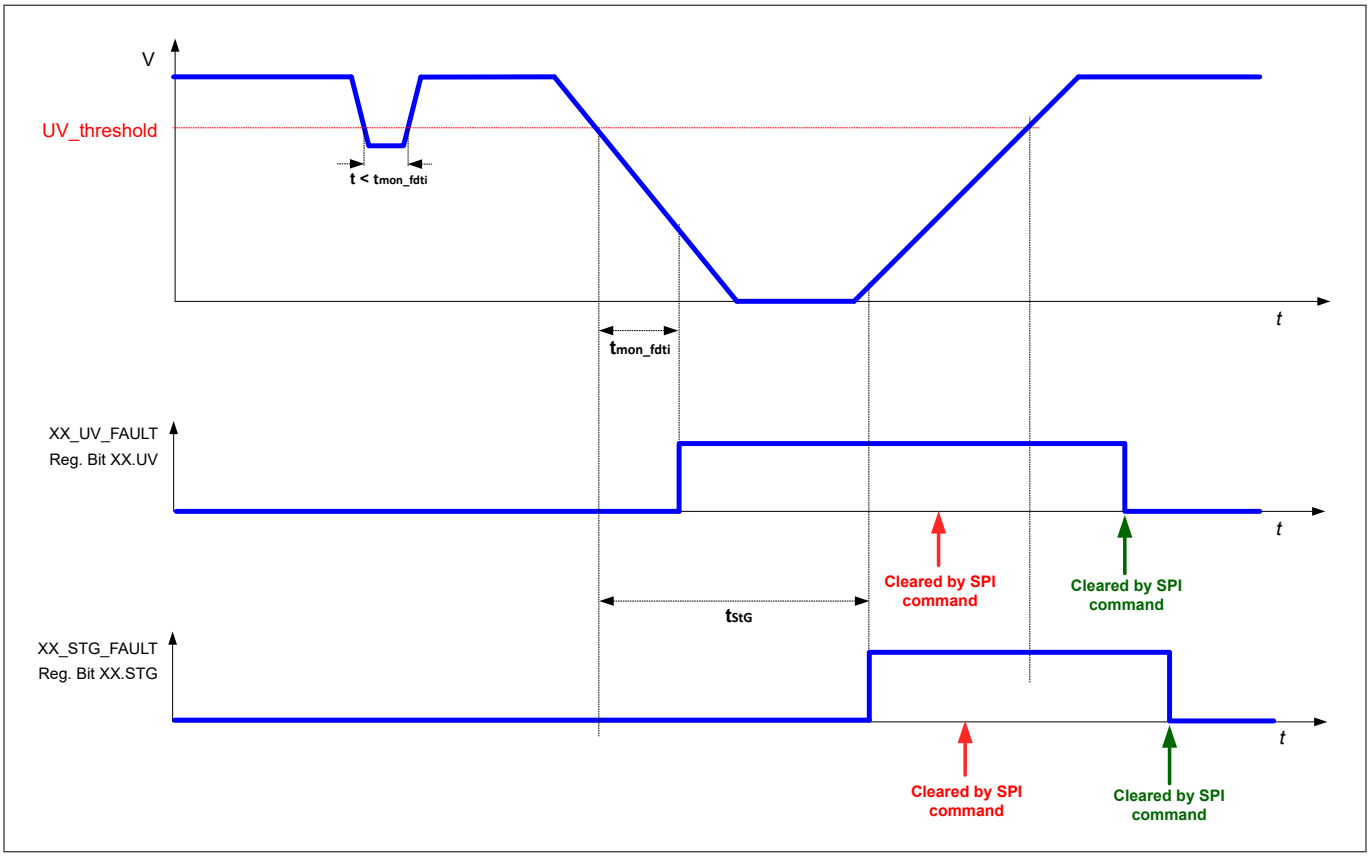


Figure 58 Timing diagram UV and STG detection

10.3.4 Electrical characteristics monitoring functions

Table 37 Electrical characteristics monitoring functions

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Overvoltage monitoring							
Vbat overvoltage shutdown threshold	V_{VS_OV}	49	52	55	V	–	DS-1355
Severe overvoltage threshold Pre-reg	$V_{R1FB\_SEV\_OV}$	6.66	6.8	6.94	V	–	DS-1356
5V5 overvoltage threshold Pre-reg	$V_{R1FB\_5V5\_OV}$	6.15	6.3	6.43	V	–	DS-1357
4V0 overvoltage threshold Pre-reg	$V_{R1FB\_4V0\_OV}$	5.10	5.2	5.3	V	–	DS-1358

(table continues...)

Table 37 (continued) Electrical characteristics monitoring functions

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Severe overvoltage threshold BUCK CORE	$V_{R3FB\_sev\_OV}$	y * 1.19	–	y * 1.56	V	y: Configured nominal BUCKCORE output voltage; y = 0.7 + x*12.5 mV; x: 0,1,...32 (register value); y = 1.15 V for x = 33	DS-2043
Overvoltage threshold BUCK CORE	V_{R3FBH_OV}	y * 1.068	y * 1.09	y * 1.112	V	y: Configured nominal BUCKCORE output voltage; y = 0.7 + x*12.5 mV; x: 0,1,...32 (register value BUCK_CORE_PW_VSEL); y = 1.15 V for x = 33	DS-1359
Overvoltage hysterese BUCK CORE	$V_{R3FBH\_OV\_HYS}$	5	15	25	mV	–	DS-1360
Severe overvoltage threshold BUCK IF	$V_{R4FB\_SEV\_OV}$	4.21	4.3	4.39	V	–	DS-1361
Overvoltage threshold BUCK IF	V_{R4FB_OV}	3.49	3.56	3.63	V	–	DS-1363
Overvoltage threshold BOOST	V_{BSTFB_OV}	6.37	6.5	6.63	V	–	DS-1365
Overvoltage hysteresis BOOST	$V_{BSTFB\_OV\_HYS}$	35	–	115	mV	–	DS-1366
Overvoltage threshold QUC	V_{QUC_OV}	3.49	3.56	3.63	V	–	DS-1369
Overvoltage hysteresis QUC	$V_{QUC\_OV\_HYS}$	20	–	70	mV	–	DS-1370
Overvoltage threshold QCO	V_{QCO_OV}	5.3	5.4	5.5	V	–	DS-1371
Overvoltage hysteresis QCO	$V_{QCO\_OV\_HYS}$	25	–	102	mV	–	DS-2153
Severe overvoltage threshold QST	$V_{QST\_SEV\_OV}$	5.95	6.25	6.5	V	–	DS-1373
Overvoltage threshold QST	V_{QST_OV}	3.49	3.56	3.63	V	–	DS-1375
Overvoltage hysteresis QST	$V_{QST\_OV\_HYS}$	20	–	70	mV	–	DS-1376
Overvoltage threshold QVR	V_{QVR_OV}	5.24	5.35	5.46	V	–	DS-1378
Overvoltage hysterese QVR	$V_{QVR\_OV\_HYS}$	30	–	100	mV	–	DS-1379

(table continues...)

Table 37 (continued) Electrical characteristics monitoring functions

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Undervoltage monitoring							
Undervoltage threshold Pre-reg	V_{R1FB_UV}	2.59	2.65	2.71	V	–	DS-1380
Undervoltage hysteresis Pre-reg	$V_{R1FB\_UV\_HYS}$	15	–	50	mV	–	DS-1381
Undervoltage threshold BUCK CORE	V_{R3FBH_UV}	y * 0.891	y * 0.91	y * 0.929	V	y: Configured nominal BUCKCORE output voltage; y = 0.7 + x*12.5 mV; x: 0,1,...32 (register value BUCK_CORE_PW_VSEL); y = 1.15 V for x = 33	DS-1382
Undervoltage hysterese BUCK CORE	$V_{R3FBH\_UV\_HYS}$	3	15	25	mV	–	DS-1383
Undervoltage threshold BUCK IF	V_{R4FB_UV}	2.9	2.97	3.036	V	–	DS-1385
Undervoltage hysteresis BUCK IF	$V_{R4FB\_UV\_HYS}$	15	–	55	mV	–	DS-1387
Undervoltage threshold BOOST	V_{BSTFB_UV}	4.9	5	5.10	V	–	DS-1388
Severe undervoltage threshold BOOST	$V_{BSTFB\_SEV\_UV}$	1.96	2	2.04	V	If BOOST is not used, it is interpreted as BUCK PREREG severe undervoltage threshold	DS-2161
Undervoltage hysteresis BOOST	$V_{BSTFB\_UV\_HYS}$	30	–	90	mV	–	DS-1389
Boost short to ground threshold	V_{BSTI_UV}	1.84	2.0	2.16	V	V_{BSTI} decreasing	DS-1955
Boost short to ground threshold hysteresis	$V_{BSTI\_UV\_HYS}$	13[1)]	25	37	mV	V_{BSTI} increasing	DS-1956
Undervoltage threshold QCO	V_{QCO_UV}	4.5	4.6	4.7	V	–	DS-1390
Undervoltage hysteresis QCO	$V_{QCO\_UV\_HYS}$	25	–	80	mV	–	DS-1391
Undervoltage threshold QUC	V_{QUC_UV}	2.9	2.97	3.036	V	–	DS-1394

(table continues...)

Table 37 (continued) Electrical characteristics monitoring functions

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Undervoltage hysteresis QUC	$V_{QUC\_UV\_HYS}$	15	–	55	mV	–	DS-1395
Undervoltage threshold QVR	V_{QVR_UV}	4.5	4.6	4.7	V	–	DS-1396
Undervoltage hysterese QVR	$V_{QVR\_UV\_HYS}$	25	–	80	mV	–	DS-1397
Undervoltage threshold QST	V_{QST_UV}	2.83	2.9	2.97	V	–	DS-1399
Undervoltage hysteresis QST	$V_{QST\_UV\_HYS}$	15	–	55	mV	–	DS-1401
Severe undervoltage threshold QST	$V_{QST\_SEV\_UV}$	2.6	2.72	2.78	V	–	DS-2007
Internal Supply undervoltage threshold	$V_{int\_sup\_UV}$	4.4	4.5	4.6	V	V_{QIS} decreasing	DS-1966
Internal Supply overvoltage threshold	$V_{int\_sup\_OV}$	6.37	6.5	6.63	V	V_{QIS} increasing	DS-2008
Voltage monitoring fault detection time	t_{mon_fdti}	6		12	µs	–	DS-2001
Voltage monitoring fault detection time standby	$t_{mon\_fdti\_stb}$	8		50	µs	–	DS-2002

1) Not subject to production test, specified by design

10.3.5 Ext. monitoring channels (VMON)

10.3.5.1 Functional description ext. monitoring channels (VMON)

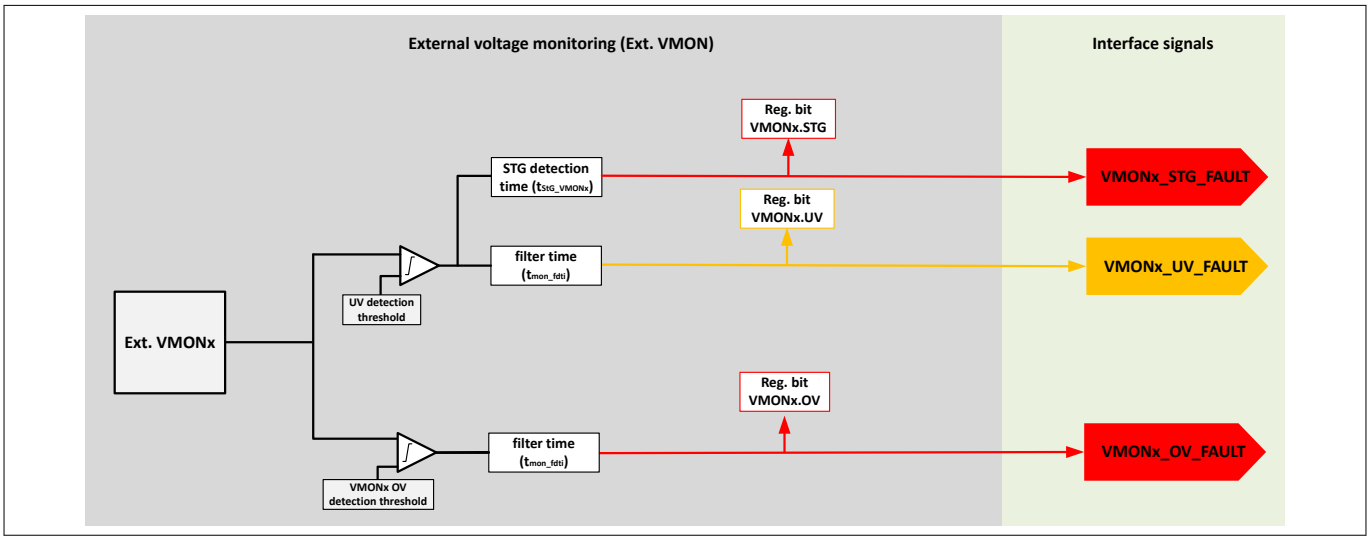


Figure 59 Functional block diagram external voltage monitoring

The device includes two channels (VMON1 or VMON2), each consists of two pins VMxFB and VMxEN. The external voltage rail is compared against a predefined threshold on the pins VM1FB and VM2FB. An external resistor divider must be used to scale the voltage that shall be monitored to the mid point of the monitoring window (typ: 0.8 V). The pins VM1EN and VM2EN are outputs to the corresponding monitoring inputs VM1FB and VM2FB. They provide a high level V_{VMxEN_H} if the automatic use detection during start-up detects the usage of the channel or, after that, if they are disabled and re-enabled via SPI. They can be used to enable and embed an external voltage regulator into the start-up and shut-down sequence of the device.

When a signal exceeds the thresholds for a duration longer than the fault detection time t_{mon_fdti}, an undervoltage or an overvoltage event is generated.

During start-up, the device detects if the external monitoring channels VMON1 or VMON2 are used within the application. If the respective external voltage monitor shall not be used in the application, the pin VMxEN must be connected to ground in order to enable the device to reliably determine whether a voltage monitor is used. For this case VMxFB can be left open. If an external voltage monitoring channel is used, VMxEN must be connected to the external regulator's enable pin. This properly integrates the start-up of the voltage rail into the start-up sequence.

***Note**: VMON1 and VMON2 are excluded from the power sequencing if not used.*

The device detects a short to ground (StG) at one of the external monitoring channels, if the output voltage at pin V_{VMxFB} stays below the undervoltage threshold V_{MONx_UV} for a time longer than the short to ground detection time t_{StG_VMONx}.

The short to ground detection times for each external monitoring channel t_{STG_VMONx} is programmable via SPI register Bitfield **DEV_PW_CFG2.VMONx_STG_TIME**

(x = 1; 2)

10.3.5.2 Electrical characteristics ext. monitoring channels (VMON)

Table 38 Electrical characteristics ext. monitoring channels (VMON)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output voltage high level (x=1 or 2)	V_{VMxEN_H}	2	–	–	V	$V_{QUC} \geq V_{QUC}$[Min]; I_{VMxEN} = -7 mA	DS-1656
Output voltage low level (X = 1 or 2)	V_{VMxEN_L}	–	–	0.7	V	I_{VMxEN} = 5 mA	DS-1657
Short to ground detection time for VMON1	t_{STG_VMON1}	1		6	ms	t_{STG_VMON1} is programmable between 1ms, 2ms, 4ms and 6ms via SPI with a default value of 6ms	DS-1942
accuracy of the short to ground detection time for VMON1	$t_{STG\_VMON1\_acc}$	t_{STG_VMON1} - (10 %*t_{STG_VMON1})	t_{STG_VMON1}	t_{STG_VMON1} + (10 %*t_{STG_VMON1})	ms		DS-1943
Short to ground detection time for VMON2	t_{STG_VMON2}	1		6	ms	t_{STG_VMON2} is programmable between 1 ms, 2 ms, 4 ms and 6 ms via SPI with a default value of 6 ms	DS-1939
Accuracy of the short to ground detection time for VMON2	$t_{STG\_VMON2\_acc}$	t_{STG_VMON2} - (10 %*t_{STG_VMON2})	t_{STG_VMON2}	t_{STG_VMON2} + (10 %*t_{STG_VMON2})	ms		DS-1938
VMON1 overvoltage threshold	$V_{mon\_MON1\_OV}$	858	872	886	mV	V_{VM1FB} increasing	DS-1957
VMON1 overvoltage hysteresis	$V_{mon\_MON1\_OV\_HYS}$	5[1)]		15	mV	V_{VM1FB} decreasing	DS-1958
VMON1 undervoltage threshold	$V_{mon\_MON1\_UV}$	716	728	740	mV	V_{VM1FB} decreasing	DS-1959
VMON1 undervoltage hysteresis	$V_{mon\_MON1\_UV\_HYS}$	5[1)]		15	mV	V_{VM1FB} increasing	DS-1960

(table continues...)

Table 38 (continued) Electrical characteristics ext. monitoring channels (VMON)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
VMON2 overvoltage threshold	$V_{mon\_MON2\_OV}$	858	872	895	mV	V_{VM2FB} increasing	DS-1961
VMON2 overvoltage hysteresis	$V_{mon\_MON2\_OV\_HYS}$	5[1)]		15	mV	V_{VM2FB} decreasing	DS-2009
VMON2 undervoltage threshold	$V_{mon\_MON2\_UV}$	716	728	750	mV	V_{VM2FB} decreasing	DS-2010
VMON2 undervoltage hysteresis	$V_{mon\_MON2\_UV\_HYS}$	5[1)]		15	mV	V_{VM2FB} increasing	DS-2011

1) Not subject to production test, specified by design

10.4 Overcurrent and overtemperature monitoring

10.4.1 Introduction

The overtemperature or overcurrent monitoring function protects the device for transient overtemperature (e.g. load dump or short circuit).

Overtemperature monitoring

The device provides an overtemperature monitoring sensor for the safety area and for all post regulators except the Standby (QST) and the reference (QVR) regulator.

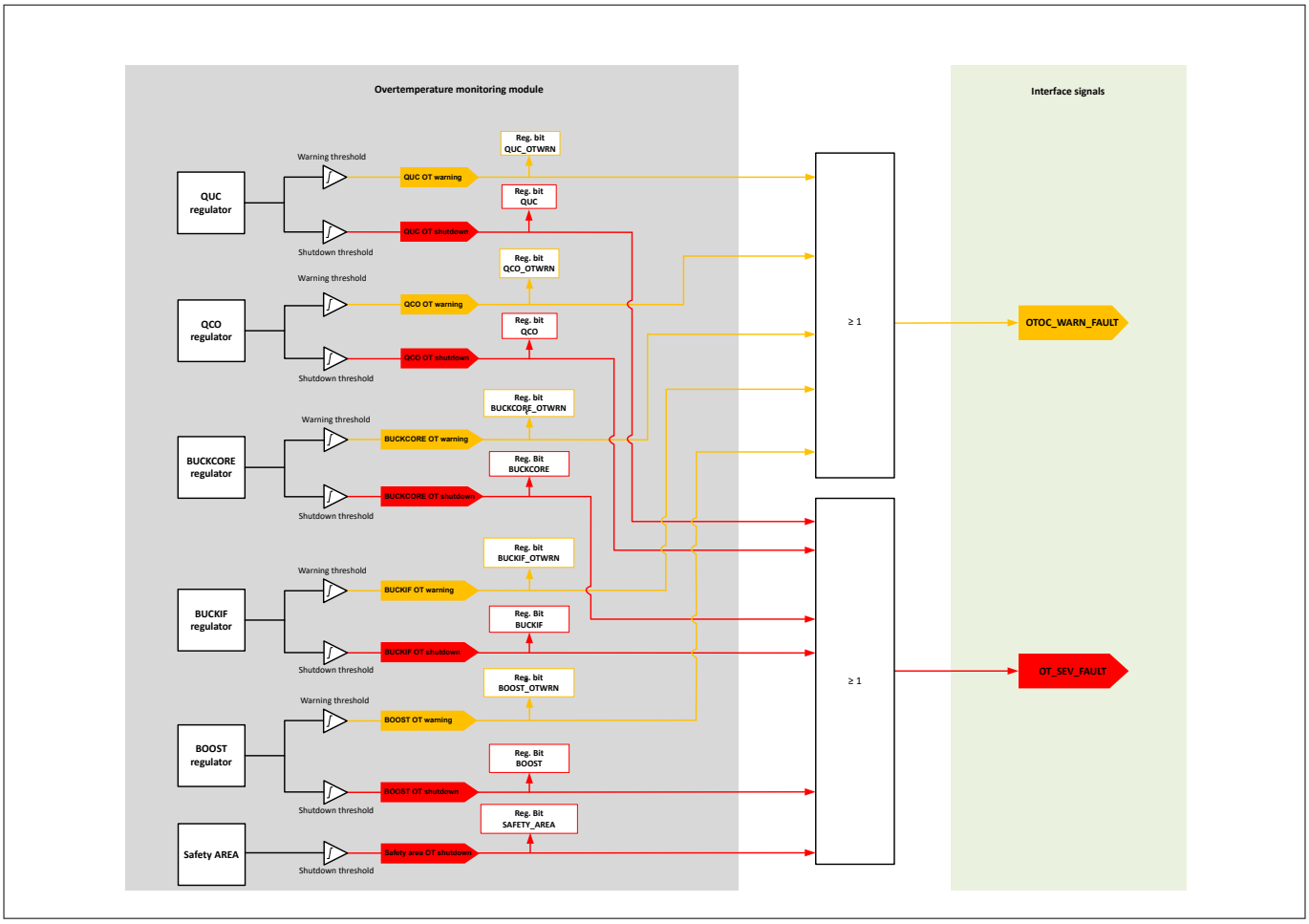


Figure 60 Functional block diagram overtemperature monitoring function

Overcurrent monitoring

The device provides overcurrent monitoring sensors for the boost regulator, the Standby regulator (QST), the internal supply (IVCC) and the reference voltage regulator (QVR).

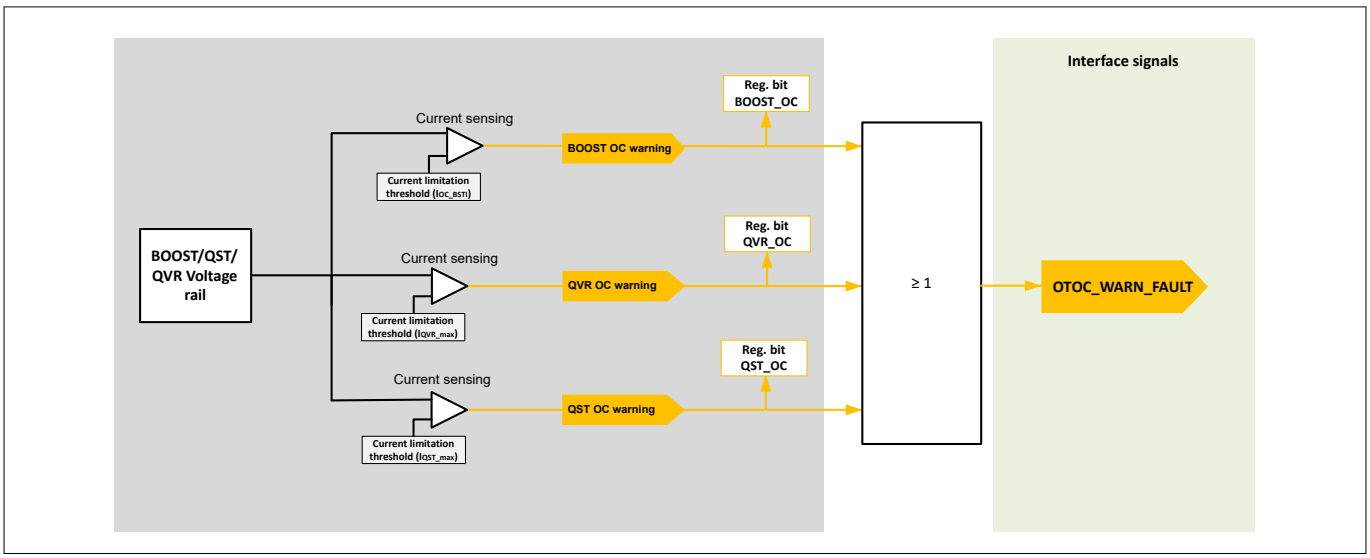


Figure 61 Functional block diagram overcurrent monitoring

10.4.2 Functional description overtemperature monitoring

Two overtemperature detection thresholds are implemented:

Overtemperature warning

If the temperature of the monitoring block exceeds the first threshold (overtemperature warning threshold (t_{PRE})), the device:

- sets the correspondent overtemperature warning bit, which can be cleared via SPI if the temperature drops below the warning threshold
- generates an overtemperature warning fault OTOC_WARN_FAULT, see Chapter 9

Overtemperature shutdown

If the temperature of the monitoring block continues to rise and exceeds the second threshold (overtemperature shutdown threshold (t_{OT})), the device:

- sets the correspondent overtemperature shutdown bit, which can be cleared via SPI if the temperature drops below the shutdown threshold
- generates an overtemperature severe fault OT_SEV_FAULT, see Chapter 9

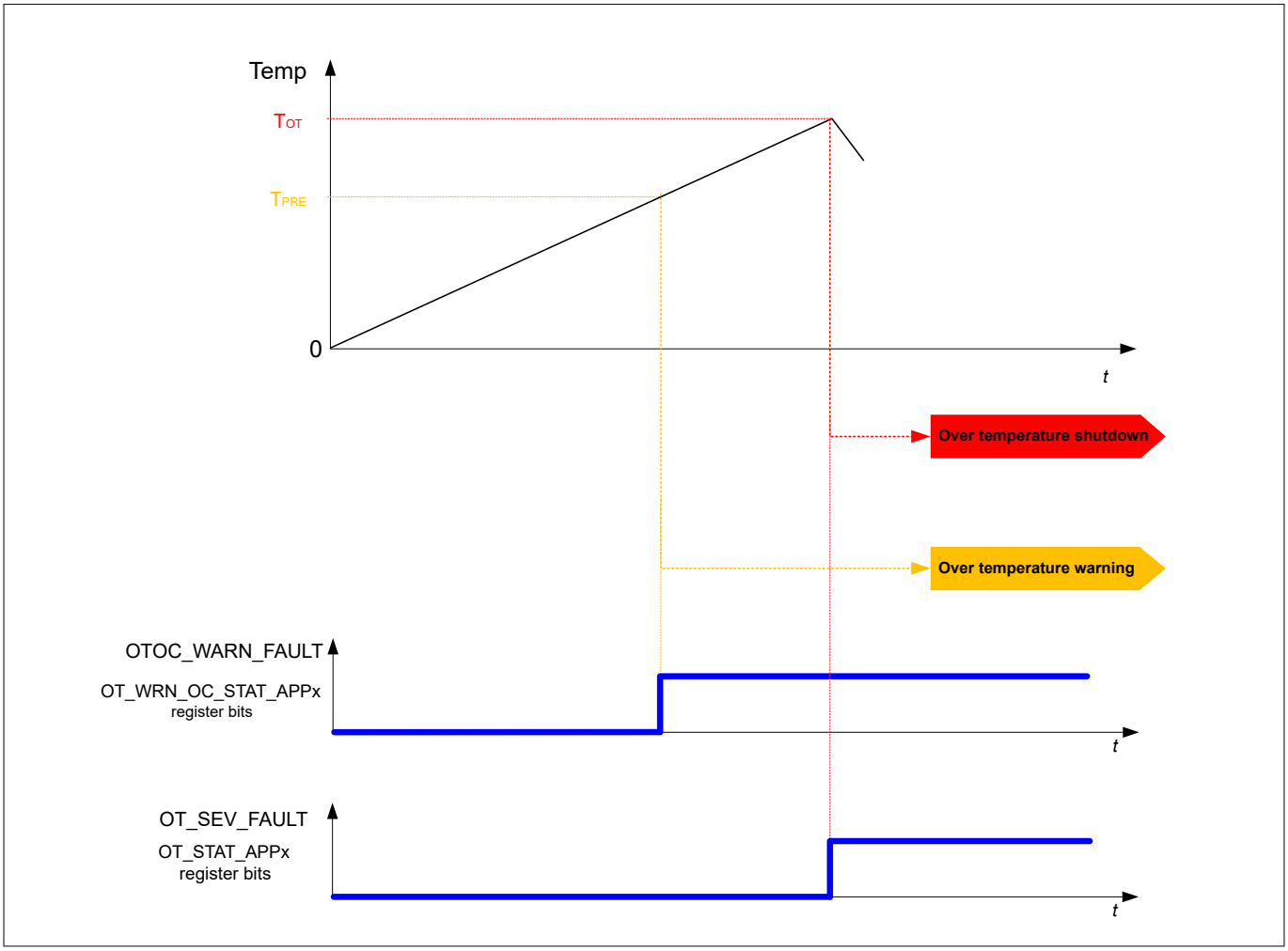


Figure 62 Signal diagram overtemperature monitoring

10.4.3 Functional description current monitoring

If the output current of the monitoring regulator reaches the overcurrent limitation threshold, the device:

- Sets the correspondent overcurrent warning bit, which can be cleared via SPI if the current drops below warning threshold
- Generates an overcurrent warning fault OTOC_WARN_FAULT, see Chapter 9
- The output voltage of the correspondent regulator starts to decrease immediately as consequence

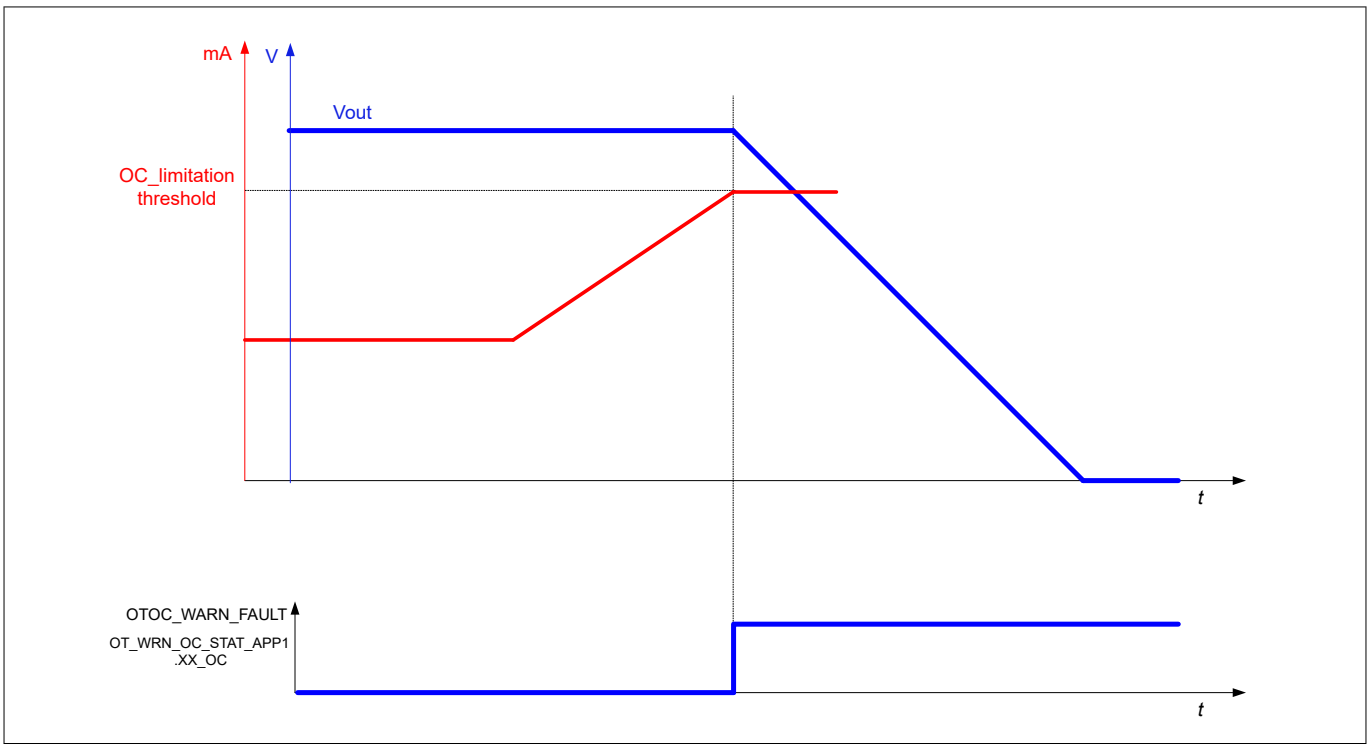


Figure 63 Signal diagram overcurrent monitoring

10.4.4 Electrical characteristics overtemperature monitoring

Table 39 Electrical characteristics overtemperature monitoring

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Overtemperature pre-warning threshold	T_{PRE}	136	146	156	°C	T_j increasing[1)]	DS-1402
Overtemperature threshold	T_{OT}	177	187	197	°C	T_j increasing[1)]	DS-1403

1) Not subject to production test, specified by design

10.5 Safe state control (SSOx)

10.5.1 Introduction

The Safe State Control module monitors the safety related signals and controls the safe state outputs. The following description summarizes the contributors to the Safe State Control function and the possibilities to adjust them.

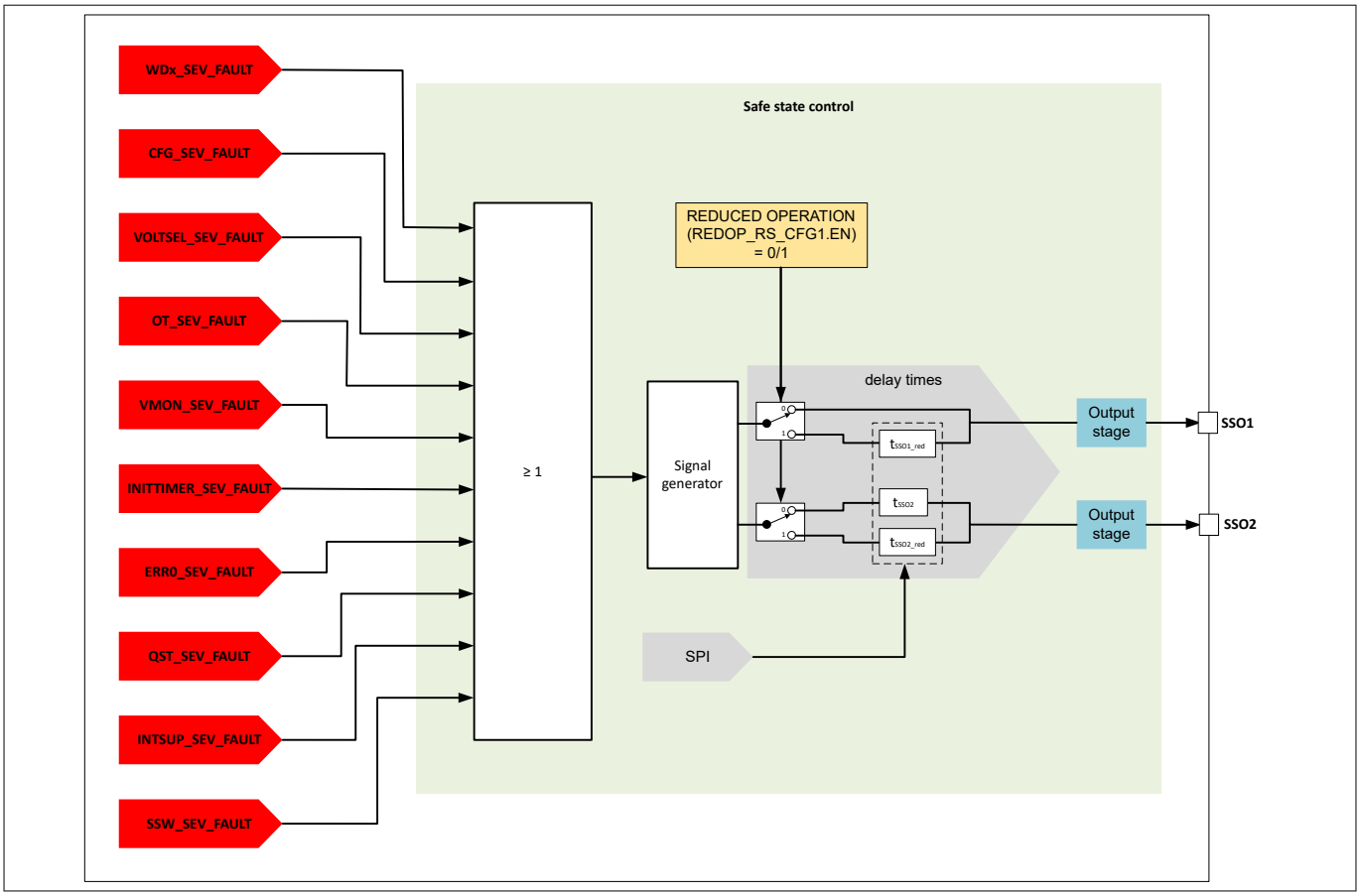


Figure 64 Functional block diagram safe sate control

The safe state control module provides two safe state output control channels:

- The safe state control channel 1 which generates a safe state output signal on pin SSO1
- The safe state control channel 2 which generates a safe state output signal on pin SSO2

The safe state control module is designed to be independent of the device power supply parts by circuitry, signals, and layout.

10.5.2 Functional descriptions shutdown path (SSOx)

The device activates the shutdown path (SSOx output LOW) in any state but NORMAL. Respectively any fault or state transition command that causes the device to leave NORMAL state, results in SSO1 or SSO2 or both to be pulled low, depending on the fault. Also refer to Reaction on detected fault.

10.5.2.1 Delay times and reaction on detected faults

The safe state control is implemented with optional delay time. these functions gives the application the possibility to generate two separate safe state output signals dependent on the application uses cases:

Single application use case:

Single application is activated by setting the register bit **REDOP_PW_CFG1.EN** to 0**.**

After detection of any severe fault, the device sets immediately the output signal on SSO1 pin to "low", while the output signal on SSO2 pin is pulled "low" after a delay time (t_{SSO2}).

The delay time (t_{SSO2}) can be configured in the register bitfield **REDOP_PW_CFG1.SSO1TOSSO2_DEL**.

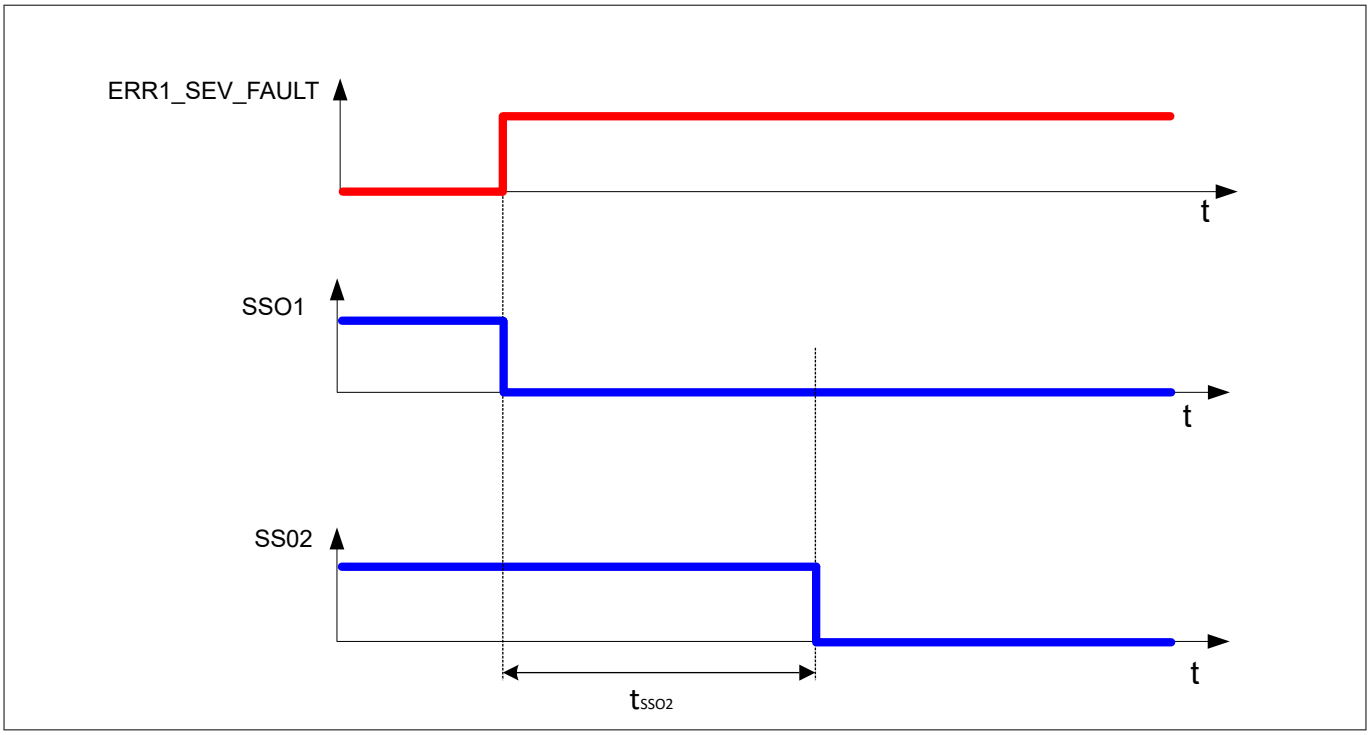


Figure 65 Flow diagram SSOx generation by single application use case, if ERR1 is the error source

(x = 1, 2)

Dual application use case:

Dual application is activated by setting the register bit **REDOP_PW_CFG1.EN** to 1**.**

The device sets the output signal on pin SSO1 or SSO2 "low" upon detection of any severe fault. In case the severe fault is originated in only one of the two applications, the related SSOx pin is set low. This activation can be delayed by configuring the delay times (t_{SSOx_red}) in the register bitfields **REDOP_PW_CFG1.SSOx_DEL**.

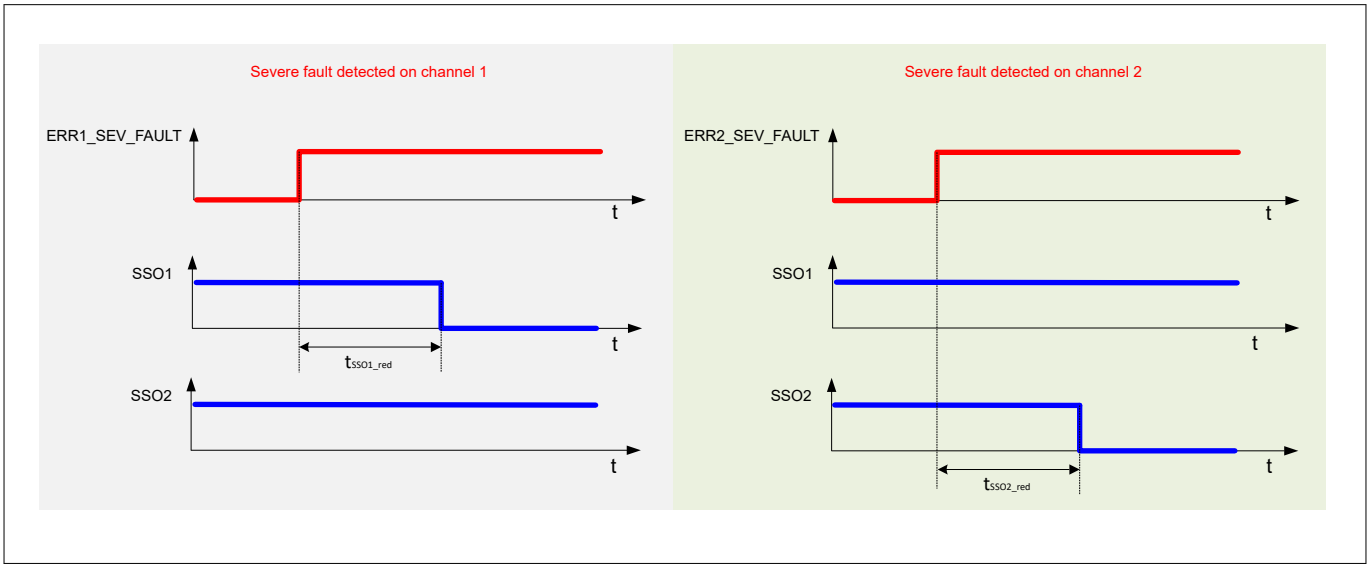


Figure 66 Flow diagram SSOx generation by dual application use case (REDOP_PW_CFG1.EN = 1)

***Note**: The delay time as described in the paragraphs above is only applied for faults that do not have a move to FAILSAFE as state transition. In other words if FAILSAFE is entered the delay times for SSO1/2 are not applied.*

10.5.3 Electrical characteristics shutdown path (SSOx)

Table 40 Electrical characteristics shutdown path (SSOx)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output high level 1 mA	V_{SSOx_HIGH}	2.9	3.2	V_{QUC}	V	I_{SSOx} ≥ -1 mA; V_{QUC} = V_{QUC} [Min]	DS-1613
Output high level 5 mA	V_{SSOx_HIGH}	2.0	2.8	V_{QUC}	V	I_{SSOx} ≥ -5 mA; V_{QUC} = V_{QUC} [Min]	DS-1615
Pull-down resistor	R_{SSOx}	70	100	130	kΩ	–	DS-1616
Output low level	V_{SSOx_LO}	–	0	0.3	V	$R_{SSOx\_PD\_EXT}$ ≤ 100 kΩ; I_{SSOx} <= 1.2 mA; QUC active; V_{QUC} ≥ 2.9 V; -40°C ≤ Tj ≤ 175°C	DS-2081
SSO2 reaction delay time	t_{SSO2}	0	–	250	ms	Timebase accuracy is t_{SSC}	DS-1618
SSO1 reaction delay time for REDUCED OPERATION	t_{SSO1_red}	0	–	250	ms	Timebase accuracy is t_{SSC}	DS-1619
SSO2 reaction delay time for REDUCED OPERATION	t_{SSO2_red}	0	–	250	ms	Timebase accuracy is t_{SSC}	DS-1620
Timebase accuracy	t_{SSC}	-10	-	10	%		DS-1999

10.6 Reaction on faults

10.6.1 Reaction on detected fault

Table 41 Reaction on detected events of regulators

Module	Event description	REDUCED OPERATION ON/OFF	State transition	IO reaction	Register name	Bitfield name
Battery Monitoring	VS OV	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	INTSUP_STAT_APP1	VBAT_OV
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	INTSUP_STAT_APP2	VBAT_OV
BOOST	BOOST OV	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP1	BOOST

(table continues...)

Table 41 (continued) Reaction on detected events of regulators

		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP 2	BOOST
	BOOST overcurrent	off	No transition	INT1	OT_WRN_OC_ STAT_APP1	BOOST_OC
		on	No transition	INT1, INT2	OT_WRN_OC_ STAT_APP1	BOOST_OC
		on	No transition	INT1, INT2	OT_WRN_OC_ STAT_APP2	BOOST_OC
	BOOST overtemperature warning	off	No transition	INT1	OT_WRN_OC_ STAT_APP1	BOOST_OT WRN
		on	No transition	INT1, INT2	OT_WRN_OC_ STAT_APP1	BOOST_OT WRN
		on	No transition	INT1, INT2	OT_WRN_OC_ STAT_APP2	BOOST_OT WRN
	BOOST short to ground or Severe undervoltage or undervoltage at BSTI pin	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	STG_STAT_AP P1	BOOST
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	STG_STAT_AP P2	BOOST
	BOOST thermal shutdown	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OT_STAT_APP 1	BOOST
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OT_STAT_APP 2	BOOST
	Undervoltage at BOOST	off	No transition	INT1	UV_STAT_APP 1	BOOST
		on	No transition	INT1, INT2	UV_STAT_APP 1	BOOST
		on	No transition	INT1, INT2	UV_STAT_APP 2	BOOST
BUCKCORE	BUCKCORE overtemperature warning	off	No transition	INT1	OT_WRN_OC_ STAT_APP1	BUCKCORE_ OTWRN
		on	No transition	INT1, INT2	OT_WRN_OC_ STAT_APP1	BUCKCORE_ OTWRN
		on	No transition	INT1, INT2	OT_WRN_OC_ STAT_APP2	BUCKCORE_ OTWRN
	BUCKCORE short to ground	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	STG_STAT_AP P1	BUCKCORE
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	STG_STAT_AP P2	BUCKCORE

(table continues...)

Table 41 (continued) Reaction on detected events of regulators

	BUCKCORE thermal shutdown	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OT_STAT_APP 1	BUCKCORE
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OT_STAT_APP 2	BUCKCORE
	BUCKCORE undervoltage	any	Move to INIT	RESOUT, SSO1, SSO2	UV_STAT_APP 1	BUCKCORE
		on	Move to INIT	RESOUT, SSO1, SSO2	UV_STAT_APP 1	BUCKCORE
	Feedback open	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP 1	BUCKCORE_FB_OPEN
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP 2	BUCKCORE_FB_OPEN
	Severe overvoltage at BUCKCORE or BUCKCORE OV	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP 1	BUCKCORE
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP 2	BUCKCORE
	Static voltage scaling completed successfully.	off	No transition	INT1	SYS_STAT_APP1	BUCKCORE_SVS_OK
		on	No transition	INT1, INT2	SYS_STAT_APP1	BUCKCORE_SVS_OK
		on	No transition	INT1, INT2	SYS_STAT_APP2	BUCKCORE_SVS_OK
	Static voltage scaling not performed due to: - Device being not in INIT or NORMAL - BUCKCORE voltage set to 1.15 V - Invalid SPI value	off	No transition	INT1	SYS_STAT_APP1	BUCKCORE_SVS_NOK
		on	No transition	INT1, INT2	SYS_STAT_APP1	BUCKCORE_SVS_NOK
		on	No transition	INT1, INT2	SYS_STAT_APP2	SBUCKCORE_SVS_NOK
	Voltage selection error. Core voltage might be corrupt.	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP1	BUCK_CORE_VOLTSEL
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP2	BUCK_CORE_VOLTSEL
BUCKIF	BUCKIF overtemperature warning	off	No transition	INT1	OT_WRN_OC_STAT_APP1	BUCKIF_OTWRN
		on	No transition	INT1, INT2	OT_WRN_OC_STAT_APP1	BUCKIF_OTWRN

(table continues...)

Table 41 (continued) Reaction on detected events of regulators

		on	No transition	INT1, INT2	OT_WRN_OC_STAT_APP2	BUCKIF_OTWRN
	BUCKIF thermal shutdown	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OT_STAT_APP1	BUCKIF
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OT_STAT_APP2	BUCKIF
	Severe overvoltage at BUCKIF or BUCKIF OV	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP1	BUCKIF
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP2	BUCKIF
	Undervoltage at BUCKIF	off	No transition	INT1	UV_STAT_APP1	BUCKIF
		on	No transition	INT1, INT2	UV_STAT_APP1	BUCKIF
		on	No transition	INT1, INT2	UV_STAT_APP2	BUCKIF
	Voltage selection error. 1.8 or 3.3 V might be corrupt and not correctly selected.	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP1	BUCKIF_VOLTSEL
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP2	BUCKIF_VOLTSEL
	Short to ground at BUCKIF	off	No transition	INT1	STG_STAT_APP1	BUCKIF
		on	No transition	INT1, INT2	STG_STAT_APP1	BUCKIF
		on	No transition	INT1, INT2	STG_STAT_APP2	BUCKIF
PREREG	PREREG short to ground	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	STG_STAT_APP1	PREREG
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	STG_STAT_APP2	PREREG
	Severe overvoltage at PREREG & PREREG OV	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP1	PREREG
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP2	PREREG
	Undervoltage at PREREG	off	No transition	INT1	UV_STAT_APP1	PREREG
		on	No transition	INT1, INT2	UV_STAT_APP1	PREREG
		on	No transition	INT1, INT2	UV_STAT_APP2	PREREG

(table continues...)

Table 41 (continued) Reaction on detected events of regulators

QCO	QCO OV	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP 1	QCO
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP 2	QCO
	QCO overtemperature warning	off	No transition	INT1	OT_WRN_OC_ STAT_APP1	QCO_OTWR N
		on	No transition	INT1, INT2	OT_WRN_OC_ STAT_APP1	QCO_OTWR N
		on	No transition	INT1, INT2	OT_WRN_OC_ STAT_APP2	QCO_OTWR N
	QCO thermal shutdown	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OT_STAT_APP 1	QCO
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OT_STAT_APP 2	QCO
	Undervoltage at QCO	off	No transition	INT1	UV_STAT_APP 1	QCO
		on	No transition	INT1, INT2	UV_STAT_APP 1	QCO
		on	No transition	INT1, INT2	UV_STAT_APP 2	QCO
	Short to ground at QCO	off	No transition	INT1	STG_STAT_AP P1	QCO
		on	No transition	INT1, INT2	STG_STAT_AP P1	QCO
		on	No transition	INT1, INT2	STG_STAT_AP P2	QCO
QST	QST OV	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP 1	QST
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP 2	QST
	QST overcurrent	off	No transition	INT1	OT_WRN_OC_ STAT_APP1	QST_OC
		on	No transition	INT1, INT2	OT_WRN_OC_ STAT_APP1	QST_OC
		on	No transition	INT1, INT2	OT_WRN_OC_ STAT_APP2	QST_OC
	QST undervoltage or Severe undervoltage	any	Move to INIT	RESOUT, SSO1, SSO2	UV_STAT_APP 1	QST
		on	Move to INIT	RESOUT, SSO1, SSO2	UV_STAT_APP 1	QST

(table continues...)

Table 41 (continued) Reaction on detected events of regulators

	QST short to ground	on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	STG_STAT_APP2	QST
	QST BIST errors, severe overvoltage	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP1	QST
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP2	QST
	QST short to ground	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	STG_STAT_APP1	QST
QST/QUC	Voltage selection error. 5 V or 3.3 V might be corrupt and not correctly selected.	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP1	QST_QUC_VOLTSEL
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP2	QST_QUC_VOLTSEL
QUC	QUC OV	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP1	QUC
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP2	QUC
	QUC overtemperature warning	off	No transition	INT1	OT_WRN_OC_STAT_APP1	QUC_OTWRN
		on	No transition	INT1, INT2	OT_WRN_OC_STAT_APP1	QUC_OTWRN
		on	No transition	INT1, INT2	OT_WRN_OC_STAT_APP2	QUC_OTWRN
	QUC short to ground	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	STG_STAT_APP1	QUC
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	STG_STAT_APP2	QUC
	QUC thermal shutdown	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OT_STAT_APP1	QUC
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OT_STAT_APP2	QUC
	QUC undervoltage	any	Move to INIT	RESOUT, SSO1, SSO2	UV_STAT_APP1	QUC
		on	Move to INIT	RESOUT, SSO1, SSO2	UV_STAT_APP1	QUC
QVR	QVR OV	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP1	QVR
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP2	QVR
	QVR overcurrent	off	No transition	INT1	OT_WRN_OC_STAT_APP1	QVR_OC

(table continues...)

Table 41 (continued) Reaction on detected events of regulators

		on	No transition	INT1, INT2	OT_WRN_OC_STAT_APP1	QVR_OC
		on	No transition	INT1, INT2	OT_WRN_OC_STAT_APP2	QVR_OC
	Undervoltage at QVR	off	No transition	INT1	UV_STAT_APP 1	QVRUV
		on	No transition	INT1, INT2	UV_STAT_APP 1	QVRUV
		on	No transition	INT1, INT2	UV_STAT_APP 2	QVR
	QVR short to ground	off	No transition	INT1	STG_STAT_APP1	QVR
		on	No transition	INT1, INT2	STG_STAT_APP1	QVR
		on	No transition	INT1, INT2	STG_STAT_APP2	QVR
VMON1	Undervoltage at VMON1	off	No transition	INT1	UV_STAT_APP 1	VMON1
		on	No transition	INT1, INT2	UV_STAT_APP 1	VMON1
		on	No transition	INT1, INT2	UV_STAT_APP 2	VMON1
	VMON1 OV	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP 1	VMON1
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP 2	VMON1
	Short to ground at VMON1	off	No transition	INT1	STG_STAT_APP1	VMON1
		on	No transition	INT1, INT2	STG_STAT_APP1	VMON1
		on	No transition	INT1, INT2	STG_STAT_APP2	VMON1
VMON2	Undervoltage at VMON2	off	No transition	INT1	UV_STAT_APP 1	VMON2
		on	No transition	INT1, INT2	UV_STAT_APP 1	VMON2
		on	No transition	INT1, INT2	UV_STAT_APP 2	VMON2
	VMON2 OV	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP 1	VMON2

(table continues...)

Table 41 (continued) Reaction on detected events of regulators

		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP2	VMON2
	Short to ground at VMON2	off	No transition	INT1	STG_STAT_APP1	VMON2
		on	No transition	INT1, INT2	STG_STAT_APP1	VMON2
		on	No transition	INT1, INT2	STG_STAT_APP2	VMON2

1) Only for move to INIT

2) Due to move to FAILSAFE also INTx will go low (QUC switched off in FAILSAFE)

(x = 1; 2)

Table 42 Reaction on detected events of the system

Module	Event description	REDUCED OPERATION ON/OFF	State transition	IO reaction	Register name	Bitfield name
SSW	Major error detected during SSW BIST or SSW was activated during normal operation	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP1	PREREG_COSW
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP2	PREREG_COSW
ENA	ENA signal detected (only when waking up form FAILSAFE, STANDBY or SLEEP)	on	Move into WAKE if device is in SLEEP or within the transition into this state. Else no transition takes place.	INT1[3)], INT2[3)]	WAKE_STAT_APP1	ENA
		on	Move into WAKE if device is in SLEEP or within the transition into this state. Else no transition takes place.	INT1[3)], INT2[3)]	WAKE_STAT_APP2	ENA

(table continues...)

Table 42 (continued) Reaction on detected events of the system

		off	Move into WAKE or INIT if device is in STANDBY or SLEEP or within the transition into those states. Else no transition takes place.	INT1[3)]	WAKE_STAT_APP1	ENA
WAK	WAK signal detected (only when waking up form FAILSAFE, STANDBY or SLEEP)	on	Move into WAKE if device is in SLEEP or within the transition into this state. Else no transition takes place.	INT1[3)], INT2[3)]	WAKE_STAT_APP2	WAK
		on	Move into WAKE if device is in SLEEP or within the transition into this state. Else no transition takes place.	INT1[3)], INT2[3)]	WAKE_STAT_APP1	WAK
		off	Move into WAKE or INIT if device is in STANDBY or SLEEP or within the transition into those states. Else no transition takes place.	INT1[3)]	WAKE_STAT_APP1	WAK
WUT	Wake-up timer (WUT) expired and woke up the device (only when waking up form STANDBY or SLEEP)	on	Move into WAKE if device is in SLEEP. Else no transition takes place.	INT2	WAKE_STAT_APP2	WUT
		on	Move into WAKE if device is in SLEEP. Else no transition takes place.	INT1, INT2	WAKE_STAT_APP1	WUT

(table continues...)

Table 42 (continued) Reaction on detected events of the system

		off	Move into WAKE or INIT if device is in STANDBY or SLEEP. Else no transition takes place.	INT1	WAKE_STAT_APP1	WUT
ERR0	ERR0 monitoring error AND ERR0 recovery is enabled	on	No transition	INT1, INT2	SYS_STAT_APP2	ERR0_ERR
		on	No transition	INT1, INT2	SYS_STAT_APP1	ERR0_ERR
		off	No transition	INT1	SYS_STAT_APP1	ERR0_ERR
	FAILSAFE was entered after ERR0 reported invalid frequency (No recovery enabled or recovery expired)	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP1	ERR0
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP2	ERR0
ERR1	ERR1 monitoring error AND ERR1 recovery is enabled (less than t_{REC})	any	No transition	INT1	SYS_STAT_APP1	ERR1_ERR
	ERR1 signal is outside of of valid frequencies (if recovery enabled: longer than t_{REC} before being set)	off	Move to INIT	RESOUT, SSO1, SSO2	INIT_ERR_APP1	ERR1
		on	Move to REDUCED OPERATION	INT2[4)]	INIT_ERR_APP2	ERR1
		on	Move to REDUCED OPERATION	INT1[6)], SSO1	INIT_ERR_APP1	ERR1
ERR2	ERR2 monitoring error AND ERR2 recovery is enabled (less than t_{REC})	on	No transition	INT2	SYS_STAT_APP2	ERR2_ERR
	ERR2 signal is outside of valid frequencies (if recovery enabled: longer than t_{REC} before being set)	on	Move to REDUCED OPERATION	INT2[6)], SSO2	INIT_ERR_APP2	ERR2
		on	Move to REDUCED OPERATION	INT1[4)]	INIT_ERR_APP1	ERR2

(table continues...)

Table 42 (continued) Reaction on detected events of the system

FSM	FAILSAFE was entered because INIT timer expired a 3rd time in a row without successful initialization.	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP1	FSM_INITTIMER
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP2	FSM_INITTIMER
	INIT timer expires 1st time Soft reset issued	off/on	Move to INIT	RESOUT, SSO1, SSO2	INIT_ERR_APP1	SOFTRES
		on	Move to INIT	RESOUT, SSO1, SSO2	INIT_ERR_APP2	SOFTRES
	INIT timer expires 2nd time in a row Hard reset issued	off/on	Move to INIT	RESOUT, SSO1, SSO2	INIT_ERR_APP1	HARDRES
		on	Move to INIT	RESOUT, SSO1, SSO2	INIT_ERR_APP2	HARDRES
	State transition into low power state (STANDBY or SLEEP) failed/ interrupted (e.g. by WAK or ENA)	off	Move into WAKE or INIT (depending on the transition)	INT1, RESOUT[1)], SSO1, SSO2	SYS_STAT_APP1	FSM_TRFAIL
	State transition into low power state (STANDBY or SLEEP) failed/ interrupted (e.g. by WAK or ENA)	on	Move into WAKE or INIT (depending on the transition)	INT1, INT2, RESOUT[1)], SSO1, SSO2	SYS_STAT_APP1	FSM_TRFAIL
		on	Move into WAKE or INIT (depending on the transition)	INT1, INT2, RESOUT[1)], SSO1, SSO2	SYS_STAT_APP2	FSM_TRFAIL
	State transition not existing or transition conditions not fulfilled.	off	No transition	INT1	SYS_STAT_APP1	FSM_NOOP
		on	No transition	INT1, INT2	SYS_STAT_APP1	FSM_NOOP
		on	No transition	INT1, INT2	SYS_STAT_APP2	FSM_NOOP
WWD1	WWD1 incorrectly triggered and error counter reaches or exceeds threshold	off	Move to INIT	RESOUT, SSO1, SSO2	INIT_ERR_APP1	WWD1_EC
		on	Move to REDUCED OPERATION	INT2[4)]	INIT_ERR_APP2	WWD1_EC
		on	Move to REDUCED OPERATION	INT1[6)], SSO1	INIT_ERR_APP1	WWD1_EC

(table continues...)

Table 42 (continued) Reaction on detected events of the system

	WWD1 missed or incorrect service (error counter below threshold)	any	No transition	INT1	SYS_STAT_APP1	WWD1_ERR
WWD2	WWD2 incorrectly triggered and error counter reaches threshold	on	Move to REDUCED OPERATION	INT2[6], SSO2	INIT_ERR_APP2	WWD2_EC
		on	Move to REDUCED OPERATION	INT1[4]	INIT_ERR_APP1	WWD2_EC
	WWD2 missed or incorrect service (error counter below threshold)	on	No transition	INT2	SYS_STAT_APP2	WWD2_ERR
FWD1	FWD1 incorrectly triggered and error counter reaches threshold	off	Move to INIT	RESOUT, SSO1, SSO2	INIT_ERR_APP1	FWD1_EC
		on	Move to REDUCED OPERATION	INT2[4]	INIT_ERR_APP2	FWD1_EC
		on	Move to REDUCED OPERATION	INT1[6], SSO1	INIT_ERR_APP1	FWD1_EC
	FWD1 response missed or incorrectly triggered (error counter below threshold)	any	No transition	INT1	SYS_STAT_APP1	FWD1_ERR
FWD2	FWD2 response missed or incorrectly triggered (error counter below threshold)	on	No transition	INT2	SYS_STAT_APP2	FWD2_ERR
	FWD2 incorrectly triggered and error counter reaches threshold	on	Move to REDUCED OPERATION	INT2[6], SSO2	INIT_ERR_APP2	FWD2_EC
		on	Move to REDUCED OPERATION	INT1[4]	INIT_ERR_APP1	FWD2_EC
INT	Interrupt flags not cleared after t_{INTx_to}	any	No transition	-	IF1	INTMISS
		on	No transition	-	IF2	INTMISS

(table continues...)

Table 42 (continued) Reaction on detected events of the system

Internal Element	Internal 2V5 rail overvoltage	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP1	INTSUP_VDD2V5
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP2	INTSUP_VDD2V5
	Internal 2V5 rail undervoltage	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	UV_STAT_APP1	INTSUP_VDD2V5_UV
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	UV_STAT_APP2	INTSUP_VDD2V5_UV
	Internal bias current too high	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	INTSUP_STAT_APP1	BIAS_HI
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	INTSUP_STAT_APP2	BIAS_HI
	Internal bias current too low	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	INTSUP_STAT_APP1	BIAS_LOW
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	INTSUP_STAT_APP2	BIAS_LOW
	Internal error; Always needs to be read when waking up from FAILSAFE (IF register is not being set in FAILSAFE but INTSUP_STAT_APPx can be set)	off	No transition	INT1	INTSUP_STAT_APP1	BG12_OV
		off	No transition	INT1	INTSUP_STAT_APP1	BG12_UV
		off	No transition	INT1	INTSUP_STAT_APP1	PMU_MAIN
		off	No transition	INT1	INTSUP_STAT_APP1	PMU_RED
		on	No transition	INT1, INT2	INTSUP_STAT_APP1	BG12_OV
		on	No transition	INT1, INT2	INTSUP_STAT_APP1	BG12_UV
		on	No transition	INT1, INT2	INTSUP_STAT_APP1	PMU_MAIN
		on	No transition	INT1, INT2	INTSUP_STAT_APP1	PMU_RED
		on	No transition	INT1, INT2	INTSUP_STAT_APP2	BG12_OV

(table continues...)

Table 42 (continued) Reaction on detected events of the system

		on	No transition	INT1, INT2	INTSUP_STAT_APP2	BG12_UV
		on	No transition	INT1, INT2	INTSUP_STAT_APP2	PMU_MAIN
		on	No transition	INT1, INT2	INTSUP_STAT_APP2	PMU_RED
	Internal IVCC overvoltage	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP1	INTSUP_IVCC
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OV_STAT_APP2	INTSUP_IVCC
	Internal IVCC undervoltage or short to ground	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	UV_STAT_APP1	INTSUP_IVCC_UV
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	UV_STAT_APP2	INTSUP_IVCC_UV
	Internal IVCC overcurrent	off	No transition	INT1	OT_WRN_OC_STAT_APP1	IVCC_OC
		on	No transition	INT1, INT2	OT_WRN_OC_STAT_APP1	IVCC_OC
		on	No transition	INT1, INT2	OT_WRN_OC_STAT_APP2	IVCC_OC
	Interval IVCC BIST errors, severe overvoltage	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP1	INTSUP_IVCC
		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP2	INTSUP_IVCC
	Double Error detected on a protected register	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP1	CFGE
	Double Error detected on a protected register	on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	SYSFAIL_STAT_APP2	CFGE
Safety Area	Overtemperature of safety area	any	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OT_STAT_APP1	SAFETY_AREA

(table continues...)

Table 42 (continued) Reaction on detected events of the system

		on	Move to FAILSAFE	RESOUT, SSO1, SSO2[2)]	OT_STAT_APP2	SAFETY_AREA
SPI	CRC wrong	off	No transition	INT1	SPI_FAIL_STAT_APP1	CRC
		on	No transition	INT1, INT2	SPI_FAIL_STAT_APP1	CRC
		on	No transition	INT1, INT2	SPI_FAIL_STAT_APP2	CRC
	CSN timeout after 2 ms	off	No transition	INT1	SPI_FAIL_STAT_APP1	CS_TO
		on	No transition	INT1, INT2	SPI_FAIL_STAT_APP1	CS_TO
		on	No transition	INT1, INT2	SPI_FAIL_STAT_APP2	CS_TO
	Frame length wrong	off	No transition	INT1	SPI_FAIL_STAT_APP1	FR_LEN
		on	No transition	INT1, INT2	SPI_FAIL_STAT_APP1	FR_LEN
		on	No transition	INT1, INT2	SPI_FAIL_STAT_APP2	FR_LEN
	Invalid address	off	No transition	INT1	SPI_FAIL_STAT_APP1	ADR
		on	No transition	INT1, INT2	SPI_FAIL_STAT_APP1	ADR
		on	No transition	INT1, INT2	SPI_FAIL_STAT_APP2	ADR
	Lock of protected registers was unsuccessful (will cause the registers to be locked again and made changes are ignored)	off	No transition	INT1	SPI_FAIL_STAT_APP1	LOCK
		on	No transition	INT1, INT2	SPI_FAIL_STAT_APP1	LOCK
		on	No transition	INT1, INT2	SPI_FAIL_STAT_APP2	LOCK
	SPI command woke up the device while in sleep	on	Move into WAKE if device is in SLEEP. Else no transition takes place.	INT1, INT2	WAKE_STAT_APP2	SPI

(table continues...)

Table 42 (continued) Reaction on detected events of the system

		on	Move into WAKE if device is in SLEEP. Else no transition takes place.	INT1, INT2	WAKE_STAT_APP1	SPI
		off	Move into WAKE if device is in SLEEP. Else no transition takes place.	INT1	WAKE_STAT_APP1	SPI
ABIST	ABIST finished execution	off	No transition	INT1	IF1	ABIST
		on	No transition	INT1, INT2	IF1	ABIST
		on	No transition	INT1, INT2	IF2	ABIST
	Any error that moves the device to FAILSAFE or INIT during an ABIST execution aborts the on-going ABIST and sets this bit.	any	No transition	RESOUT, SSO1, SSO2	SYSFAIL_STAT_APP1	ABIST
		on	No transition	RESOUT, SSO1, SSO2	SYSFAIL_STAT_APP2	ABIST
Application1	Application 1 was reason for entering REDUCED OPERATION	on	Move to REDUCED OPERATION	INT2[4)]	SYS_STAT_APP2	APP1_FAIL
	INIT timer expired a second time in RED. OP. due to application 1 not being able to reinitialize	on	Move to INIT	RESOUT, SSO2	INIT_ERR_APP1	REDOP_RES2
	INIT timer expired the first time in RED. OP. due to application 1 not being able to reinitialize	on	Move to REDUCED OPERATION	INT1	INIT_ERR_APP1	REDOP_RES1
Application2	Application 2 was reason for entering REDUCED OPERATION	on	Move to REDUCED OPERATION	INT1[4)]	SYS_STAT_APP1	APP2_FAIL

(table continues...)

Table 42 (continued) Reaction on detected events of the system

	INIT timer expired a second time in RED. OP. due to application 2 not being able to reinitialize	on	Move to INIT	RESOUT, SSO1	INIT_ERR_APP2	REDOP_RES2
	INIT timer expired the first time in RED. OP. due to application 2 not being able to reinitialize	on	Move to REDUCED OPERATION	INT2	INIT_ERR_APP2	REDOP_RES1

1) Only for move to INIT
2) Due to move to FAILSAFE also INTx will go low (QUC switched off in FAILSAFE)
3) Only if BUCKCORE and QUC are on
4) Configurable via SPI
5) Only if REDUCED OPERATION is enabled
6) Application reset
(x = 1; 2)

10.7 Analog built-in self test (ABIST)

10.7.1 Analog built-in self test (ABIST) - overview

The device contains an analog built in self-test function that can be triggered by the microcontroller. It serves the purpose to test the overvoltage and undervoltage comparators for the external and internal voltage rails, as well as the corresponding safety logic. By performing these tests, it can be ensured, that the monitoring works correctly and the warning and safety paths in the system are intact. The device differentiates between the following main configuration for the ABIST:

- Comparators Only (no deglitching)
- Full path including deglitching logic and interrupt generation (INTx)
- Full path including deglitching logic and secondary shutdown path (SSOx)

(x = 1;2)

The configuration for the mentioned tests is done in the registers:

- ABIST_CTRL0
- ABIST_SELECT0
- ABIST_SELECT1
- ABIST_SELECT2

In addition, the device allows specific analog tests, that affect the safety logic directly. For that the register

- ABIST_CTRL1

must be written accordingly.

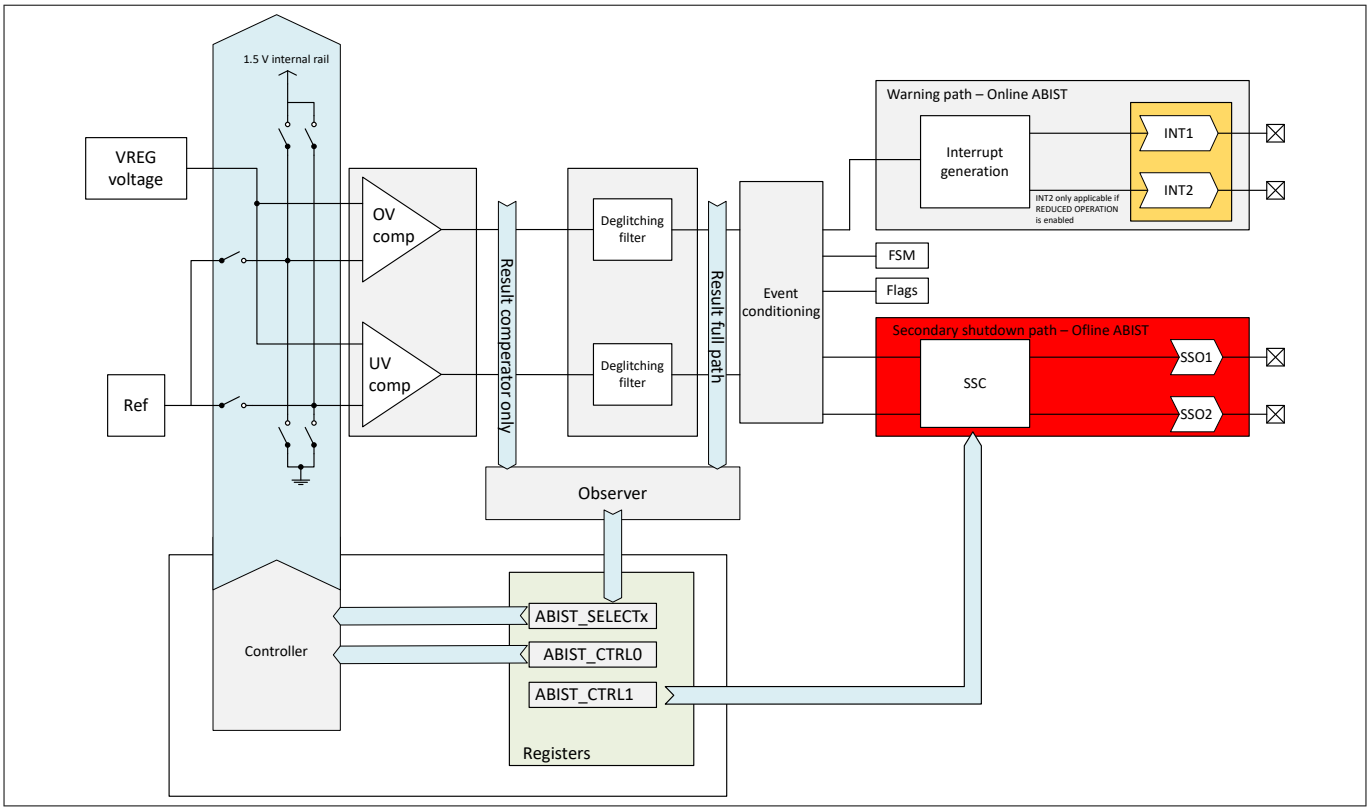


Figure 67 ABIST block diagram

10.7.2 ABIST - comparators only

The device provides the functionality to only test the comparators without the deglitching logic. During the test the overvoltage and undervoltage comparators are forced into error condition, by either connecting the reference input to ground or internal 1.5 V. This condition will only be applied for a time which does not exceed the deglitching logic filter time. Hence the remaining path (warning path, secondary shutdown path) is not tested any further.

10.7.3 ABIST - full path

The device provides the functionality to test the internal overvoltage and undervoltage comparators including the corresponding deglitching logic. This will consequently issue the respective full path as well (warning path, secondary shutdown path). When the full path to test to check SSO1/2 is started, the device must be in NORMAL state. For all other full path test executions the device can also be started in INIT or WAKE. Following the comparators are forced into error condition which is maintained for a time long enough to also trigger the deglitching logic. This will result in a corresponding event for the remaining path. If the test is started in NORMAL a state transition into WAKE will also occur (only for secondary shutdown path comparators, else no transition). Whether an interrupt at INT1/2 or a secondary shutdown path at SSO1/2 is issued, depends on the selection of the comparators, that has been made before the test was started. An overview of the corresponding comparator assignment can be found in the following table:

Table 43 ABIST - Comparator assignment to secondary shutdown path or warning path

Comparator	Secondary shutdown path	Interrupt
PREREG OV	x	
QST OV	x	
QUC OV	x	

(table continues...)

Table 43 (continued) ABIST - Comparator assignment to secondary shutdown path or warning path

BUCKCORE OV	x	
QCO OV	x	
QVR OV	x	
BUCKIF OV	x	
BOOST OV	x	
VMON1 OV	x	
VMON2 OV	x	
IVCC OV	x	
VDD2V5 OV	*	
PREREG SEVOV	*	
BUCKCORE SEVOV	*	
BUCKIF SEVOV	*	
R3FBL_OPEN	*	
PREREG UV		x
QST UV	x	
QUC UV	x	
BUCKCORE UV	x	
QCO UV		x
QVR UV		x
BUCKIF UV		x
BOOST UV		x
VMON1 UV		x
VMON2 UV		x
IVCC UV	x	
VDD2V5 UV	*	
BSTI UV	*	
BST_DEEP_UV	x	
VBAT OV	x	
BG12 UV		x
BG12 OV		x
BIASLOW	x	
BIASHI	x	
VDD1V5 UV	*	
VDD1V5 OV	*	

(table continues...)

Table 43 (continued) ABIST - Comparator assignment to secondary shutdown path or warning path

VDD5V0 UV	*	
VDD5V0 OV	*	

*) Comparators contribute to the secondary shutdown path but are not testable in full path by the ABIST.

***Note**: An interrupt for a single test execution (only one comparator tested) will show two interrupts at the device. One for the comparator test and one for the completion of the test execution. If multiple comparators are tested only one interrupt for test completion will be issued. The SSO1/2 event, as well as the state transition into WAKE from NORMAL takes only place once for each test execution. Meaning, that if a test sequence is being run for the full path, only the first comparator will trigger the state transition and its corresponding full path reaction (secondary shutdown path). All others will simply test the deglitching logic and set the corresponding flags.*

***Note**: To see the entire reaction chain for the full path, which includes the trigger of the INT pin or SSO1/2 pin (depending on the selected comparators) as well as the flagging of the respective error or status bits, it must be ensured by the integrator that all affected regulators that shall be tested are also enabled.*

10.7.4 ABIST - configuration and execution

To execute the ABIST the following selections and configurations must be made:

- ABIST_CTRL0:
  - START: Starts the ABIST
  - PATH: determines whether the full path or only the comparators are being tested
  - SINGLE: determines whether only a single comparator or an entire sequence (only the selected comparators in ABIST_SELECT0/1/2) is executed
  - INT: must be configured to select the test either for the warning path (interrupt related comparators) or the secondary shutdown path (SSO1/2 related comparators
  - STATUS: indicates whether the ABIST has finished with or without errors
  - ALL: if set, all comparators in ABIST_SELECT0/1/2 are automatically selected and the test is executed with PATH = 0 and SINGLE = 0 except BSTI UV comparator
- ABIST_SELECT0/1/2: determines which comparators shall be tested during execution

Note: Integrator must ensure that the bit ABIST_SELECT1.BSTIUV is set to 0, especially before starting any ABIST operation in case an error in BSTI UV is reported

When the execution of the ABIST has finished:

1. An interrupt is issued
2. Check if ABIST_CTRL0.START = 0
3. ABIST without errors: ABIST_CTRL0.STATUS = 0x5
4. ABIST with errors: ABIST_CTRL0.STATUS = 0xA
5. Read ABIST_SELECT0/1/2:
   - 0: Comparator intact
   - 1: Comparator failed test

10.7.5 ABIST - testing the secondary shutdown path logic

In addition to the above described comparator tests, the device provides the option to directly force and hereby test the activation of the secondary shutdown path. This can be done for each SSO1/2 separately and is applied immediately once the register ABIST_CTRL1 is written.

The following tests can be applied by writing ABIST_CTRL1:

- OV_1V5_TRIG: forces an overvoltage at the internal 1.5 V supply of the secondary shutdown path logic
  - Expected result: SSO1/2 must be activated (pulled low)
- ABIST_CLK_EN: enables the internal clock signal for the SSOx reaction
  - Must be used in combination with the other bits in ABIST_CTRL1. For further references the Safety Manual provides more information.
- SS1_EN_BIST: interrupts the safety clock signal only for SS1
  - Expected result: SSO1 must be activated (pulled low)
- SS2_EN_BIST: interrupts the safety clock signal only for SS2
  - Expected result: SSO2 must be activated (pulled low)

11 Interrupt function (INT)

11.1 Introduction

The interrupt module is used to inform the microcontoller that a system event has been detected by the device. It is a request to the microcontoller to perform a diagnostic of the device.

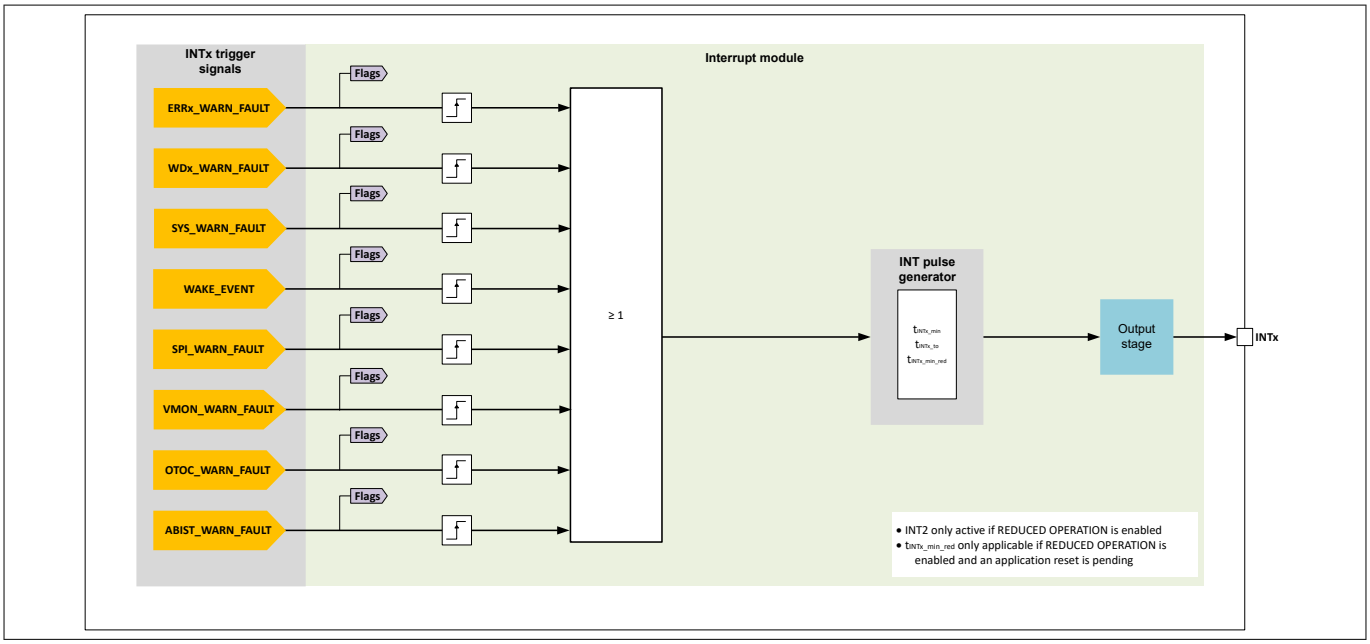


Figure 68 Functional block diagram Interrupt function

The interrupt module provides two interrupt channels.

General occurrences are reported on INT1. If REDUCED OPERATION is enabled, INT1 and INT2 are additionally activated for their application specific error cases (see Reaction on faults).

Each interrupt pin INTx (x = 1 or 2) is a push-pull stage.

The device can be configured for single application or dual application use cases.

Single Application use case (default configuration):

In this case, any interrupt-triggered signal detection activates the interrupt on the output pin INT1.

Dual Application use case:

Dual applications use case can be activated via SPI by setting the bit **REDOP_PW_CFG1.EN** to 1.

In this case (see Reaction on faults):

- The detection of the Interrupt-triggered signal on application 1 activates the interrupt on the output pin INT1
- The detection of the Interrupt-triggered signal on application 2 activates the interrupt on the output pin INT2
- The detection of general events is reported at both interrupt lines INT1 and INT2
- The detection of a severe fault **(WD1_SEV_FAULT or ERR1_SEV_FAULT)** on application 1 activates an interrupt on the application 2 if SPI bit **REDOP_RS_CFG1.INT2_DIS** is set to 0 (Condition: Device must be in NORMAL or REDUCED OPERATION state)
- The detection of a severe fault **(WD2_SEV_FAULT or ERR2_SEV_FAULT)** on application 2 activates an interrupt on the application 1 if SPI bit **REDOP_RS_CFG1.INT1_DIS** is set to 0 (Condition: Device must be in NORMAL or REDUCED OPERATION state)

11.2 Interrupt activation

The default output value of the interrupt pin is logical high (no interrupt pending). The device activates an interrupt by setting the related interrupt pin to "low".

After the interrupt pin becomes inactive (Interrupt signal transition from "low" to "high"), a minimum active time t_{INTx_to} has to elapse before new interrupt requests can reactivate the pin. The t_{INTx_to} time starts with the next rising edge of the interrupt pin.

The occurrence of an interrupt is latched in a status register and can be read and cleared on a write command via SPI after removing the failure.

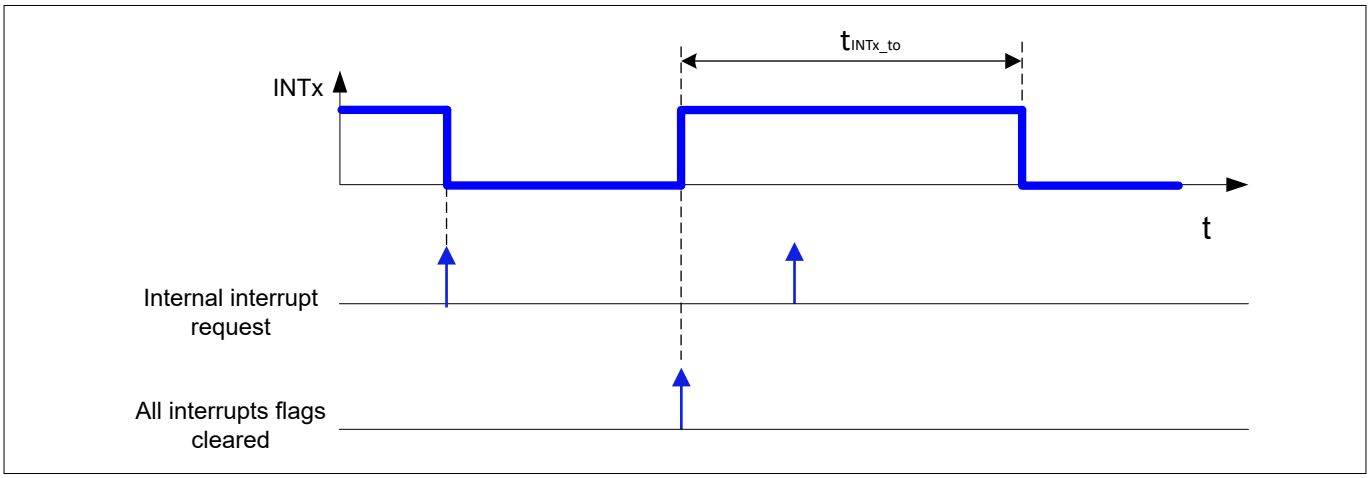


Figure 69 Activation of the interrupt pin INTx (set interrupt pin to logical low)

11.3 Interrupt deactivation

The interrupt will be deactivated and set to logical "high" under the following conditions:

- If all dedicated interrupt flags are cleared after the minimum interrupt pulse width t_{INTx_min} AND before t_{INTx_to} is expired (see figure deactivating of interrupt by clearing all dedicated interrupt flags).
- If t_{INTx_min} expires, and all interrupt flags have been cleared in time(see figure deactivating of interrupt by the minimum pulse width if interrupt flags are cleared too early)
- If $t_{INTx\_min\_red}$ expires and REDUCED OPERATION is enabled while an application reset is pending
- If t_{INTx_to} expires and not all interrupt flags have been cleared in time(see figure deactivating of interrupt by t_{INTx_to} if interrupt flags cleared too late). In this case a missing interrupt is detected, the bit **IFx.INTMISS** is set and can be clear via SPI

(x=1,2)

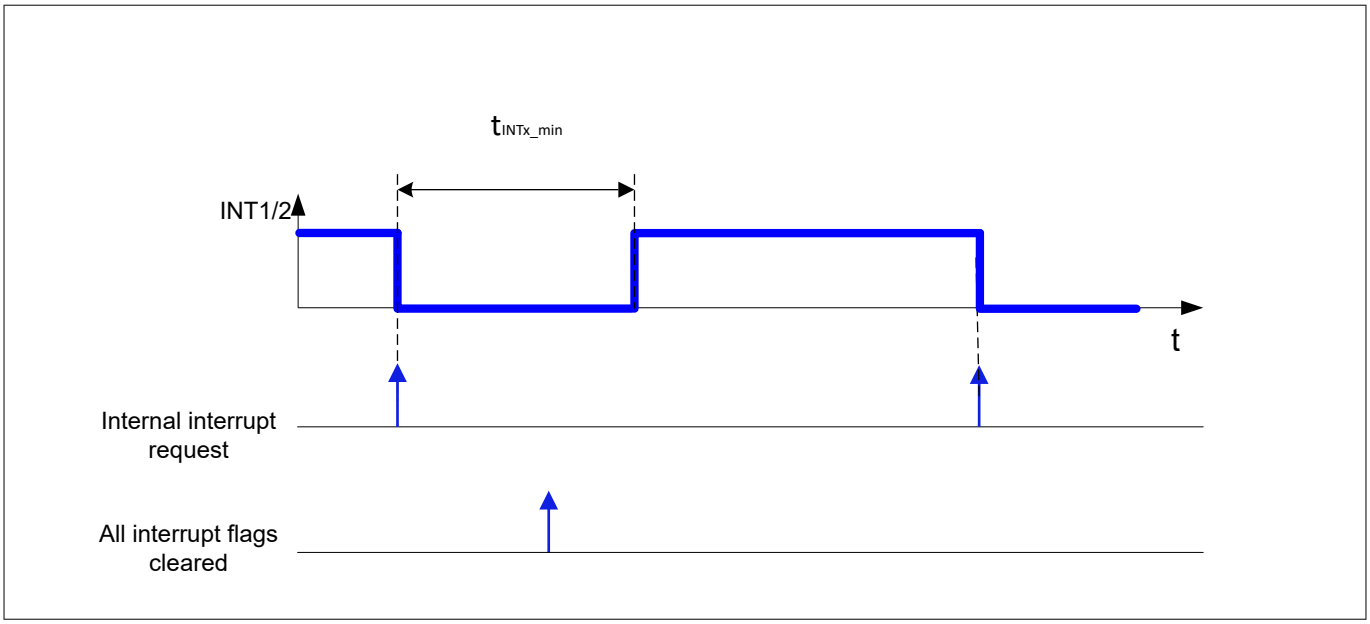


Figure 70 **Deactivating of interrupt by the minimum pulse width if interrupt flags are cleared before expiration of t_{INTx_min}**

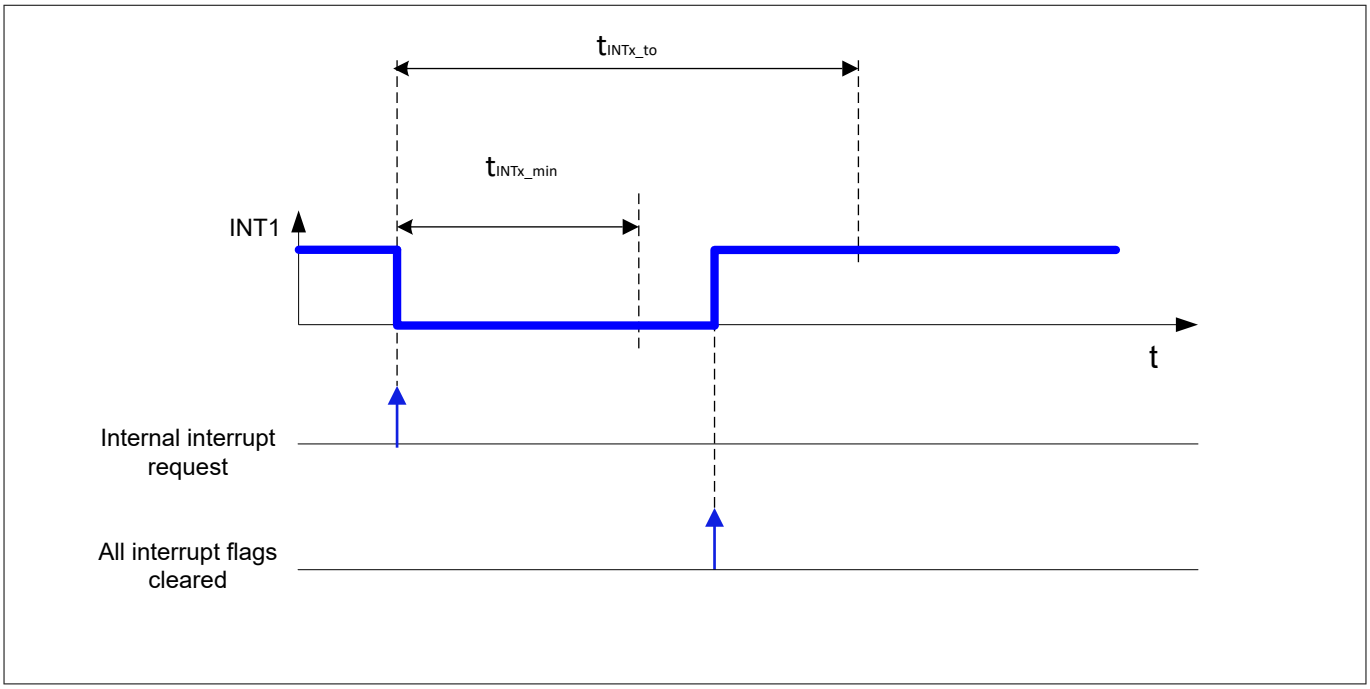


Figure 71 **Deactivating of interrupt by clearing all dedicated interrupt flags**

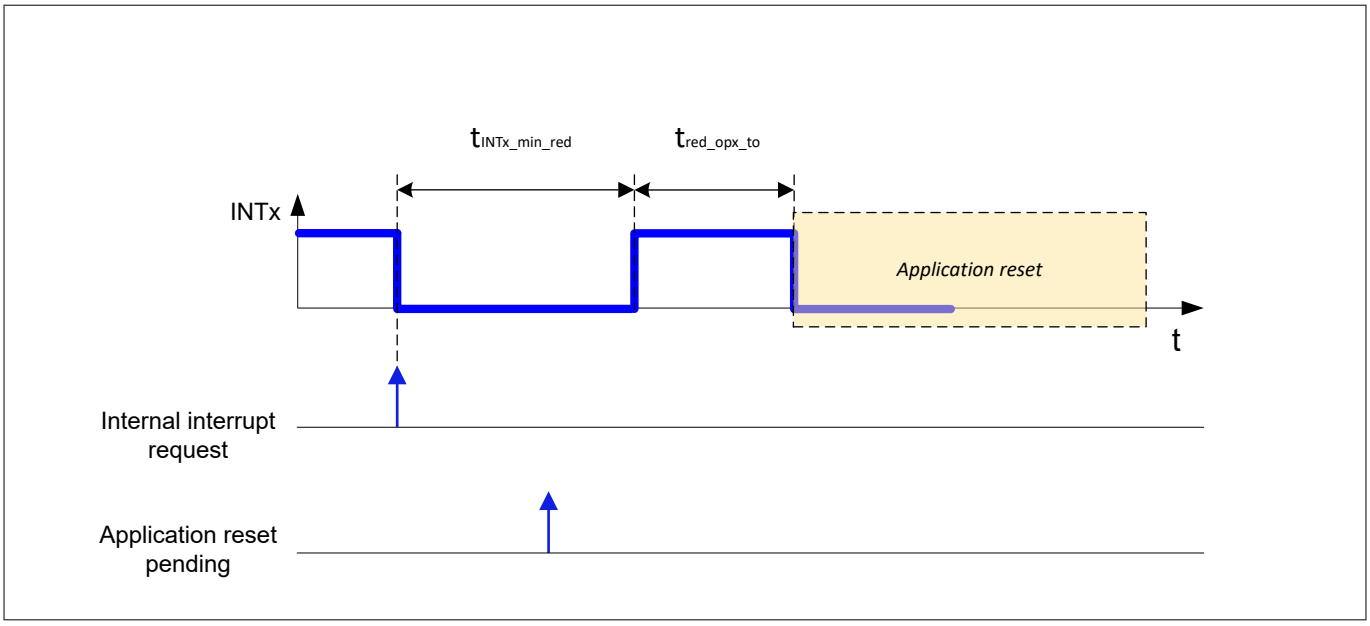


Figure 72 Deactivation of interrupt by pending application reset

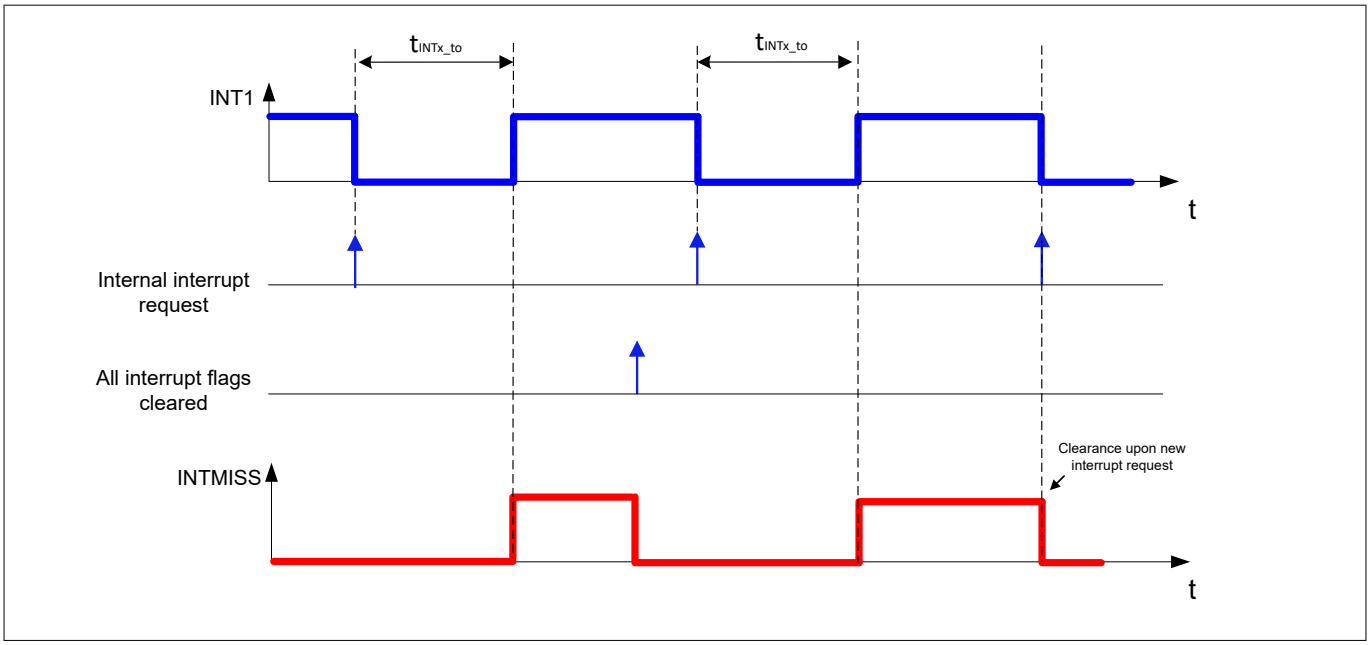


Figure 73 Missed interrupt (Deactivating of interrupt by timeout (t_{INTx_to}) if interrupt flags cleared too late)

11.4 Electrical characteristics interrupt (INT)

Table 44 Electrical characteristics interrupt (INT)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output voltage high level	V_{INT_H}	2	–	–	V	$V_{QUC} \geq V_{QUC}$[Min]; I_{INT} = -7 mA; Parameter applicable to INT1 and SYNC_IN/INT2	DS-1642
Output voltage low level	V_{INT_L}	–	–	0.7	V	I_{INT} = 5.5 mA; Parameter applicable to INT1 and SYNC_IN/INT2	DS-1643
Pin output rise time	t_{INT_RISE}	–	–	25	ns	$C_{INT,load}$ = 50 pF[1)]	DS-1644
Pin output fall time	t_{INT_FALL}	–	–	25	ns	$C_{INT,load}$ = 50 pF[1)]	DS-1645
Minimum interrupt pulse width for single application use case	t_{INTx_min}	90	100	150	µs	[1)]	DS-1646
Interrupt pulse timeout	t_{INTx_to}	270	300	350	µs	[1)]	DS-1647
Minimum interrupt pulse width for dual application used case - application reset pending	$t_{INTx\_min\_red}$	50	55	60	µs	[1)]	DS-1649

1) Not subject to production test, specified by design

12 Reset function (RESOUT)

12.1 Functional description reset function (RESOUT)

12.1.1 Introduction

The Reset module is used to reset a group of applications (Application Reset) or to reset the total system (System Reset) based on the configuration and the source of the reset. An application reset is only active if REDUCED OPERATION is enabled.

12 Reset function (RESOUT)

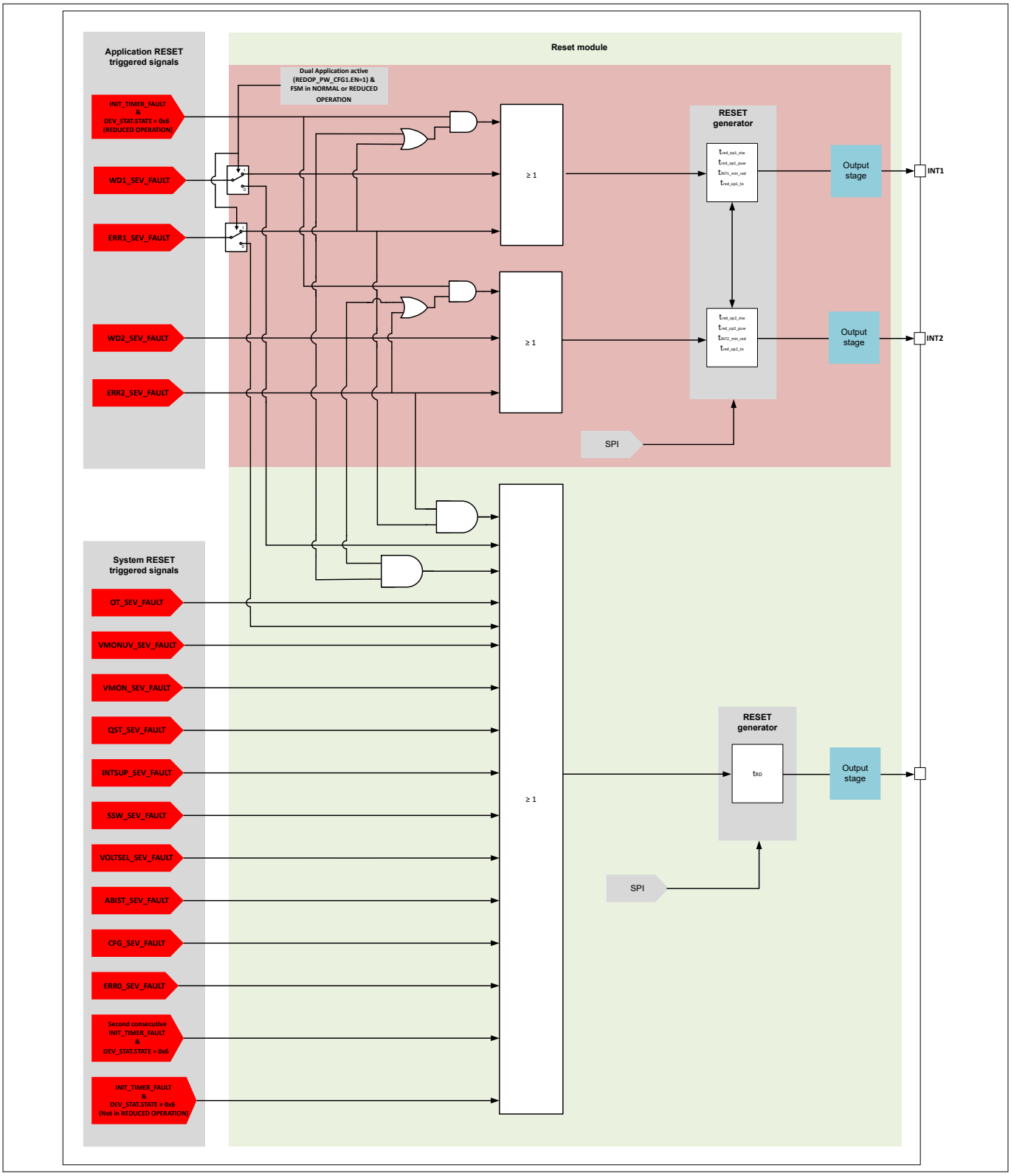


Figure 74 Functional block diagram reset function

The reset module provides following reset channels:

- Two channels for application reset. The application reset is activated on the output pins INTx (x = 1 or 2) if an application reset-triggered signal is detected on the related application (valid only for dual application use case (bit **REDOP_PW_CFG1.EN** = 1))
- One channel for system reset. The system reset is activated on the output pin RESOUT if:
  - a system reset-triggered signal is detected
  - an application reset-triggered signal is detected on both applications (valid only for dual application use case **REDOP_PW_CFG1.EN** = 1)

12.1.2 Application Reset (REDUCED OPERATION ENABLE)

12.1.2.1 Activation

The device activates an application reset by generating a "low" pulse on the related interrupt pin (INTx) if one of the following application-reset-triggered signals is detected on the corresponding application:

- A severe fault of the WD or ERRx monitoring(WDx_SEV_FAULT or ERRx_SEV_FAULT), see application reset activation
- The INIT timer elapses once (INIT_TIMER_FAULT) when the device is in REDUCED OPERATION state (SPI Bitfield **DEV_STAT.STATE = 0x6**), see application reset activation INIT timer fault.

The duration of the pulse length ($t_{red\_opx\_puw}$) is configurable via SPI and can be calculated with following formula:

	Calculation	$t_{red\_opx\_stw}$	STEP
Pulse type 1 (default):	$t_{red\_opx\_puw}$ = STEP × $t_{red\_opx\_stw}$	10 µs (TYP)	1 ... 8
Pulse type 2:	$t_{red\_opx\_puw}$ = STEP × $t_{red\_opx\_stw}$;	100 µs (TYP)	1 ... 8

$t_{red\_opx\_stw}$ can be configured via SPI bit **REDOP_RS_CFG2.REDOP_RESOUT_APP_TB**, the default value is 10 µs and STEP can be configured via SPI bit **REDOP_RS_CFG2.REDOP_RESOUT_APPx_DUR.**

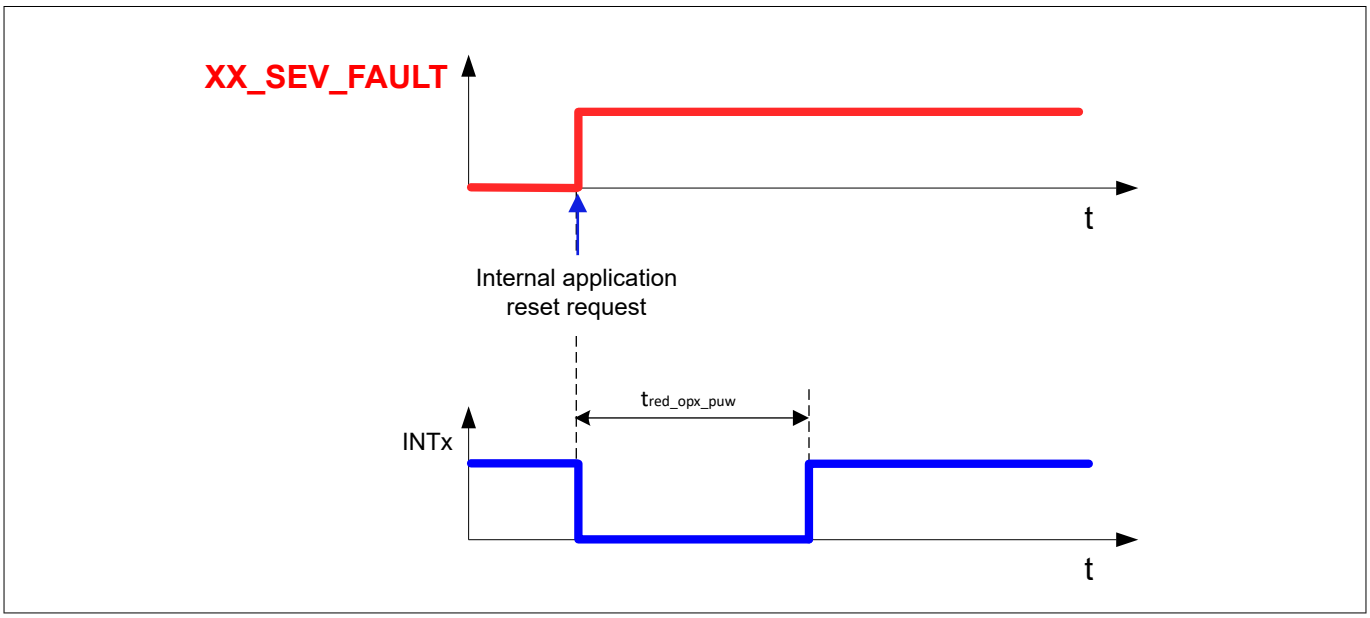


Figure 75 Activation of the application reset due to a severe fault

(xx: ERR1/2 or WD1/2 or INIT timer expiration in combination with one of the modules ERR1/2 or WD1/2)

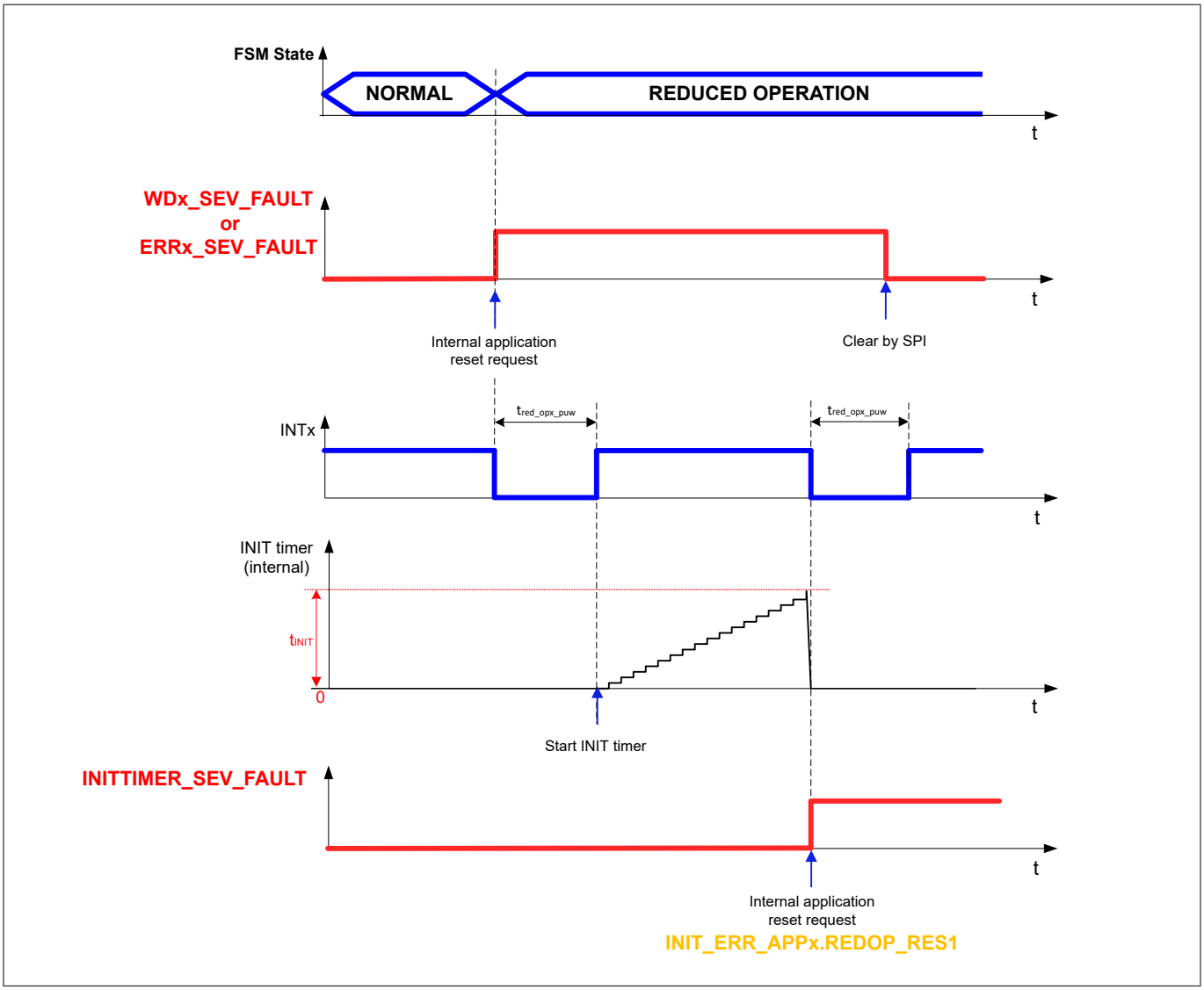


Figure 76 Activation of the application reset due to INIT_TIMER_FAULT

(x = 1; 2)

If the application reset is activated when the interrupt is active, the device sequentially:

1. Waits for the minimum interrupt pulse width $t_{INTx\_min\_red}$
2. Releases the interrupt line and waits for $t_{red\_opx\_to}$
3. Generates the interrupt pulse with its configurable width $t_{red\_opx\_puw}$

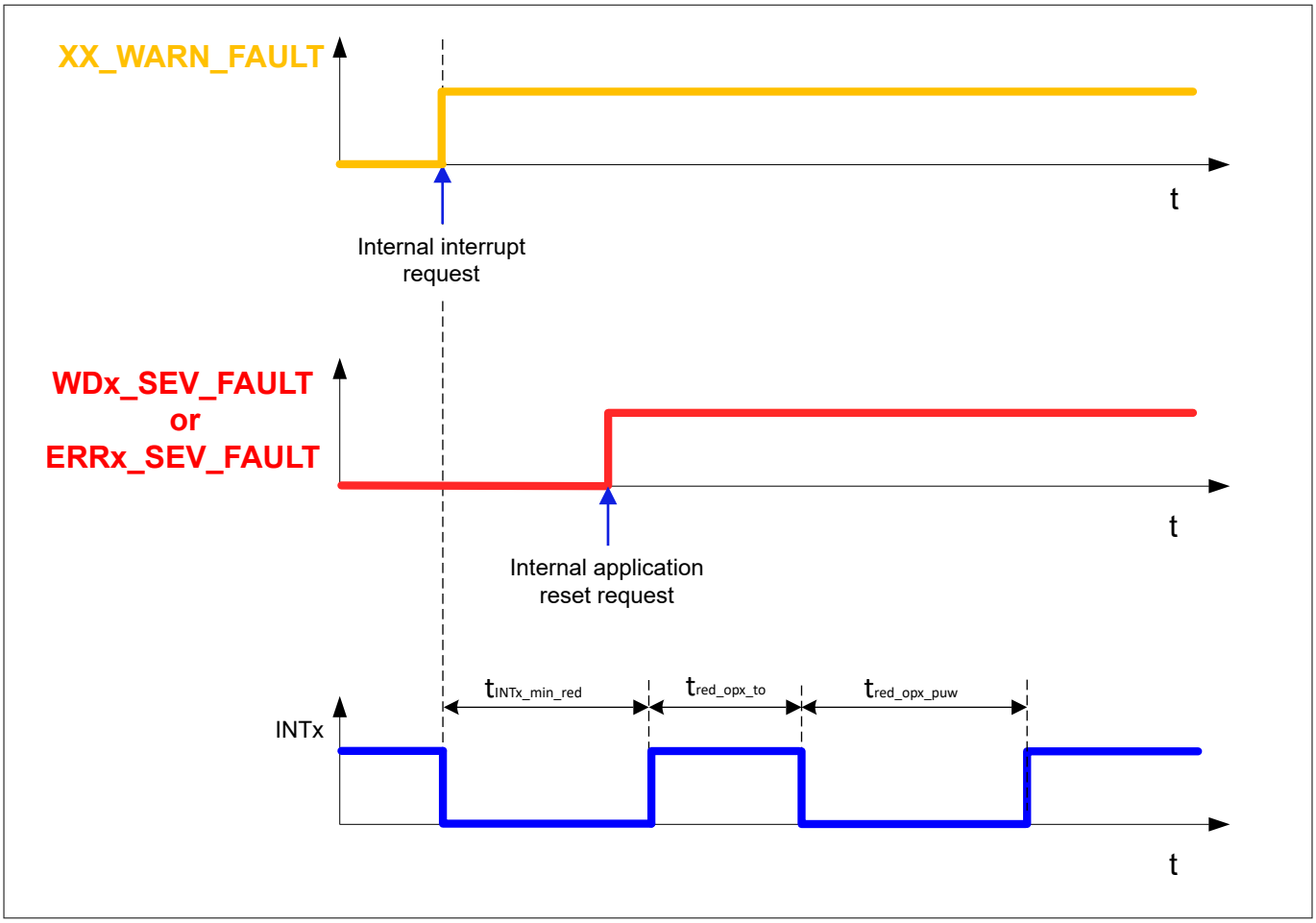


Figure 77 Application reset activation with interrupt active

If the INIT timer elapses **once** in REDUCED OPERATION state, the device:

- generates an INIT_TIMER_FAULT,
- activates a new application reset,
- sets the bit **INIT_ERR_APPx.REDOP_RES1**; which can be clear by SPI after removing the fault.
- remains in REDUCED OPERATION

If the INIT timer elapses **twice** in REDUCED OPERATION state, the device

- generates an INIT_TIMER_FAULT
- activates a system reset
- sets the error bits **INIT_ERR_APP1.REDOP_RES2** and **INIT_ERR_APP2.REDOP_RES2**; which can be clear by SPI after removing the fault.
- moves to INIT state, see Chapter 9.

12.1.3 System Reset

12.1.3.1 Activation

The reset output pin RESOUT is an open drain structure. An internal pull up current (I_{RESOUT_PU}) is pulling the output towards V_{QUC}. As soon as a system reset condition occurs, the device triggers a reset by pulling pin RESOUT below V_{RESOUT_LOW}.

An additional external pull-up resistor can be connected between the RESOUT and V_{QUC} pins to speed up the low-to-high transition.

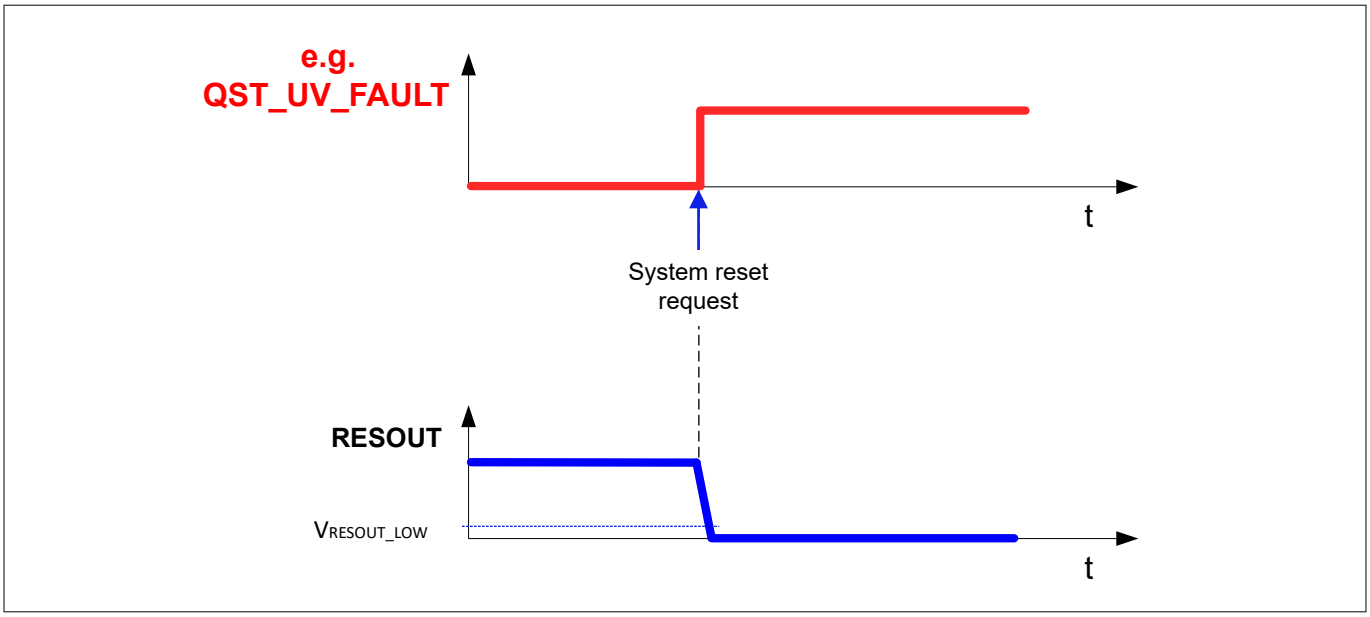


Figure 78 Activation of a system reset

12.1.3.2 Hard and Soft reset

Definition

Based on the detected system fault, the device generates a **"Soft Reset" (WARM RESET)** or a **"Hard Reset" (COLD RESET)** after entering INIT sate, see Chapter 9.

- It is called a **"Soft Reset"** if pin RESOUT goes below V_{RESOUT_LOW}, but the pre and post regulator output voltages are not switched off.
- It is called a **"Hard Reset"** if pin RESOUT goes below V_{RESOUT_LOW}, and all regulator output voltages are switched off.

If the INIT timer elapses **once** in INIT or in WAKE state, the device:

- activates a soft reset
- generates an INIT_TIMER_FAULT
- set the bit **INIT_ERR_APPx.SOFTRES**; which can be clear by SPI
- moves into INIT state, see Chapter 9

If the INIT timer elapses **second time** in a row in INIT state, the device

- activates a hard reset, all regulator output voltages are switched off
- generates INIT_TIMER_FAULT
- sets the error bit **INIT_ERR_APPx.HARDRES**; which can be clear by SPI after removing the fault
- moves into INIT state, see Chapter 9

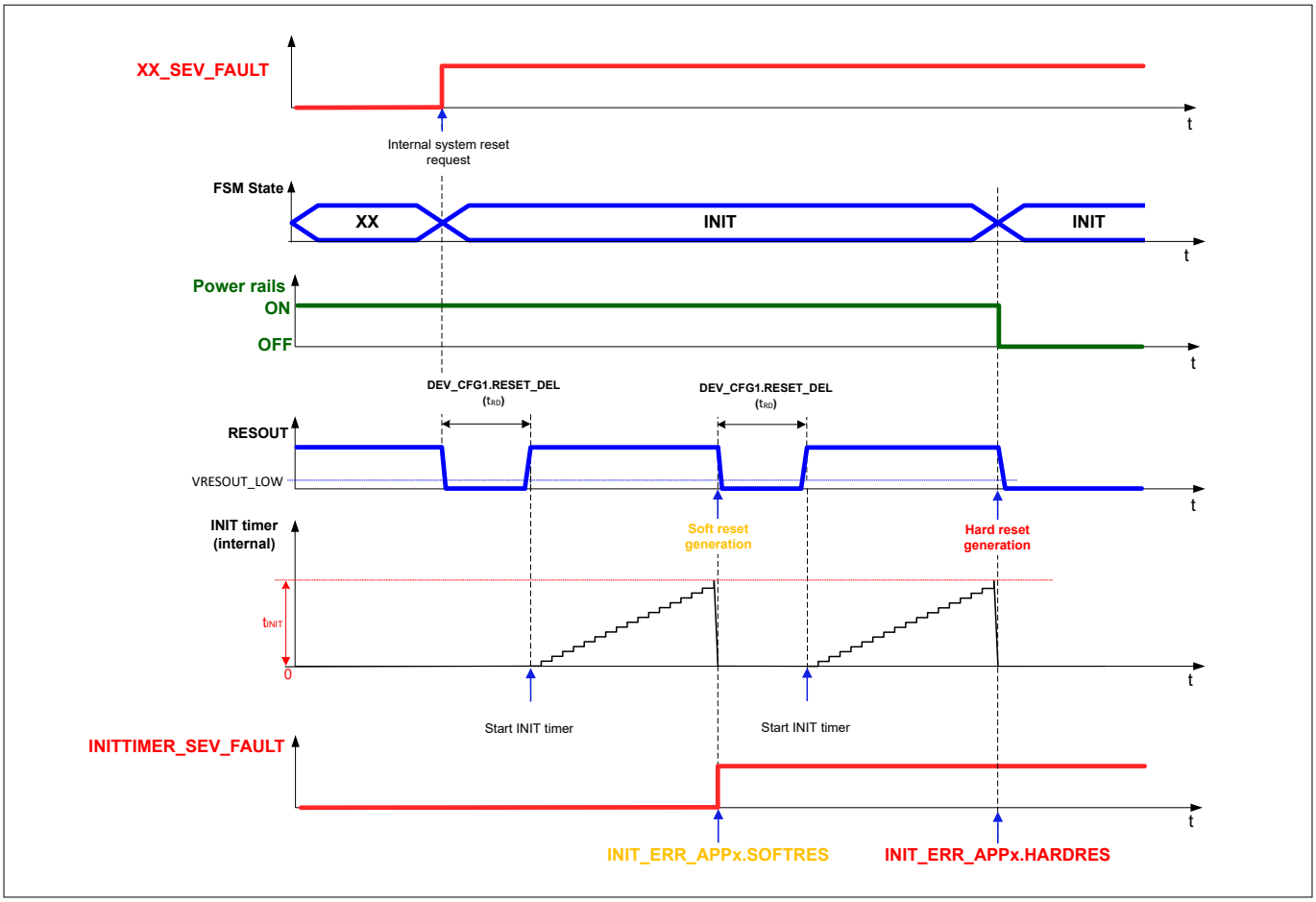


Figure 79 Signal diagram Soft and Hard reset activation

Reset release

After a soft reset generation, the device releases the reset by setting the output pin RESOUT "high" after the reset delay time (t_{RD}).

After a hard reset generation, the device waits for QST, QUC and BUCKCORE to reached their undervoltage threshold during the power up sequencing schema A or the power up sequencing schema B. Only if this was successful, the device:

1. Waits for the reset delay time t_{RD}
2. Sets the output pin RESOUT "high"

Reset Delay time configuration

Upon starting up from POWERDOWN or STANDBY with WUT and QST disabbled, the default value of the reset delay time can is set by hardware, see HWCFG.

The configuration of the reset delay time t_{RD} is configurable during runtime in the register **DEV_CFG1.RESET_DEL**.

12.2 Electrical characteristics reset function (RESOUT)

Table 45 Electrical characteristics reset function (RESOUT)

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
RESOUT start up delay time 2ms	t_{RD_2ms}	1.8	2	2.2	ms	RESOUT start up delay time is set to 2ms by HWCFG 1)	DS-1539
RESOUT start up delay time 10ms	t_{RD_10ms}	9	10	11	ms	RESOUT start up delay time is set to 10ms by HWCFG 1)	DS-1540
Pull-up current	I_{RESOUT_PU}	-180	-55	-15	µA	$V_{RESOUT} \leq 2.0$ V	DS-2131
Low level	V_{RESOUT_LOW}	–	–	0.4	V	$V_{QUC} = V_{QUC}$ [Typ]; I_{RESOUT} = 3.5 mA	DS-1558
REDUCED OPERATION configurable reset step (default)	$t_{red\_opx\_stw}$	9	10	11	µs	Default configuration 1)	DS-1648
REDUCED OPERATION reset timeout	$t_{red\_opx\_to}$	9	10	11	µs	1)	DS-1650
Output fall time	t_{RESOUT_FALL}	–	–	25	ns	$C_{RESOUT,load}$ = 50 pF 1)	DS-1559

1) Not subject to production test, specified by design

13 Microcontroller programming support (MPS)

The device includes a Microcontroller Programming Support (MPS) function, during which the following events are masked:

- MCU reset events (RESOUT) due to ERR1/2 pin monitoring reactions
- MCU reset events (RESOUT) due to watchdog reactions
- MCU reset events (RESOUT) due to all INIT timers (including REDUCED OPERATION) expiration reactions (INIT timer is stopped or not started)
- Transition to FAILSAFE due to ERR0 pin monitoring reaction. In case ERR0 is triggered, the device will move to INIT state without generating a reset events

This allows for example a programming of the µC without interruptions.

***Note**: All other faults generates their respective response and other behaviors of the device remain the same.*

The MPS mode can be configured:

- Via hardware by setting the correspondent resistor value as describe in the HWCFG table
  - The MPS mode selection is refreshed only after a power cycle has been performed
- Via SPI command
  - MPS mode can be enable or disable in all FSM modes (**DEV_CFG1.MPS_EN**).

14 SPI

The Serial Peripheral Interface (SPI) is the communication link between the device and the microcontroller and supports multi-slave operation in full-duplex mode with 32 bit data access. The data transmission starts with the MSB. The clock polarity (CPOL) is 0 and the clock phase (CPHA) is 1.

The SPI uses 4 interface signals for synchronization and data transfer:

- CSN: SPI chip select (active low)
- SCK: SPI clock
- SDI: SPI data input
- SDO: SPI data output

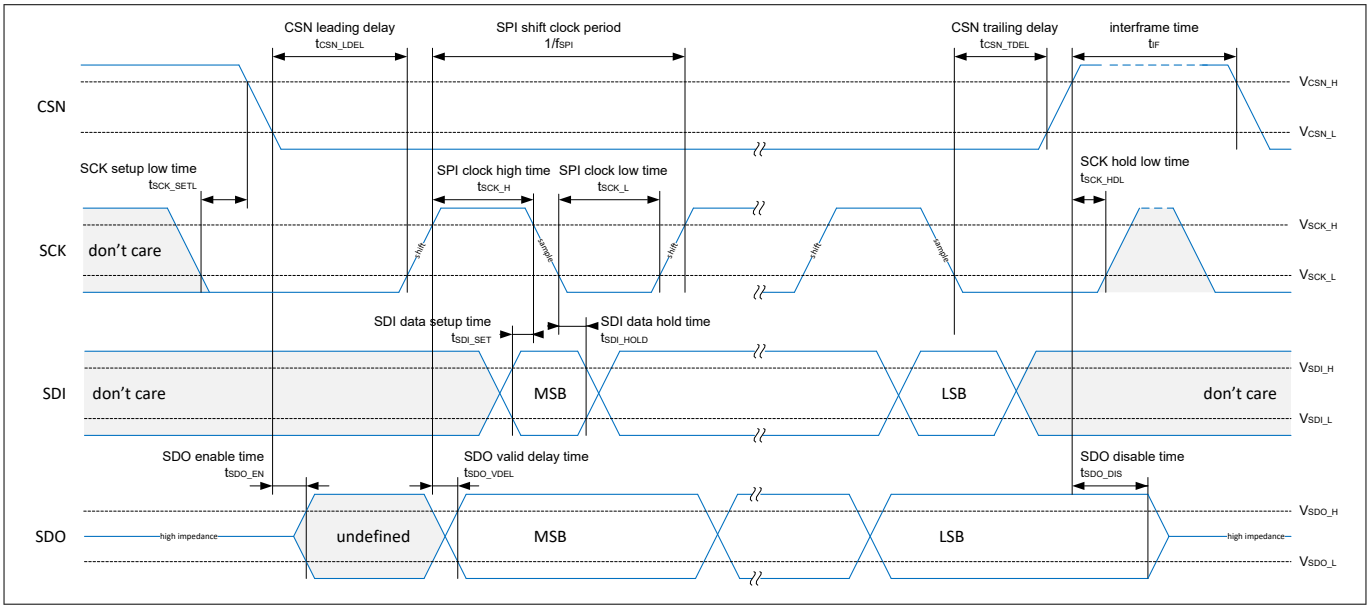


Figure 80 SPI signals

14.1 Functional description SPI

14.1.1 SPI data transfer

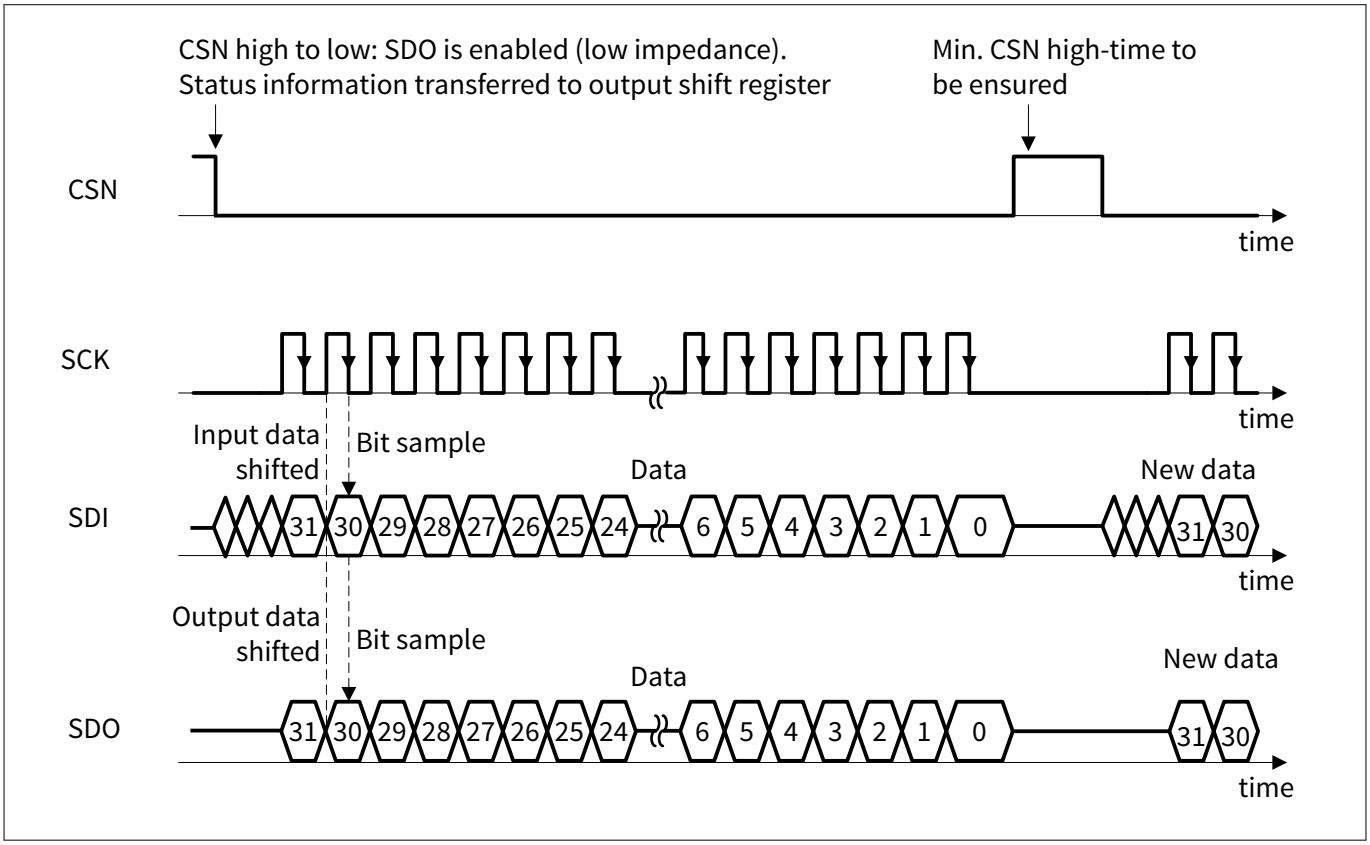


Figure 81 SPI data transfer

The SPI transfer begins when the device is selected by setting the CSN pin to "low". On every SCK rising edge data is shifted in on SDI (MSB first) and respectively shifted out on SDO (MSB first). The data on SDI is sampled on every falling edge of SCK. The SPI transfer is terminated by detecting a "high" signal at CSN. While CSN is at "high" level, SDO is set to high impedance.

The SPI does not support daisy chaining.

14.1.2 SPI frame format

The following section defines the SPI frame formats and defines the SPI service.

14.1.2.1 SPI transfer

An SPI transfer consists of the following frames:

- SDI frame
- SDO frame

After 32 shift clock cycles the device has received the SDI frame and the master (microcontroller) has received the SDO frame. Figure 82 illustrates the structure of an SPI transfer.

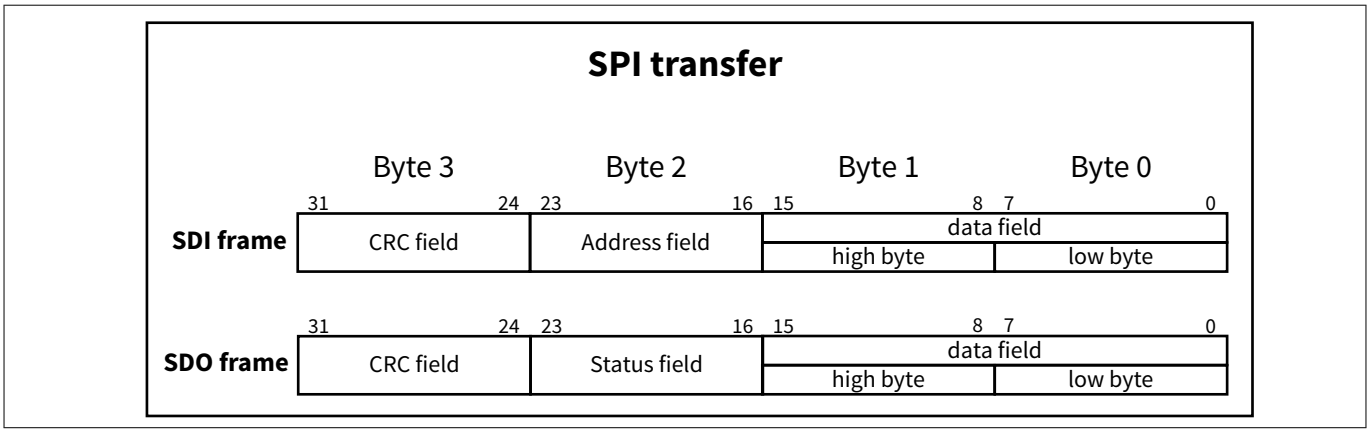


Figure 82 SPI transfer structure

14.1.2.2 SPI service

An SPI service can be a write service or a read service and consists of two SPI transfers. The first SPI transfer (request) contains the request information in the SDI frame which the master (microcontroller) sends to the device. The SDO frame of the first SPI transfer (request) contains the response information of the previous service and is not relevant for the current service. The second SPI transfer (response) contains the response information in the SDO frame. The SDI frame contains the request information of the next service and is not relevant for the current service. Figure 83 shows the structure of the SPI service.

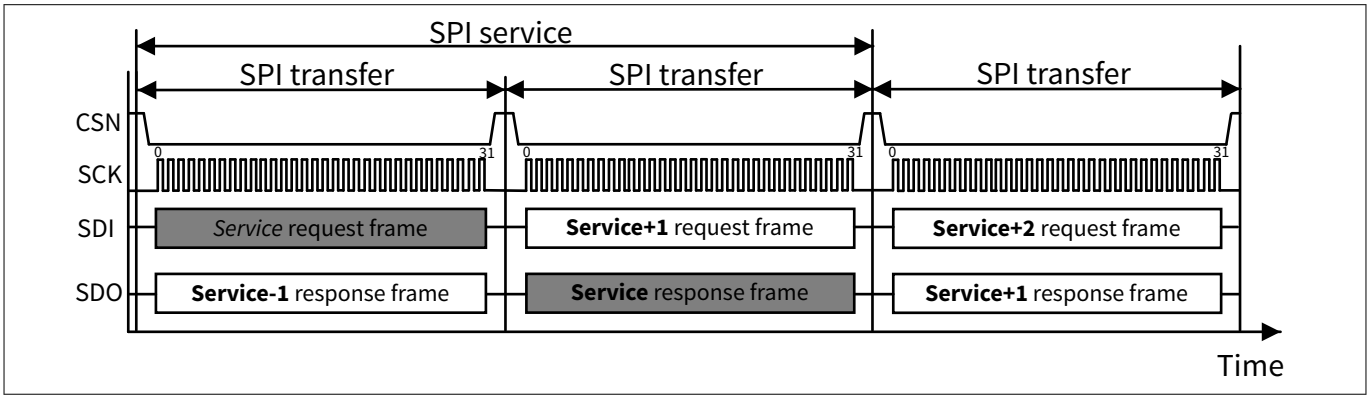


Figure 83 SPI service and transfer definition

14.1.2.3 SPI read service

A read service consists of two SPI transfers (request SPI transfer and response SPI transfer). Figure 84 illustrates the structure of the read service.

Request SPI transfer SDI frame

- CRC field: The calculation process of the CRC value is described in Chapter 14.1.2.5
- Address field: The value of the address field must be FF_H, which defines a read service
- Data field: The data field contains the address of the register which shall be read

Response SPI transfer SDO frame

- CRC field: The calculation process of the CRC value is described in Chapter 14.1.2.5
- Status field: The status field is described in Chapter 14.1.2.6
- Data field: The data field contains the value of the register which was addressed in the request SPI transfer SDI frame

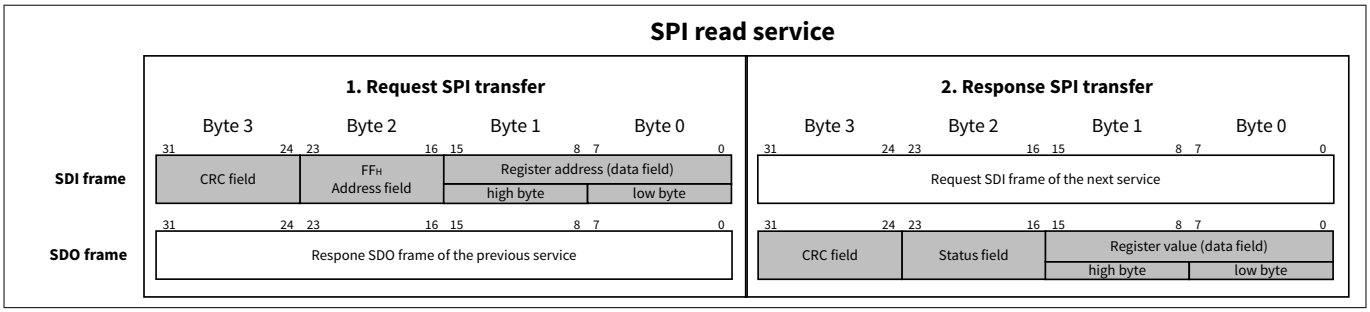


Figure 84 Structure of the read service

14.1.2.4 SPI write service

A write service consist of two SPI transfers (request SPI transfer and response SPI transfer). Figure 85 illustrates the structure of the read service.

Request SPI transfer SDI frame

- CRC field: The calculation process of the CRC value is described in Chapter 14.1.2.5
- Address field: The address field contains the address to the register which shall be written
- Data field: The data field contains the value which shall be written to the register

Response SPI transfer SDO Frame

- CRC field: The calculation process of the CRC value is described in Chapter 14.1.2.5
- Status field: The status field is described in Chapter 14.1.2.6
- Data field: The data field contains the new value of the register after it was written

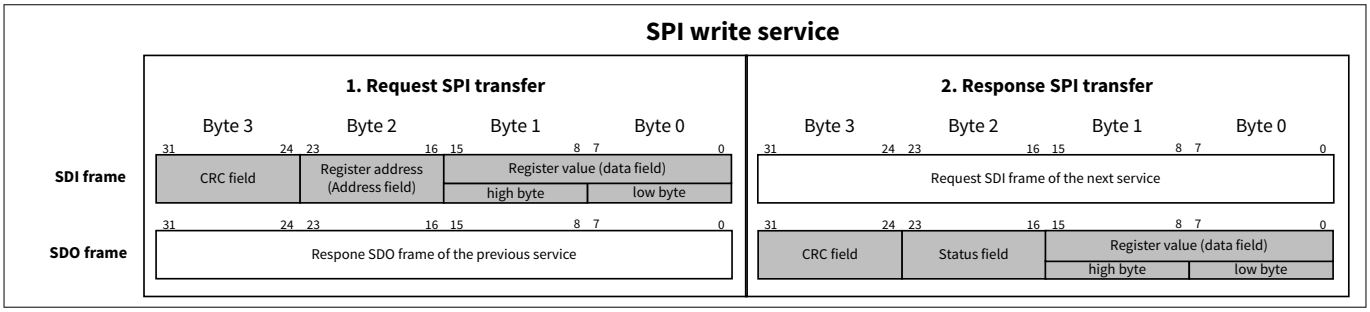


Figure 85 Structure of the SPI write service

14.1.2.5 CRC field

This chapter describes the CRC calculation from the point of view of the microcontroller and of the device.

The CRC calculation uses the CRC8 of SAE J1850 standard.

The mathematical background for the CRC8 calculation and algorithm is described in the CRC AUTOSAR specification Version 4.3.1. The following C# example code explains the algorithm for calculating the CRC8.

```
Byte crc8(Byte[] data ,uint length) {
    Byte crc;
    uint i,bit;

    //Inital value must be 0xFF
    crc = 0xFF;
    for ( i=0 ; i<length ; i++ ) {
        crc ^= data[i];
        for ( bit=0 ; bit<8 ; bit++ ) {
            if ( (crc & 0x80)!=0 ) {
                crc <<= 1;
                crc ^= 0x1D;  //Polynomial is 0x1D
            }
            else {
                crc <<= 1;
            }
        }
    }

    return (Byte)~crc;
}
```

The microcontroller calculates the CRC in the SDI frame (see Chapter) and must checks the CRC in the SDO frame (see Chapter).

The device calculates the CRC in the SDO frame (see Chapter) and must check the CRC in the SDI frame (see Chapter).

14.1.2.5.1 CRC microcontroller handling

CRC calculation

The CRC calculation includes the following SDI frame elements (Figure 86):

- Low byte of the data field
- High byte of the data field
- Address field

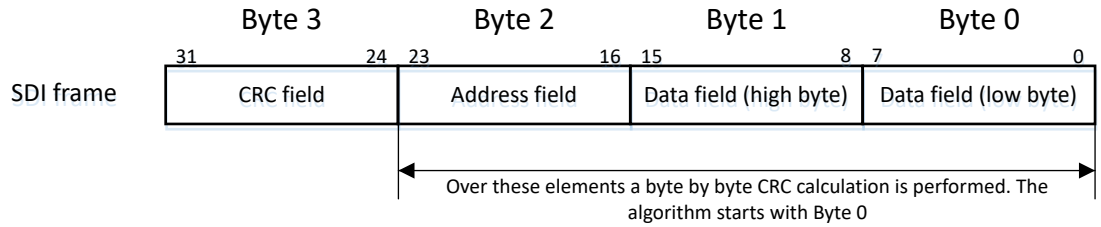


Figure 86 Byte order for SAE J1850 CRC calculation

To write to the register address 83_H the register value $01F2_H$, the CRC algorithm (see Chapter 14.1.2.5) requires the following input parameters:

- Input bytefield parameter data: {$F2_H$, 01_H, 83_H}
- Input parameter length: 3

The result of the CRC calculation is 37_H. The SDI frame which must be sent from the microcontroller shows Figure 87.

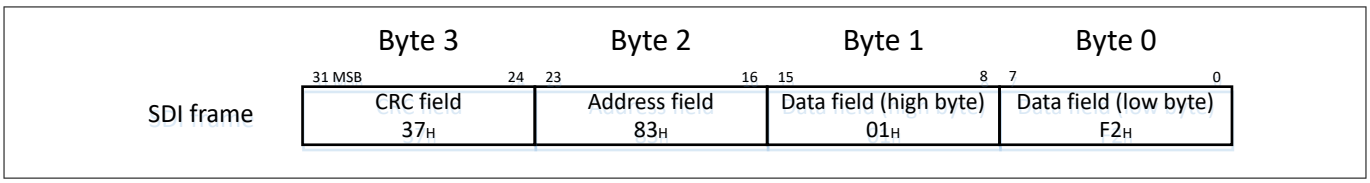


Figure 87 SDI frame example

CRC check

The CRC check includes the following SDO frame elements (Figure 88):

- Low byte of the data field
- High byte of the data field
- Status field
- CRC field

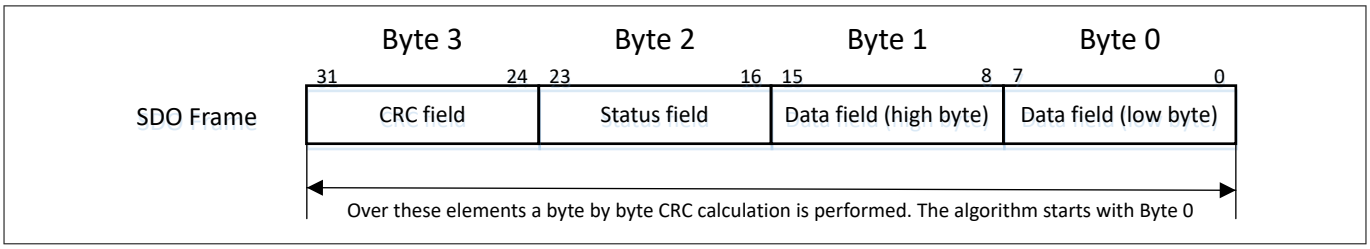


Figure 88 Byte order for SAE J1850 CRC check

Example:

If the microcontroller receives the frame in Figure 89, then the CRC algorithm (see Chapter 14.1.2.5) requires the following input parameter:

- Input bytefield parameter data: {$F2_H$, 01_H, 83_H, 37_H}
- Input parameter length: 4

The result of the CRC check must always be $3B_H$. Any other value means that the frame is corrupt. The value $3B_H$ is called magic number in the AUTOSAR CRC specification.

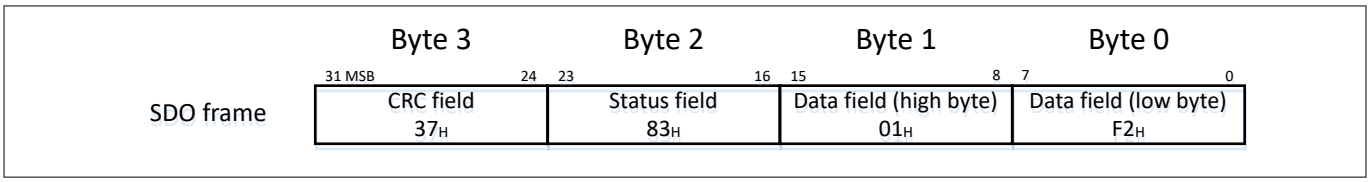


Figure 89 SDO frame example

14.1.2.5.2 CRC device handling

CRC calculation

The CRC calculation includes the following SDO frame elements (Figure 90):

- Low byte of the data field
- High byte of the data field
- Status field

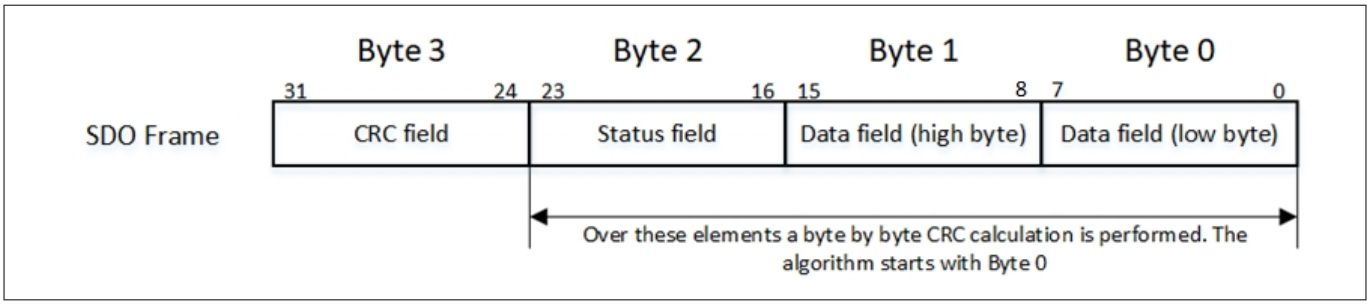


Figure 90 Byte order for SAE J1850 CRC calculation

If the status field has the value 83_H and the data field has the value $01F2_H$, the CRC algorithm (see Chapter 14.1.2.5) requires the following input parameters:

- Input bytefield parameter data: {$F2_H$, 01_H, 83_H}
- Input parameter length: 3

The result of the CRC calculation is 37_H.

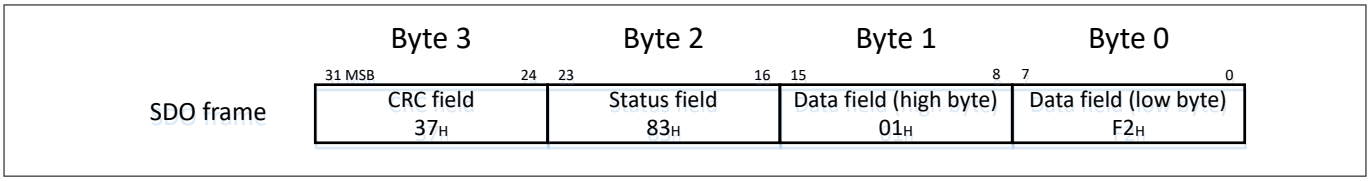


Figure 91 SDO frame example

CRC check

The CRC check includes the following SDI frame elements (Figure 92):

- Low byte of the data field
- High byte of the data field
- Address field
- CRC field

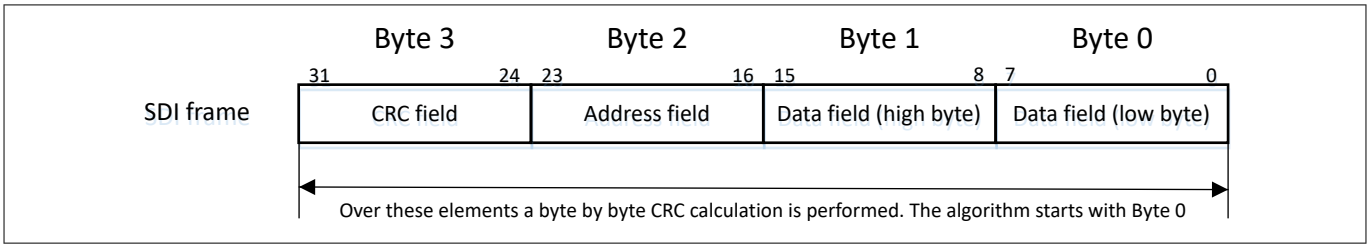


Figure 92 Byte order for SAE J1850 CRC calculation

Example:

If the device receives the frame in Figure 93, then the CRC algorithm (see Chapter 14.1.2.5) requires the following input parameter:

- Input bytefield parameter data: {$F2_H$, 01_H, 83_H, 37_H}
- Input parameter length: 4

The result of the CRC check is always $3B_H$. A different value implies that the frame is corrupt. The value $3B_H$ is called magic number in the AUTOSAR CRC specification.

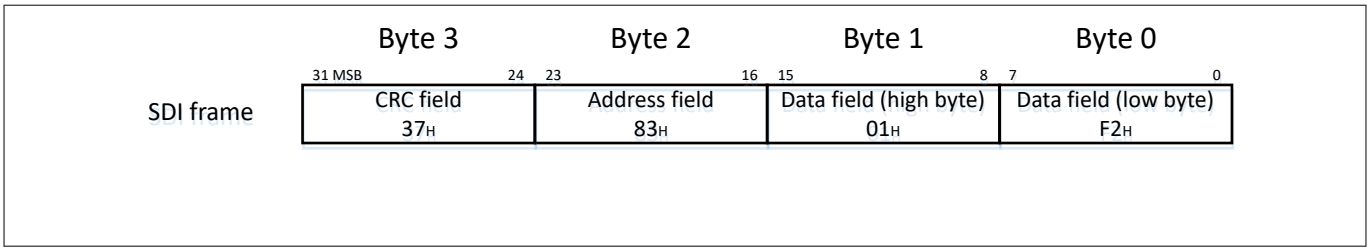


Figure 93 SDI frame example

14.1.2.6 Status field

Figure 94 shows the structure of the status field. The following chapters defines the functionality of the status field bits in detail.

BIT number in the SDI frame of a reponse command

23	22	21	20	19	18	17	16
Res	LFOK	Can be defined by the product					

Figure 94 Structure of the status field

The device implements the following bit fields in the SDO frame status field bits 21 to 16:

Table 46 Device specific status field

Bit number referred to SDO frame	Bit number referred to status field	Function
[21]	[5]	**INTMISS:** Flag for interrupt not serviced in time t_{INTx_to}
[20]	[4]	**MON:** Flag for monitor interrupt (IF1.MON)
[19]	[3]	**OTW:** Flag for overtemperature warning interrupt (IF1.OTW)
[18]	[2]	**CL2ERR:** Flag for fault detected on WWD2, FWD2 or ERR2
[17]	[1]	**CL1ERR:** Flag for fault detected on WWD1, FWD1 or ERR1
[16]	[0]	**ERRMISS:** Flag for fault detected on any ERR[x]

Note:
The status flag only is updated upon arrival/request of the last frame.

14.1.2.6.1 Last frame OK (LFOK)

Table 47 Last frame OK

Encoding	Description
0_b	Error encountered in the SDI frame of last request frame
1_b	Read service or write service successfully executed

The error handling and the reason for an LFOK = 0 are described in Chapter 14.1.2.7.

Note:
It is recommended to check the status of LFOK before processing SPI frame independent of INT

14.1.2.7 Error mechanism

In case a failure happens in the SPI communication (see Table 48), the LFOK bit is set to "0" (see Table 47). In this case the response SPI transfer contains a error code. Figure 95 shows the structure of the response SPI transfer.

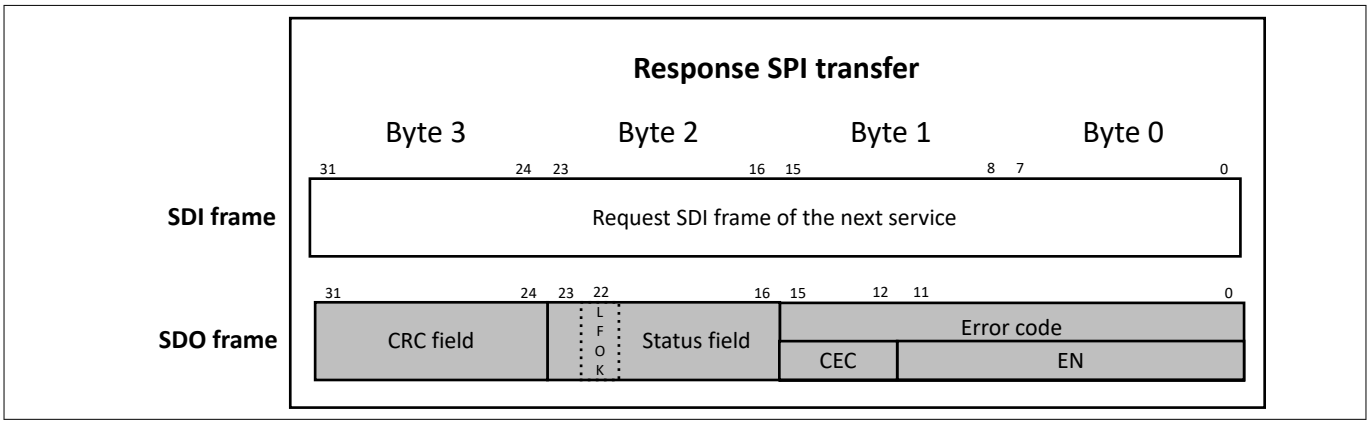


Figure 95 Error response SPI transfer

The error code consists of the following items:

- Communication error code (CEC)
- Error number (EN which is only used for internal usage)

Table 48 SPI communication failure

CEC	Description
0x0	reserved
0x1	Frame error detected - frame frame length invalid of previous SPI communication - frame ignored
0x2	CRC error detected - frame ignored
0x3	reserved
0x4	Access to none existing register (if SPI interframe is >5.2 us) If SPI interframe is <5.2 us an error frame of 0xF1000000 can be responded instead
0x5	reserved
0x6	reserved
0x7	Internal error while accessing a register

***Note**: In case a communication error code is received which is not listed, contact customer support, please.*

14.1.2.8 SPI response with MPS ON

If MPS is enabled and MCU fails servicing ERRs/WDs, the device moves to INIT and performs the initialization sequence with RESOUT high.

Due to the initialization activity after the move to INIT event, there is a window of maximum 75µs, in which the SDO response needs longer (2.5 µs) to be available. If the SPI interframe space is shorter, the response on SDO has a 0xF1000000 error frame ("no data available") when the next SPI frame is transferred, even though the request is executed. Software can implement one out of the following countermeasures to avoid the error frame condition:

- Increase interframe space to 2.5 µs (typ.)

- Make SPI handler robust on receiving the error frame
- If there is a fault injection test on ERRs and WDs it is suggested to avoid SPI communication from the point of fault injection until 75µs after SSO1 decreases. Due to analog delays SSO1 decreases up to 30 µs after the actual move to INIT event.

14.2 Electrical characteristics SPI

Table 49 Electrical characteristics SPI

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SPI timing							
SPI frequency	f_{SPI}	–	–	10	MHz	1)	DS-1577
CSN leading delay	t_{CSN_LDEL}	200	–	–	ns	1)	DS-2075
CSN trailing delay	t_{CSN_TDEL}	100	–	–	ns	1)	DS-1579
Interframe time	t_{IF}	1	–	–	µs	CSN rising to CSN falling edge 1)	DS-1580
SCK setup low time	t_{SCK_SETL}	100	–	–	ns	1)	DS-1581
SCK clock high time	t_{SCK_H}	45	–	–	ns	1)	DS-1582
SCK clock low time	t_{SCK_L}	45	–	–	ns	1)	DS-1583
SCK hold low time	t_{SCK_HDL}	100	–	–	ns	1)	DS-1584
SDI data setup time	t_{SDI_SET}	10	–	–	ns	1)	DS-1585
SDI data hold time	t_{SDI_HOLD}	10	–	–	ns	1)	DS-1586
SDO enable time	t_{SDO_EN}	–	–	50	ns	1)	DS-1587
SDO valid delay time (high frequency)	t_{SDO_VDEL}	–	–	136	ns	$C_{SDO,load}$ = 50 pF; f_{SPI} < 1 MHz 1)	DS-1588
SDO valid delay time (high frequency)	t_{SDO_VDEL}	–	–	36 + 0.1/ f_{SPI}	ns	$C_{SDO,load}$ = 50 pF; 1 MHz ≤ f_{SPI} ≤ 10 MHz 1)	DS-1589
SDO disable time	t_{SDO_DIS}	–	–	100	ns	1)	DS-1590
SPI input signal rise time (SDI, SCK, CSN)	$t_{SPI,r}$	–	–	100	ns	f_{SPI} < 1 MHz; Parameter applicable to all SPI input pins SDI, SCK and CSN 1)	DS-1591
SPI input signal rise time (SDI, SCK, CSN)	$t_{SPI,r}$	–	–	0.1/ f_{SPI}	ns	1 MHz ≤ f_{SPI} ≤ 10 MHz; Parameter applicable to all SPI input pins SDI, SCK and CSN 1)	DS-1592
SPI input signal fall time (SDI, SCK, CSN)	$t_{SPI,f}$	–	–	100	ns	f_{SPI} < 1 MHz; Parameter applicable to all SPI input pins SDI, SCK and CSN 1)	DS-1593

(table continues...)

Table 49 (continued) Electrical characteristics SPI

V_{VS} = 6.0 V to 36 V, T_j = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SPI input signal fall time (SDI, SCK, CSN)	$t_{SPI,f}$	–	–	0.1/ f_{SPI}	ns	1 MHz ≤ f_{SPI} ≤ 10 MHz; Parameter applicable to all SPI input pins SDI, SCK and CSN 1)	DS-1594
SPI microcontroller interface							
SPI input voltage high level	V_{SPI_H}	2	–	V_{QUC}	V	V_{SPI} increasing, V_{QUC} ≥ V_{QUC} [Min]; Parameter applicable to all SPI input pins SDI, SCK and CSN	DS-1596
SPI input voltage low level	V_{SPI_L}	0	–	0.8	V	V_{SPI} decreasing; Parameter applicable to all SPI input pins SDI, SCK and CSN	DS-1597
SPI input voltage hysteresis	V_{SPI_HYS}	–	200	–	mV	V_{QUC} = V_{QUC} [Typ]; Parameter applicable to all SPI input pins SDI, SCK and CSN	DS-1599
SPI input capacitance	C_{SPI}	–	4	15	pF	Parameter applicable to all SPI input pins SDI, SCK and CSN 1)	DS-1600
CSN pull-up current	I_{CSN}	-180	-55	–	µA	V_{CSN} ≤ V_{QUC}[Typ] 1)	DS-1601
SCK pull-down current	I_{SCK}	–	135	330	µA	V_{SCK} ≤ V_{QUC}[Typ] 1)	DS-1602
SDI pull-down current	I_{SDI}	–	135	330	µA	V_{SDI} = V_{QUC} 1)	DS-1603
SDO output voltage high level	V_{SDO_H}	2	–	–	V	V_{QUC} ≥ V_{QUC}[Min]; I_{SDO} = -7 mA 1)	DS-1605
SDO output voltage low level	V_{SDO_L}	–	–	0.7	V	I_{SDO} = 5.5 mA 1)	DS-1606
SDO tristate capacitance	C_{SDO}	–	4	15	pF	1)	DS-1607
SDO tristate leakage current	I_{SDO_leak}	-10	–	10	µA	1)	DS-1608

1) Not subject to production test, specified by design

15 Reset classes

There are in total 6 reset classes. Each bitfield is assigned to one of these six reset classes and is reset to its reset value accordingly upon an occurrence of the events listed in the reset class. The reset classes are set up in a way so that the next higher reset class fully includes the lower reset class (for example: R3 contains R2, R2 contains R1,...).

15.1 R0 - Reset class

Bitfields assigned to reset class R0 are reset to their reset value upon occurrence of the following events:

- POR (power on reset, disconnect battery)
- STANDBY no WUT AND no QST active (entering STANDBY state without activating the wake-up timer nor using the standby voltage regulator QST)

15.2 R1 - Reset class

Bitfields assigned to reset class R1 are reset to their reset value upon occurrence of the following events:

- POR
- STANDBY no WUT AND no QST active
- STANDBY

15.3 R2 - Reset class

Bitfields assigned to reset class R2 are reset to their reset value upon occurrence of the following events:

- POR
- STANDBY no WUT AND no QST active
- STANDBY
- FAILSAFE

15.4 R3 - Reset class

Bitfields assigned to reset class R3 are reset to their reset value upon occurrence of the following events:

- POR
- STANDBY no WUT AND no QST active
- STANDBY
- FAILSAFE
- RESOUT pulled low
- INIT (entering INIT state)

15.5 R3_C1 - Reset class

Bitfields assigned to reset class R3_C1 are reset to their reset value upon occurrence of the following events:

- POR
- STANDBY no WUT AND no QST active
- STANDBY
- FAILSAFE
- RESOUT pulled low
- INIT
- REDUCED OPERATION (entering REDUCED OPERATION caused by a application 1 fault)

Registers and bitfields that belong to this reset class are:

- ERR1_RS_CFG

- WD1_RS_CFG0
- WD1_RS_CFG1
- FWD1_RS_HBTP_CFG
- WWD1_RS_CW_CFG
- WWD1_RS_OW_CFG
- FWD1_STAT
- WWD1_ECNT_STAT

15.6 R3_C2 - Reset class

Bitfields assigned to reset class R3_C2 are reset to their reset value upon occurrence of the following events:

- POR
- STANDBY no WUT AND no QST active
- STANDBY
- FAILSAFE
- RESOUT pulled low
- INIT
- REDUCED OPERATION (entering REDUCED OPERATION caused by a application 2 fault)

Registers and bitfields that belong to this reset class are:

- ERR2_RS_CFG
- WD2_RS_CFG0
- WD2_RS_CFG1
- FWD2_RS_HBTP_CFG
- WWD2_RS_CW_CFG
- WWD2_RS_OW_CFG
- FWD2_STAT
- WWD2_ECNT_STAT

16 Collection registers, error reporting and clearance of bitfields

The device provides error registers that are being set if respective error events occur (see Reaction on faults). To simplify the diagnosis procedure collection registers are implemented which bundle a group of error registers and only set one bit in the collection registers. By providing this piece of information it allows the integrator in a first step to only read the collection registers and follow the path of the error report, instead of always reading all error registers. The entire set up is available in a doubled up structure in case REDUCED OPERATION is enabled and two application threads access the information. If REDUCED OPERATION is not used, these doubled up registers are inactive and won't feedback any reliable result.

Failure and error bits are cleared by writing the respective bit with "1". Any other read and write access stays without effect.

In addition, the overview of the error reporting provides the assignment to the error classes used. In general, there is a distinction between a severe fault (xx_SEV_FAULT) and a warning fault (xx_WARN_FAULT).

Severe fault:

A severe fault is associated with a critical event in either the device or the system parameters monitored by the device, that could have caused the application to become unreliable and already is unreliable and must not be allowed to enter normal operation. Depending on the fault several recovery attempts such as a soft reset, a hard reset or a move to FAILSAFE will take place. In any case the signals SSO1/2 will be issued to indicated that the application cannot be assumed to be fully functional and must be brought into a safe state.

Warning fault:

A warning is associated with an event in either the device or the system parameters monitored by the device, which do not directly jeopardise the normal functionality of the application. A warning fault is indicated by issuing an interrupt. The application, however, remains in a normal functionality and no safe state is indicated via SSO1/2.

16.1 Error reporting generating an interrupt

Errors that trigger an interrupt (INT) are collected in the IFx register. Events that are bundled in this registers are listed in the following table.

Table 50 Errors generating an interrupt - Collection register: IF1

IF1 bitfield	Error register	Error class	Error bitfield	Description
SYSFAIL_ERR	SYS_STAT_APP1	ERRx_WARN_FAULT	ERR0_ERR	ERR0 monitoring error AND ERR0 recovery is enabled
			ERR1_ERR	ERR1 monitoring error AND ERR1 recovery is enabled
		WDx_WARN_FAULT	WWD1_ERR	WWD1 missed or incorrect service (error counter below threshold)
			FWD1_ERR	FWD1 response missed or incorrectly triggered (error counter below threshold)
		SYS_WARN_FAULT		

(table continues...)

Table 50 (continued) Errors generating an interrupt - Collection register: IF1

IF1 bitfield	Error register	Error class	Error bitfield	Description
			FSM_NOOP	State transition not existing or transition conditions not fulfilled.
			FSM_TRFAIL	State transition into low power state (STANDBY or SLEEP) failed/interrupted (e.g. by WAK or ENA)
			BUCKCORE_SVS_NOK	Static voltage scaling not performed due to: - Device being no in INIT or NORMAL - BUCKCORE voltage set to 1.15 V
			BUCKCORE_SVS_OK	Static voltage scaling completed successfully.
			APP2_FAIL	Application 2 was reason for entering REDUCED OPERATION
WUT_EVT	WAKE_STAT_APP1	WAKE_EVENT	ENA	ENA signal detected
			WAK	WAK signal detected
			WUT	Wake-up timer (WUT) expired and woke up the device
			SPI	SPI command woke up the device
SPI_FAIL	SPI_FAIL_STAT_APP1	SPI_WARN_FAULT	LOCK	Lock of protected registers was unsuccessful
			CRC	CRC wrong
			FR_LEN	Frame length wrong
			ADR	Invalid address
			CS_TO	CSN timeout after 2 ms
MON	STG_STAT_APP1	VMON_WARN_FAULT	BUCKIF	Short to ground at BUCKIF BUCKIF is switched off

(table continues...)

Table 50 (continued) Errors generating an interrupt - Collection register: IF1

IF1 bitfield	Error register	Error class	Error bitfield	Description
			QCO	Short to ground at QCO QCO is switched off
			QVR	Short to ground at QVR QVR is switched off
			VMON1	Short to ground at VMON1 VMON1 rail is disabled
			VMON2	Short to ground at VMON2 VMON2 rail is disabled
	UV_STAT_APP1		PREREG	Undervoltage at PREREG
			BOOST	Undervoltage at BOOST
			QCO	Undervoltage at QCO
			BUCKIF	Undervoltage at BUCKIF
			QVRUV	Undervoltage at QVR
			VMON1	Undervoltage at VMON1
			VMON2	Undervoltage at VMON2
	INTSUP_STAT_APP1		PMU_RED	Internal error; Always needs to be read when waking up from FAILSAFE (IF register is not being set in FAILSAFE but INTSUP_STAT_APPx could have been set)
			PMU_MAIN	Internal error; Always needs to be read when waking up from FAILSAFE (IF register is not being set in FAILSAFE but INTSUP_STAT_APPx could have been set)

(table continues...)

Table 50 (continued) Errors generating an interrupt - Collection register: IF1

IF1 bitfield	Error register	Error class	Error bitfield	Description
			BG12_OV	Internal error; Always needs to be read when waking up from FAILSAFE (IF register is not being set in FAILSAFE but INTSUP_STAT_APPx could have been set)
			BG12_UV	Internal error; Always needs to be read when waking up from FAILSAFE (IF register is not being set in FAILSAFE but INTSUP_STAT_APPx could have been set)
OT_WRN_OC_ERR	OT_WRN_OC_STAT_APP1	OTOC_WARN_FAULT	IVCC_OC	Internal error
			QST_OC	QST overcurrent
			BUCKCORE_OTWRN	BUCKCORE overtemperature warning
			BUCKIF_OTWRN	BUCKIF overtemperature warning
			BOOST_OTWRN	BOOST overtemperature warning
			BOOST_OC	BOOST overcurrent
			QUC_OTWRN	QUC overtemperature warning
			QCO_OTWRN	QCO overtemperature warning
			QVR_OC	QVR overcurrent
ABIST	-	ABIST_WARN_FAULT	-	ABIST finished execution
INTMISS	-	-	-	Interrupt flags not cleared after tINTx_to

(x = 1; 2)

If REDUCED OPERATION is enabled, also the following bits are set:

Table 51 Errors generating an interrupt - Reduced Operation - Collection register: IF2

IF2 bitfield	Error register	Error class	Error bitfield	Description
SYSFAIL_ERR	SYS_STAT_APP2	ERRx_WARN_FAULT	ERR0_ERR	ERR0 monitoring error
			ERR2_ERR	ERR2 monitoring error AND ERR2 recovery is enabled
		WDx_WARN_FAULT	WWD2_ERR	WWD2 missed or incorrect service (error counter below threshold)
			FWD2_ERR	FWD2 response missed or incorrectly triggered (error counter below threshold)
		SYS_WARN_FAULT	FSM_NOOP	State transition not existing or transition conditions not fulfilled.
			FSM_TRFAIL	State transition into low power state (STANDBY or SLEEP) failed/interrupted (e.g. by WAK or ENA)
			BUCKCORE_SVS_NOK	Static voltage scaling not performed due to: - Device being not in INIT or NORMAL - BUCKCORE voltage set to 1.15 V
			BUCKCORE_SVS_OK	Static voltage scaling completed successfully.
			APP1_FAIL	Cluster 1 was reason for entering REDUCED OPERATION
WUT_EVT	WAKE_STAT_APP2	WAKE_EVENT	ENA	ENA signal detected
			WAK	WAK signal detected
			WUT	Wake-up timer (WUT) expired and woke up the device

(table continues...)

Table 51 (continued) Errors generating an interrupt - Reduced Operation - Collection register: IF2

IF2 bitfield	Error register	Error class	Error bitfield	Description
			SPI	SPI command woke up the device
SPI_FAIL	SPI_FAIL_STAT_APP2	SPI_WARN_FAULT	LOCK	Lock of protected registers was unsuccessful
			CRC	CRC wrong
			FR_LEN	Frame length wrong
			ADR	Invalid address
			CS_TO	CSN timeout after 2 ms
MON	STG_STAT_APP2	VMON_WARN_FAULT	BUCKIF	Short to ground at BUCKIF BUCKIF is switched off
			QCO	Short to ground at QCO QCO is switched off
			QVR	Short to ground at QVR QVR is switched off
			VMON1	Short to ground at VMON1 VMON1 rail is disabled
			VMON2	Short to ground at VMON2 VMON2 rail is disabled
	UV_STAT_APP2		PREREG	Undervoltage at PREREG
			BOOST	Undervoltage at BOOST
			QCO	Undervoltage at QCO
			BUCKIF	Undervoltage at BUCKIF
			QVR	Undervoltage at QVR
			VMON1	Undervoltage at VMON1
			VMON2	Undervoltage at VMON2

(table continues...)

Table 51 (continued) Errors generating an interrupt - Reduced Operation - Collection register: IF2

IF2 bitfield	Error register	Error class	Error bitfield	Description
	INTSUP_STAT_APP2		PMU_RED	Internal error; Always needs to be read when waking up from FAILSAFE (IF register is not being set in FAILSAFE but INTSUP_STAT_APPx could have been set)
			PMU_MAIN	Internal error; Always needs to be read when waking up from FAILSAFE (IF register is not being set in FAILSAFE but INTSUP_STAT_APPx could have been set)
			BG12_OV	Internal error; Always needs to be read when waking up from FAILSAFE (IF register is not being set in FAILSAFE but INTSUP_STAT_APPx could have been set)
			BG12_UV	Internal error; Always needs to be read when waking up from FAILSAFE (IF register is not being set in FAILSAFE but INTSUP_STAT_APPx could have been set)
OT_WRN_OC_ERR	OT_WRN_OC_STAT_APP2	OTOC_WARN_FAULT	IVCC_OC	Internal error
			QST_OC	QST overcurrent
			BUCKCORE_OTWRN	BUCKCORE overtemperature warning
			BUCKIF_OTWRN	BUCKIF overtemperature warning
			BOOST_OTWRN	BOOST overtemperature warning

(table continues...)

Table 51 (continued) Errors generating an interrupt - Reduced Operation - Collection register: IF2

IF2 bitfield	Error register	Error class	Error bitfield	Description
			BOOST_OC	BOOST overcurrent
			QUC_OTWRN	QUC overtemperature warning
			QCO_OTWRN	QCO overtemperature warning
			QVR_OTWRN	QVR overcurrent
ABIST	-	ABIST_WARN_FAULT	-	ABIST finished execution
INTMISS	-	-	-	Interrupt flags not cleared after tINTx_to

(x = 1; 2)

16.2 Error reporting causing a move to INIT or REDUCED OPERATION

Errors that trigger a move to INIT usually also trigger a reset (RESOUT) and are collected in the INIT_ERR_APPx register. Events that are bundled in this registers are listed in the following table. For MPS (see Microcontroller programming support (MPS)) enabled, some move to INITs do not issue an reset.

Table 52 Errors causing a move to INIT - Collection register: INIT_ERR_APP1

INIT_ERR_APP1 bitfield	Error class	Error register	Error bitfield	Description
VMONF	VMONUV_SEV_FAULT	UV_STAT_APP1	BUCKCORE	BUCKCORE undervoltage
			QUC	QUC undervoltage
			QST	QST undervoltage
WWD1_EC	WDx_SEV_FAULT	-	-	WWD1 incorrectly triggered and error counter reaches threshold
WWD2_EC		-	-	WWD2 incorrectly triggered and error counter reaches threshold
FWD1_EC		-	-	FWD1 incorrectly triggered and error counter reaches threshold

(table continues...)

Table 52 (continued) Errors causing a move to INIT - Collection register: INIT_ERR_APP1

INIT_ERR_APP1 bitfield	Error class	Error register	Error bitfield	Description
FWD2_EC		-	-	FWD2 incorrectly triggered and error counter reaches threshold
ERR1	ERRx_SEV_FAULT	-	-	ERR1 signal is outside of valid frequencies (if recovery enabled: longer than tREC before being set)
ERR2		-	-	ERR2 signal is outside of valid frequencies (if recovery enabled: longer than tREC before being set)
REDOP_RES1	INITTIMER_SEV_FAULT	-	-	INIT timer expired the first time in RED. OP. due to application 1 not being able to reinitialize
REDOP_RES2		-	-	INIT timer expired a second time in RED. OP.
SOFTRES		-	-	INIT timer expires 1st time → Soft reset issued
HARDRES		-	-	INIT timer expires 2nd time consecutively → Hard reset issued

(x = 1; 2)

If REDUCED OPERATION is enabled, also the following bits are set:

Table 53 Errors causing a move to INIT - Reduced Operation - Collection register: INIT_ERR_APP2

INIT_ERR_APP2 bitfield	Error class	Error register	Error bitfield	Description
VMONF	VMONUV_SEV_FAULT	UV_STAT_APP1	BUCKCORE	BUCKCORE undervoltage
			QUC	QUC undervoltage

(table continues...)

Table 53 (continued) Errors causing a move to INIT - Reduced Operation - Collection register: INIT_ERR_APP2

INIT_ERR_APP2 bitfield	Error class	Error register	Error bitfield	Description
			QST	QST undervoltage
WWD1_EC	WDx_SEV_FAULT	—	—	WWD1 incorrectly triggered and error counter reaches threshold
WWD2_EC		—	—	WWD2 incorrectly triggered and error counter reaches threshold
FWD1_EC		—	—	FWD1 incorrectly triggered and error counter reaches threshold
FWD2_EC		—	—	FWD2 incorrectly triggered and error counter reaches threshold
ERR1	ERRx_SEV_FAULT	—	—	ERR1 signal is outside of valid frequencies (if recovery enabled: longer than tREC before being set)
ERR2		—	—	ERR2 signal is outside of valid frequencies (if recovery enabled: longer than tREC before being set)
REDOP_RES1	INITTIMER_SEV_FAULT	—	—	INIT timer expired the first time in RED. OP. due to application 2 not being able to reinitialize
REDOP_RES2		—	—	INIT timer expired a second time in RED. OP.
SOFTRES		—	—	INIT timer expires 1st time → Soft reset issued

(table continues...)

Table 53 (continued) Errors causing a move to INIT - Reduced Operation - Collection register: INIT_ERR_APP2

INIT_ERR_APP2 bitfield	Error class	Error register	Error bitfield	Description
HARDRES		—	—	INIT timer expires 2nd time consecutively → Hard reset issued

(x = 1; 2)

16.3 Error reporting causing a move to FAILSAFE

Errors that trigger a move to FAILSAFE are collected in the register. Only exception is the bit ABIST. It is being set only, if during an ABIST execution an error occurs that moves the device into INIT or FAILSAFE and is by itself no trigger for a state transition.

Table 54 Errors causing a move to FAILSAFE - Collection register: SYSFAIL_STAT_APP1

SYSFAIL_STAT_APP1 bitfield	Error class	Error register	Error bitfield	Description
QST_QUC_VOLTSEL	VOLTSEL_SEV_FAULT	-	-	Voltage selection error. 5 V or 3.3 V might be corrupt and not correctly selected.
BUCKIF_VOLTSEL		-	-	Voltage selection error. 1.8 or 3.3 V might be corrupt and not correctly selected.
BUCK_CORE_VOLTSEL		-	-	Voltage selection error. Core voltage might be corrupt.
OT	OT_SEV_FAULT	OT_STAT_APP1	BUCKCORE	BUCKCORE thermal shutdown
			BUCKIF	BUCKIF thermal shutdown
			BOOST	BOOST thermal shutdown
			QUC	QUC thermal shutdown
			QCO	QCO thermal shutdown
			SAFETY_AREA	Overtemperature of safety area

(table continues...)

Table 54 (continued) Errors causing a move to FAILSAFE - Collection register: SYSFAIL_STAT_APP1

SYSFAIL_STAT_APP1 bitfield	Error class	Error register	Error bitfield	Description
VMON	VMON_SEV_FAULT	STG_STAT_APP1	BUCKCORE	BUCKCORE short to ground
			BOOST	BOOST short to ground & Severe undervoltage
			QUC	QUC short to ground
			QST	QST short to ground
			PREREG	PREREG short to ground & Severe undervoltage
		OV_STAT_APP1	BUCKCORE	Severe overvoltage at BUCKCORE & BUCKCORE OV
			BUCKCORE_FB_OPEN	Feedback open
			PREREG	Severe overvoltage at PREREG & PREREG OV
			BUCKIF	Severe overvoltage at BUCKIF & BUCKIF OV
			BOOST	BOOST OV
			QUC	QUC OV
			QCO	QCO OV
			QVR	QVR OV
			QST	QST OV
			VMON1	VMON1 OV
			VMON2	VMON2 OV
			INTSUP_VDD2V5	Internal 2V5 rail overvoltage
			INTSUP_IVCC	Internal IVCC overvoltage
		UV_STAT_APP1	INTSUP_VDD2V5_UV	Internal 2V5 rail undervoltage
			INTSUP_IVCC_UV	Internal IVCC undervoltage

(table continues...)

Table 54 (continued) Errors causing a move to FAILSAFE - Collection register: SYSFAIL_STAT_APP1

SYSFAIL_STAT_APP1 bitfield	Error class	Error register	Error bitfield	Description
		INTSUP_STAT_APP1	BIAS_HI	Internal bias current too high
			BIAS_LOW	Internal bias current too low
			VBAT_OV	VS OV
FSM_INITTIMER	INITTIMER_SEV_FAULT	-	-	FAILSAFE was entered because INIT timer expired a 3rd time without successful initialization.
ERR0	ERR0_SEV_FAULT	-	-	FAILSAFE was entered after ERR0 reported invalid frequency.
QST	QST_SEV_FAULT	-	-	Set for: QST BIST errors, severe overvoltage
INTSUP_IVCC	INTSUP_SEV_FAULT	-	-	Set for: QIS BIST errors, severe overvoltage
PREREG_COSW	SSW_SEV_FAULT	-	-	BIST major error SSC or SSW was activated during normal operation
CFGE	CFG_SEV_FAULT	-	-	Double Error detected on a protected register
ABIST	ABIST_SEV_FAULT	-	-	Any error that moves the device to FAILSAFE or INIT and is not part of the ABIST routine will abort the on-going ABIST and set this bit.

(x = 1; 2)

If REDUCED OPERATION is enabled, also the following bits are set:

Table 55 Errors causing a move to FAILSAFE - Reduced Operation - Collection register: SYSFAIL_STAT_APP2

SYSFAIL_STAT_APP2 bitfield	Error class	Error register	Error bitfield	Description
QST_QUC_VOLTSEL	VOLTSEL_SEV_FAULT	-	-	Voltage selection error. 5 V or 3.3 V might be corrupt and not correctly selected.
BUCKIF_VOLTSEL		-	-	Voltage selection error. 1.8 V or 3.3 V might be corrupt and not correctly selected.
BUCK_CORE_VOLTSEL		-	-	Voltage selection error. Core voltage might be corrupt.
OT	OT_SEV_FAULT	OT_STAT_APP2	BUCKCORE	BUCKCORE thermal shutdown
			BUCKIF	BUCKIF thermal shutdown
			BOOST	BOOST thermal shutdown
			QUC	QUC thermal shutdown
			QCO	QCO thermal shutdown
			SAFETY_AREA	Overtemperature of safety area
VMON	VMON_SEV_FAULT	STG_STAT_APP2	BUCKCORE	BUCKCORE short to ground
			BOOST	BOOST short to ground & severe undervoltage
			QUC	QUC short to ground
			QST	QST short to ground
			PREREG	PREREG short to ground & severe undervoltage
		OV_STAT_APP2	BUCKCORE	Severe overvoltage at BUCKCORE & BUCKCORE OV

(table continues...)

Table 55 (continued) Errors causing a move to FAILSAFE - Reduced Operation - Collection register: SYSFAIL_STAT_APP2

SYSFAIL_STAT_APP2 bitfield	Error class	Error register	Error bitfield	Description
			BUCKCORE_FB_OPEN	Feedback open
			PREREG	Severe overvoltage at PREREG & PREREG OV
			BUCKIF	Severe overvoltage at BUCKIF & BUCKIF OV
			BOOST	BOOST OV
			QUC	QUC OV
			QCO	QCO OV
			QVR	QVR OV
			QST	QST OV
			VMON1	VMON1 OV
			VMON2	VMON2 OV
			INTSUP_VDD2V5	Internal 2V5 rail overvoltage
			INTSUP_IVCC	Internal IVCC overvoltage
		UV_STAT_APP2	INTSUP_VDD2V5_UV	Internal 2V5 rail undervoltage
			INTSUP_IVCC_UV	Internal IVCC undervoltage
		INTSUP_STAT_APP2	BIAS_HI	Internal bias current too high
			BIAS_LOW	Internal bias current too low
			VBAT_OV	VS OV
FSM_INITTIMER	INITTIMER_SEV_FAULT	-	-	FAILSAFE was entered because INIT timer expired a 3rd time without successful initialization.
ERR0	ERR0_SEV_FAULT	-	-	FAILSAFE was entered after ERR0 reported invalid frequency.

(table continues...)

Table 55 (continued) Errors causing a move to FAILSAFE - Reduced Operation - Collection register: SYSFAIL_STAT_APP2

SYSFAIL_STAT_APP2 bitfield	Error class	Error register	Error bitfield	Description
QST	QST_SEV_FAULT	-	-	Set for: QST BIST errors, severe overvoltage
INTSUP_IVCC	INTSUP_SEV_FAULT	-	-	Set for: QIS BIST errors, severe overvoltage
PREREG_COSW	SSW_SEV_FAULT	-	-	BIST major error SSC or SSW was activated during normal operation
CFGE	CFG_SEV_FAULT	-	-	Double error detected on a protected register
ABIST	ABIST_SEV_FAULT	-	-	Any error that moves the device to FAILSAFE or INIT and is not part of the ABIST routine will abort the on-going ABIST and set this bit.

(x = 1; 2)

16.4 Status reporting - Miscellaneous registers

Device status information are collected in VMON_STAT and DEV_STAT.

	Status bitfield	Description
VMON_STAT	all	Indicates whether voltage regulators are within range or outside of it. If a regulator is switched off the bits read as 0.
DEV_STAT	all	Provides an overview of the devices general state (e.g. Enabled regulators, State, Autodetection)

17 Protected registers - Protected write and reflected status registers

The device contains protected registers to avoid unintentional access to safety related parameters. A protected register always consists of a pair of a configurable "protected write" register and its corresponding "reflected status" shadow register. These registers first need to be unlocked before new content can be written. New content must always be written to the protected write register. In order for new changes take effect, the registers have to be locked again. With the lock sequence new content is transferred to the reflected status registers.

Registers that belong to the class of protected registers are labeled as below in their names:

Protected write	*<registername>*_PW_*<registername>*
Reflected status	*<registername>*_RS_*<registername>*

17.1 Unlock/lock sequence

To unlock and lock protected register, the following steps must be executed:

1. Unlock registers: Write 0xB5CA to register **PROT_CFG.KEY**
2. Write changes to protected write registers
3. Lock registers: Write 0xD396 to register **PROT_CFG.KEY**

Before writing changes to protected write registers and checking whether changes took effect by reading reflected status registers, the current lock status of the protected registers can be read in **PROT_STAT.LOCK**. In addition the error bit SPI_FAIL_STAT_APP1.LOCK is set in case something went wrong during the unlock/lock sequence. In such case written values will not become effective and RS registers are not updated. If REDUCED OPERATION is enabled also SPI_FAIL_STAT_APP2.LOCK is set.

18 Registers description

18.1 Registers overview - OTHERSR2 (ascending offset address)

Table 56 Registers overview - OTHERSR2 (ascending offset address)

Short name	Long name	Offset address	See
DEV_CFG4	Device configuration 4 *R2)	000_H	210
REDOP_RS_CFG2	Reduced operation reflected status configuration 2 register - *R2)	001_H	212
PROT_CFG	Protection configuration register - *R2)	002_H	213
DEV_RS_CFG3	Device reflected status configuration Register *R2)	003_H	214
WUT_CFG0	Wake up timer LSB Value (*R2)	004_H	216
WUP_CFG1	Wake up timer MSB Value (*R2)	005_H	217
WAKE_STAT_APP1	Wakeup status flags for Application 1 *R2)	006_H	218
WAKE_STAT_APP2	Wakeup status flags for Application 2 *R2)	007_H	219
INIT_ERR_APP1	INIT and REDUCED OPERATION Error Status flags for Application 1 *R2)	008_H	220
INIT_ERR_APP2	INIT and REDUCED OPERATION Error Status flags for Application 2 *R2)	009_H	222
IF1	Interrupt flags for Application 1 that trigger INT1 *R2)	$00A_H$	224
IF2	Interrupt flags for Application 2 that trigger INT2 *R2)	$00B_H$	226
SYS_STAT_APP1	System status flags for Application 1 that trigger INT1 *R2)	$00C_H$	228
SYS_STAT_APP2	System status flags for Application 2 that trigger INT2 *R2)	$00D_H$	230
SPI_FAIL_STAT_APP1	SPI failure status flags that triggers INT1 *R2)	$00E_H$	232
SPI_FAIL_STAT_APP2	SPI status flags for Application 2 that trigger INT2 *R2)	$00F_H$	233
UV_STAT_APP1	Monitor status flags register 2 for Application 1 *R2)	010_H	234
UV_STAT_APP2	Monitor status flags register 2 for Application 2 *R2)	011_H	236
OT_WRN_OC_STAT_APP1	Over temperature warning and over current status flags *R2)	012_H	238
OT_WRN_OC_STAT_APP2	Over temperature warning /Over current status flags for Application 2 *R2)	013_H	240
VMON_STAT	Voltage monitor status *R2)	014_H	242
DEV_STAT	Device status register *R2)	015_H	244
DCDC_FREQ_SYNC	DC-DC switching frequency change *R2)	016_H	246
FREQ_SPREAD	DC-DC Frequency spread-spectrum control register *R2)	017_H	248
ABIST_CTRL0	ABIST control 0 *R2)	018_H	250
ABIST_CTRL1	ABIST control 1 *R2)	019_H	251
ABIST_SELECT0	ABIST select 0 *R2)	$01A_H$	252
ABIST_SELECT1	ABIST select 1 *R2)	$01B_H$	254
ABIST_SELECT2	ABIST select 2 *R2)	$01C_H$	256

(table continues...)

Table 56 (continued) Registers overview - OTHERSR2 (ascending offset address)

Short name	Long name	Offset address	See
GTM	Global testmode *R2)	$01D_H$	258
REDOP_RS_CFG1	Reduced operation reflected status configuration 1 register - *R2)	$01E_H$	259

18.2 Registers overview - ERR (ascending offset address)

Table 57 Registers overview - ERR (ascending offset address)

Short name	Long name	Offset address	See
ERR0_PW_CFG	ERR0 protection write configuration register *R2)	$01F_H$	261
ERR0_RS_CFG	ERR0 reflected status configuration register *R3)	020_H	262
ERR1_PW_CFG	ERR1 protection write configuration register *R2)	021_H	263
ERR1_RS_CFG	ERR1 reflected status configuration register *R3_C1)	022_H	264
ERR2_PW_CFG	ERR2 protection write configuration register *R2)	023_H	265
ERR2_RS_CFG	ERR2 reflected status configuration register *R3_C2)	024_H	266

18.3 Registers overview - OTHERSR0 (ascending offset address)

Table 58 Registers overview - OTHERSR0 (ascending offset address)

Short name	Long name	Offset address	See
DEV_CFG1	Device configuration 1 register *R0)	025_H	267
DEV_PW_CFG2	Device protected write configuration 2 register *R0)	026_H	269
DEV_RS_CFG2	Device reflected status configuration 2 register *R0)	027_H	270

18.4 Registers overview - OTHERSR1 (ascending offset address)

Table 59 Registers overview - OTHERSR1 (ascending offset address)

Short name	Long name	Offset address	See
SYSFAIL_STAT_APP1	System failure status register for application 1 *R1)	029_H	271
SYSFAIL_STAT_APP2	System failure status flags for application 2 *R1)	$02A_H$	273
STG_STAT_APP1	Short to ground status register for application 1 *R1)	$02B_H$	275
STG_STAT_APP2	Short to ground status register for application 2 *R1)	$02C_H$	277
OV_STAT_APP1	Overvoltage status register for application 1 *R1)	$02D_H$	279
OV_STAT_APP2	Overvoltage status register for application 2 *R1)	$02E_H$	281
INTSUP_STAT_APP1	Internal supply status register for application 1 *R1)	$02F_H$	283
INTSUP_STAT_APP2	Internal supply status register for application 2 *R1)	030_H	284

(table continues...)

Table 59 (continued) Registers overview - OTHERSR1 (ascending offset address)

Short name	Long name	Offset address	See
OT_STAT_APP1	Over temperature status register for application 1 *R1)	031_H	285
OT_STAT_APP2	Over temperature status register for application 2 *R1)	032_H	286
PROT_STAT	Protection status *R1)	033_H	287
REDOP_PW_CFG1	Reduced operation protected write configuration 1 register - *R1)	034_H	288
REDOP_PW_CFG2	Reduced operation protected write configuration 2 register - *R1)	035_H	290
DEV_PW_CFG3	Device protected write configuration 3 register *R1)	036_H	291

18.5 Registers overview - WATCHDOG (ascending offset address)

Table 60 Registers overview - WATCHDOG (ascending offset address)

Short name	Long name	Offset address	See
WD1_PW_CFG0	Watchdog 1 protected write configuration 0 register *R2)	037_H	293
WD1_RS_CFG0	Watchdog 1 reflected status configuration 0 register - *R3_C1	038_H	294
WD1_PW_CFG1	Watchdog 1 protected write configuration 1 register *R2)	039_H	295
WD1_RS_CFG1	Watchdog 1 reflected status configuration 1 register- *R3_C1	$03A_H$	296
FWD1_PW_HBTP_CFG	Functional watchdog 1 protected write heart beat timer period configuration register - *R2)	$03B_H$	297
FWD1_RS_HBTP_CFG	Functional watchdog 1 reflected status heart beat timer period configuration register *R3_C1	$03C_H$	298
WWD1_PW_CW_CFG	Window watchdog 1 protected write closed window configuration register - *R2)	$03D_H$	299
WWD1_RS_CW_CFG	Window watchdog 1 reflected status closed window configuration register *R3_C1)	$03E_H$	300
WWD1_PW_OW_CFG	Window watchdog 1 protected write open window configuration register - *R2)	$03F_H$	301
WWD1_RS_OW_CFG	Window watchdog 1 reflected status open window configuration register - *R3_C1)	040_H	302
WWD1_TRIG	Window watchdog 1 trigger- *R2)	041_H	303
FWD1_RSP	Functional watchdog 1 response register - *R2)	042_H	304
FWD1_RSP_SYNC	Functional watchdog 1 response register with synchronization of the heartbeat timer - *R2)	043_H	305
FWD1_STAT	Functional watchdog 1 status register - *R3_C1)	044_H	306
WWD1_ECNT_STAT	Window watchdog 1 error counter status register - *R3_C1)	045_H	307
WD2_PW_CFG0	Watchdog 2 protected write configuration 0 register - *R2)	046_H	308
WD2_RS_CFG0	Watchdog 2 reflected status configuration 0 register- *R3_C2)	047_H	309

(table continues...)

Table 60 (continued) Registers overview - WATCHDOG (ascending offset address)

Short name	Long name	Offset address	See
WD2_PW_CFG1	Watchdog 2 protected write configuration 1 - *R2)	048_H	310
WD2_RS_CFG1	Watchdog 2 reflected status configuration 1 register - *R3_C2)	049_H	311
FWD2_PW_HBTP_CFG	Functional watchdog 2 protected write heart beat timer period configuration register - *R2)	$04A_H$	312
FWD2_RS_HBTP_CFG	Functional watchdog 2 reflected status heart beat timer period configuration register *R3_C2)	$04B_H$	313
WWD2_PW_CW_CFG	Window watchdog 2 protected write closed window configuration register - *R2)	$04C_H$	314
WWD2_RS_CW_CFG	Window watchdog 2 reflected status closed window configuration register *R3_C2)	$04D_H$	315
WWD2_PW_OW_CFG	Window watchdog 2 protected write open window configuration register - *R2)	$04E_H$	316
WWD2_RS_OW_CFG	Window watchdog 2 reflected status open window configuration register *R3_C2)	$04F_H$	317
WWD2_TRIG	Window watchdog 2 service - *R2)	050_H	318
FWD2_RSP	Functional watchdog 2 response register - *R2)	051_H	319
FWD2_RSP_SYNC	Functional watchdog 2 response register with synchronization - *R2)	052_H	320
FWD2_STAT	Functional watchdog 2 status register - *R3_C2)	053_H	321
WWD2_ECNT_STAT	Window watchdog 2 status register - *R3_C2)	054_H	322

18.6 Register overview - MISC (ascending offset address)

Table 61 Register overview - MISC (ascending offset address)

Short name	Long name	Offset address	See
SSW_DIAG	Safety switch diagnostics, *R1)	055_H	323
BUCK_CORE_PW_VSEL	BUCK CORE protected write voltage selection register *R1)	056_H	324
BUCK_CORE_RS_VSEL	BUCK CORE reflected status voltage selection register *R2)	057_H	325
VCORESTAT	Buck core voltage selection stat, *R2)	058_H	326
VCOREMONSTAT	Buck core voltage selection monitors stat, *R2)	059_H	327
WUT_STAT0	Wake Up Timer value after exiting from STANDBY or SLEEP (lower 16 bits)	$05A_H$	328
WUT_STAT1	Wake Up Timer value after exiting from STANDBY or SLEEP (upper 8 bits)	$05B_H$	329

18.7 Registers overview - DEVICEID (ascending offset address)

Table 62 Registers overview - DEVICEID (ascending offset address)

Short name	Long name	Offset address	See
CHPID	Chip product identifier	$1F0_H$	330
CHREV	Chip product version and revision	$1F1_H$	331
MANID	Manufacturer ID	$1F2_H$	332

18.8 Device configuration 4 *R2)

DEV_CFG4 Offset address: 000_H

Device configuration 4 *R2) Reset values see: Table 63

15	14	13	12	11	10	9	8
FSM_SDT_VMON12		**Res**				**DCDC_SYNC_IN_EN**	**WUT_EN**
rw		r				rw	rw

7	6	5	4	3	2	1	0
WUT_CYC	**WUT_PRESC**	**FSM_SDT_TMR**		**FSM_TRDEL**			
rw	rw	rw		rw			

Field	Bits	Type	Description
FSM_TRDEL	3:0	rw	**Transition delay (TRDEL) into low power states (STANDBY, SLEEP)** 0_H 100 µs 1_H 200 µs 2_H 300 µs 3_H 400 µs 4_H 500 µs 5_H 600 µs 6_H 700 µs 7_H 800 µs 8_H 900 µs 9_H 1000 µs A_H 1100 µs B_H 1200 µs C_H 1300 µs D_H 1400 µs E_H 1500 µs F_H 1600 µs
FSM_SDT_TMR	5:4	rw	**Shut down timer (tSDT_TMR) for internal regulators of power down sequencing** 00_B 0 01_B 500 µs 10_B 1000 µs 11_B 1500 µs
WUT_PRESC	6	rw	**Wake up timer cycle period pre-scaler** 0_B Disabled 1_B Enabled
WUT_CYC	7	rw	**Wake timer cycle period** 0_B 10 µs 1_B 10 ms

(table continues...)

(continued)

Field	Bits	Type	Description
WUT_EN	8	rw	**Wake timer enable** 0_B Disabled 1_B Enabled
DCDC_SYNC_IN_EN	9	rw	**Enable synchronization input (only applicable when REDUCED OPERATION is disabled, since it uses SYNC_IN pin shared with INT2)** 0_B Disable 1_B Enable
FSM_SDT_VMON12	15:14	rw	**Shut down timer for VMON1 and VMON2 of power down sequencing** 00_B 0 µs 01_B 500 µs 10_B 1 ms 11_B 1.5 ms

Table 63 Reset values of DEV_CFG4

Reset	Reset value	Note
	$C038_H$	Reset class R2)

18.9 Reduced operation reflected status configuration 2 register - *R2)

REDOP_RS_CFG2

Reduced operation reflected status configuration 2 register - *R2)

Offset address: 001_H

Reset values see: Table 64

15	14	13	12	11	10	9	8
REDOP_RESOUT_APP2_DUR			REDOP_RESOUT_APP1_DUR			REDOP_RESOUT_APP_TB	Res
r			r			r	r

7	6	5	4	3	2	1	0
Res							
r							

Field	Bits	Type	Description
REDOP_RESOUT_APP_TB	9	r	**Partial reset timer step, selectable between 10 µs or 100 µs** 0_B 10 µs 1_B 100 µs
REDOP_RESOUT_APP1_DUR	12:10	r	**Application reset pulse duration duration for INT1** 000_B (0 + 1)*10 µs for REDOP_RESOUT_APP_TB = 0; ((0 + 1)*100 + 50) µs for REDOP_RESOUT_APP_TB = 1 … 111_B (7 + 1)*10 µs for REDOP_RESOUT_APP_TB = 0; ((7 + 1)*100 + 50) µs for REDOP_RESOUT_APP_TB = 1
REDOP_RESOUT_APP2_DUR	15:13	r	**Application reset pulse duration duration for INT2** 000_B (0 + 1)*10 µs for REDOP_RESOUT_APP_TB = 0; ((0 + 1)*100 + 50) µs for REDOP_RESOUT_APP_TB = 1 … 111_B (7 + 1)*10 µs for REDOP_RESOUT_APP_TB = 0; ((7 + 1)*100 + 50) µs for REDOP_RESOUT_APP_TB = 1

Table 64 Reset values of REDOP_RS_CFG2

Reset	Reset value	Note
	0000_H	Reset class R2)

18.10 Protection configuration register - *R2)

Controls UNLOCK/LOCK mechanism for password protected registers. UNLOCK allows to program registers, LOCK updates effective content of programmed ones. Any other value lead to LOCKed state, discarding pending changes if any.

PROT_CFG Offset address: 002_H

Protection configuration register - *R2) Reset values see: Table 65

15	14	13	12	11	10	9	8
KEY							
rw							

7	6	5	4	3	2	1	0
KEY							
rw							

Field	Bits	Type	Description
KEY	15:0	rw	**KEY value** $B5CA_H$ Registers unlocked $D396_H$ Registers locked

Table 65 Reset values of PROT_CFG

Reset	Reset value	Note
	$D396_H$	Reset class R2)

18.11 Device reflected status configuration Register *R2)

DEV_RS_CFG3 Offset address: 003_H

Device reflected status configuration Register *R2) Reset values see: Table 66

15	14	13	12	11	10	9	8
Res					VMON2_EN	VMON1_EN	BOOST_EN
r					r	r	r

7	6	5	4	3	2	1	0
BUCKINT_EN	QUC_EN	BUCKCORE_EN	QCO_EN	QVR_EN	FSM_STATEREQ		
r	r	r	r	r	r		

Field	Bits	Type	Description
FSM_STATEREQ	2:0	r	**Request for device state transition.** 000_B NONE 001_B INIT 010_B NORMAL 011_B SLEEP 100_B STANDBY 101_B WAKE 110_B NONE 111_B NONE
QVR_EN	3	r	**Enable request for reference voltage.** 0_B Disabled 1_B Enabled
QCO_EN	4	r	**Enable request for communication LDO.** 0_B Disabled 1_B Enabled
BUCKCORE_EN	5	r	**Enable request for BUCKCORE** 0_B Disabled 1_B Enabled
QUC_EN	6	r	**Enable request for QUC** 0_B Disabled 1_B Enabled
BUCKINT_EN	7	r	**Enable request for BUCK interface** 0_B Disabled 1_B Enabled
BOOST_EN	8	r	**Enable request for Boost** 0_B Disabled 1_B Enabled

(table continues...)

(continued)

Field	Bits	Type	Description
VMON1_EN	9	r	**Enable request for External Monitoring1** 0_B Disabled 1_B Enabled
VMON2_EN	10	r	**Enable request for External Monitoring2** 0_B Disabled 1_B Enabled

Table 66 Reset values of DEV_RS_CFG3

Reset	Reset value	Note
	0000_H	Reset class R2)

18.12 Wake up timer LSB Value (*R2)

WUT_CFG0 Offset address: 004_H

Wake up timer LSB Value [*R2) Reset values see: Table 67

15	14	13	12	11	10	9	8
TIMVALL							
rw							

7	6	5	4	3	2	1	0
TIMVALL							
rw							

Field	Bits	Type	Description
TIMVALL	15:0	rw	**Wake timer compare value, 16bit lsb**

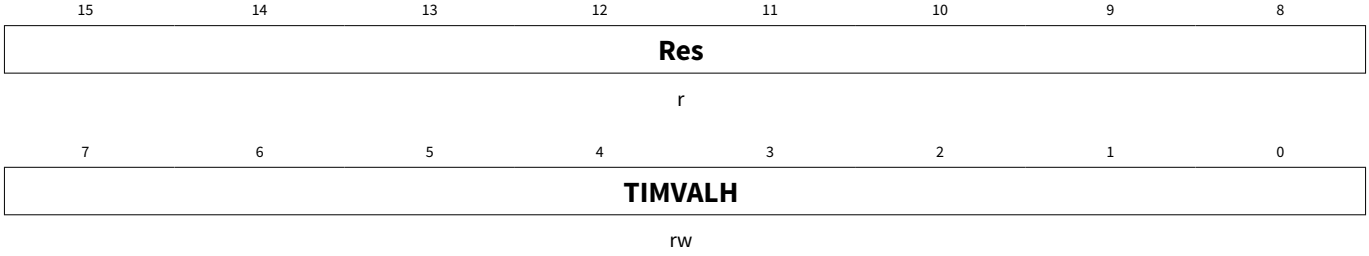
Table 67 Reset values of WUT_CFG0

Reset	Reset value	Note
	0000_H	Reset class R2)

18.13 Wake up timer MSB Value (*R2)

WUP_CFG1 Offset address: 005_H

Wake up timer MSB Value [*R2) Reset values see: Table 68



Field	Bits	Type	Description
TIMVALH	7:0	rw	**Wake timer compare value (23:16) (msb)**

Table 68 Reset values of WUP_CFG1

Reset	Reset value	Note
	0000_H	Reset class R2)

18.14 Wakeup status flags for Application 1 *R2)

WAKE_STAT_APP1 Offset address: 006_H

Wakeup status flags for Application 1 *R2) Reset values see: Table 69

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			**SPI**	**WUT**	**Res**	**ENA**	**WAK**
r			rw1c	rw1c	r	rw1c	rw1c

Field	Bits	Type	Description
WAK	0	rw1c	**Wakeup by WAK signal, bit is set if SLEEP, FAILSAFE or STANDBY state left because of WAK** 0_B No event detected 1_B Event detected
ENA	1	rw1c	**Wake by ENA signal, bit is set if SLEEP, FAILSAFE or STANDBY state left because of ENA** 0_B No event detected 1_B Event detected
WUT	3	rw1c	**Wakeup by wake timer** 0_B No event detected 1_B Event detected
SPI	4	rw1c	**Wakeup by SPI** 0_B No event detected 1_B Event detected

Table 69 Reset values of WAKE_STAT_APP1

Reset	Reset value	Note
	0000_H	Reset class R2)

18.15 Wakeup status flags for Application 2 *R2)

WAKE_STAT_APP2 Offset address: 007_H

Wakeup status flags for Application 2 *R2) Reset values see: Table 70

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			SPI	WUT	Res	ENA	WAK
r			rw1c	rw1c	r	rw1c	rw1c

Field	Bits	Type	Description
WAK	0	rw1c	**Wakeup by WAK signal, bit is set if SLEEP, FAILSAFE or STANDBY state left because of WAK** 0_B No event detected 1_B Event detected
ENA	1	rw1c	**Wake by ENA signal, bit is set if SLEEP, FAILSAFE or STANDBY state left because of ENA** 0_B No event detected 1_B Event detected
WUT	3	rw1c	**Wakeup by wake timer, bit will also be set if device leaves STANDBY state because of wakeup timer expired** 0_B No event detected 1_B Event detected
SPI	4	rw1c	**Wakeup by SPI from SLEEP state** 0_B No event detected 1_B Event detected

Table 70 Reset values of WAKE_STAT_APP2

Reset	Reset value	Note
	0000_H	Reset class R2)

18.16 INIT and REDUCED OPERATION Error Status flags for Application 1 *R2)

INIT_ERR_APP1

Offset address: 008_H

INIT and REDUCED OPERATION Error Status flags for Application 1 *R2)

Reset values see: Table 71

15	14	13	12	11	10	9	8
HARDRES	**SOFTRES**	**Res**		**REDOP_RES2**	**REDOP_RES1**	**Res**	
rw1c	rw1c	r		rw1c	rw1c	r	

7	6	5	4	3	2	1	0
ERR2	**ERR1**	**Res**	**FWD2_EC**	**FWD1_EC**	**WWD2_EC**	**WWD1_EC**	**VMONF**
rw1c	rw1c	r	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
VMONF	0	rw1c	**Voltage monitor failure which lead to INIT (see chapter: Collection registers)** 0_B No fault 1_B Fault occurred
WWD1_EC	1	rw1c	**Window watchdog1 error counter reached the error threshold** 0_B No fault 1_B Fault occurred
WWD2_EC	2	rw1c	**Window watchdog2 error counter reached the error threshold** 0_B No fault 1_B Fault occurred
FWD1_EC	3	rw1c	**Functional watchdog1 error counter reached the error threshold** 0_B No fault 1_B Fault occurred
FWD2_EC	4	rw1c	**Functional watchdog2 error counter reached the error threshold** 0_B No fault 1_B Fault occurred
ERR1	6	rw1c	**ERR1 failure** 0_B No fault 1_B Fault occurred
ERR2	7	rw1c	**ERR2 failure** 0_B No fault 1_B Fault occurred
REDOP_RES1	10	rw1c	**REDUCED OPERATION reset has been generated because REDUCED OPERATION timer expired once (same timer as INIT timer)** 0_B No fault 1_B Fault occurred

(table continues...)

(continued)

Field	Bits	Type	Description
REDOP_RES2	11	rw1c	**REDUCED OPERATION reset has been generated because REDUCED OPERATION timer expired twice (same timer as INIT timer); Move to INIT is triggered** 0_B No fault 1_B Fault occurred
SOFTRES	14	rw1c	**Soft reset generated** 0_B No soft reset occurred 1_B Soft reset occurred
HARDRES	15	rw1c	**Hard reset generated because INIT timer expired twice** 0_B No hard reset occurred 1_B Hard reset occurred

Table 71 Reset values of INIT_ERR_APP1

Reset	Reset value	Note
	0000_H	Reset class R2)

18.17 INIT and REDUCED OPERATION Error Status flags for Application 2 *R2)

INIT_ERR_APP2

Offset address: 009_H

INIT and REDUCED OPERATION Error Status flags for Application 2 *R2)

Reset values see: Table 72

15	14	13	12	11	10	9	8
HARDRES	**SOFTRES**	**Res**		**REDOP_RES2**	**REDOP_RES1**	**Res**	
rw1c	rw1c	r		rw1c	rw1c	r	

7	6	5	4	3	2	1	0
ERR2	**ERR1**	**Res**	**FWD2_EC**	**FWD1_EC**	**WWD2_EC**	**WWD1_EC**	**VMONF**
rw1c	rw1c	r	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
VMONF	0	rw1c	**Voltage monitor failure which lead to INIT (see chapter: Collection registers)** 0_B No fault 1_B Fault occurred
WWD1_EC	1	rw1c	**Window watchdog1 error counter reached the error threshold** 0_B No fault 1_B Fault occurred
WWD2_EC	2	rw1c	**Window watchdog2 error counter reached the error threshold** 0_B No fault 1_B Fault occurred
FWD1_EC	3	rw1c	**Functional watchdog1 error counter reached the error threshold** 0_B No fault 1_B Fault occurred
FWD2_EC	4	rw1c	**Functional watchdog2 error counter reached the error threshold** 0_B No fault 1_B Fault occurred
ERR1	6	rw1c	**error1 monitor failure** 0_B No fault 1_B Fault occurred
ERR2	7	rw1c	**error2 monitor failure** 0_B No fault 1_B Fault occurred
REDOP_RES1	10	rw1c	**REDUCED OPERATION reset has been generated because REDUCED OPERATION timer expired once** 0_B No fault 1_B Fault occurred

(table continues...)

(continued)

Field	Bits	Type	Description
REDOP_RES2	11	rw1c	**REDUCED OPERATION reset has been generated because REDUCED OPERATION timer expired twice** 0_B No fault 1_B Fault occurred
SOFTRES	14	rw1c	**Soft reset generated because the Init timer expired once** 0_B No soft reset occurred 1_B Soft reset occurred
HARDRES	15	rw1c	**Hard reset generated because Init timer expired twice** 0_B No hard reset occurred 1_B Hard reset occurred

Table 72 Reset values of INIT_ERR_APP2

Reset	Reset value	Note
	0000_H	Reset class R2)

18.18 Interrupt flags for Application 1 that trigger INT1 *R2)

IF1 Offset address: $00A_H$

Interrupt flags for Application 1 that trigger INT1 *R2) Reset values see: Table 73

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
INTMISS	**ABIST**	**Res**	**OT_WRN_OC_ERR**	**MON**	**SPI_FAIL**	**WUT_EVT**	**SYSFAIL_ERR**
r	rw1c	r	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
SYSFAIL_ERR	0	rw1c	**INT1 is triggered, because a system event has occured (see chapter: Collection registers)** 0_B No interrupt 1_B Interrupt occured
WUT_EVT	1	rw1c	**INT1 is triggered, because a wake up event has occured (see chapter: Collection registers)** 0_B No interrupt 1_B Interrupt occurred
SPI_FAIL	2	rw1c	**INT1 is triggered, because a SPI_FAIL has occured (see chapter: Collection registers)** 0_B No interrupt 1_B Interrupt occurred
MON	3	rw1c	**INT1 is triggered, because a monitoring event has occured (see chapter: Collection registers)** 0_B No interrupt 1_B Interrupt occurred
OT_WRN_OC_ERR	4	rw1c	**INT1 is triggered, because a overtemperature warning or overcurrent has occured (see chapter: Collection registers)** 0_B No interrupt 1_B Interrupt occurred
ABIST	6	rw1c	**Requested ABIST operation performed or interrupted. ABIST is not continued automatically.** 0_B No interrupt 1_B Interrupt occurred
INTMISS	7	r	**Interrupt INT1 has not been serviced within tINTTO time** 0_B No interrupt 1_B Interrupt occurred

Table 73 Reset values of IF1

Reset	Reset value	Note
	0000_H	Reset class R2)

18.19 Interrupt flags for Application 2 that trigger INT2 *R2)

IF2 Offset address: $00B_H$

Interrupt flags for Application 2 that trigger INT2 *R2) Reset values see: Table 74

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
INTMISS	**ABIST**	**Res**	**OT_WRN_OC_ERR**	**MON**	**SPI_FAIL**	**WUT_EVT**	**SYSFAIL_ERR**
r	rw1c	r	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
SYSFAIL_ERR	0	rw1c	**INT2 is triggered, because a system event has occured (see chapter: Collection registers)** 0_B No interrupt 1_B Interrupt occurred
WUT_EVT	1	rw1c	**INT2 is triggered, because a wake up event has occured (see chapter: Collection registers)** 0_B No interrupt 1_B Interrupt occurred
SPI_FAIL	2	rw1c	**INT2 is triggered, because a SPI_FAIL has occured (see chapter: Collection registers)** 0_B No interrupt 1_B Interrupt occurred
MON	3	rw1c	**INT2 is triggered, because a monitoring event has occured (see chapter: Collection registers)** 0_B No interrupt 1_B Interrupt occurred
OT_WRN_OC_ERR	4	rw1c	**INT2 is triggered, because a overtemperature warning or overcurrent has occured (see chapter: Collection registers)** 0_B No interrupt 1_B Interrupt occurred
ABIST	6	rw1c	**Requested ABIST operation performed or interrupted. ABIST is not continued automatically.** 0_B No interrupt 1_B Interrupt occurred
INTMISS	7	r	**Interrupt INT2 has not been serviced within tINTTO time** 0_B No interrupt 1_B Interrupt occurred

Table 74 Reset values of IF2

Reset	Reset value	Note
	0000_H	Reset class R2)

18.20 System status flags for Application 1 that trigger INT1 *R2)

SYS_STAT_APP1

Offset address: $00C_H$

System status flags for Application 1 that trigger INT1 *R2)

Reset values see: Table 75

15	14	13	12	11	10	9	8
Res						BUCKCORE_SVS_NOK	BUCKCORE_SVS_OK
r						rw1c	rw1c

7	6	5	4	3	2	1	0
APP2_FAIL	ERR1_ERR	ERR0_ERR	FSM_NOOP	FSM_TRFAIL	FWD1_ERR	WWD1_ERR	Res
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	r

Field	Bits	Type	Description
WWD1_ERR	1	rw1c	**Window watchdog 1 error interrupt flag. Service was incorrect or missed.** 0_B No event occurred 1_B Event detected
FWD1_ERR	2	rw1c	**Functional watchdog 1 error interrupt flag. Service was incorrect or missed.** 0_B No event occured 1_B Event occured
FSM_TRFAIL	3	rw1c	**Transition to low power state (STANDBY/SLEEP) failed** 0_B No occurrence 1_B Transition unscuccessful
FSM_NOOP	4	rw1c	**Requested state transition via DEVCTRL could not be performed because either path between current state and requested state does not exist (eg. INIT to SLEEP), or paths exists but pre-conditions are not satisfied (e.g. INIT to NORMAL, but WWD enabled and not serviced).** 0_B No occurrence 1_B Transition was not executed
ERR0_ERR	5	rw1c	**ERR0 error status flag** 0_B No occurrence 1_B Invalid frequency - recovery time started
ERR1_ERR	6	rw1c	**ERR1 error status flag** 0_B No occurrence 1_B Invalid frequency - recovery time started
APP2_FAIL	7	rw1c	**Application 2 entered REDUCED OPERATION** 0_B No occurrence 1_B Application 2 fault occurred

(table continues...)

(continued)

Field	Bits	Type	Description
BUCKCORE_SVS_OK	8	rw1c	**BUCK CORE static voltage scaling procedure completed successfully.** 0_B Not completed 1_B Completed successfully
BUCKCORE_SVS_NOK	9	rw1c	**BUCK CORE static voltage scaling procedure was unsuccessful, because the device is not in state NORMAL or INIT or BUCKCORE output voltage is set to 1.15 V.** 0_B No occurrence 1_B BUCK CORE voltage scaling was unsuccessful

Table 75 Reset values of SYS_STAT_APP1

Reset	Reset value	Note
	0000_H	Reset class R2)

18.21 System status flags for Application 2 that trigger INT2 *R2)

SYS_STAT_APP2

Offset address: $00D_H$

System status flags for Application 2 that trigger INT2 *R2)

Reset values see: Table 76

15	14	13	12	11	10	9	8
Res						BUCKCORE_SVS_NOK	BUCKCORE_SVS_OK
r						rw1c	rw1c

7	6	5	4	3	2	1	0
APP1_FAIL	ERR2_ERR	ERR0_ERR	FSM_NOOP	FSM_TRFAIL	FWD2_ERR	WWD2_ERR	Res
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	r

Field	Bits	Type	Description
WWD2_ERR	1	rw1c	**Window watchdog 2 error interrupt flag. Service was incorrect or missed.** 0_B No event occurred 1_B Event detected
FWD2_ERR	2	rw1c	**Functional watchdog 1 error interrupt flag. Service was incorrect or missed.** 0_B No event detected 1_B Event detected
FSM_TRFAIL	3	rw1c	**Transition to low power state (STANDBY/SLEEP) failed** 0_B No occurrence 1_B Transition unsuccessful
FSM_NOOP	4	rw1c	**Requested state transition via DEVCTRL could not be performed because either path between current state and requested state does not exist (eg. INIT to SLEEP), or paths exists but pre-conditions are not satisfied (e.g. INIT to NORMAL, but WWD enabled and not serviced).** 0_B No occurrence 1_B Transition was not executed
ERR0_ERR	5	rw1c	**ERR0 error status flag** 0_B No occurrence 1_B Invalid frequency - recovery time started
ERR2_ERR	6	rw1c	**ERR2 error status flag** 0_B No occurrence 1_B Invalid frequency - recovery time started
APP1_FAIL	7	rw1c	**Application 1 entered REDUCED OPERATION** 0_B No occurrence 1_B Application 1 fault occurred

(table continues...)

(continued)

Field	Bits	Type	Description
BUCKCORE_SVS_OK	8	rw1c	**BUCK CORE static voltage scaling procedure completed successfully.** 0_B Not completed 1_B Completed successfully
BUCKCORE_SVS_NOK	9	rw1c	**BUCK CORE static voltage scaling procedure was unsuccessful, because the device is not in state NORMAL or INIT or BUCKCORE output voltage is set to 1.15 V.** 0_B No occurrence 1_B BUCK CORE voltage scaling was unsuccessful

Table 76 Reset values of SYS_STAT_APP2

Reset	Reset value	Note
	0000_H	Reset class R2)

18.22 SPI failure status flags that triggers INT1 *R2)

SPI_FAIL_STAT_APP1 Offset address: $00E_H$

SPI failure status flags that triggers INT1 *R2) Reset values see: Table 77

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			**LOCK**	**CS_TO**	**ADR**	**FR_LEN**	**CRC**
r			rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
CRC	0	rw1c	**CRC error in SPI frame** 0_B No error 1_B CRC wrong
FR_LEN	1	rw1c	**Invalid frame length, number of detected SPI clock cycles different than 32** 0_B Frame length ok 1_B Frame length incorrect
ADR	2	rw1c	**Invalid address in SPI frame** 0_B No occurrence 1_B Address not existing
CS_TO	3	rw1c	**Error in duration of SPI transaction, nCS low for more than 2 ms** 0_B No occurrence 1_B CSN timeout
LOCK	4	rw1c	**Error during LOCK/UNLOCK procedure or write attempts to locked registers** 0_B No occurrence 1_B LOCK/UNLOCK sequence failed

Table 77 Reset values of SPI_FAIL_STAT_APP1

Reset	Reset value	Note
	0000_H	Reset class R2)

18.23 SPI status flags for Application 2 that trigger INT2 *R2)

SPI_FAIL_STAT_APP2 Offset address: $00F_H$

SPI status flags for Application 2 that trigger INT2 *R2) Reset values see: Table 78

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			**LOCK**	**CS_TO**	**ADR**	**FR_LEN**	**CRC**
r			rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
CRC	0	rw1c	**CRC error in SPI frame** 0_B No error 1_B CRC wrong
FR_LEN	1	rw1c	**Invalid frame length, number of detected SPI clock cycles different than 32** 0_B Frame length ok 1_B Frame length incorrect
ADR	2	rw1c	**Invalid address in SPI frame** 0_B No occurrence 1_B Address not existing
CS_TO	3	rw1c	**Error in duration of SPI transaction, nCS low for more than 2 ms** 0_B No occurrence 1_B CSN timeout
LOCK	4	rw1c	**Error during LOCK/UNLOCK procedure or write attempts to locked registers** 0_B No occurrence 1_B LOCK/UNLOCK sequence failed

Table 78 Reset values of SPI_FAIL_STAT_APP2

Reset	Reset value	Note
	0000_H	Reset class R2)

18.24 Monitor status flags register 2 for Application 1 *R2)

UV_STAT_APP1 Offset address: 010_H

Monitor status flags register 2 for Application 1 *R2) Reset values see: Table 79

15	14	13	12	11	10	9	8
Res				INTSUP_VDD2V5_UV	INTSUP_IVCC_UV	BUCKIF	VMON2
r				rw1c	rw1c	rw1c	rw1c

7	6	5	4	3	2	1	0
VMON1	BOOST	QVR	QCO	BUCKCORE	QST	QUC	PREREG
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
PREREG	0	rw1c	**Pre-regulator voltage under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
QUC	1	rw1c	**QUC under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
QST	2	rw1c	**QST under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
BUCKCORE	3	rw1c	**BUCKCORE under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
QCO	4	rw1c	**QCO under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
QVR	5	rw1c	**QVR under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
BOOST	6	rw1c	**BOOST under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
VMON1	7	rw1c	**VMON1 under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
VMON2	8	rw1c	**VMON2 under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred

(table continues...)

(continued)

Field	Bits	Type	Description
BUCKIF	9	rw1c	**BUCKIF under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
INTSUP_IVCC_UV	10	rw1c	**Internal supply IVCC under voltage status flag, *R1)** 0_B No occurrence 1_B Undervoltage occurred
INTSUP_VDD2V5_UV	11	rw1c	**Internal supply VDD 2.5 V under voltage status flag, *R1)** 0_B No occurrence 1_B Undervoltage occurred

Table 79 Reset values of UV_STAT_APP1

Reset	Reset value	Note
	0000_H	Reset class R2)

18.25 Monitor status flags register 2 for Application 2 *R2)

UV_STAT_APP2 Offset address: 011_H

Monitor status flags register 2 for Application 2 *R2) Reset values see: Table 80

15	14	13	12	11	10	9	8
Res				INTSUP_2V5_UV	INTSUP_IVCC_UV	BUCKIF	VMON2
r				rw1c	rw1c	rw1c	rw1c

7	6	5	4	3	2	1	0
VMON1	BOOST	QVR	QCO	BUCKCORE	QST	QUC	PREREG
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
PREREG	0	rw1c	**Pre-regulator voltage under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
QUC	1	rw1c	**QUC under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
QST	2	rw1c	**QST under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
BUCKCORE	3	rw1c	**BUCKCORE under voltage status flag** 0_B No occurrence 1_B Undervolage occurred
QCO	4	rw1c	**QCO under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
QVR	5	rw1c	**QVR under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
BOOST	6	rw1c	**Boost voltage under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
VMON1	7	rw1c	**VMON1 voltage under voltage status flag** 0_B No occurrence 1_B Undervoltage occurrence
VMON2	8	rw1c	**Mon2 voltage under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred

(table continues...)

(continued)

Field	Bits	Type	Description
BUCKIF	9	rw1c	**BUCKIF under voltage status flag** 0_B No occurrence 1_B Undervoltage occurred
INTSUP_IVCC_UV	10	rw1c	**IVCC voltage under voltage status flag *R1)** 0_B No occurrence 1_B Undervoltage occurred
INTSUP_2V5_UV	11	rw1c	**2V5 voltage under voltage status flag *R1)** 0_B No occurrence 1_B Undervoltage occurred

Table 80 Reset values of UV_STAT_APP2

Reset	Reset value	Note
	0000_H	Reset class R2)

18.26 Over temperature warning and over current status flags *R2)

OT_WRN_OC_STAT_APP1

Over temperature warning and over current status flags *R2)

Offset address: 012_H

Reset values see: Table 81

15	14	13	12	11	10	9	8
Res							BOOST_OC
r							rw1c

7	6	5	4	3	2	1	0
IVCC_OC	QUC_OTWRN	BOOST_OTWRN	BUCKIF_OTWRN	BUCKCORE_OTWRN	QVR_OC	QCO_OTWRN	QST_OC
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
QST_OC	0	rw1c	**QST over current** 0_B No occurrence 1_B Over current occurred
QCO_OTWRN	1	rw1c	**QCO over temperature warning** 0_B No occurrence 1_B Overtemperature warning
QVR_OC	2	rw1c	**QVR over current** 0_B No occurrence 1_B Over current occurred
BUCKCORE_OTWRN	3	rw1c	**BUCKCORE overtemperature warning** 0_B No occurrence 1_B Overtemperature warning
BUCKIF_OTWRN	4	rw1c	**BUCKIF overtemperature warning** 0_B No occurrence 1_B Overtemperature warning
BOOST_OTWRN	5	rw1c	**BOOST overtemperature warning** 0_B No occurrence 1_B Overtemperature warning
QUC_OTWRN	6	rw1c	**QUC over temperature warning** 0_B No occurrence 1_B Overtemperature warning
IVCC_OC	7	rw1c	**IVCC over current warning** 0_B No occurrence 1_B Over current occurred
BOOST_OC	8	rw1c	**BOOST over current** 0_B No occurrence 1_B Over current occurred

Table 81 Reset values of OT_WRN_OC_STAT_APP1

Reset	Reset value	Note
	0000_H	Reset class R2)

18.27 Over temperature warning /Over current status flags for Application 2 *R2)

OT_WRN_OC_STAT_APP2 Offset address: 013_H

Over temperature warning /Over current status flags for Application 2 *R2) Reset values see: Table 82

15	14	13	12	11	10	9	8
Res							BOOST_OC
r							rw1c

7	6	5	4	3	2	1	0
IVCC_OC	QUC_OTWRN	BOOST_OTWRN	BUCKIF_OTWRN	BUCKCORE_OTWRN	QVR_OC	QCO_OTWRN	QST_OC
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
QST_OC	0	rw1c	**QST over current** 0_B No occurrence 1_B Over current occurred
QCO_OTWRN	1	rw1c	**QCO over temperature warning** 0_B No occurrence 1_B Overtemperature warning
QVR_OC	2	rw1c	**QVR over current** 0_B No occurrence 1_B Over current occurred
BUCKCORE_OTWRN	3	rw1c	**BUCKCORE overtemperature warning** 0_B No occurrence 1_B Overtemperature warning
BUCKIF_OTWRN	4	rw1c	**BUCKIF overtemperature warning** 0_B No occurrence 1_B Overtemperature warning
BOOST_OTWRN	5	rw1c	**BOOST overtemperature warning** 0_B No occurrence 1_B Overtemperature warning
QUC_OTWRN	6	rw1c	**QUC over temperature warning** 0_B No occurrence 1_B Overtemperature warning
IVCC_OC	7	rw1c	**IVCC over current warning** 0_B No occurrence 1_B Over current occurred
BOOST_OC	8	rw1c	**BOOST over current** 0_B No occurrence 1_B Over current occurred

Table 82 Reset values of OT_WRN_OC_STAT_APP2

Reset	Reset value	Note
	0000_H	Reset class R2)

18.28 Voltage monitor status *R2)

VMON_STAT Offset address: 014_H

Voltage monitor status *R2) Reset values see: Table 83

15	14	13	12	11	10	9	8
Res					VMON2_ST	VMON1_ST	IVCC_ST
r					r	r	r

7	6	5	4	3	2	1	0
QUC_ST	PREREG_ST	BOOST_ST	BUCKINT_ST	QVR_ST	QCO_ST	BUCKCORE_ST	QST_ST
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
QST_ST	0	r	**Standby LDO voltage status** 0_B Voltage is out of range or not enabled 1_B Voltage is OK
BUCKCORE_ST	1	r	**Core voltage status** 0_B Voltage is out of range or not enabled 1_B Voltage is OK
QCO_ST	2	r	**Communication voltage status** 0_B Voltage is out of range or not enabled 1_B Voltage is OK
QVR_ST	3	r	**Reference voltage status** 0_B Voltage is out of range or not enabled 1_B Voltage is OK
BUCKINT_ST	4	r	**Buckint voltage status** 0_B Voltage is out of range or not enabled 1_B Voltage is OK
BOOST_ST	5	r	**Boost voltage status** 0_B Voltage is out of range or not enabled 1_B Voltage is OK
PREREG_ST	6	r	**Prereg voltage status** 0_B Voltage is out of range or not enabled 1_B Voltage is OK
QUC_ST	7	r	**QUC voltage status** 0_B Voltage is out of range or not enabled 1_B Voltage is OK
IVCC_ST	8	r	**IVCC voltage status** 0_B Voltage is out of range or not enabled 1_B Voltage is OK

(table continues...)

(continued)

Field	Bits	Type	Description
VMON1_ST	9	r	**MON1 voltage status** 0_B Voltage is out of range or not enabled 1_B Voltage is OK
VMON2_ST	10	r	**MON2 voltage status** 0_B Voltage is out of range or not enabled 1_B Voltage is OK

Table 83 Reset values of VMON_STAT

Reset	Reset value	Note
	0000_H	Reset class R2)

18.29 Device status register *R2)

DEV_STAT Offset address: 015_H

Device status register *R2) Reset values see: Table 84

15	14	13	12	11	10	9	8
VMON2_AUTO_DET	**VMON1_AUTO_DET**	**BOOST_AUTO_DET**	**BUCKINT_AUTO_DET**	**SSW_AUTO_DET**	**VMON2_EN**	**VMON1_EN**	**BOOST_EN**
r	r	r	r	r	r	r	r

7	6	5	4	3	2	1	0
BUCKIF_EN	**QUC_EN**	**BUCKCORE_EN**	**QCO_EN**	**QVR_EN**	**STATE**		
r	r	r	r	r	r		

Field	Bits	Type	Description
STATE	2:0	r	**Current device state** 000_B reserved 001_B INIT 010_B NORMAL 011_B SLEEP 100_B STANDBY 101_B WAKE 110_B REDUCED_OPERATION 111_B reserved
QVR_EN	3	r	**QVR status** 0_B Disabled 1_B Enabled
QCO_EN	4	r	**QCO status** 0_B Disabled 1_B Enabled
BUCKCORE_EN	5	r	**BUCKCORE status** 0_B Disabled 1_B Enabled
QUC_EN	6	r	**QUC status** 0_B Disabled 1_B Enabled
BUCKIF_EN	7	r	**BUCKIF status** 0_B Disabled 1_B Enabled
BOOST_EN	8	r	**BOOST status** 0_B Disabled 1_B Enabled

(table continues...)

(continued)

Field	Bits	Type	Description
VMON1_EN	9	r	**External voltage monitor channel 1 status** 0_B Disabled 1_B Enabled
VMON2_EN	10	r	**External voltage monitor channel 2 status** 0_B Disabled 1_B Enabled
SSW_AUTO_DET	11	r	**Safety switch auto detect** 0_B not detected 1_B detected
BUCKINT_AUTO_DET	12	r	**BUCKINT autodetection result: 0 not detected, 1 detected** 0_B not detected 1_B detected
BOOST_AUTO_DET	13	r	**BOOST autodetection result: 0 not detected, 1 detected** 0_B not detected 1_B detected
VMON1_AUTO_DET	14	r	**VMON1 autodetection result: 0 not detected, 1 detected** 0_B not detected 1_B detected
VMON2_AUTO_DET	15	r	**VMON2 autodetection result: 0 not detected, 1 detected** 0_B not detected 1_B detected

Table 84 Reset values of DEV_STAT

Reset	Reset value	Note
	0000_H	Reset class R2)

18.30 DC-DC switching frequency change *R2)

DCDC_FREQ_SYNC Offset address: 016_H

DC-DC switching frequency change *R2) Reset values see: Table 85

15	14	13	12	11	10	9	8
PREREG_BOOST_PHSHFT	**BOOST_BUCKIF_PHSHFT**	**Res**			**BOOST_DRIVER_CONFIG**		**BUCKIF_DRIVER_CONFIG**
rw	rw	r			rw		rw

7	6	5	4	3	2	1	0
BUCKIF_DRIVER_CONFIG	**BUCKCORE_DRIVER_CONFIG**		**PREREG_DRIVER_CONFIG**		**DCDC_FREQSEL**		
rw	rw		rw		rw		

Field	Bits	Type	Description
DCDC_FREQSEL	2:0	rw	**DC-DC switching frequency (fDCDC) change** 000_B 1.8 MHz 001_B 1.9 MHz 010_B 2.0 MHz 011_B 2.1 MHz 100_B 2.2 MHz - default/center value 101_B 2.3 MHz 110_B 2.4 MHz 111_B 2.4 MHz
PREREG_DRIVER_CONFIG	4:3	rw	**Drive strength configuration for BUCK PREREG** 00_B Full strenght 01_B 66% of full strength 10_B 33% of full strength 11_B **RESERVED**: Do not use, currently selects 33% strength
BUCKCORE_DRIVER_CONFIG	6:5	rw	**Drive strength configuration for BUCK CORE** 00_B Full strenght 01_B 50% of full strength 10_B 25% of full strength 11_B Do not use, currently selects 25% strength
BUCKIF_DRIVER_CONFIG	8:7	rw	**Drive strength configuration for BUCK IF** 00_B Full strenght 01_B 50% of full strength 10_B 25% of full strength 11_B **RESERVED**: Do not use, currently selects 25% strength

(table continues...)

(continued)

Field	Bits	Type	Description
BOOST_DRIVER_CONFIG	10:9	rw	**Drive strength configuration for BOOST** 00_B Full strenght 01_B 50% of full strength 10_B 25% of full strength 11_B **RESERVED**: Do not use, currently selects 25% strength
BOOST_BUCKIF_PHSHFT	14	rw	**180 degree phase shift between BOOST and BUCKIF** 0_B Disable phase shift 1_B Enable phase shift
PREREG_BOOST_PHSHFT	15	rw	**180 degree phase shift between BOOST and PREREG** 0_B Disable Phase Shift 1_B Enable Phase Shift

Table 85 Reset values of DCDC_FREQ_SYNC

Reset	Reset value	Note
	0004_H	Reset class R2)

18.31 DC-DC Frequency spread-spectrum control register *R2)

FREQ_SPREAD

DC-DC Frequency spread-spectrum control register *R2)

Offset address: 017_H

Reset values see: Table 86

15	14	13	12	11	10	9	8
Res		**FRE_SP_AMPLITUDE**				**FRE_SP_FSTEP**	
r		rw				rw	

7	6	5	4	3	2	1	0
FRE_SP_TIMEBASE			**FRE_SP_METH**			**FRE_SP_BUCK_IF_EN**	**FRE_SP_EN**
rw			rw			rw	rw

Field	Bits	Type	Description
FRE_SP_EN	0	rw	**Enable spread spectrum** 0_B Disabled 1_B Enabled
FRE_SP_BUCK_IF_EN	1	rw	**Enable spread spectrum for BUCKIF (ignored when FRE_SP_EN is 0)** 0_B Disabled 1_B Enabled
FRE_SP_METH	4:2	rw	**These bits define the method for vary the frequency spectrum** 000_B Triangle 001_B Triangle with dithering 010_B Triangle with pseudorandom period 011_B Triangle with pseudorandom period and dithering 100_B Triangle with pseudorandom half-period 101_B Triangle with pseudorandom half-period and dithering 110_B Triangle with pseudorandom ramp 111_B Triangle with pseudorandom ramp and dithering
FRE_SP_TIMEBASE	7:5	rw	**These bits define the timings for varying the frequency spectrum** 000_B Frequency changes every 3.5 us 001_B Frequency changes every 7 us 010_B Frequency changes every 10.5 us 011_B Frequency changes every 14 us 100_B Frequency changes every 17.5 us 101_B Frequency changes every 21 us 110_B Frequency changes every 24.5 us 111_B Frequency changes every 28 us
FRE_SP_FSTEP	9:8	rw	**These bits define the frequency step for varying the frequency spectrum** 00_B 0.625% variation 01_B 1.25% variation 10_B 2.5% variation 11_B **RESERVED**: Do not use. Currently maps to 2.5% variation

(table continues...)

(continued)

Field	Bits	Type	Description
FRE_SP_AMPLITUDE	13:10	rw	**Defines the maximum width of the triangular ramp with respect to the center value** 0_H 12 frequency steps 1_H 1 frequency step 2_H 2 frequency steps 3_H 3 frequency steps 4_H 4 frequency steps 5_H 5 frequency steps 6_H 6 frequency steps 7_H 7 frequency steps 8_H 8 frequency steps 9_H 9 frequency steps A_H 10 frequency steps B_H 11 frequency steps C_H 12 frequency steps D_H 13 frequency steps E_H 14 frequency steps F_H 15 frequency steps

Table 86 Reset values of FREQ_SPREAD

Reset	Reset value	Note
	0000_H	Reset class R2)

18.32 ABIST control 0 *R2)

ABIST_CTRL0 Offset address: 018_H

ABIST control 0 *R2) Reset values see: Table 87

15	14	13	12	11	10	9	8
Res							**ALL**
r							rwh

7	6	5	4	3	2	1	0
STATUS				**INT**	**SINGLE**	**PATH**	**START**
r				rw	rw	rwh	rwh

Field	Bits	Type	Description
START	0	rwh	**Start ABIST operation, the operation itself will be started. This bit is cleared after ABIST operation has been performed** 0_B Operation done or not started 1_B Start operation
PATH	1	rwh	**Select the path which should be covered by ABIST operation** 0_B Comparator only 1_B Comparator and correspondig deglitching logic
SINGLE	2	rw	**Select whether a single comparator shall be tested or all comparators in predefined sequence** 0_B Predefined sequence 1_B Single comparator test
INT	3	rw	**Selection for safe state related comparators or interrupt related comparators** 0_B Safe state related comparators 1_B Interrupt related comparators
STATUS	7:4	r	**ABIST global status information after requested operation has been performed, information shall only be considered valid, once START bit is cleared** 5_H Selected ABIST operation performed without errors A_H Selected ABIST operation performed with errors, check respective ABIST_SELECTx registers
ALL	8	rwh	**When set to '1' all comparators are automatically selected.** 0_B Comparators executed as selected in ABIST_CTRL0 and ABIST_SELECT0/1/2 1_B All comparators are tested with PATH = 0 and SINGLE = 0

Table 87 Reset values of ABIST_CTRL0

Reset	Reset value	Note
	0000_H	Reset class R2)

18.33 ABIST control 1 *R2)

ABIST_CTRL1 Offset address: 019_H

ABIST control 1 *R2) Reset values see: Table 88

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			SS2_EN_BIST	SS1_EN_BIST	ABIST_CLK_EN	Res	OV_1V5_TRIG
r			rw	rw	rw	r	rw

Field	Bits	Type	Description
OV_1V5_TRIG	0	rw	**Enable overvoltage trigger for protected 1.5 V comparator for analog safe state control** 0_B Disabled 1_B Enabled
ABIST_CLK_EN	2	rw	**Select ABIST clock to generate local 2 MHz clock** 0_B Disable 1_B Enable
SS1_EN_BIST	3	rw	**Enables ABIST for SSO1. Requires ABIST_CTRL1.ABIST_CLK_EN=1 and ABIST_CTRL1.OV_1V5_TRIG=1** 0_B Disable 1_B Enable
SS2_EN_BIST	4	rw	**Enables ABIST for SSO2. Requires ABIST_CTRL1.ABIST_CLK_EN=1 and ABIST_CTRL1.OV_1V5_TRIG=1** 0_B Disable 1_B Enable

Table 88 Reset values of ABIST_CTRL1

Reset	Reset value	Note
	0000_H	Reset class R2)

18.34 ABIST select 0 *R2)

ABIST_SELECT0 Offset address: $01A_H$

ABIST select 0 *R2) Reset values see: Table 89

15	14	13	12	11	10	9	8
R3FBL_OPEN	**BUCKIF_SEVOV**	**BUCKCORE_SEVOV**	**PREREG_SEVOV**	**VDD2V5OV**	**IVCCOV**	**VMON2OV**	**VMON1OV**
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

7	6	5	4	3	2	1	0
BOOSTOV	**BUCKIFOV**	**QVROV**	**QCOOV**	**BUCKCOREOV**	**QSTOV**	**QUCOV**	**PREREGOV**
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
PREREGOV	0	rwh	**Select Pre-regulator OV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
QUCOV	1	rwh	**Select uC LDO OV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
QSTOV	2	rwh	**Select Standby LDO OV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
BUCKCOREOV	3	rwh	**Select Core voltage OV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
QCOOV	4	rwh	**Select COM OV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
QVROV	5	rwh	**Select VREF OV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
BUCKIFOV	6	rwh	**Buck_int OV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator

(table continues...)

(continued)

Field	Bits	Type	Description
BOOSTOV	7	rwh	**BOOST OV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
VMON1OV	8	rwh	**VMON1 OV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
VMON2OV	9	rwh	**VMON2 OV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
IVCCOV	10	rwh	**IVCCOV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
VDD2V5OV	11	rwh	**VDD2V5 OV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
PREREG_SEVOV	12	rwh	**Select Pre-regulator Severe OV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
BUCKCORE_SEVOV	13	rwh	**Select BUCKCORE Severe OV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
BUCKIF_SEVOV	14	rwh	**Select BUCKINT Severe OV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
R3FBL_OPEN	15	rwh	**Select R3FBL comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator

Table 89 Reset values of ABIST_SELECT0

Reset	Reset value	Note
	0000_H	Reset class R2)

18.35 ABIST select 1 *R2)

ABIST_SELECT1 Offset address: $01B_H$

ABIST select 1 *R2) Reset values see: Table 90

15	14	13	12	11	10	9	8
Res		BST_DEEP_UV	BSTIUV	VDD2V5UV	IVCCUV	VMON2UV	VMON1UV
r		rwh	rwh	rwh	rwh	rwh	rwh

7	6	5	4	3	2	1	0
BOOSTUV	BUCKINTUV	QVRUV	QCOUV	BUCKCOREUV	QSTUV	QUCUV	PREREGUV
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
PREREGUV	0	rwh	**Select pre regulator UV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
QUCUV	1	rwh	**Select uC UV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
QSTUV	2	rwh	**Select STBY UV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
BUCKCOREUV	3	rwh	**Select VCORE UV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
QCOUV	4	rwh	**Select COM UV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
QVRUV	5	rwh	**Select VREF UV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
BUCKINTUV	6	rwh	**Select Buck_int UV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator

(table continues...)

(continued)

Field	Bits	Type	Description
BOOSTUV	7	rwh	**Select Boost UV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
VMON1UV	8	rwh	**Select VMON1 UV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
VMON2UV	9	rwh	**Select VMON2 UV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
IVCCUV	10	rwh	**Select IVCC UV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
VDD2V5UV	11	rwh	**Select VDD2V5 UV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
BSTIUV	12	rwh	**BSTI UV comparator for ABIST operation** 0_B No error detected 1_B Error detected (during internal checks)
BST_DEEP_UV	13	rwh	**Select BST_DEEP_UV comparator for ABIST operation** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator

Table 90 Reset values of ABIST_SELECT1

Reset	Reset value	Note
	0000_H	Reset class R2)

18.36 ABIST select 2 *R2)

ABIST_SELECT2 Offset address: $01C_H$

ABIST select 2 *R2) Reset values see: Table 91

15	14	13	12	11	10	9	8
Res							VDD5V0OV
r							rwh

7	6	5	4	3	2	1	0
VDD5V0UV	VDD1V5OV	VDD1V5UV	BIASHI	BIASLOW	BG12OV	BG12UV	VBATOV
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
VBATOV	0	rwh	**Supply voltage VS1/2 is too high** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
BG12UV	1	rwh	**Bandgap comparator UV condition** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
BG12OV	2	rwh	**Bandgap comparator OV condition** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
BIASLOW	3	rwh	**Bias current too low** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
BIASHI	4	rwh	**Bias current too high** 0_B Not selected 1_B Selected; Bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
VDD1V5UV	5	rwh	**Select internal 1.5 V domain undervoltage comparator** 0_B Comparator test not selected 1_B Comparator test selected
VDD1V5OV	6	rwh	**Select internal 1.5 V domain overvoltage comparator** 0_B Comparator test not selected 1_B Comparator test selected
VDD5V0UV	7	rwh	**Select internal 2.5 V domain undervoltage comparator** 0_B Comparator test not selected 1_B Comparator test selected

(table continues...)

(continued)

Field	Bits	Type	Description
VDD5V0OV	8	rwh	**Select internal 2.5 V domain overvoltage comparator** 0_B Comparator test not selected 1_B Comparator test selected

Table 91 Reset values of ABIST_SELECT2

Reset	Reset value	Note
	0000_H	Reset class R2)

18.37 Global testmode *R2)

GTM Offset address: $01D_H$

Global testmode *R2) Reset values see: Table 92

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res						**NTM**	**TM**
r						r	r

Field	Bits	Type	Description
TM	0	r	**Test mode status** 0_B Device is in normal mode 1_B Device is in test mode
NTM	1	r	**Test mode status inverted** 0_B Device is in test mode 1_B Device is in normal mode

Table 92 Reset values of GTM

Reset	Reset value	Note
	0002_H	Reset class R2)

18.38 Reduced operation reflected status configuration 1 register - *R2)

REDOP_RS_CFG1

Reduced operation reflected status configuration 1 register - *R2)

Offset address: $01E_H$

Reset values see: Table 93

15	14	13	12	11	10	9	8
Res	**SSO1TOSSO2_DEL**			**Res**		**INT2_DIS**	**INT1_DIS**
r	r			r		r	r

7	6	5	4	3	2	1	0
SSO2_DEL			**SSO1_DEL**			**Res**	**EN**
r			r			r	r

Field	Bits	Type	Description
EN	0	r	**Enable reduced operation - *R3)** 0_B Disable 1_B Enable
SSO1_DEL	4:2	r	**Safe state output 1 delay (tSSO1_red) - only active if REDUCED OPERATION is enabled** 000_B 0 ms 001_B 10 ms 010_B 50 ms 011_B 100 ms 100_B 250 ms 101_B Do not use. Maps to 0 ms … 111_B Do not use. Maps to 0 ms
SSO2_DEL	7:5	r	**Safe state output 2 delay (tSSO2_red) - only active if REDUCED OPERATION is enabled** 000_B 0 ms 001_B 10 ms 010_B 50 ms 011_B 100 ms 100_B 250 ms 101_B Do not use. Maps to 0 ms … 111_B Do not use. Maps to 0 ms
INT1_DIS	8	r	**Disable generation of INT1 due to Cluster 2 entering REDUCED OPERATION** 0_B Allow generation of INT1 when application 2 enters REDUCED OPERATION 1_B Disable generation of INT1 related to application 2 entering REDUCED OPERATION

(table continues...)

(continued)

Field	Bits	Type	Description
INT2_DIS	9	r	**Disable generation of INT2 due to Cluster 1 entering REDUCED OPERATION** 0_B Allow generation of INT2 when application 1 enters REDUCED OPERATION 1_B Disable generation of INT2 related to application 1 entering REDUCED OPERATION
SSO1TOSSO2_DEL	14:12	r	**Safe state output 2 delay to Safe state output 1 (tSSO2) when REDUCED OPERATION is disabled** 000_B 0 ms 001_B 10 ms 010_B 50 ms 011_B 100 ms 100_B 250 ms 101_B Do not use. Maps to 0 ms … 111_B Do not use. Maps to 0 ms

Table 93 Reset values of REDOP_RS_CFG1

Reset	Reset value	Note
	0000_H	Reset class R2)

18.39 ERR0 protection write configuration register *R2)

ERR0_PW_CFG Offset address: $01F_H$

ERR0 protection write configuration register *R2) Reset values see: Table 94

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			SLP_EN	EN	TREC_EN	TREC	
r			rw	rw	rw	rw	

Field	Bits	Type	Description
TREC	1:0	rw	**ERR0 pin monitor recovery time** 00_B 1 ms 01_B 2.5 ms 10_B 5 ms 11_B 10 ms
TREC_EN	2	rw	**Enabling of recovery time functionality for ERR0 pin monitor** 0_B Disabled 1_B Enabled
EN	3	rw	**Enable ERR0 pin monitor** 0_B Disabled 1_B Enabled
SLP_EN	4	rw	**Enabling of ERR0 pin monitor functionality while the system is in SLEEP state** 0_B Disabled 1_B Enabled

Table 94 Reset values of ERR0_PW_CFG

Reset	Reset value	Note
	0008_H	Reset class R2)

18.40 ERR0 reflected status configuration register *R3)

ERR0_RS_CFG Offset address: 020_H

ERR0 reflected status configuration register *R3) Reset values see: Table 95

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			SLP_EN	EN	TREC_EN	TREC	
r			r	r	r	r	

Field	Bits	Type	Description
TREC	1:0	r	**ERR0 pin monitor recovery time** 00_B 1 ms 01_B 2.5 ms 10_B 5 ms 11_B 10 ms
TREC_EN	2	r	**Enabling of recovery time functionality for ERR0 pin monitor** 0_B Disabled 1_B Enabled
EN	3	r	**Enable ERR0 pin monitor** 0_B Disabled 1_B Enabled
SLP_EN	4	r	**Enabling of ERR0 pin monitor functionality while the system is in SLEEP state** 0_B Disabled 1_B Enabled

Table 95 Reset values of ERR0_RS_CFG

Reset	Reset value	Note
	0008_H	Reset class R3) C1

18.41 ERR1 protection write configuration register *R2)

ERR1_PW_CFG Offset address: 021_H

ERR1 protection write configuration register *R2) Reset values see: Table 96

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			**SLP_EN**	**EN**	**TREC_EN**	**TREC**	
r			rw	rw	rw	rw	

Field	Bits	Type	Description
TREC	1:0	rw	**ERR1 pin monitor recovery time** 00_B 1 ms 01_B 2.5 ms 10_B 5 ms 11_B 10 ms
TREC_EN	2	rw	**Enabling of recovery time functionality for ERR1 pin monitor** 0_B Disabled 1_B Enabled
EN	3	rw	**Enable ERR1 pin monitor** 0_B Disabled 1_B Enabled
SLP_EN	4	rw	**Enabling of ERR1 pin monitor functionality while the system is in SLEEP state** 0_B Disabled 1_B Enabled

Table 96 Reset values of ERR1_PW_CFG

Reset	Reset value	Note
	0008_H	Reset class R2)

18.42 ERR1 reflected status configuration register *R3_C1)

ERR1_RS_CFG Offset address: 022_H

ERR1 reflected status configuration register *R3_C1) Reset values see: Table 97

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			SLP_EN	EN	TREC_EN	TREC	
r			r	r	r	r	

Field	Bits	Type	Description
TREC	1:0	r	**ERR1 pin monitor recovery time** 00_B 1 ms 01_B 2.5 ms 10_B 5 ms 11_B 10 ms
TREC_EN	2	r	**Enabling of recovery time functionality for ERR1 pin monitor** 0_B Disabled 1_B Enabled
EN	3	r	**Enable ERR1 pin monitor** 0_B Disabled 1_B Enabled
SLP_EN	4	r	**Enabling of ERR1 pin monitor functionality while the system is in SLEEP state** 0_B Disabled 1_B Enabled

Table 97 Reset values of ERR1_RS_CFG

Reset	Reset value	Note
	0008_H	Reset class R3) C1

18.43 ERR2 protection write configuration register *R2)

ERR2_PW_CFG Offset address: 023_H

ERR2 protection write configuration register *R2) Reset values see: Table 98

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			**SLP_EN**	**EN**	**TREC_EN**	**TREC**	
r			rw	rw	rw	rw	

Field	Bits	Type	Description
TREC	1:0	rw	**ERR2 pin monitor recovery time** 00_B 1 ms 01_B 2.5 ms 10_B 5 ms 11_B 10 ms
TREC_EN	2	rw	**Enabling of recovery time functionality for ERR2 pin monitor** 0_B Disabled 1_B Enabled
EN	3	rw	**Enable ERR2 pin monitor** This bit has only an effect if REDOP_RS_CFG1.EN is 1 0_B Disabled 1_B Enabled
SLP_EN	4	rw	**Enabling of ERR2 pin monitor functionality while the system is in SLEEP state** 0_B Disabled 1_B Enabled

Table 98 Reset values of ERR2_PW_CFG

Reset	Reset value	Note
	0008_H	Reset class R2)

18.44 ERR2 reflected status configuration register *R3_C2)

ERR2_RS_CFG Offset address: 024_H

ERR2 reflected status configuration register *R3_C2) Reset values see: Table 99

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			SLP_EN	EN	TREC_EN	TREC	
r			r	r	r	r	

Field	Bits	Type	Description
TREC	1:0	r	**ERR2 pin monitor recovery time** 00_B 1 ms 01_B 2.5 ms 10_B 5 ms 11_B 10 ms
TREC_EN	2	r	**Enabling of recovery time functionality for ERR2 pin monitor** 0_B Disabled 1_B Enabled
EN	3	r	**Enable ERR2 pin monitor** This bit has only an effect if REDOP_RS_CFG1.EN is 1 0_B Disabled 1_B Enabled
SLP_EN	4	r	**Enabling of ERR2 pin monitor functionality while the system is in SLEEP state** 0_B Disabled 1_B Enabled

Table 99 Reset values of ERR2_RS_CFG

Reset	Reset value	Note
	0008_H	Reset class R3) C2

18.45 Device configuration 1 register *R0)

DEV_CFG1 Offset address: 025_H

Device configuration 1 register *R0) value: 0206_H

15	14	13	12	11	10	9	8
Res						**ABIST_EN**	**Res**
r						rw	r

7	6	5	4	3	2	1	0
HWCFG_STAT				**MPS_EN**	**RESET_DEL**		
r				rwh	rwh		

Field	Bits	Type	Description
RESET_DEL	2:0	rwh	**Reset delay time (tRD); Starts upon QST, QUC and BUCKCORE are above their UV thresholds.** 000_B 200 µs 001_B 400 µs 010_B 800 µs 011_B 1 ms 100_B 2 ms 101_B 4 ms 110_B 10 ms 111_B 20 ms
MPS_EN	3	rwh	**Microcontroller programming support enable** 0_B Disabled 1_B Enabled
HWCFG_STAT	7:4	r	**This bit reflects the status of the hardware configuration pin** 0_H 1 kOhm 1_H 2.2 kOhm 2_H 3.3 kOhm 3_H 4.7 kOhm 4_H 6.8 kOhm 5_H 10 kOhm 6_H 15 kOhm 7_H Reserved value 8_H Reserved value 9_H 22 kOhm A_H 33 kOhm B_H 47 kOhm C_H 68 kOhm D_H 100 kOhm E_H 150 kOhm F_H 200 kOhm

(table continues...)

(continued)

Field	Bits	Type	Description
ABIST_EN	9	rw	**Autostart of analog built in self test for voltage monitoring when waking up from FAILSAFE, STANDBY and POWERDOWN.** 0_B ABIST only executed when waking up from STANDBY (if WUT and QST are both OFF) or from POWERDOWN 1_B ABIST executed when waking up from STANDBY or from POWERDOWN or from FAILSAFE

18.46 Device protected write configuration 2 register *R0)

DEV_PW_CFG2 Offset address: 026_H

Device protected write configuration 2 register *R0) value: $F001_H$

15	14	13	12	11	10	9	8
VMON2_STG_TIME		**VMON1_STG_TIME**		**Res**			
rw		rw		r			

7	6	5	4	3	2	1	0
Res				**QST_MODE**	**SSW_OC_TH**		**QST_EN**
r				rw	rw		rw

Field	Bits	Type	Description
QST_EN	0	rw	**Activation of standby LDO** 0_B Disabled 1_B Enabled
SSW_OC_TH	2:1	rw	**Safety switch overcurrent detection threshold.** 00_B 0.755 V 01_B 0.944 V 10_B 1.04 V 11_B 1.22 V
QST_MODE	3	rw	**Selects between 2 different modes of controlling standby LDO via QSTEN** 0_B **PMIC_MODE**: QST is selectable only when the device is moving to STANDBY. QST is on in all other states, independently of QST_EN. 1_B **USER_MODE**: QST supply on or off,can be configured by QST_EN
VMON1_STG_TIME	13:12	rw	**Filter time to detect a short-to-ground on external voltage monitor channel 1** 00_B 1 ms 01_B 2 ms 10_B 4 ms 11_B 6 ms
VMON2_STG_TIME	15:14	rw	**Filter t ime to detect a short-to-ground on external voltage monitor channel 2** 00_B 1 ms 01_B 2 ms 10_B 4 ms 11_B 6 ms

18.47 Device reflected status configuration 2 register *R0)

DEV_RS_CFG2 Offset address: 027_H

Device reflected status configuration 2 register *R0) value: $F001_H$

15	14	13	12	11	10	9	8
VMON2_STG_TIME		**VMON1_STG_TIME**		**Res**			
r		r		r			

7	6	5	4	3	2	1	0
Res				**QST_MODE**	**SSW_OC_TH**		**QST_EN**
r				r	r		r

Field	Bits	Type	Description
QST_EN	0	r	**Activation of standby LDO** 0_B Disabled 1_B Enabled
SSW_OC_TH	2:1	r	**Safety switch overcurrent detection threshold.** 00_B 0.755 V 01_B 0.944 V 10_B 1.04 V 11_B 1.22 V
QST_MODE	3	r	**Selects between 2 different modes of controlling standby LDO via QSTEN** 0_B **PMIC_MODE**: QST is selectable only when the device is moving to STANDBY. QST is on in all other states, independently of QST_EN. 1_B **USER_MODE**: QST supply on or off,can be configured by QST_EN
VMON1_STG_TIME	13:12	r	**Time to detect a short-to-ground on external voltage monitor channel 1** 00_B 1 ms 01_B 2 ms 10_B 4 ms 11_B 6 ms
VMON2_STG_TIME	15:14	r	**Time to detect a short-to-ground on external voltage monitor channel 2** 00_B 1 ms 01_B 2 ms 10_B 4 ms 11_B 6 ms

18.48 System failure status register for application 1 *R1)

SYSFAIL_STAT_APP1 Offset address: 029_H

System failure status register for application 1 *R1) Reset values see: Table 100

15	14	13	12	11	10	9	8
Res				**ABIST**	**CFGE**	**PREREG_COSW**	**INTSUP_IVCC**
r				rw1c	rw1c	rw1c	rw1c

7	6	5	4	3	2	1	0
QST	**ERR0**	**FSM_INITTIMER**	**VMON**	**OT**	**BUCK_CORE_VOLTSEL**	**BUCKIF_VOLTSEL**	**QST_QUC_VOLTSEL**
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
QST_QUC_VOLTSEL	0	rw1c	**QST and QUC voltage selection error. Nominal voltage of QST and QUC might be corrupt (3.3 V or 5 V).** 0_B No occurrence 1_B Fault occurred
BUCKIF_VOLTSEL	1	rw1c	**BUCK IF voltage selection error. Nominal voltage of BUCKIF might be corrupt (1.8 V or 3.3 V).** 0_B No occurrence 1_B Fault occurred
BUCK_CORE_VOLTSEL	2	rw1c	**BUCK CORE voltage selection error. Nominal voltage of BUCKCORE might be corrupt.** 0_B No occurrence 1_B Fault occurred
OT	3	rw1c	**Over temperature failure. (see chapter: Collection registers)** 0_B No fault 1_B Fault occurred
VMON	4	rw1c	**Voltage monitor failure (see chapter: Collection registers)** 0_B No fault 1_B Fault occurred
FSM_INITTIMER	5	rw1c	**Init timer failure due to the third INIT failure in row. The device moved to FAILSAFE state.** 0_B No fault 1_B Fault occurred
ERR0	6	rw1c	**ERR0 failure** 0_B No fault 1_B Fault occurred
QST	7	rw1c	**Standby LDO (QST) failure; Also set if BIST of QST retunred an error** 0_B No fault 1_B Fault occurred

(table continues...)

(continued)

Field	Bits	Type	Description
INTSUP_IVCC	8	rw1c	**Internal supply IVCC failure; Also set if BIST of QIS retunred an error** 0_B No fault 1_B Fault occurred
PREREG_COSW	9	rw1c	**Reports major faults detected during SSW BIST and overcurrent on SSW** 0_B No fault 1_B Fault occurred
CFGE	10	rw1c	**DED for Cluster1 config registers** 0_B Write 0 - no action 1_B Event detected, write 1 to clear the flag
ABIST	11	rw1c	**ABIST operation interrupted by move to INIT or move to FAILSAFE fault** 0_B No fault 1_B Fault occurred

Table 100 Reset values of SYSFAIL_STAT_APP1

Reset	Reset value	Note
	0000_H	Reset class R1)

18.49 System failure status flags for application 2 *R1)

SYSFAIL_STAT_APP2 Offset address: $02A_H$

System failure status flags for application 2 *R1) Reset values see: Table 101

15	14	13	12	11	10	9	8
Res				ABIST	CFGE	PREREG_COSW	INTSUP_IVCC
r				rw1c	rw1c	rw1c	rw1c

7	6	5	4	3	2	1	0
QST	ERR0	FSM_INITTIMER	VMON	OT	BUCK_CORE_VOLTSEL	BUCKIF_VOLTSEL	QST_QUC_VOLTSEL
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
QST_QUC_VOLTSEL	0	rw1c	**QST and QUC voltage selection error. Nominal voltage of QST and QUC might be corrupt (3.3 V or 5 V).** 0_B No occurrence 1_B Fault occurred
BUCKIF_VOLTSEL	1	rw1c	**BUCK IF voltage selection error. Nominal voltage of BUCKIF might be corrupt (1.8 V or 3.3 V).** 0_B No occurrence 1_B Fault occurred
BUCK_CORE_VOLTSEL	2	rw1c	**BUCK CORE voltage selection error. Nominal voltage of BUCKCORE might be corrupt.** 0_B No occurrence 1_B Fault occurred
OT	3	rw1c	**Over temperature failure (see chapter: Collection registers)** 0_B No occurrence 1_B Fault occurred
VMON	4	rw1c	**Voltage monitor failure (see chapter: Collection registers)** 0_B No occurrence 1_B Fault occurred
FSM_INITTIMER	5	rw1c	**Init timer failure due to the third INIT failure in row. The device moved to FAILSAFE state.** 0_B No occurrence 1_B Fault occurred
ERR0	6	rw1c	**ERR0 failure** 0_B No occurrence 1_B Fault occurred
QST	7	rw1c	**Standby LDO (QST) failure** 0_B No occurrence 1_B Fault occurred

(table continues...)

(continued)

Field	Bits	Type	Description
INTSUP_IVCC	8	rw1c	**Internal supply IVCC failure** 0_B No occurrence 1_B Fault occurred
PREREG_COSW	9	rw1c	**Reports severe faults detected during SSW BIST** 0_B No occurrence 1_B Fault occurred
CFGE	10	rw1c	**DED for Cluster 2 config registers** 0_B Write 0 - no action 1_B Event detected, write 1 to clear the flag
ABIST	11	rw1c	**ABIST operation interrupted by move to INIT or move to FAILSAFE fault** 0_B No occurrence 1_B Fault occurred

Table 101 Reset values of SYSFAIL_STAT_APP2

Reset	Reset value	Note
	0000_H	Reset class R1)

18.50 Short to ground status register for application 1 *R1)

STG_STAT_APP1 Offset address: $02B_H$

Short to ground status register for application 1 *R1) Reset values see: Table 102

15	14	13	12	11	10	9	8
Res						VMON2	VMON1
r						rw1c	rw1c

7	6	5	4	3	2	1	0
BOOST	BUCKIF	QVR	QCO	BUCKCORE	QST	QUC	PREREG
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
PREREG	0	rw1c	**Pre-regulator voltage short to ground status flag** 0_B No fault 1_B Fault occurred
QUC	1	rw1c	**MCU LDO short to ground status flag** 0_B No fault 1_B Fault occurred
QST	2	rw1c	**Standby LDO short to ground status flag** 0_B No fault 1_B Fault occurred
BUCKCORE	3	rw1c	**Buckcore voltage short to ground status flag** 0_B No fault 1_B Fault occurred
QCO	4	rw1c	**Communication LDO short to ground status flag** 0_B No fault 1_B Fault occurred
QVR	5	rw1c	**Reference LDO short to groung status flag** 0_B No fault 1_B Fault occurred
BUCKIF	6	rw1c	**Buck interface short to ground status flag** 0_B No fault 1_B Fault occurred
BOOST	7	rw1c	**Boost short to ground status flag** 0_B No fault 1_B Event detected
VMON1	8	rw1c	**VMON1 short to ground status flag** 0_B No fault 1_B Fault occurred
VMON2	9	rw1c	**VMON2 short to ground status flag** 0_B No fault 1_B Fault occurred

Table 102 Reset values of STG_STAT_APP1

Reset	Reset value	Note
	0000_H	Reset class R1)

18.51 Short to ground status register for application 2 *R1)

STG_STAT_APP2 Offset address: $02C_H$

Short to ground status register for application 2 *R1) Reset values see: Table 103

15	14	13	12	11	10	9	8
Res						VMON2	VMON1
r						rw1c	rw1c

7	6	5	4	3	2	1	0
BOOST	BUCKIF	QVR	QCO	BUCKCORE	QST	QUC	PREREG
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
PREREG	0	rw1c	**Pre-regulator voltage short to ground status flag** 0_B No fault 1_B Fault occurred
QUC	1	rw1c	**MCU LDO short to ground status flag** 0_B No fault 1_B Fault occurred
QST	2	rw1c	**Standby LDO short to ground status flag** 0_B No fault 1_B Fault occurred
BUCKCORE	3	rw1c	**Buckcore voltage short to ground status flag** 0_B No fault 1_B Fault occurred
QCO	4	rw1c	**Communication LDO short to ground status flag** 0_B No fault 1_B Fault occurred
QVR	5	rw1c	**Voltage reference short to groung status flag** 0_B No fault 1_B Fault occurred
BUCKIF	6	rw1c	**Buckint short to ground status flag** 0_B No fault 1_B Fault occurred
BOOST	7	rw1c	**Boost short to ground status flag** 0_B No fault 1_B Fault occurred
VMON1	8	rw1c	**VMON1 short to ground status flag** 0_B No fault 1_B Fault occurred
VMON2	9	rw1c	**VMON2 short to ground status flag** 0_B No fault 1_B Fault occurred

Table 103 Reset values of STG_STAT_APP2

Reset	Reset value	Note
	0000_H	Reset class R1)

18.52 Overvoltage status register for application 1 *R1)

OV_STAT_APP1 Offset address: $02D_H$

Overvoltage status register for application 1 *R1) Reset values see: Table 104

15	14	13	12	11	10	9	8
Res			BUCKCORE_FB_OPEN	INTSUP_VDD2V5	INTSUP_IVCC	BUCKIF	PREREG
r			rw1c	rw1c	rw1c	rw1c	rw1c

7	6	5	4	3	2	1	0
VMON2	VMON1	BOOST	QVR	QCO	BUCKCORE	QST	QUC
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
QUC	0	rw1c	**QUC over voltage status flag** 0_B No fault 1_B Fault occurred
QST	1	rw1c	**Standby LDO QST over voltage status flag** 0_B No fault 1_B Fault occurred
BUCKCORE	2	rw1c	**BUCKCORE over voltage status flag** 0_B No fault 1_B Fault occurred
QCO	3	rw1c	**QCO over voltage status flag** 0_B No fault 1_B Fault occurred
QVR	4	rw1c	**QVR over voltage status flag** 0_B No fault 1_B Fault occurred
BOOST	5	rw1c	**BOOST over voltage status flag** 0_B No fault 1_B Fault occurred
VMON1	6	rw1c	**External volatage monitor channel 1 over voltage status flag** 0_B No fault 1_B Fault occurred
VMON2	7	rw1c	**External volatage monitor channel 2 over voltage status flag** 0_B No fault 1_B Fault occurred
PREREG	8	rw1c	**Pre-regulator over voltage status flag** 0_B No fault 1_B Fault occurred

(table continues...)

(continued)

Field	Bits	Type	Description
BUCKIF	9	rw1c	**Buck interface over voltage status flag** 0_B No fault 1_B Fault occurred
INTSUP_IVCC	10	rw1c	**Internal supply IVCC LDO over voltage status flag (Internal monitoring)** 0_B No fault 1_B Fault occurred
INTSUP_VDD2V5	11	rw1c	**Internal supply VDD 2V5 LDO over voltage status flag (Internal monitoring)** 0_B No fault 1_B Fault occurred
BUCKCORE_FB_OPEN	12	rw1c	**BUCKCORE feedback open status flag** 0_B No fault 1_B Fault occurred

Table 104 Reset values of OV_STAT_APP1

Reset	Reset value	Note
	0000_H	Reset class R1)

18.53 Overvoltage status register for application 2 *R1)

OV_STAT_APP2 Offset address: $02E_H$

Overvoltage status register for application 2 *R1) Reset values see: Table 105

15	14	13	12	11	10	9	8
Res			BUCKCORE_GND_OPEN	VDD2V5OV	INTSUP_IVCC	BUCKIF	PREREG
	r		rw1c	rw1c	rw1c	rw1c	rw1c

7	6	5	4	3	2	1	0
VMON2	VMON1	BOOST	QVR	QCO	BUCKCORE	QST	QUC
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
QUC	0	rw1c	**MCU LDO over voltage status flag** 0_B No fault 1_B Fault occurred
QST	1	rw1c	**Standby LDO QST over voltage status flag** 0_B No fault 1_B Fault occurred
BUCKCORE	2	rw1c	**BUCKCORE over voltage status flag** 0_B No fault 1_B Fault occurred
QCO	3	rw1c	**QCO over voltage status flag** 0_B No fault 1_B Fault occurred
QVR	4	rw1c	**QVR over voltage status flag** 0_B No fault 1_B Fault occurred
BOOST	5	rw1c	**BOOST over voltage status flag** 0_B No fault 1_B Fault occurred
VMON1	6	rw1c	**External volatage monitor channel 1 over voltage status flag** 0_B No fault 1_B Fault occurred
VMON2	7	rw1c	**External volatage monitor channel 2 over voltage status flag** 0_B No fault 1_B Fault occurred
PREREG	8	rw1c	**Pre-regulator over voltage status flag** 0_B No fault 1_B Fault occurred

(table continues...)

(continued)

Field	Bits	Type	Description
BUCKIF	9	rw1c	**BUCKIF over voltage status flag** 0_B No fault 1_B Fault occurred
INTSUP_IVCC	10	rw1c	**Internal supply IVCC LDO over voltage status flag (Internal monitoring)** 0_B No fault 1_B Fault occurred
VDD2V5OV	11	rw1c	**Internal supply VDD 2V5 LDO over voltage status flag (Internal monitoring)** 0_B No fault 1_B Fault occurred
BUCKCORE_GND_OPEN	12	rw1c	**Buckcore ground open status flag** 0_B No fault 1_B Fault occurred

Table 105 Reset values of OV_STAT_APP2

Reset	Reset value	Note
	0000_H	Reset class R1)

18.54 Internal supply status register for application 1 *R1)

INTSUP_STAT_APP1 Offset address: $02F_H$

Internal supply status register for application 1 *R1) Reset values see: Table 106

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res	**PMU_RED**	**PMU_MAIN**	**BIAS_HI**	**BIAS_LOW**	**BG12_OV**	**BG12_UV**	**VBAT_OV**
r	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
VBAT_OV	0	rw1c	**Battery voltage supply (VS) over voltage** 0_B No fault 1_B Fault occurred
BG12_UV	1	rw1c	**Internal bandgap comparator detected UV condition (Internal monitoring)** 0_B No fault 1_B Fault occurred
BG12_OV	2	rw1c	**Internal bandgap comparator detected OV condition (Internal monitoring)** 0_B No fault 1_B Fault occurred
BIAS_LOW	3	rw1c	**Internal bias current too low (Internal monitoring)** 0_B No fault 1_B Fault occurred
BIAS_HI	4	rw1c	**Internal bias current too high (Internal monitoring)** 0_B No fault 1_B Fault occurred
PMU_MAIN	5	rw1c	**PMU main pass element fail (Internal monitoring)** 0_B No fault 1_B Fault occurred
PMU_RED	6	rw1c	**PMU redundant pass element fail (Internal monitoring)** 0_B No fault 1_B Fault occurred

Table 106 Reset values of INTSUP_STAT_APP1

Reset	Reset value	Note
	0000_H	Reset class R1)

18.55 Internal supply status register for application 2 *R1)

INTSUP_STAT_APP2 Offset address: 030_H

Internal supply status register for application 2 *R1) Reset values see: Table 107

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res	**PMU_RED**	**PMU_MAIN**	**BIAS_HI**	**BIAS_LOW**	**BG12_OV**	**BG12_UV**	**VBAT_OV**
r	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
VBAT_OV	0	rw1c	**Battery voltage supply (VS) over voltage** 0_B No fault 1_B Fault occurred
BG12_UV	1	rw1c	**Internal bandgap comparator detected UV condition (Internal monitoring)** 0_B No fault 1_B Fault occurred
BG12_OV	2	rw1c	**Internal bandgap comparator detected OV condition (Internal monitoring)** 0_B No fault 1_B Fault occurred
BIAS_LOW	3	rw1c	**Internal bias current too low (Internal monitoring)** 0_B No fault 1_B Fault occurred
BIAS_HI	4	rw1c	**Internal bias current too high (Internal monitoring)** 0_B No fault 1_B Fault occurred
PMU_MAIN	5	rw1c	**PMU main pass element fail (Internal monitoring)** 0_B No fault 1_B Fault occurred
PMU_RED	6	rw1c	**PMU redundant pass element fail (Internal monitoring)** 0_B No fault 1_B Fault occurred

Table 107 Reset values of INTSUP_STAT_APP2

Reset	Reset value	Note
	0000_H	Reset class R1)

18.56 Over temperature status register for application 1 *R1)

OT_STAT_APP1 Offset address: 031_H

Over temperature status register for application 1 *R1) Reset values see: Table 108

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res		**BOOST**	**BUCKIF**	**BUCKCORE**	**SAFETY_AREA**	**QCO**	**QUC**
r		rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
QUC	0	rw1c	**QUC over temperature** 0_B No fault 1_B Fault occurred
QCO	1	rw1c	**QCO over temperature** 0_B No fault 1_B Fault occurred
SAFETY_AREA	2	rw1c	**Over temperature of Safety area temperature sensor** 0_B No fault 1_B Fault occurred
BUCKCORE	3	rw1c	**Buckcore over temperature** 0_B No fault 1_B Fault occurred
BUCKIF	4	rw1c	**BUCKIF over temperature** 0_B No fault 1_B Fault occurred
BOOST	5	rw1c	**BOOST over temperature** 0_B No fault 1_B Fault occurred

Table 108 Reset values of OT_STAT_APP1

Reset	Reset value	Note
	0000_H	Reset class R1)

18.57 Over temperature status register for application 2 *R1)

OT_STAT_APP2 Offset address: 032_H

Over temperature status register for application 2 *R1) Reset values see: Table 109

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res		**BOOST**	**BUCKIF**	**BUCKCORE**	**SAFETY_AREA**	**QCO**	**QUC**
r		rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
QUC	0	rw1c	**QUC over temperature** 0_B No fault 1_B Fault occurred
QCO	1	rw1c	**QCO over temperature** 0_B No fault 1_B Fault occurred
SAFETY_AREA	2	rw1c	**Over temperature of Safety area temperature sensor** 0_B No fault 1_B Fault occurred
BUCKCORE	3	rw1c	**BUCKCORE over temperature** 0_B No fault 1_B Fault occurred
BUCKIF	4	rw1c	**BUCKIF over temperature** 0_B No fault 1_B Fault occurred
BOOST	5	rw1c	**BOOST over temperature** 0_B No fault 1_B Fault occurred

Table 109 Reset values of OT_STAT_APP2

Reset	Reset value	Note
	0000_H	Reset class R1)

18.58 Protection status *R1)

PROT_STAT Offset address: 033_H

Protection status *R1) Reset values see: Table 110

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res							**LOCK**
r							r

Field	Bits	Type	Description
LOCK	0	r	**Protected register password status** 0_B Registers unlocked 1_B Registers locked

Table 110 Reset values of PROT_STAT

Reset	Reset value	Note
	0001_H	Reset class R1)

18.59 Reduced operation protected write configuration 1 register - *R1)

This register contains configuration related to the reduce operation mode. All setting will be applied if reduce operation mode is enabled (EN = 1).

REDOP_PW_CFG1

Offset address: 034_H

Reduced operation protected write configuration 1 register - *R1)

Reset values see: Table 111

15	14	13	12	11	10	9	8
Res	**SSO1TOSSO2_DEL**			**Res**		**INT2_DIS**	**INT1_DIS**
r	rw			r		rw	rw

7	6	5	4	3	2	1	0
SSO2_DEL			**SSO1_DEL**			**Res**	**EN**
rw			rw			r	rw

Field	Bits	Type	Description
EN	0	rw	**Enable reduced operation *R2)** 0_B Disabled 1_B Enabled
SSO1_DEL	4:2	rw	**Safe state output 1 delay (tSSO1_red)** 000_B 0 ms 001_B 10 ms 010_B 50 ms 011_B 100 ms 100_B 250 ms 101_B Do not use. Maps to 0 ms … 111_B Do not use. Maps to 0 ms
SSO2_DEL	7:5	rw	**Safe state output 2 delay (tSSO2_red)** 000_B 0 ms 001_B 10 ms 010_B 50 ms 011_B 100 ms 100_B 250 ms 101_B Do not use. Maps to 0 ms … 111_B Do not use. Maps to 0 ms
INT1_DIS	8	rw	**Disable generation of INT1 due to Cluster 2 entering REDUCED OPERATION** 0_B Allow generation of INT1 when Cluster 2 enters REDUCED OPERATION 1_B Disable generation of INT1 related to Cluster 2 entering REDUCED OPERATION

(table continues...)

(continued)

Field	Bits	Type	Description
INT2_DIS	9	rw	**Disable generation of INT2 due to Cluster 1 entering REDUCED OPERATION** 0_B Allow generation of INT2 when Cluster 1 enters REDUCED OPERATION 1_B Disable generation of INT2 related to Cluster 1 entering REDUCED OPERATION
SSO1TOSSO2_DEL	14:12	rw	**Safe state output 2 delay to Safe state output 1 (tSSO2) when REDUCED OPERATION is disabled** 000_B 0 ms 001_B 10 ms 010_B 50 ms 011_B 100 ms 100_B 250 ms 101_B Do not use. Maps to 0 ms … 111_B Do not use. Maps to 0 ms

Table 111 Reset values of REDOP_PW_CFG1

Reset	Reset value	Note
	0000_H	Reset class R1)

18.60 Reduced operation protected write configuration 2 register - *R1)

This register contains configuration related to the reduce operation mode. All setting will be applied if reduce operation mode is enabled (EN = 1).

REDOP_PW_CFG2

Reduced operation protected write configuration 2 register - *R1)

Offset address: 035_H

Reset values see: Table 112

15	14	13	12	11	10	9	8
REDOP_RESOUT_APP2_DUR			REDOP_RESOUT_APP1_DUR			REDOP_RESOUT_APP_TB	Res
rw			rw			rw	r

7	6	5	4	3	2	1	0
Res							
r							

Field	Bits	Type	Description
REDOP_RESOUT_APP_TB	9	rw	**Reset timer time base for application reset pulse** 0_B 10 µs 1_B 100 µs
REDOP_RESOUT_APP1_DUR	12:10	rw	**Application reset pulse duration for INT1** 000_B (0 + 1)*10 µs for REDOP_RESOUT_APP_TB = 0; ((0 + 1)*100 + 50) µs for REDOP_RESOUT_APP_TB = 1 … 111_B (7 + 1)*10 µs for REDOP_RESOUT_APP_TB = 0; ((7 + 1)*100 + 50) µs for REDOP_RESOUT_APP_TB = 1
REDOP_RESOUT_APP2_DUR	15:13	rw	**Application reset pulse duration for INT2** 000_B (0 + 1)*10 µs for REDOP_RESOUT_APP_TB = 0; ((0 + 1)*100 + 50) µs for REDOP_RESOUT_APP_TB = 1 … 111_B (7 + 1)*10 µs for REDOP_RESOUT_APP_TB = 0; ((7 + 1)*100 + 50) µs for REDOP_RESOUT_APP_TB = 1

Table 112 Reset values of REDOP_PW_CFG2

Reset	Reset value	Note
	0000_H	Reset class R1)

18.61 Device protected write configuration 3 register *R1)

DEV_PW_CFG3 Offset address: 036_H

Device protected write configuration 3 register *R1) Reset values see: Table 113

15	14	13	12	11	10	9	8
Res					VMON2_EN	VMON1_EN	BOOST_EN
r					rw	rw	rw

7	6	5	4	3	2	1	0
BUCKIF_EN	QUCEN	BUCKCORE_EN	QCO_EN	QVR_EN	FSM_STATEREQ		
rw	rw	rw	rw	rw	rw		

Field	Bits	Type	Description
FSM_STATEREQ	2:0	rw	**Request for device state transition.** 000_B NONE 001_B INIT 010_B NORMAL 011_B SLEEP 100_B STANDBY 101_B WAKE 110_B NONE 111_B NONE
QVR_EN	3	rw	**Enable request for reference voltage.** 0_B Disabled 1_B Enabled
QCO_EN	4	rw	**Enable request for communication LDO.** 0_B Disabled 1_B Enabled
BUCKCORE_EN	5	rw	**Enable request for BUCKCORE.** 0_B Disabled 1_B Enabled
QUCEN	6	rw	**Enable request for QUC.** 0_B Disabled 1_B Enabled
BUCKIF_EN	7	rw	**Enable request for Buck interface.** 0_B Disabled 1_B Enabled
BOOST_EN	8	rw	**Enable request for Boost.** 0_B Disabled 1_B Enabled

(table continues...)

(continued)

Field	Bits	Type	Description
VMON1_EN	9	rw	**Enable request for external voltage monitoring channel 1.** 0_B Disabled 1_B Enabled
VMON2_EN	10	rw	**Enable request for external voltage monitoring channel 2.** 0_B Disabled 1_B Enabled

Table 113 Reset values of DEV_PW_CFG3

Reset	Reset value	Note
	0000_H	Reset class R1)

18.62 Watchdog 1 protected write configuration 0 register *R2)

WD1_PW_CFG0

Watchdog 1 protected write configuration 0 register *R2)

Offset address: 037_H

Reset values see: Table 114

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
WWD_ETHR				**WWD_EN**	**FWD_EN**	**WWD_TSEL**	**CYC**
rw				rw	rw	rw	rw

Field	Bits	Type	Description
CYC	0	rw	**Watchdog 1 cycle time** 0_B 0.1 ms tick period 1_B 1 ms tick period
WWD_TSEL	1	rw	**Window watchdog (WWD1) trigger selection** 0_B External WDI input used as a WWD trigger 1_B WWD is triggered by SPI
FWD_EN	2	rw	**Functional watchdog (FWD1) enable** 0_B Disabled 1_B Enabled
WWD_EN	3	rw	**Window watchdog (WWD1) enable** 0_B Disabled 1_B Enabled
WWD_ETHR	7:4	rw	**Window watchdog error counter threshold.**

Table 114 Reset values of WD1_PW_CFG0

Reset	Reset value	Note
	$009B_H$	Reset class R2)

18.63 Watchdog 1 reflected status configuration 0 register - *R3_C1

WD1_RS_CFG0

Watchdog 1 reflected status configuration 0 register - *R3_C1

Offset address: 038_H

Reset values see: Table 115

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
WWD_ETHR				**WWD_EN**	**FWD_EN**	**WWD_TSEL**	**CYC**
r				r	r	r	r

Field	Bits	Type	Description
CYC	0	r	**Watchdog 1 cycle time** 0_B 0.1 ms tick period 1_B 1 ms tick period
WWD_TSEL	1	r	**Window watchdog (WWD1) trigger selection.** 0_B External WDI input used as a WWD trigger 1_B WWD is triggered by SPI
FWD_EN	2	r	**Functional watchdog enable (FWD1)** 0_B Disabled 1_B Enabled
WWD_EN	3	r	**Window watchdog enable (WWD1)** 0_B Disabled 1_B Enabled
WWD_ETHR	7:4	r	**Window watchdog error threshold.**

Table 115 Reset values of WD1_RS_CFG0

Reset	Reset value	Note
	$009B_H$	Reset class R3) C1

18.64 Watchdog 1 protected write configuration 1 register *R2)

WD1_PW_CFG1

Watchdog 1 protected write configuration 1 register *R2)

Offset address: 039_H

Reset values see: Table 116

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res		CYC_DIV	SLP_EN	FWD_ETHR			
r		rw	rw	rw			

Field	Bits	Type	Description
FWD_ETHR	3:0	rw	**Functional watchdog error threshold.**
SLP_EN	4	rw	**Watchdog1 is active in sleep state** 0_B Disabled 1_B Enabled
CYC_DIV	5	rw	**Apply an additional divider of 10 to the cycle time** 0_B Disabled 1_B Enabled

Table 116 Reset values of WD1_PW_CFG1

Reset	Reset value	Note
	0009_H	Reset class R2)

18.65 Watchdog 1 reflected status configuration 1 register- *R3_C1

WD1_RS_CFG1

Offset address: $03A_H$

Watchdog 1 reflected status configuration 1 register- *R3_C1

Reset values see: Table 117

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res		CYC_DIV	SLPEN	FWD_ETHR			
r		r	r	r			

Field	Bits	Type	Description
FWD_ETHR	3:0	r	**Functional watchdog error threshold.**
SLPEN	4	r	**Watchdog1 is active in sleep state** 0_B Disabled 1_B Enabled
CYC_DIV	5	r	**Additional divider of 10 to the cycle time is applied** 0_B Disabled 1_B Enabled

Table 117 Reset values of WD1_RS_CFG1

Reset	Reset value	Note
	0009_H	Reset class R3) C1

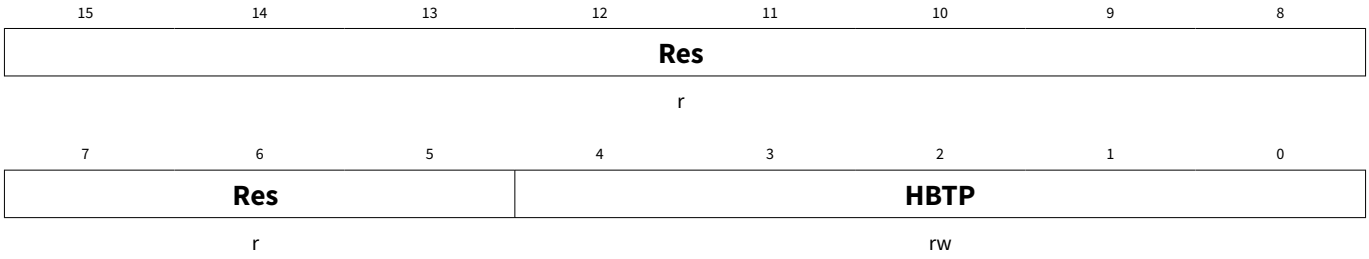
18.66 Functional watchdog 1 protected write heart beat timer period configuration register - *R2)

FWD1_PW_HBTP_CFG

Offset address: $03B_H$

Functional watchdog 1 protected write heart beat timer period configuration register - *R2)

Reset values see: Table 118



Field	Bits	Type	Description
HBTP	4:0	rw	**Functional watchdog 1 heartbeat timer period** 00_H (0 * 50 + 50) * time base … $1F_H$ (31 * 50 + 50) * time base

Table 118 Reset values of FWD1_PW_HBTP_CFG

Reset	Reset value	Note
	$000B_H$	Reset class R2)

18.67 Functional watchdog 1 reflected status heart beat timer period configuration register *R3_C1

FWD1_RS_HBTP_CFG

Functional watchdog 1 reflected status heart beat timer period configuration register *R3_C1

Offset address: $03C_H$

Reset values see: Table 119

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			HBTP				
r			r				

Field	Bits	Type	Description
HBTP	4:0	r	**Functional watchdog 1 heartbeat timer period** 00_H (0 * 50 + 50) * time base … $1F_H$ (31 * 50 + 50) * time base

Table 119 Reset values of FWD1_RS_HBTP_CFG

Reset	Reset value	Note
	$000B_H$	Reset class R3) C1

18.68 Window watchdog 1 protected write closed window configuration register - *R2)

WWD1_PW_CW_CFG

Offset address: $03D_H$

Window watchdog 1 protected write closed window configuration register - *R2)

Reset values see: Table 120

15	14	13	12	11	10	9	8
CW_DIS	**Res**						
rw	r						

7	6	5	4	3	2	1	0
Res			**CW**				
r			rw				

Field	Bits	Type	Description
CW	4:0	rw	**Closed window time** 00_H (0 * 50 + 50) * time base … $1F_H$ (31 * 50 + 50) * time base
CW_DIS	15	rw	**Disable the closed window (CW) of the window watchdog (WWD)** 0_B Closed window enabled 1_B Closed window disabled

Table 120 Reset values of WWD1_PW_CW_CFG

Reset	Reset value	Note
	0006_H	Reset class R2)

18.69 Window watchdog 1 reflected status closed window configuration register *R3_C1)

WWD1_RS_CW_CFG

Offset address: $03E_H$

Window watchdog 1 reflected status closed window configuration register *R3_C1)

Reset values see: Table 121

15	14	13	12	11	10	9	8
CW_DIS	**Res**						
r	r						

7	6	5	4	3	2	1	0
Res			**CW**				
r			r				

Field	Bits	Type	Description
CW	4:0	r	**Closed window time** 00_H (0 * 50 + 50) * time base … $1F_H$ (31 * 50 + 50) * time base
CW_DIS	15	r	**Disable the closed window (CW) of the window watchdog (WWD)** 0_B Closed window enabled 1_B Closed window disabled

Table 121 Reset values of WWD1_RS_CW_CFG

Reset	Reset value	Note
	0006_H	Reset class R3) C1

18.70 Window watchdog 1 protected write open window configuration register - *R2)

WWD1_PW_OW_CFG

Offset address: $03F_H$

Window watchdog 1 protected write open window configuration register - *R2)

Reset values see: Table 122

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			OW				
r			rw				

Field	Bits	Type	Description
OW	4:0	rw	**Open window time** 00_H (0 * 50 + 50) * time base … $1F_H$ (31 * 50 + 50) * time base

Table 122 Reset values of WWD1_PW_OW_CFG

Reset	Reset value	Note
	$000B_H$	Reset class R2)

18.71 Window watchdog 1 reflected status open window configuration register - *R3_C1)

WWD1_RS_OW_CFG

Offset address: 040_H

Window watchdog 1 reflected status open window configuration register - *R3_C1)

Reset values see: Table 123

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			OW				
r			r				

Field	Bits	Type	Description
OW	4:0	r	**Open window time** 00_H (0 * 50 + 50) * time base … $1F_H$ (31 * 50 + 50) * time base

Table 123 Reset values of WWD1_RS_OW_CFG

Reset	Reset value	Note
	$000B_H$	Reset class R3) C1

18.72 Window watchdog 1 trigger- *R2)

WWD1_TRIG Offset address: 041_H

Window watchdog 1 trigger- *R2) Reset values see: Table 124

15	14	13	12	11	10	9	8
TRIG_STAT	**Res**						
r	r						

7	6	5	4	3	2	1	0
Res							**TRIG**
r							rw

Field	Bits	Type	Description
TRIG	0	rw	**This bit triggers the window watchdog 1. For successful trigger, inverted value must be written.**
TRIG_STAT	15	r	**Last internal trigger value (TRIG bit) received via SPI.**

Table 124 Reset values of WWD1_TRIG

Reset	Reset value	Note
	0000_H	Reset class R2)

18.73 Functional watchdog 1 response register - *R2)

FWD1_RSP Offset address: 042_H

Functional watchdog 1 response register - *R2) Reset values see: Table 125

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
RSP							
rw							

Field	Bits	Type	Description
RSP	7:0	rw	**Response byte**

Table 125 Reset values of FWD1_RSP

Reset	Reset value	Note
	0000_H	Reset class R2)

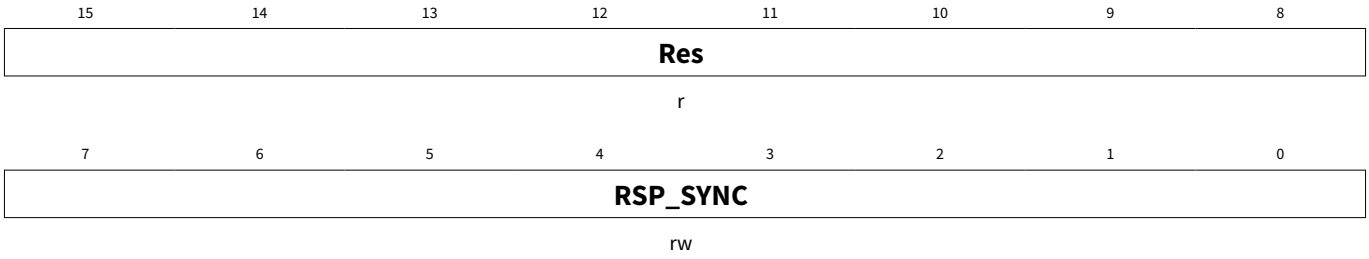
18.74 Functional watchdog 1 response register with synchronization of the heartbeat timer - *R2)

FWD1_RSP_SYNC

Functional watchdog 1 response register with synchronization of the heartbeat timer - *R2)

Offset address: 043_H

Reset values see: Table 126



Field	Bits	Type	Description
RSP_SYNC	7:0	rw	**Functional watchdog response byte and heartbeat timer synchronization**

Table 126 Reset values of FWD1_RSP_SYNC

Reset	Reset value	Note
	0000_H	Reset class R2)

18.75 Functional watchdog 1 status register - *R3_C1)

FWD1_STAT Offset address: 044_H

Functional watchdog 1 status register - *R3_C1) Reset values see: Table 127

15	14	13	12	11	10	9	8
Res					ECNT		
r					r		

7	6	5	4	3	2	1	0
ECNT	RSP_OK	RSPC		QUEST			
r	r	r		r			

Field	Bits	Type	Description
QUEST	3:0	r	**Functional watchdog question. Represents the value of the question, that is currently being asked.**
RSPC	5:4	r	**Functional watchdog response counter value. Represents the response which is currently expected (RESP3/2/1/0).**
RSP_OK	6	r	**Functional watchdog response status** 0_B Response message is wrong 1_B All received bytes in response message are correct
ECNT	10:7	r	**Functional watchdog error counter value**

Table 127 Reset values of FWD1_STAT

Reset	Reset value	Note
	0030_H	Reset class R3) C1

18.76 Window watchdog 1 error counter status register - *R3_C1)

WWD1_ECNT_STAT

Window watchdog 1 error counter status register - *R3_C1)

Offset address: 045_H

Reset values see: Table 128

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res				**ECNT**			
r				r			

Field	Bits	Type	Description
ECNT	3:0	r	**Error counter value**

Table 128 Reset values of WWD1_ECNT_STAT

Reset	Reset value	Note
	0000_H	Reset class R3) C1

18.77 Watchdog 2 protected write configuration 0 register - *R2)

WD2_PW_CFG0

Watchdog 2 protected write configuration 0 register - *R2)

Offset address: 046_H

Reset values see: Table 129

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
WWD_ETHR				WWD_EN	FWD_EN	WWD_TSEL	CYC
rw				rw	rw	rw	rw

Field	Bits	Type	Description
CYC	0	rw	**Watchdog 2 cycle time** 0_B 0.1 ms tick period 1_B 1 ms tick period
WWD_TSEL	1	rw	**Window watchdog (WWD2) trigger selection.** 0_B External WDI input used as a WWD trigger 1_B WWD is triggered by SPI
FWD_EN	2	rw	**Functional watchdog (FWD2) enable** 0_B Disabled 1_B Enabled
WWD_EN	3	rw	**Window watchdog (WWD2) enable** 0_B Disabled 1_B Enabled
WWD_ETHR	7:4	rw	**Window watchdog error threshold.**

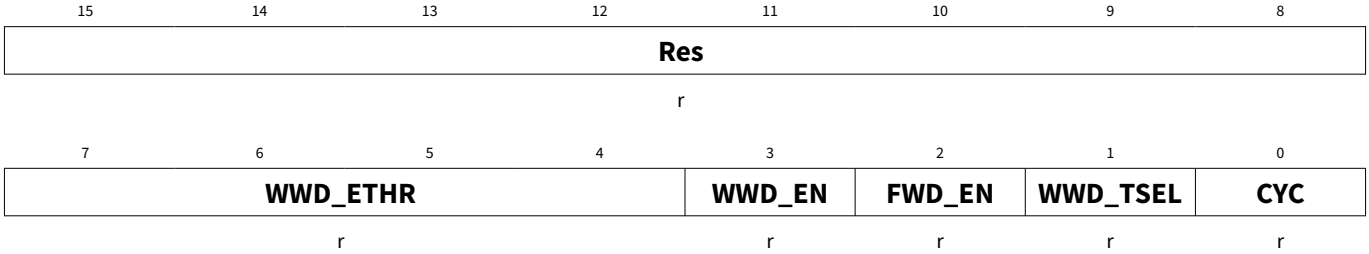
Table 129 Reset values of WD2_PW_CFG0

Reset	Reset value	Note
	$009B_H$	Reset class R2)

18.78 Watchdog 2 reflected status configuration 0 register- *R3_C2)

WD2_RS_CFG0 Offset address: 047_H

Watchdog 2 reflected status configuration 0 register- *R3_C2) Reset values see: Table 130



Field	Bits	Type	Description
CYC	0	r	**Watchdog 2 cycle time** 0_B 0.1 ms tick period 1_B 1 ms tick period
WWD_TSEL	1	r	**Window watchdog (WWD2) trigger selection.** 0_B External WDI input used as a WWD trigger 1_B WWD is triggered by SPI write to WWDSCMD register
FWD_EN	2	r	**Functional watchdog (FWD2) enable** 0_B Disabled 1_B Enabled
WWD_EN	3	r	**Window watchdog (WWD2) enable** 0_B Disabled 1_B Enabled
WWD_ETHR	7:4	r	**Window watchdog error threshold.**

Table 130 Reset values of WD2_RS_CFG0

Reset	Reset value	Note
	$009B_H$	Reset class R3) C2

18.79 Watchdog 2 protected write configuration 1 - *R2)

WD2_PW_CFG1 Offset address: 048_H

Watchdog 2 protected write configuration 1 - *R2) Reset values see: Table 131

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res		**CYC_DIV**	**SLP_EN**	**FWD_ETHR**			
r		rw	rw	rw			

Field	Bits	Type	Description
FWD_ETHR	3:0	rw	**Functional watchdog error threshold.**
SLP_EN	4	rw	**Watchdog 2 is active in sleep state** 0_B Disabled 1_B Enabled
CYC_DIV	5	rw	**Apply an additional divider of 10 to the cycle time** 0_B Disabled 1_B Enabled, additional divider

Table 131 Reset values of WD2_PW_CFG1

Reset	Reset value	Note
	0009_H	Reset class R2)

18.80 Watchdog 2 reflected status configuration 1 register - *R3_C2)

WD2_RS_CFG1

Watchdog 2 reflected status configuration 1 register - *R3_C2)

Offset address: 049_H

Reset values see: Table 132

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res		CYC_DIV	SLP_EN	FWD_ETHR			
r		r	r	r			

Field	Bits	Type	Description
FWD_ETHR	3:0	r	**Functional watchdog error threshold.**
SLP_EN	4	r	**Watchdog 2 is active in sleep state** 0_B Disabled 1_B Enabled
CYC_DIV	5	r	**Additional divider of 10 to the cycle time is applied** 0_B Disabled 1_B Enabled

Table 132 Reset values of WD2_RS_CFG1

Reset	Reset value	Note
	0009_H	Reset class R3) C2

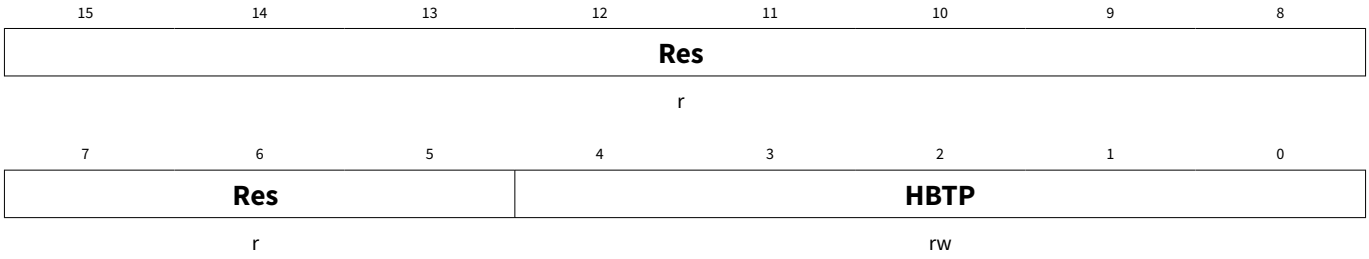
18.81 Functional watchdog 2 protected write heart beat timer period configuration register - *R2)

FWD2_PW_HBTP_CFG

Offset address: $04A_H$

Functional watchdog 2 protected write heart beat timer period configuration register - *R2)

Reset values see: Table 133



Field	Bits	Type	Description
HBTP	4:0	rw	**Functional watchdog 2 heartbeat timer period** 00_H (0 * 50 + 50) wd time base … $1F_H$ (31 * 50 + 50) wd time base

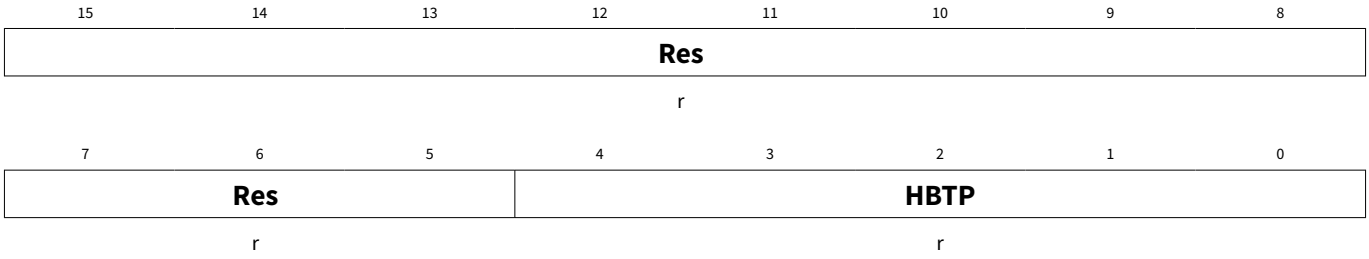
Table 133 Reset values of FWD2_PW_HBTP_CFG

Reset	Reset value	Note
	$000B_H$	Reset class R2)

18.82 Functional watchdog 2 reflected status heart beat timer period configuration register *R3_C2)

FWD2_RS_HBTP_CFG Offset address: $04B_H$

Functional watchdog 2 reflected status heart beat timer period configuration register *R3_C2) Reset values see: Table 134



Field	Bits	Type	Description
HBTP	4:0	r	**Functional watchdog 2 heartbeat timer period** 00_H (0 * 50 + 50) wd time base … $1F_H$ (31 * 50 + 50) wd time base

Table 134 Reset values of FWD2_RS_HBTP_CFG

Reset	Reset value	Note
	$000B_H$	Reset class R3) C2

18.83 Window watchdog 2 protected write closed window configuration register - *R2)

WWD2_PW_CW_CFG

Offset address: $04C_H$

Window watchdog 2 protected write closed window configuration register - *R2)

Reset values see: Table 135

15	14	13	12	11	10	9	8
CW_DIS	**Res**						
rw	r						

7	6	5	4	3	2	1	0
Res			**CW**				
r			rw				

Field	Bits	Type	Description
CW	4:0	rw	**Closed window time** 00_H (0 * 50 + 50) wd time base … $1F_H$ (31 * 50 + 50) wd time base
CW_DIS	15	rw	**Disable the closed window (CW) of the window watchdog (WWD)** 0_B Closed window enabled 1_B Closed window disabled

Table 135 Reset values of WWD2_PW_CW_CFG

Reset	Reset value	Note
	0006_H	Reset class R2)

18.84 Window watchdog 2 reflected status closed window configuration register *R3_C2)

WWD2_RS_CW_CFG

Window watchdog 2 reflected status closed window configuration register *R3_C2)

Offset address: $04D_H$

Reset values see: Table 136

15	14	13	12	11	10	9	8
CW_DIS	**Res**						
r	r						

7	6	5	4	3	2	1	0
Res				**CW**			
r				r			

Field	Bits	Type	Description
CW	4:0	r	**Closed window time** 00_H (0 * 50 + 50) wd time base … $1F_H$ (31 * 50 + 50) wd time base
CW_DIS	15	r	**Disable the closed window (CW) of the window watchdog (WWD)** 0_B Closed window enabled 1_B Closed window disabled

Table 136 Reset values of WWD2_RS_CW_CFG

Reset	Reset value	Note
	0006_H	Reset class R3) C2

18.85 Window watchdog 2 protected write open window configuration register - *R2)

WWD2_PW_OW_CFG

Offset address: $04E_H$

Window watchdog 2 protected write open window configuration register - *R2)

Reset values see: Table 137

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			OW				
r			rw				

Field	Bits	Type	Description
OW	4:0	rw	**Open window time** 00_H (0 * 50 + 50) wd time base … $1F_H$ (31 * 50 + 50) wd time base

Table 137 Reset values of WWD2_PW_OW_CFG

Reset	Reset value	Note
	$000B_H$	Reset class R2)

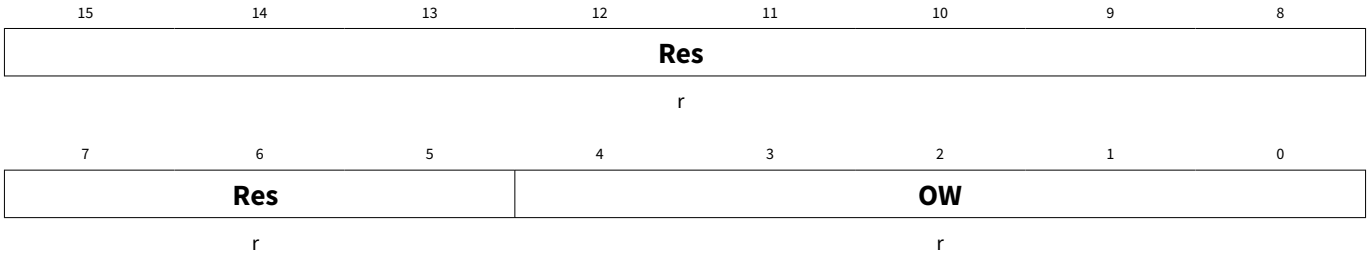
18.86 Window watchdog 2 reflected status open window configuration register *R3_C2)

WWD2_RS_OW_CFG

Offset address: $04F_H$

Window watchdog 2 reflected status open window configuration register *R3_C2)

Reset values see: Table 138



Field	Bits	Type	Description
OW	4:0	r	**Open window time** 00_H (0 * 50 + 50) wd time base … $1F_H$ (31 * 50 + 50) wd time base

Table 138 Reset values of WWD2_RS_OW_CFG

Reset	Reset value	Note
	$000B_H$	Reset class R3) C2

18.87 Window watchdog 2 service - *R2)

WWD2_TRIG Offset address: 050_H

Window watchdog 2 service - *R2) Reset values see: Table 139

15	14	13	12	11	10	9	8
TRIG_STAT	**Res**						
r	r						

7	6	5	4	3	2	1	0
Res							**TRIG**
r							rw

Field	Bits	Type	Description
TRIG	0	rw	**This bit triggers the window watchdog 2. For successful trigger, inverted value must be written.**
TRIG_STAT	15	r	**Last internal service value (TRIG bit) received via SPI.**

Table 139 Reset values of WWD2_TRIG

Reset	Reset value	Note
	0000_H	Reset class R2)

18.88 Functional watchdog 2 response register - *R2)

FWD2_RSP Offset address: 051_H

Functional watchdog 2 response register - *R2) Reset values see: Table 140

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
RSP							
rw							

Field	Bits	Type	Description
RSP	7:0	rw	**Response byte**

Table 140 Reset values of FWD2_RSP

Reset	Reset value	Note
	0000_H	Reset class R2)

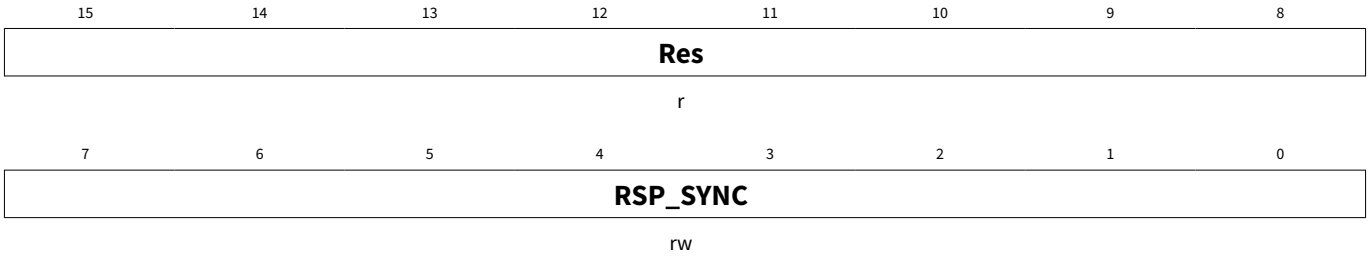
18.89 Functional watchdog 2 response register with synchronization - *R2)

FWD2_RSP_SYNC

Functional watchdog 2 response register with synchronization - *R2)

Offset address: 052_H

Reset values see: Table 141



Field	Bits	Type	Description
RSP_SYNC	7:0	rw	**Functional watchdog response byte and heartbeat timer synchronization**

Table 141 Reset values of FWD2_RSP_SYNC

Reset	Reset value	Note
	0000_H	Reset class R2)

18.90 Functional watchdog 2 status register - *R3_C2)

FWD2_STAT Offset address: 053_H

Functional watchdog 2 status register - *R3_C2) Reset values see: Table 142

15	14	13	12	11	10	9	8
Res					ECNT		
r					r		

7	6	5	4	3	2	1	0
ECNT	RSP_OK	RSPC		QUEST			
r	r	r		r			

Field	Bits	Type	Description
QUEST	3:0	r	**Functional watchdog question**
RSPC	5:4	r	**Functional watchdog response counter value**
RSP_OK	6	r	**Functional watchdog response status** 0_B Response message is wrong 1_B All received bytes in response message are correct
ECNT	10:7	r	**Functional watchdog error counter value**

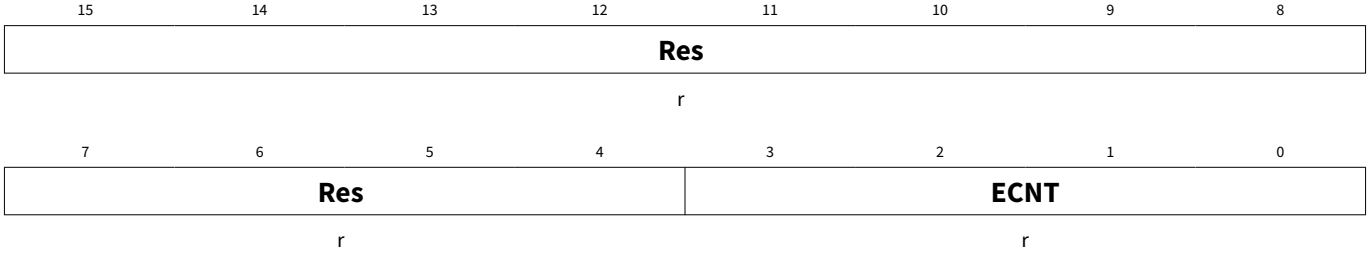
Table 142 Reset values of FWD2_STAT

Reset	Reset value	Note
	0030_H	Reset class R3) C2

18.91 Window watchdog 2 status register - *R3_C2)

WWD2_ECNT_STAT Offset address: 054_H

Window watchdog 2 status register - *R3_C2) Reset values see: Table 143



Field	Bits	Type	Description
ECNT	3:0	r	**Error counter value**

Table 143 Reset values of WWD2_ECNT_STAT

Reset	Reset value	Note
	0000_H	Reset class R3) C2

18.92 Safety switch diagnostics, *R1)

SSW_DIAG

Safety switch diagnostics, *R1)

Offset address: 055_H

Reset values see: Table 144

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res			**EBIST4**	**EBIST3**	**EBIST2**	**EBIST1**	**EBIST0**
r			r	r	r	r	r

Field	Bits	Type	Description
EBIST0	0	r	**Indicates if SSW is intact** 0_B No fault 1_B SSW check not passed
EBIST1	1	r	**Indicates if high side switch at PREREG is intact** 0_B No fault 1_B HS switch of PREREG defect
EBIST2	2	r	**Indicates if SSW gate can be discharged** 0_B No fault 1_B SSW gate could not be discharged
EBIST3	3	r	**Indicates if low side switch of PREREG is intact** 0_B No fault 1_B LS switch of PREREG defect
EBIST4	4	r	**Sanity check on SSW charge pump chain** 0_B No fault 1_B Sanity check unsuccessful

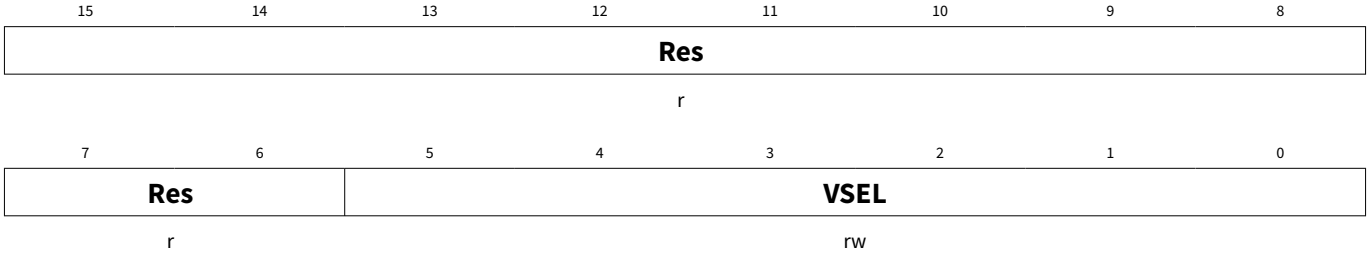
Table 144 Reset values of SSW_DIAG

Reset	Reset value	Note
	0000_H	Reset class R1)

18.93 BUCK CORE protected write voltage selection register *R1)

BUCK_CORE_PW_VSEL Offset address: 056_H

BUCK CORE protected write voltage selection register *R1) Reset values see: Table 145



Field	Bits	Type	Description
VSEL	5:0	rw	**Voltage selection (0.7 V to 1.1 V; 12.5 mV steps)** 00_H BUCKCORE output voltage: 0.7 V + 0*12.5 mV … 20_H BUCKCORE output voltage: 0.7 V + 32*12.5 mV **others,** reserved

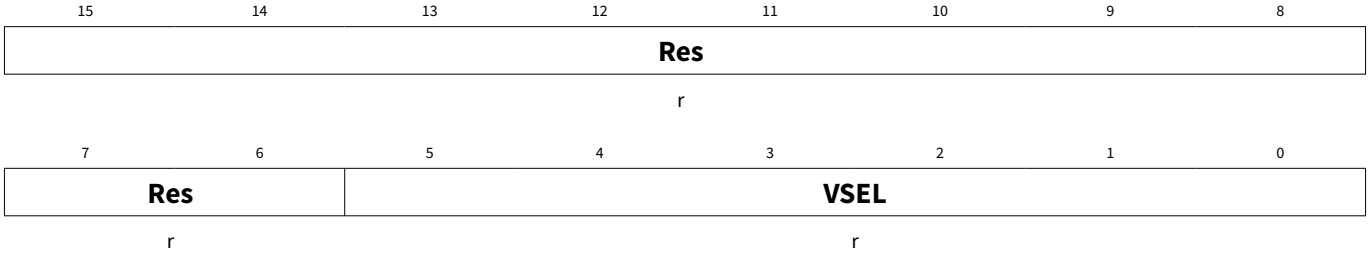
Table 145 Reset values of BUCK_CORE_PW_VSEL

Reset	Reset value	Note
	0000_H	

18.94 BUCK CORE reflected status voltage selection register *R2)

BUCK_CORE_RS_VSEL Offset address: 057_H

BUCK CORE reflected status voltage selection register *R2) Reset values see: Table 146



Field	Bits	Type	Description
VSEL	5:0	r	**Voltage selection status register (0.7 V to 1.1 V; 12.5 mV steps)** 00_H BUCKCORE output voltage: 0.7 V + 0*12.5 mV … 20_H BUCKCORE output voltage: 0.7 V + 32*12.5 mV **others,** reserved

Table 146 Reset values of BUCK_CORE_RS_VSEL

Reset	Reset value	Note
	$001A_H$	Reset class R2)

18.95 Buck core voltage selection stat, *R2)

VCORESTAT Offset address: 058_H

Buck core voltage selection stat, *R2) Reset values see: Table 147

15	14	13	12	11	10	9	8
Res							
r							

7	6	5	4	3	2	1	0
Res		**VOUT**					
r		r					

Field	Bits	Type	Description
VOUT	5:0	r	**Current voltage out for buckcore, *R2)** 00_H BUCKCORE output voltage set to 0.7 V + 0*12.5 mV … 20_H BUCKCORE output voltage set to 0.7 V + 32*12.5 mV 21_H BUCKCORE output voltage set to 1.15 V; Not allowed to be used for static voltage scaling! **others,** reserved

Table 147 Reset values of VCORESTAT

Reset	Reset value	Note
	0000_H	Reset class R2)

18.96 Buck core voltage selection monitors stat, *R2)

VCOREMONSTAT Offset address: 059_H

Buck core voltage selection monitors stat, *R2) Reset values see: Table 148

15	14	13	12	11	10	9	8
Res		**OVTH**					
r		r					

7	6	5	4	3	2	1	0
Res		**UVTH**					
r		r					

Field	Bits	Type	Description
UVTH	5:0	r	**Under voltage thresholds for buckcore voltage selection, *R2)** 00_H BUCKCORE undervoltage threshold for VOUT = 0.7 V + 0*12.5 mV … 20_H BUCKCORE undervoltage threshold for VOUT = 0.7 V + 32*12.5 mV 21_H BUCKCORE undervoltage threshold for VOUT = 1.15 V **others,** reserved
OVTH	13:8	r	**Over voltage thresholds for buckcore voltage selection, *R2)** 00_H BUCKCORE overvoltage threshold for VOUT = 0.7 V + 0*12.5 mV … 20_H BUCKCORE overvoltage threshold for VOUT = 0.7 V + 32*12.5 mV 21_H BUCKCORE overvoltage threshold for VOUT = 1.15 V **others,** reserved

Table 148 Reset values of VCOREMONSTAT

Reset	Reset value	Note
	0000_H	Reset class R2)

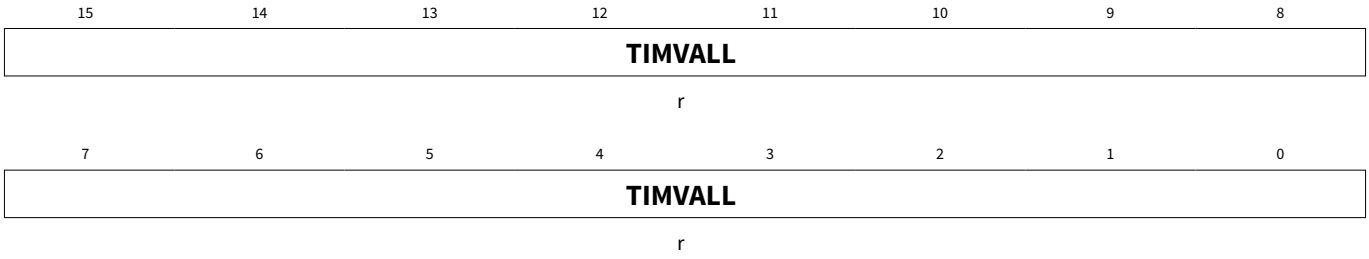
18.97 Wake Up Timer value after exiting from STANDBY or SLEEP (lower 16 bits)

WUT_STAT0

Offset address: $05A_H$

Wake Up Timer value after exiting from STANDBY or SLEEP [lower 16 bits]

value: 0000_H



Field	Bits	Type	Description
TIMVALL	15:0	r	**Lower 16 bit of wake-up timer value: LSB bit 0; MSB bit15**

18.98 Wake Up Timer value after exiting from STANDBY or SLEEP (upper 8 bits)

WUT_STAT1

Offset address: $05B_H$

Wake Up Timer value after exiting from STANDBY or SLEEP [upper 8 bits)

value: 0000_H

15	14	13	12	11	10	9	8
CYC	**PRESC**	**Res**					
r	r	r					

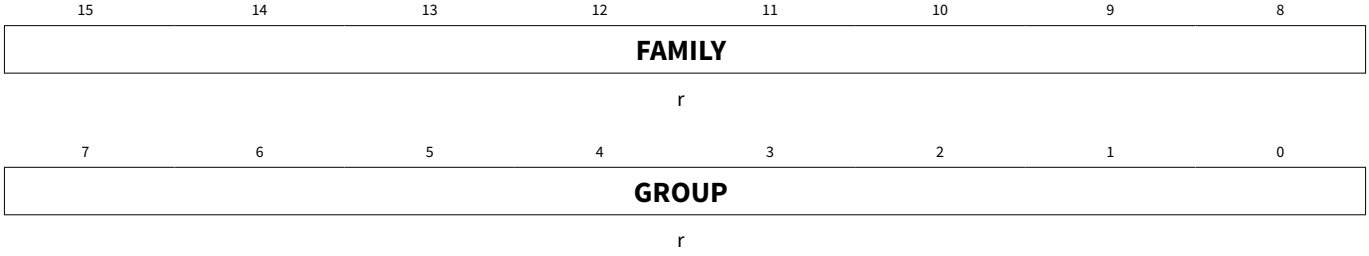
7	6	5	4	3	2	1	0
TIMVALH							
r							

Field	Bits	Type	Description
TIMVALH	7:0	r	**Higher 8 bits of wake-up timer value: LSB bit0; MSB bit 7**
PRESC	14	r	0_B Disabled 1_B Enabled
CYC	15	r	0_B 10 µs 1_B 10 ms

18.99 Chip product identifier

CHPID Offset address: $1F0_H$

Chip product identifier value: 0201_H



Field	Bits	Type	Description
GROUP	7:0	r	**Chip product group** 01_H GP_PMIC
FAMILY	15:8	r	**Chip family** 02_H TLF4D985

18.100 Chip product version and revision

CHREV Offset address: $1F1_H$

Chip product version and revision value: 0003_H

15	14	13	12	11	10	9	8
VERSION							
r							

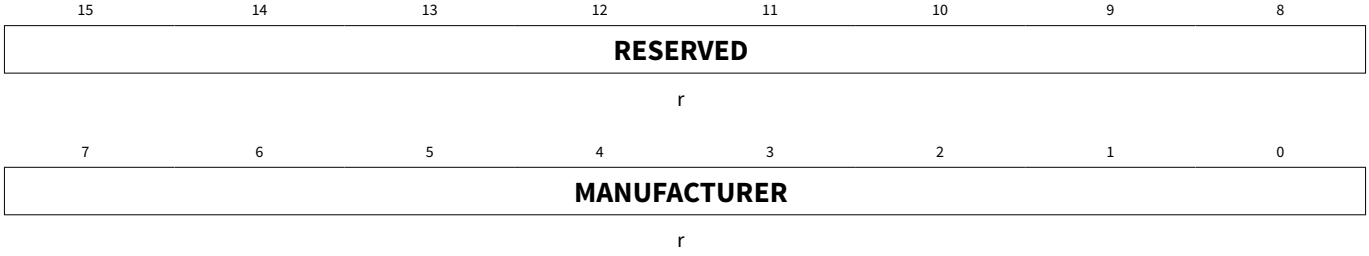
7	6	5	4	3	2	1	0
REVISION							
r							

Field	Bits	Type	Description
REVISION	7:0	r	**Chip revision** 01_H A11 02_H A21 03_H A31 (TLF4D985QxV0xR1)
VERSION	15:8	r	**Chip product version** 01_H TLF4D985QxV01 02_H TLF4D985QxV02 03_H TLF4D985QxV03

18.101 Manufacturer ID

MANID Offset address: $1F2_H$

Manufacturer ID value: $00C1_H$



Field	Bits	Type	Description
MANUFACTURER	7:0	r	**MANUFACTURER** $C1_H$ Infineon technologies AG
RESERVED	15:8	r	**RESERVED**

19 Application information

19.1 Application diagram

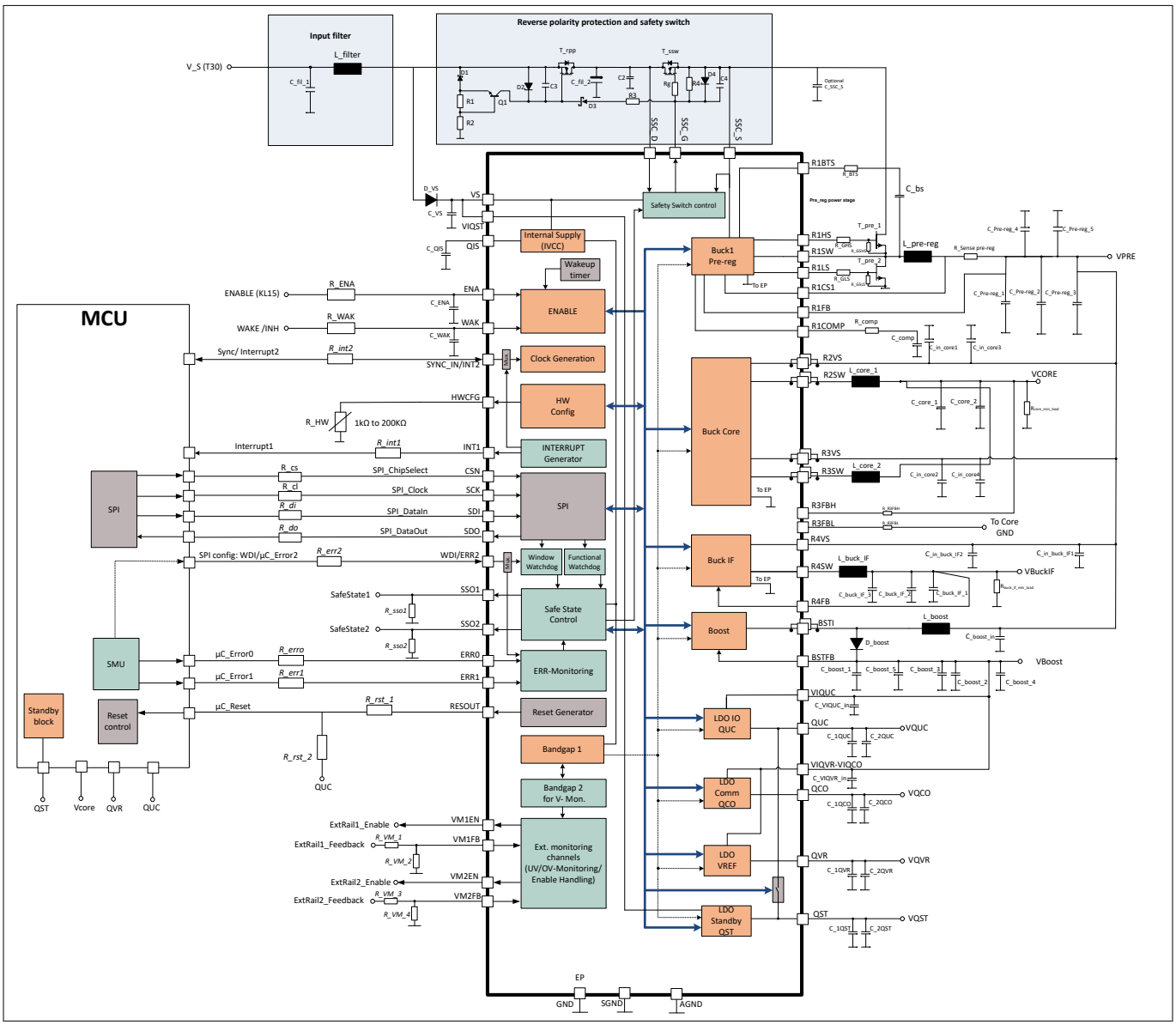


Figure 96 Application diagram

19.2 BOM recommendation

Table 149 BOM recommendation

Block	Symbol	Value	Description	Note
Input Filter	C_fil_1	10 µF	Surface mount ceramic capacitor	Max voltage depending on application (50 V for 12 V application and 100 V for 24 V application)
	C_fil_2	220 µF	Electrolytic capacitor	Max voltage depending on application (50 V for 12 V application and 100 V for 24 V application)
	L_filter	4.7 µH	Shielded filter Power Inductor	Inductor selection depending on EMC requirement
QIS & Input voltage	C_QIS	1 µF	Surface mount ceramic capacitor	–
	C_VS	4.7 µF	Surface mount ceramic capacitors	–
	D_VS	d_schottky	reverse polarity protection diode for low current path	–
Reverse battery protection (RPP) and safety switch (SSC)	C2	10 µF	Surface mount ceramic capacitor	Max voltage depending on application (50 V for 12 V application and 100 V for 24 V application)
	C3	1 nF	Surface mount ceramic capacitor	–
	C4	1 nF	Surface mount ceramic capacitor	–
	T_rpp	RPP + SSC MOSFET	N-Channel MOSFETs (logic level)	IPG20N06S2L-35A (dual MOSFET) or IAUZ40N06S5L050 (single) or similar
	T_ssw			
	D1	VBD = 60 V	Schottky diode to prevent current flowing via R1 and R2 in normal supply condition	–

(table continues...)

Table 149 (continued) BOM recommendation

Block	Symbol	Value	Description	Note
	D2	VZ = 10 V	Zener diode to protect gate of RPP MOSFET	–
	D3	VBD = 60 V	Schottky diode to prevent current bypassing RPP and SSW via R4 and R5 in normal supply condition	RB558VYM150FH
	D4	VZ = 6.2 V	Zener diode to protect the PMIC VGS driver	–
	Q1	npn	Low leakage npn transistor, to discharge the RPP MOSFET when the battery voltage is below ground	Recommended low leakage at VCB = 40 V at hot
	R1	47 kΩ	Standard thick film chip resistor	–
	R2	47 kΩ	Standard thick film chip resistor	–
	R3	300 kΩ	Standard thick film chip resistor	–
	R4	300 kΩ	Standard thick film chip resistor	–
	Rg	10 Ω	Gate resistor for the control of the external safety switch	–
	C_SSC_S	1 µF (Max)	Surface mount ceramic capacitors	optional: To improve EMC performance. However dimension the capacitance to meet safety goals as it might have an effect on system's response to fault conditions.
PREREG	C_Pre_reg_1 C_Pre_reg_2	3 × 22 µF	Surface mount ceramic capacitors	Nominal values of capacitances are recommended taking into account

(table continues...)

Table 149 (continued) BOM recommendation

Block	Symbol	Value	Description	Note
	C_Pre_reg_3			all derating factors (voltage, temperature and aging)
	C_Pre_reg_4	1 µF	Surface mount ceramic capacitor	–
	C_Pre_reg_5	100 nF	Surface mount ceramic capacitor	–
	L_pre_reg	6.8 µH	Shielded power inductor	Select inductor according to the over current limitation
	T_pre_1	External MOSFETs	N-Channel MOSFETs (logic level)	IPG20N06S4L-26A (dual MOSFET) or IAUZ40N06S5L050 (single) or similar
	T_pre_2			IPG20N06S4L-26A (dual MOSFET) or IAUZ40N06S5L050 (single) or similar
	R_COMP	12 kΩ	Standard thick film chip resistor	For 10 A current capability
		25 kΩ	Standard thick film chip resistor	For 5 A current capability
	C_COMP	1.5 nF	Surface mount ceramic capacitor	For 5 A current capability
		2.7 nF	Surface mount ceramic capacitor	For 10 A current capability
	R_Sense_pre-reg	10 mΩ	Standard thick film chip resistor, tol. ±1%	For 10 A current capability
		20 mΩ	Standard thick film chip resistor, tol. ±1%	For 5 A current capability
	C_bs	100 nF	Surface mount ceramic capacitor	–
	R_BTS	–	Boot strap line resistance for limiting inrush currents	If EMC does not require it, set it to 0 Ω

(table continues...)

Table 149 (continued) BOM recommendation

Block	Symbol	Value	Description	Note
	R_GHS	–	Gate resistor for limiting gate currents	If EMC does not require it, set it to 0 Ω
	R_GSHS	–	–	optional: Only if use case assumption requires it for safety reasons
	R_GSLS	–	–	optional Only if use case assumption requires it for safety reasons
	R_GLS	–	Gate resistor for limiting gate currents	If EMC does not require it, set it to 0 Ω
BOOST	C_boost_in	100 nF	Surface mount ceramic capacitor	–
	C_boost_1	100 nF	Surface mount ceramic capacitor	–
	C_boost_2	1 µF	Surface mount ceramic capacitor	–
	C_boost_3	10 µF	Surface mount ceramic capacitor	–
	C_boost_4	100 nF	Surface mount ceramic capacitor	–
	C_boost_5	47 nF	Surface mount ceramic capacitor	–
	D_boost	d_schottky	Schottky Rectifier	MSS2P3 or similar
	L_boost	3.3 µH	Shielded Power Inductor	Select inductance according to the over current limitation
BUCK CORE	C_in_core1	2 × 4.7 µF	Surface mount ceramic capacitors	–
	C_in_core2			
	C_in_core3	2 × 100 nF	Surface mount ceramic capacitors	–
	C_in_core4			
	C_core_1	2 × 47 µF	Surface mount ceramic capacitors	consider to use additional capacitance in case it is necessary.
	C_core_2			

(table continues...)

Table 149 (continued) BOM recommendation

Block	Symbol	Value	Description	Note
	L_core_1	1 µH	Shielded power inductor	Select inductor according to the over current limitation
	L_core_2	1 µH	Shielded power inductor	Select inductor according to the over current limitation
	R_core_min_load	–	–	Pick accordingly to fulfill Minimum output current - BUCK CORE
	R_R3FBH	10 - 100 Ω	–	optional: Only required if use case assumption requires it for safety reasons
	R_R3FBL	10 - 100 Ω	–	optional: Only required if use case assumption requires it for safety reasons
BUCK IF	C_in_buck_IF1	1 µF	Surface mount ceramic capacitors	–
	C_in_buck_IF2	100 nF	Surface mount ceramic capacitors	–
	C_buck_IF_1	47 µF	Surface mount ceramic capacitors	–
	C_buck_IF_2	1 µF	Surface mount ceramic capacitor	–
	C_buck_IF_3	100 nF	Surface mount ceramic capacitor	–
	L_buck_IF	2.2 µH	Shielded power inductor	Select inductor according to the over current limitation
	R_buck_if_min_load	–	–	Pick accordingly to fulfill Minimum output current - BUCK IF
LDO_Capacitors	C_1QCO	4.7 µF	Surface mount ceramic capacitor	–

(table continues...)

Table 149 (continued) BOM recommendation

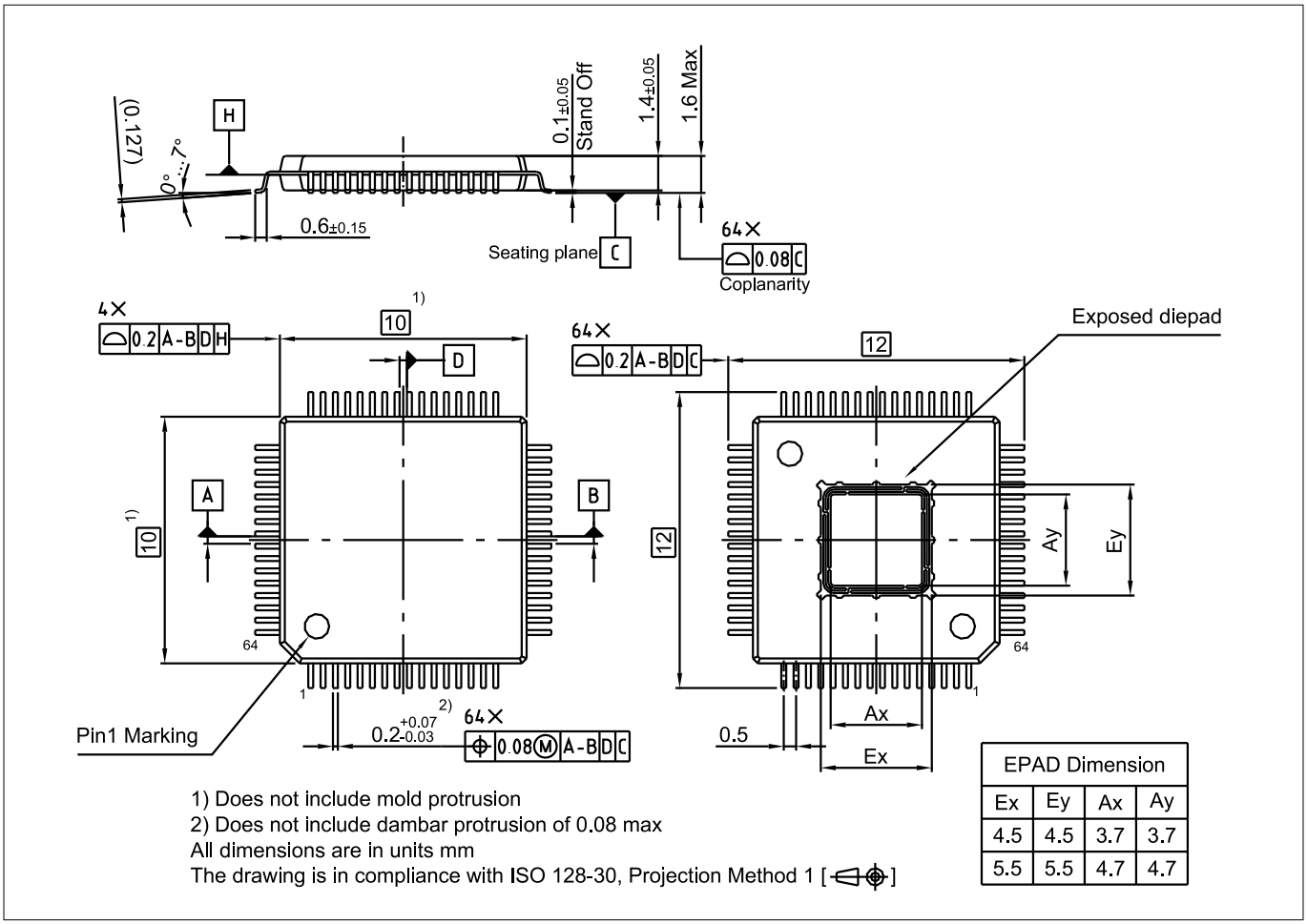
Block	Symbol	Value	Description	Note
	C_2QCO	–	Surface mount ceramic capacitor	Redundant setup might be required for safety context. Dimension according to EC table of QCO.
	C_1QST	4.7 µF	Surface mount ceramic capacitor	–
	C_2QST	–	Surface mount ceramic capacitor	Redundant setup might be required for safety context. Dimension according to EC table of QST.
	C_1QUC	4.7 µF	Surface mount ceramic capacitor	–
	C_2QUC	–	Surface mount ceramic capacitor	Redundant setup might be required for safety context. Dimension according to EC table of QUC.
	C_1QVR	4.7 µF	Surface mount ceramic capacitor	–
	C_2QVR	–	Surface mount ceramic capacitor	Redundant setup might be required for safety context. Dimension according to EC table of QVR.
	C_IQUC_in	100 nF	Surface mount ceramic capacitor	optional
	C_IQVR_in	100 nF	Surface mount ceramic capacitor	optional
ENA/WAK	C_ENA	10 nF	Surface mount ceramic capacitor	optional
	C_WAK	10 nF	Surface mount ceramic capacitor	optional
	R_ENA	10 kΩ	Standard thick film chip resistor	optional
	R_WAK	10 kΩ	Standard thick film chip resistor	optional

Table 150 BOM deviation for output capacitances of switch mode power supplies

SMPS	Effective capacitance	Deviation
PREREG	C_{PR}*[typ]*	-40%
BUCKCORE	$C_{buck\_core\_1/2}$*[typ]*	-30%
BUCKIF	C_{BUCK_IF}*[typ]*	-40%
BOOST	C_{bst}*[typ]*	-40%

***Note**: When deviating to the values, as specified in the table above, for the output capacitances of the switch mode regulators, the dynamic performance as specified in the datasheet can be impacted and it would require a dedicated assessment of the behavior in the application's context.*

20 Package information



EPAD Dimension			
Ex	Ey	Ax	Ay
4.5	4.5	3.7	3.7
5.5	5.5	4.7	4.7

Figure 97 PG-LQFP-64[1)]

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations, the device is available as a Green Product. Green Products are RoHS compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Information on packages

For more information on packages, such as recommendations on assembly, refer to www.infineon.com/packages.

[1] Exposed pad dimensions [mm] for this product: E_x: 5.5, E_y: 5.5, A_x: 4.7, A_y: 4.7.

21 Revision history

Revision	Date	Changes
1.00	2026-01-09	Datasheet created

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