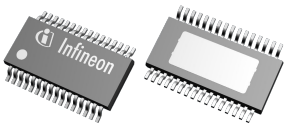
MOTIX™ TLE994x/TLE995x
Datasheet, Z8F80225297



RoHS

AEC Qualified

ISO 26262 compliant

Features

- 32-bit Arm® Cortex®-M23 core at up to 40 MHz, 27 interrupts
- Single power supply from 5.5 V to 29 V
- On-chip clock generation
- CRC engine for data integrity
- 72 KB flash with EEPROM emulation, 6 KB RAM
- LIN protocol support (LINUART) and LIN transceiver with safe transmit off
- High voltage monitoring pin (MON)
- Fast synchronous communication interface (SSC)
- Two/three-phase bridge driver (BDRV) with charge pump, PWM generation (CCU7) and safe switch off path
- Low-side shunt current sense amplifier and comparator (CSA)
- Fast 12-bit ADC for measuring up to 16 inputs with high and low voltage range
- 10x 16-bit timer (GPT12 and CCU7), 1x 24-bit timer (SYSTICK)
- 5x GPIOs (incl. RESET, SWD) and 3x GPIs (analog and digital)
- Safety: ISO26262 Safety Element out of Context for safety requirements up to ASIL-B
- Security: Arm® TrustZone enabling software isolation
- Temperature range T_J: -40°C up to 175°C
- Compact application footprint with TSDSO-32 package

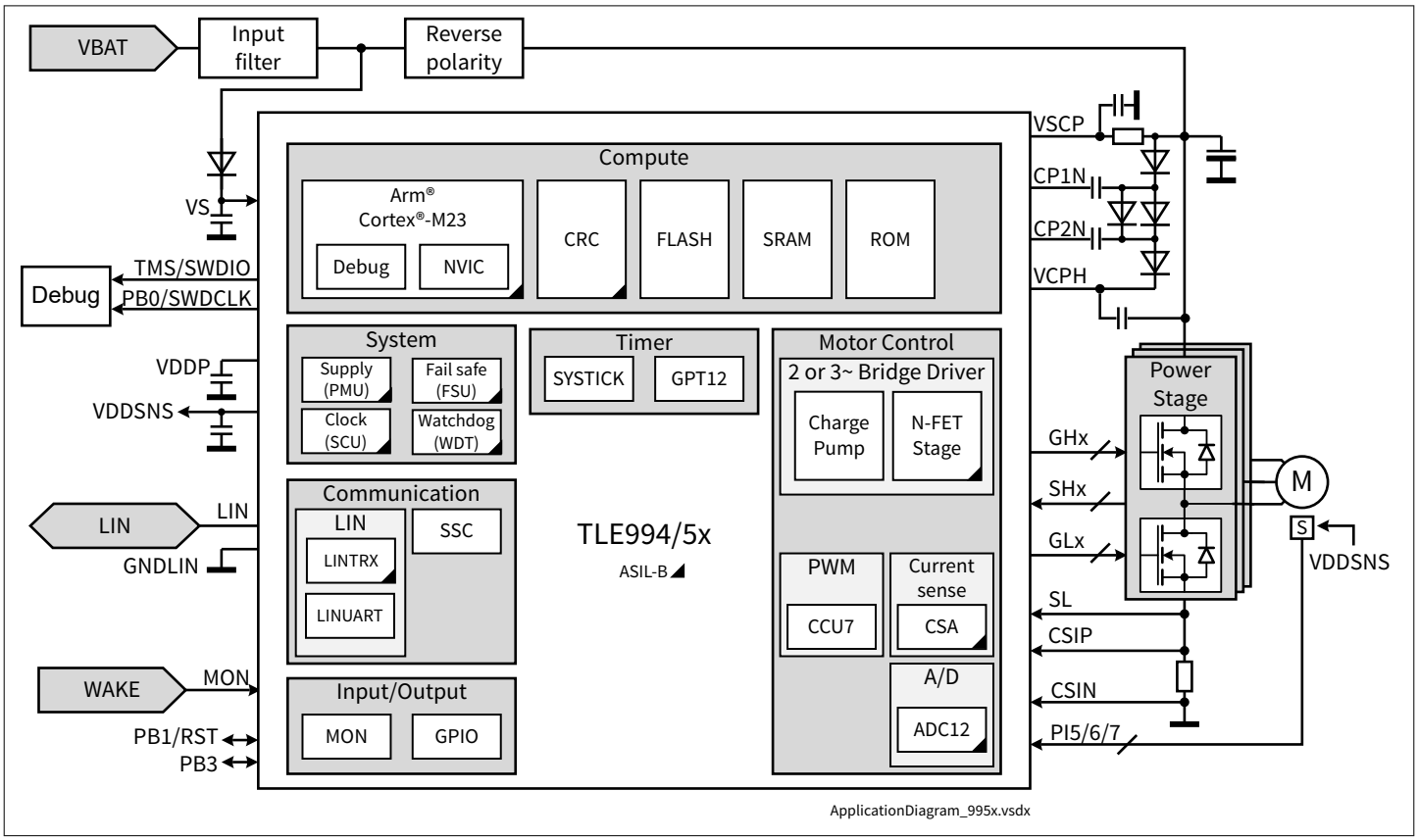
Potential applications

- Automotive motor control for auxiliary drives like pumps and fans in thermal management systems

Product validation

Product validation according to AEC-Q100, Grade 0 and Grade 1. Qualified for automotive applications.

Description



Product type	Package	Temperature grade	Flash/RAM [KB]	Frequency [MHz]	BDRV
TLE9944EQA40	TSDSO-32	Grade-1	72/6	40	2-phase
TLE9944EQW40	TSDSO-32	Grade-0	72/6	40	2-phase
TLE9954EQA40	TSDSO-32	Grade-1	72/6	40	3-phase
TLE9954EQW40	TSDSO-32	Grade-0	72/6	40	3-phase

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1 Block diagram

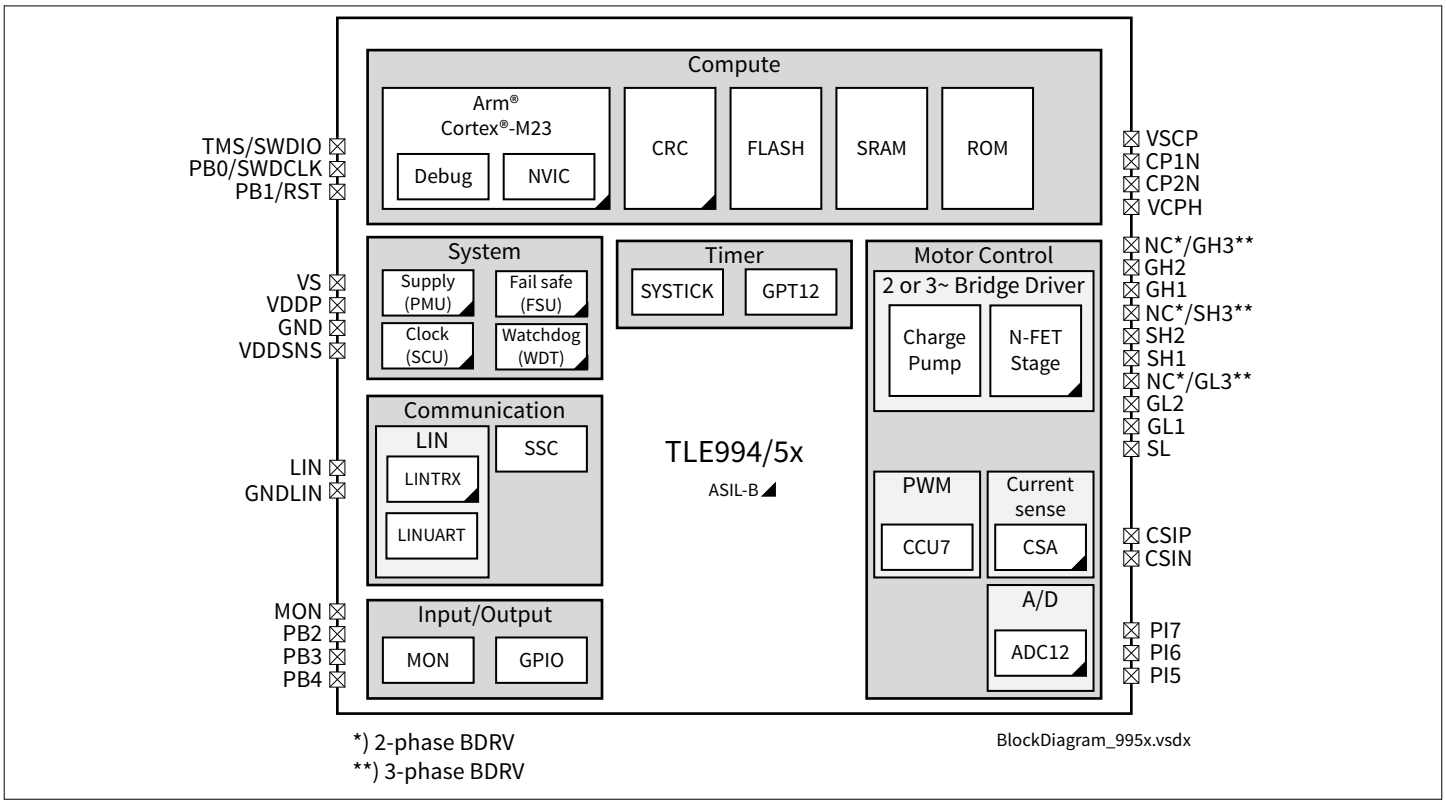

Figure 1 Block diagram

2 Pin configuration

2.1 Pin assignment

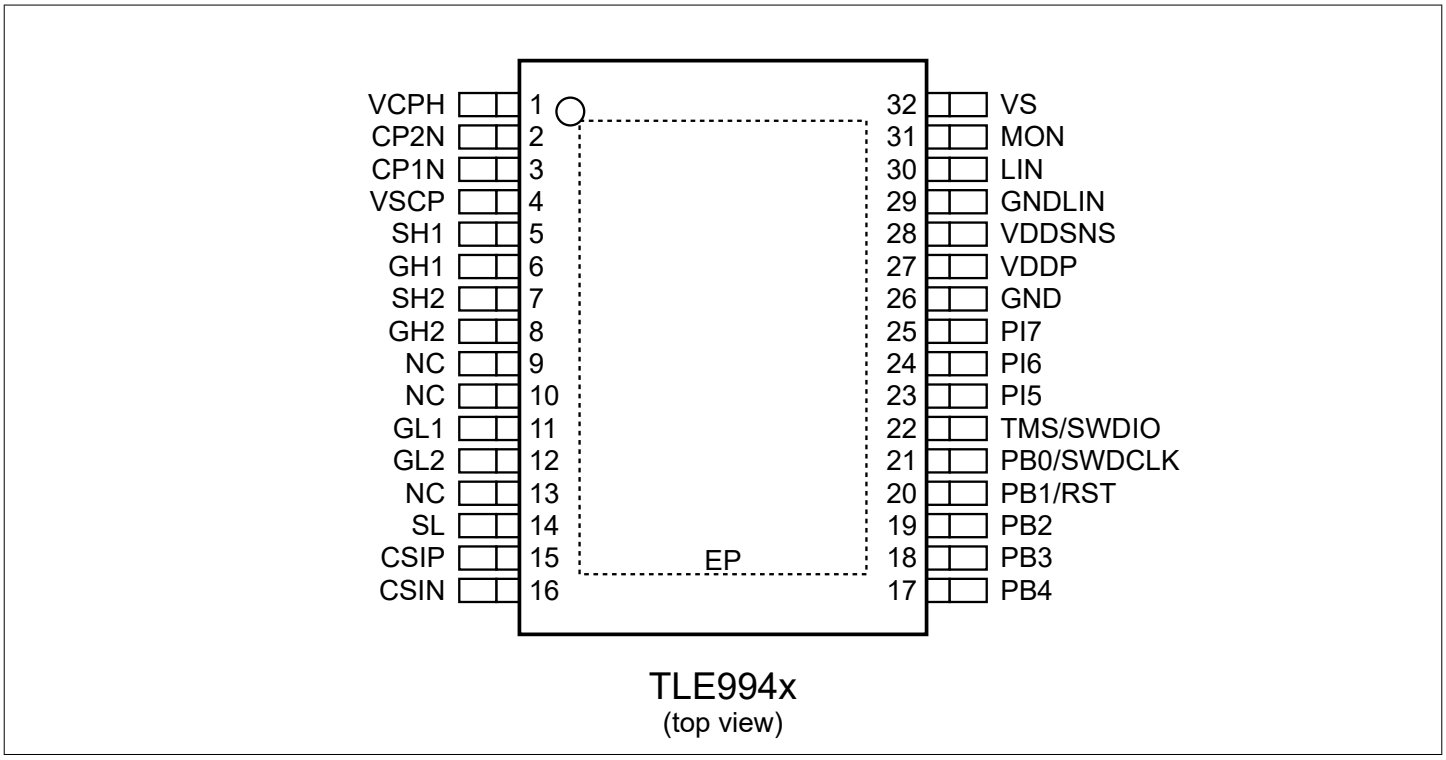

Figure 2 TLE994x pinout

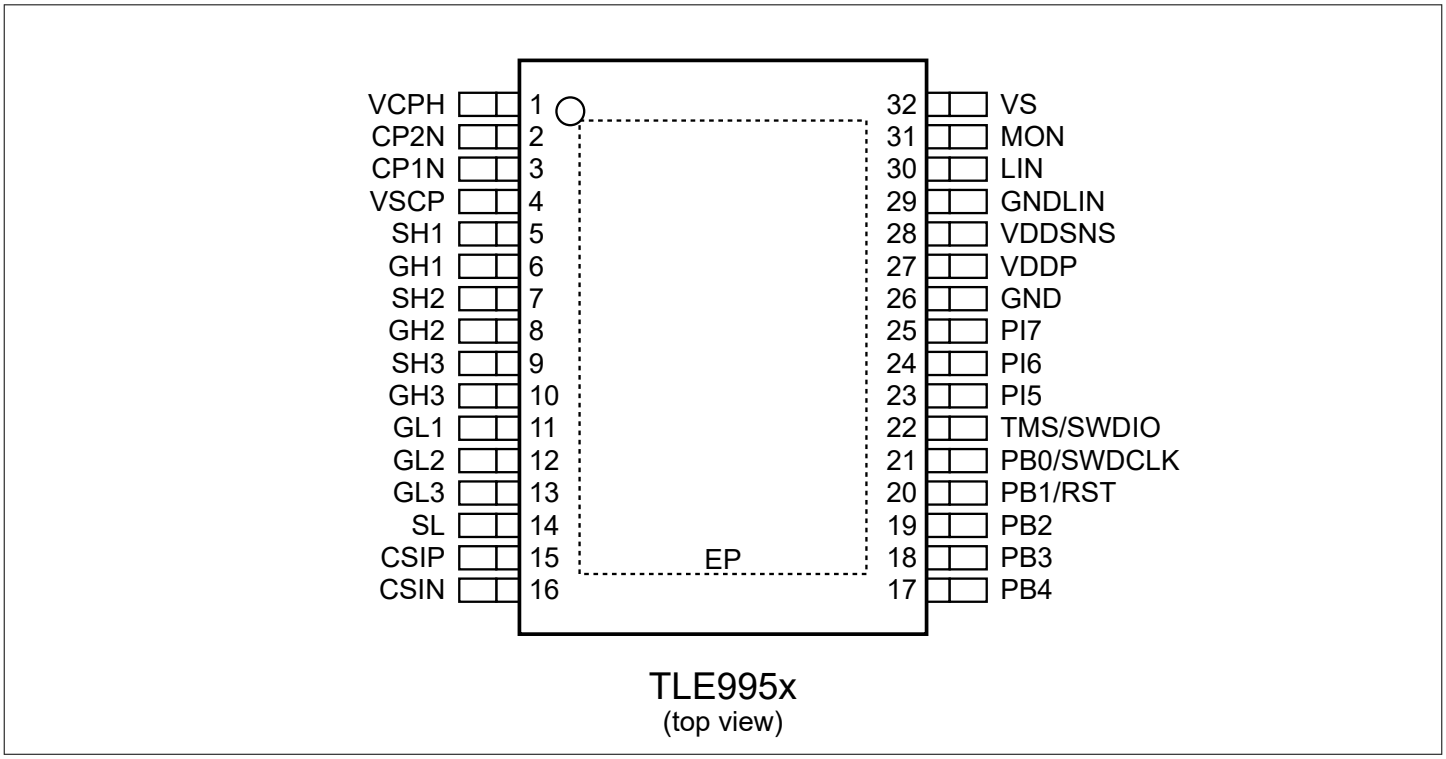

Figure 3 TLE995x pinout

2.2 Pin definitions and functions

Table 1 Pin definitions and functions

Pin no.	Symbol	Function	Comment
1	VCPH	Charge pump output voltage	–
2	CP2N	Charge pump stage 2 driver output	–
3	CP1N	Charge pump stage 1 driver output	–
4	VSCP	Voltage supply charge pump	–
5	SH1	Source external high-side MOSFET 1	–
6	GH1	Gate external high-side MOSFET 1	–
7	SH2	Source external high-side MOSFET 2	–
8	GH2	Gate external high-side MOSFET 2	–
9	NC	–	2-phase BDRV
9	SH3	Source external high-side MOSFET 3	3-phase BDRV
10	NC	–	2-phase BDRV
10	GH3	Gate external high-side MOSFET 3	3-phase BDRV
11	GL1	Gate external low-side MOSFET 1	–
12	GL2	Gate external low-side MOSFET 2	–
13	NC	–	2-phase BDRV
13	GL3	Gate external low-side MOSFET 3	3-phase BDRV
14	SL	Source external low-side MOSFETs	–
15	CSIP	Current sense amplifier positive input	–
16	CSIN	Current sense amplifier negative input	–
17	PB4	Port 4 (bidirectional)	–
18	PB3	Port 3 (bidirectional)	–
19	PB2	Port 2 (bidirectional)	–
20	PB1/RST	Port 1 (bidirectional) / reset	–
21	PB0/ SWDCLK	Port 0 (bidirectional) / bootlatch / serial wire debug clock	–
22	TMS/ SWDIO	Test mode select input / bootlatch / serial wire debug I/O	–
23	PI5	Port 5 (input: analog and digital)	–
24	PI6	Port 6 (input: analog and digital)	–
25	PI7	Port 7 (input: analog and digital)	–
26	GND	Ground	–
27	VDDP	Port supply voltage regulator output	–
28	VDDSNS	Protected 5-V output	–

(table continues...)

Table 1 (continued) Pin definitions and functions

Pin no.	Symbol	Function	Comment
29	GNDLIN	Ground LIN bus	–
30	LIN	LIN bus	–
31	MON	High-voltage monitor input	–
32	VS	Voltage supply	–
–	EP	Exposed pad (backside)	Connect to GND

3 General product characteristics

The following conditions apply to all electrical characteristics unless otherwise specified:

- V_{VS} = 5.5 V to 29 V
- V_{VSCP} = 8 V to 29 V (for BDRV only)
- Grade 0 devices: T_j = -40°C to 175°C
- Grade 1 devices: T_j = -40°C to 150°C
- All voltages with respect to ground
- Positive current flowing into pin

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Voltages – supply pins							
Input voltage	V_S	-0.3	–	40	V	Suppressed load dump acc. to ISO16750-2	PRQ-948
Voltage range VSCP	V_{VSCP}	-0.3	–	48	V	For negative voltages see overload condition	PRQ-1246
VDDP DC output voltage	V_{VDDP}	-0.3	–	5.5	V	–	PRQ-950
VDDSNS load switch output	V_{VDDSNS}	-0.3	–	5.5	V	–	PRQ-949
Slew rate VSCP	SR_{VSCP}	-10	–	10	V/µs	–	PRQ-1247
Voltages – high-voltage pins							
Voltage range MON	V_{MON}	-0.3	–	40	V	–	PRQ-951
Voltage range GHx	V_{GHx}	-8	–	48	V	–	PRQ-1248
Voltage range GHx vs. SHx	$V_{GHx\_vs\_SHx}$	-0.3	–	14	V	–	PRQ-1249
Voltage range SHx	V_{SHx}	-8	–	48	V	–	PRQ-1250
Voltage range GLx	V_{GLx}	-8	–	48	V	–	PRQ-1251
Voltage range GLx vs. SL	$V_{GLx\_vs\_SL}$	-0.3	–	14	V	–	PRQ-1252
Voltage range SL	V_{SL}	-8	–	48	V	–	PRQ-1253
Slew rate Sxx	SR_{Sxx}	-1	–	1	V/ns	–	PRQ-1254
Voltage range CPxN	V_{CPxN}	-0.3	–	V_{VSCP} + 0.3 V	V	–	PRQ-1255
Voltage range VCPH	V_{VCPH}	-0.3	–	48	V	–	PRQ-1256
Voltages – LIN transceiver							
Input voltage at LIN bus	V_{BUS}	-40	–	40	V	–	PRQ-1377

(table continues...)

Table 2 (continued) Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Voltages – GPIOs							
Voltage on port pin PBx, PIx and TMS	V_{IN}	-0.3	–	V_{VDDP} + 0.3	V	$V_{IN} < V_{VDDPmax}$	PRQ-1458
Voltages – current sense amplifier inputs							
Voltage range CSIP and CSIN	V_{CSIx}	-8	–	8	V	–	PRQ-1346
Currents							
Max. current at VCPH pin	I_{VCPH}	-15	–	–	mA	–	PRQ-1257
Temperatures							
Device junction temperature	T_J	-40	–	175	°C	For Grade 0 devices	PRQ-954
Device junction temperature	T_J	-40	–	150	°C	For Grade 1 devices	PRQ-955
ESD robustness							
ESD robustness all pins (HBM)	V_{ESD_HBM1}	-2	–	2	kV	1)	PRQ-923
ESD robustness LIN vs. GNDLIN (HBM)	V_{ESD_HBM2}	-6	–	6	kV	1)	PRQ-1517
ESD robustness all pins (CDM)	V_{ESD_CDM1}	-500	–	500	V	2)	PRQ-924
ESD robustness corner pins (CDM)	V_{ESD_CDM2}	-750	–	750	V	2)	PRQ-925

1) Human body model (HBM) robustness according to AEC-Q100-002.
2) Charged device model (CDM) robustness according to AEC-Q100-011 Rev-D; voltage refers to test condition (TC) mentioned in the standard.

EMC

EMC susceptibility according to BISS generic IC test specification, release 2.0.

***Notes**:*

1. *Stresses above those listed under “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the section "functional range" is not implied. Furthermore, only single error cases are assumed. More than one stress/error case may also damage the device.*
2. *Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions the voltage on VDD pins with respect to ground shall not exceed the values defined by the absolute maximum ratings.*
3. *Lifetime statements are an anticipation based on an extrapolation of Infineon’s qualification test results. The actual lifetime of a component depends on its form of application and type of use etc. and may deviate from such statement. Lifetime statements shall in no event extend the agreed warranty period.*

3.1.1 Overload currents

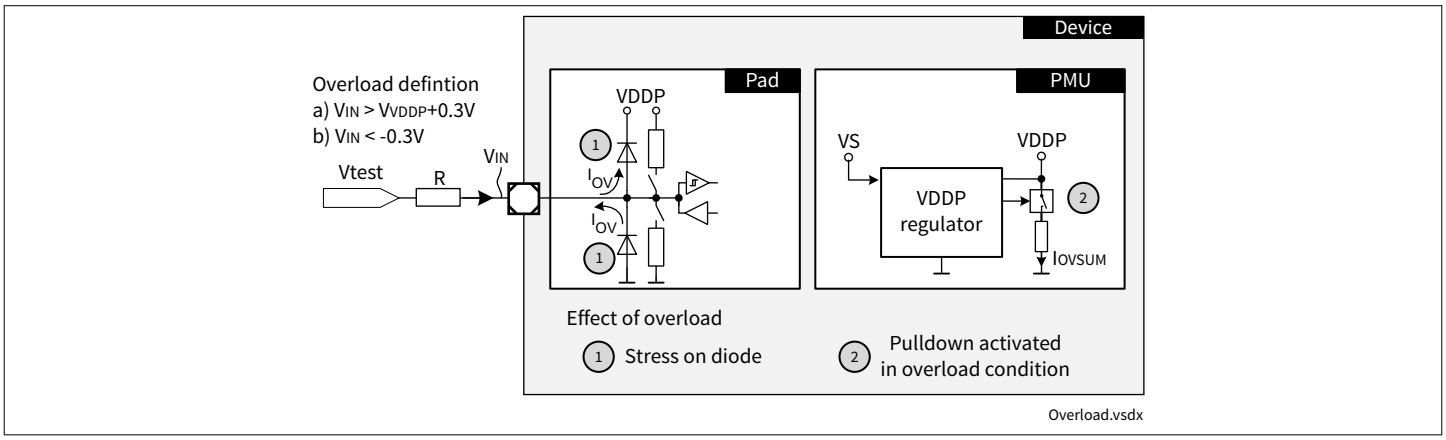

Figure 4 Example application diagram showing GPIO overload current definition (I_{OV})

An overload current condition occurs if the input voltage at PBx/PIx V_{IN} < -0.3 V or V_{IN} > V_{VDDP} + 0.3 V. The overload current I_{OV} must be limited.

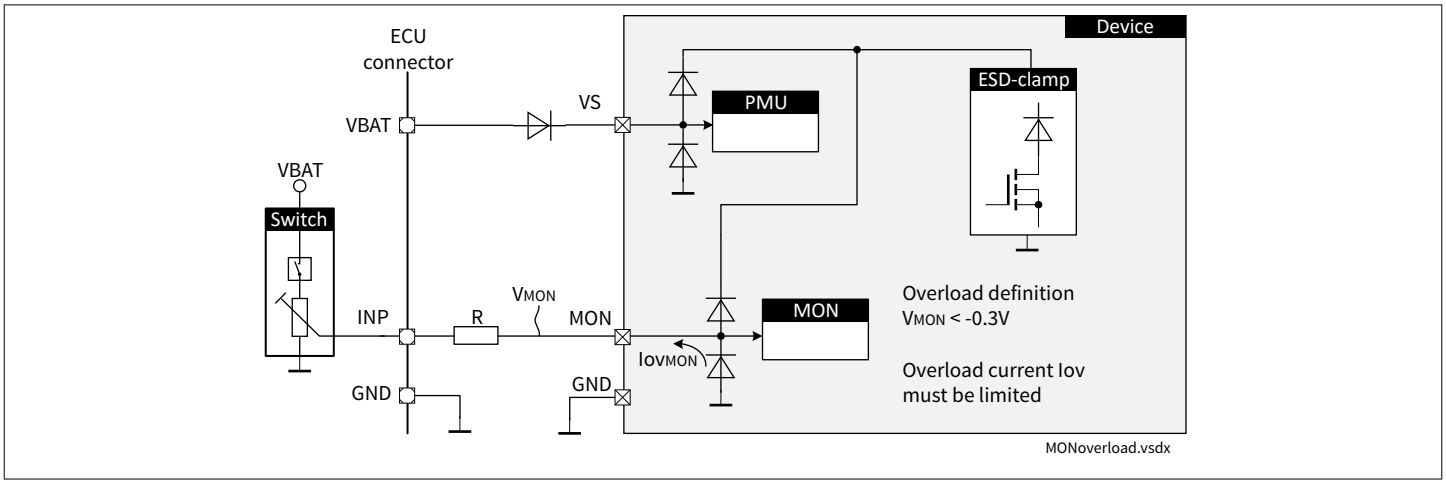

Figure 5 Example application diagram showing MON overload current definition (I_{OVMON})

An overload current condition occurs if the input voltage V_{MON} < -0.3 V. The overload current I_{OVMON} must be limited.

Table 3 Overload currents

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Overload current on PBx and TMS	I_{OVPB}	-2	–	2	mA	[1] Overload current must be limited, for example, via series resistor	PRQ-1459
Overload current on PIx	I_{OVPI}	-1	–	2	mA	[1] Overload current must be limited, for example, via series resistor	PRQ-1460
Sum of overload currents	I_{OVSUM}	-4	–	4	mA	[1] The number of pins with overload must be limited to maximum 4 pins	PRQ-1461

(table continues...)

Table 3 (continued) Overload currents

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Overload current on VSCP pin	I_{OVVSCP}	-500	–	–	mA	t < 8 ms	PRQ-1258
Overload current on MONx pin(s)	I_{OVMON}	-28	–	–	mA	–	PRQ-953

1) Overload conditions occur if the standard operating conditions are exceeded, for example, the input voltage V_{IN} at the pin exceeds the specified range: $V_{IN} > V_{VDDP} + 0.3$ V ($I_{OV} > 0$) or $V_{IN} < -0.3$ V ($I_{OV} < 0$).

3.2 Functional range

The following functional range must not be exceeded in order to ensure correct operation of the device. All parameters specified in the following sections refer to these operating conditions unless otherwise indicated.

Table 4 Functional range

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Input voltage range VS	V_S	5.5	–	29	V	*1)*	PRQ-1540
Extended input voltage range VS	V_S	29	–	35	V	Allowed for $t \leq 400$ ms With parameter deviation	PRQ-1541
Extended input voltage range VS	V_S	3.6	–	5.5	V	Due to derived voltage dependency following modules show parameter deviation: GPIO, CSA, ADC12, MON, BDRV, LINTRX	PRQ-1542
Voltage range VSCP	V_{VSCP}	8	–	29	V	–	PRQ-1259
Extended voltage range VSCP	V_{VSCP_EXT}	29	–	32	V	Allowed for t_{max} < 400 ms With parameter deviations	PRQ-1260
Extended voltage range VSCP	V_{VSCP_EXT}	7	–	8	V	With parameter deviations	PRQ-1261

1) At T_j > 150°C with slow power-up ramps at VS the device starts up between V_S = 5.5 V to 7 V.

3.3 Current consumption

Table 5 Current consumption

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Current consumption in Active mode	I_{VS_act40}	–	25	30	mA	V_S = 3.6 V to 29 V; see table "Active mode current consumption"	PRQ-905

(table continues...)

Table 5 (continued) Current consumption

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Current consumption in Active mode with reduced frequency	I_{VS_act20}	–	–	18	mA	V_S = 3.6 V to 29 V; see table "Active mode current consumption"	PRQ-907
Current consumption in Active mode with LIN receive only	I_{VS_actLIN}	–	–	15	mA	VS = 3.6 V to 29 V; see table "Active mode current consumption"	PRQ-908
Current consumption in Sleep mode	I_{VS_slp}	–	20	35	µA	V_S = 7.3 V to 18 V; T_J = -40°C to 85°C; see table "Sleep mode current consumption"	PRQ-910
Current consumption in Stop mode	I_{VS_stp}	–	60	80	µA	V_S = 7.3 V to 18 V; T_J = -40°C to 85°C; see table "Stop mode current consumption"	PRQ-912
ON-state current consumption VSCP	$I_{VSCP(ON)}$	–	35	60	mA	Bridge driver fully operating. I_{VCPH} = -8 mA	PRQ-1263
OFF-state current consumption VSCP	$I_{VSCP(OFF)}$	–	–	3	µA	Bridge driver off. V_S = 13.5 V; T_J = 85°C	PRQ-1264

3.3.1 Active mode, Sleep mode and Stop mode current consumption

Table 6 Active mode current consumption

	I_{VS_act40}	I_{VS_act20}	I_{VS_actLIN}
SYS0CLK	40 MHz	20 MHz	20 MHz
MCU subsystem	Active	Active	Active with CPU in IDLE mode
Timers and communication	Active	Active	Disabled
ADC, CSA	Converting	Converting	Disabled
LINTRX	Receiving	Receiving	In receive-only mode
BDRV, CP	PWM at 3 ph with 20 kHz[1)]	PWM at 3 ph with 20 kHz[1)]	Disabled
VDDSNS	No load	No load	Disabled
GPIO	Input without load	Input without load	Input without load
Wake configuration	Via MON	Via MON	Via MON

[1)] Only applicable for functional range V_{VSCP} = 8 V to 29 V

Table 7 Sleep mode current consumption

	I_{VS_slp}
SYS0CLK	Off
MCU subsystem	Off
Timers and communication	Off
ADC, CSA	Off
LINTRX	Off
BDRV, CP	SSO active
VDDSNS	Off
GPIO	Input, terminated to GND or VDDP without load
MON	Terminated to GND or VS
Wake configuration	Via LIN

Table 8 Stop mode current consumption

	I_{VS_stp}
SYS0CLK	Off
MCU subsystem	Stopped
Timers and communication	Off
ADC, CSA	Off
LINTRX	Off
BDRV, CP	SSO active
VDDSNS	Off
GPIO	Input, terminated to GND or VDDP without load
MON	Terminated to GND or VS
Wake configuration	Via LIN

3.4 Thermal resistance

Table 9 Thermal resistance

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Junction to case for TSDSO32	R_{THJC}	–	5	–	K/W	T_A = 85°C	PRQ-913
Junction to ambient for TSDSO32	R_{THJA}	–	32	–	K/W	1) T_A = 85°C	PRQ-914
Psi junction to top for TSDSO32	Ψ_{JT}	–	4	–	K/W	1) T_A = 85°C	PRQ-1610

1) According to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board. Board: 76.2x114.3x1.5mm^3 with 2 inner copper layers (35µm thick), with thermal via array under the exposed pad contacting the first inner copper layer and 300mm^2 cooling area on the bottom layer (70µm).

4 Power management unit (PMU)

4.1 Features overview

The power management unit (PMU) manages all functions related to the device power supply and its supervision. The PMU controls all operating mode transitions and ensures fail-safe behavior.

The PMU provides following features:

- Power supply topology
  - Linear voltage regulator VDDP for internal peripherals supply
  - Power switch VDDSNS for off-chip circuitry supply (for example, sensors)
  - Linear voltage regulator VDDC for internal logic supply
  - Linear voltage regulator VDD1V5NVM for the non-volatile memory supply
- State machine
- Wake management
- Fail-safe supervision
  - Supply monitor, monitoring of fail-safe relevant voltages
  - Clock monitor
  - Fail-safe window watchdog for CPU execution timing monitoring
  - Overtemperature monitoring
- Interrupt management
- Reset management controlling the reset behavior of the entire device
  - Bi-directional reset input/output (I/O) as reset input and reset output indicating an internally generated reset
- Data retention memory for data storage

4.2 Block diagram

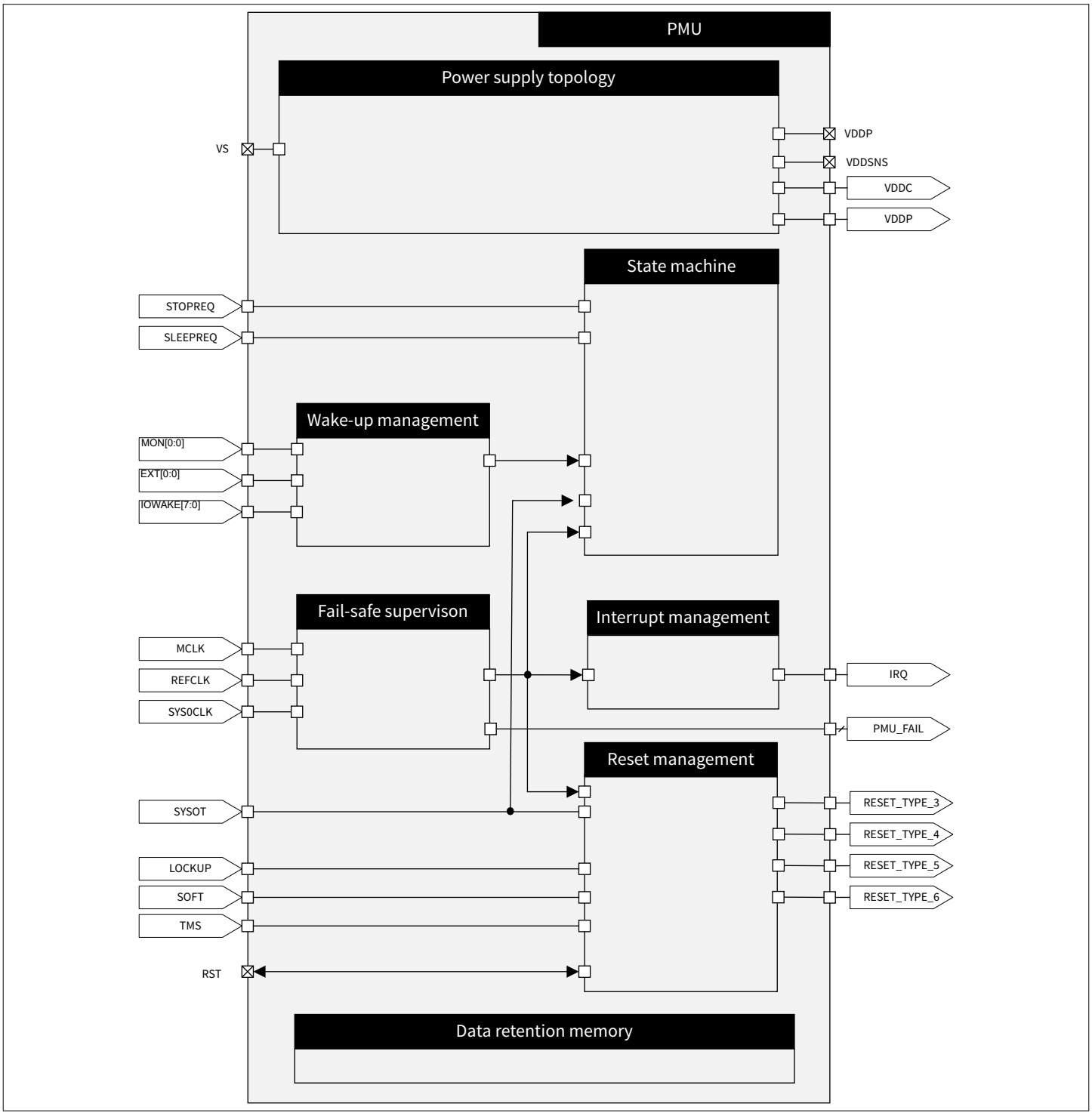

Figure 6 PMU block diagram

4.3 Electrical characteristics PMU

4.3.1 VDDP low-dropout linear regulator

Table 10 VDDP low-dropout linear regulator

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
VDDP DC output voltage	V_{VDDP}	4.9	5.0	5.1	V	0 mA ≥ I_{VDDP} ≥ $I_{VDDPSRC}$	PRQ-1039
VDDP DC output current capability	$I_{VDDPSRC}$	0	–	45	mA	VDDSNS disabled External application type of loads	PRQ-1016
VDDP transient load regulation	ΔV_{DDP}	-100	–	100	mV	t_r = 1 µs t_f = 1 µs I_{VDDP} = 20% to 80% to 20% of $I_{VDDPSRC(max)}$	PRQ-1040
VDDP transient line regulation	ΔV_{DDP}	-500	–	500	mV	I_{VDDP} = 5 mA V_S steps from 5.5 V to 18 V to 5.5 V with $\Delta V/\Delta t$ = 5 V/µs	PRQ-1041
VDDP regulator dropout voltage	$V_{VDDPDROP}$	–	100	300	mV	T_J = 125 °C I_{VDDP} = 20 mA $V_S = V_{S\_EXT(min)}$	PRQ-1042
VDDP regulator current limit	$I_{VDDPILIM}$	90	130	250	mA	V_{VDDP} = 0 V	PRQ-1043
VDDP regulator current limit signal filter time	$t_{VDDPILIMFT}$	2	4	6	µs	–	PRQ-1044
VDDP current limit power-up blanking time	$t_{VDDPILIMBT}$	400	500	600	µs	–	PRQ-1056
VDDP monitor undervoltage falling threshold	$V_{VDDPUVFALL}$	3	3.1	3.2	V	–	PRQ-1045
VDDP monitor undervoltage hysteresis	$V_{VDDPUVHYS}$	215	300	350	mV	–	PRQ-1046
VDDP monitor undervoltage warning falling threshold	$V_{VDDPUVWFALL}$	4.3	4.5	4.7	V	–	PRQ-1048
VDDP monitor undervoltage warning hysteresis	$V_{VDDPUVWHYS}$	80	100	120	mV	–	PRQ-1047
VDDP monitor overvoltage rising threshold	$V_{VDDPOVRISE}$	5.65	5.9	6.15	V	–	PRQ-1050

(table continues...)

Table 10 (continued) VDDP low-dropout linear regulator

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
VDDP monitor overvoltage hysteresis	$V_{VDDPOVHYS}$	100	120	140	mV	–	PRQ-1049
VDDP overshoot at startup	ΔV_{DDP}	–	–	100	mV	–	PRQ-1051
PSRR VDDP regulator	$PSRR_{VDDP}$	50	55	–	dB	V_S = 13.5 V f = 1 kHz $I_{VDDPSRC}$ = 20 mA	PRQ-1052
PSRR VDDP regulator	$PSRR_{VDDP}$	38	43	–	dB	V_S = 13.5 V f = 10 kHz $I_{VDDPSRC}$ = 20 mA	PRQ-1053
PSRR VDDP regulator	$PSRR_{VDDP}$	15	20	–	dB	V_S = 13.5 V f = 100 kHz $I_{VDDPSRC}$ = 20 mA	PRQ-1054

4.3.2 VDDSNS low-dropout load switch

Table 11 VDDSNS low-dropout load switch

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
VDDSNS load switch dropout voltage	$V_{VDDSNSDROP}$	–	250	500	mV	VDDSNS enabled $I_{VDDSNS} = I_{VDDSNSSRC(max)}$	PRQ-1058
VDDSNS DC output current capability	$I_{VDDSNSSRC}$	0	–	30	mA	–	PRQ-1015
VDDSNS load switch current limit	$I_{VDDSNSILIM}$	30	45	60	mA	V_{VDD} = 5 V V_{VDDSNS} = 0 V VDDSNS enabled	PRQ-1059
VDDSNS load switch current limit signal filter time	$t_{VDDSNSILIMFT}$	2	4	6	µs	–	PRQ-1060
VDDSNS turn-on time	$t_{VDDSNSON}$	–	700	1000	µs	C_{VDDSNS} = 2 µF VDDSNS load = 2 kΩ VDDSNS enable event to V_{VDDSNS} = 90% of target value	PRQ-1061
VDDSNS pull-down resistance	$R_{VDDSNSPD}$	–	3	6	kΩ	VDDSNS disabled	PRQ-1064

4.3.3 System state control

Table 12 System state control

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Unsupplied to Active mode	$t_{UNSUP2ACT}$	–	–	5	ms	Time power-up event to first instruction execution in user software or BSL ready	PRQ-1600
Active to Stop mode	$t_{ACT2STP}$	–	–	250	µs	Triggered by Stop mode request	PRQ-1071
Active to Sleep mode	$t_{ACT2SLP}$	–	–	250	µs	Triggered by Sleep mode request	PRQ-1072
Sleep to Active mode	$t_{SLP2ACT}$	–	–	5	ms	Triggered by a wake-up event	PRQ-1601
Fail-sleep to Active mode	$t_{FSLP2ACT}$	–	–	5	ms	Triggered by wake-up event	PRQ-1602
Stop to Active mode	$t_{STP2ACT}$	–	–	300	µs	Triggered by a wake-up event	PRQ-1075

4.3.4 Reset management

Table 13 Reset management

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
RESET output active low time	$t_{RESETOUT}$	80	100	120	µs	–	PRQ-1076
RESET blind time	$t_{RESETBLIND}$	800	–	1250	µs	–	PRQ-1077
RESET input low pulse width	$t_{RESETLPW}$	150	–	–	µs	–	PRQ-1078

4.3.5 PMU overtemperature

Table 14 PMU overtemperature

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Overtemperature protection	T_{JPMU_OT}	175	185	195	°C	–	PRQ-1021
Overtemperature signal filter time	t_{PMU_OTFT}	6	8	10	µs	–	PRQ-1023

5 System control unit (SCU)

5.1 Features overview

The system control unit (SCU) provides the clocks for the MCU and peripherals in all operation modes. The SCU provides the operation mode control and interrupt assignment for dedicated peripherals and the NMI.

The SCU provides following features:

- Clock sources
- Clock configuration
- Operation mode control
- Interrupt assignment

5.2 Block diagram

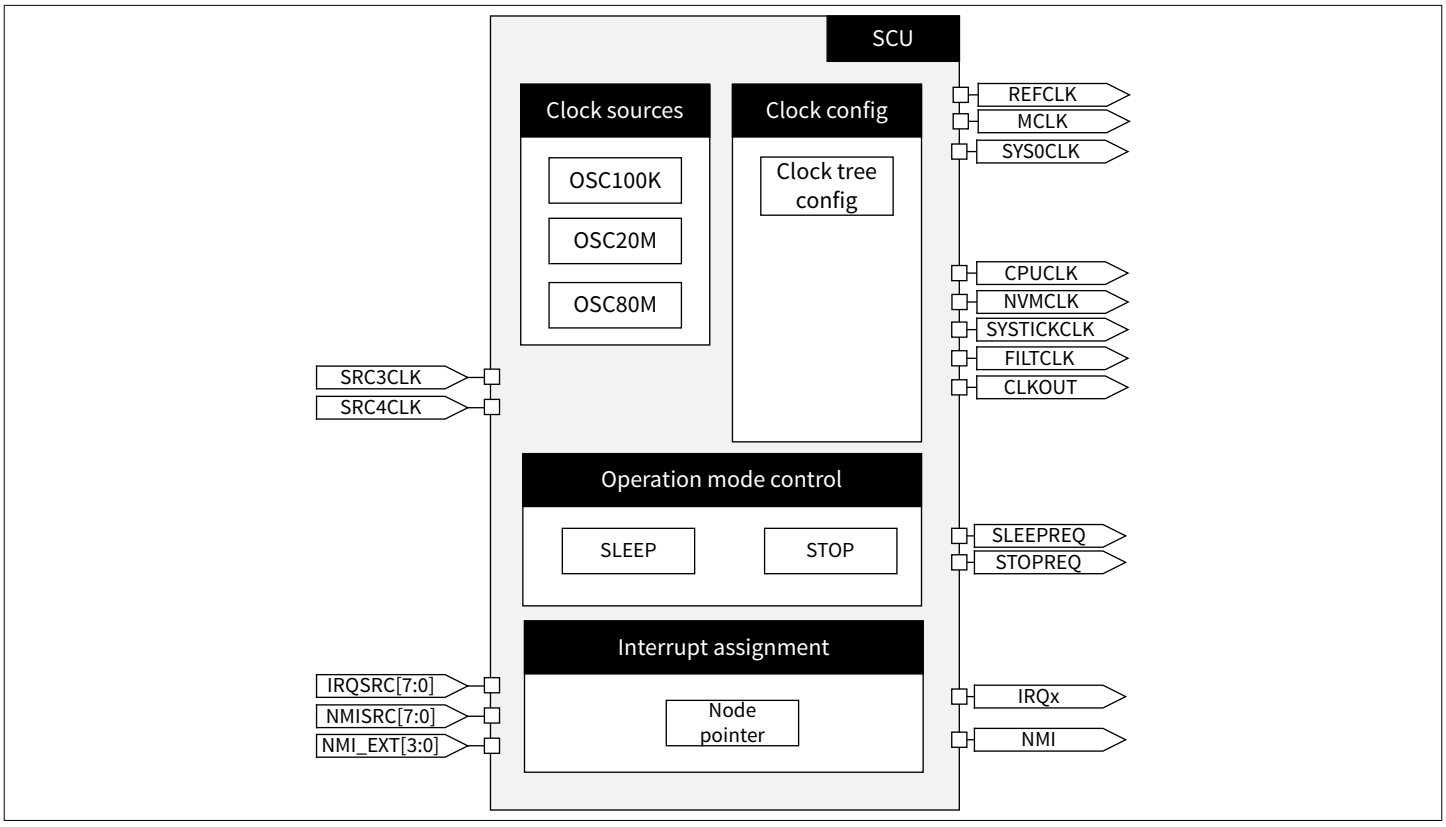

Figure 7 SCU block diagram

5.3 Electrical characteristics SCU

5.3.1 Clock sources

Table 15 Electrical characteristics clock sources

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Oscillator 80 MHz	f_{OSC80M}	78.8	80	81.2	MHz	–	PRQ-1108
Oscillator 20 MHz	f_{OSC20M}	17	20	23	MHz	–	PRQ-1110
Oscillator 100 kHz	$f_{OSC100K}$	85	100	115	kHz	–	PRQ-1111

5.3.2 Clock control

Table 16 Electrical characteristics clock control

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SYS0CLK frequency	$f_{SYS0CLK}$	1.9	40	40.6	MHz	–	PRQ-1096
Filter clock frequency	$f_{FILTCLK}$	1.9	2	2.1	MHz	To be ensured by user configuration	PRQ-1097

5.3.3 Clock monitoring

Table 17 Electrical characteristics clock monitoring

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Reference clock (REFCLK) failure detection time	$t_{REFCLKFD}$	11	14	17	µs	Timing is referred to the master clock (MCLK)	PRQ-1098
Master clock (MCLK) watchdog timeout to device reset time	$t_{M\_CLKLOSS}$	25	30	35	µs	Timing is referred to the standby clock (REFCLK)	PRQ-1099

5.3.4 Peripheral control

Table 18 Electrical characteristics peripheral control

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Peripheral control sequencing time	t_{POWSEQ}	–	–	0.2	ms	–	PRQ-1100

6 Fail-safe unit (FSU)

6.1 Features overview

The safe shutdown mechanism brings the bridge driver (BDRV) into a safe off-state and disables the LIN transceiver's (LINTRX) output stage.

6.2 Block diagram

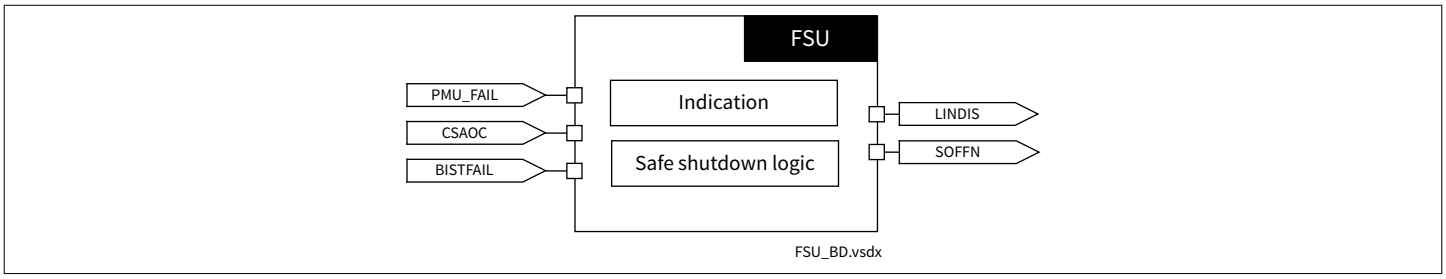

Figure 8 FSU block diagram

7 Microcontroller subsystem (MCU)

7.1 Features overview

The microcontroller subsystem (MCU) consists of the CPU, memory system, and other CPU-centric functions.
The MCU provides following features:

- Arm® Cortex®-M23 core with Thumb® and Thumb®-2 instruction set
  - Fast multiply (one cycle)
  - Fast divide (17 cycles)
- TrustZone® for Arm®v8-M
  - Four security attribution units (SAU)
  - Four non-secure memory protection regions
  - Four secure memory protection regions
- Memory protection unit (MPU)
- Memory system
  - Non-volatile memory (Flash) with up to 72 KB
  - Volatile data memory (SRAM) with up to 6 KB
  - Memory access protection
  - Built-in error correction
- Read-only memory (BootROM) providing different functionalities
  - Startup procedure
  - Bootstrap loader (BSL)
  - Flash utilities (API)
- Debug access port (DAP) accessible via serial wire debug (SWD)
  - Halt after reset (HAR)
  - Four hardware breakpoints
  - Two data watchpoints
  - System memory access
  - Can be disabled for IP protection
- Nested vectored interrupt controller (NVIC)
  - 32 external interrupt inputs
  - Programmable interrupt priority levels
  - Dynamic re-prioritization
- System timer (SYSTICK) with interrupt capability
- CRC engine to enable data integrity

***Note**:* *This product does not implement any cybersecurity requirements. Therefore, no ISO 21434-compliant development can be claimed for this product.*

However, a cybersecurity risk analysis (TARA- Threat Analysis and Risk Assessment) has been performed for this product, in accordance with the ISO 21434.

The cybersecurity claims, derived out of this risk analysis, are mandatory to be implemented by any customer integrating this product into a cybersecurity-relevant environment, to sufficiently mitigate the risk of cybersecurity threats to this product, which were identified during the product risk analysis.

These cybersecurity claims can be found in the Datasheet Addendum Z8F80819882.

7.2 Block diagram

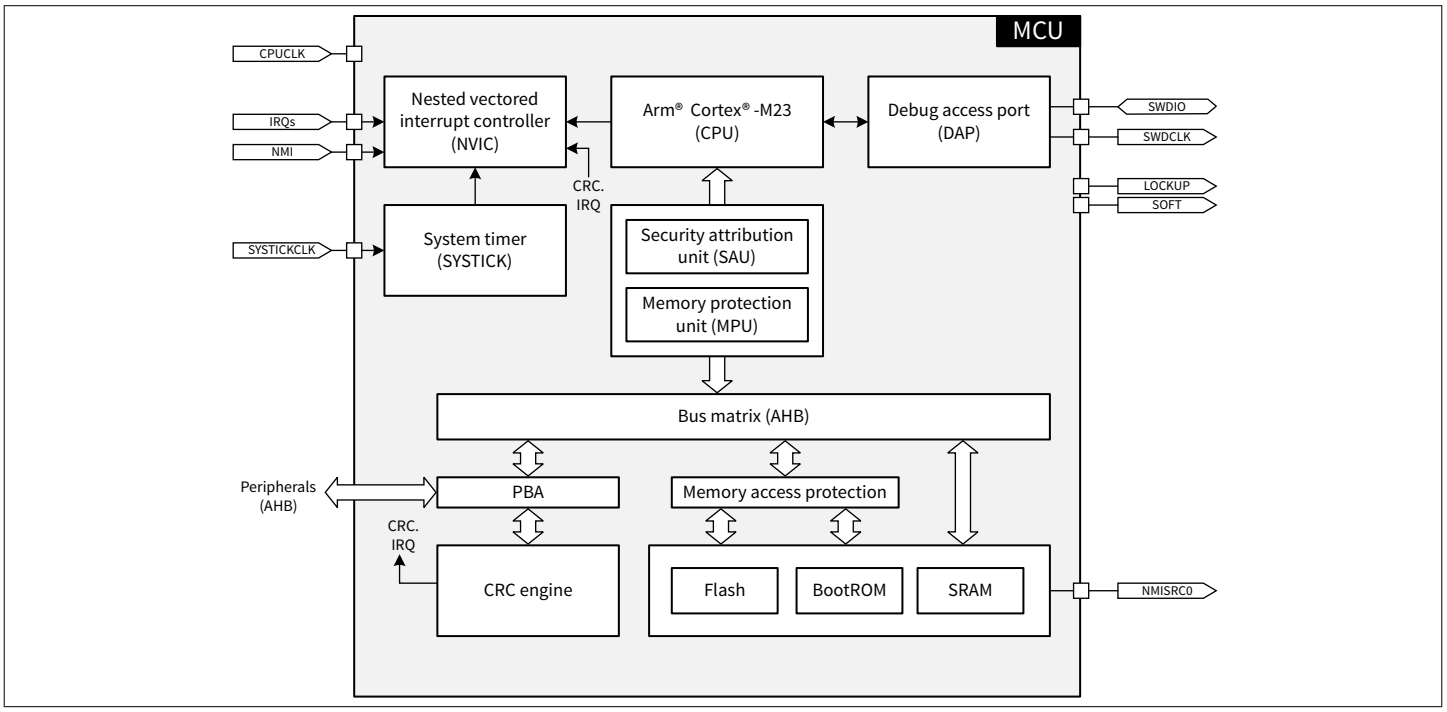

Figure 9 MCU block diagram

7.3 Electrical characteristics FLASH

Table 19 Electrical characteristics FLASH

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Write time per page	t_{WR}	–	3	3.5	ms	–	PRQ-1138
Erase time per sector/ page	t_{ER}	4	4.5	–	ms	–	PRQ-1139
Endurance normal	N_{ER}	1000	–	–	cycles	Number of times a Flash page belonging to the UBSL or UCODE segment can be cycled (write-erase).	PRQ-1140
Endurance high	N_{ER1}	30000	–	–	cycles	Number of times a Flash page belonging to the UDATA or EEPROM segment can be cycled (write-erase).	PRQ-1141
Data retention for normal endurance	t_{RET}	20	50	–	years	–	PRQ-1142
Data retention for high endurance	t_{RET1}	5	–	–	years	–	PRQ-1143

8 High-voltage monitor (MON)

8.1 Features overview

The high-voltage monitor input (MON) monitors external voltage levels above or below the threshold V_{MONth}.
The MON provides following features:

- High-voltage inputs with threshold voltage 3 V (typ.)
- Programmable edge slope
- Programmable pull-up and pull-down devices
- Programmable wake-up capability
- Available as peripheral interconnection and IRQ

8.2 Block diagram

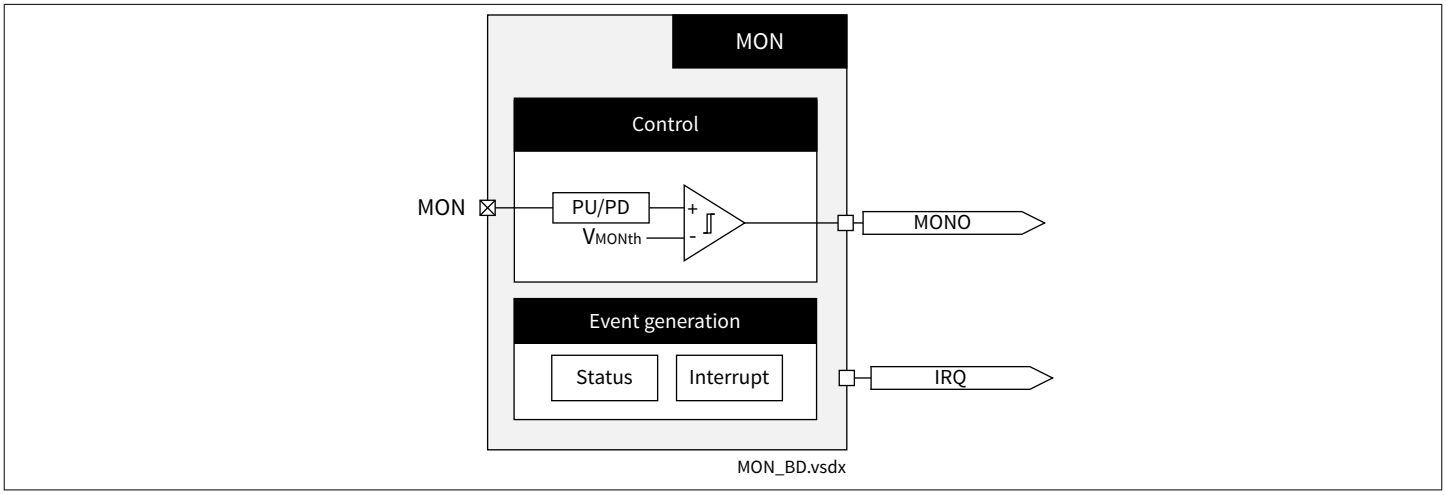

Figure 10 MON block diagram

8.3 Electrical characteristics MON

Table 20 High voltage monitor (MON)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
External voltage monitoring threshold	V_{MONth}	2	3	3.5	V	–	PRQ-1065
External voltage monitoring threshold hysteresis	$V_{MONth,hys}$	0.1	–	0.7	V	–	PRQ-1066
Pull-up current	$I_{PU,MON}$	-20	-10	-3	uA	V_{MON} = 3.5 V	PRQ-1067
Pull-down current	$I_{PD,MON}$	3	10	20	uA	V_{MON} = 2 V	PRQ-1068
Input leakage current	$I_{LK,MON}$	-2	–	2	uA	–	PRQ-1069

9 Temperature sensor (DTS)

9.1 Features overview

The temperature sensor (DTS) provides a voltage correlated to the die temperature.

9.2 Block diagram

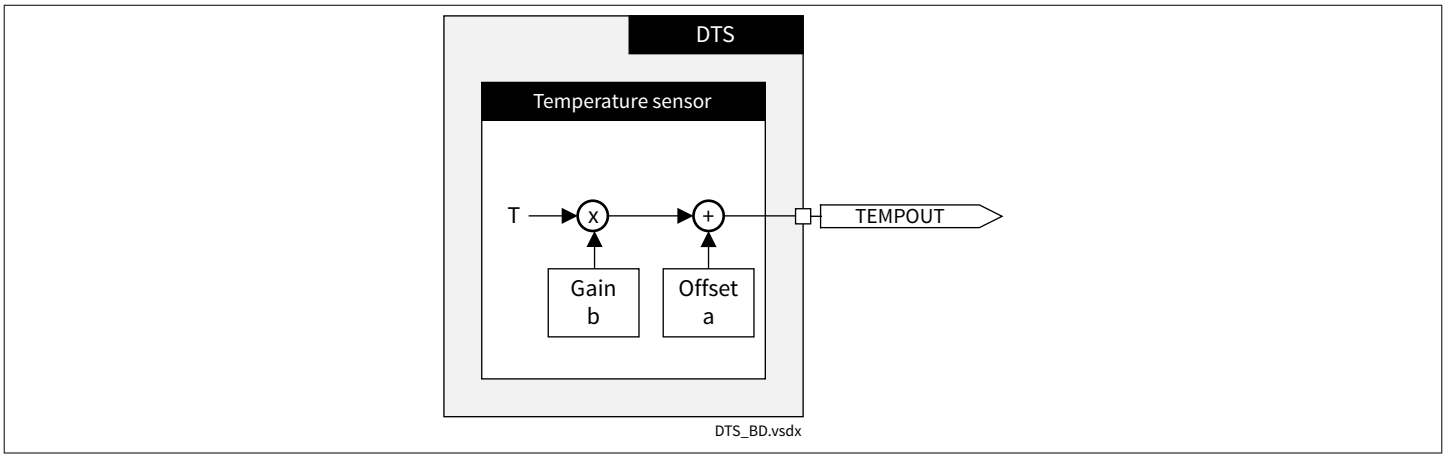

Figure 11 DTS block diagram

9.3 Electrical characteristics DTS

Table 21 Electrical characteristics DTS

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Accuracy 1	Acc_1	-20	–	20	K	-40°C < T_j < 85°C	PRQ-1534
Accuracy 2	Acc_2	-5	–	5	K	85°C ≤ Tj ≤ 125°C	PRQ-1537
Accuracy 3	Acc_3	-10	–	10	K	125°C < T_j < 175°C	PRQ-1536
Offset coefficient (a)	a	–	266	–	mV	–	PRQ-1538
Gain coefficient (b)	b	–	4.26	–	mV/°C	–	PRQ-1539

10 General purpose input and outputs (GPIO)

10.1 Features overview

A general purpose input/output (GPIO) consists of the input/output driver stage and the port control logic.
The GPIO provides following features:

Input/output port functions (PBx)

- The output state is programmable and the input state is readable
- The output driver is programmable as push-pull, open drain, and tri-state
- The output driver is programmable in strength and slew rate
- The port has programmable pull-up and pull-down devices
- The output driver has multiple alternate input options
- The input is available as peripheral interconnection and IRQ

Input port functions (PIx)

- The input state is readable
- The port has programmable pull-up and pull-down devices
- The input is available as peripheral interconnection and IRQ

10.2 Block diagram

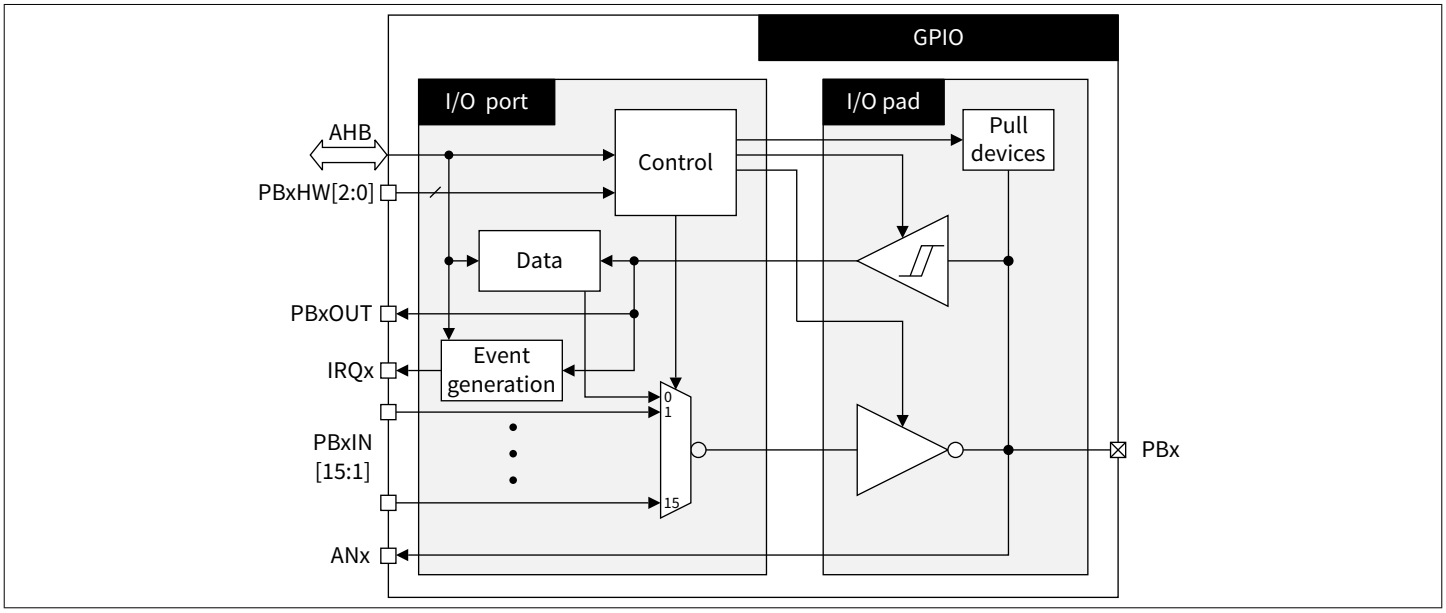

Figure 12 Block diagram for bi-directional port type GPIO (PBx)

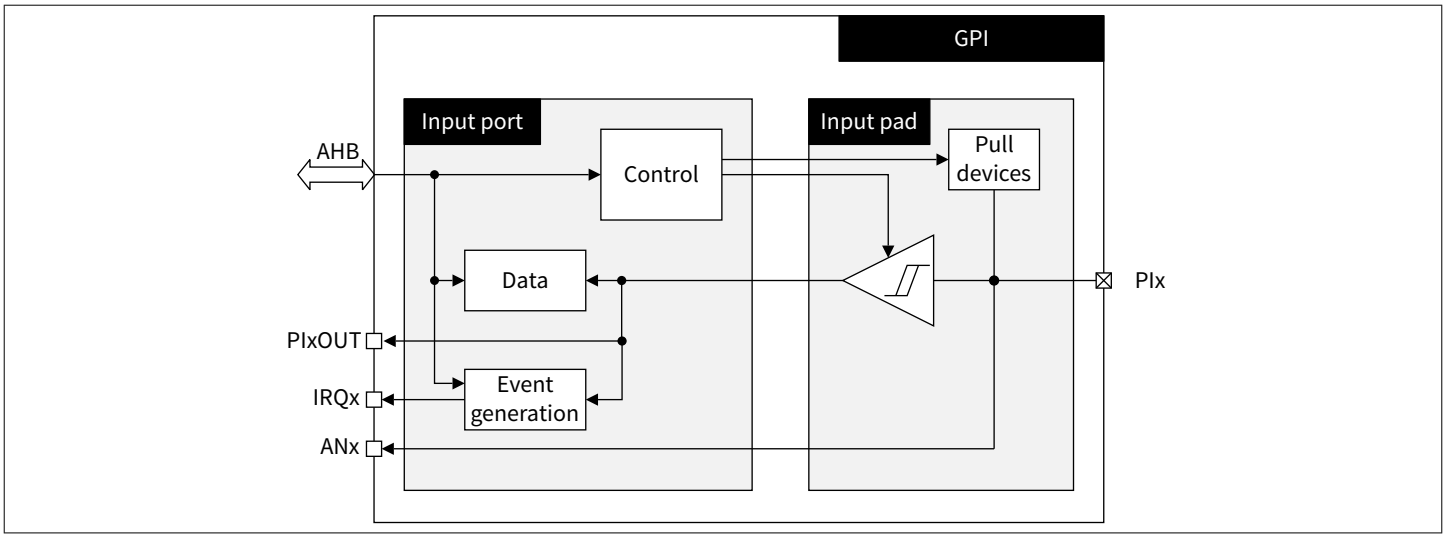

Figure 13 Block diagram for uni-directional port type GPI (PIx)

10.3 Electrical characteristics GPIO

10.3.1 Voltages and currents

A pull-up/pull-down device can be selected to keep or force current on PBx/PIx:

- Keep current: limit the current through this pin below the keep current (I_{PUK}, I_{PDK}) so that the enabled pull device can keep the pin level
- Force current: drive at least the force current (I_{PUF}, I_{PDF}) through this pin to override the pin level driven by the enabled pull device

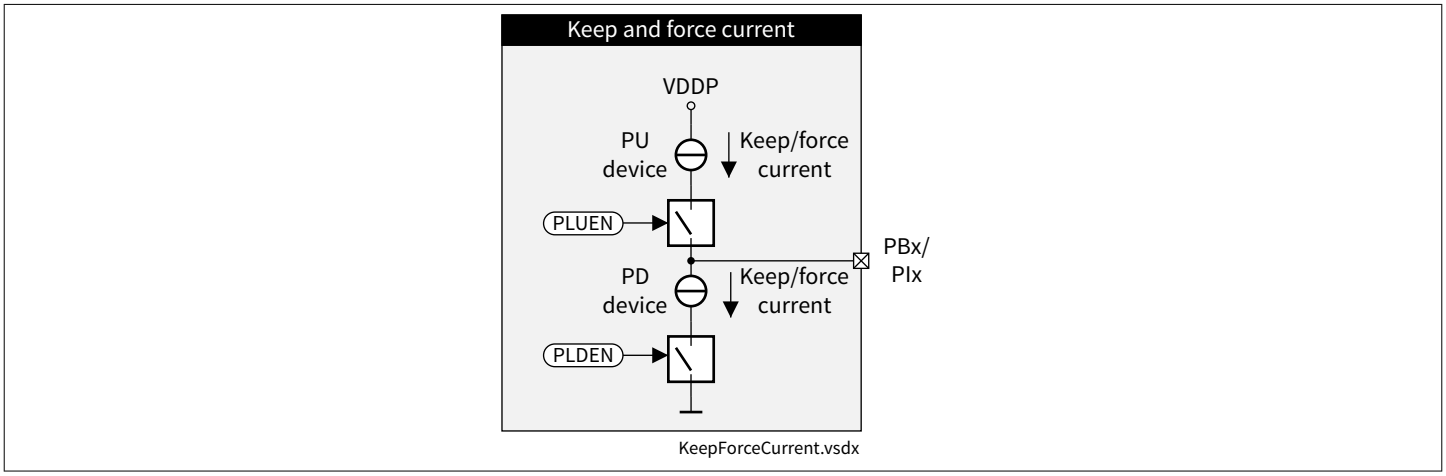

Figure 14 Keep and force current diagram

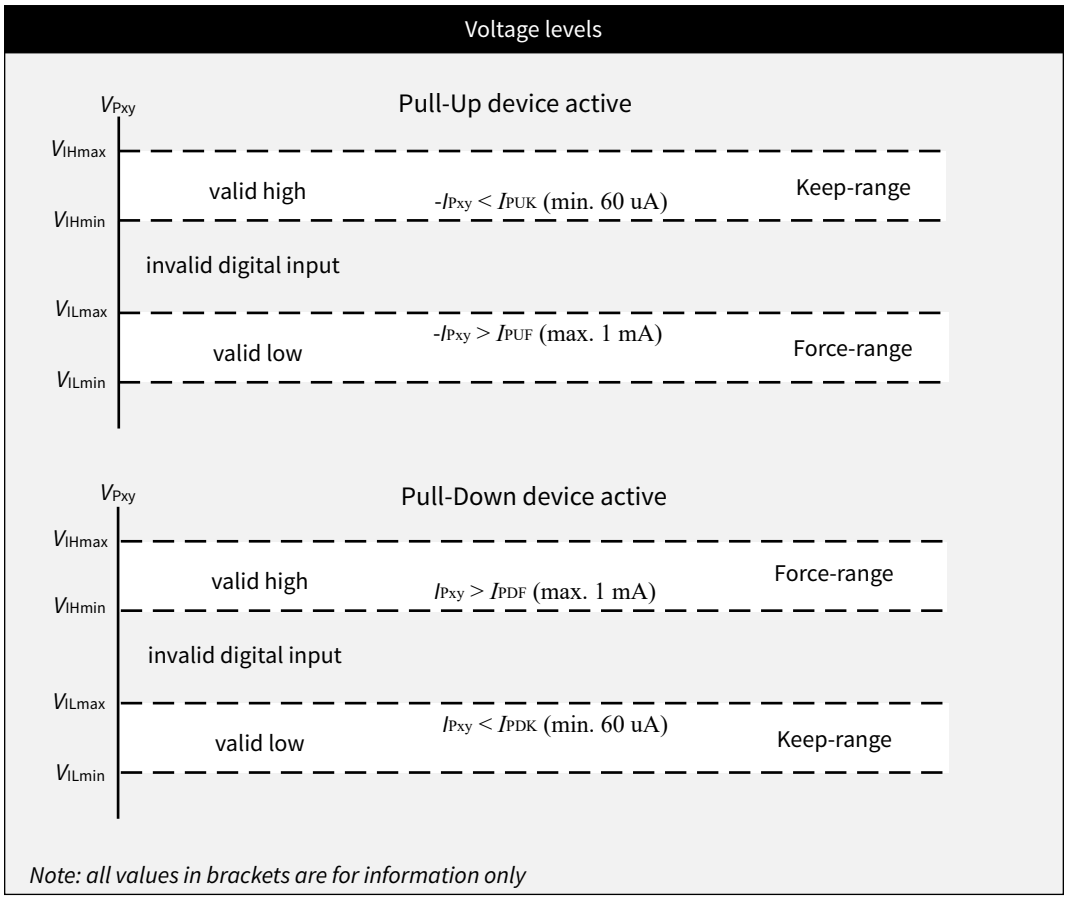

Figure 15 Voltage levels

10.3.2 Input stage and pull devices

Table 22 Input stage and pull devices

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Input low voltage	V_{IL}	-0.3	–	0.3 × V_{VDDP}	V	1) 2.55 V ≤ V_{VDDP} ≤ 5.5 V	PRQ-1475
Input high voltage	V_{IH}	0.7 × V_{VDDP}	–	V_{VDDP} + 0.3	V	1) 2.55 V ≤ V_{VDDP} ≤ 5.5 V	PRQ-1476
Input hysteresis	V_{HYS}	0.11 × V_{VDDP}	–	–	V	4.5 V ≤ V_{VDDP} ≤ 5.5 V Series resistance = 0 Ω	PRQ-1477
Input hysteresis	V_{HYSext}	0.04 × V_{VDDP}	–	–	V	1) 2.55 V ≤ V_{VDDP} < 4.5 V Series resistance = 0 Ω	PRQ-1478

(table continues...)

Table 22 (continued) Input stage and pull devices

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Pull-up keep current	I_{PUK}	60	–	–	µA	4.5 V ≤ V_{VDDP} ≤ 5.5 V V_{IN} = V_{IHmin} IPU definition (non-default): positive current flowing out of pin	PRQ-1479
Pull-up force current	I_{PUF}	–	–	1	mA	4.5 V ≤ V_{VDDP} ≤ 5.5 V V_{IN} = V_{ILmax} IPU definition (non-default): positive current flowing out of pin	PRQ-1480
Pull-down keep current	I_{PDK}	60	–	–	µA	4.5 V ≤ V_{VDDP} ≤ 5.5 V V_{IN} = V_{ILmax}	PRQ-1481
Pull-down force current	I_{PDF}	–	–	1	mA	4.5 V ≤ V_{VDDP} ≤ 5.5 V V_{IN} = V_{IHmin}	PRQ-1482

1) The actual VDDP voltage range depends on the extended supply voltage ranges given in the general characteristics of the product.

10.3.3 Output driver

Table 23 Output driver

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output low voltage at maximum current	V_{OLmax}	–	–	1	V	*1)* I_{OL} ≤ I_{OLmax} 2.55 V ≤ V_{VDDP} ≤ 5.5 V	PRQ-1483
Output low voltage at nominal current	V_{OLnom}	–	–	0.4	V	*1)* I_{OL} ≤ I_{OLnom} 2.55 V ≤ V_{VDDP} ≤ 5.5 V	PRQ-1484
Output high voltage at maximum current	V_{OHmax}	V_{VDDP} - 1.0	–	–	V	*1)* I_{OH} ≤ I_{OHmax} 2.55 V ≤ V_{VDDP} ≤ 5.5 V	PRQ-1485
Output high voltage at nominal current	V_{OHnom}	V_{VDDP} - 0.4	–	–	V	*1)* I_{OH} ≤ I_{OHnom} 2.55 V ≤ V_{VDDP} ≤ 5.5 V	PRQ-1486
Output slope (strong driver, sharp edge), rise / fall time	t_{slpshp}	–	–	15	ns	20% / 80% of V_{VDDP} C_L ≤ 100 pF	PRQ-1487

(table continues...)

Table 23 (continued) Output driver

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output slope (strong driver, sharp edge), rise / fall time	t_{slpshp}	–	–	5	ns	20% / 80% of V_{VDDP} $C_L \leq 20$ pF	PRQ-1488
Output slope (medium driver), rise / fall time	t_{slpmed}	–	–	50	ns	20% / 80% of V_{VDDP} $C_L \leq 100$ pF	PRQ-1489
Output slope (medium driver), rise / fall time	t_{slpmed}	–	–	12	ns	20% / 80% of V_{VDDP} $C_L \leq 20$ pF	PRQ-1490

1) The actual VDDP voltage range depends on the extended supply voltage ranges given in the general characteristics of the product.

10.3.4 Current limits for output driver

Table 24 Current limits for output driver

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output current, strong driver	I_{OLHs5}	–	1.6	5	mA	*1)* $V_{VDDP} \geq 4.5$ V	PRQ-1491
Output current, medium driver	I_{OLHm5}	–	1	3	mA	*1)* $V_{VDDP} \geq 4.5$ V	PRQ-1492
Output current, weak driver	I_{OLHw5}	–	0.25	0.5	mA	*1)* $V_{VDDP} \geq 4.5$ V	PRQ-1493
Output current, strong driver	I_{OLHs3}	–	1	3	mA	*1) 2)* 2.55 V ≤ V_{VDDP} < 4.5 V	PRQ-1494
Output current, medium driver	I_{OLHm3}	–	0.8	1.8	mA	*1) 2)* 2.55 V ≤ V_{VDDP} < 4.5 V	PRQ-1495
Output current, weak driver	I_{OLHw3}	–	0.15	0.3	mA	*1) 2)* 2.55 V ≤ V_{VDDP} < 4.5 V	PRQ-1496

1) Typ. values: nominal output current (I_{OLnom}, I_{OHnom}).
Max. values: maximum output current (I_{OLmax}, I_{OHmax}).
Values are valid for both low-side and high-side currents.
Positive current flowing into the pin for I_{OL} and out of the pin for I_{OH}.

2) The actual VDDP voltage range depends on the extended supply voltage ranges given in the general characteristics of the product.

10.3.5 Leakage current and pin capacitance

Table 25 Leakage current and pin capacitance

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Leakage current PI	I_{LKPI}	-400	–	+400	nA	$T_J \leq 85°C$ $0\ V < V_{IN} < V_{VDDP}$	PRQ-1497
Leakage current PI	$I_{LKPIext}$	-1	–	+1	µA	$0\ V < V_{IN} < V_{VDDP}$	PRQ-1498
Leakage current PB	I_{LKPB}	-5	–	+5	µA	$T_J \leq 85°C$ $0\ V < V_{IN} < V_{VDDP}$	PRQ-1499
Leakage current PB	$I_{LKPBext}$	-22	–	+22	µA	$0\ V < V_{IN} < V_{VDDP}$	PRQ-1500
Pin capacitance	C_P	–	–	10	pF	$f > 1$ MHz	PRQ-1501

11 LIN transceiver (LINTRX)

11.1 Features overview

The LIN transceiver (LINTRX) for the Local Interconnect Network (LIN) operates as a bus driver between the protocol controller and the physical network.

The LINTRX is compliant with:

- ISO17987 standard, backward-compatible with LIN1.3, LIN2.0, LIN 2.1 and LIN2.2
- SAE J2602

The LINTRX provides following features:

- Operating modes
  - Normal mode
  - Receive-only mode
  - Wake-capable mode
  - Off mode
- Slope modes
  - Normal slope for up to 20 kBit/s
  - Fast slope for up to 62.5 kBit/s
  - Flash mode for 115 kBit/s
- Protection
  - Overtemperature shutdown
  - Undervoltage shutdown
  - Overcurrent protection
  - TXD timeout

11.2 Block diagram

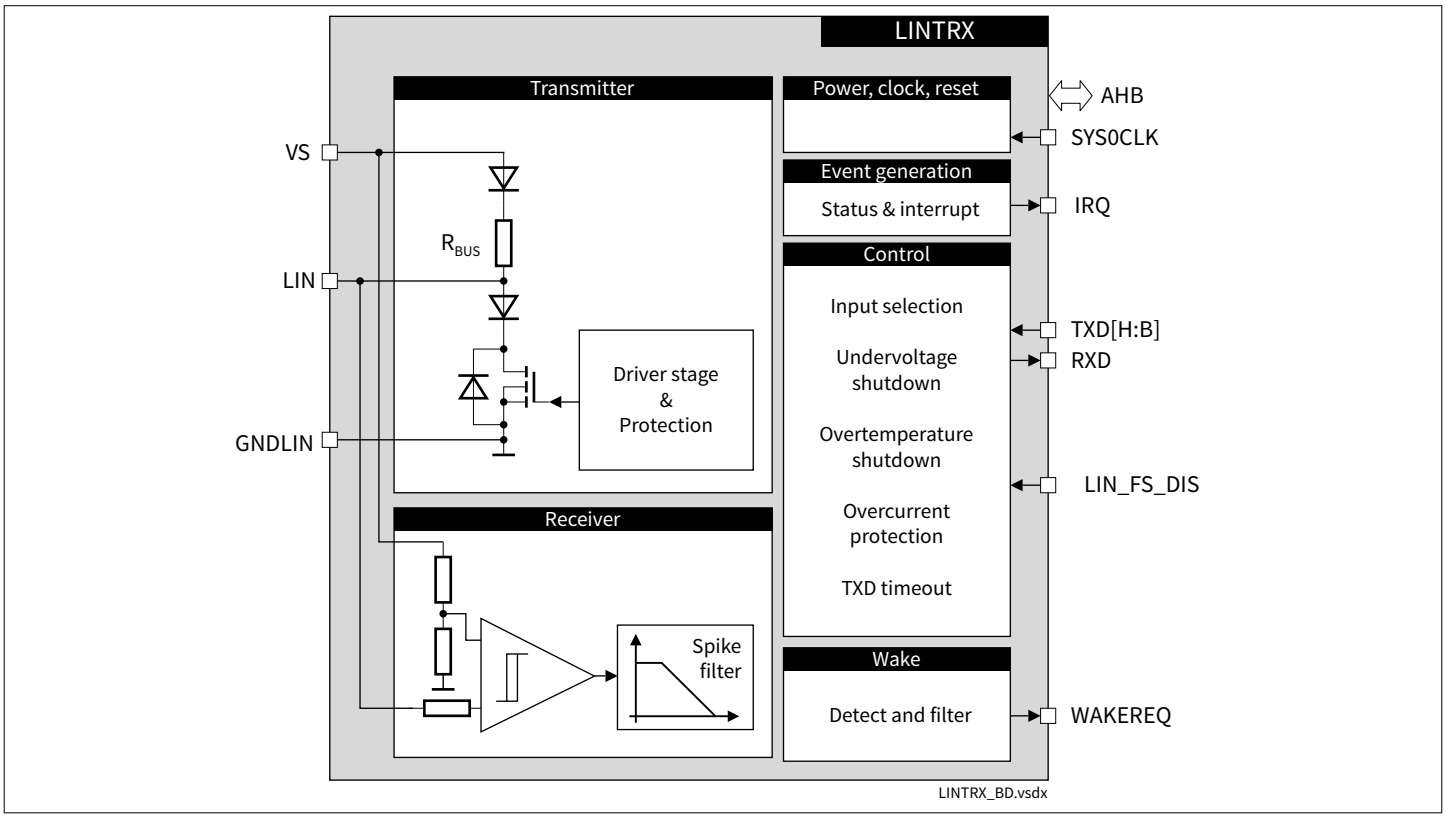

Figure 16 LINTRX block diagram

11.3 Electrical characteristics LINTRX

11.3.1 Failsafe features

Table 26 Failsafe features

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Undervoltage detection threshold for VS	UV_{VS}	–	5.0	5.5	V	–	PRQ-1387
Undervoltage detection threshold hysteresis	UV_{HYS}	–	300	–	mV	–	PRQ-1388

11.3.2 General timing characteristics

Table 27 General timing characteristics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Undervoltage filter time	$t_{S,Filter}$	1	–	10	µs	–	PRQ-1389
Undervoltage recovery time	$t_{S,recovery}$	–	–	20	µs	–	PRQ-1390
TxD timeout time	t_{TxD}	8	–	28	ms	–	PRQ-1391
TxD timeout recovery time	$t_{TO,REC}$	–	–	20	µs	–	PRQ-1392
Wake-up dominant pulse width	$t_{WK,bus}$	30	–	150	µs	Including both analog and digital filter times	PRQ-1393

11.3.3 LIN bus interface

Table 28 LIN bus interface

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Bus short circuit current	I_{LIN_SC}	40	85	150	mA	$V_{LIN} = V_S$	PRQ-1394
Leakage current driver off and bus dominant	$I_{BUS\_PAS\_dom}$	-1	-0.5	–	mA	V_{LIN} = 0 V	PRQ-1395
Leakage current driver off and bus recessive	$I_{BUS\_PAS\_rec}$	–	1	20	µA	V_S = 5.5 V V_{LIN} = 18 V	PRQ-1396
Leakage current loss of ground	$I_{BUS\_NO\_GND}$	-1	-0.5	1	mA	V_S = 0 V V_{LIN} = -12V	PRQ-1397
Leakage current loss of battery	$I_{BUS\_NO\_BAT}$	–	1	20	µA	V_S = 0 V 0 V < V_{LIN} < 18 V	PRQ-1398
Transceiver input pin capacitance	C_{LIN_IN}	–	15	30	pF	–	PRQ-1400
Network pull-up resistance (responder node) for 30 participants	$R_{BUS\_responder\ 30}$	27.66	33	40	kΩ	1)	PRQ-1544

1) Pull-up resistor present in Normal mode, also present in Sleep mode.

11.3.4 LIN transmitter

Table 29 LIN transmitter

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Bus recessive output voltage	V_{BUS_ro}	0.8 × V_S	–	V_S	V	TXD input high; LIN pin unconnected; 5.5 V < V_S < 18 V	PRQ-1401
LIN diode voltage drop	V_{Ser_Diode}	0.4	0.7	1.0	V	TXD input high; I_{Ser_Diode} = 75 µA	PRQ-1402
Bus dominant output voltage	$V_{BUS\_dom\_low}$	–	–	0.2 × V_S	V	TXD input low; R_L = 500 Ω; 7.3 V ≤ V_S ≤ 10 V	PRQ-1403
Bus dominant output voltage	$V_{BUS\_dom\_med}$	–	–	2.1	V	TXD input low; R_L = 500 Ω; 10 V < V_S ≤ 18 V	PRQ-1404
Bus dominant output voltage	$V_{BUS\_dom\_deep}$	–	–	1.5	V	TXD input low; R_L = 500 Ω; 5.5 V < V_S ≤ 7.3 V	PRQ-1405

11.3.5 LIN receiver

Table 30 LIN receiver

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Receiver threshold voltage, recessive to dominant edge	V_{th_dom}	0.4 × V_S	0.44 × V_S	–	V	Dominant state	PRQ-1406
Receiver threshold voltage, dominant to recessive edge	V_{th_rec}	–	0.56 × V_S	0.6 × V_S	V	Recessive state	PRQ-1407
Receiver hysteresis	V_{HYS}	0.07 × V_S	0.12 × V_S	0.175 × V_S	V	V_{HYS} = V_{th_rec} - V_{th_dom}	PRQ-1408
Receiver dominant state	V_{BUSdom}	-40	–	0.4 × V_S	V	–	PRQ-1409
Receiver recessive state	V_{BUSrec}	0.6 × V_S	–	40	V	–	PRQ-1410
Receiver center voltage	V_{BUS_CNT}	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	V_{BUS_CNT} = (V_{th_dom} + V_{th_rec}) / 2	PRQ-1411
Wake-up threshold voltage	V_{th_wk}	0.4 × V_S	0.5 × V_S	0.6 × V_S	V	Device set to wake mode	PRQ-1412

11.3.6 Dynamical parameter, LIN receiver and transmitter

Table 31 Dynamical parameter, LIN receiver and transmitter

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Propagation delay BUS to RxDLIN ("dominant" to "low")	$t_{Rec\_PD\_f}$	1	3.5	6	µs	Transmitter is set to normal slope mode V_S = 5.5 V ... 18 V 1)	PRQ-1413
Propagation delay BUSx to RxDLIN ("recessive" to "high")	$t_{Rec\_PD\_r}$	1	3.5	6	µs	Transmitter is set to normal slope mode V_S = 5.5 V ... 18 V 1)	PRQ-1414
Receiver propagation delay symmetry in normal slope mode	$t_{rx\_pd\_sym}$	-2	–	2	µs	Transmitter is set to normal slope mode V_S = 5.5 V ... 18 V $t_{rx\_LIN\_pd\_sym} = t_{rx\_LIN\_pdf} - t_{rx\_LIN\_pdr}$ 1)	PRQ-1415
Duty cycle D1 (20 kBit/s, 7 V < VS < 18 V)	*D1*	0.396	–	–		Transmitter is set to normal slope mode $TH_{Rec(max)} = 0.744 \times V_S$, $TH_{Dom(max)} = 0.581 \times V_S$, V_S = 7.0 V ... 18 V, t_{Bit} = 50 µs, $D1 = t_{bus\_rec(min)} / 2 \times t_{BIT}$ 2)	PRQ-1416
Duty cycle D1 (20 kBit/s, 5.5 V < VS < 7 V)	$D1_{low\_VS}$	0.396	–	–		Transmitter is set to normal slope mode $TH_{Rec(max)} = 0.665 \times V_S$ $TH_{Dom(max)} = 0.499 \times V_S$ V_S = 5.5 V ... 7.0 V t_{Bit} = 50 µs $D1 = t_{bus\_rec(min)} / 2 \times t_{Bit}$ 2)	PRQ-1417
Duty cycle D2 (20 kBit/s, 7.6 V < VS < 18 V)	*D2*	–	–	0.581		Transmitter is set to normal slope mode $TH_{Rec(min)} = 0.422 \times V_S$; $TH_{Dom(min)} = 0.284 \times V_S$; V_S = 7.6 V ... 18 V; t_{Bit} = 50 µs; $D2 = t_{bus\_rec(max)} / 2 \times t_{Bit}$ 2)	PRQ-1418

(table continues...)

Table 31 (continued) Dynamical parameter, LIN receiver and transmitter

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Duty cycle D2 (20 kBit/s, 6.1 V < VS < 7 V)	$D2_{low\_VS}$	–	–	0.581		Transmitter is set to normal slope mode $TH_{Rec(min)} = 0.496 \times V_S$ $TH_{Dom(min)} = 0.361 \times V_S$ $V_S = 6.1$ V ... 7.6 V $t_{Bit} = 50$ µs $D2 = t_{bus\_rec(max)} / 2 \times t_{Bit}$ 2)	PRQ-1419
Duty cycle D3 (10.4 kBit/s, 7 V < VS < 18 V)	$D3$	0.417	–	–		Transmitter is set to normal slope mode $TH_{Rec(max)} = 0.778 \times V_S$ $TH_{Dom(max)} = 0.616 \times V_S$ $V_S = 7.0$ V ... 18 V $t_{Bit} = 96$ µs $D3 = t_{bus\_rec(min)} / 2 \times t_{Bit}$ 2)	PRQ-1420
Duty cycle D3 (10.4 kBit/s, 5.5 V < VS < 7 V)	$D3_{low\_VS}$	0.417	–	–		Transmitter is set to normal slope mode $TH_{Rec(max)} = 0.665 \times V_S$ $TH_{Dom(max)} = 0.499 \times V_S$ $V_S = 5.5$ V ... 7.0 V $t_{Bit} = 96$ µs $D3 = t_{bus\_rec(min)} / 2 \times t_{Bit}$ 2)	PRQ-1421
Duty cycle D4 (10.4 kBit/s, 7.6 V < VS < 18 V)	$D4$	–	–	0.59		Transmitter is set to normal slope mode $TH_{Rec(min)} = 0.389 \times V_S$ $TH_{Dom(min)} = 0.251 \times V_S$ $V_S = 7.6$ V ... 18 V $t_{Bit} = 96$ µs $D4 = t_{bus\_rec(max)} / 2 \times t_{Bit}$ 2)	PRQ-1422

(table continues...)

Table 31 (continued) Dynamical parameter, LIN receiver and transmitter

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Duty cycle D4 (10.4 kBit/s, 6.1 V < VS < 7 V)	$D4_{low\_VS}$	–	–	0.59		Transmitter is set to normal slope mode $TH_{Rec(min)} = 0.496 \times V_S$ $TH_{Dom(min)} = 0.361 \times V_S$ $V_S = 6.1$ V ... 7.6 V $t_{Bit} = 96$ µs $D4 = t_{bus\_rec(max)} / 2 \times t_{Bit}$ 2)	PRQ-1423
Duty cycle D5 (62.5 kBit/s, 7 V < VS < 18 V)	$D5$	0.33	–	–		Transmitter is set to fast slope mode $TH_{Rec(max)} = 0.744 \times V_S$ $TH_{Dom(max)} = 0.581 \times V_S$ $V_S = 7.0$ V ... 18 V $t_{Bit} = 50$ µs $D5 = t_{bus\_rec(min)} / 2 \times t_{Bit}$ 3)	PRQ-1424
Duty cycle D5 (62.5 kBit/s, 5.5 V < VS < 7 V)	$D5_{low\_VS}$	0.33	–	–		Transmitter is set to fast slope mode $TH_{Rec(max)} = 0.665 \times V_S$ $TH_{Dom(max)} = 0.499 \times V_S$ $V_S = 5.5$ V ... 7.0 V $t_{Bit} = 50$ µs $D5 = t_{bus\_rec(min)} / 2 \times t_{Bit}$ 3)	PRQ-1425
Duty cycle D6 (62.6 kBit/s, 7.6 V < VS < 18 V)	$D6$	–	–	0.63		Transmitter is set to fast slope mode $TH_{Rec(min)} = 0.422 \times V_S$ $TH_{Dom(min)} = 0.284 \times V_S$ $V_S = 7.6$ V ... 18 V $t_{Bit} = 50$ µs $D6 = t_{bus\_rec(max)} / 2 \times t_{Bit}$ 3)	PRQ-1426

(table continues...)

Table 31 (continued) Dynamical parameter, LIN receiver and transmitter

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Duty cycle D6 (62.5 kBit/s, 6.1 V < VS < 7 V)	$D6_{low\_VS}$	–	–	0.63		Transmitter is set to fast slope mode $TH_{Rec(min)} = 0.496 \times V_S$ $TH_{Dom(min)} = 0.361 \times V_S$ $V_S = 6.1\ V \ldots 7.6\ V$ $t_{Bit} = 50\ \mu s$ $D6 = t_{bus\_rec(max)} / 2 \times t_{Bit}$ 3)	PRQ-1427
Duty cycle D7 (115 kBit/s, VS = 13.5 V)	$D7$	0.356	–	0.5		Transmitter is set to flash slope mode $TH_{Rec(max)} = 0.6 \times V_S$ $TH_{Dom(max)} = 0.4 \times V_S$ $V_S = 13.5\ V$ $T_j = 25°C$ $t_{Bit} = 8.7\ \mu s$ $D7 = t_{bus\_rec(min)} / 2 \times t_{BIT}$ 4)	PRQ-1428
Wake-up spike filter time	$t_{WK\_ana,bus}$	3	–	15	µs	$V_S = 5.5\ V \ldots 18\ V$	PRQ-1430
Propagation delay BUSx to RxDLIN ("recessive" to "high") in fast slope mode	$t_{rx\_LIN\_fsm\_pdr}$	1	3.5	6	µs	Transmitter is set to fast slope mode $V_S = 5.5\ V \ldots 18\ V$ 1)	PRQ-1545
Propagation delay BUS to RxDLIN ("dominant" to "low") in fast slope mode	$t_{rx\_LIN\_fsm\_pdf}$	1	3.5	6	µs	Transmitter is set to fast slope mode $V_S = 5.5\ V \ldots 18\ V$ 1)	PRQ-1546
Receiver propagation delay symmetry in fast slope mode	$t_{rx\_LIN\_pd\_fsm\_sym}$	-800	–	800	ns	Transmitter is set to fast slope mode $V_S = 5.5\ V \ldots 18\ V$ $t_{rx\_LIN\_pd\_fsm\_sym} = t_{rx\_LIN\_fsm\_pdf} - t_{rx\_LIN\_fsm\_pdr}$ 1)	PRQ-1547
Propagation delay BUSx to RxDLIN ("recessive" to "high") in flash slope mode	$t_{rx\_LIN\_flsm\_pdr}$	1	3.5	6	µs	Transmitter is set to flash slope mode $V_S = 13.5\ V$ $T_j = 25°C$ 1)	PRQ-1548

(table continues...)

Table 31 (continued) Dynamical parameter, LIN receiver and transmitter

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Propagation delay BUS to RxDLIN ("dominant" to "low") in flash slope mode	$t_{rx\_LIN\_flsm\_pdf}$	1	3.5	6	µs	Transmitter is set to flash slope mode V_S = 13.5 V T_j = 25°C *1)*	PRQ-1549
Receiver propagation delay symmetry in flash slope mode	$t_{rx\_LIN\_pd\_flsm\_sym}$	-450	–	200	ns	Transmitter is set to flash slope mode V_S = 13.5 V T_j = 25°C $t_{rx\_LIN\_pd\_flsm\_sym}$ = $t_{rx\_LIN\_flsm\_pdf}$ - $t_{rx\_LIN\_flsm\_pdr}$ *1) 4)*	PRQ-1550

1) Refer to "Receiver propagation delay diagram"
2) Load 1: C_{BUS} / R_L = 1 nF / 1 kΩ
Load 2: C_{BUS} / R_L = 6.8 nF / 660 Ω
Load 3: C_{BUS} / R_L = 10 nF / 500 Ω
3) Load: C_{BUS} / R_L = 1 nF / 1 kΩ
4) Load: C_{BUS} / R_L = 220 pF / 500 Ω

11.3.7 Thermal characteristics

Table 32 Thermal characteristics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Thermal shutdown temperature, rising	T_{TSD}	175	185	195	°C	–	PRQ-1431
Thermal shutdown hysteresis	ΔT	5	10	20	°C	–	PRQ-1432

11.3.8 Duty cycle timing diagram and receiver propagation delay

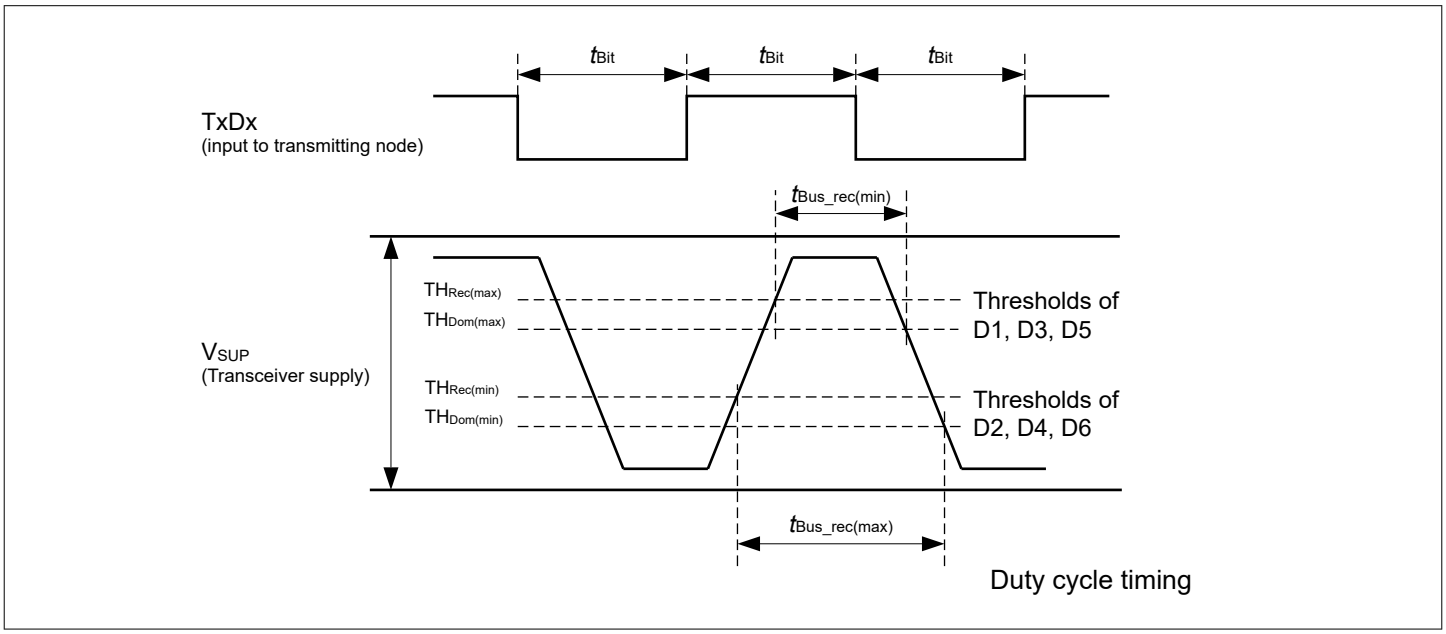

Figure 17 Duty cycle timing diagram

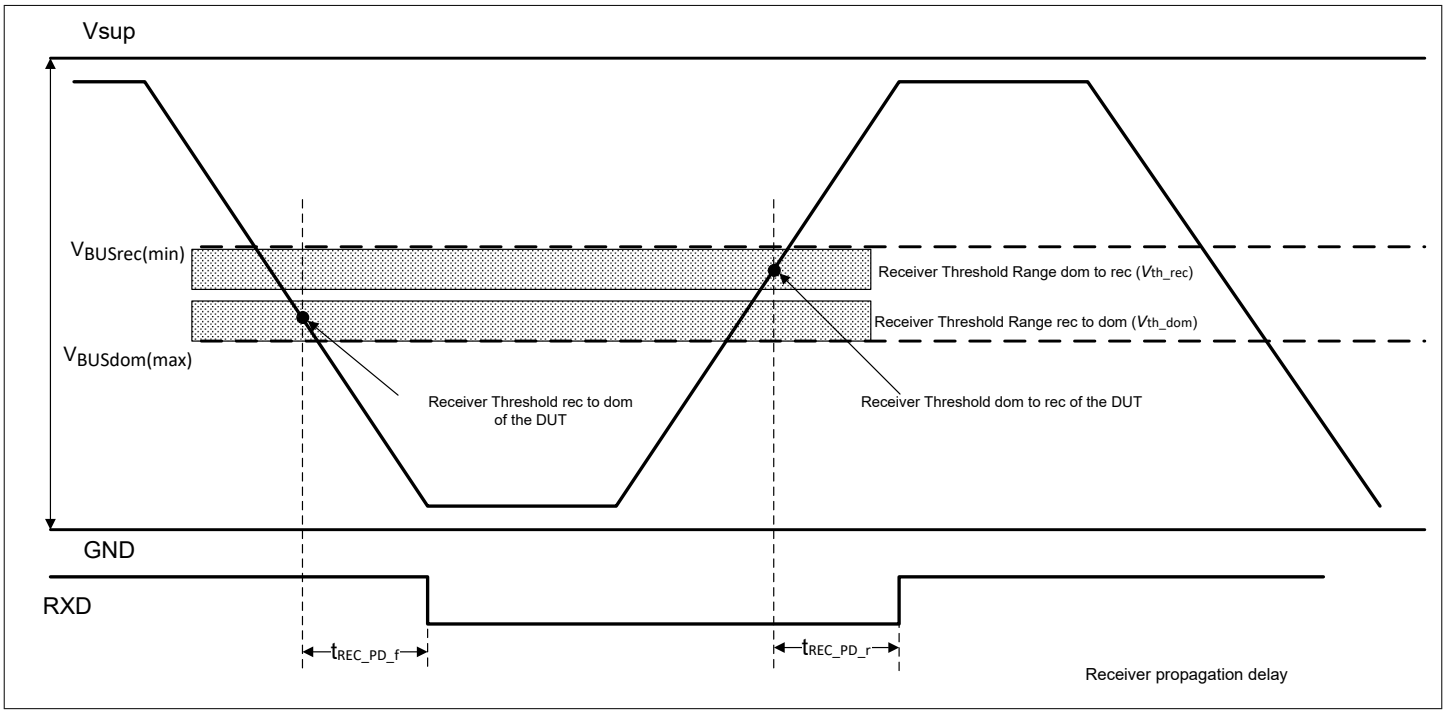

Figure 18 Receiver propagation delay diagram

12 LIN universal asynchronous receiver transmitter (LINUART)

12.1 Features overview

The LINUART is a UART based communication interface. The LINUART can be connected to a LIN transceiver or to port pins.

The LINUART provides following features:

- Input stage with a programmable filter and a selection for external transmit trigger
- Baudrate generator with fractional divider
- UART based receive and transmit control with collision detection and loop delay measurement
- UART based receive and transmit buffer
- LIN protocol support with header generation and detection, autobaud adjustment and flow control
- Output stage with control options for the output signal
- Event generation with status and interrupt request

12.2 Block diagram

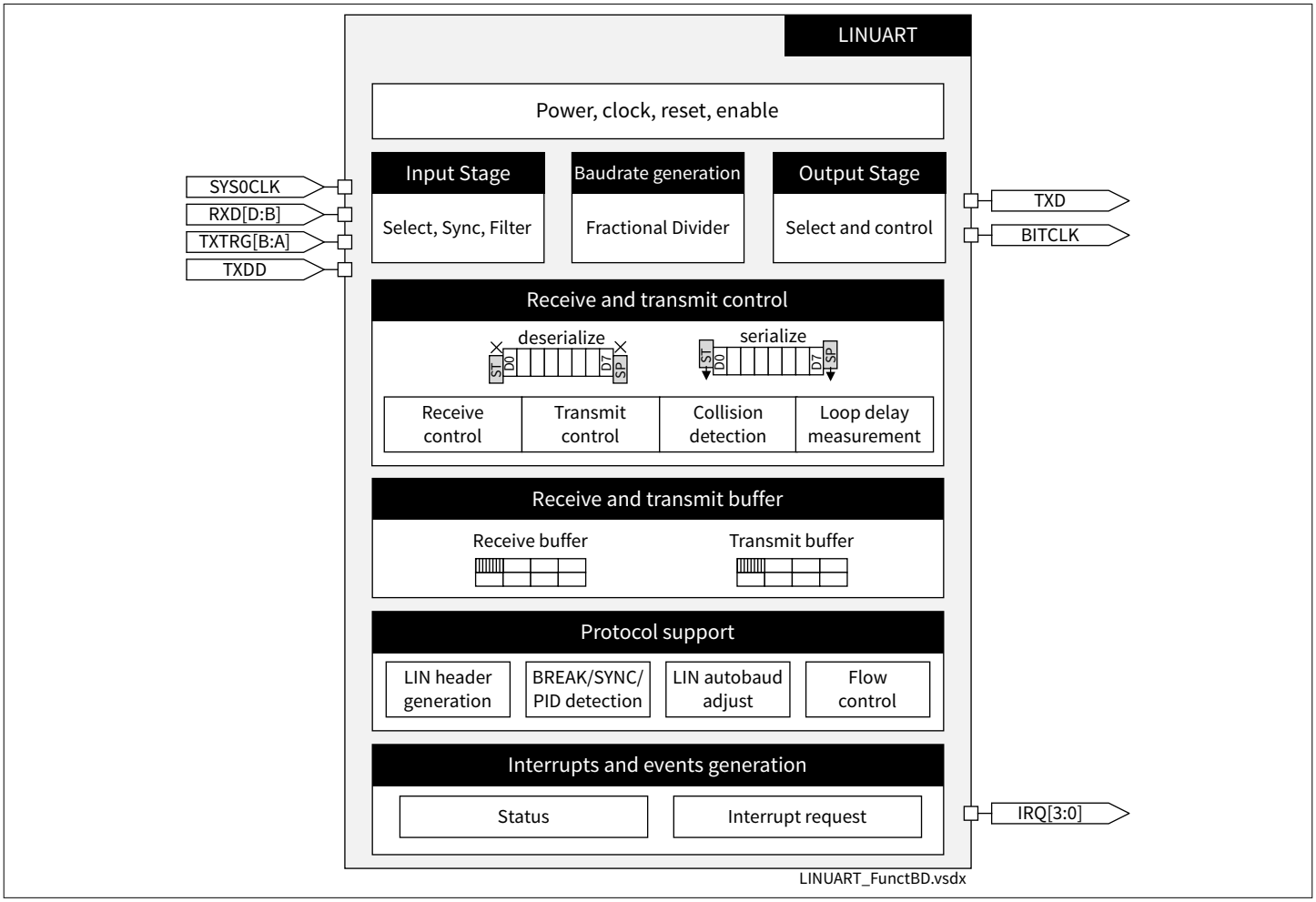

Figure 19 LINUART block diagram

13 High-speed synchronous serial interface (SSC)

13.1 Features overview

The high-speed synchronous serial interfaces (SSC) supports both full-duplex and half-duplex serial synchronous communication.

The SSC provides following features:

- Commander and responder mode operation
  - Full-duplex or half-duplex operation
- Transmit and receive buffered
- Flexible data format
  - Programmable number of data bits: 2 to 64 bits
  - Programmable shift direction: least significant bit (LSB) or most significant bit (MSB) shift first
  - Programmable clock polarity: idle low or high state for the shift clock
  - Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- Variable baud rate up to 10 MBaud (responder mode) or 20 MBaud (commander mode)
- Chip Select (commander) for 1 to 4 responders
- Chip Select (responder)
- Compatible with serial peripheral interface (SPI)
- Interrupt generation:
  - Interrupt on a transmitter empty condition
  - Interrupt on a receiver full condition
  - Interrupt on an error condition (receive, phase, baud rate, transmit error)

13.2 Block diagram

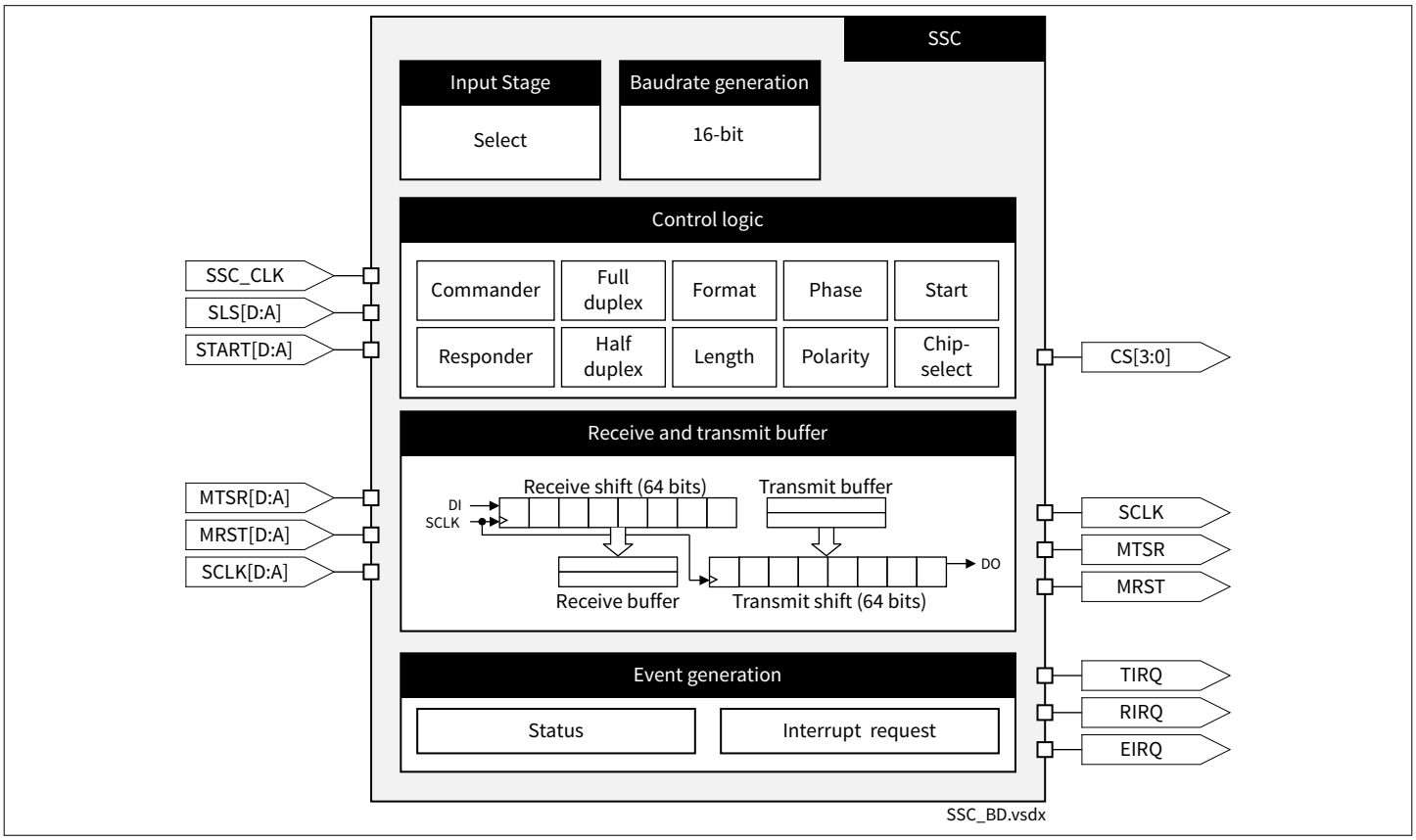

Figure 20 SSC block diagram

13.3 SSC timing diagram

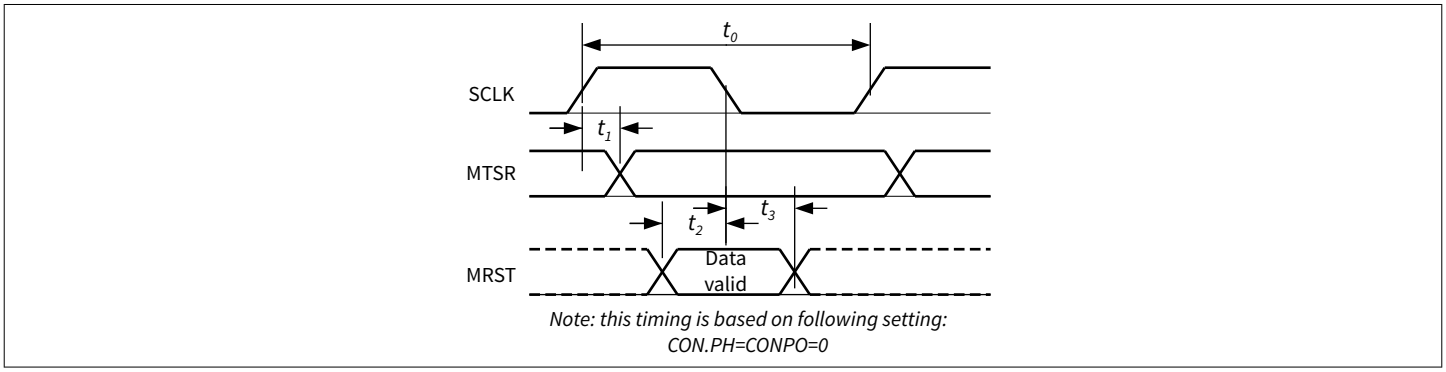

Figure 21 SSC commander timing

13.4 Electrical characteristics SSC

Table 33 SSC commander mode timing

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SCLK clock period	t_0	$2 \times T_{SSC\_CLK}$	–	–	ns	$V_{VDDP} > 2.7$ V $C_L = 50$ pF	PRQ-1454
MTSR delay from SCLK	t_1	10	–	–	ns	$V_{VDDP} > 2.7$ V $C_L = 50$ pF	PRQ-1455
MRST setup to SCLK	t_2	10	–	–	ns	$V_{VDDP} > 2.7$ V $C_L = 50$ pF	PRQ-1456
MRST hold from SCLK	t_3	15	–	–	ns	$V_{VDDP} > 2.7$ V $C_L = 50$ pF	PRQ-1457

14 General purpose timer units (GPT12)

14.1 Features overview

The general purpose timer (GPT12) consists of five 16-bit timers, which are grouped into two timer blocks GPT1 and GPT2. The two timer blocks can be used independently for various use cases like timing, event counting, pulse width measurement, pulse generation, frequency multiplication, and other purposes.

The GPT1 provides following features:

- A maximum resolution of module clock divided by 4
- 3 independent timers/counters
- Timers/counters can be concatenated
- 4 operating modes:
  - Timer mode
  - Gated timer mode
  - Counter mode
  - Incremental interface mode
- Reload and capture functionality
- The GPT1 has multiple input options
- The GPT1 has one output as peripheral interconnection and an IRQ

The GPT2 provides following features:

- A maximum resolution of module clock divided by 2
- 2 independent timers/counters
- Timers/counters can be concatenated
- 3 operating modes:
  - Timer mode
  - Gated timer mode
  - Counter mode
- Extended capture and reload functions
- The GPT2 has multiple input options
- The GPT2 has one output as peripheral interconnection and an IRQ

14.2 Block diagram

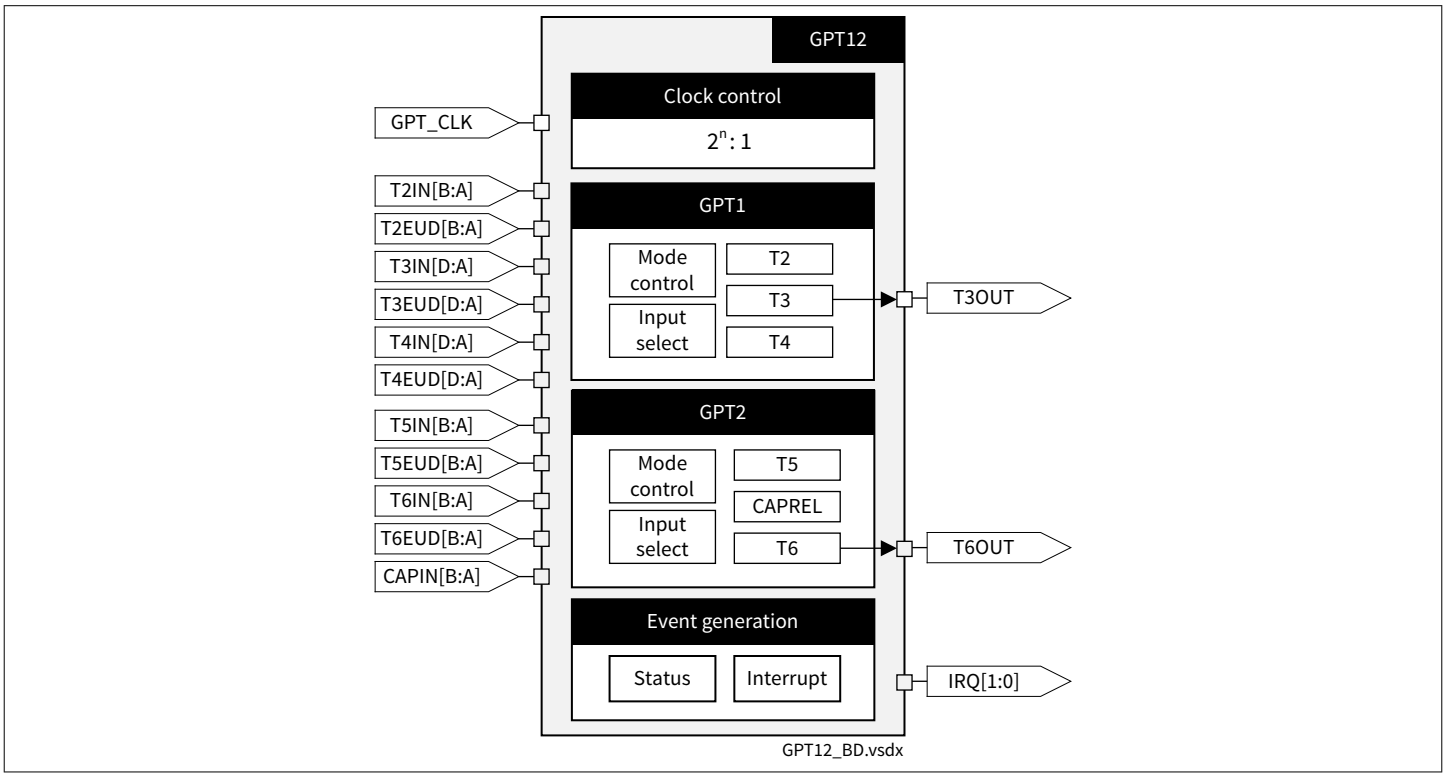

Figure 22 GPT12 block diagram

15 Capture/compare unit 7 (CCU7)

15.1 Features overview

The capture/compare unit 7 (CCU7) is a high-resolution 16-bit timer unit for motor control.
The CCU7 provides following features:

- Five 16-bit timers T12, T13, T14, T15, and T16
- Multi channel mode for block commutation
- Programmable Hall-sensor pattern detection
- Fast emergency stop without CPU load via external signal

The timer T12 provides following features:

- One time base with three channels
- Each channel has two programmable compares for symmetrical and asymmetrical PWM generation
- Can be used with the dead-time control unit
- Shadow mechanism for coherent update of PWM generation related registers
- Single-shot mode
- Start can be controlled by external events
- Count external events
- Multiple input options
- Multiple outputs as peripheral interconnection and IRQ

The timers T13, T14, T15, and T16 provide following features:

- Independent time bases for each timer with one programmable compare channel
- Can be used with the dead-time control unit (except for T13)
- Shadow mechanism for coherent update of PWM generation related registers
- Single-shot mode
- Start can be controlled by external events and can be synchronized to each other and to T12
- Count external events

15.2 Block diagram

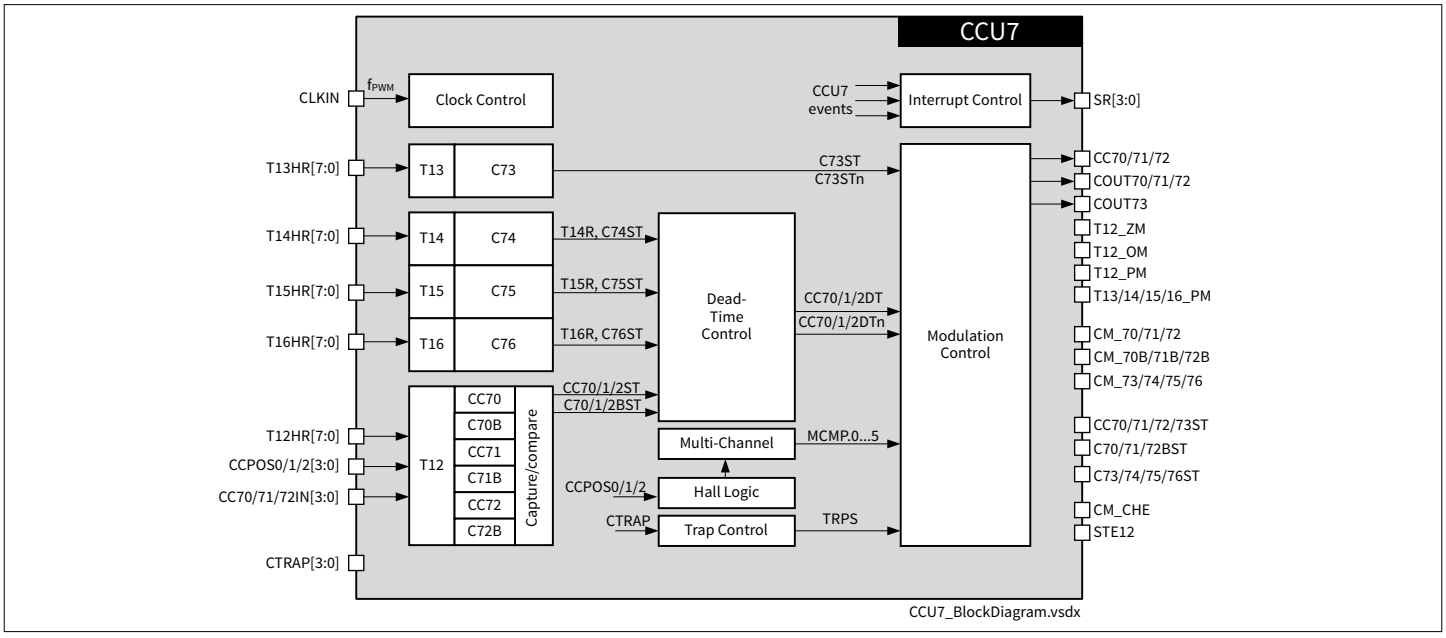

Figure 23 CCU7 block diagram

16 Current sense amplifier (CSA)

16.1 Features overview

The current sense amplifier (CSA) allows current measurements with an external shunt resistor in low-side configuration.

The CSA provides following features:

- Amplification of a near-ground differential input voltage to a single-ended output voltage
- Selectable uni-directional or bi-directional current sense mode (V_{CSO_OFF} = typ. 0.5 V, 2 V)
- Programmable gain settings (G = typ. 11.34, 14.65, 20.65, 25.1, 35.1, 50.1)
- Programmable shunt overcurrent threshold
- Programmable shunt overcurrent filter time
- Short settling time

16.2 Block diagram

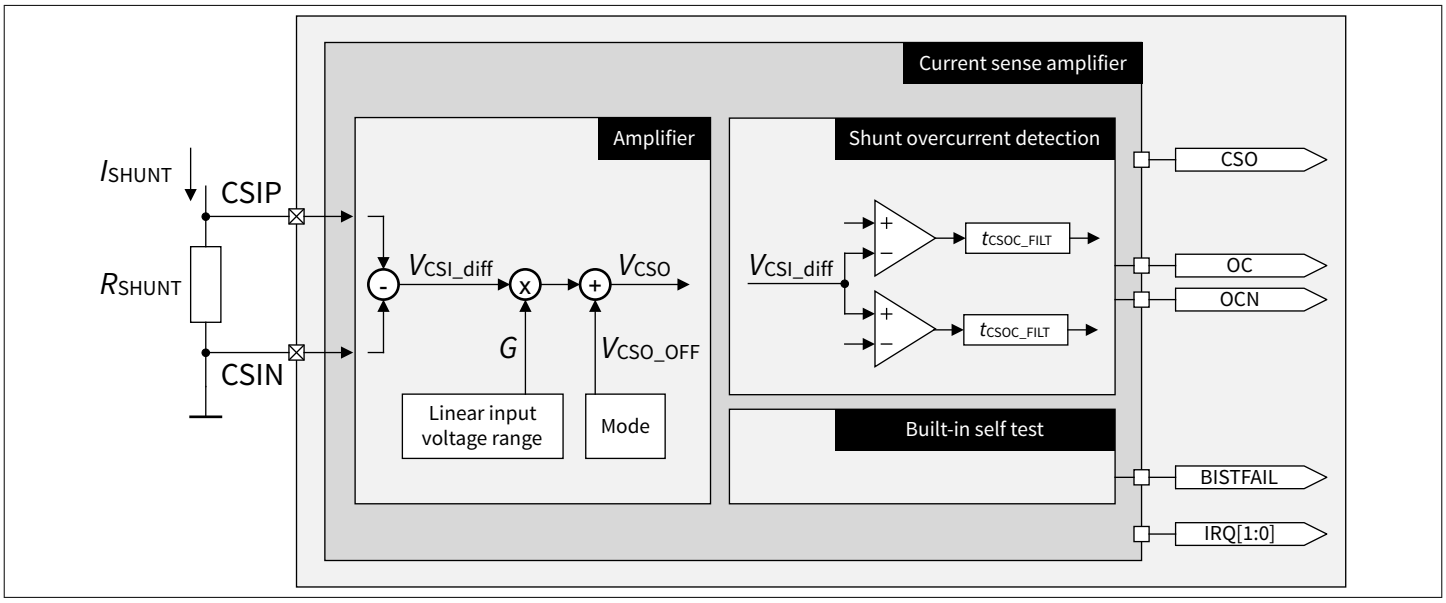

Figure 24 CSA block diagram

16.3 Electrical characteristics CSA

16.3.1 Current sense amplifier

Table 34 Current sense amplifier

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Operating common mode input voltage range referred to GND (CSIP - GND) or (CSIN - GND)	V_{CSIx_CM}	-2	–	2	V	–	PRQ-1353

(table continues...)

Table 34 (continued) Current sense amplifier

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Single-ended linear output voltage range	V_{CSO}	0.5	–	3.5	V	–	PRQ-1608
Input offset voltage	V_{CSA_OS}	-1.3	0	+1.3	mV	–	PRQ-1354
Output voltage offset accuracy	A_{CSO_OFF}	-2.5	–	+2.5	%	Refers to the nominal value of the output voltage offset selected by the programmable parameter V_{CSO_OFF}	PRQ-1597
Gain accuracy	A_{GAIN}	-1	–	+1	%	Refers to the nominal value of the gain selected by the programmable parameter V_{CSI_lin}	PRQ-1355
Gain drift	G_{DRIFT}	-0.1	–	+0.1	%	Refers to the nominal value of the gain selected by the programmable parameter V_{CSI_lin}	PRQ-1356
Gain temperature drift	ΔG_{TD}	-50	–	+50	ppm/K	Refers to the nominal value of the gain selected by the programmable parameter V_{CSI_lin}	PRQ-1357
Linearity error	E_{LIN}	-15		15	mV	Maximum deviation from best-fit line	PRQ-1596
Input resistance	R_{CSIx}	1.6	2	2.4	kΩ	–	PRQ-1531
Gain test voltage	$V_{CSI\_gain\_test}$	22	25	28	mV	–	PRQ-1532
CSA settling time to 98%	t_{CSA_SET}	–	1000	1500	ns	–	PRQ-1358

16.3.2 Shunt overcurrent detection

Table 35 Shunt overcurrent detection

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Shunt positive overcurrent threshold accuracy	A_{CSOCP}	-2.5	–	+2.5	%	Refers to the nominal value of the programmable parameter k_{CSOC}	PRQ-1359
Shunt negative overcurrent threshold accuracy	A_{CSOCN}	-4	–	+4	%	Refers to the nominal value of the programmable parameter k_{CSOC}	PRQ-1595
Shunt overcurrent filter time accuracy	A_{CSOC_FILT}	-20	–	+20	%	Refers to the nominal value of the programmable parameter t_{CSOC_FILT}	PRQ-1360

17 Analog to digital converter (ADC12)

17.1 Features overview

The ADC12 is a successive approximation analog to digital converter which can be used for analog signal measurement optimized for BLDC motor control. It has a deterministic behavior regarding to the sample event and conversion timing, as well as for a sequence of conversions. The ADC12 operates autonomously in the background without the need for real-time critical interaction with the MCU subsystem.

The ADC12 provides following features:

- ADC kernel performance:
  - 12-bit resolution for all analog inputs
  - High accuracy of typ. 0.3% of the input range (*ACC*)
  - Fast sampling time (t_{samp_MV}, t_{samp_HV}, t_{samp_SHx})
  - Fast total conversion time (typ. 850 ns for a 12-bit value)
- Analog inputs ANx:
  - High-voltage input range from 0 V to 29 V
  - Medium-voltage input range from 0 V to 4 V resp. 5 V
  - Low-voltage input range from 0 V to 2.44 V
- Sequencer control
  - Trigger logic for deterministic control of complex conversion sequences
  - Sequencer for up to four independent sequences with up to four digital channels
- Channel control
  - Channel configuration to assign analog inputs to one or more of 16 possible digital channels
  - Channel class for programmable conversion timing
- Result generation
  - Each analog input has a programmable calibration setting
  - Each digital channel has its own result register
  - Up to four digital comparators with 8-bit upper/lower thresholds
  - Up to four first-order IIR filters
- The ADC12 has multiple input options
- The ADC12 has multiple outputs as peripheral interconnection and IRQ

17.2 Block diagram

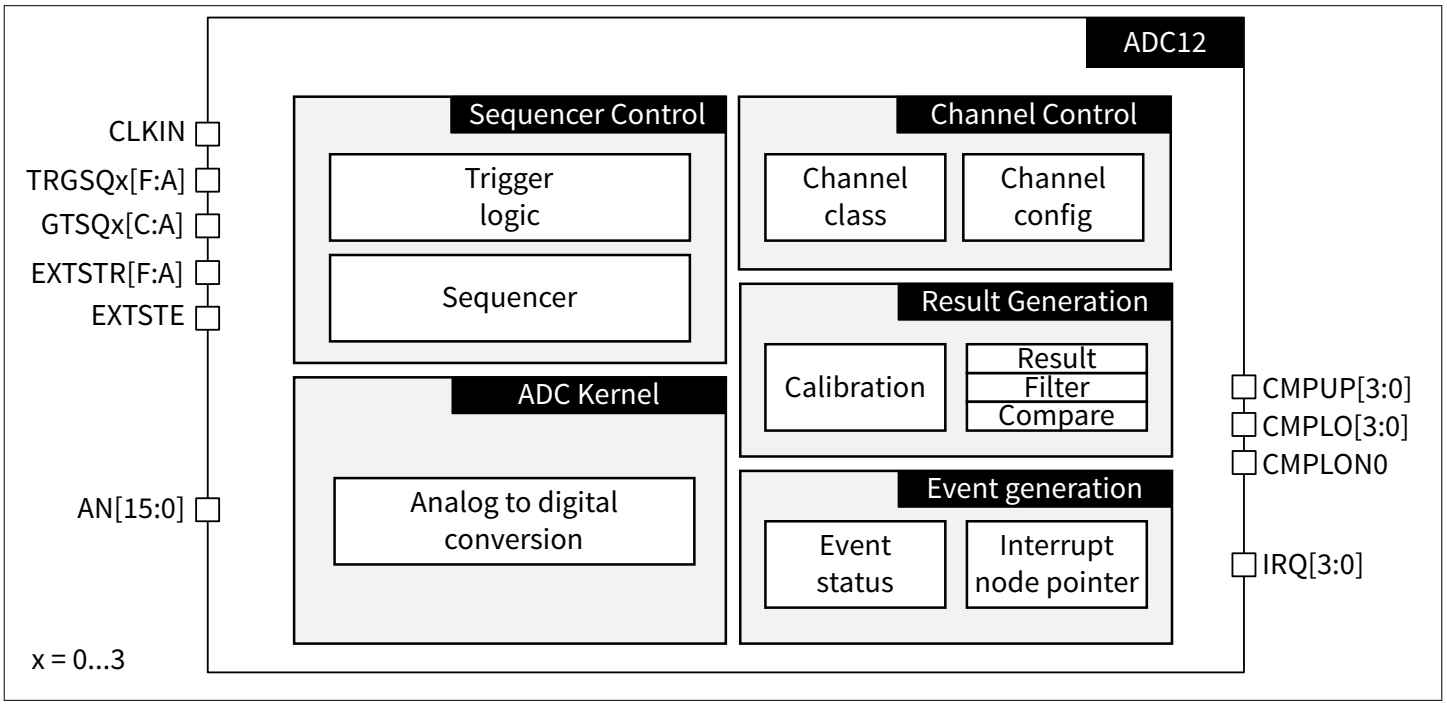

Figure 25 ADC12 block diagram

17.3 Electrical characteristics ADC12

17.3.1 Timing

Table 36 Timing

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Kernel clock	f_{kernel}	20	–	50	MHz	ADC module clock divider to be programmed accordingly	PRQ-1237
Sample time HV input	t_{samp_HV}	200	–	–	ns	Sample time control to be programmed accordingly	PRQ-1238
Sample time SHx input	t_{samp_SHx}	1000	–	–	ns	Sample time control to be programmed accordingly	PRQ-1239
Sample time MV input	t_{samp_MV}	200	–	–	ns	Sample time control to be programmed accordingly	PRQ-1240

17.3.2 Performance

Table 37 Performance

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Differential nonlinearity	*DNL*	-0.999	–	2.5	LSB12	Input referred No missing codes	PRQ-1243
RMS noise	*RMS*	–	–	2.3	LSB12	Input referred 1 sigma value	PRQ-1244
Accuracy for input voltage range 1	*ACC1*	-16	–	+16	LSB12	Input referred $0 \le V_{IN} \le 30\%$ FSR	PRQ-1606
Accuracy for input voltage range 2	*ACC2*	-20	–	+20	LSB12	Input referred 30% FSR $< V_{IN} \le 50\%$ FSR	PRQ-1607
Accuracy for input voltage range 3	*ACC3*	-30	–	+30	LSB12	Input referred 50% FSR $< V_{IN} \le$ FSR	PRQ-1245

18 Bridge driver (BDRV)

18.1 Features overview

The bridge driver (BDRV) provides floating gate drivers to control external normal-level n-channel MOSFETs arranged in half bridges for motor control applications.

The BDRV provides following features:

- Control signals are selectable from multiple sources
- Current-driven output stages with programmable gate current profile
- Timing measurements of on/off delays and on/off slope durations
- Automatic detection of the active MOSFET
- Programmable cross-conduction protection time
- Shoot-through protection
- Safe switch-off path to switch off the BDRV in a defined way in case of faults
- Passive pull-down mode to keep MOSFETs off if the BDRV is disabled
- 2-stage charge pump for low-voltage operation and static MOSFET gate control
- Monitoring of supply voltage and charge pump output voltage
- Adjustable short-circuit detection in on and off state
- Open-load detection in off state
- Overtemperature detection and shutdown

18.2 Block diagram

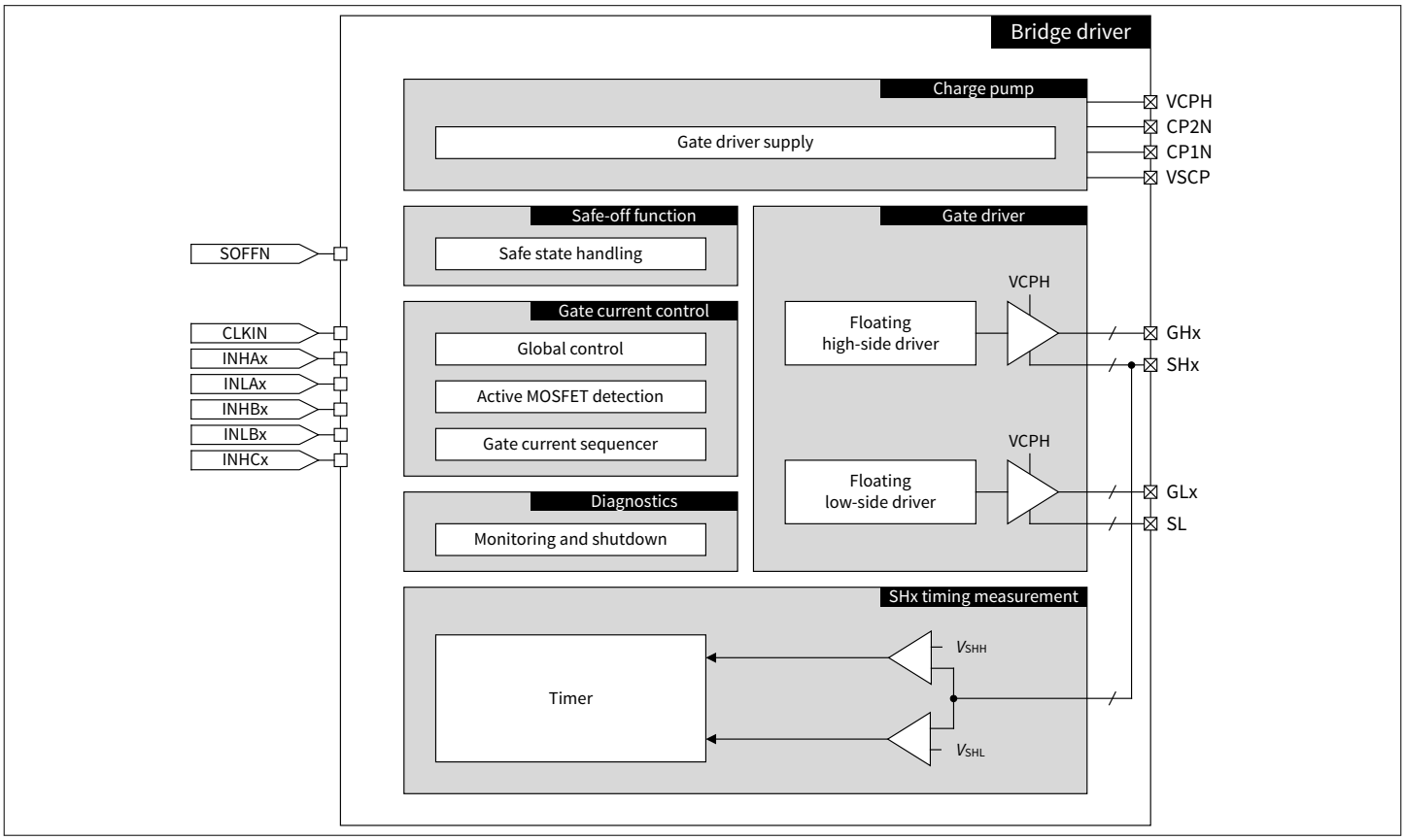

Figure 26 BDRV block diagram

18.3 Electrical characteristics BDRV

18.3.1 Charge pump

Table 38 Charge pump

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Charge pump frequency	f_{CP}	220	250	280	kHz	–	PRQ-1293
Regulated charge pump output voltage VCPH vs. VSCP	V_{CPH}	11	–	16	V	1) I_{VCPH} = -8mA	PRQ-1294
Regulated charge pump output voltage VCPH vs. VSCP	V_{CPH}	11	–	16	V	2) I_{VCPH} = -4 mA Charge pump in low-supply-voltage configuration	PRQ-1295
Maximum charge pump load current	I_{VCPH}	-8	–	–	mA	1)	PRQ-1296

(table continues...)

Table 38 (continued) Charge pump

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Maximum charge pump load current	I_{VCPH}	-4	–	–	mA	2) Charge pump in low-supply-voltage configuration	PRQ-1297
Charge pump high-voltage mode select threshold	V_{VSCP_HV}	16	–	18	V	Rising edge	PRQ-1298
Charge pump low-voltage mode select threshold	V_{VSCP_LV}	8	–	9	V	Falling edge	PRQ-1299

1) The current is calculated by I_{VCPH} = number of switching MOSFETs × f_{PWM} × Q_g = 6 × 20 kHz × 55 nC = 6.6 mA + additional external circuity supplied by charge pump (1.4 mA).
2) The current is calculated by I_{VCPH} = number of switching MOSFETs × f_{PWM} × Q_g = 6 × 20 kHz × 30 nC = 3.6 mA + additional external circuity supplied by charge pump (0.4 mA).

18.3.2 Gate driver

Table 39 Gate driver

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ON-state output voltage Gxx vs. Sxx	$V_{GS(ON)}$	9	–	11	V	1) $V_{VSCP} \geq 8$ V, $I_{VCPH} \geq -8$ mA	PRQ-1300
ON-state output voltage Gxx vs. Sxx	$V_{GS(ON)}$	7	–	11	V	1) $V_{VSCP} \geq 7$ V, $I_{VCPH} \geq -8$ mA	PRQ-1301
ON-state output voltage Gxx vs. Sxx	$V_{GS(ON)}$	6	–	11	V	2) $V_{VSCP} \geq 4.5$ V, $I_{VCPH} \geq -4$ mA Charge pump in low-supply-voltage configuration	PRQ-1302
OFF-state output voltage Gxx vs. Sxx	$V_{GS(OFF)}$	–	–	1.5	V	Programmable gate current settings < 32	PRQ-1304
OFF-state output voltage Gxx vs. Sxx	$V_{GS(OFF)}$	–	–	2	V	Programmable gate current settings ≥ 32	PRQ-1305
Gate current accuracy	A_{GATE}	-67	–	+67	%	Refers to the nominal value of the programmable gate current for setting 0	PRQ-1306
Gate current accuracy	A_{GATE}	-33.4	–	+33.4	%	Refers to the nominal value of the programmable gate current for setting 63	PRQ-1307

(table continues...)

Table 39 (continued) Gate driver

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Gate current channel-to-channel variation	A_{GATE_C2C}	-50	–	+50	%	–	PRQ-1308
Gate current settling time	t_{GATE_SET}	–	–	100	ns	–	PRQ-1309

1) The current is calculated by I_{VCPH} = number of switching MOSFETs × f_{PWM} × Q_g = 6 × 20 kHz × 55 nC = 6.6 mA + additional external circuity supplied by charge pump (1.4 mA).
2) The current is calculated by I_{VCPH} = number of switching MOSFETs × f_{PWM} × Q_g = 6 × 20 kHz × 30 nC = 3.6 mA + additional external circuity supplied by charge pump (0.4 mA).

18.3.3 SHx timing measurement

Table 40 SHx timing measurement

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
High-side timing measurement comparator threshold	V_{SHH}	V_{VSCP} - 2.5 V	V_{VSCP} - 2.25 V	V_{VSCP} - 2 V	V	–	PRQ-1310
Low-side timing measurement comparator threshold	V_{SHL}	2	2.25	2.5	V	–	PRQ-1311
Delay of timing measurement comparators	t_{SHx}	5	–	20	ns	–	PRQ-1312

18.3.4 Diagnostics

Table 41 Diagnostics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Thermal shutdown junction temperature	T_{JSD}	175	185	195	°C	Rising edge	PRQ-1313
Thermal shutdown hysteresis	T_{jHYS}	5	10	15	°C	–	PRQ-1314
Thermal shutdown filter time	t_{TSDf}	5	10	15	µs	–	PRQ-1315
Drain-source overvoltage threshold accuracy 0	A_{DSOV_TH0}	-25	–	+25	%	Refers to the nominal value of the programmable parameter V_{DSOV_TH} for setting 0	PRQ-1603

(table continues...)

Table 41 (continued) Diagnostics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Drain-source overvoltage threshold accuracy x	A_{DSOV_THx}	-20	–	+20	%	Refers to the nominal values of the programmable parameter V_{DSOV_TH} for all settings except 0	PRQ-1316
Drain-source monitoring blank time accuracy	A_{VDS_BLK}	-15	–	+15	%	Refers to the nominal values of the programmable parameters t_{VDS_BLK} and $t_{VDS\_BLK\_FW}$	PRQ-1317
Drain-source monitoring filter time accuracy	A_{VDS_FILT}	-15	–	+15	%	Refers to the nominal values of the programmable parameter t_{VDS_FILT}	PRQ-1318
VSCP undervoltage threshold	V_{VSCP_UV}	4	4.25	4.5	V	–	PRQ-1319
VSCP undervoltage hysteresis	$V_{VSCP\_UV\_HYS}$	50	150	400	mV	–	PRQ-1320
VSCP overvoltage threshold	V_{VSCP_OV}	32	33.5	35	V	–	PRQ-1321
VSCP overvoltage hysteresis	$V_{VSCP\_OV\_HYS}$	350	500	900	mV	–	PRQ-1322
VSCP shutdown filter time	t_{VSCP_SD}	20	30	40	µs	–	PRQ-1323
VCPH undervoltage threshold accuracy	A_{VCPH_UV}	-0.5	–	0.5	V	Refers to the nominal values of the programmable parameter V_{VCPH_UV}	PRQ-1324
VCPH shutdown filter time	t_{VCPH_SD}	50	60	70	µs	–	PRQ-1325

19 Application information

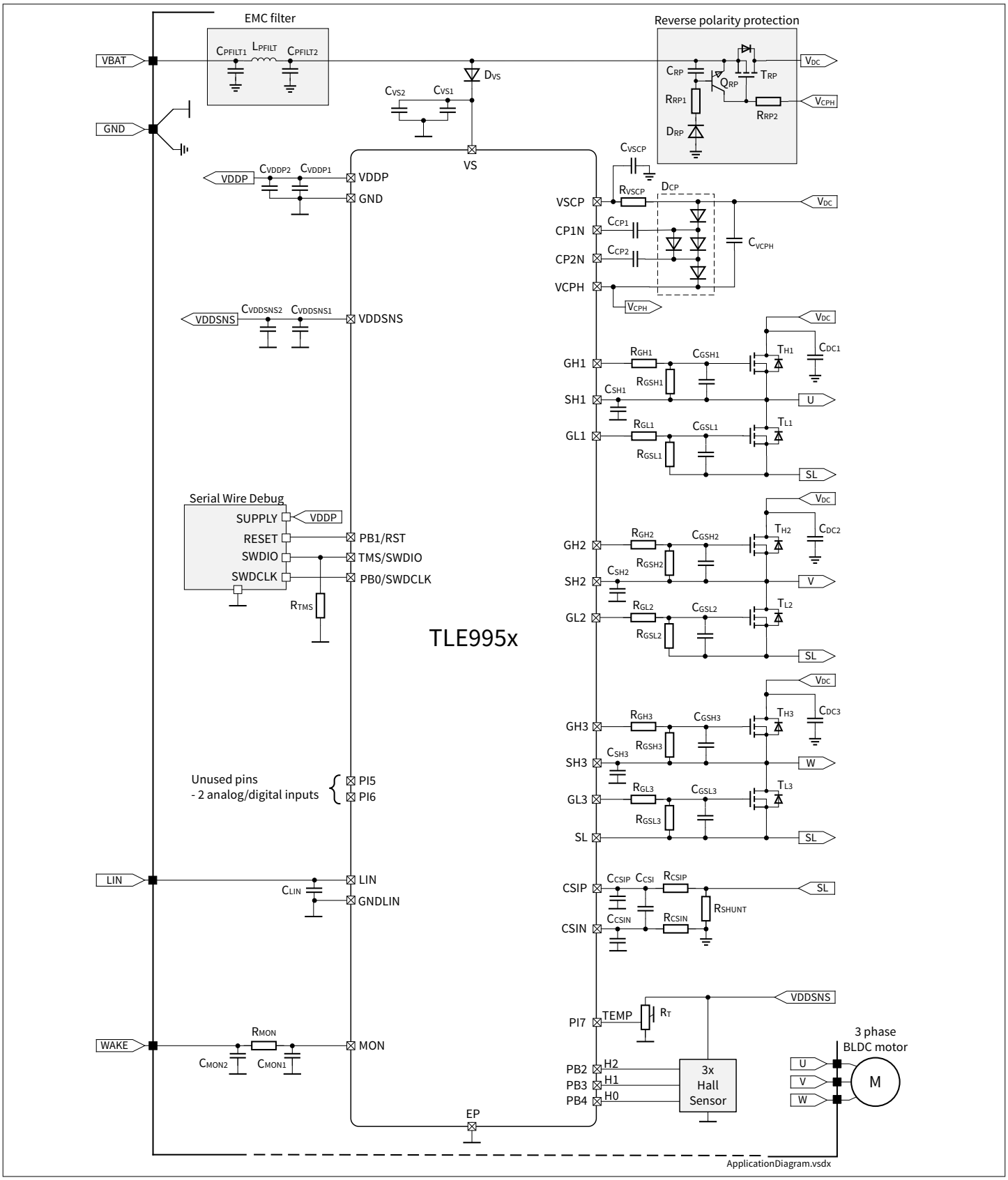

Figure 27 Application diagram (example)

Table 42 External component list (BOM)

Symbol	Function	Component
$C_{PFILT1, 2}$	EMC filter capacitors	application dependent, e.g. 22 µF
L_{PFILT}	EMC filter coil	application dependent, e.g. 4.7µH
D_{VS}	Reverse polarity protection diode	application dependent, PN or Schottky type e.g. BAS52-02V or BAS3010B-03W
C_{VS1}	Decoupling capacitor at VS pin	min 100 nF, ceramic type (X7R)
C_{VS2}	Buffer capacitor at VS pin	application dependent, >22 µF
C_{VDDP1}	Decoupling capacitor at VDDP pin	min 100 nF, ceramic type (X7R)
C_{VDDP2}	Buffer capacitor at VDDP pin	e. g. 4.7 µF
$C_{VDDSNS1}$	Decoupling capacitor at VDDSNS pin	min 100 nF, ceramic type (X7R)
$C_{VDDSNS2}$	Buffer capacitor at VDDSNS pin	application dependent, e. g. 1 µF
R_{TMS}	Pull-down resistor at TMS/SWDIO pin	e. g. 4.7 kOhm
C_{LIN}	Decoupling capacitor at LIN pin	min 220 pF
R_{MON}	Resistor at MON pin	application dependent, e. g. 1 kOhm
C_{MON1}	Filter capacitor 1 at MON pin	application dependent, e. g. 1 nF
C_{MON2}	Filter capacitor 2 at MON connector	application dependent, e. g. 10 nF
T_{RP}	Reverse polarity protection MOSFET	application dependent, e. g. IAUC100N04S6N015
Q_{RP}	Reverse polarity protection transistor	e. g. BC817
C_{RP}	Reverse polarity protection capacitor	e. g. 1 nF
R_{RP1}	Reverse polarity protection resistor 1	e. g. 10 kOhm
R_{RP2}	Reverse polarity protection resistor 2	e. g. 3.3 kOhm
D_{RP}	Reverse polarity protection diode	e. g. BAS52-02V or BAS3010B-03W
C_{VSCP}	Filter capacitor at VSCP pin	application dependent, e. g. 1 µF
R_{VSCP}	Filter resistor at VSCP pin	application dependent, e. g. 2 Ohm
C_{CP1}	Charge pump flying capacitor 1	e. g. 220 nF
C_{CP2}	Charge pump flying capacitor 2	e. g. 220 nF
C_{VCPH}	Charge pump storage capacitor between VCPH and VSCP pins	e. g. 470 nF
D_{CP}	Diode array between VCPH, CP1N, CP2N and VSCP pins	e. g. BAV99S or BAT54XY
$T_{H1, 2, 3}$	N-channel MOSFET as high-side switch	application dependent, e. g. IAUC100N04S6N015
$T_{L1, 2, 3}$	N-channel MOSFET as low-side switch	application dependent, e. g. IAUC100N04S6N015
$C_{DC1, 2, 3}$	DC link capacitor per phase 1, 2 , 3	application dependent, e. g. 220 µF
$R_{GH1, 2, 3}$	Gate resistor for high-side switch	optional, e. g. 2 Ohm
$R_{GSH1, 2, 3}$	Gate-source resistor for high-side switch	optional, e. g. 100 kOhm

(table continues...)

Table 42 (continued) External component list (BOM)

Symbol	Function	Component
$C_{GSH1, 2, 3}$	Gate-source capacitor for high-side switch	optional, e. g. 1 nF
$C_{SH1, 2, 3}$	Source capacitor for high-side switch	optional, e. g. 1 nF
$R_{GL1, 2, 3}$	Gate resistor for low-side switch	optional, e. g. 2 Ohm
$R_{GSL1, 2, 3}$	Gate-source resistor for low-side switch	optional, e. g. 100 kOhm
$C_{GSL1, 2, 3}$	Gate-source capacitor for low-side switch	optional, e. g. 1 nF
C_{CSIP}	Filter capacitor	application dependent, e. g. 1 nF
C_{CSIN}	Filter capacitor	application dependent, e. g. 1 nF
C_{CSI}	Filter capacitor	application dependent, e. g. 1 nF
R_{CSIN}	Filter resistor	application dependent, e. g. 10 Ohm
R_{CSIP}	Filter resistor	application dependent, e. g. 10 Ohm
R_{SHUNT}	Shunt resistor	application dependent, e. g. 5 mOhm
R_T	Thermal resistor	optional, e. g. NTC
H1, H2, H3	Hall sensor 1, 2, 3	optional, e. g. TLE4963-1M

19.1 ESD tests

***Note**: Tests for ESD robustness according to IEC61000-4-2 “gun test” (150 pF, 330 Ω) were performed. The results and test condition will be available in a test report. The target values for the test are listed in the table below.*

Table 43 ESD "gun test"

Performed test	Result	Unit	Remarks
ESD at pin LIN, versus GND	>6	kV	1) positive pulse
ESD at pin LIN, versus GND	<-6	kV	1) negative pulse
ESD at pins MON, VS, VSCP, versus GND	>6	kV	1) 2) positive pulse
ESD at pins MON, VS, VSCP, versus GND	<-6	kV	1) 2) negative pulse

1) ESD susceptibility “ESD GUN”, tested by external test house (IBEE Zwickau, EMC Test report Nr. xx-xx-xx), according to “LIN Conformance Test Specification Package for LIN 2.1, October 10th, 2008” and “Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Application - AUDI, BMW, Daimler, Porsche, Volkswagen - Revision 1.3 / 2012”.
2) With external circuit as shown in the simplified application diagram.

20 Package

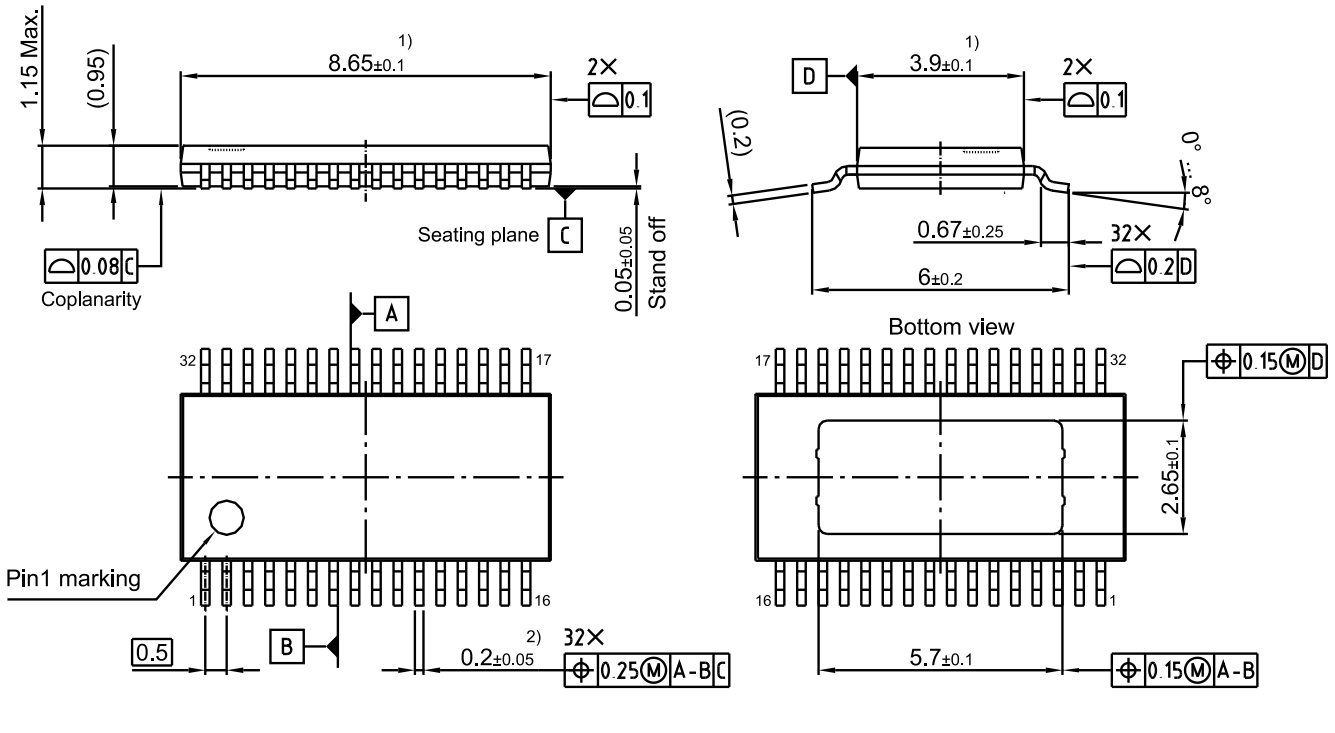

Figure 28 Package dimensions PG-TSDSO-32-1

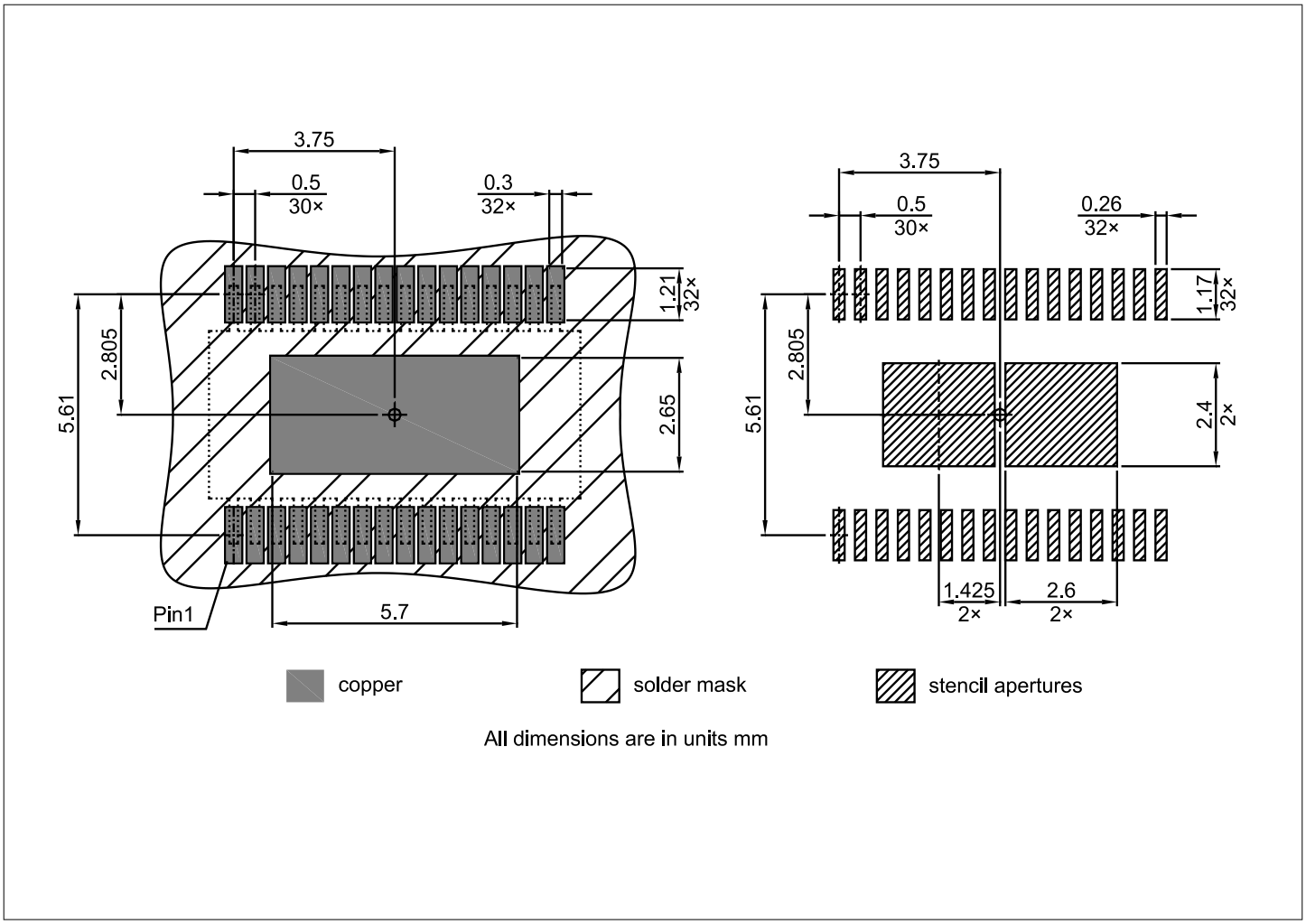

Figure 29 Footprint dimensions PG-TSDSO-32-1

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

21 Revision history

Revision number	Date of release	Description of changes
Rev. 1.00	2025-07-07	Initial version

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