OPTIREG™ linear TLE42744GV33

3.3 V low dropout linear voltage regulator

AEC Qualified

RoHS

PG-TO263-3

Features

- Very low current consumption
- Output voltages 3.3 V ±2%
- Output current up to 400 mA
- Very low dropout voltage
- Output current limitation
- Reverse-polarity protection
- Overtemperature shutdown
- Wide temperature range from -40°C up to 150°C
- Green Product (RoHS-compliant)

Potential applications

- Suitable for use in automotive electronics

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The OPTIREG™ linear TLE42744GV33 is a monolithic integrated low dropout voltage regulator for load currents up to 400 mA. An input voltage up to 40 V is regulated to $V_{Q,nom}$ = 3.3 V with a precision of ±2%. The device is designed for the harsh environment of automotive applications. Therefore, it is protected against overload, short-circuit, and overtemperature conditions by the implemented output current limitation and the overtemperature shutdown circuit. The TLE42744GV33 can be also used in all other applications requiring a stabilized 3.3 V voltage.

Due to its very low quiescent current, the TLE42744GV33 is dedicated for use in applications permanently connected to V_{BAT}.

Type	Package	Marking
TLE42744GV33	PG-TO263-3	42744V33

Table of contents

1 Block diagram

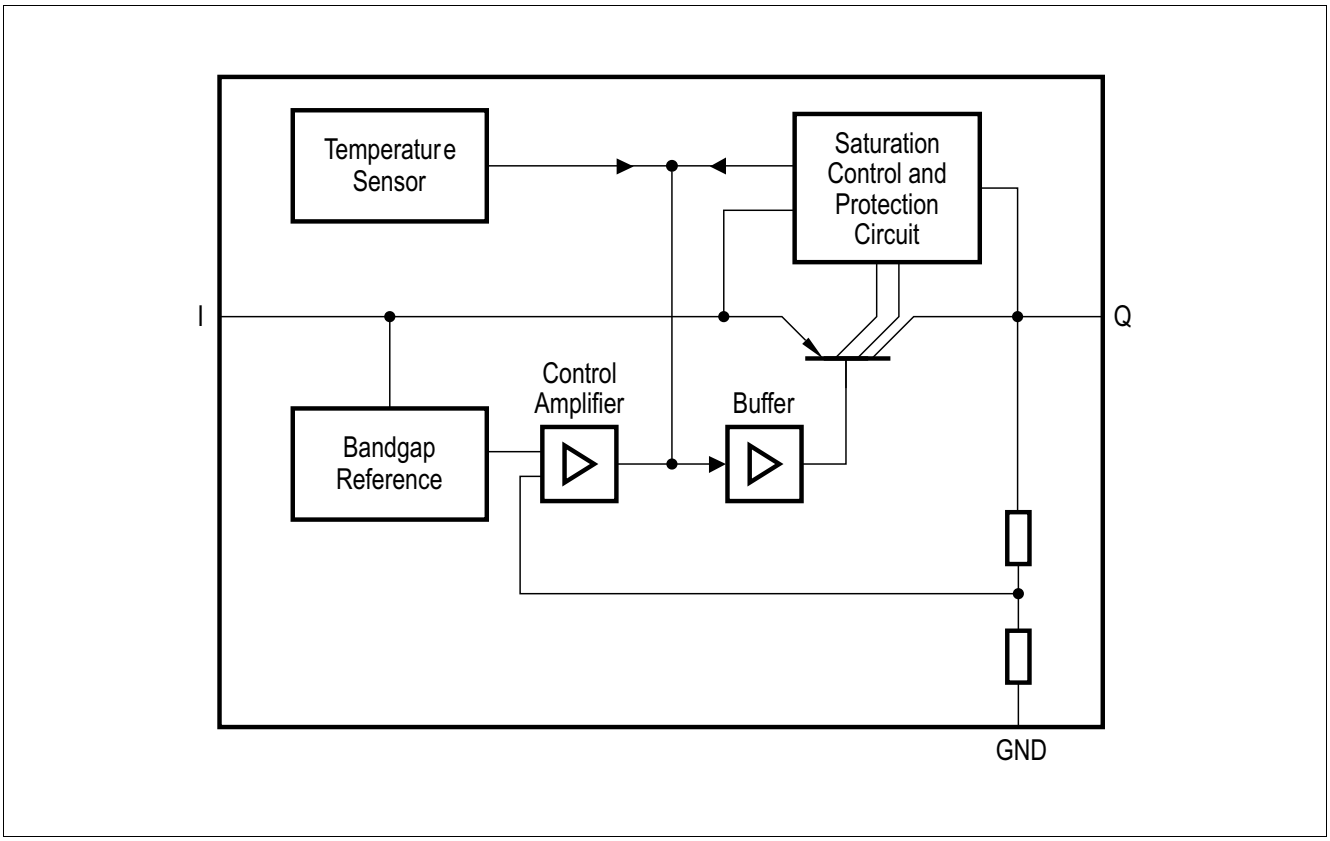


Figure 1 Block diagram

2 Pin configuration

2.1 Pin assignment

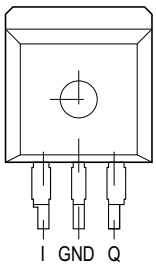


Figure 2 Pin configuration

2.2 Pin definitions and functions

Table 1 Pin definitions and functions

Pin	Symbol	Function
1	I	**Input** Block to ground directly at the IC with a ceramic capacitor
2	GND	**Ground** Internally connected to heat slug
3	Q	**Output** Block to ground with a capacitor close to the IC terminals, respecting the values given for its capacitance and ESR in **Table 3**
Heat slug	–	**Heat slug** Internally connected to GND; connect to GND and heatsink area

3 General product characteristics

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings[1)]

T_j = -40°C to +150°C, all voltages with respect to ground, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input I							
Voltage	V_I	-42	–	45	V	–	P_4.1.1
Output Q							
Voltage	V_Q	-1	–	40	V	–	P_4.1.2
Temperature							
Junction temperature	T_j	-40	–	150	°C	–	P_4.1.3
Storage temperature	T_{stg}	-50	–	150	°C	–	P_4.1.4
ESD susceptibility							
ESD absorption	$V_{ESD,HBM}$	-4	–	4	kV	[2)] Human body model (HBM)	P_4.1.5
ESD absorption	$V_{ESD,CDM}$	-1000	–	1000	V	[3)] Charge device model (CDM) at all pins	P_4.1.6

1) Not subject to production test, specified by design.
2) ESD susceptibility human body model (HBM) according to AEC-Q100-002 - JESD22-A114.
3) ESD susceptibility charged device model (CDM) according to ESDA STM5.3.1.

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

3.2 Functional range

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage	V_I	4.7	–	40	V		P_4.2.2
Output capacitor's requirements for stability	C_Q	22		–	µF	1)	P_4.2.3
Output capacitor's requirements for stability	$ESR(C_Q)$	–		3	Ω	2)	P_4.2.4
Junction temperature	T_j	-40		150	°C	–	P_4.2.5

1) The minimum output capacitance requirement is applicable for a worst-case capacitance tolerance of 30%.
2) Relevant ESR value at f = 10 kHz.

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

3.3 Thermal resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 4 Thermal resistance[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	3.6	–	K/W	Measured to heat slug	P_4.3.6
Junction to ambient	R_{thJA}	–	22	–	K/W	2) FR4 2s2p board	P_4.3.7
Junction to ambient	R_{thJA}	–	74	–	K/W	3) FR4 1s0p board, footprint only	P_4.3.8
Junction to ambient	R_{thJA}	–	42	–	K/W	3) FR4 1s0p board, 300 mm² heatsink area	P_4.3.9
Junction to ambient	R_{thJA}	–	34	–	K/W	3) FR4 1s0p board, 600 mm² heatsink area	P_4.3.10

1) Not subject to production test, specified by design.
2) The specified R_{thJA} value is according to JEDEC JESD51-2,-5,-7 at natural convection on an FR4 2s2p board. The product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with two inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable, a thermal via array under the exposed pad contacted the first inner copper layer.
3) The specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on an FR4 1s0p board. The product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with one copper layer (1 × 70 µm Cu).

4 Electrical characteristics

4.1 Electrical characteristics of the voltage regulator

Table 5 Electrical characteristics

V_I = 13.5 V, T_j = -40°C to +150°C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output Q							
Output voltage	V_Q	3.23	3.3	3.37	V	5 mA < I_Q < 400 mA; 4.7 V < V_I < 28 V	P_5.1.3
Output voltage	V_Q	3.23	3.3	3.37	V	5 mA < I_Q < 200 mA; 4.7 V < V_I < 40 V	P_5.1.4
Load regulation	$\Delta V_{Q,lo}$	–	40	70	mV	I_Q = 5 mA to 300 mA	P_5.1.7
Line regulation	$\Delta V_{Q,li}$	–	10	25	mV	V_I = 12 V to 32 V; I_Q = 5 mA	P_5.1.8
Output current limitation	I_Q	400	600	1100	mA	1)	P_5.1.9
Power supply ripple rejection	*PSRR*	–	60	–	dB	2) f_r = 100 Hz; V_r = 0.5 Vpp	P_5.1.10
Temperature output voltage drift	$\frac{dV_Q}{dT}$	–	0.5	–	mV/K	–	P_5.1.11
Overtemperature shutdown threshold	$T_{j,sd}$	151	–	200	°C	2) T_j increasing	P_5.1.12
Overtemperature shutdown threshold hysteresis	$T_{j,sdh}$	–	25	–	°C	2) T_j decreasing	P_5.1.13
Current consumption							
Quiescent current $I_q = I_I - I_Q$	I_q	–	100	220	µA	I_Q = 1 mA	P_5.1.14
Current consumption $I_q = I_I - I_Q$	I_q	–	8	15	mA	I_Q = 250 mA	P_5.1.15
Current consumption $I_q = I_I - I_Q$	I_q	–	20	30	mA	I_Q = 400 mA	P_5.1.17

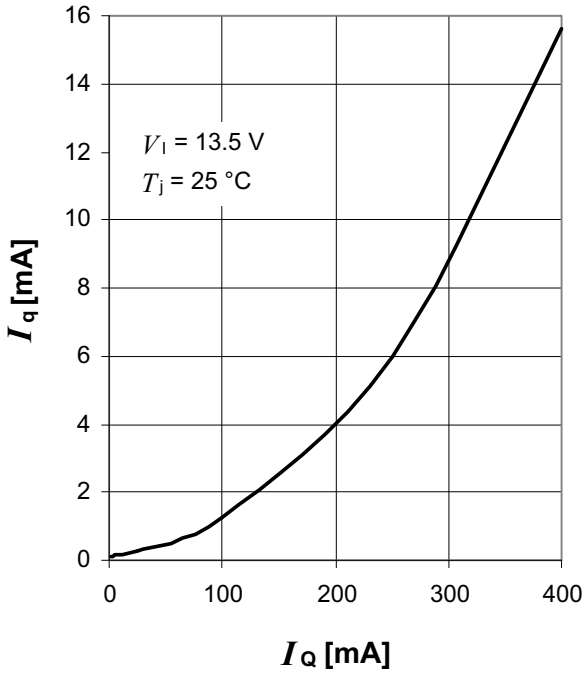
1) Measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at V_I = 13.5 V.

2) Not subject to production test, specified by design.

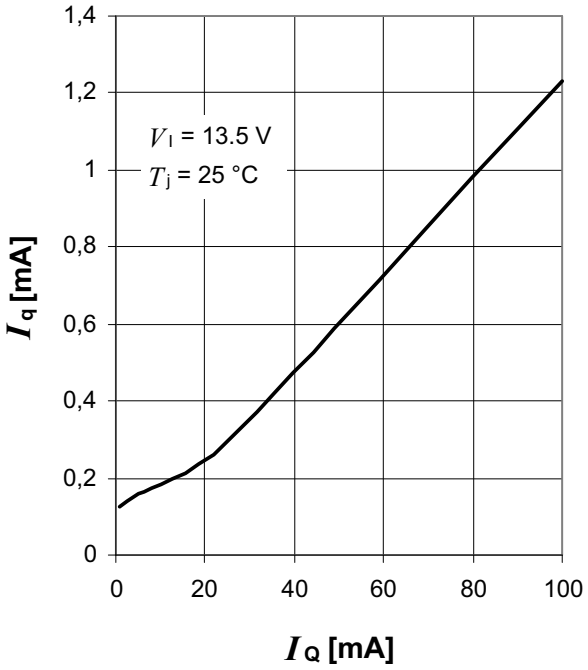
5 Typical performance characteristics

5.1 Typical performance characteristics of the voltage regulator

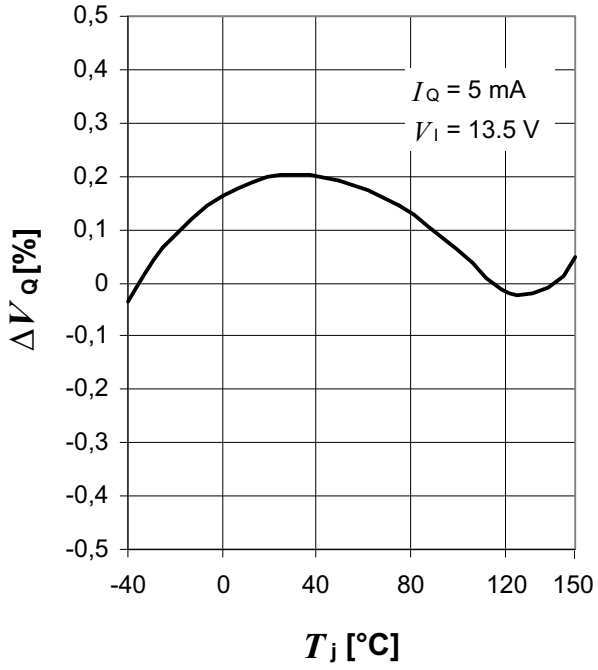
Current consumption I_q versus output current I_Q



Current consumption I_q versus low output current I_Q

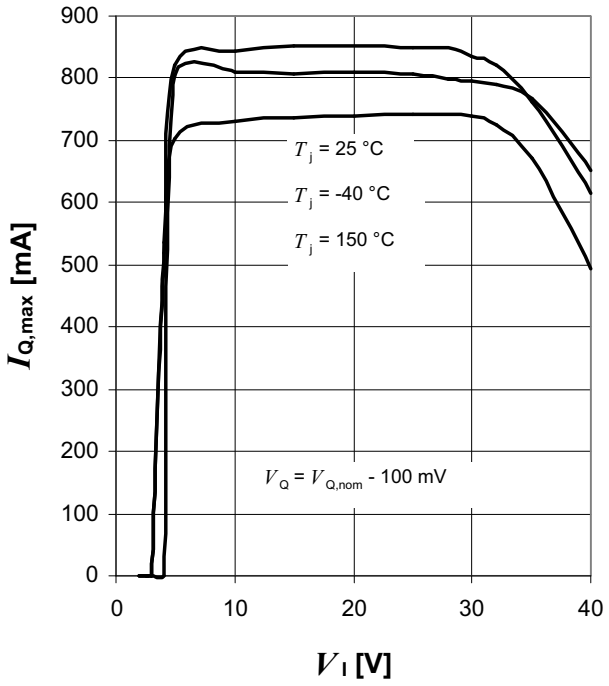


Output voltage variation ΔV_Q versus junction temperature T_J

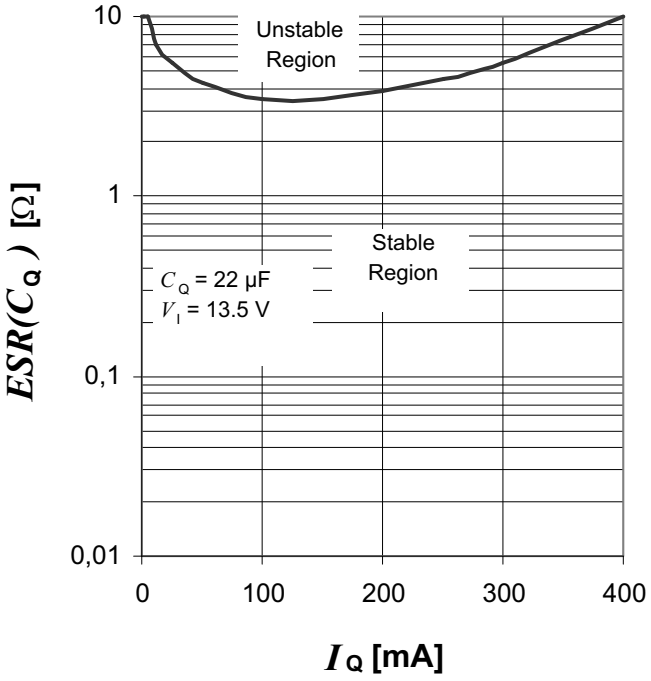


Typical performance characteristics

Maximum output current I_Q versus input voltage V_I



Region of stability: output capacitor's $ESR(C_Q)$ versus output current I_Q



6 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition, or quality of the device.

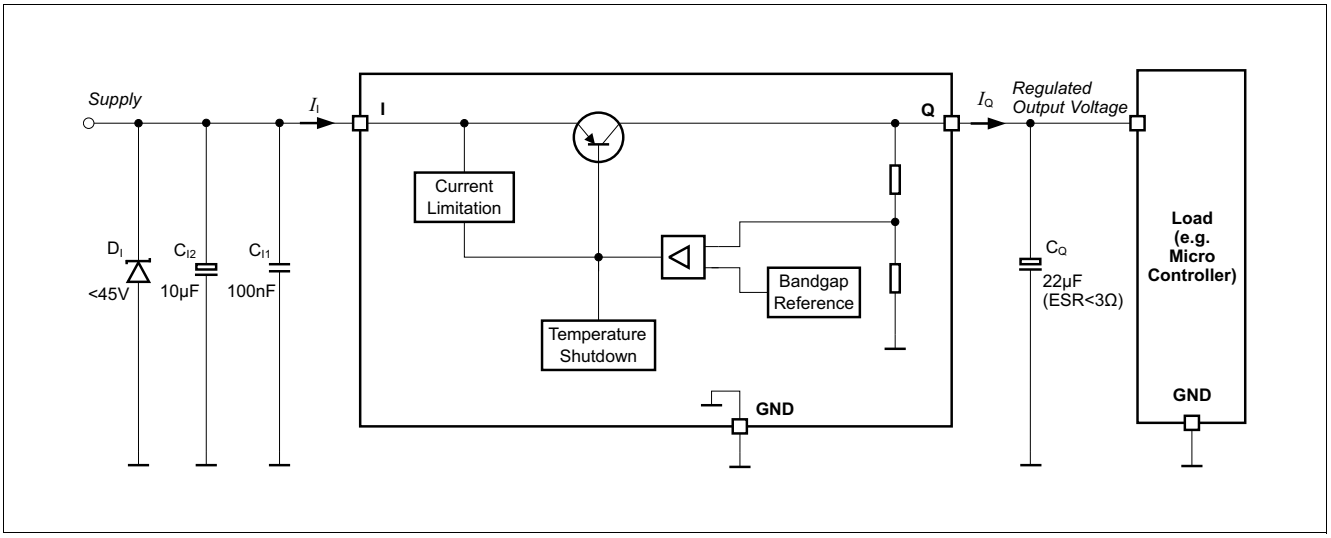


Figure 3 Application diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

6.1 Selection of external components

6.1.1 Input pin

The typical input circuitry for a linear voltage regulator is shown in **Figure 3**.

A ceramic capacitor at the input, in the range of 100 nF to 470 nF, is recommended to filter out the high frequency disturbances imposed by the line, for example, ISO pulses 3a/b. This capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10 µF to 470 µF is recommended as an input buffer to smooth out high energy pulses, such as ISO pulse 2a. This capacitor should be placed close to the input pin of the linear voltage regulator on the PCB.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and protect the device against any damage due to overvoltage.

The external components at the input are not mandatory for the operation of the voltage regulator, but they are recommended in case of possible external disturbances.

6.1.2 Output pin

An output capacitor is mandatory for the stability of linear voltage regulators.

The requirement to the output capacitor is given in **Table 3**. The graph **Region of stability: output capacitor's ESR(C_Q) versus output current I_Q** shows the stable operation range of the device.

Application information

The TLE42744GV33 is designed to be stable with extremely low-ESR capacitors. According to the automotive environment, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the regulator's output and GND pins, and on the same side of the PCB as the regulator itself.

In case of rapid transients of input voltage or load current, the capacitance should be dimensioned in accordance, and verified in the real application that the output stability requirements are fulfilled.

6.2 Thermal considerations

Knowing the input voltage, the output voltage, and the load profile of the application, the total power dissipation can be calculated:

$$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q \quad (6.1)$$

with

- P_D: continuous power dissipation
- V_I: input voltage
- V_Q: output voltage
- I_Q: output current
- I_q: quiescent current

The maximum acceptable thermal resistance R_{thJA} can then be calculated:

$$R_{thJA,\,max} = \frac{T_{j,\,max} - T_a}{P_D} \quad (6.2)$$

with

- $T_{j,max}$: maximum allowed junction temperature
- T_a: ambient temperature

Based on the above calculation, the proper PCB type and the necessary heat sink area can be determined with reference to the specification in **Table 4**.

Example

Application conditions:

V_I = 13.5 V
V_Q = 3.3 V
I_Q = 250 mA
T_a = 75°C

Application information

Calculation of $R_{thJA,max}$:

$$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q$$
$$= (13.5\ V - 3.3\ V) \times 250\ mA + 13.5\ V \times 15\ mA$$
$$= 2.55\ W + 0.2025\ W$$
$$= 2.7525\ W$$

$$R_{thJA,max} = (T_{j,max} - T_a)/P_D$$
$$= (150°C - 75°C)/2.7525\ W$$
$$= 27.25\ K/W$$

As a result, the PCB design must ensure a thermal resistance R_{thJA} lower than 27.25 K/W. By considering the thermal resistance as provided in **Table 4**, a FR4 2s2p board is required in this case.

6.3 Reverse polarity protection

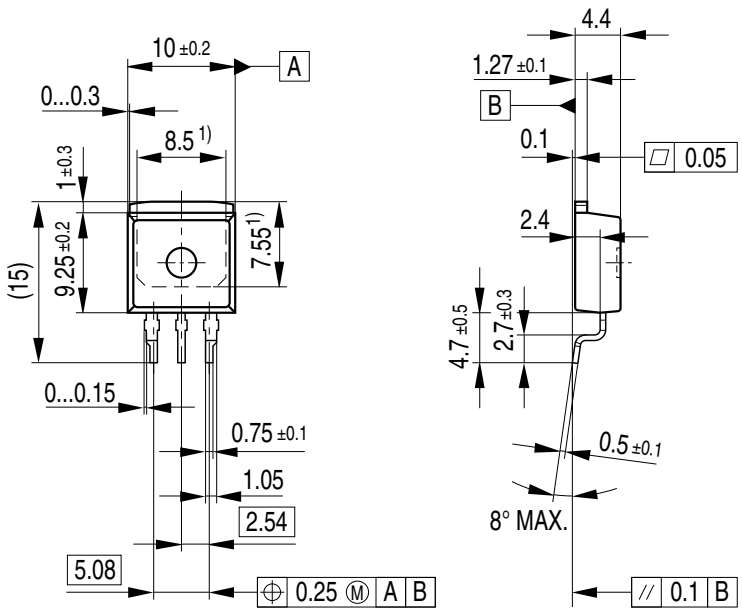
The TLE42744GV33 is self-protected against reverse-polarity faults and allows negative supply voltage. External reverse-polarity diode is not needed. However, the absolute maximum ratings of the device as specified in **Table 2** must be kept.

The reverse voltage causes several small currents to flow into the IC hence increasing its junction temperature. As the thermal-shutdown circuitry does not work in the reverse polarity condition, designers have to consider this in their thermal design.

6.4 Further application information

For further information, visit **https://www.infineon.com**.

7 Package information



1) Typical
All metal surfaces: tin plated, except area of cut.
Metal surface min. x=7.25, y=6.9

Figure 4 PG-TO263-3[1)]

Green Product (RoHS-compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a Green Product. Green Products are RoHS-compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

1) Dimensions in mm

8 Revision history

Revision	Date	Changes
1.4	2025-02-01	Separation of the TLE42744 rev. 1.30 datasheet into individual product offerings Template update and editorial changes
1.3	2018-03-05	Marking update in chapter overview (TLE42744GSV33 and TLE42744DV33) Updated template on the last page
1.2	2014-07-03	Application information added PG-TO252-3 and PG-SSOP-14 EP package outlines updated
1.1	2010-01-13	Updated version datasheet: version TLE42744EV50 in PG-SSOP-14 exposed pad and all related description added; 3.3 V versions TLE42744GV33 in PG-TO263-3, TLE42744DV33 in PG-TO252-3 and TLE42744GSV33 in PG-SOT223-4 and all related description added
1.0	2009-01-14	Initial version final datasheet

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