OPTIREG™ linear TLE4267-2G

5V Low drop voltage post regulator

AEC Qualified RoHS

Features

- Output voltage tolerance ≤ ±2%
- 400 mA output current capability
- Low drop voltage
- Very low standby current consumption
- Input voltage up to 40 V
- Overvoltage protection up to 60 V (≤ 400 ms)
- Reset function down to 1 V output voltage
- Adjustable reset time
- On/off logic
- Overtemperature protection
- Reverse polarity protection
- Short-circuit proof
- Wide temperature range
- Suitable for use in automotive electronics
- Green Product (RoHS compliant)

Potential applications

General automotive applications.

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The TLE4267-2G is a low drop voltage regulator with a 5 V output voltage for automotive applications in a PG-TO220-7 package. It supplies an output current up to 400 mA. The device is short circuit-proof and has an overtemperature protection circuit. The device also has a reset output with a reset delay that can be set by an external capacitor. The two logic inputs, inhibit and hold, allow for implementation of a self-holding circuit without external components. When the device is turned off, the output voltage drops to 0 V and current consumption tends towards 0 µA.

Type	Package	Marking
TLE4267-2G	PG-TO220-7	4267-2G

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1 Block diagram

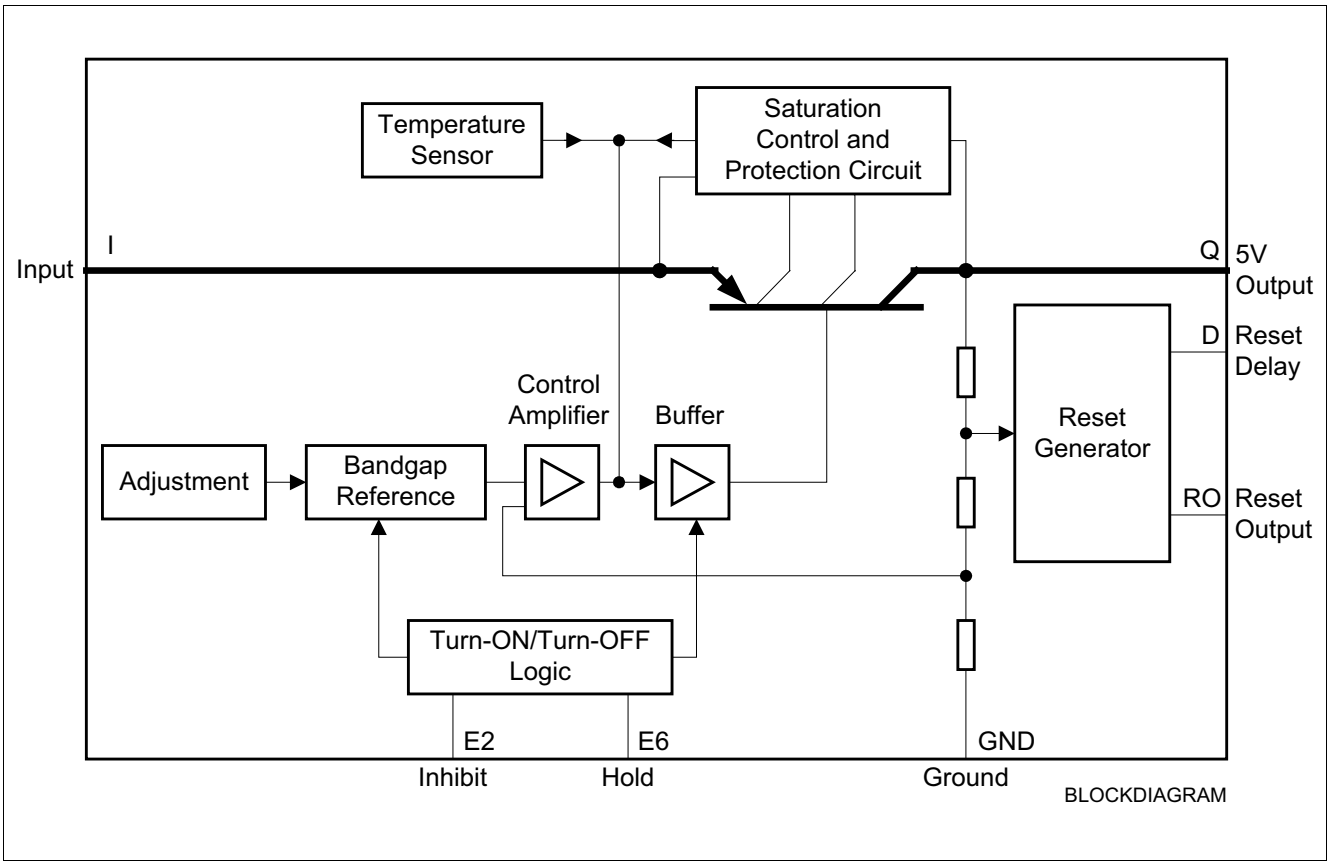


Figure 1 Block diagram

2 Pin configuration

2.1 Pin assignment

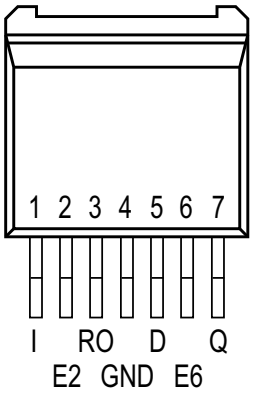


Figure 2 Pin configuration

2.2 Pin definitions and functions

Table 1 Pin definition and function

Pin	Symbol	Function
1	I	**Input;** it is recommended to place small ceramic capacitor close to the pin to GND in order to compensate line influences
2	E2	**Inhibit;** device is enabled by a high signal on this pin; internal pull-down resistor of 100 kΩ
3	RO	**Reset output;** open-collector output internally connected to the output via a resistor of 30 kΩ
4	GND	**Ground;** connected to exposed paddle
5	D	**Reset delay;** connect via capacitor to GND
6	E6	**Hold;** see **Table 8** for function; this input is connected to output voltage via a pull-up resistor of 50 kΩ
7	Q	**Output voltage;** connect output capacitor C_Q to GND close to the pin, respecting the values specified for its capacitance and ESR in **Table 3**

3 General product characteristics

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings [1)]

T_j = -40°C to +150°C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input I							
Voltage	V_I	-42	–	42	V	–	P_3.1.1
Voltage	V_I	–	–	60	V	$t \leq 400$ ms	P_3.1.2
Reset output RO							
Voltage	V_{RO}	-0.3	–	7	V	–	P_3.1.3
Reset delay							
Voltage	V_D	-0.3	–	42	V	–	P_3.1.4
Output O							
Voltage	V_Q	-0.3	–	7	V	–	P_3.1.5
Inhibit							
Voltage	V_{E2}	-42	–	42	V	–	P_3.1.6
Current	I_{E2}	-5	–	5	mA	$t \leq 400$ ms	P_3.1.7
Hold E6							
Voltage	V_{E6}	-0.3	–	7	V	–	P_3.1.8
GND							
Current	I_{GND}	-0.5	–	–	A	–	P_3.1.9
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_3.1.10
Storage temperature	T_{stg}	-50	–	150	°C	–	P_3.1.11
ESD susceptibility							
ESD robustness to GND	$V_{ESD,HBM}$	-2	–	2	kV	HBM[2)]	P_3.1.12
ESD robustness to GND	$V_{ESD,CDM}$	-500	–	500	V	CDM[3)]; all pins except 1, 7	P_3.1.13
ESD robustness pins 1, 7 to GND	$V_{ESD,CDM}$	-750	–	750	V	CDM[4)]	P_3.1.14

1) Not subject to production test, specified by design.
2) Human body model (HBM) robustness according to AEC-Q100-002.
3) Charge device model (CDM) robustness according to AEC-Q100-011, Rev-D; voltage level refers to test conditions (TC) mentioned in the standard.
4) Charge Device model (CDM) robustness according to AEC-Q100-011, Rev-D; voltage level refers to test conditions (TC) mentioned in the standard.

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent device destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

3.2 Functional range

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage range	V_I	5.5	–	40	V	see diagram	P_3.2.1
Capacitance of output capacitor for stability	C_Q	22	–	–	µF	1)2)	P_3.2.2
Equivalent series resistance of output capacitor	ESR(C_Q)	–	–	3	Ω	1)	P_3.2.3
Junction temperature	T_j	-40	–	150	°C	–	P_3.2.4

1) Not subject to production test, specified by design
2) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%

Note: Within the functional or operating range, the device operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the electrical characteristics table.

3.3 Thermal resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 4 Thermal resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Thermal resistance							
Junction ambient	R_{thJA}	–	–	65	K/W	1)	P_3.3.1
Junction-case	R_{thJC}	–	–	6	K/W	1)	P_3.3.2
Junction-case	Z_{thJC}	–	–	2	K/W	1) $T < 1$ ms	P_3.3.3

1) Not subject to production test, specified by design

4 Block description and electrical characteristics

4.1 Voltage regulation

The TLE4267-2G regulates an input voltage V_I in the range of 5.5 V up to 40 V to a nominal output of V_Q = 5 V. The internal control amplifier compares a reference voltage to a voltage that is proportional to the output voltage and drives the base of the pass transistor accordingly via a buffer.
The accuracy of the internal reference is optimized by resistance adjustment internally. Saturation control as a function of the load current prevents an over-saturating of the power element.

4.1.1 Electrical characteristics voltage regulation

Table 5 Electrical characteristics voltage regulation

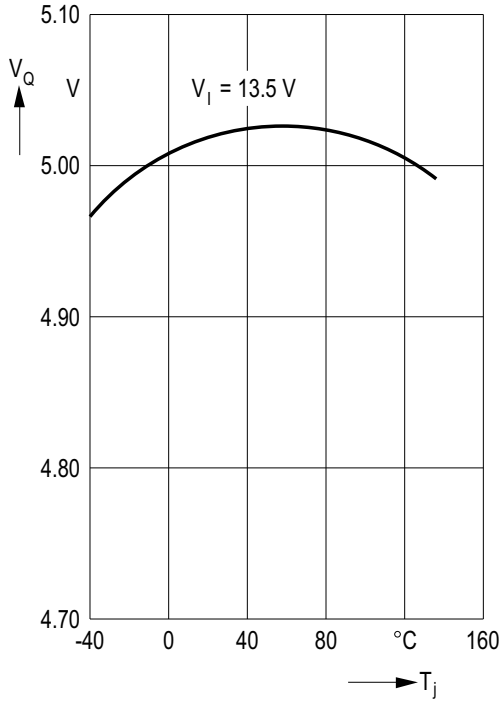
V_I = 13.5 V; -40 °C < T_j < 125 °C; V_{E2} > 4 V (unless specified otherwise)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output voltage	V_Q	4.9	5	5.1	V	5 mA ≤ I_Q ≤ 400 mA; 6 V ≤ V_I ≤ 26 V	P_4.2.1
Output voltage	V_Q	4.9	5	5.1	V	5 mA ≤ I_Q ≤ 150 mA; 6 V ≤ V_I ≤ 40 V	P_4.2.2
Output current limiting	I_Q	500	–	–	mA	T_j = 25 °C	P_4.2.3
Current consumption $I_q = I_I - I_Q$	I_q	–	–	50	µA	Device turned off	P_4.2.4
Current consumption $I_q = I_I - I_Q$	I_q	–	1.0	10	µA	T_j = 25 °C; device turned off	P_4.2.5
Current consumption $I_q = I_I - I_Q$	I_q	–	1.3	4	mA	I_Q = 5 mA; device turned on	P_4.2.6
Current consumption $I_q = I_I - I_Q$	I_q	–	–	60	mA	I_Q = 400 mA	P_4.2.7
Current consumption $I_q = I_I - I_Q$	I_q	–	–	80	mA	I_Q = 400 mA V_I = 5 V	P_4.2.8
Drop voltage	V_{Dr}	–	0.3	0.6	V	I_Q = 400 mA[1)]	P_4.2.9
Load regulation	ΔV_Q	–	–	50	mV	5 mA ≤ I_Q ≤ 400 mA	P_4.2.10
Line regulation	ΔV_Q	–	15	25	mV	V_I = 6 V to 36 V; I_Q = 5 mA	P_4.2.11
Power supply ripple rejection	*PSSR*	–	54	–	dB	f_r = 100 Hz; V_r = 0.5 V_{pp}	P_4.2.12
Longterm stability	ΔV_Q	–	0	–	mV	1000 h	P_4.2.13
Overvoltage protection							
Turn-off voltage	$V_{I,OV}$	42	44	46	V	V_I increasing	P_4.2.14
Turn-on voltage	$V_{I,turn\ on}$	36	–	–	V	V_I decreasing after turn-off	P_4.2.15

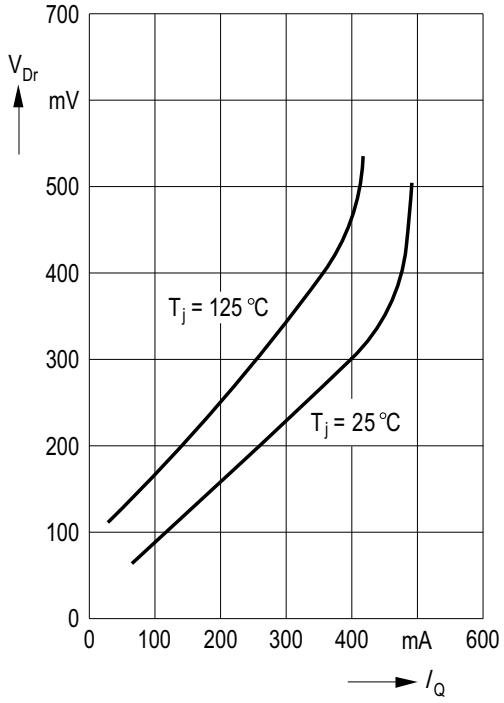
1) Drop voltage = V_I - V_Q (measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at V_I = 13.5 V)

4.1.2 Typical performance characteristics voltage regulation

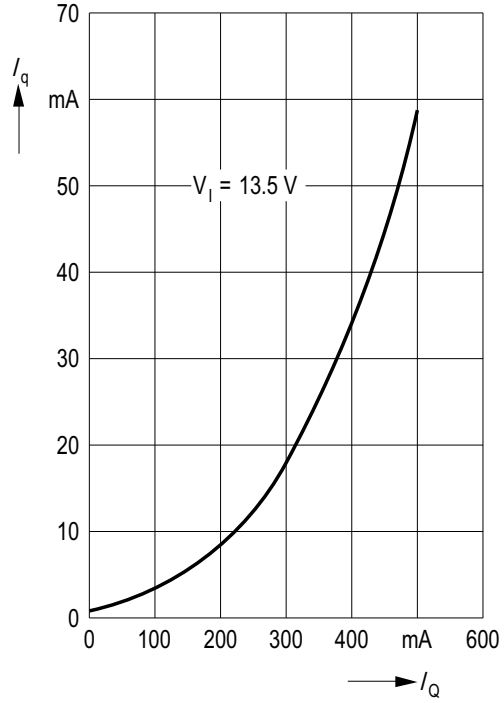
Output voltage V_Q versus temperature T_j



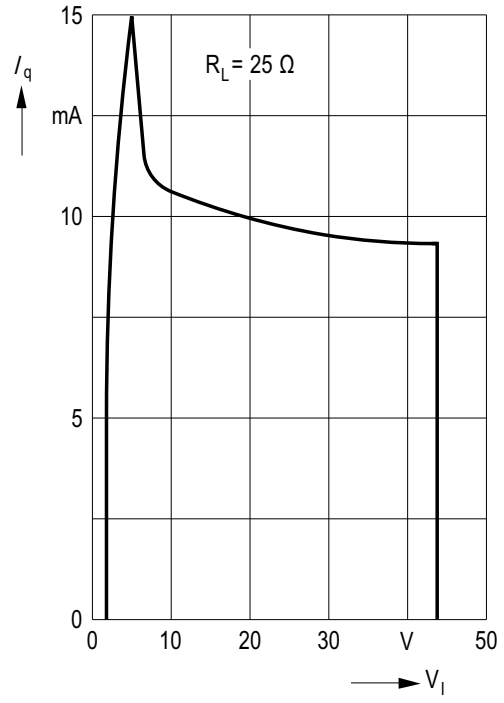
Dropout voltage V_{DR} versus output current I_Q



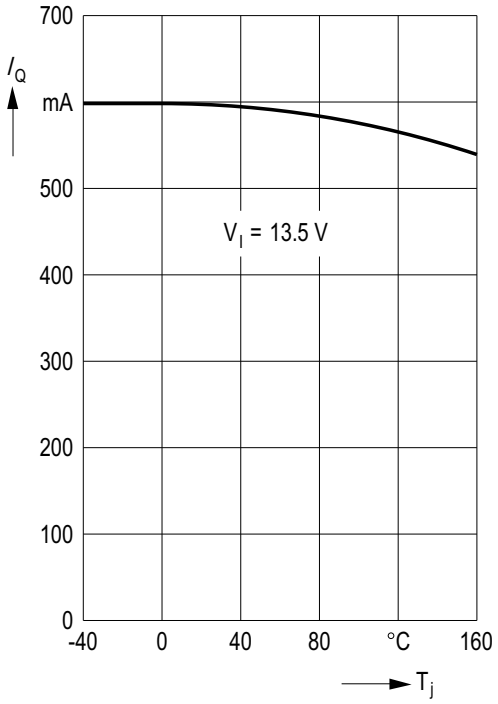
Current consumption I_q versus output current I_Q



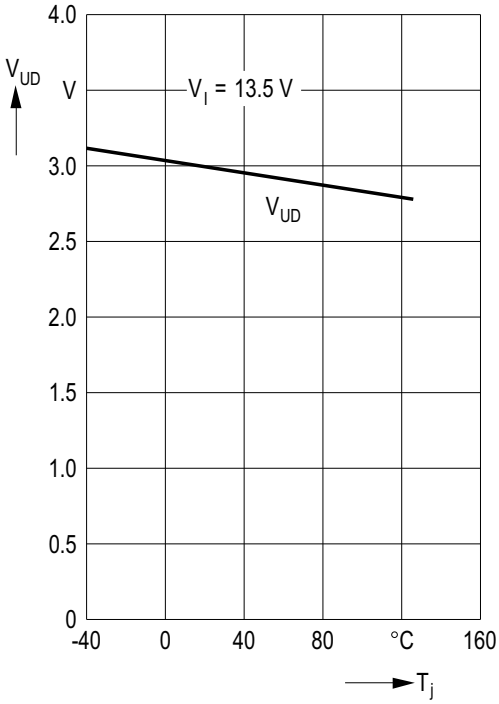
Current consumption I_q versus input voltage V_I



Output current limiting I_Q versus temperature T_j



Output current limiting I_Q versus input voltage V_I



4.2 Reset function

A reset signal is generated for an output voltage of $V_Q < V_{RT}$. The reset delay can be set with an external capacitor. The reset output R_O is high state if the voltage on the delay capacitor C_D is greater or equal V_{UD}. The delay capacitance C_D is charged with the current I_D for output voltages greater than the reset threshold V_{RT}. If the output voltage drops below than V_{RT} a fast discharge of the delay capacitor C_D sets in. As V_{CD} drops below V_{LD} the reset output R_O is set to low (see **Figure 3**). The reset delay can be adjusted by dimensioning the capacitance of the external capacitor C_D.

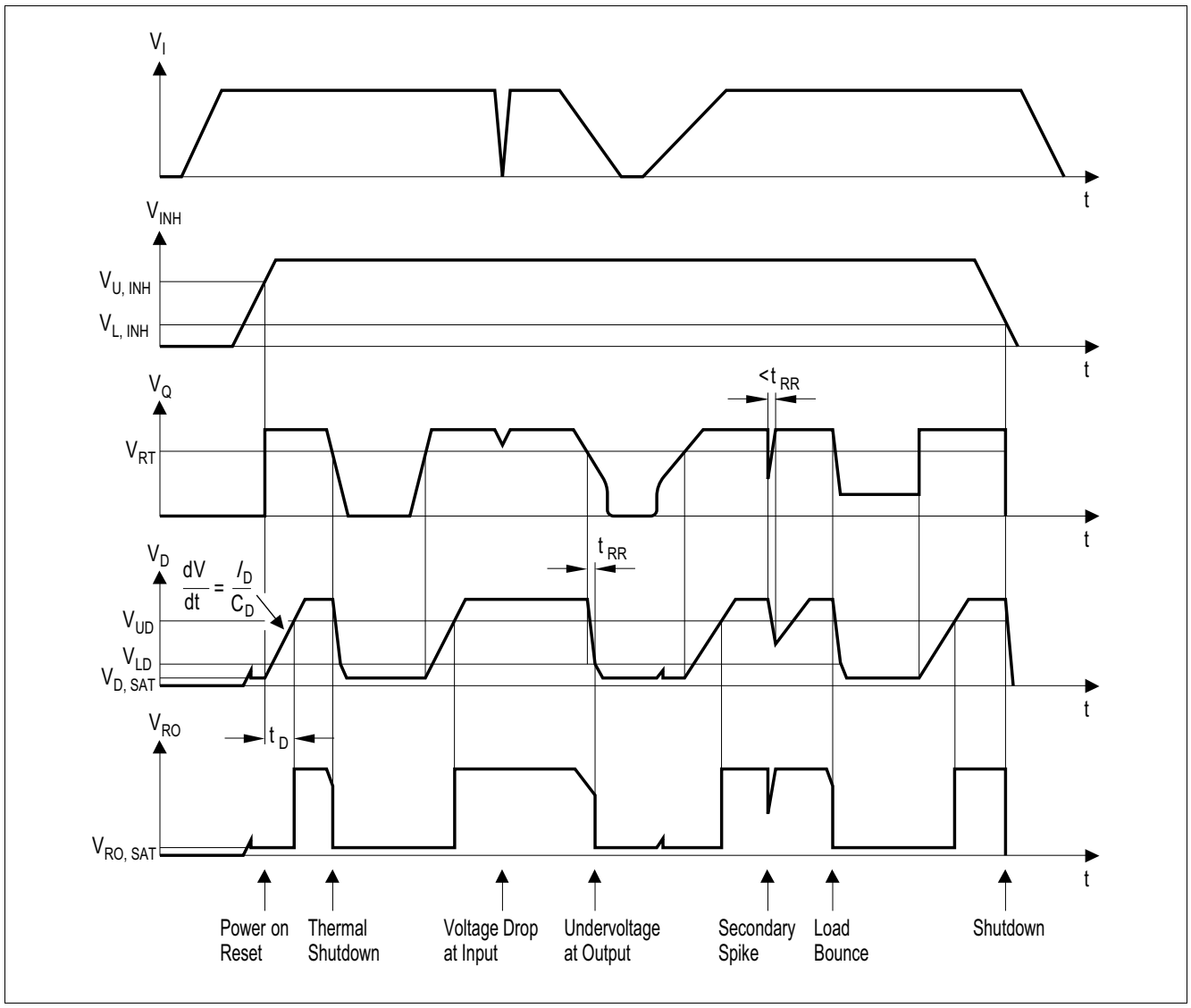


Figure 3 Time response

4.2.1 Electrical characteristics reset function

Table 6 Electrical characteristics reset function

V_I = 13.5 V; -40 °C < T_j < 125 °C; V_{E2} > 4 V (unless specified otherwise)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Switching threshold	V_{RT}	4.5	4.65	4.8	V	V_Q decreasing	P_4.3.1
Reset high level	–	4.5	–	–	V	R_{ext} = ∞	P_4.3.2
Saturation voltage	$V_{RO,SAT}$	–	0.1	0.4	V	R_R = 4.7 kΩ [1)]	P_4.3.3
Internal pull-up resistor	R_{RO}	–	30	–	kΩ	–	P_4.3.4
Saturation voltage	$V_{D,SAT}$	–	50	100	mV	V_Q < V_{RT}	P_4.3.5
Charge current	I_D	8	15	25	µA	V_D = 1.5 V	P_4.3.6
Upper delay switching threshold	V_{UD}	2.6	3	3.3	V	–	P_4.3.7

Table 6 Electrical characteristics (cont'd)**reset function**

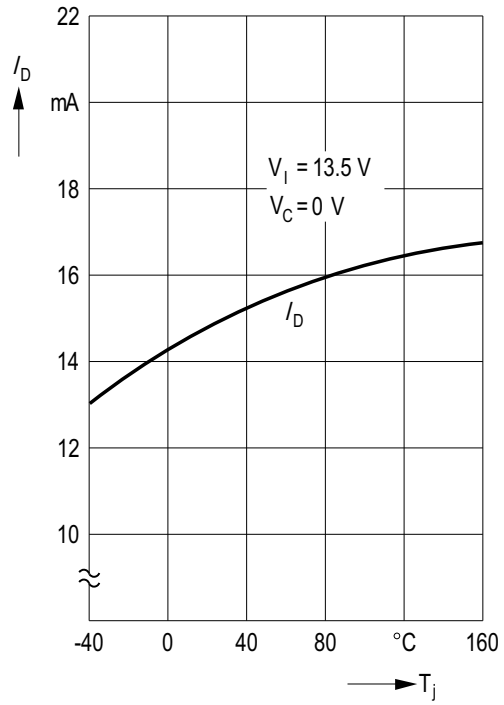
V_I = 13.5 V; -40 °C < T_j < 125 °C; V_{E2} > 4 V (unless specified otherwise)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Delay time	t_D	–	20	–	ms	C_D = 100 nF	P_4.3.8
Lower delay switching threshold	V_{LD}	–	0.43	–	V	–	P_4.3.9
Reset reaction time	t_{RR}	–	2	–	µs	C_D = 100 nF	P_4.3.10

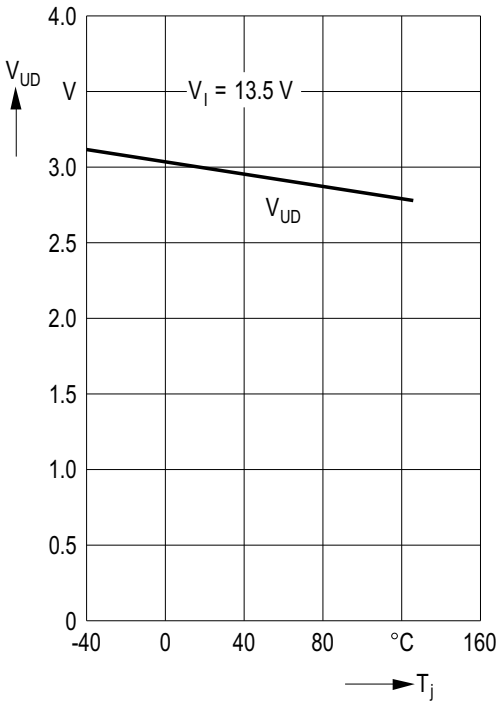
1) The reset output is Low for 1 V < V_Q < V_{RT}

4.2.2 Typical performance characteristics reset function

Charge current I_D versus temperature T_j



Delay switching threshold V_{UD} versus temperature T_j



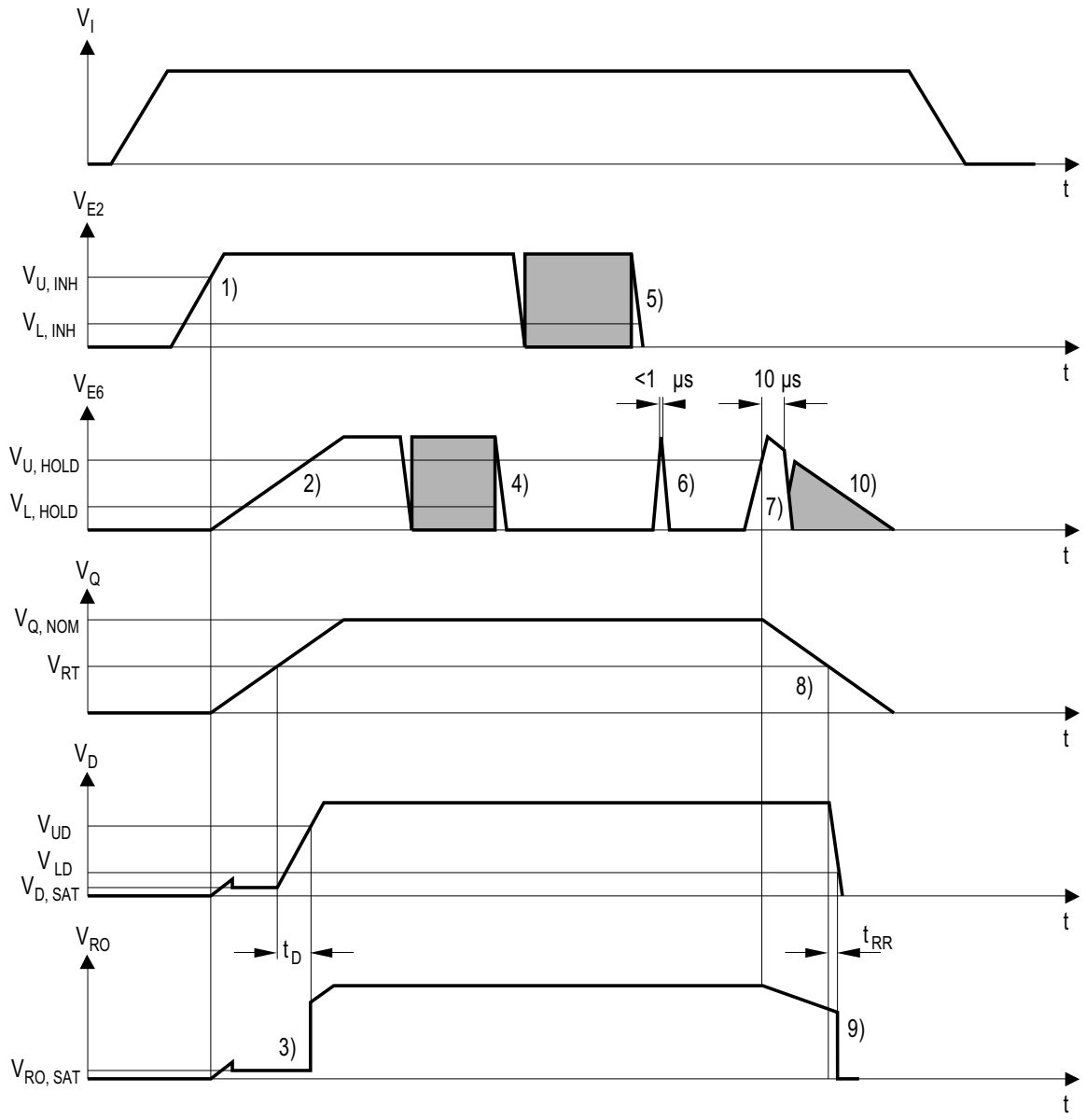
4.3 Inhibit and hold functionality

The device has two logic inputs, E2 and E6. A voltage of V_{E2} greater than 4.0 V applied to E2 pin (Inhibit) during for example ignition, turns the device on.
Depending on the voltage on pin E6 (Hold) the device can stay in active state even if V_{E2} goes to low level. This makes it simple to implement a self-holding circuit without external components. **Table 7** shows the truth table for the turn-on turn-off logic controlled by the inputs voltages on E2 (Inhibit) and E6 (Hold).

Table 7 Truth table for Turn-ON/Turn-OFF logic

E2, Inhibit [1]	E6, Hold [2]	V_Q	Remarks
L	X	OFF	Initial state
H	X	ON	Regulator switched on via Inhibit, by ignition for example
H	L	ON	Hold clamped active to ground by controller while Inhibit is still high
X	L	ON	Previous state remains, even ignition is shut off: self-holding state
L	L	ON	Ignition shut off while regulator is in self-holding state
L	H	OFF	Regulator shut down by releasing of Hold while Inhibit remains Low, final state. No active clamping required by external self-holding circuit (µC) to keep regulator in off-state.

1) E2, Inhibit: enable function, active high
2) E6, Hold: hold and release function, active low



1) Enable active
2) Hold inactive, pulled up by V_Q
3) Power-ON reset
4) Hold active, clamped to GND by external µC
5) Enable inactive, clamped by int. pull-down resistor
6) Pulse width smaller than 1 µs
7) Hold inactive, released by µC
8) Voltage controller shutdown
9) Output-low reset
10) No switch on via V_{E6} possible after E6 was released to $V_{E6} > V_{E6, rel}$ for more than 4µs

Figure 4 Enable and hold behavior

4.3.1 Electrical characteristics inhibit and hold function

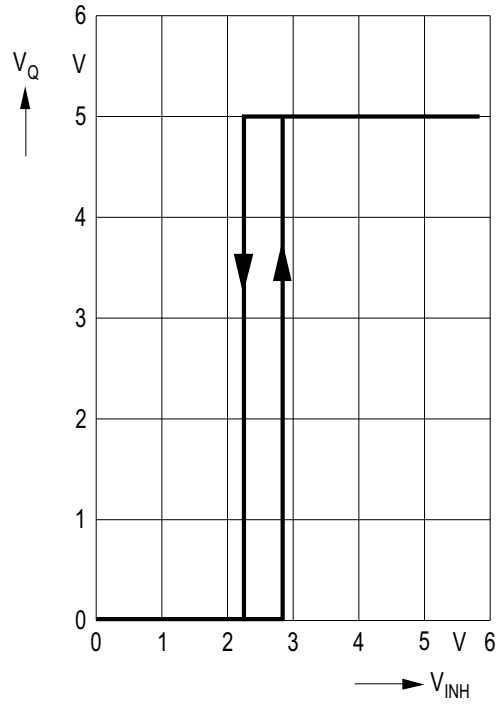
Table 8 Electrical characteristics inhibit and hold function

V_I = 13.5 V; -40 °C < T_j < 125 °C; V_{E2} > 4 V (unless specified otherwise)

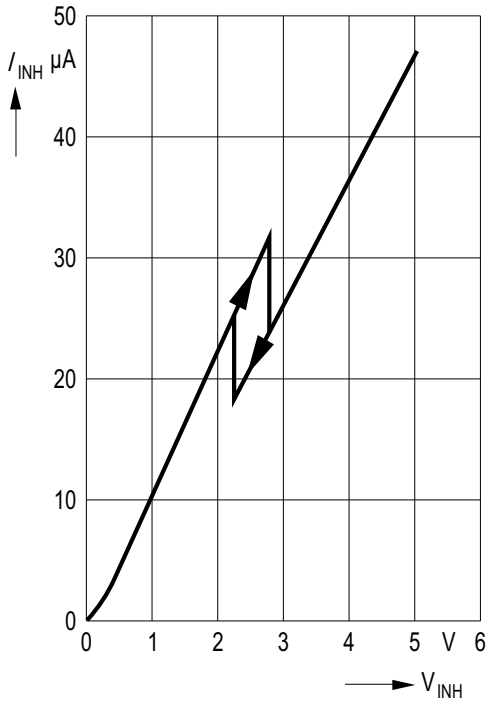
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Turn-on voltage	$V_{U,INH}$	–	3	4	V	Device turned on	P_4.4.1
Turn-off voltage	$V_{L,INH}$	2	–	–	V	Device turned off	P_4.4.2
Pull-down resistor	R_{INH}	50	100	200	kΩ	–	P_4.4.3
Hysteresis	ΔV_{INH}	0.2	0.5	0.8	V	–	P_4.4.4
Input current	I_{INH}	–	35	100	µA	V_{INH} = 4 V	P_4.4.5
Hold voltage	$V_{U,HOLD}$	30	35	40	%	Referred to V_Q	P_4.4.6
Turn-off voltage	$V_{L,HOLD}$	60	70	80	%	Referred to V_Q	P_4.4.7
Pull-up resistor	R_{HOLD}	20	50	100	kΩ	–	P_4.4.8

4.3.2 Typical performance characteristics inhibit

Output voltage V_Q versus inhibit voltage V_{INH}



Inhibit current I_{INH} versus inhibit voltage V_{INH}



5 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

5.1 Application diagram

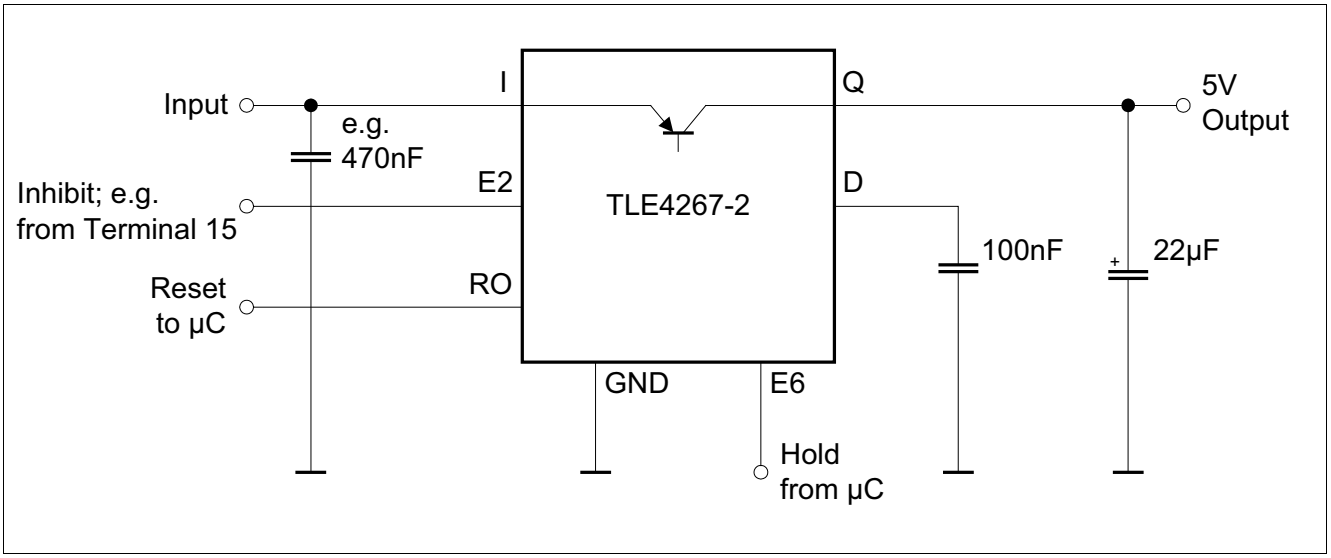


Figure 5 Application diagram

Note: This is a very simplified example of a application circuit. The function must be verified in the real application.

5.2 Selection of external components

The input capacitor C_I is necessary for compensation of line influences. The resonant circuit consisting of lead inductance and input capacitance can be damped by a resistor of approx. 1 Ω in series with C_I.

The output capacitor C_Q is necessary for the stability of the regulating circuit. Stability is guaranteed at values of greater than 22 µF and an ESR of less than 3 Ω within the operating temperature range.
An example of a test circuit is shown in **Figure 6**.

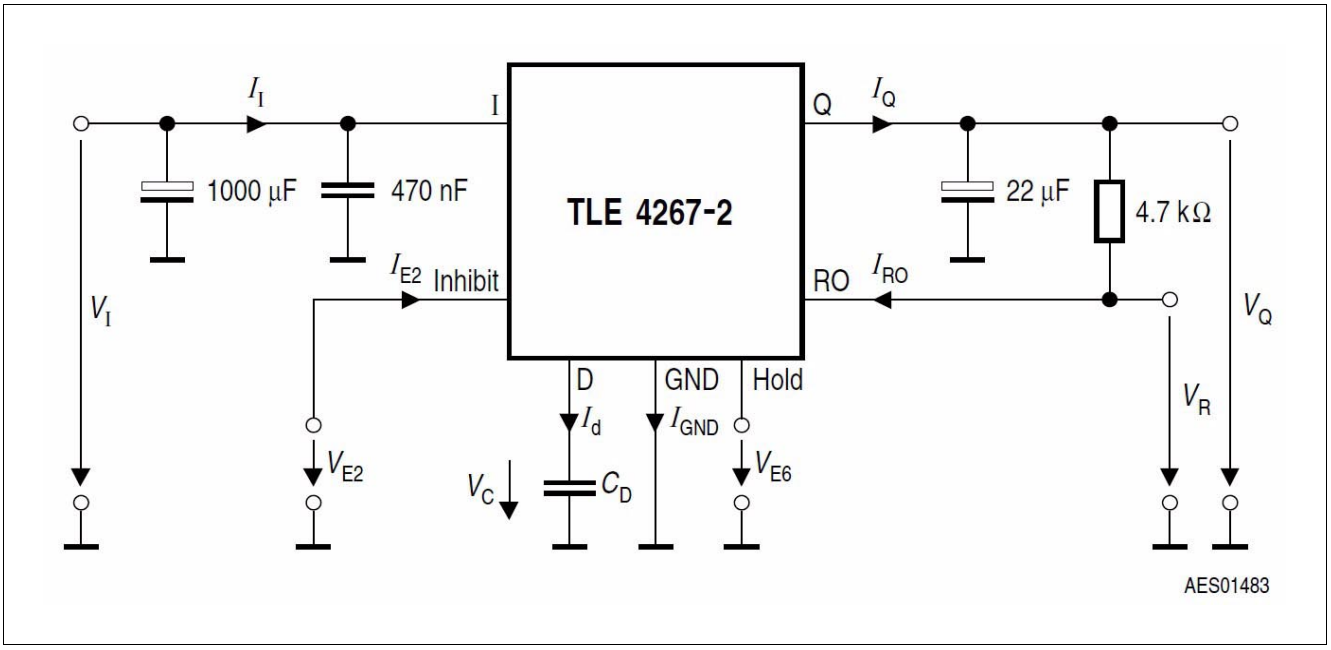


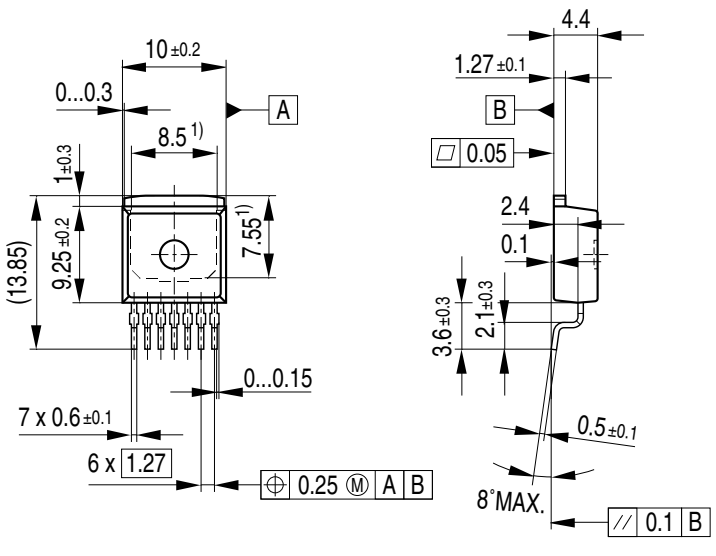
Figure 6 Test circuit

Note: This is a very simplified example of a test circuit. The function must be verified in the real application.

5.3 Further application information

- For further information you may contact **http://www.infineon.com/**

6 Package information



1) Typical
Metal surface min. X = 7.25, Y = 6.9
All metal surfaces tin plated, except area of cut.

Figure 7 PG-TO220-7[1] (Plastic Small Outline Transistor)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (that is Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

1) Dimensions in mm

7 Revision history

Revision	Date	Changes
1.1	2023-06-19	• Updated layout and template. • Text reformulations and restructuring (editorial) • Moved the ESD rating from features into the absolute max ratings section • Moved C_Q and $C_{Q(ESR)}$ requirements from pin definition table to functional range • Removed reference to discontinued PG-TO263-7 package
1.0	2012-04-03	Initial datasheet for TLE4267-2

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