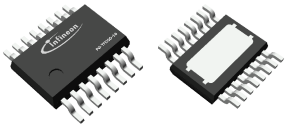
LITIX™ Interior

Features



- 32-bit Arm® Cortex®-M23 core
  - One clock per machine cycle architecture
  - Single cycle multiplier
  - Hardware divider
- On-chip memory
  - 32 kB Flash (including 1000 TP memory)
  - 576 Bytes 1000 TP memory
  - 3 kB SRAM
  - Boot ROM for startup firmware and Flash routines
- On-chip oscillator and on-chip debug support via 2-wire SWD

RoHS

AEC Qualified

Potential applications

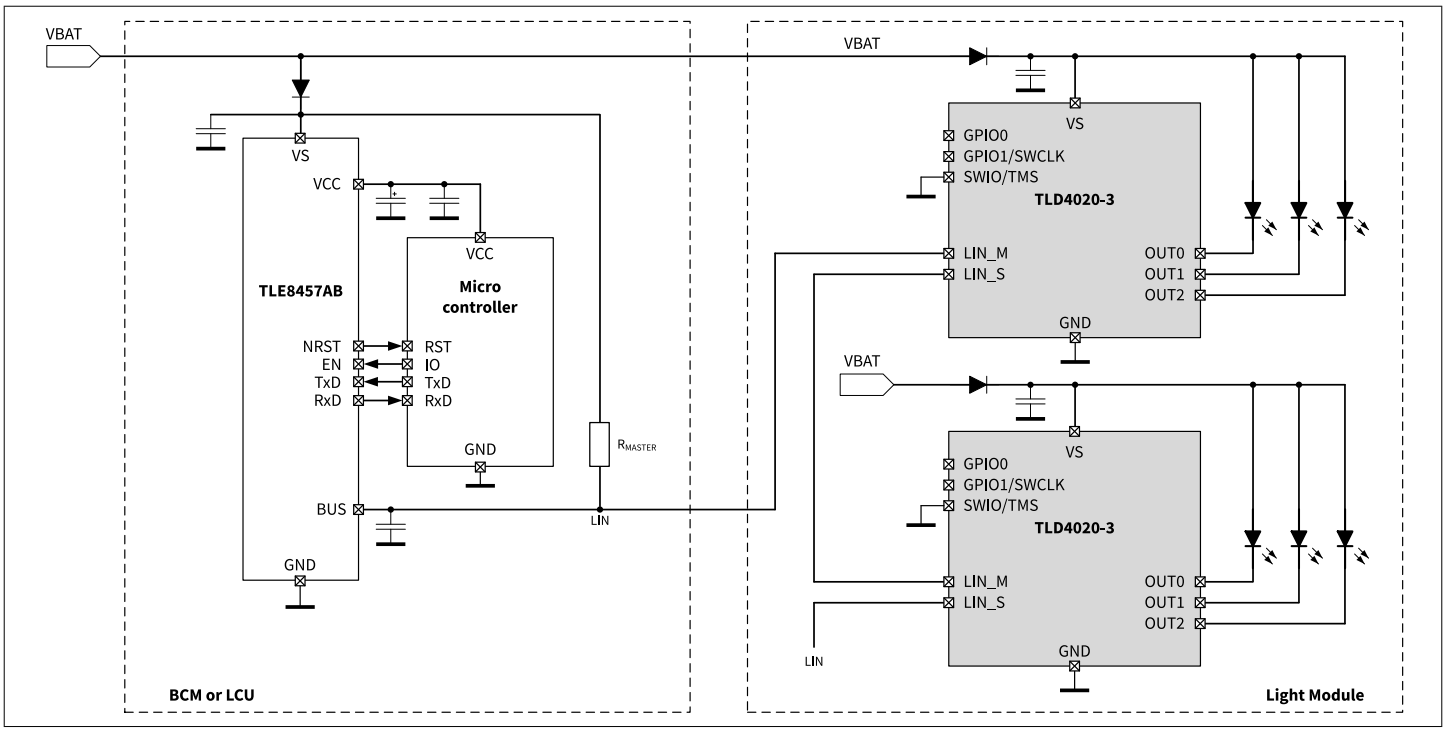
- Three channel LED driver for automotive interior lighting applications with LIN interface
- Contour lighting using a single light source with constant or slowly changing light patterns
- Functional and switch illumination
- Surface lighting requiring single LED

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100, Grade 1.

Description

The TLD4020-3ET is a three channel device with integrated and protected output stages. It is designed to control RGB LEDs with a current up to 51.5 mA as linear current sink (LCS). The power stages can be configured in parallel for higher load currents. Each individual power output stage is configurable via a 5-bit current set value. In total 3 independent and individual PWM configurations can be set. A LIN interface is used for programming (via bootloader), control and diagnostic feedback.



Product type	Package	Marking
TLD4020-3ET	PG-TFDSO-16	402

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1 Product description

1.1 Product summary

Table 1 Product summary

Parameter	Symbol	Values
Power supply operating voltage	$V_{S(OP)}$	5.5 V ... 29 V
Maximum output voltage	V_{OUT_max}	40 V
Nominal load current (Linear current sink)	I_{L_nom}	51.5 mA
Output current accuracy T_J = 25°C	A_{IOUT_25}	±5%
Minimum dropout voltage	$V_{DR,all}$	1.2 V, I_{OUT} ≥ 90% of 51.5 mA

1.2 Additional features

- Optimized for electromagnetic compatibility (EMC)
- Optimized for low electromagnetic emission (EME)
- Optimized for high immunity against electromagnetic interference (EMI)
- Green product (RoHS compliant)
- Automotive temperature range of -40°C to 125°C
- One full duplex serial interface (UART), with LIN support
- One ISO 17987-4 series LIN transceiver
- LIN bootstrap loader to program the flash via LIN (LIN BSL)
- Three integrated low-side current sinks
- 11-bit differential A/D converter
- Integrated 11-bit digital temperature sensor (DTS)
- One GPIO controllable via PWM Engine to drive external circuitry

2 Block diagram and terms

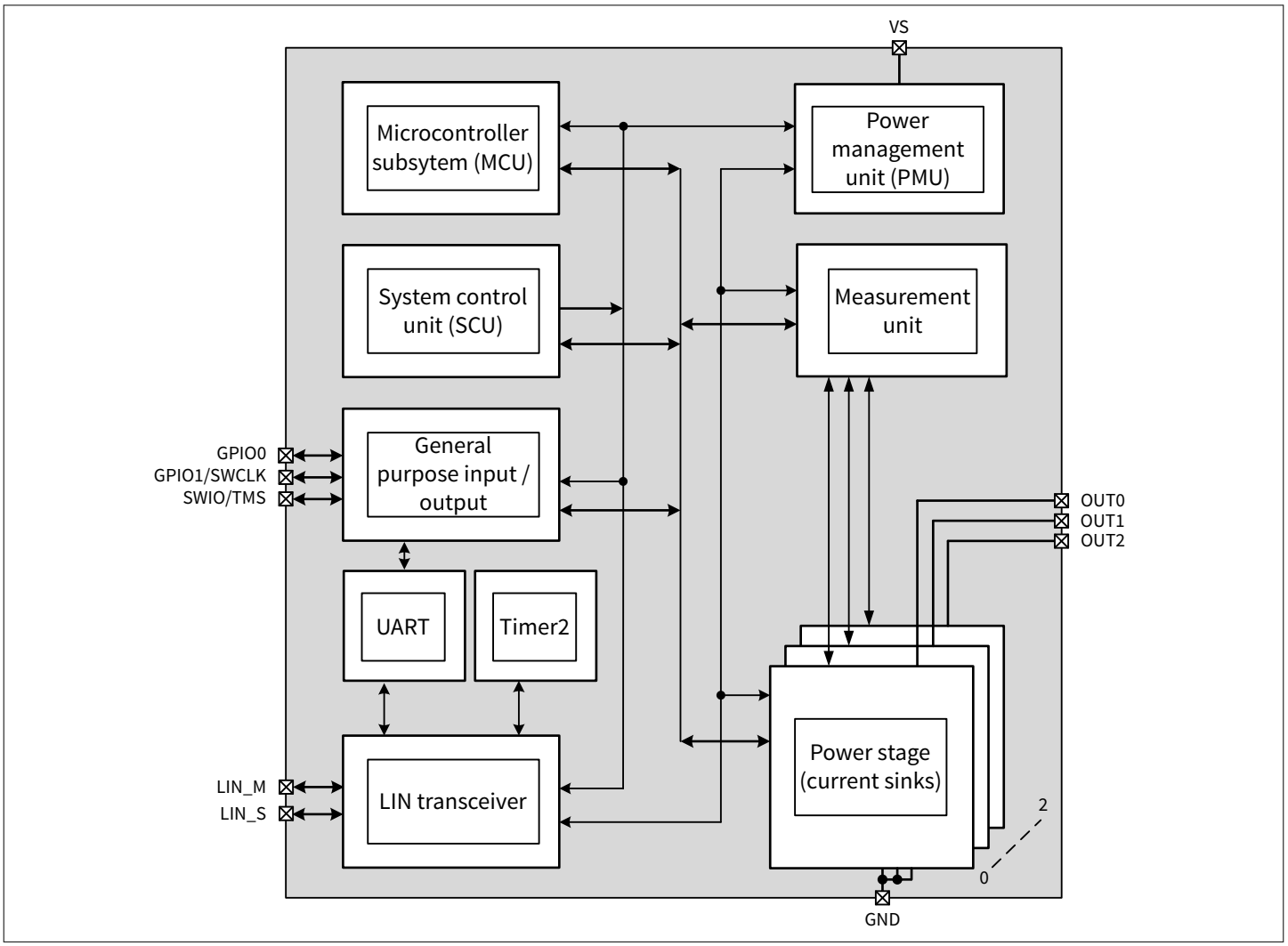


Figure 1 Block diagram of TLD4020-3ET

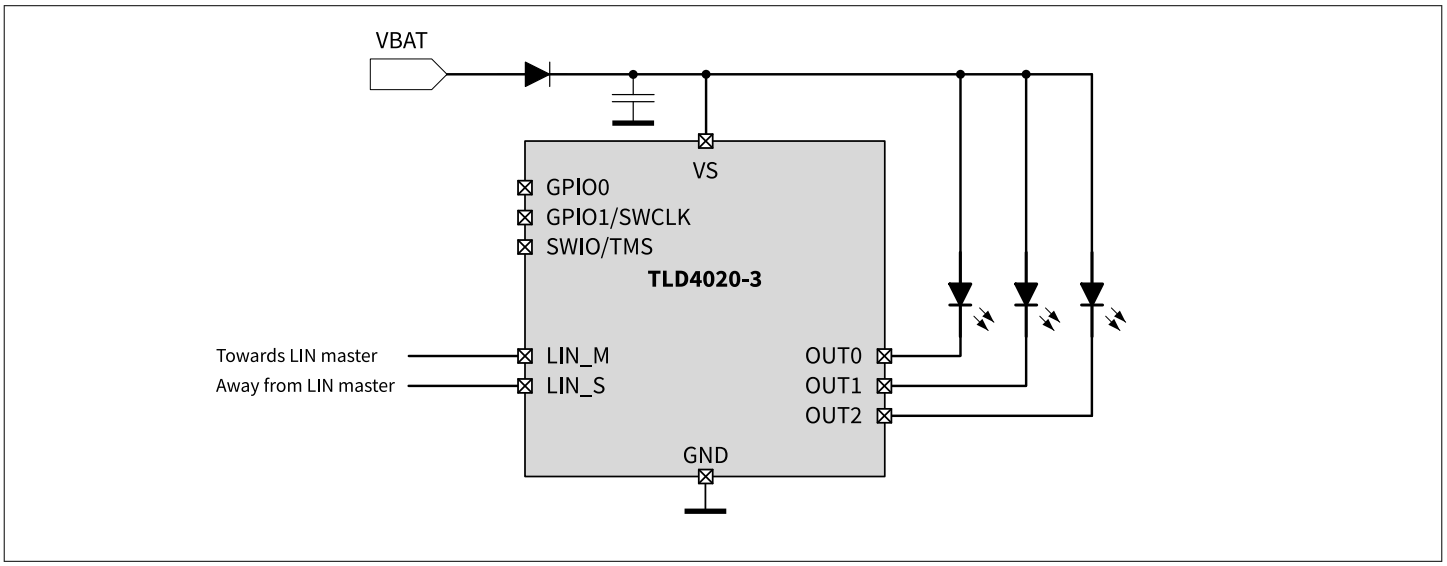


Figure 2 Application block diagram (simplified)

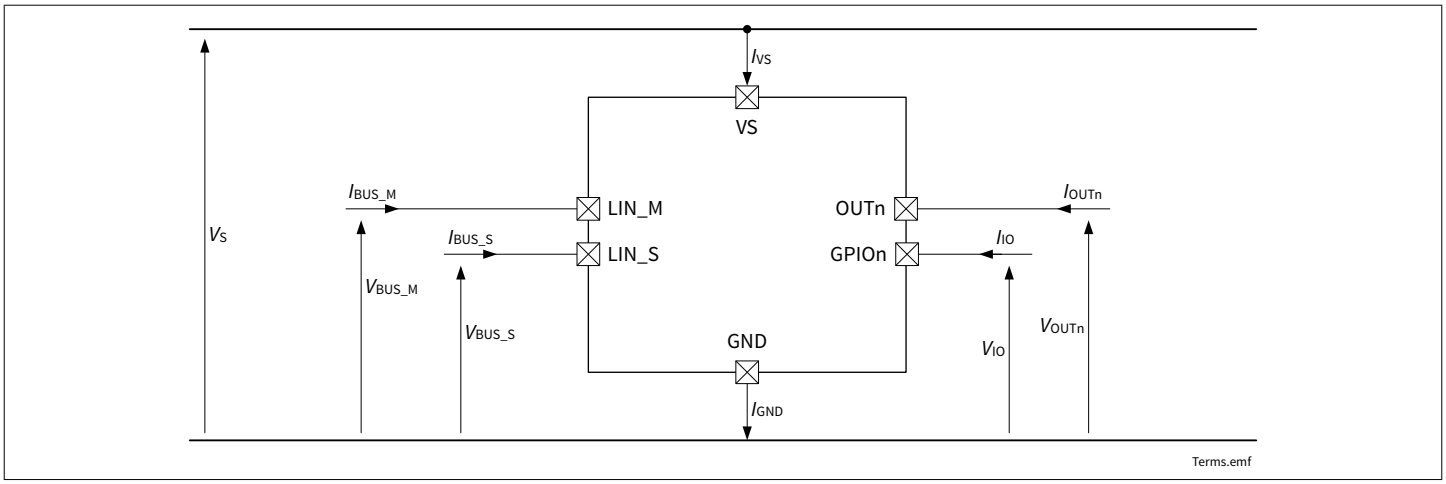


Figure 3 Terms and definitions

OUTn: n denotes the channel number from 0 to 2
GPIOn: n denotes the GPIO number from 0 to 1

3 Pin configuration

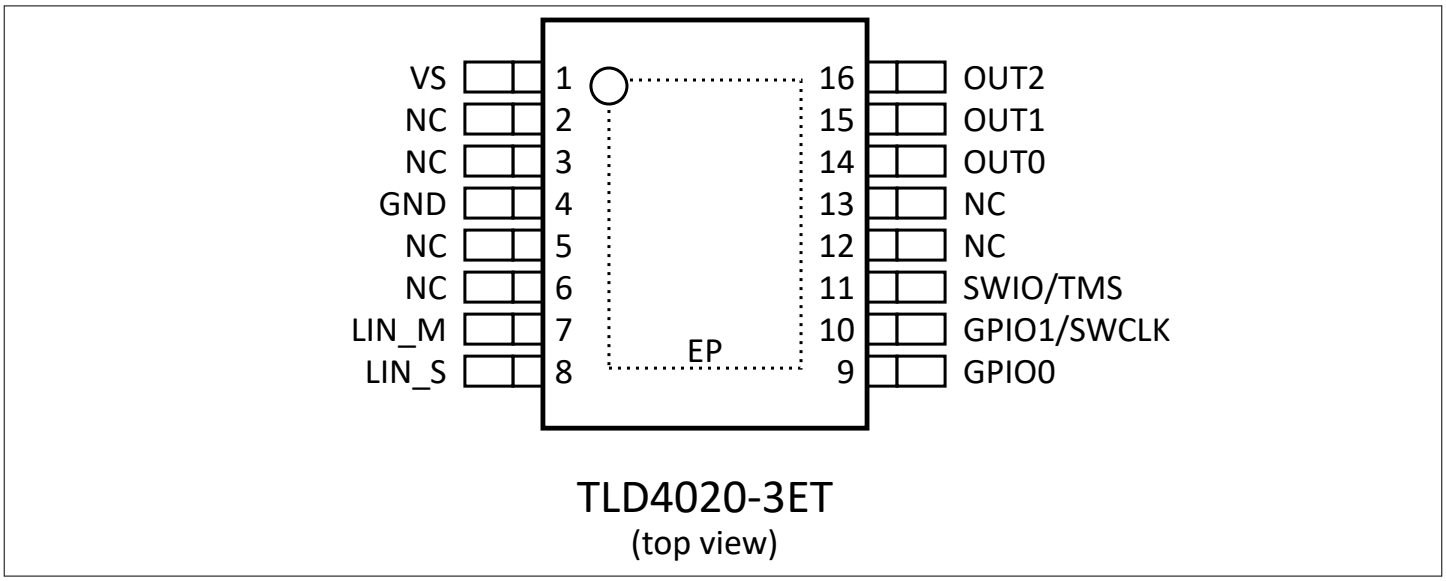


Figure 4 PG-TFDSO-16

Table 2 Pin definitions and functions

Pin	Symbol	Function
1	VS	**Power supply voltage** Battery supply input
2, 3	NC	Not connected
4	GND	**Ground** Ground potential. Connect externally close to the chip
5, 6	NC	Not connected
7	LIN_M	**LIN master** LIN connection towards direction of the master device
8	LIN_S	**LIN slave** LIN connection away from master device
9	GPIO0	**GPIO/RXD** Can be used for voltage measurements or as general-purpose input/output. Can be used as a wake-up source from sleep mode. Can be driven by dedicated PWM signal. Can be set as UART receive data input (RXD)
10	GPIO1/SWCLK	**GPIO/SWD clock/TXD** Can be used for voltage measurements or as general-purpose input/output. Can be used as a wake-up source from sleep mode. Can be set as UART transmit data output (TXD) Serial Wire Debug clock
11	SWIO/TMS	**SWD IO/TMS** Serial Wire Debug input/output TMS pin for debug mode entry

(table continues...)

Table 2 (continued) Pin definitions and functions

Pin	Symbol	Function
12, 13	NC	Not connected
14...16	OUT0...OUT2	**Output channel** Open-drain linear current sink. Connect to the target load
–	EP	**Exposed pad** Connect to external heat spreading copper area connected to electrical GND. Recommendation is to use the GND layer of a PCB with thermal vias. The exposed pad does not replace the electrical GND pin

4 General product characteristics

4.1 Absolute maximum ratings

Table 3 Absolute maximum ratings

T_J = -40°C to +150°C; all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified) [1)].

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply pins							
Power supply voltage	V_S	-0.3	–	40	V	Suppressed load dump acc. to ISO16750-2	PRQ-142
Output pins							
Power output voltage	V_{OUT}	-0.3	–	40	V	–	PRQ-3150
Power output current	I_{OUT}	0	–	56.65	mA	–	PRQ-495
GPIO pins							
Voltage at pin GPIO0, GPIO1, TMS	V_{IO}	-0.3	–	5.5	V	–	PRQ-898
Current at pin GPIO0, GPIO1, TMS	I_{IO}	0	–	4	mA	–	PRQ-3162
LIN							
Voltage at pin LIN_M, LIN_S	V_{BUS}	-27	–	40	V	–	PRQ-1138
Temperatures							
Junction temperature	T_J	-40	–	150	°C	–	PRQ-144
Ambient temperature	T_A	-40	–	125	°C	–	PRQ-145
ESD susceptibility							
ESD susceptibility all pins (HBM)	$V_{ESD(HBM)}$	-2	–	2	kV	ESD susceptibility, Human Body Model "HBM" according to AEC Q100-002	PRQ-150
ESD susceptibility LIN vs GND (HBM)	$V_{ESD(HBM)_GND}$	-8	–	8	kV	ESD susceptibility, Human Body Model "HBM" according to AEC Q100-002	PRQ-151
ESD susceptibility all pins (CDM)	$V_{ESD(CDM)}$	-500	–	500	V	ESD susceptibility, Charged Device Model "CDM" according to AEC Q100-011 Rev D	PRQ-152

(table continues...)

Table 3 (continued) Absolute maximum ratings

T_J = -40°C to +150°C; all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified) [1].

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ESD susceptibility corner pins (CDM)	$V_{ESD(CDM)_CR}$	-750	–	750	V	ESD susceptibility, Charged Device Model "CDM" according to AEC Q100-011 Rev D	PRQ-153

1) Not subject to production test - specified by design

***Note**:* *1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional range

Table 4 Functional range

T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified) [1].

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply pins							
Supply voltage operating range	$V_{S(OP)}$	5.5	13.5	29	V	–	PRQ-162
Extended supply voltage operating range	$V_{S(OP,EXT)}$	29	–	40	V	Allowed for t ≤ 400ms; with parameter deviation	PRQ-3149
Supply voltage for LIN transceiver	$V_{S(LIN)}$	5.5	13.5	18	V	–	PRQ-967
VS capacitor range	C_{VS}	2	–	–	µF	2) 3)	PRQ-164
Temperatures							
Junction temperature	T_J	-40	–	150	°C	–	PRQ-529
Power stage pins							
Output voltage operating range	$V_{OUT(OP)}$	0	–	29	V	–	PRQ-897
Output current per channel	I_{OUT}	0	–	51.5	mA	–	PRQ-532
Output capacitor range	C_{OUT}	0	–	10	nF	–	PRQ-534

(table continues...)

Table 4 (continued) Functional range

T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified) [1].

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output inductance range	L_{OUT}	0	–	0.5	µH	C_{OUT} < 10 nF	PRQ-536

1) Not subject to production test - specified by design
2) Ceramic capacitor is recommended
3) When DC voltage is applied to a ceramic capacitor, the effective capacitance is reduced due to DC bias effect. The table above therefore lists the minimum value as capacitance. In order to meet the minimum capacitance requirement, the nominal value of the capacitor may have to be scaled accordingly to take the drop of capacitance into account for a given DC voltage at the outputs of regulators

4.3 Thermal resistance

Table 5 Thermal resistance

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Thermal characterization parameter junction to top	Ψ_{JTOP}	–	10	–	K/W	1)	PRQ-3154
Thermal resistance junction to soldering point	R_{thJSP}	–	10	–	K/W	1) Simulated at exposed pad	PRQ-3155
Thermal resistance junction to ambient	R_{thJA}	–	40	–	K/W	1)	PRQ-3156

1) Not subject to production test - specified by design

***Note**: Specified R_{th} values are according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the product (chip + package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. Simulation done at T_{AMB} = 85°C with all channels on, $P_{DISSIPATION}$ = 1.5 W and a homogeneous temperature distribution across the device.*

5 Power management unit (PMU)

5.1 Features overview

- Power management control with diagnosis
- System mode control (startup, sleep, active, and failsleep in case of severe system failures)
- Wake configuration and management
- Reset management according to the system modes
- Windowed watchdog providing a highly reliable and safe way to recover from software or hardware failures
- Configurable with SFRs. Supports error condition signaling to the MCU via interrupt
- Data retention registers available in all PMU modes
- Linear voltage regulator VDDP for internal analog/digital logic supply
- Linear voltage regulator VDDC for internal digital logic supply

5.2 Block diagram

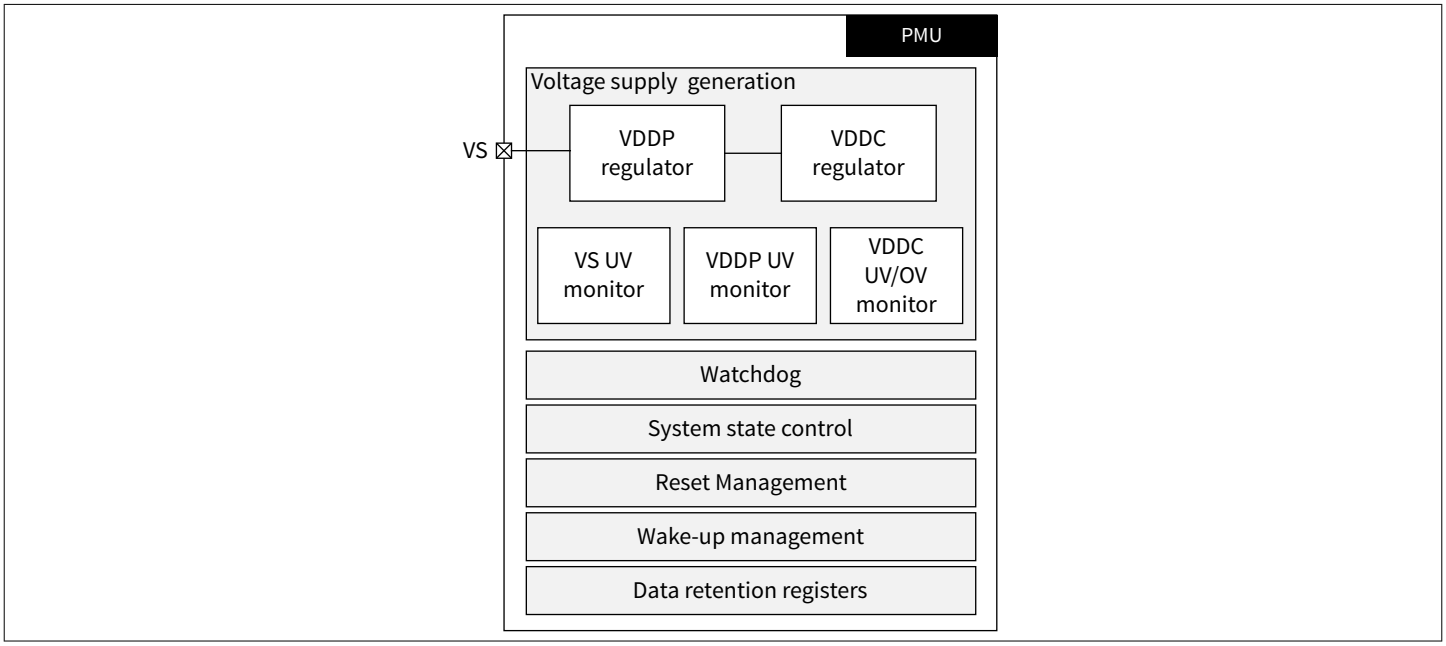


Figure 5 PMU block diagram

5.3 Electrical characteristics PMU

5.3.1 PMU operating conditions

Table 6 Electrical characteristics

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values reference conditions: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Power supply undervoltage monitor	V_{SUV_MON}	4.8	–	5.35	V	V_S voltage falling	PRQ-3157

(table continues...)

Table 6 (continued) Electrical characteristics

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values reference conditions: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Power-down voltage	V_{S_PD}	–	–	3.6	V	V_S voltage falling	PRQ-479

5.3.2 Current consumption

Table 7 Electrical characteristics

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values reference conditions: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Active mode current consumption	$I_{VS(ACTIVE)}$	–	5.5	10	mA	Active mode: SYS0_CLK = 40 MHz, CPU_CLK = 20 MHz. MCU executing code from NVM, MCU subsystem only, all other external peripherals disabled	PRQ-481
Sleep mode current consumption	$I_{VS(SLEEP)}$	–	20	50	µA	T_J = -40 °C to 85 °C Sleep mode V_S = 7.3 V to 18 V $V_{BUS} = V_{BUS_REC}$	PRQ-480
Sleep mode current consumption	$I_{VS(SLEEP)}$	–	150	200	µA	T_J = -40 °C to 85 °C Sleep mode V_S = 3.6 V to 7.3 V $V_{BUS} = V_{BUS_REC}$	PRQ-2893
Fail-sleep mode current consumption	$I_{VS(SLEEP)}$	–	20	50	µA	T_J = -40 °C to 85 °C Fail-sleep mode V_S = 7.3 V to 18 V $V_{BUS} = V_{BUS_REC}$	PRQ-2894
Sleep mode current consumption	$I_{VS(SLEEP, LIN_S2G)}$	–	–	1.8	mA	[1] T_J = -40 °C to 85 °C Sleep mode V_S = 7.3 V to 18 V V_{BUS} = 0 V	PRQ-3161

1) Not subject to production test - specified by design

5.3.3 Power supply DC specification

Table 8 Electrical characteristics

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values reference conditions: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Extended input voltage range	V_{S_EXT}	3.6	–	5.5	V	1)	PRQ-2851

1) Not subject to production test - specified by design

5.3.4 System state control

Table 9 Electrical characteristics

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values reference conditions: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Unsupplied to Active mode	$t_{UNSUP2ACT}$	–	–	3.5	ms	1) Time power-up event to first instruction execution in user software or BSL ready	PRQ-3159
Active to Sleep mode	$t_{ACT2SLP}$	–	–	250	µs	Triggered by WFE command	PRQ-835
Sleep to Active mode	$t_{SLP2ACT}$	–	–	2.5	ms	Triggered by a wake-up event	PRQ-2316
Fail-sleep to Active mode	$t_{FSLP2ACT}$	–	–	2.5	ms	1) Triggered by wake-up event	PRQ-2318

1) Not subject to production test - specified by design

6 System control unit (SCU)

6.1 Features overview

The system control unit (SCU) provides the clocks for the MCU and peripherals in all operation modes. Within the SCU the interrupt requests from the peripherals are processed and mapped.

The SCU provides following features:

- Clock sources management
- Clock tree configuration
- Operation mode control
- Interrupt mapping features

6.2 Block diagram

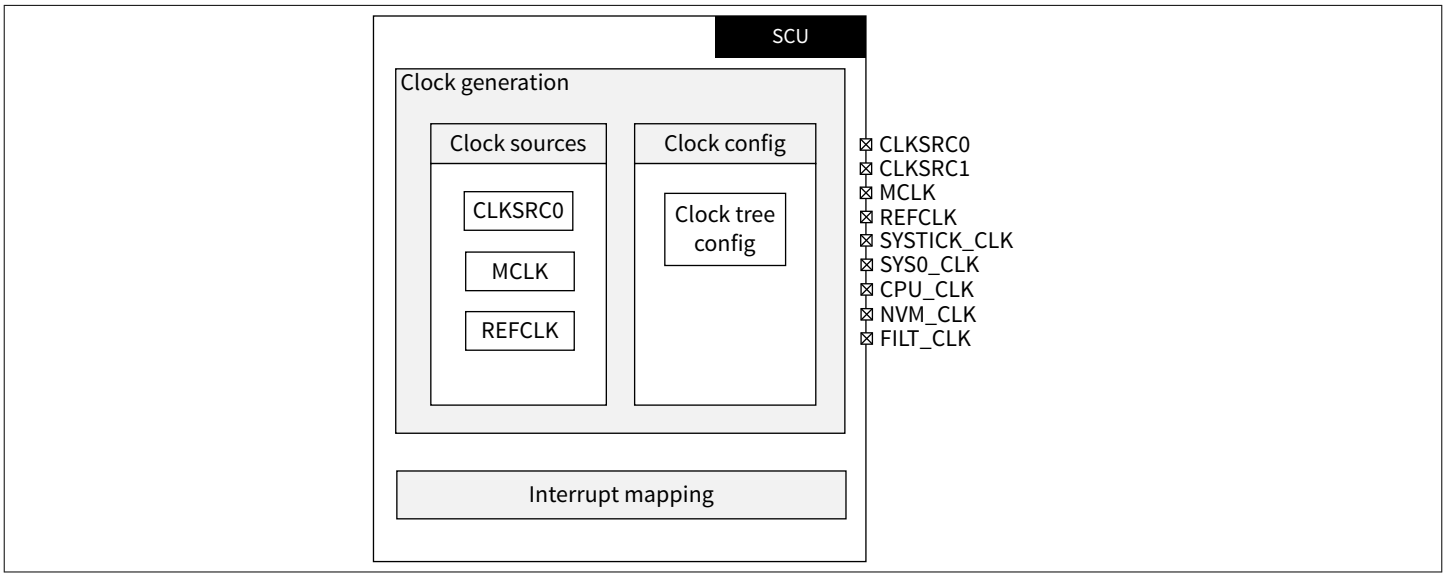


Figure 6 SCU block diagram

6.3 Electrical characteristics SCU

6.3.1 Clock control

Table 10 Electrical characteristics

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values reference conditions: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SYS0_CLK frequency	f_{SYS0_CLK}	39.4	40	40.6	MHz	To be ensured by user configuration	PRQ-3170
Filter clock frequency	f_{FILT_CLK}	1.9	2	2.1	MHz	1) 2) To be ensured by user configuration	PRQ-3103

1) Not subject to production test - specified by design

2) It has to be ensured that the frequency resulting from combined configuration of SYS0_CLK and relevant 1/N clock divider lies within the specified range

6.3.2 Clock sources

Table 11 Electrical characteristics

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values reference conditions: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Clock source 0 frequency	$f_{CLKSRC0}$	39.4	40	40.6	MHz	$T_J \leq 150$ °C	PRQ-2828
Master clock frequency	f_{MCLK}	17	20	23	MHz	1)	PRQ-482
Reference clock frequency	f_{REFCLK}	85	100	115	kHz	1)	PRQ-3132

1) Not subject to production test - specified by design

7 Microcontroller subsystem (MCU)

7.1 Features overview

The Microcontroller subsystem (MCU) consists of a CPU, a memory system, an interrupt system, a debug infrastructure and a system timer.

The MCU provides following features:

- Arm® Cortex®-M23 core with Thumb® and Thumb® -2 instruction set
- Memory system
  - Non-volatile memory (Flash)
  - Volatile data memory (SRAM)
  - Memory access protection
  - Built-in error correction
- Read-only memory (BootROM) providing different functionalities
  - Startup procedure
  - Bootstrap loader (BSL)
  - Flash utilities (API)
- Debug Access Port (DAP) accessible via Serial Wire Debug (SWD)
  - Halt After Reset (HAR) support
  - Four hardware breakpoints
  - Two data watchpoints
  - System memory access
  - Can be disabled for IP protection
- Nested vectored interrupt controller (NVIC)
  - 8 external interrupt inputs
  - Programmable interrupt priority levels
  - Dynamic re-prioritization
- System timer (SYSTICK) with interrupt capability

7.2 Block diagram

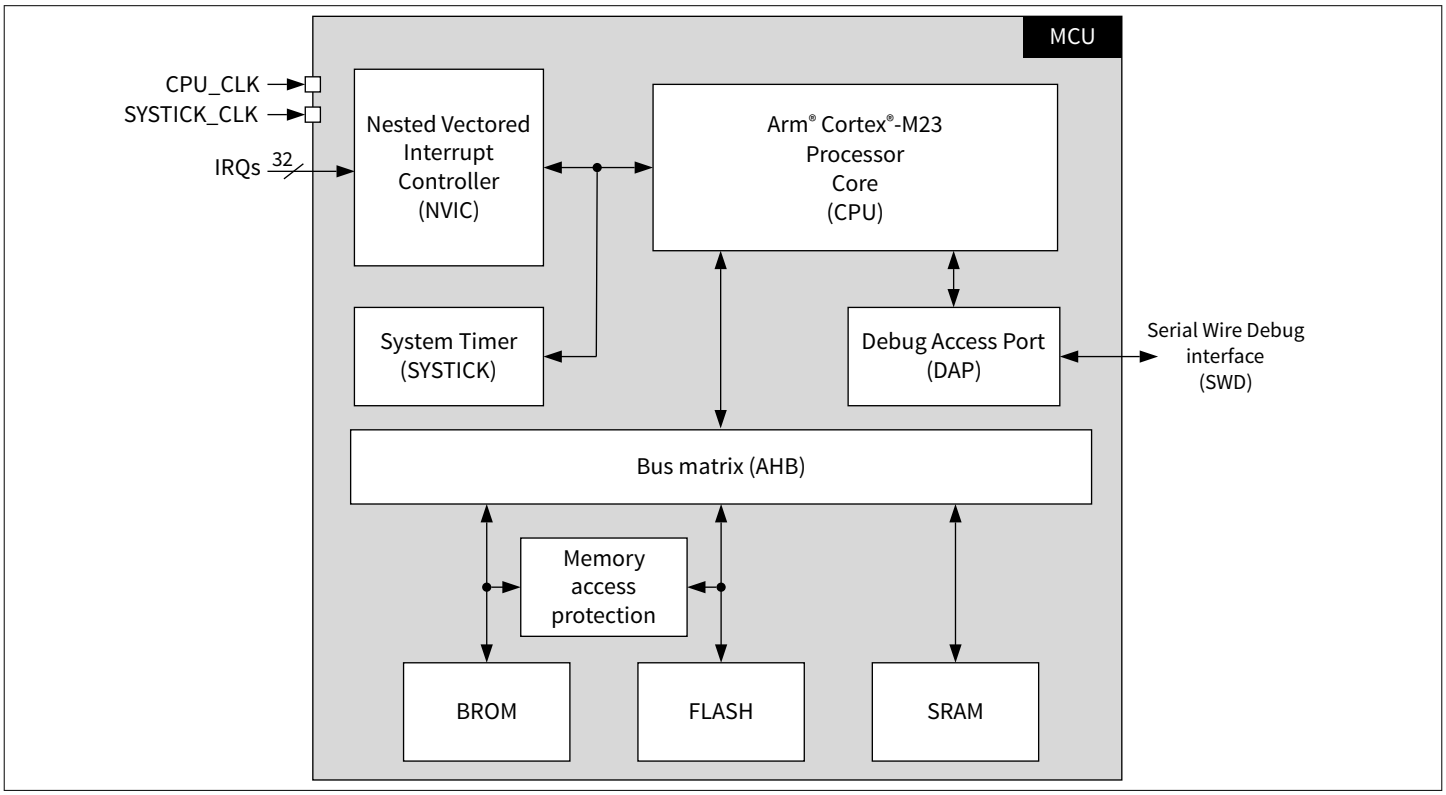


Figure 7 MCU block diagram

7.3 Electrical characteristics NVM

Table 12 Electrical characteristics

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified) [1]. Typical values reference conditions: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
BROM size	n_{BROM}	8	–	–	kB	–	PRQ-140
SRAM size	n_{SRAM}	3	–	–	kB	–	PRQ-137
Flash size	n_{FLASH}	32	–	–	kB	–	PRQ-139
1000TP size	n_{1000TP}	576	–	–	Byte	–	PRQ-141
Write time per page	t_{WR}	–	3	3.5	ms	Page size: 64 bytes	PRQ-2811
Erase time per sector/ page	t_{ER}	4	4.5	–	ms	Sector size: 2 kB	PRQ-2813
Endurance normal	N_{ER}	1000	–	–	cycles	–	PRQ-147
Data retention for normal endurance	t_{RET}	20	50	–	years	–	PRQ-646

1) Not subject to production test - specified by design

8 General purpose input/output (GPIO)

8.1 Features overview

The device provides two general purpose input/output pins GPIO0 and GPIO1. The GPIOs can be used as

- Open drain digital input/output for signaling
- Wake-up source from sleep mode
- Analog input connected to the internal ADC multiplexer for external measurements, for example external NTC/PTC measurements
- GPIO0 as digital output connected to internal PWM Engine to drive external circuitry
- GPIO0 and GPIO1 as respectively digital input connected to UART_RX and digital output connected to UART_TX

The GPIOn pins integrate an internal pull-down function, where the pull-down current is defined by I_{IO_PD}.

The pull-down current can be activated when the pin is configured as a digital input pin and is disabled if the pin is used as an analog input pin.

The GPIOs can be configured via register as analog input pins for external voltage measurements, for example for external NTC/PTC temperature measurements.

The pull-down function is disabled in case the GPIOn is configured as analog input pin.

8.2 Electrical characteristics GPIO

Table 13 Electrical characteristics

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values reference conditions: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
General purpose input / output							
IO low voltage	V_{IO_L}	0	–	0.8	V	–	PRQ-853
IO high voltage	V_{IO_H}	2.0	–	–	V	Internally clamped if the input current is ≤ I_{IO} and pin is configured as input	PRQ-854
Digital input voltage range	V_{DIN}	0	–	5	V	–	PRQ-881
Input pull-down current	I_{IO_PD}	3	10	25	µA	V_{IO} = 5 V; configured as digital input	PRQ-856
Input leakage current	I_{IL}	-1	–	1	µA	V_{IO} = 4 V; configured as analog input	PRQ-857
Output impedance	R_{IO}	–	–	200	Ω	V_{IO} = 0.4 V; configured as digital output low	PRQ-3163
Filter time for GPIO wake-up	t_{WK_IO}	4	–	32	µs	1) Filter time can be adjusted via register	PRQ-928

1) Not subject to production test - specified by design

9 Measurement unit

9.1 Features overview

Measurement unit includes:

- 11-bit ADC with 3 inputs allowing measurement of LED forward voltage
- Two inputs for GPIO voltage measurement
- 11-bit digital temperature sensor (DTS) for monitoring the chip temperature
- 11-bit supply monitoring

9.2 Electrical characteristics Measurement unit

Table 14 Electrical characteristics

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values reference conditions: V_S = 13.5 V, T_J = 25°C [1) 2)]

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ADC							
Conversion resolution	n_{VRES}	11	–	–	Bit	12-bit with oversampling feature enabled	PRQ-900
Differential nonlinearity error	*DNL*	-1	–	2.5	LSB	Oversampling disabled	PRQ-902
Integral nonlinearity	*INL*	-4	–	4	LSB	Oversampling disabled	PRQ-903
Offset	ADC_{offset}	-7	–	7	LSB	Oversampling disabled	PRQ-904
Gain error	ADC_{gain}	-1.5	–	1.5	%	Oversampling disabled	PRQ-905
Sampling rate	f_S	250	–	–	kS/s	[3)]	PRQ-906
DTS							
DTS absolute accuracy	A_{DTS_abs}	-10	–	+10	K	–	PRQ-913

1) ADC results compensated by gain and offset values of config. sector
2) For DTS refer to PRQ-913
3) Not subject to production test - specified by design

10 Power stage

10.1 Features overview

The Power stage provides following features:

- Three open-drain linear current sink output power stages
- Three individually configurable start and stop PWM compare registers to configure the duty cycle and phase shift
- One master PWM frequency f_{PWM}
- Output current individually configurable for each channel
- Parallel output operation
- Integrated thermal overload protection
- Integrated short to ground detection

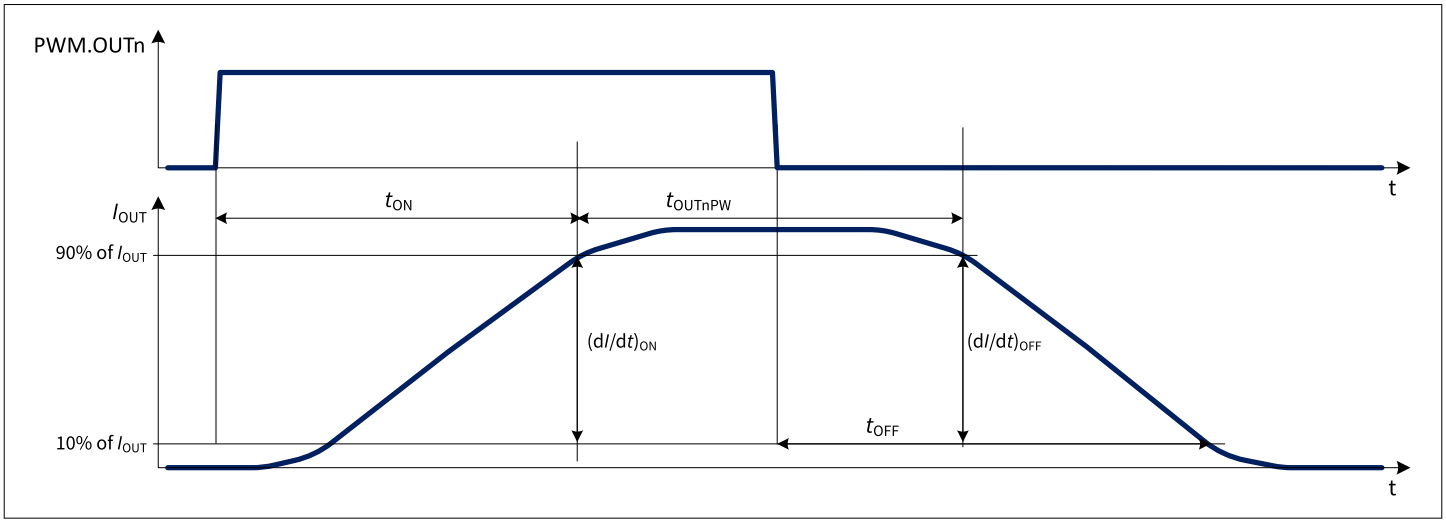


Figure 8 Output stage timing definition

10.2 Electrical characteristics Power stage

Table 15 Electrical characteristics

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values reference conditions: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Leakage currents							
Output leakage current	$I_{OUT-LEAK_85}$	–	–	3	µA	$T_J \leq 85°C$	PRQ-365
Output leakage current	$I_{OUT-LEAK}$	–	–	7	µA	$T_J \leq 150°C$	PRQ-366
Pull-up resistor at OUTn	R_{PU}	13.5	20	33	kΩ	Active mode; (V_S - V_{OUT}) = 1.5 V Enabled via register	PRQ-3152

(table continues...)

Table 15 (continued) Electrical characteristics

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values reference conditions: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output current accuracy and drop-out voltage							
Output current accuracy	A_{IOUT_25}	-5	–	5	%	$T_J \geq 25°C$; full scale range, where 5.0 mA ≤ I_{OUT} ≤ 51.5 mA	PRQ-367
Output current accuracy	A_{IOUT}	-10	–	10	%	-40°C ≤ T_J < 150°C; full scale range, where 5.0 mA ≤ I_{OUT} ≤ 51.5 mA	PRQ-369
Output current channel matching	I_{OUTn}, I_{OUTn+1}	-5	–	5	%	$(I_{OUTn}-I_{average})/I_{average}$, full scale range, where 5.0 mA ≤ I_{OUT} ≤ 51.5 mA	PRQ-372
Drop out voltage - all channels active	$V_{DR,all}$	1.2	–	–	V	$T_J \leq 150°C$, all channels active, $I_{OUT} \geq 90\%$ of 51.5 mA	PRQ-376
PWM engine							
Number of PWM channels	n_{PWM_CH}	3	–	–	–	1)	PRQ-379
PWM clock prescaler	n_{PWM_PS}	1	1	64	–	1) Integer value	PRQ-2796
PWM resolution	n_{PWM}	16	–	–	Bit	1)	PRQ-381
PWM frequency	f_{PWM}	–	–	2500	Hz	1)	PRQ-2979
PWM frequency drift	f_{DRIFT}	-1	–	1	%	1) -20°C ≤ T_J < 125°C	PRQ-382
PWM output timing							
PWM turn on time (fast)	t_{ONfast}	–	300	900	ns	Fast switching mode; I_{OUT} = 90% of 30.0 mA; see Figure 8	PRQ-385
PWM turn off time (fast)	$t_{OFFfast}$	–	300	900	ns	Fast switching mode; I_{OUT} = 10% of 30.0 mA; see Figure 8	PRQ-393
PWM turn on time (normal)	$t_{ONnormal}$	15	20	25	µs	Normal switching mode; I_{OUT} = 90% of 51.5 mA; see Figure 8	PRQ-387
PWM turn off time (normal)	$t_{OFFnormal}$	15	20	25	µs	Normal switching mode; I_{OUT} = 10% of 51.5 mA; see Figure 8	PRQ-395

(table continues...)

Table 15 (continued) Electrical characteristics

V_S = 5.5 V to 29 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values reference conditions: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Current rise slew rate (normal)	dI/dt_{ON}	1.8	2.6	3.34	mA/µs	Normal switching mode; I_{OUT} rising from 10% to 90% of 51.5 mA; see Figure 8	PRQ-389
Current falling slew rate (normal)	dI/dt_{OFF}	-3.34	-2.6	-1.8	mA/µs	I_{OUT} falling from 90% to 10% of 51.5 mA; see Figure 8	PRQ-391
Protection							
Thermal shutdown temperature	$T_{J_SD_LCS}$	165	175	200	°C	1)	PRQ-399
Thermal shutdown hysteresis	$\Delta T_{J_SD_LCS}$	5	10	15	K	1)	PRQ-400

1) Not subject to production test - specified by design

11 UART

11.1 Features overview

UART module provides the following features:

- Full-duplex asynchronous modes
  - 8-bit data frames, LSB first
  - Fixed or variable baud rate
- Receive buffered (1 byte)
- Interrupt generation on the completion of a data transmission or reception
- Baud rate generator with fractional divider for generating a wide range of baud rates, such as 9.6 kbit/s, 19.2 kbit/s, 115.2 kbit/s
- LIN support: hardware logic for break and sync byte detection
- LIN support: connected to timer channel for synchronization to LIN baud rate (autobaud)
- Possibility to expose the module to GPIOs

The following figure shows the standard UART byte field consisting of a start bit, eight data bits and one stop bit. This structure is the basis for data transfer between communication partners. The LSB of the data is transmitted first and the MSB last. The start bit is encoded as a low and the stop bit is encoded as a high bit.

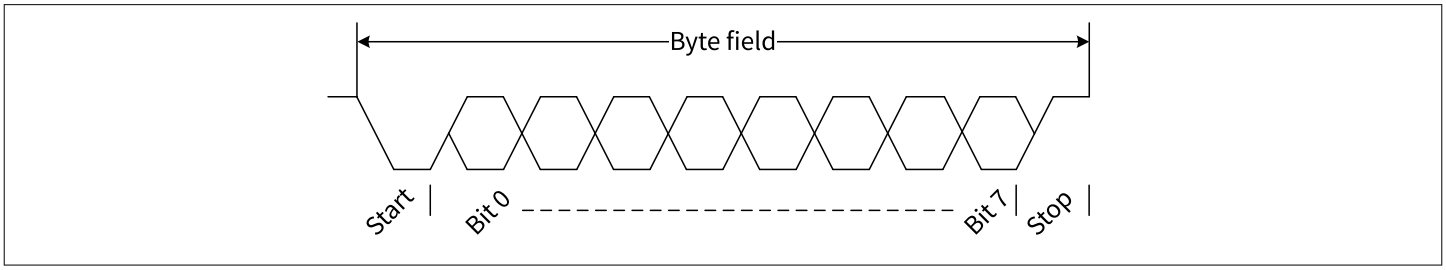


Figure 9 UART byte field

The following baud rates can be configured via register:

Supported baud rates (bit/s)

- 2 400
- 4 800
- 9 600
- 19 200
- 20 000
- 115 200

12 LIN transceiver

12.1 Features overview

The LIN module is a transceiver for the local interconnect network (LIN) compliant with the LIN2.2 standard, backward compatible to LIN1.3, LIN2.0 and LIN2.1. It operates as a bus driver between the protocol controller and the physical network. The LIN bus is a single wire, bi-directional bus typically used for in-vehicle networks, using baud rates between 2.4 kbit/s and 20 kbit/s. Additionally baud rates up to 115 kbit/s are implemented to support BSL feature.

The LIN module offers several different operation modes, including a LIN sleep mode and the LIN normal mode. The integrated slope control allows to use several data transmission rates with optimized EMC performance. For data transfer at the end of line, a flash mode up to 115 kbit/s is implemented.

The device implements an LIN transceiver according to ISO 17987 series.

General functional features

- Compliant to LIN2.2 standard, backward compatible to LIN2.1, LIN2.0 and LIN1.3

Special features

- Measurement of LIN master baud rate via Timer2
- LIN can be used as generic input/output pin with dedicated register bitfield
- TxD timeout feature (optional, on by default)
- Overcurrent limitation and overtemperature protection
- LIN module fully resettable via global enable bit

Operation modes features

- LIN sleep mode (LSLM)
- LIN receive-only mode (LROM)
- LIN normal mode (LNM)
- High voltage input/output mode (LHVIO)
- Auto-addressing SNPD and NAD via bus shunt method (BSM)

Slope modes features

- Normal slope mode (20 kbit/s)
- Flash mode (115.2 kbit/s)

Wake-up features

- LIN bus wake-up. The wake-up happens on the falling edge of the LIN signal to allow wake-up and decoding of the same frame. It is also possible to enter the sleep mode with LIN dominant (caused by LIN shorted to GND, for example).

12.2 Block diagram

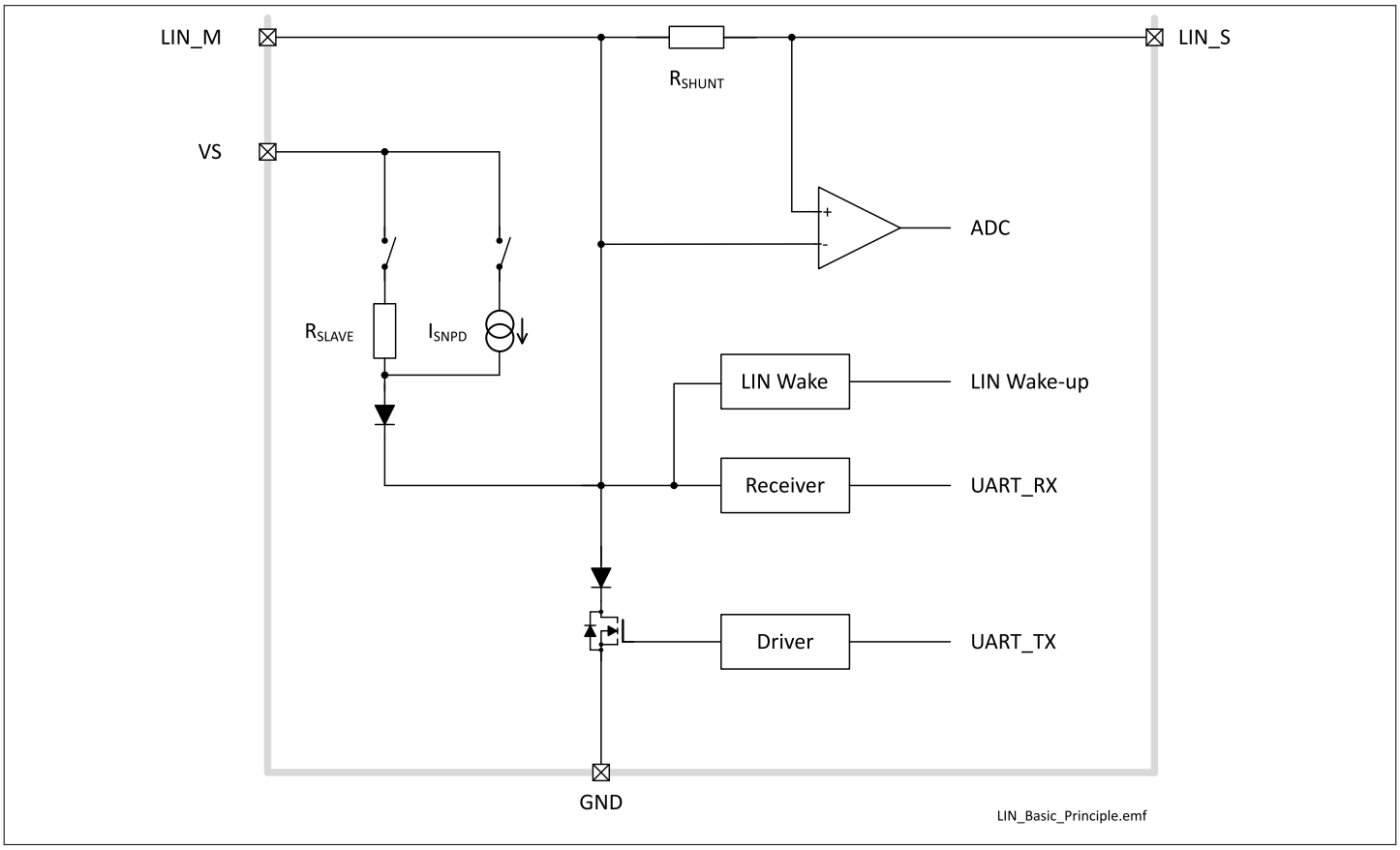


Figure 10 LIN basic principle diagram

12.3 Electrical characteristics LIN transceiver

Table 16 Electrical characteristics

V_S = 5.5 V to 18 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values reference conditions: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Bus receiver interface							
Receiver threshold voltage, recessive to dominant edge	V_{th_dom}	0.4 × V_S	0.45 × V_S	0.53 × V_S	V	SAE J2602	PRQ-644
Receiver dominant state	V_{BUS_DOM}	-27	–	0.4 × V_S	V	ISO 17987-4 (Param 17)	PRQ-645
Receiver threshold voltage, dominant to recessive edge	V_{th_rec}	0.47 × V_S	0.55 × V_S	0.6 × V_S	V	SAE J2602	PRQ-651
Receiver recessive state	V_{BUS_REC}	0.6 × V_S	–	1.15 × V_S	V	[1] ISO 17987-4 (Param 18)	PRQ-652

(table continues...)

Table 16 (continued) Electrical characteristics

V_S = 5.5 V to 18 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values reference conditions: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Receiver center voltage	V_{BUS_CNT}	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	[2] ISO 17987-4 (Param 19)	PRQ-653
Receiver hysteresis	ΔV_{HYS}	0.07 × V_S	0.12 × V_S	0.175 × V_S	V	[3] ISO 17987-4 (Param 20)	PRQ-654
Wake-up threshold voltage	V_{BUS_WK}	0.4 × V_S	0.5 × V_S	0.6 × V_S	V	–	PRQ-655
Bus transmitter interface							
Bus recessive output voltage	V_{BUS_RO}	0.8 × V_S	–	V_S	V	V_{TxD} = high level	PRQ-657
Bus dominant output voltage	V_{BUS_DO}	–	–	2.1	V	V_{TxD} = low level; R_{BUS} = 500 Ω; 10 V < V_S ≤ 18 V	PRQ-3095
Bus dominant output voltage low supply	V_{BUS_DO}	–	–	0.2 × V_S	V	V_{TxD} = low level; R_{BUS} = 500 Ω; 7.3 V ≤ V_S ≤ 10 V	PRQ-3094
Bus dominant output voltage deep supply	V_{BUS_DO}	–	–	1.5	V	V_{TxD} = low level; R_{BUS} = 500 Ω; 5.5 V < V_S ≤ 7.3 V	PRQ-3096
Bus short circuit current	I_{BUS_LIM}	40	130	190	mA	Current limitation for driver dominant state; V_{BUS} ≤ 18 V; ISO 17987-4 (Param 12)	PRQ-658
Leakage current loss of ground	$I_{BUS_NO_GND}$	-1	-0.5	1	mA	V_S = V_{GND} = 12 V; 0 < V_{BUS} < 18 V; ISO 17987-4 (Param 15)	PRQ-3160
Leakage current loss of battery	$I_{BUS_NO_BAT}$	–	10	20	µA	V_S = 0 V; 0 V < V_{BUS} < 18 V; ISO 17987-4 (Param 16)	PRQ-660
Leakage current driver off and bus dominant	$I_{BUS_PAS_dom}$	-1	–	–	mA	V_S = 18 V; V_{BUS} = 0 V; ISO 17987-4 (Param 13)	PRQ-661
Leakage current driver off and bus recessive	$I_{BUS_PAS_rec}$	–	–	20	µA	V_S = 8 V; V_{BUS} = 18 V; LIN 2.2 / ISO 17987-4 (Param 14)	PRQ-662
Bus pull-up resistance	R_{SLAVE}	27.66	33	40	kΩ	Normal mode, also present in sleep mode; ISO 17987-4 (Param 26)	PRQ-663

(table continues...)

Table 16 (continued) Electrical characteristics

V_S = 5.5 V to 18 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values reference conditions: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Auto-addressing specifications							
Functional range while auto-addressing	V_{S_AA}	9	–	15	V	4)	PRQ-3167
Temperature range while auto-addressing	T_{AMB_AA}	0	–	50	°C	4)	PRQ-3168
Pull-up current source	I_{SNPD}	–	–	4.0	mA	Configurable via register $V_S = V_{S_AA}$	PRQ-3166
Shunt resistor	R_{SHUNT}	0.5	0.8	1.2	Ω	–	PRQ-3158
Bus voltage range	V_{BUS_AA}	0	–	2.5	V	4) Bus dominant voltage while auto-addressing	PRQ-3169
Timing							
TXD dominant time out	$t_{TXD_LIN_TO}$	7.8	8	8.2	ms	V_{TXD} = 0 V; filter clock output frequency = 2 MHz	PRQ-685
Dominant time for bus wake-up	t_{WK_BUS}	30	–	150	µs	4) Including analog and digital filter time. Digital filter time can be adjusted via register	PRQ-656
Dominant analog filter time for bus wake-up	$t_{WK_BUS_filter}$	3	–	15	µs	4) Analog filter time of transceiver. An additional digital filter is required to achieve the required wake-up time	PRQ-131
AC Characteristics							
Propagation delay bus dominant to RxD LOW	$t_{d(L)_R}$	1	–	6	µs	4) C_L = 20 pF; ISO 17987-4 (Param 31)	PRQ-664
Propagation delay bus recessive to RxD HIGH	$t_{d(H)_R}$	1	–	6	µs	4) C_L = 20 pF; ISO 17987-4 (Param 31)	PRQ-665
Receiver propagation delay symmetry	t_{sym_R}	-2	–	2	µs	4) $t_{sym_R} = t_{d(H)_R} - t_{d(L)_R}$; ISO 17987-4 (Param 32)	PRQ-666
AC Characteristics - Low battery supply							
Low ECU battery voltage input	$V_{battECU_low}$	6.5	–	8	V	4) 5)	PRQ-2973

(table continues...)

Table 16 (continued) Electrical characteristics

V_S = 5.5 V to 18 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values reference conditions: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Low IC battery voltage input	V_{battIC_low}	5.5	–	7	V	4)	PRQ-2974
Duty cycle D1 at low battery supply	n_{D1_low}	0.396	–	–	–	6) Duty cycle 1 at low battery supply. $TH_{Rec(max)} = 0.665 \times V_S$; $TH_{Dom(max)} = 0.499 \times V_S$; V_S = 5.5 V to 7 V; t_{bit} = 50 µs; $n_{D1_low} = t_{bus_rec(min)}/(2 \times t_{bit})$; ISO 17987-4 (Param 88)	PRQ-2975
Duty cycle D2 at low battery supply	n_{D2_low}	–	–	0.581	–	6) Duty cycle 2 at low battery supply. $TH_{Rec(min)} = 0.496 \times VS$; $TH_{Dom(min)} = 0.361 \times VS$; VS = 6.1 V to 7.6 V; t_{bit} = 50 µs; $n_{D2_low} = t_{bus_rec(max)}/(2 \times t_{bit})$; ISO 17987-4 (Param 89)	PRQ-2976
Duty cycle D3 at low battery supply	n_{D3_low}	0.417	–	–	–	6) Duty cycle 3 at low battery supply. $TH_{Rec(max)} = 0.665 \times VS$; $TH_{Dom(max)} = 0.499 \times VS$; VS = 5.5 V to 7 V; t_{bit} = 96 µs $n_{D3_low} = t_{bus_rec(min)}/(2 \times t_{bit})$; ISO 17987-4 (Param 90)	PRQ-2977

(table continues...)

Table 16 (continued) Electrical characteristics

V_S = 5.5 V to 18 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values reference conditions: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Duty cycle D4 at low battery supply	n_{D4_low}	–	–	0.590	–	[6] Duty cycle 4 at low battery supply. $TH_{Rec(min)} = 0.496 \times VS$; $TH_{Dom(min)} = 0.361 \times VS$; VS = 6.1 V to 7.6 V; t_{bit} = 96 µs $n_{D4_low} = t_{bus_rec(max)}/(2 \times t_{bit})$; ISO 17987-4 (Param 91)	PRQ-2978
AC Characteristics - Transceiver normal slope mode							
Duty cycle D1 normal slope mode (for worst case at 20 kbit/s)	n_{D1}	0.396	–	–	–	[6] Duty cycle 1. $TH_{Rec(max)} = 0.744 \times V_S$; $TH_{Dom(max)} = 0.581\times V_S$; V_S = 7 V to 18 V t_{bit} = 50 µs; $n_{D1} = t_{bus_rec(min)}/(2 \times t_{bit})$; ISO 17987-4 (Param 27)	PRQ-667
Duty cycle D2 normal slope mode (for worst case at 20 kbit/s)	n_{D2}	–	–	0.581	–	[6] Duty cycle 2. $TH_{Rec(min)} = 0.422 \times V_S$; $TH_{Dom(min)} = 0.284\times V_S$; V_S = 7.6 V to 18 V t_{bit} = 50 µs; $n_{D2} = t_{bus_rec(max)}/(2 \times t_{bit})$; ISO 17987-4 (Param 28)	PRQ-668
Duty cycle D3 normal slope mode (for worst case at 10.4 kbit/s)	n_{D3}	0.417	–	–	–	[6] Duty cycle 3. $TH_{Rec(max)} = 0.778 \times V_S$; $TH_{Dom(max)} = 0.616\times V_S$; V_S = 7 V to 18 V t_{bit} = 96 µs; $n_{D3} = t_{bus_rec(min)} / (2 \times t_{bit})$; ISO 17987-4 (Param 29)	PRQ-672

(table continues...)

Table 16 (continued) Electrical characteristics

V_S = 5.5 V to 18 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Chapter 2 (unless otherwise specified). Typical values reference conditions: V_S = 13.5 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Duty cycle D4 normal slope mode (for worst case at 10.4 kbit/s)	n_{D4}	–	–	0.590	–	6) Duty cycle 4. $TH_{Rec(min)}$ = 0.389 × V_S; $TH_{Dom(min)}$ = 0.251× V_S; V_S = 7.6 V to 18 V t_{bit} = 96 µs; $n_{D4} = t_{bus_rec(max)} / (2 \times t_{bit})$; ISO 17987-4 (Param 30)	PRQ-673
AC Characteristics - Flash mode							
Duty cycle D7 (for worst case at 115 kbit/s)	n_{D7}	0.356	–	0.5	–	Duty cycle 7. Flash Mode selected; $TH_{Rec(max)} = 0.6 \times V_S$; $TH_{Dom(max)} = 0.4\times V_S$; T_J = 25°C; t_{bit} = 8.7 µs; V_S = 13.5 V; $n_{D7} = t_{bus_rec(min)}/(2\times t_{bit})$; Load 1 ($C_{BUS}$ / R_{BUS}) = 200 pF / 500 Ω	PRQ-682
LIN input capacitance	C_{BUS}	–	20	35	pF	4)	PRQ-684
Protection							
Thermal shutdown temperature	$T_{J_SD_LIN}$	165	175	200	°C	4)	PRQ-686
Thermal shutdown hysteresis	$\Delta T_{J_SD_LIN}$	5	10	15	K	4)	PRQ-687

1) Maximum limit not subject to production test - specified by design
2) $V_{BUS_CNT} = (V_{th_dom} + V_{th_rec})/2$
3) $V_{HYS} = V_{th_rec} - V_{th_dom}$
4) Not subject to production test - specified by design
5) $V_{battECU}$ is measured at the ECU input power pins. All voltages are referenced to the local ECU ground
6) Bus load concerning LIN Spec 2.2 (C_{BUS}; R_{BUS}):
   Load 1 = 1 nF; 1 kΩ
   Load 2 = 6.8 nF; 660 Ω
   Load 3 = 10 nF; 500 Ω

***Note**: The voltages and currents listed in above table apply to both V_{BUS_M}, V_{BUS_S} and I_{BUS_M}, I_{BUS_S} as shown in Figure 3.*

13 Timer2

13.1 Features overview

The Timer2 provides the following features:

- One channel 16-bit capture mode

The timer module supports LIN autobaud detection by using pin LIN_M as an input for edge detection.

Operating conditions addressed by channel capture mode are as following:

- Count up only
- Start counting from 0000_{16}, overflow at $FFFF_{16}$
- Reload event triggered by overflow condition
- Reload value fixed at 0000_{16}
- Capture event triggered by falling/rising adge at input pin LIN_M
- Captured timer value stored in register
- Interrupt is generated with reload or capture event

14 Application Information

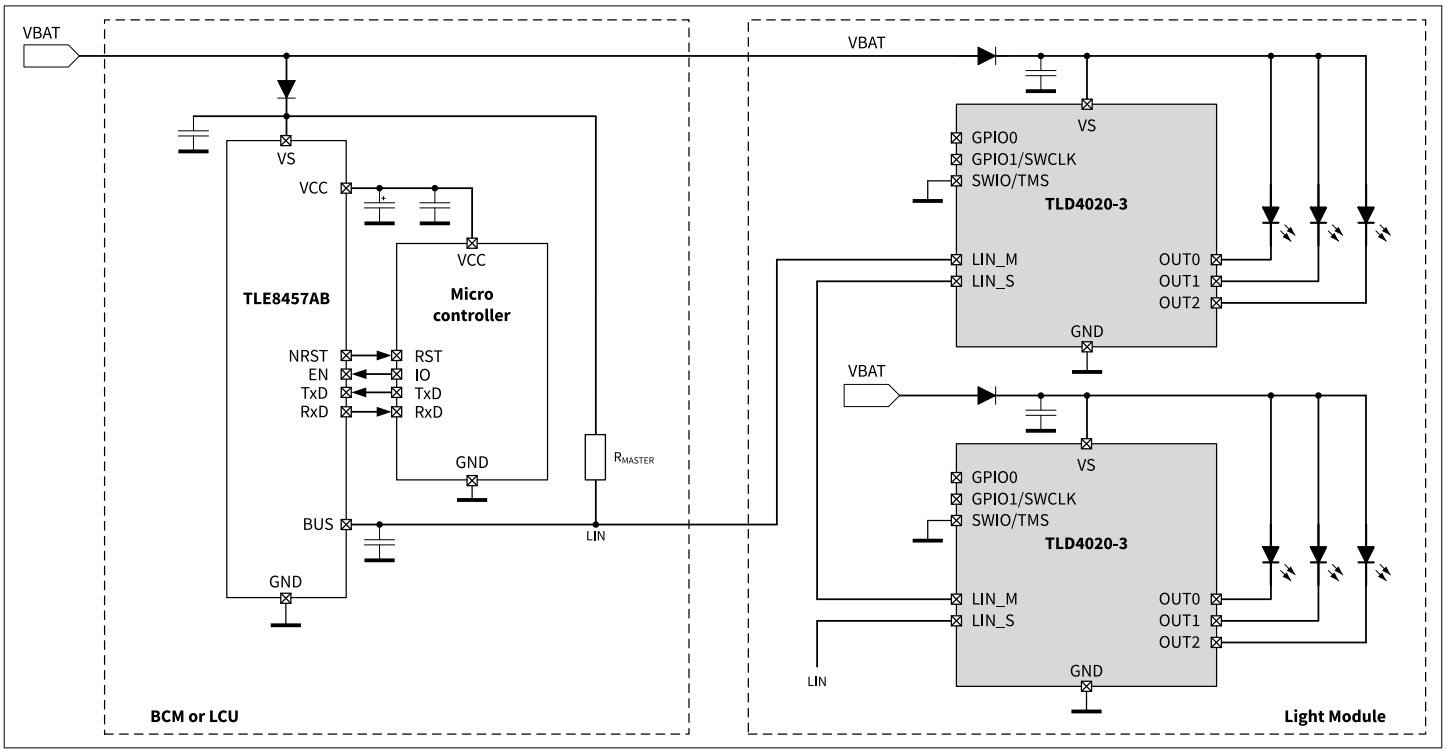


Figure 11 Application diagram

15 Package dimensions

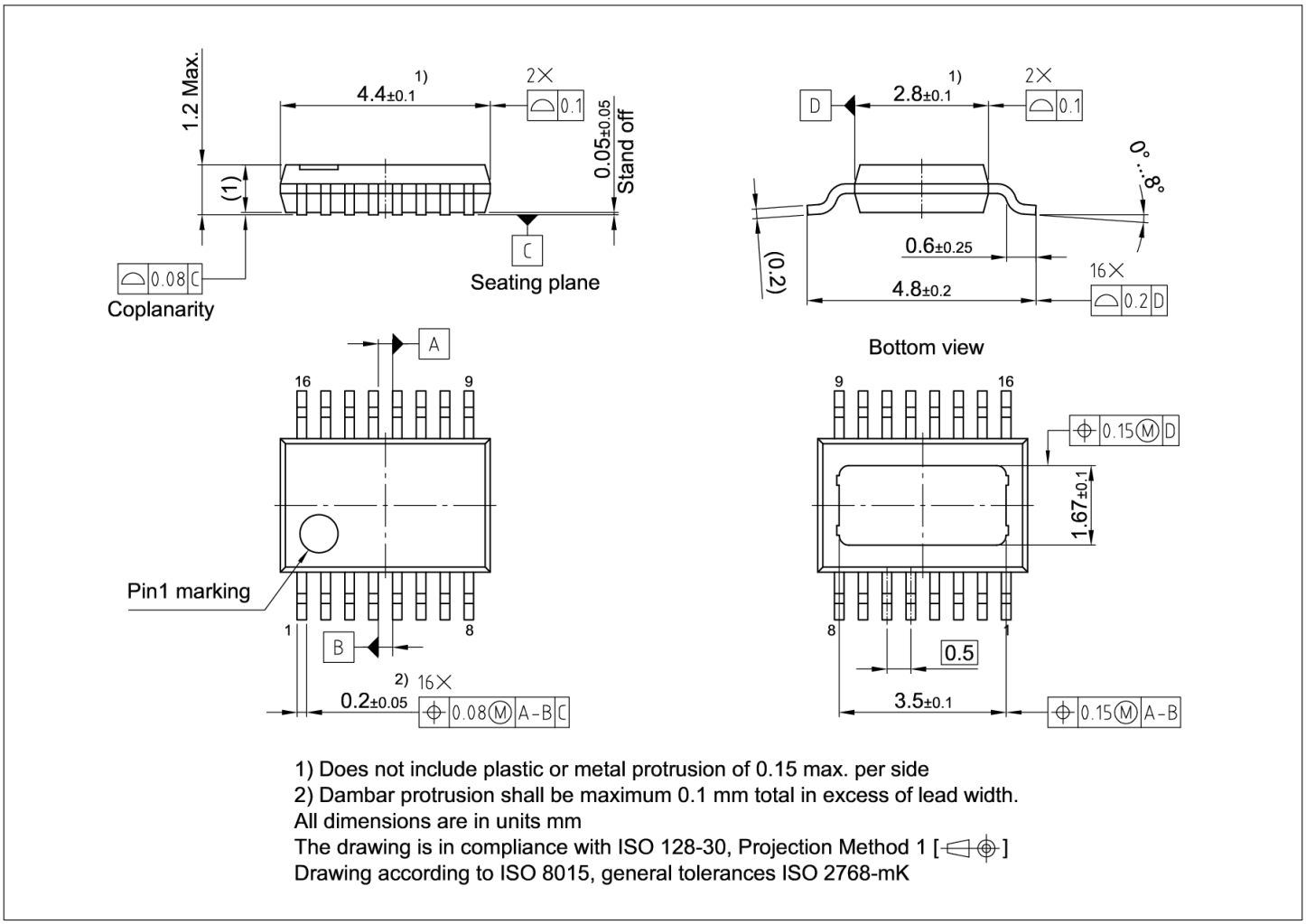


Figure 12 Package outline PG-TFDSO-16

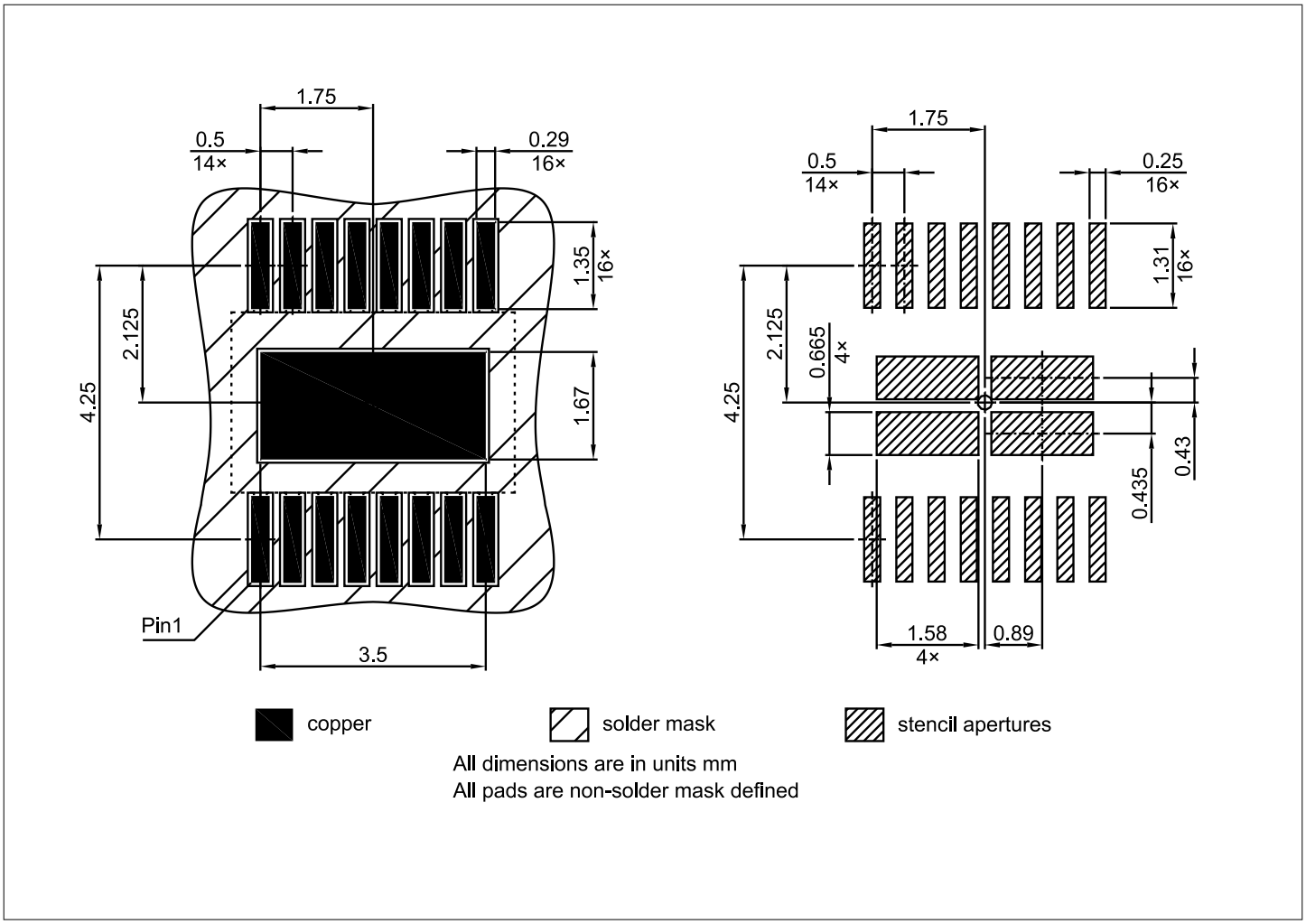


Figure 13 PG-TFDSO-16 package pads and stencil

Note*: *Green product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).
For further information on packages, please visit our website: https://www.infineon.com/packages

Revision history

Document version	Date of release	Description of changes
Rev. 2.00	2025-04-15	• Editorial changes • Deleted PRQ-497, PRQ-538, PRQ-539, PRQ-659, PRQ-797, PRQ-799, PRQ-896, PRQ-1125, PRQ-1131, PRQ-2471, PRQ-2474, PRQ-2853, PRQ-2890, PRQ-2891 • Added PRQ-3150, PRQ-3152, PRQ-3154, PRQ-3155, PRQ-3156, PRQ-3157, PRQ-3158, PRQ-3159, PRQ-3160, PRQ-3161, PRQ-3162, PRQ-3163, PRQ-3166, PRQ-3167, PRQ-3168, PRQ-3169, PRQ-3170
Rev. 1.01	2025-01-08	• Deleted PRQ-921 • PRQ-2851: Updated Min and Condition
Rev. 1.00	2024-10-14	• Initial document release

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