

# 英飞凌32 位

微控制器

## TC39x

32 位单片机

BC/BD版

## 32 位单片机

## 数据手册

V 1.2, 2021-03

# 微控制器

**Edition 2021-03**

**Published by**

**Infineon Technologies AG**

**81726 Munich, Germany**

**© 2021 Infineon Technologies AG**

**All Rights Reserved.**

### **Legal Disclaimer**

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie"). With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

### **Information**

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office ([www.infineon.com](http://www.infineon.com))

### **Warnings**

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

**本数据手册的原文使用英文撰写。为方便起见，英飞凌提供了译文；由于翻译过程中可能使用了自动化工具，英飞凌不保证译文的准确性。为确认准确性，请务必访问 [infineon.com](http://infineon.com) 参考最新的英文版本（控制文档）。**

---

**Revision History**

<b>Page or Item</b>	<b>Subjects (major changes since previous revision)</b>
<b>V 0.4, 2015-05</b>	
	Version 0.4 is the first version of this document
<b>V 0.6, 2017-09</b>	
	The history is documented in the last chapter
<b>V 0.7, 2018-07</b>	
	The history is documented in the last chapter
<b>V 1.0, 2018-10</b>	
	The history is documented in the last chapter
<b>V 1.1, 2019-09</b>	
	The history is documented in the last chapter
<b>V 1.2, 2021-03</b>	
	The history is documented in the last chapter

**Trademarks of Infineon Technologies AG**

AURIX™, C166™, CanPAK™, CIPOST™, CIPURSE™, EconoPACK™, CoolMOST™, CoolSET™, CORECONTROL™, CROSSAVE™, DAVE™, DI-POL™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPIM™, EconoPACK™, EiceDRIVER™, eupec™, FCOS™, HITFET™, HybridPACK™, I<sup>2</sup>RF™, ISOFACE™, IsoPACK™, MIPAQ™, ModSTACK™, my-d™, NovalithIC™, OptiMOS™, ORIGA™, POWERCODE™, PRIMARION™, PrimePACK™, PrimeSTACK™, PRO-SIL™, PROFET™, RASIC™, ReverSave™, SatRIC™, SIEGET™, SINDRION™, SIPMOST™, SmartLEWIS™, SOLID FLASH™, TEMPFET™, thinQ!™, TRENCHSTOP™, TriCore™.

**Other Trademarks**

Advance Design System™ (ADS) of Agilent Technologies, AMBA™, ARM™, MULTI-ICE™, KEIL™, PRIMECELL™, REALVIEW™, THUMB™, μVision™ of ARM Limited, UK. AUTOSAR™ is licensed by AUTOSAR development partnership. Bluetooth™ of Bluetooth SIG Inc. CAT-iq™ of DECT Forum. COLOSSUS™, FirstGPS™ of Trimble Navigation Ltd. EMV™ of EMVCo, LLC (Visa Holdings Inc.). EPCOST™ of Epcos AG. FLEXGO™ of Microsoft Corporation. FlexRay™ is licensed by FlexRay Consortium. HYPERTERMINAL™ of Hilgraeve Incorporated. IEC™ of Commission Electrotechnique Internationale. IrDA™ of Infrared Data Association Corporation. ISO™ of INTERNATIONAL ORGANIZATION FOR STANDARDIZATION. MATLAB™ of MathWorks, Inc. MAXIM™ of Maxim Integrated Products, Inc. MICROTEC™, NUCLEUS™ of Mentor Graphics Corporation. MIPI™ of MIPI Alliance, Inc. MIPS™ of MIPS Technologies, Inc., USA. muRata™ of MURATA MANUFACTURING CO., MICROWAVE OFFICE™ (MWO) of Applied Wave Research Inc., OmniVision™ of OmniVision Technologies, Inc. Openwave™ Openwave Systems Inc. RED HAT™ Red Hat, Inc. RFMD™ RF Micro Devices, Inc. SIRIUS™ of Sirius Satellite Radio Inc. SOLARIS™ of Sun Microsystems, Inc. SPANSION™ of Spansion LLC Ltd. Symbian™ of Symbian Software Limited. TAIYO YUDEN™ of Taiyo Yuden Co. TEAKLITE™ of CEVA, Inc. TEKTRONIX™ of Tektronix Inc. TOKO™ of TOKO KABUSHIKI KAISHA TA. UNIX™ of X/Open Company Limited. VERILOG™, PALLADIUM™ of Cadence Design Systems, Inc. VLYNQ™ of Texas Instruments Incorporated. VXWORKS™, WIND RIVER™ of WIND RIVER SYSTEMS, INC. ZETEX™ of Diodes Zetex Limited.

商标最新更新日期 2011-11-11

## 目录

<b>1</b>	<b>特性概要</b> .....	<b>7</b>
<b>2</b>	<b>引脚定义和功能:</b> .....	<b>12</b>
2.1	LFBGA-516 封装变体引脚配置 .....	15
2.2	LFBGA-292 封装变体引脚配置 .....	173
2.3	LFBGA-292 ADAS 封装变体引脚配置 .....	277
2.4	焊盘框中焊盘的顺序 .....	376
2.5	标志.....	403
<b>3</b>	<b>电气规格参数</b> .....	<b>405</b>
3.1	参数解释.....	405
3.2	绝对最大额定值.....	406
3.3	过载下的引脚可靠性.....	407
3.4	工作条件.....	410
3.5	5 V / 3.3 V 可切换焊盘 .....	413
3.6	高性能 LVDS 焊盘.....	432
3.7	VADC 参数 .....	435
3.8	DSADC 参数 .....	439
3.9	MHz 振荡器.....	442
3.10	备用时钟.....	444
3.11	温度感应器.....	445
3.12	电源电流.....	446
3.12.1	计算 1.25 V 电流消耗 .....	452
3.13	电源基础结构和电源启动.....	453
3.13.1	供电上升和下降行为 .....	454
3.13.1.1	单电源模式 (a) .....	454
3.13.1.2	单电源模式 (e) .....	456
3.13.1.3	外部供电模式 (d) .....	458
3.13.1.4	外部供电模式 (h) .....	460
3.14	复位时间.....	462
3.15	EVR .....	465
3.16	系统锁相环 (SYS_PLL) .....	473
3.17	外设锁相环 (PER_PLL) .....	474
3.18	交流规格.....	475
3.19	JTAG参数 .....	476
3.20	DAP 参数 .....	478
3.21	ASCLIN SPI 主时序 .....	480
3.22	QSPI 时序、主模式和从模式.....	482
3.23	MSC时序 5 V 操作 .....	486
3.24	以太网接口 (ETH) 特性.....	488
3.24.1	ETH 测量参考点 .....	488
3.24.2	ETH管理信号参数 (ETH_MDC、ETH_MDIO) .....	489
3.24.3	ETH MII 参数 .....	490
3.24.4	ETH RMII 参数 .....	491
3.24.5	ETH RGMII 参数 .....	492
3.25	E-Ray 参数 .....	493
3.26	HSCT 参数.....	495
3.27	Inter-IC (I2C) 接口时序.....	497
3.28	SDMMC 接口时序 .....	500
3.29	FSP 参数 .....	501

3.30	雷达接口时序.....	502
3.31	EBU时序.....	503
3.31.1	BFCLKO 输出时钟时序 .....	503
3.31.2	EBU 异步时序 .....	503
3.31.3	EBU 突发模式访问时序 .....	507
3.31.4	EBU 仲裁信号时序 .....	509
3.32	Flash 目标参数 .....	510
3.33	质量声明.....	515
3.34	封装外形尺寸 .....	517
3.34.1	封装参数.....	518
<b>4</b>	<b>记录.....</b>	<b>519</b>
4.1	从0.4版本到0.6版本的变更 .....	519
4.2	从0.6版本到0.7版本的变更 .....	529
4.3	从0.7版本到1.0版本的变更 .....	535
4.4	从1.0版本到1.1版本的变更 .....	541
4.5	从1.1版本到1.2版本的变更 .....	542

## 1 特性概要

TC39x产品系列具有以下特点：

- 具有六个CPU核心的高性能微控制器
- 六个 32 位超标量 TriCore CPU (TC1.6.2P)，每个都具有以下特点：
  - 卓越的实时性能
  - 强大的位处理能力
  - 完全集成的 DSP 功能
  - 乘法累加单元能够实现每个周期2次MAC运算
  - 全流水线浮点单元(FPU)
  - 全温度范围内运行速度高达 300 MHz
  - 高达 240/96 KB 的数据暂存器 RAM (DSPR)
  - 高达 64 KB 的指令暂存器 RAM (PSPR)
  - 高达 64 KB 的数据 RAM (DLMU)
  - 32 KB 指令高速缓存 (ICACHE)
  - 16 KB 数据缓存 (DCACHE)
- 四个 TC1.6.2P 的锁步影子核心
- 多个片上存储器
  - 所有嵌入式 NVM 和 SRAM 均受到 ECC 保护
  - 高达 16 MB 的程序闪存 (PFLASH)
  - 高达 1 MB 的可用于 EEPROM 仿真数据的闪存式存储器 (DFLASH 0)
  - 768 KB 内存 (LMU)
  - 引导只读存储器 (BROM)
- 具有安全数据传输的 128 通道 DMA 控制器
- 先进的中断系统 (ECC保护)
- 高性能片上总线结构
  - 可提供总线主控器、CPU 和内存之间快速并行访问的64 位交叉互连总线 (SRI)
  - 用于片上外设和功能单元的 32 位系统外设总线 (SPB)
  - SRI 至 SPB 总线桥 (SFI 桥)
- 某些型号可选配硬件安全模块 (HSM)
- 处理安全监测警报的安全管理单元 (SMU)
- 具有 ECC、内存初始化和 MBIST 功能 (MTU) 的内存测试单元
- 用于检查数字 I/O 的硬件 I/O 监视器 (IOM)
- 多功能片上外设单元
  - 8 个异步/同步串行通道 (ASCLIN)，支持硬件 LIN (V1.3、V2.0、V2.1 和 J2602)，速率高达 50 MBaud
  - 6 个队列 SPI 接口通道 (QSPI)，具有主从功能，速率高达 50 Mbit/s
  - 2 个高速串行链路 (HSSL)，用于处理器间串行通讯，速度高达 320 Mbit/s
  - 4 个串行微秒总线接口 (MSC)，用于将串行端口扩展到外部电源设备
  - 3 个 MCMCAN 模块，每个模块带有 4 个 CAN 节点，可通过 FIFO 缓冲实现高效数据处理
  - 25 个单边半字节传输 (SENT) 通道，用于连接传感器
  - 2 个 FlexRay™模块，带 2 个通道 (E-Ray)，支持 V2.1

- 一个通用定时器模块 (GTM)，提供一组强大的数字信号滤波和定时器功能，以实现自主和复杂的输入/输出管理
- 1个捕获/比较 6 模块（两个内核：CCU60 和 CCU61）
- 1个通用定时器单元（GPT12）
- 4个符合V1.3的通道外设传感器接口（PSI5）
- 1个带串行 PHY 的外围传感器接口 (PSI5-S)
- 2个符合 V2.1 的集成电路总线接口 (I2C)
- 1 IEEE802.3以太网 MAC (ETH)，带有 RMII 和 MII 接口 (ETH)
- 1个外部总线接口（EBU）
- 多功能逐次逼近型 ADC (VADC)
  - 20个独立 ADC 内核集群
  - 输入电压范围为 0 V 至 5.5V（ADC 电源）
- Delta-Sigma ADC (DSADC)
  - 14个通道
- 数字可编程 I/O 端口
- 支持OCDS Level 1 片上调试（CPU、DMA、片上总线）
- 多核调试、实时跟踪和校准
- 四/五线JTAG (IEEE 1149.1) 或 DAP (器件访问端口) 接口
- 电源管理系统和片上调节器
- 带有系统 PLL 和外设 PLL 的时钟生成单元
- 嵌入式电压调节器
- 符合 AEC-Q100 的汽车应用要求（仅适用于相应销售代码的交付发布后）
- ISO 26262 安全要素，不依赖于上下文，安全要求高达 ASIL D（仅适用于 IFX 发布的“安全包发布说明”中列出的销售代码）

**订购信息**

英飞凌微控制器的订购代码提供了特定产品的准确参考。此订购代码标识：

- 衍生物本身，即其功能集、温度范围和电源电压
- 封装和供应类型

**表 1-1 平台特点概述**

<b>Feature</b>	<b>TC39x</b>	
CPUs	Type	TC1.6.2
	Cores / Checker Cores	6 / 4
	Max. Freq.	300 MHz
Cache per CPU	Program	32 KB
	Data	16 KB
SRAM per CPU	PSPR	64 KB
	DSPR	240 KB for CPU0,1/ 96 KB else
	DLMU	64 KB
SRAM global	LMU	768 KB
	DAM	128 KB
Extension Memory	TCM	2 MB
	XCM	2 MB
	XTM	16 KB
Program Flash	Size	16 MB
	Banks	5 x 3 MB, 1 x 1 MB
Data Flash	Size (single-ended)	1 MB (DF0) + 128 KB (DF1)
DMA	Channels	128
CONVCTRL	Modules	1
EVADC	Primary Groups/Channels	8 / 64
	Secondary Groups/Channels	4 / 64
	Fast Compare Channels	8
EDSADC	Channels	14

**表 1-1 平台特点概述 (续)**

<b>Feature</b>		<b>TC39x</b>
GTM	Clusters	12 (5 @ 200MHz, 7 @ 100MHz)
	TIM (8 ch)	8
	TOM (16 ch)	6
	ATOM (8 ch)	12
	MCS (8 ch)	10
	CMU / ICM	1 / 1
	PSM	3
	TBU channels <sup>1)</sup>	4 (TBU0-3)
	SPE	6
	CMP / MON	1 / 1
	BRC / DPLL	1 / 1
	CDTM modules	7
DTM modules	24 (10 on TOM, 14 on ATOM)	
Timer	GPT12	1
	CCU6	1
STM	Modules	6
FlexRay	Modules	2
	Channels	2 x 2
CAN	Modules	3
	Nodes	3 x 4
	of which support TT-CAN	1
QSPI	Modules	6
	HSCI Channels	2
ASCLIN	Modules	12
I2C	Interfaces	2
SENT	Channels	25
PSI5	Modules	4
PSI5-S	Modules	1
HSSL	Channels	2
MSC	Channels	4
EBU	External Bus	1
SDMMC	eMMC/SD Interface	1
Ethernet (10/100Mbit/1Gbit)	Modules	1
FCE	Modules	1
Safety Support	SMU	yes
	IOM	yes
SPU	Modules	2

**表 1-1 平台特点概述 (续)**

Feature		TC39x
RIF	Modules	2
HSPDM	Modules	1
Security	HSM+	1
Debug	OCDS	yes
	MCDS	yes
	miniMCDS	no
	miniMCDS TRAM	- KB
	AGBT <sup>2)</sup>	yes
Low Power Features	Standby RAM	2
	SCR	yes
Packages	Type	LFBGA-516 / LFBGA-292
I/O	Type	5 V CMOS / 3.3 V CMOS / LVDS
T <sub>ambient</sub>	Range	-40 ... +150°C

1) TBU3 具有作为角度时钟的特殊用途。

2) Aurora Gigabit Trace 模块 (AGBT) 是一个追踪调试接口，仅供开发使用（不用于量产）。它仅适用于具有功能包 E、T 的特定仿真设备，以及具有功能包 A、H 的 TC39x、TC37xEXT、TC35x、TC33xEXT 的 ADAS 设备。AGBT I/O 功能仅适用于 292 或更多引脚。有关 AGBT 参数的详细信息，请参阅“TC3xx 仿真设备”数据手册。

## 2 引脚定义和功能:

下图显示了不同封装变体的 TC39x 逻辑符号:

- LFBGA-516 (图 2-1)
- LFBGA-292 (图 2-2)
- LFBGA-292 ADAS 功能集 (图 2-3)

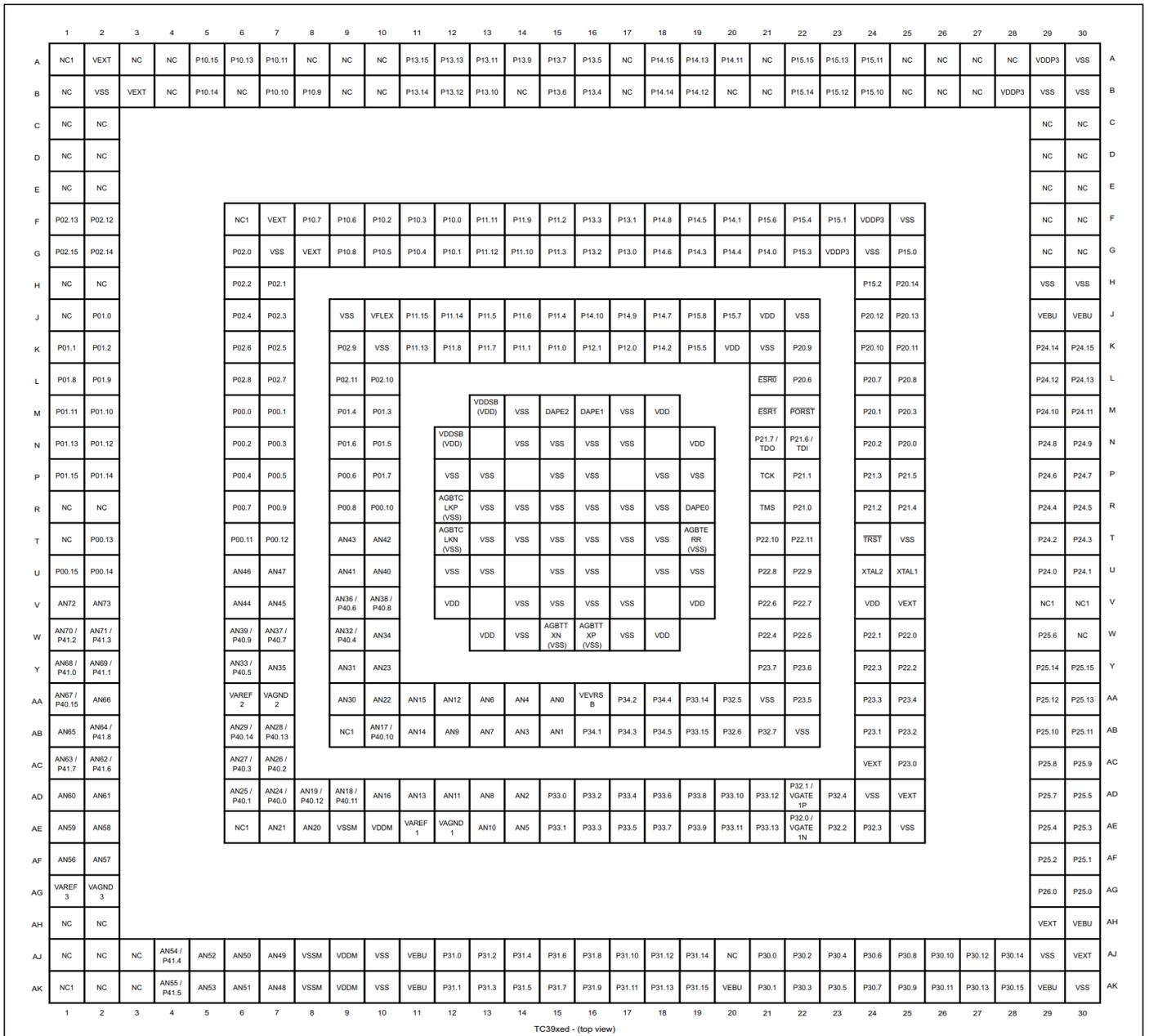


图 2-1 封装变体 LFBGA-516 的逻辑符号

引脚定义和功能:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	NC1	VEXT	P10.7	P10.6	P10.2	P10.3	P10.0	P11.11	P11.9	P11.2	P13.3	P13.1	P14.8	P14.5	P14.1	P15.6	P15.4	P15.1	VDDP3	VSS	A
B	P02.0	VSS	VEXT	P10.8	P10.5	P10.4	P10.1	P11.12	P11.10	P11.3	P13.2	P13.0	P14.6	P14.3	P14.4	P14.0	P15.3	VDDP3	VSS	P15.0	B
C	P02.2	P02.1																	P15.2	P20.14	C
D	P02.4	P02.3		VSS	VFLEX	P11.15	P11.14	P11.5	P11.6	P11.4	P14.10	P14.9	P14.7	P15.8	P15.7	VDD	VSS		P20.12	P20.13	D
E	P02.6	P02.5		P02.9	VSS	P11.13	P11.8	P11.7	P11.1	P11.0	P12.1	P12.0	P14.2	P15.5	VDD	VSS	P20.9		P20.10	P20.11	E
F	P02.8	P02.7		P02.11	P02.10											ESR0	P20.6		P20.7	P20.8	F
G	P00.0	P00.1		P01.4	P01.3			VDDSB (VDD)	VSS	DAPE2	DAPE1	VSS	VDD			ESR1	FORST		P20.1	P20.3	G
H	P00.2	P00.3		P01.6	P01.5			VDDSB (VDD)	VSS	VSS	VSS	VSS	VSS	VDD		P21.7 / TDO	P21.6 / TDI		P20.2	P20.0	H
J	P00.4	P00.5		P00.6	P01.7			VSS	VSS	VSS	VSS	VSS	VSS	VSS		TCK	P21.1		P21.3	P21.5	J
K	P00.7	P00.9		P00.8	P00.10			AGBTC LKP (VSS)	VSS	VSS	VSS	VSS	VSS	DAPE0		TMS	P21.0		P21.2	P21.4	K
L	P00.11	P00.12		AN43	AN42			AGBTC LKN (VSS)	VSS	VSS	VSS	VSS	VSS	AGBTE RR (VSS)		P22.10	P22.11		TRST	VSS	L
M	AN46	AN47		AN41	AN40			VSS	VSS	VSS	VSS	VSS	VSS	VSS		P22.8	P22.9		XTAL2	XTAL1	M
N	AN44	AN45		AN36 / P40.6	AN38 / P40.8			VDD	VSS	VSS	VSS	VSS	VSS	VDD		P22.6	P22.7		VDD	VEXT	N
P	AN39 / P40.9	AN37 / P40.7		AN32 / P40.4	AN34			VDD	VSS	AGBTT XN (VSS)	AGBTT XP (VSS)	VSS	VDD			P22.4	P22.5		P22.1	P22.0	P
R	AN33 / P40.5	AN35		AN31	AN23											P23.7	P23.6		P22.3	P22.2	R
T	VAREF 2	VAGND 2		AN30	AN22	AN15	AN12	AN6	AN4	AN0	VEVRS B	P34.2	P34.4	P33.14	P32.5	VSS	P23.5		P23.3	P23.4	T
U	AN29 / P40.14	AN28 / P40.13		NC1	AN17 / P40.10	AN14	AN9	AN7	AN3	AN1	P34.1	P34.3	P34.5	P33.15	P32.6	P32.7	VSS		P23.1	P23.2	U
V	AN27 / P40.3	AN26 / P40.2																	VEXT	P23.0	V
W	AN25 / P40.1	AN24 / P40.0	AN19 / P40.12	AN18 / P40.11	AN16	AN13	AN11	AN8	AN2	P33.0	P33.2	P33.4	P33.6	P33.8	P33.10	P33.12	P32.1 / VGATE 1P	P32.4	VSS	VEXT	W
Y	NC1	AN21	AN20	VSSM	VDDM	VAREF 1	VAGND 1	AN10	AN5	P33.1	P33.3	P33.5	P33.7	P33.9	P33.11	P33.13	P32.0 / VGATE 1N	P32.2	P32.3	VSS	Y

TC39xed - (top view)

图 2-2 封装变体 LFBGA-292 的逻辑符号

引脚定义和功能:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		
A	NC1	VEXT	NC	P51_1 1	P51_9	P51_7	P51_5	P51_3	P51_1	P11.11	P11.9	P11.2	P14.8	P14.5	P14.1	P15.6	P15.4	P15.1	VDDP3	VSS	A	
B	NC	VSS	VEXT	P51_1 0	P51_8	P51_6	P51_4	P51_2	P51_0	P11.12	P11.10	P11.3	P14.6	P14.3	P14.4	P14.0	P15.3	VDDP3	VSS	P15.0	B	
C	P50_1	P50_0																	P15.2	P20.14	C	
D	P50_3	P50_2		VSS	VFLEX	P11.15	P11.14	P11.5	P11.6	P11.4	P14.10	P14.9	P14.7	P15.8	P15.7	VDD	VSS			P20.12	P20.13	D
E	P50_5	P50_4		P10.0	VSS	P11.13	P11.8	P11.7	P11.1	P11.0	P12.1	P12.0	P14.2	P15.5	VDD	VSS	P20.9			P20.10	P20.11	E
F	P50_7	P50_6		P10.1	P10.2											ESR0	P20.6			P20.7	P20.8	F
G	P50_9	P50_8		P10.3	P10.4			VDD	VSS	DAPE2	DAPE1	VSS	VDD				ESR1	PORST		P20.1	P20.3	G
H	P50_1 1	P50_1 0		P10.5	P10.6		VDD		VSS	VSS	VSS	VSS		VDD			P21.7 / TDO	P21.6 / TDI		P20.2	P20.0	H
J	P02.0	P02.1		P10.8	P10.7		VSS	VSS		VSS	VSS		VSS	VSS			TCK	P21.1		P21.3	P21.5	J
K	P02.2	P02.3		P02.4	P02.5		AGBTC LKP (VSS)	VSS	VSS	VSS	VSS	VSS	VSS	DAPE0			TMS	P21.0		P21.2	P21.4	K
L	P02.6	P00.0		P02.7	P02.8		AGBTC LKN (VSS)	VSS	VSS	VSS	VSS	VSS	VSS	AGBTE RR (VSS)			P22.10	P22.11		TRST	VSS	L
M	P00.2	P00.1		P00.3	P00.4		VSS	VSS		VSS	VSS		VSS	VSS			P22.8	P22.9		XTAL2	XTAL1	M
N	P00.8	P00.7		P00.6	P00.5		VDD		VSS	VSS	VSS		VSS	VDD			P22.6	P22.7		VDD	VEXT	N
P	P00.10	P00.9		AN47	AN45		VDD	VSS	AGBTT XN (VSS)	AGBTT XP (VSS)	VSS	VDD					P22.4	P22.5		P22.1	P22.0	P
R	P00.11	P00.12		AN25 / P40.1	AN23												P23.7	P23.6		P22.3	P22.2	R
T	VAREF 2	VAGND 2		AN24 / P40.0	AN22	AN15	AN12	AN6	AN4	AN0	VEVRS B	P34.2	P34.4	P33.14	P32.5	VSS	P23.5			P23.3	P23.4	T
U	AN44	AN46		NC1	AN17 / P40.10	AN14	AN9	AN7	AN3	AN1	P34.1	P34.3	P34.5	P33.15	P32.6	P32.7	VSS			P23.1	P23.2	U
V	AN39 / P40.9	AN37 / P40.7																		VEXT	P23.0	V
W	AN36 / P40.6	AN38 / P40.8	AN19 / P40.12	AN18 / P40.11	AN16	AN13	AN11	AN8	AN2	P33.0	P33.2	P33.4	P33.6	P33.8	P33.10	P33.12	P32.1 / VGATE 1P	P32.4	VSS	VEXT	W	
Y	NC1	AN21	AN20	VSSM	VDDM	VAREF 1	VAGND 1	AN10	AN5	P33.1	P33.3	P33.5	P33.7	P33.9	P33.11	P33.13	P32.0 / VGATE 1N	P32.2	P32.3	VSS	Y	

TC39xed\_adas - (top view)

图 2-3 封装变体 LFBGA-292 ADAS 的逻辑符号

## 2.1 LFBGA-516 封装变体引脚配置

表 2-1 端口 P00 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
M6	P00.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN4_10			Mux input channel 4 of TIM module 5
	GTM_TIM3_IN0_1			Mux input channel 0 of TIM module 3
	GTM_TIM2_IN0_1			Mux input channel 0 of TIM module 2
	CCU61_CTRAPA			Trap input capture
	CCU60_T12HRE			External timer start 12
	MSC0_INJ0			Injection signal from port
	GETH_MDIOA			MDIO Input
	P00.0			O0
	GTM_TOUT9	O1	GTM muxed output	
	IOM_REF0_9		Reference input 0	
	ASCLIN3_ASCLK	O2	Shift clock output	
	ASCLIN3_ATX	O3	Transmit output	
	IOM_MON2_15		Monitor input 2	
	IOM_REF2_15		Reference input 2	
	—	O4	Reserved	
	CAN10_TXD	O5	CAN transmit output node 0	
	—	O6	Reserved	
	CCU60_COUT63	O7	T13 PWM channel 63	
	IOM_MON1_6		Monitor input 1	
IOM_REF1_0	Reference input 1			
GETH_MDIO	MDIO Output			

表 2-1 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
M7	P00.1	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM5_IN5_11			<b>Mux input channel 5 of TIM module 5</b>
	GTM_TIM3_IN1_1			<b>Mux input channel 1 of TIM module 3</b>
	GTM_TIM2_IN1_1			<b>Mux input channel 1 of TIM module 2</b>
	CCU60_CC60INB			<b>T12 capture input 60</b>
	ASCLIN3_ARXE			<b>Receive input</b>
	EDSADC_DSCIN5A			<b>Modulator clock input, channel 5</b>
	CAN10_RXDA			<b>CAN receive input node 0</b>
	PSI5_RX0A			<b>RXD inputs (receive data) channel 0</b>
	CCU61_CC60INA			<b>T12 capture input 60</b>
	SENT_SENT0B			<b>Receive input channel 0</b>
	EDSADC_DSCIN7B			<b>Modulator clock input, channel 7</b>
	EVADC_G9CH11			AI
	EDSADC_EDS5NA	<b>Negative analog input channel 5, pin A</b>		
	P00.1	O0	<b>General-purpose output</b>	
	GTM_TOUT10	O1	<b>GTM muxed output</b>	
	IOM_REF0_10	O2	<b>Reference input 0</b>	
	ASCLIN3_ATX		<b>Transmit output</b>	
	IOM_MON2_15		<b>Monitor input 2</b>	
	IOM_REF2_15	O3	<b>Reference input 2</b>	
	—		<b>Reserved</b>	
	EDSADC_DSCOUT5	O4	<b>Modulator clock output</b>	
	EDSADC_DSCOUT7	O5	<b>Modulator clock output</b>	
	SENT_SPC0	O6	<b>Transmit output</b>	
CCU61_CC60	O7	<b>T12 PWM channel 60</b>		
IOM_MON1_8		<b>Monitor input 1</b>		
IOM_REF1_13		<b>Reference input 1</b>		

表 2-1 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
N6	P00.2	I	SLOW / PU1 / VEXT / ES1	<b>General-purpose input</b>
	GTM_TIM5_IN6_11			<b>Mux input channel 6 of TIM module 5</b>
	GTM_TIM3_IN1_2			<b>Mux input channel 1 of TIM module 3</b>
	GTM_TIM2_IN1_2			<b>Mux input channel 1 of TIM module 2</b>
	EDSADC_DSDIN7B			<b>Digital datastream input, channel 7</b>
	EDSADC_DSDIN5A			<b>Digital datastream input, channel 5</b>
	SENT_SENT1B			<b>Receive input channel 1</b>
	EVADC_G9CH10	AI	<b>Analog input channel 10, group 9</b>	
	EDSADC_EDS5PA		<b>Positive analog input channel 5, pin A</b>	
	P00.2	O0	<b>General-purpose output</b>	
	GTM_TOUT11	O1	<b>GTM muxed output</b>	
	IOM_REF0_11		<b>Reference input 0</b>	
	ASCLIN3_ASCLK	O2	<b>Shift clock output</b>	
	CAN21_TXD	O3	<b>CAN transmit output node 1</b>	
	PSI5_TX0	O4	<b>TXD outputs (send data)</b>	
	IOM_MON1_14		<b>Monitor input 1</b>	
	IOM_REF1_14		<b>Reference input 1</b>	
	CAN03_TXD	O5	<b>CAN transmit output node 3</b>	
	IOM_MON2_8		<b>Monitor input 2</b>	
	IOM_REF2_8		<b>Reference input 2</b>	
	QSPI3_SLSO4	O6	<b>Master slave select output</b>	
	CCU61_COUT60	O7	<b>T12 PWM channel 60</b>	
	IOM_MON1_11		<b>Monitor input 1</b>	
	IOM_REF1_10		<b>Reference input 1</b>	

表 2-1 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
N7	P00.3	I	SLOW / PU1 / VEXT / ES1	<b>General-purpose input</b>	
	GTM_TIM5_IN7_10			<b>Mux input channel 7 of TIM module 5</b>	
	GTM_TIM3_IN2_1			<b>Mux input channel 2 of TIM module 3</b>	
	GTM_TIM2_IN2_1			<b>Mux input channel 2 of TIM module 2</b>	
	CCU60_CC61INB			<b>T12 capture input 61</b>	
	EDSADC_DSCIN3A			<b>Modulator clock input, channel 3</b>	
	EDSADC_ITR5F			<b>Trigger/Gate input, channel 5</b>	
	PSI5_RX1A			<b>RXD inputs (receive data) channel 1</b>	
	CAN03_RXDA			<b>CAN receive input node 3</b>	
	CAN21_RXDA			<b>CAN receive input node 1</b>	
	PSI5S_RXA			<b>RX data input</b>	
	SENT_SENT2B			<b>Receive input channel 2</b>	
	CCU61_CC61INA			<b>T12 capture input 61</b>	
	EVADC_G9CH9			AI	<b>Analog input channel 9, group 9</b>
	EDSADC_EDS5NB				<b>Negative analog input channel 5, pin B</b>
	P00.3	O0	<b>General-purpose output</b>		
	GTM_TOUT12	O1	<b>GTM muxed output</b>		
	IOM_REF0_12		<b>Reference input 0</b>		
	ASCLIN3_ASLSO	O2	<b>Slave select signal output</b>		
	—	O3	<b>Reserved</b>		
	EDSADC_DSCOUT3	O4	<b>Modulator clock output</b>		
	—	O5	<b>Reserved</b>		
	SENT_SPC2	O6	<b>Transmit output</b>		
	CCU61_CC61	O7	<b>T12 PWM channel 61</b>		
	IOM_MON1_9		<b>Monitor input 1</b>		
	IOM_REF1_12		<b>Reference input 1</b>		

表 2-1 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
P6	P00.4	I	SLOW / PU1 / VEXT / ES1	<b>General-purpose input</b>	
	GTM_TIM6_IN4_1			<b>Mux input channel 4 of TIM module 6</b>	
	GTM_TIM3_IN3_1			<b>Mux input channel 3 of TIM module 3</b>	
	GTM_TIM2_IN3_1			<b>Mux input channel 3 of TIM module 2</b>	
	SCU_E_REQ2_2			<b>ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>	
	SENT_SENT3B			<b>Receive input channel 3</b>	
	EDSADC_DSDIN3A			<b>Digital datastream input, channel 3</b>	
	EDSADC_SGNA			<b>Carrier sign signal input</b>	
	ASCLIN10_ARXA			<b>Receive input</b>	
	GTM_DTMA5_0			<b>CDTM5_DTM4</b>	
	GTM_DTMT3_0			<b>CDTM3_DTM0</b>	
	EVADC_G9CH8			AI	<b>Analog input channel 8, group 9</b>
	EDSADC_EDS5PB				<b>Positive analog input channel 5, pin B</b>
	P00.4	O0	<b>General-purpose output</b>		
	GTM_TOUT13	O1	<b>GTM muxed output</b>		
	IOM_REF0_13		<b>Reference input 0</b>		
	PSI5S_TX	O2	<b>TX data output</b>		
	CAN11_TXD	O3	<b>CAN transmit output node 1</b>		
	PSI5_TX1	O4	<b>TXD outputs (send data)</b>		
	IOM_MON1_15		<b>Monitor input 1</b>		
	EVADC_FC4BFLOUT	O5	<b>Boundary flag output, FC channel 4</b>		
	SENT_SPC3	O6	<b>Transmit output</b>		
	CCU61_COUT61	O7	<b>T12 PWM channel 61</b>		
IOM_MON1_12	<b>Monitor input 1</b>				
IOM_REF1_9	<b>Reference input 1</b>				

表 2-1 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
P7	P00.5	I	SLOW / PU1 / VEXT / ES1	<b>General-purpose input</b>
	GTM_TIM3_IN4_1			<b>Mux input channel 4 of TIM module 3</b>
	GTM_TIM3_IN0_11			<b>Mux input channel 0 of TIM module 3</b>
	GTM_TIM2_IN4_1			<b>Mux input channel 4 of TIM module 2</b>
	CCU60_CC62INB			<b>T12 capture input 62</b>
	EDSADC_DSCIN2A			<b>Modulator clock input, channel 2</b>
	PSI5_RX2A			<b>RXD inputs (receive data) channel 2</b>
	CCU61_CC62INA			<b>T12 capture input 62</b>
	SENT_SENT4B			<b>Receive input channel 4</b>
	CAN11_RXDB			<b>CAN receive input node 1</b>
	GTM_DTMT1_1			<b>CDTM1_DTM0</b>
	GTM_DTMT4_2			<b>CDTM4_DTM0</b>
	EVADC_G9CH7			AI
	P00.5	O0	<b>General-purpose output</b>	
	GTM_TOUT14	O1	<b>GTM muxed output</b>	
	IOM_REF0_14		<b>Reference input 0</b>	
	EDSADC_CGPWMN	O2	<b>Negative carrier generator output</b>	
	QSPI3_SLSO3	O3	<b>Master slave select output</b>	
	EDSADC_DSCOUT2	O4	<b>Modulator clock output</b>	
	EVADC_FC0BFLOUT	O5	<b>Boundary flag output, FC channel 0</b>	
	SENT_SPC4	O6	<b>Transmit output</b>	
	CCU61_CC62	O7	<b>T12 PWM channel 62</b>	
	IOM_MON1_10		<b>Monitor input 1</b>	
IOM_REF1_11		<b>Reference input 1</b>		

表 2-1 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
P9	P00.6	I	SLOW / PU1 / VEXT / ES1	<b>General-purpose input</b>
	GTM_TIM3_IN5_1			<b>Mux input channel 5 of TIM module 3</b>
	GTM_TIM3_IN1_14			<b>Mux input channel 1 of TIM module 3</b>
	GTM_TIM2_IN5_1			<b>Mux input channel 5 of TIM module 2</b>
	EDSADC_ITR4F			<b>Trigger/Gate input, channel 4</b>
	EDSADC_DSDIN2A			<b>Digital datastream input, channel 2</b>
	SENT_SENT5B			<b>Receive input channel 5</b>
	ASCLIN5_ARXA			<b>Receive input</b>
	GTM_DTMA6_0			<b>CDTM6_DTM4</b>
	GTM_DTMT3_1			<b>CDTM3_DTM0</b>
	EVADC_G9CH6	AI	<b>Analog input channel 6, group 9</b>	
	P00.6	O0	<b>General-purpose output</b>	
	GTM_TOUT15	O1	<b>GTM muxed output</b>	
	IOM_REF0_15		<b>Reference input 0</b>	
	EDSADC_CGPWMP	O2	<b>Positive carrier generator output</b>	
	EVADC_FC5BFLOUT	O3	<b>Boundary flag output, FC channel 5</b>	
	PSI5_TX2	O4	<b>TXD outputs (send data)</b>	
	IOM_REF1_15		<b>Reference input 1</b>	
	EVADC_EMUX10	O5	<b>Control of external analog multiplexer interface 1</b>	
	SENT_SPC5	O6	<b>Transmit output</b>	
	CCU61_COUT62	O7	<b>T12 PWM channel 62</b>	
	IOM_MON1_13		<b>Monitor input 1</b>	
	IOM_REF1_8		<b>Reference input 1</b>	

表 2-1 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
R6	P00.7	I	SLOW / PU1 / VEXT / ES1	<b>General-purpose input</b>
	GTM_TIM3_IN6_1			<b>Mux input channel 6 of TIM module 3</b>
	GTM_TIM3_IN2_11			<b>Mux input channel 2 of TIM module 3</b>
	GTM_TIM2_IN6_1			<b>Mux input channel 6 of TIM module 2</b>
	CCU61_CC60INC			<b>T12 capture input 60</b>
	SENT_SENT6B			<b>Receive input channel 6</b>
	EDSADC_DSCIN4A			<b>Modulator clock input, channel 4</b>
	GPT120_T2INA			<b>Trigger/gate input of timer T2</b>
	CCU61_CCPOS0A			<b>Hall capture input 0</b>
	CCU60_T12HRB			<b>External timer start 12</b>
	GTM_DTMT0_2			<b>CDTM0_DTM0</b>
	EVADC_G9CH5	AI	<b>Analog input channel 5, group 9</b>	
	EDSADC_EDS4NA		<b>Negative analog input channel 4, pin A</b>	
	P00.7	O0	<b>General-purpose output</b>	
	GTM_TOUT16	O1	<b>GTM muxed output</b>	
	ASCLIN5_ATX	O2	<b>Transmit output</b>	
	EVADC_FC2BFLOUT	O3	<b>Boundary flag output, FC channel 2</b>	
	EDSADC_DSCOUT4	O4	<b>Modulator clock output</b>	
	EVADC_EMUX11	O5	<b>Control of external analog multiplexer interface 1</b>	
	SENT_SPC6	O6	<b>Transmit output</b>	
	CCU61_CC60	O7	<b>T12 PWM channel 60</b>	
	IOM_MON1_8		<b>Monitor input 1</b>	
	IOM_REF1_13		<b>Reference input 1</b>	

表 2-1 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
R9	P00.8	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM3_IN7_1			Mux input channel 7 of TIM module 3
	GTM_TIM3_IN3_11			Mux input channel 3 of TIM module 3
	GTM_TIM2_IN7_1			Mux input channel 7 of TIM module 2
	CCU61_CC61INC			T12 capture input 61
	SENT_SENT7B			Receive input channel 7
	EDSADC_DSDIN4A			Digital datastream input, channel 4
	GPT120_T2EUDA			Count direction control input of timer T2
	CCU61_CCPOS1A			Hall capture input 1
	CCU60_T13HRB			External timer start 13
	ASCLIN10_ARXB			Receive input
	EVADC_G9CH4			AI
	EDSADC_EDS4PA		Positive analog input channel 4, pin A	
	P00.8	O0	General-purpose output	
	GTM_TOUT17	O1	GTM muxed output	
	QSPI3_SLSO6	O2	Master slave select output	
	ASCLIN10_ATX	O3	Transmit output	
	—	O4	Reserved	
	EVADC_EMUX12	O5	Control of external analog multiplexer interface 1	
	SENT_SPC7	O6	Transmit output	
	CCU61_CC61	O7	T12 PWM channel 61	
	IOM_MON1_9		Monitor input 1	
	IOM_REF1_12		Reference input 1	

表 2-1 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
R7	P00.9	I	SLOW / PU1 / VEXT / ES1	<b>General-purpose input</b>
	GTM_TIM4_IN0_7			<b>Mux input channel 0 of TIM module 4</b>
	GTM_TIM1_IN0_1			<b>Mux input channel 0 of TIM module 1</b>
	GTM_TIM0_IN0_1			<b>Mux input channel 0 of TIM module 0</b>
	CCU61_CC62INC			<b>T12 capture input 62</b>
	SENT_SENT8B			<b>Receive input channel 8</b>
	CCU61_CCPOS2A			<b>Hall capture input 2</b>
	EDSADC_DSCIN1A			<b>Modulator clock input, channel 1</b>
	EDSADC_ITR3F			<b>Trigger/Gate input, channel 3</b>
	GPT120_T4EUDA			<b>Count direction control input of timer T4</b>
	CCU60_T13HRC			<b>External timer start 13</b>
	CCU60_T12HRC			<b>External timer start 12</b>
	EVADC_G9CH3			AI
	EDSADC_EDS4NB	<b>Negative analog input channel 4, pin B</b>		
	P00.9	O0	<b>General-purpose output</b>	
	GTM_TOUT18	O1	<b>GTM muxed output</b>	
	QSPI3_SLSO7	O2	<b>Master slave select output</b>	
	ASCLIN3_ARTS	O3	<b>Ready to send output</b>	
	EDSADC_DSCOUT1	O4	<b>Modulator clock output</b>	
	ASCLIN4_ATX	O5	<b>Transmit output</b>	
	SENT_SPC8	O6	<b>Transmit output</b>	
	CCU61_CC62	O7	<b>T12 PWM channel 62</b>	
	IOM_MON1_10		<b>Monitor input 1</b>	
IOM_REF1_11	<b>Reference input 1</b>			

表 2-1 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
R10	P00.10	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM4_IN1_11			Mux input channel 1 of TIM module 4
	GTM_TIM1_IN1_1			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_1			Mux input channel 1 of TIM module 0
	SENT_SENT9B			Receive input channel 9
	EDSADC_DSDIN1A			Digital datastream input, channel 1
	EVADC_G9CH2			Analog input channel 2, group 9
	EDSADC_EDS4PB	AI		Positive analog input channel 4, pin B
	P00.10	O0		General-purpose output
	GTM_TOUT19	O1		GTM muxed output
	ASCLIN4_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	SENT_SPC9	O6		Transmit output
	CCU61_COUT63	O7		T13 PWM channel 63
	IOM_MON1_7			Monitor input 1
	IOM_REF1_7			Reference input 1
T6	P00.11	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM4_IN2_11			Mux input channel 2 of TIM module 4
	GTM_TIM1_IN2_1			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_1			Mux input channel 2 of TIM module 0
	CCU60_CTRAPA			Trap input capture
	EDSADC_DSCIN0A			Modulator clock input, channel 0
	CCU61_T12HRE			External timer start 12
	SENT_SENT10B	Receive input channel 10		
	EVADC_G9CH1	AI		Analog input channel 1, group 9
	EVADC_FC3CH0			Analog input FC channel 3
	P00.11	O0		General-purpose output
	GTM_TOUT20	O1		GTM muxed output
	ASCLIN4_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	EDSADC_DSCOUT0	O4		Modulator clock output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-1 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
T7	P00.12	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM4_IN3_11			Mux input channel 3 of TIM module 4
	GTM_TIM1_IN3_1			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_1			Mux input channel 3 of TIM module 0
	ASCLIN3_ACTSA			Clear to send input
	EDSADC_DSDIN0A			Digital datastream input, channel 0
	ASCLIN4_ARXA			Receive input
	SENT_SENT11B			Receive input channel 11
	EVADC_G9CH0			AI
	EVADC_FC2CH0		Analog input FC channel 2	
	P00.12	O0	General-purpose output	
	GTM_TOUT21	O1	GTM muxed output	
	—	O2	Reserved	
	—	O3	Reserved	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	CCU61_COUT63	O7	T13 PWM channel 63	
	IOM_MON1_7		Monitor input 1	
IOM_REF1_7		Reference input 1		
T2	P00.13	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM6_IN5_2			Mux input channel 5 of TIM module 6
	GTM_TIM5_IN0_1			Mux input channel 0 of TIM module 5
	GTM_TIM4_IN0_1			Mux input channel 0 of TIM module 4
	EDSADC_DSDIN6A			Digital datastream input, channel 6
	P00.13	O0	General-purpose output	
	GTM_TOUT167	O1	GTM muxed output	
	—	O2	Reserved	
	—	O3	Reserved	
	CCU_EXTCLK1	O4	External Clock 1	
	—	O5	Reserved	
	—	O6	Reserved	
	—	O7	Reserved	

表 2-1 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
U2	P00.14	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM6_IN6_2			<b>Mux input channel 6 of TIM module 6</b>
	GTM_TIM5_IN7_1			<b>Mux input channel 7 of TIM module 5</b>
	GTM_TIM4_IN7_1			<b>Mux input channel 7 of TIM module 4</b>
	EDSADC_DSCIN6A			<b>Modulator clock input, channel 6</b>
	P00.14	O0		<b>General-purpose output</b>
	GTM_TOUT166	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	EDSADC_DSCOUT6	O4		<b>Modulator clock output</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
U1	P00.15	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM6_IN7_2			<b>Mux input channel 7 of TIM module 6</b>
	GTM_TIM5_IN1_1			<b>Mux input channel 1 of TIM module 5</b>
	GTM_TIM4_IN1_1			<b>Mux input channel 1 of TIM module 4</b>
	EDSADC_ITR6F			<b>Trigger/Gate input, channel 6</b>
	P00.15	O0		<b>General-purpose output</b>
	GTM_TOUT168	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	CCU_EXTCLK0	O4		<b>External Clock 0</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>

表 2-2 端口 P01 功能

Ball	Symbol	Ctrl.	Buffer Type	Function	
J2	P01.0	I	SLOW / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM5_IN4_1			Mux input channel 4 of TIM module 5	
	GTM_TIM4_IN4_1			Mux input channel 4 of TIM module 4	
	GTM_TIM2_IN6_13			Mux input channel 6 of TIM module 2	
	CAN21_RXDE			CAN receive input node 1	
	EDSADC_ITR6E			Trigger/Gate input, channel 6	
	CAN03_RXDF			CAN receive input node 3	
	ASCLIN6_ARXB			Receive input	
	P01.0	O0	General-purpose output		
	GTM_TOUT155	O1	GTM muxed output		
	—	O2	Reserved		
	—	O3	Reserved		
	—	O4	Reserved		
	—	O5	Reserved		
—	O6	Reserved			
—	O7	Reserved			
K1	P01.1	I	SLOW / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM5_IN1_2			Mux input channel 1 of TIM module 5	
	GTM_TIM4_IN1_2			Mux input channel 1 of TIM module 4	
	EDSADC_ITR8E			Trigger/Gate input, channel 8	
	ERAY1_RXDA1			Receive Channel A1	
	SENT_SENT15B			Receive input channel 15	
	P01.1			O0	General-purpose output
	GTM_TOUT159			O1	GTM muxed output
	—	O2	Reserved		
	—	O3	Reserved		
	ASCLIN6_ATX	O4	Transmit output		
	—	O5	Reserved		
	—	O6	Reserved		
	—	O7	Reserved		

表 2-2 端口 P01 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
K2	P01.2	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN5_1			Mux input channel 5 of TIM module 5
	GTM_TIM4_IN5_1			Mux input channel 5 of TIM module 4
	EDSADC_DSCIN7A			Modulator clock input, channel 7
	P01.2	O0		General-purpose output
	GTM_TOUT156	O1		GTM muxed output
	—	O2		Reserved
	CAN03_TXD	O3		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	—	O4		Reserved
	CAN21_TXD	O5		CAN transmit output node 1
	EDSADC_DSCOUT7	O6		Modulator clock output
	—	O7		Reserved
M10	P01.3	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN5_2			Mux input channel 5 of TIM module 4
	GTM_TIM2_IN0_14			Mux input channel 0 of TIM module 2
	GTM_TIM0_IN5_8			Mux input channel 5 of TIM module 0
	QSPI3_SLSIB			Slave select input
	EDSADC_ITR7F			Trigger/Gate input, channel 7
	EVADC_G9CH14	AI		Analog input channel 14, group 9
	P01.3	O0		General-purpose output
	GTM_TOUT111	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	QSPI3_SLSO9	O4		Master slave select output
	CAN01_TXD	O5		CAN transmit output node 1
	IOM_MON2_6			Monitor input 2
	IOM_REF2_6			Reference input 2
	—	O6		Reserved
	—	O7		Reserved

表 2-2 端口 P01 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
M9	P01.4	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN6_2			Mux input channel 6 of TIM module 4
	GTM_TIM2_IN1_14			Mux input channel 1 of TIM module 2
	GTM_TIM0_IN6_8			Mux input channel 6 of TIM module 0
	CAN01_RXDC			CAN receive input node 1
	EDSADC_ITR7E			Trigger/Gate input, channel 7
	EVADC_G9CH13	AI		Analog input channel 13, group 9
	P01.4	O0		General-purpose output
	GTM_TOUT112	O1		GTM muxed output
	—	O2		Reserved
	ASCLIN9_ASLSO	O3		Slave select signal output
	QSPI3_SLSO10	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
—	O7	Reserved		
N10	P01.5	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN3_2			Mux input channel 3 of TIM module 5
	GTM_TIM2_IN3_7			Mux input channel 3 of TIM module 2
	GTM_TIM2_IN2_7			Mux input channel 2 of TIM module 2
	QSPI3_MRSTC			Master SPI data input
	EDSADC_DSCIN8A			Modulator clock input, channel 8
	ASCLIN9_ARXA			Receive input
	EVADC_G9CH12	AI		Analog input channel 12, group 9
	P01.5	O0		General-purpose output
	GTM_TOUT113	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	QSPI3_MRST	O4		Slave SPI data output
	IOM_MON2_3			Monitor input 2
	IOM_REF2_3			Reference input 2
	—	O5		Reserved
	EDSADC_DSCOUT8	O6		Modulator clock output
—	O7	Reserved		

表 2-2 端口 P01 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
N9	P01.6	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN6_2			Mux input channel 6 of TIM module 5
	GTM_TIM5_IN5_3			Mux input channel 5 of TIM module 5
	GTM_TIM2_IN5_7			Mux input channel 5 of TIM module 2
	QSPI3_MTSRC			Slave SPI data input
	EDSADC_DSDIN8A			Digital datastream input, channel 8
	P01.6			O0
	GTM_TOUT114	O1		GTM muxed output
	—	O2		Reserved
	ASCLIN9_ASCLK	O3		Shift clock output
	QSPI3_MTSR	O4		Master SPI data output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
P10	P01.7	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN7_2			Mux input channel 7 of TIM module 5
	GTM_TIM2_IN7_7			Mux input channel 7 of TIM module 2
	QSPI3_SCLKC			Slave SPI clock inputs
	EDSADC_ITR8F			Trigger/Gate input, channel 8
	ASCLIN9_ARXB			Receive input
	P01.7			O0
	GTM_TOUT115	O1		GTM muxed output
	—	O2		Reserved
	ASCLIN9_ATX	O3		Transmit output
	QSPI3_SCLK	O4		Master SPI clock output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-2 端口 P01 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
L1	P01.8	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN4_2			Mux input channel 4 of TIM module 5
	GTM_TIM5_IN0_10			Mux input channel 0 of TIM module 5
	GTM_TIM4_IN4_2			Mux input channel 4 of TIM module 4
	CAN00_RXDF			CAN receive input node 0
	ERAY1_RXDB1			Receive Channel B1
	EDSADC_DSDIN9A			Digital datastream input, channel 9
	SENT_SENT17B			Receive input channel 17
	ASCLIN0_ARXC			Receive input
	CAN20_RXDE			CAN receive input node 0
	ASCLIN7_ARXB			Receive input
	P01.8	O0	General-purpose output	
	GTM_TOUT162	O1	GTM muxed output	
	—	O2	Reserved	
	—	O3	Reserved	
	—	O4	Reserved	
	—	O5	Reserved	
—	O6	Reserved		
EVADC_FC4BFLOUT	O7	Boundary flag output, FC channel 4		
L2	P01.9	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN2_1			Mux input channel 2 of TIM module 5
	GTM_TIM5_IN1_11			Mux input channel 1 of TIM module 5
	GTM_TIM4_IN2_1			Mux input channel 2 of TIM module 4
	EDSADC_DSCIN9A			Modulator clock input, channel 9
	SENT_SENT16B			Receive input channel 16
	P01.9	O0	General-purpose output	
	GTM_TOUT160	O1	GTM muxed output	
	ASCLIN7_ATX	O2	Transmit output	
	—	O3	Reserved	
	—	O4	Reserved	
	—	O5	Reserved	
	EDSADC_DSCOUT9	O6	Modulator clock output	
	EVADC_FC5BFLOUT	O7	Boundary flag output, FC channel 5	

表 2-2 端口 P01 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
M2	P01.10	I	SLOW / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM5_IN5_2			Mux input channel 5 of TIM module 5	
	GTM_TIM5_IN2_9			Mux input channel 2 of TIM module 5	
	GTM_TIM4_IN5_3			Mux input channel 5 of TIM module 4	
	EDSADC_ITR9F			Trigger/Gate input, channel 9	
	SENT_SENT18B			Receive input channel 18	
	GTM_DTMT4_0			CDTM4_DTM0	
	GTM_DTMA6_1			CDTM6_DTM4	
	GTM_DTMT3_2			CDTM3_DTM0	
	P01.10			O0	General-purpose output
	GTM_TOUT163			O1	GTM muxed output
	ASCLIN7_ASCLK			O2	Shift clock output
	—			O3	Reserved
	—			O4	Reserved
—	O5	Reserved			
—	O6	Reserved			
EVADC_FC6BFLOUT	O7	Boundary flag output, FC channel 6			
M1	P01.11	I	SLOW / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM5_IN7_3			Mux input channel 7 of TIM module 5	
	GTM_TIM5_IN3_11			Mux input channel 3 of TIM module 5	
	GTM_TIM4_IN7_2			Mux input channel 7 of TIM module 4	
	EDSADC_ITR9E			Trigger/Gate input, channel 9	
	SENT_SENT19B			Receive input channel 19	
	GTM_DTMT4_1			CDTM4_DTM0	
	GTM_DTMA5_1			CDTM5_DTM4	
	GTM_DTMA6_2			CDTM6_DTM4	
	P01.11			O0	General-purpose output
	GTM_TOUT165			O1	GTM muxed output
	ASCLIN7_ASLSO			O2	Slave select signal output
	—			O3	Reserved
	—			O4	Reserved
—	O5	Reserved			
—	O6	Reserved			
EVADC_FC7BFLOUT	O7	Boundary flag output, FC channel 7			

表 2-2 端口 P01 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
N2	P01.12	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM6_IN0_3			<b>Mux input channel 0 of TIM module 6</b>
	GTM_TIM5_IN0_2			<b>Mux input channel 0 of TIM module 5</b>
	GTM_TIM4_IN0_2			<b>Mux input channel 0 of TIM module 4</b>
	EDSADC_DSDIN10A			<b>Digital datastream input, channel 10</b>
	EDSADC_ITR10F			<b>Trigger/Gate input, channel 10</b>
	P01.12	O0		<b>General-purpose output</b>
	GTM_TOUT158	O1		<b>GTM muxed output</b>
	ASCLIN7_ATX	O2		<b>Transmit output</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	ERAY1_TXDA	O6		<b>Transmit Channel A</b>
	—	O7		<b>Reserved</b>
N1	P01.13	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM6_IN1_3			<b>Mux input channel 1 of TIM module 6</b>
	GTM_TIM5_IN3_1			<b>Mux input channel 3 of TIM module 5</b>
	GTM_TIM4_IN3_1			<b>Mux input channel 3 of TIM module 4</b>
	EDSADC_DSCIN10A			<b>Modulator clock input, channel 10</b>
	EDSADC_ITR10E			<b>Trigger/Gate input, channel 10</b>
	P01.13	O0		<b>General-purpose output</b>
	GTM_TOUT161	O1		<b>GTM muxed output</b>
	ASCLIN0_ATX	O2		<b>Transmit output</b>
	IOM_MON2_12			<b>Monitor input 2</b>
	IOM_REF2_12			<b>Reference input 2</b>
	—			O3
	CAN00_TXD	O4		<b>CAN transmit output node 0</b>
	IOM_MON2_5			<b>Monitor input 2</b>
	IOM_REF2_5			<b>Reference input 2</b>
	CAN20_TXD	O5		<b>CAN transmit output node 0</b>
	ERAY1_TXDB	O6		<b>Transmit Channel B</b>
	EDSADC_DSCOUT10	O7		<b>Modulator clock output</b>

表 2-2 端口 P01 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
P2	P01.14	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM6_IN2_3			<b>Mux input channel 2 of TIM module 6</b>
	GTM_TIM5_IN6_3			<b>Mux input channel 6 of TIM module 5</b>
	GTM_TIM4_IN6_3			<b>Mux input channel 6 of TIM module 4</b>
	EDSADC_DSDIN11A			<b>Digital datastream input, channel 11</b>
	EDSADC_ITR11F			<b>Trigger/Gate input, channel 11</b>
	P01.14			O0
	GTM_TOUT164	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	ERAY1_TXENA	O6		<b>Transmit Enable Channel A</b>
	—	O7		<b>Reserved</b>
P1	P01.15	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM6_IN3_3			<b>Mux input channel 3 of TIM module 6</b>
	GTM_TIM5_IN6_1			<b>Mux input channel 6 of TIM module 5</b>
	GTM_TIM4_IN6_1			<b>Mux input channel 6 of TIM module 4</b>
	EDSADC_DSDIN7A			<b>Digital datastream input, channel 7</b>
	EDSADC_DSCIN11A			<b>Modulator clock input, channel 11</b>
	EDSADC_ITR11E			<b>Trigger/Gate input, channel 11</b>
	P01.15	O0		<b>General-purpose output</b>
	GTM_TOUT157	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
EDSADC_DSCOUT11	O7	<b>Modulator clock output</b>		

表 2-3 端口 P02 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
G6	P02.0	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN0_2			<b>Mux input channel 0 of TIM module 1</b>
	GTM_TIM0_IN0_2			<b>Mux input channel 0 of TIM module 0</b>
	CCU61_CC60INB			<b>T12 capture input 60</b>
	ASCLIN2_ARXG			<b>Receive input</b>
	CCU60_CC60INA			<b>T12 capture input 60</b>
	SCU_E_REQ3_2			<b>ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	GTM_DTMA0_0			<b>CDTM0_DTM4</b>
	P02.0			O0
	GTM_TOUT0	O1	<b>GTM muxed output</b>	
	IOM_REF0_0	O2	<b>Reference input 0</b>	
	ASCLIN2_ATX		<b>Transmit output</b>	
	IOM_MON2_14		<b>Monitor input 2</b>	
	IOM_REF2_14	O3	<b>Reference input 2</b>	
	QSPI3_SLSO1		<b>Master slave select output</b>	
	EDSADC_CGPWMN	O4	<b>Negative carrier generator output</b>	
	CAN00_TXD	O5	<b>CAN transmit output node 0</b>	
	IOM_MON2_5	O5	<b>Monitor input 2</b>	
	IOM_REF2_5		<b>Reference input 2</b>	
	ERAY0_TXDA	O6	<b>Transmit Channel A</b>	
	CCU60_CC60	O7	<b>T12 PWM channel 60</b>	
	IOM_MON1_2		<b>Monitor input 1</b>	
	IOM_REF1_6		<b>Reference input 1</b>	

表 2-3 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
H7	P02.1	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN1_2			<b>Mux input channel 1 of TIM module 1</b>
	GTM_TIM0_IN1_2			<b>Mux input channel 1 of TIM module 0</b>
	ERAY0_RXDA2			<b>Receive Channel A2</b>
	ASCLIN2_ARXB			<b>Receive input</b>
	CAN00_RXDA			<b>CAN receive input node 0</b>
	SCU_E_REQ2_1			<b>ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	P02.1	O0		<b>General-purpose output</b>
	GTM_TOUT1	O1		<b>GTM muxed output</b>
	IOM_REF0_1			<b>Reference input 0</b>
	QSPI4_SLSO7	O2		<b>Master slave select output</b>
	QSPI3_SLSO2	O3		<b>Master slave select output</b>
	EDSADC_CGPWMP	O4		<b>Positive carrier generator output</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	CCU60_COUT60	O7		<b>T12 PWM channel 60</b>
	IOM_MON1_3			<b>Monitor input 1</b>
	IOM_REF1_3			<b>Reference input 1</b>

表 2-3 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
H6	P02.2	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN2_2			<b>Mux input channel 2 of TIM module 1</b>
	GTM_TIM0_IN2_2			<b>Mux input channel 2 of TIM module 0</b>
	CCU61_CC61INB			<b>T12 capture input 61</b>
	CCU60_CC61INA			<b>T12 capture input 61</b>
	SENT_SENT14B			<b>Receive input channel 14</b>
	P02.2			O0
	GTM_TOUT2	O1		<b>GTM muxed output</b>
	IOM_REF0_2	O2		<b>Reference input 0</b>
	ASCLIN1_ATX			<b>Transmit output</b>
	IOM_MON2_13			<b>Monitor input 2</b>
	IOM_REF2_13	O3		<b>Reference input 2</b>
	QSPI3_SLSO3			<b>Master slave select output</b>
	PSI5_TX0			<b>TXD outputs (send data)</b>
	IOM_MON1_14	O4		<b>Monitor input 1</b>
	IOM_REF1_14			<b>Reference input 1</b>
	CAN02_TXD	O5		<b>CAN transmit output node 2</b>
	IOM_MON2_7			<b>Monitor input 2</b>
	IOM_REF2_7			<b>Reference input 2</b>
	ERAY0_TXDB	O6		<b>Transmit Channel B</b>
	CCU60_CC61	O7		<b>T12 PWM channel 61</b>
	IOM_MON1_1			<b>Monitor input 1</b>
	IOM_REF1_5			<b>Reference input 1</b>

表 2-3 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
J7	P02.3	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN3_2			<b>Mux input channel 3 of TIM module 1</b>
	GTM_TIM0_IN3_2			<b>Mux input channel 3 of TIM module 0</b>
	EDSADC_DSCIN5B			<b>Modulator clock input, channel 5</b>
	ERAY0_RXDB2			<b>Receive Channel B2</b>
	CAN02_RXDB			<b>CAN receive input node 2</b>
	ASCLIN1_ARXG			<b>Receive input</b>
	MSC1_SDI1			<b>Upstream asynchronous input signal</b>
	PSI5_RX0B			<b>RXD inputs (receive data) channel 0</b>
	SENT_SENT13B			<b>Receive input channel 13</b>
	P02.3			O0
	GTM_TOUT3	O1	<b>GTM muxed output</b>	
	IOM_REF0_3		<b>Reference input 0</b>	
	ASCLIN2_ASLSO	O2	<b>Slave select signal output</b>	
	QSPI3_SLSO4	O3	<b>Master slave select output</b>	
	EDSADC_DSCOUT5	O4	<b>Modulator clock output</b>	
	—	O5	<b>Reserved</b>	
	—	O6	<b>Reserved</b>	
	CCU60_COUT61	O7	<b>T12 PWM channel 61</b>	
	IOM_MON1_4		<b>Monitor input 1</b>	
IOM_REF1_2	<b>Reference input 1</b>			

表 2-3 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
J6	P02.4	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN4_1			<b>Mux input channel 4 of TIM module 1</b>
	GTM_TIM0_IN4_1			<b>Mux input channel 4 of TIM module 0</b>
	CCU61_CC62INB			<b>T12 capture input 62</b>
	EDSADC_DSDIN5B			<b>Digital datastream input, channel 5</b>
	QSPI3_SLSIA			<b>Slave select input</b>
	CCU60_CC62INA			<b>T12 capture input 62</b>
	I2C0_SDAA			<b>Serial Data Input 0</b>
	CAN11_RXDA			<b>CAN receive input node 1</b>
	CAN0_ECTT1			<b>External CAN time trigger input</b>
	SENT_SENT12B			<b>Receive input channel 12</b>
	P02.4	O0		<b>General-purpose output</b>
	GTM_TOUT4	O1		<b>GTM muxed output</b>
	IOM_REF0_4			<b>Reference input 0</b>
	ASCLIN2_ASCLK	O2		<b>Shift clock output</b>
	QSPI3_SLSO0	O3		<b>Master slave select output</b>
	PSI5S_CLK	O4		<b>PSI5S CLK is a clock that can be used on a pin to drive the external PHY.</b>
	I2C0_SDA	O5		<b>Serial Data Output</b>
	ERAY0_TXENA	O6		<b>Transmit Enable Channel A</b>
	CCU60_CC62	O7		<b>T12 PWM channel 62</b>
IOM_MON1_0	<b>Monitor input 1</b>			
IOM_REF1_4	<b>Reference input 1</b>			

表 2-3 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
K7	P02.5	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN5_1			<b>Mux input channel 5 of TIM module 1</b>
	GTM_TIM0_IN5_1			<b>Mux input channel 5 of TIM module 0</b>
	EDSADC_DSCIN4B			<b>Modulator clock input, channel 4</b>
	I2C0_SCLA			<b>Serial Clock Input 0</b>
	PSI5_RX1B			<b>RXD inputs (receive data) channel 1</b>
	PSI5S_RXB			<b>RX data input</b>
	QSPI3_MRSTA			<b>Master SPI data input</b>
	SENT_SENT3C			<b>Receive input channel 3</b>
	CAN0_ECTT2			<b>External CAN time trigger input</b>
	P02.5	O0	<b>General-purpose output</b>	
	GTM_TOUT5	O1	<b>GTM muxed output</b>	
	IOM_REF0_5		<b>Reference input 0</b>	
	CAN11_TXD	O2	<b>CAN transmit output node 1</b>	
	QSPI3_MRST	O3	<b>Slave SPI data output</b>	
	IOM_MON2_3		<b>Monitor input 2</b>	
	IOM_REF2_3		<b>Reference input 2</b>	
	EDSADC_DSCOUT4	O4	<b>Modulator clock output</b>	
	I2C0_SCL	O5	<b>Serial Clock Output</b>	
	ERAY0_TXENB	O6	<b>Transmit Enable Channel B</b>	
CCU60_COUT62	O7	<b>T12 PWM channel 62</b>		
IOM_MON1_5		<b>Monitor input 1</b>		
IOM_REF1_1		<b>Reference input 1</b>		

表 2-3 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
K6	P02.6	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM3_IN0_10			<b>Mux input channel 0 of TIM module 3</b>
	GTM_TIM1_IN6_1			<b>Mux input channel 6 of TIM module 1</b>
	GTM_TIM0_IN6_1			<b>Mux input channel 6 of TIM module 0</b>
	CCU60_CC60INC			<b>T12 capture input 60</b>
	SENT_SENT2C			<b>Receive input channel 2</b>
	EDSADC_DSDIN4B			<b>Digital datastream input, channel 4</b>
	EDSADC_ITR5E			<b>Trigger/Gate input, channel 5</b>
	GPT120_T3INA			<b>Trigger/gate input of core timer T3</b>
	CCU60_CCPOS0A			<b>Hall capture input 0</b>
	CCU61_T12HRB			<b>External timer start 12</b>
	QSPI3_MTSRA			<b>Slave SPI data input</b>
	RIF0_RAMP1B			<b>External RAMP B input</b>
	P02.6			O0
	GTM_TOUT6	O1	<b>GTM muxed output</b>	
	IOM_REF0_6		<b>Reference input 0</b>	
	PSI5S_TX	O2	<b>TX data output</b>	
	QSPI3_MTSR	O3	<b>Master SPI data output</b>	
	PSI5_TX1	O4	<b>TXD outputs (send data)</b>	
	IOM_MON1_15		<b>Monitor input 1</b>	
	EVADC_EMUX00	O5	<b>Control of external analog multiplexer interface 0</b>	
	—	O6	<b>Reserved</b>	
	CCU60_CC60	O7	<b>T12 PWM channel 60</b>	
	IOM_MON1_2		<b>Monitor input 1</b>	
	IOM_REF1_6		<b>Reference input 1</b>	

表 2-3 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
L7	P02.7	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM3_IN1_10			<b>Mux input channel 1 of TIM module 3</b>
	GTM_TIM1_IN7_1			<b>Mux input channel 7 of TIM module 1</b>
	GTM_TIM0_IN7_1			<b>Mux input channel 7 of TIM module 0</b>
	CCU60_CC61INC			<b>T12 capture input 61</b>
	SENT_SENT1C			<b>Receive input channel 1</b>
	EDSADC_DSCIN3B			<b>Modulator clock input, channel 3</b>
	EDSADC_ITR4E			<b>Trigger/Gate input, channel 4</b>
	GPT120_T3EUDA			<b>Count direction control input of core timer T3</b>
	PSI5_RX2B			<b>RXD inputs (receive data) channel 2</b>
	CCU60_CCPOS1A			<b>Hall capture input 1</b>
	QSPI3_SCLKA			<b>Slave SPI clock inputs</b>
	CCU61_T13HRB			<b>External timer start 13</b>
	P02.7	O0	<b>General-purpose output</b>	
	GTM_TOUT7	O1	<b>GTM muxed output</b>	
	IOM_REF0_7		<b>Reference input 0</b>	
	—	O2	<b>Reserved</b>	
	QSPI3_SCLK	O3	<b>Master SPI clock output</b>	
	EDSADC_DSCOUT3	O4	<b>Modulator clock output</b>	
	EVADC_EMUX01	O5	<b>Control of external analog multiplexer interface 0</b>	
SENT_SPC1	O6	<b>Transmit output</b>		
CCU60_CC61	O7	<b>T12 PWM channel 61</b>		
IOM_MON1_1		<b>Monitor input 1</b>		
IOM_REF1_5		<b>Reference input 1</b>		

表 2-3 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
L6	P02.8	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM3_IN2_10			<b>Mux input channel 2 of TIM module 3</b>
	GTM_TIM3_IN0_2			<b>Mux input channel 0 of TIM module 3</b>
	GTM_TIM2_IN0_2			<b>Mux input channel 0 of TIM module 2</b>
	CCU60_CC62INC			<b>T12 capture input 62</b>
	SENT_SENT0C			<b>Receive input channel 0</b>
	CCU60_CCPOS2A			<b>Hall capture input 2</b>
	EDSADC_DSDIN3B			<b>Digital datastream input, channel 3</b>
	EDSADC_ITR3E			<b>Trigger/Gate input, channel 3</b>
	GPT120_T4INA			<b>Trigger/gate input of timer T4</b>
	CCU61_T12HRC			<b>External timer start 12</b>
	CCU61_T13HRC			<b>External timer start 13</b>
	GTM_DTMA0_1			<b>CDTM0_DTM4</b>
	P02.8			00
	GTM_TOUT8	01	<b>GTM muxed output</b>	
	IOM_REF0_8		<b>Reference input 0</b>	
	QSPI3_SLSO5	02	<b>Master slave select output</b>	
	ASCLIN8_ASCLK	03	<b>Shift clock output</b>	
	PSI5_TX2	04	<b>TXD outputs (send data)</b>	
	IOM_REF1_15		<b>Reference input 1</b>	
	EVADC_EMUX02	05	<b>Control of external analog multiplexer interface 0</b>	
	GETH_MDC	06	<b>MDIO clock</b>	
	CCU60_CC62	07	<b>T12 PWM channel 62</b>	
	IOM_MON1_0		<b>Monitor input 1</b>	
	IOM_REF1_4		<b>Reference input 1</b>	

表 2-3 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
K9	P02.9	I	SLOW / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM4_IN2_2			Mux input channel 2 of TIM module 4	
	GTM_TIM3_IN3_10			Mux input channel 3 of TIM module 3	
	GTM_TIM0_IN2_10			Mux input channel 2 of TIM module 0	
	SENT_SENT20B			Receive input channel 20	
	ASCLIN8_ARXA			Receive input	
	P02.9			O0	General-purpose output
	GTM_TOUT116			O1	GTM muxed output
	ASCLIN2_ATX			O2	Transmit output
	IOM_MON2_14				Monitor input 2
	IOM_REF2_14	Reference input 2			
	ASCLIN8_ATX	O3	Transmit output		
	—	O4	Reserved		
	CAN01_TXD	O5	CAN transmit output node 1		
	IOM_MON2_6		Monitor input 2		
	IOM_REF2_6	Reference input 2			
	—	O6	Reserved		
—	O7	Reserved			
L10	P02.10	I	SLOW / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM4_IN3_2			Mux input channel 3 of TIM module 4	
	GTM_TIM3_IN4_11			Mux input channel 4 of TIM module 3	
	GTM_TIM0_IN3_10			Mux input channel 3 of TIM module 0	
	ASCLIN2_ARXC			Receive input	
	CAN01_RXDE			CAN receive input node 1	
	SENT_SENT21B			Receive input channel 21	
	ASCLIN8_ARXB			Receive input	
	P02.10			O0	General-purpose output
	GTM_TOUT117			O1	GTM muxed output
	—	O2	Reserved		
	—	O3	Reserved		
	—	O4	Reserved		
	—	O5	Reserved		
	—	O6	Reserved		
	—	O7	Reserved		

表 2-3 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
L9	P02.11	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM4_IN4_3			<b>Mux input channel 4 of TIM module 4</b>
	GTM_TIM3_IN5_12			<b>Mux input channel 5 of TIM module 3</b>
	GTM_TIM0_IN7_7			<b>Mux input channel 7 of TIM module 0</b>
	SENT_SENT22B			<b>Receive input channel 22</b>
	EVADC_G9CH15	AI		<b>Analog input channel 15, group 9</b>
	P02.11	O0		<b>General-purpose output</b>
	GTM_TOUT118	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	ASCLIN8_ASLSO	O3		<b>Slave select signal output</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
F2	P02.12	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM5_IN0_3			<b>Mux input channel 0 of TIM module 5</b>
	GTM_TIM4_IN0_3			<b>Mux input channel 0 of TIM module 4</b>
	GTM_TIM3_IN6_12			<b>Mux input channel 6 of TIM module 3</b>
	EDSADC_DSDIN12A			<b>Digital datastream input, channel 12</b>
	EDSADC_ITR12F			<b>Trigger/Gate input, channel 12</b>
	SENT_SENT23B			<b>Receive input channel 23</b>
	P02.12	O0		<b>General-purpose output</b>
	GTM_TOUT151	O1		<b>GTM muxed output</b>
	QSPI3_SLSO5	O2		<b>Master slave select output</b>
	QSPI4_SLSO4	O3		<b>Master slave select output</b>
	ASCLIN6_ASLSO	O4		<b>Slave select signal output</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
—	O7	<b>Reserved</b>		

表 2-3 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
F1	P02.13	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN2_2			Mux input channel 2 of TIM module 5
	GTM_TIM4_IN2_3			Mux input channel 2 of TIM module 4
	GTM_TIM3_IN7_11			Mux input channel 7 of TIM module 3
	EDSADC_DSCIN12A			Modulator clock input, channel 12
	EDSADC_ITR12E			Trigger/Gate input, channel 12
	SENT_SENT24B			Receive input channel 24
	P02.13	O0		General-purpose output
	GTM_TOUT153	O1		GTM muxed output
	QSPI3_SLSO7	O2		Master slave select output
	QSPI4_SLSO6	O3		Master slave select output
	CAN00_TXD	O4		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	CAN20_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	EDSADC_DSCOUT12	O7		Modulator clock output
G2	P02.14	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN3_3			Mux input channel 3 of TIM module 5
	GTM_TIM4_IN3_3			Mux input channel 3 of TIM module 4
	GTM_TIM2_IN4_14			Mux input channel 4 of TIM module 2
	CAN20_RXDD			CAN receive input node 0
	CAN00_RXDH			CAN receive input node 0
	EDSADC_DSDIN13A			Digital datastream input, channel 13
	EDSADC_ITR13F			Trigger/Gate input, channel 13
	P02.14			O0
	GTM_TOUT154	O1		GTM muxed output
	ASCLIN6_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-3 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
G1	P02.15	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN1_3			Mux input channel 1 of TIM module 5
	GTM_TIM4_IN1_3			Mux input channel 1 of TIM module 4
	GTM_TIM2_IN5_14			Mux input channel 5 of TIM module 2
	EDSADC_DSCIN13A			Modulator clock input, channel 13
	EDSADC_ITR13E			Trigger/Gate input, channel 13
	P02.15			O0
	GTM_TOUT152	O1		GTM muxed output
	QSPI3_SLSO6	O2		Master slave select output
	QSPI4_SLSO5	O3		Master slave select output
	ASCLIN6_ATX	O4		Transmit output
	—	O5		Reserved
	ERAY1_TXENB	O6		Transmit Enable Channel B
	EDSADC_DSCOUT13	O7		Modulator clock output

表 2-4 端口 P10 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
F12	P10.0	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN0_12			Mux input channel 0 of TIM module 4
	GTM_TIM1_IN4_2			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_2			Mux input channel 4 of TIM module 0
	GPT120_T6EUIDB			Count direction control input of core timer T6
	ASCLIN11_ARXA			Receive input
	GETH_RXERC			Receive Error MII
	GTM_DTMA5_2			CDTM5_DTM4
	P10.0	O0		General-purpose output
	GTM_TOUT102	O1		GTM muxed output
	ASCLIN11_ATX	O2		Transmit output
	QSPI1_SLSO10	O3		Master slave select output
	—	O4		Reserved
	EVADC_FC6BFLOUT	O5		Boundary flag output, FC channel 6
—	O6	Reserved		
—	O7	Reserved		

表 2-4 端口 P10 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
G12	P10.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN4_12			Mux input channel 4 of TIM module 4
	GTM_TIM1_IN1_3			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_3			Mux input channel 1 of TIM module 0
	GPT120_T5EUDB			Count direction control input of timer T5
	QSPI1_MRSTA			Master SPI data input
	GTM_DTMT0_1			CDTM0_DTM0
	P10.1	O0	General-purpose output	
	GTM_TOUT103	O1	GTM muxed output	
	QSPI1_MTSR	O2	Master SPI data output	
	QSPI1_MRST	O3	Slave SPI data output	
	IOM_MON2_1		Monitor input 2	
	IOM_REF2_1		Reference input 2	
	MSC0_EN1	O4	Chip Select	
	EVADC_FC1BFLOUT	O5	Boundary flag output, FC channel 1	
	—	O6	Reserved	
	—	O7	Reserved	
F10	P10.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN5_12			Mux input channel 5 of TIM module 4
	GTM_TIM1_IN2_3			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_3			Mux input channel 2 of TIM module 0
	CAN02_RXDE			CAN receive input node 2
	MSC0_SDI1			Upstream asynchronous input signal
	QSPI1_SCLKA			Slave SPI clock inputs
	GPT120_T6INB			Trigger/gate input of core timer T6
	SCU_E_REQ2_0			ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	GTM_DTMT2_2	CDTM2_DTM0		
	P10.2	O0	General-purpose output	
	GTM_TOUT104	O1	GTM muxed output	
	IOM_MON2_9		Monitor input 2	
	—		Reserved	
	QSPI1_SCLK	O3	Master SPI clock output	
	MSC0_EN0	O4	Chip Select	
	EVADC_FC3BFLOUT	O5	Boundary flag output, FC channel 3	
—	O6	Reserved		
—	O7	Reserved		

表 2-4 端口 P10 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
F11	P10.3	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN6_10			Mux input channel 6 of TIM module 4
	GTM_TIM1_IN3_3			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_3			Mux input channel 3 of TIM module 0
	QSPI1_MTSRA			Slave SPI data input
	SCU_E_REQ3_0			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	GPT120_T5INB			Trigger/gate input of timer T5
	P10.3	O0	General-purpose output	
	GTM_TOUT105	O1	GTM muxed output	
	IOM_MON2_10	O2	Monitor input 2	
	—		Reserved	
	QSPI1_MTSR	O3	Master SPI data output	
	MSC0_EN0	O4	Chip Select	
	—	O5	Reserved	
	CAN02_TXD	O6	CAN transmit output node 2	
	IOM_MON2_7	O7	Monitor input 2	
	IOM_REF2_7		Reference input 2	
—	Reserved			
G11	P10.4	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN7_3			Mux input channel 7 of TIM module 4
	GTM_TIM1_IN6_2			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_2			Mux input channel 6 of TIM module 0
	QSPI1_MTSRC			Slave SPI data input
	CCU60_CCPOS0C			Hall capture input 0
	GPT120_T3INB			Trigger/gate input of core timer T3
	ASCLIN11_ARXB	Receive input		
	P10.4	O0	General-purpose output	
	GTM_TOUT106	O1	GTM muxed output	
	IOM_MON2_11	O2	Monitor input 2	
	—		Reserved	
	QSPI1_SLSO8	O3	Master slave select output	
	QSPI1_MTSR	O4	Master SPI data output	
	MSC0_EN0	O5	Chip Select	
	—	O6	Reserved	
	—	O7	Reserved	

表 2-4 端口 P10 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
G10	P10.5	I	SLOW / PU2 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM4_IN3_13			<b>Mux input channel 3 of TIM module 4</b>
	GTM_TIM1_IN2_4			<b>Mux input channel 2 of TIM module 1</b>
	GTM_TIM0_IN2_4			<b>Mux input channel 2 of TIM module 0</b>
	PMS_HWCFG4IN			<b>HWCFG4 pin input</b>
	CAN20_RXDA			<b>CAN receive input node 0</b>
	MSC0_INJ1			<b>Injection signal from port</b>
	P10.5	O0		<b>General-purpose output</b>
	GTM_TOUT107	O1		<b>GTM muxed output</b>
	IOM_REF2_9			<b>Reference input 2</b>
	ASCLIN2_ATX	O2		<b>Transmit output</b>
	IOM_MON2_14			<b>Monitor input 2</b>
	IOM_REF2_14			<b>Reference input 2</b>
	QSPI3_SLSO8	O3		<b>Master slave select output</b>
	QSPI1_SLSO9	O4		<b>Master slave select output</b>
	GPT120_T6OUT	O5		<b>External output for overflow/underflow detection of core timer T6</b>
	ASCLIN2_ASLSO	O6		<b>Slave select signal output</b>
	PSI5_TX3	O7		<b>TXD outputs (send data)</b>

表 2-4 端口 P10 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
F9	P10.6	I	SLOW / PU2 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM4_IN2_13			<b>Mux input channel 2 of TIM module 4</b>
	GTM_TIM1_IN3_4			<b>Mux input channel 3 of TIM module 1</b>
	GTM_TIM0_IN3_4			<b>Mux input channel 3 of TIM module 0</b>
	PSI5_RX3C			<b>RXD inputs (receive data) channel 3</b>
	ASCLIN2_ARXD			<b>Receive input</b>
	QSPI3_MTSRB			<b>Slave SPI data input</b>
	PMS_HWCFG5IN			<b>HWCFG5 pin input</b>
	P10.6	O0	<b>General-purpose output</b>	
	GTM_TOUT108	O1	<b>GTM muxed output</b>	
	IOM_REF2_10		<b>Reference input 2</b>	
	ASCLIN2_ASCLK	O2	<b>Shift clock output</b>	
	QSPI3_MTSR	O3	<b>Master SPI data output</b>	
	GPT120_T3OUT	O4	<b>External output for overflow/underflow detection of core timer T3</b>	
	CAN20_TXD	O5	<b>CAN transmit output node 0</b>	
	QSPI1_MRST	O6	<b>Slave SPI data output</b>	
	IOM_MON2_1		<b>Monitor input 2</b>	
	IOM_REF2_1		<b>Reference input 2</b>	
	EVADC_FC7BFLOUT	O7	<b>Boundary flag output, FC channel 7</b>	

表 2-4 端口 P10 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
F8	P10.7	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN0_3			<b>Mux input channel 0 of TIM module 1</b>
	GTM_TIM0_IN0_3			<b>Mux input channel 0 of TIM module 0</b>
	GPT120_T3EUIDB			<b>Count direction control input of core timer T3</b>
	ASCLIN2_ACTSA			<b>Clear to send input</b>
	QSPI3_MRSTB			<b>Master SPI data input</b>
	SCU_E_REQ0_2			<b>ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	CCU60_CCPOS1C			<b>Hall capture input 1</b>
	P10.7	O0	<b>General-purpose output</b>	
	GTM_TOUT109	O1	<b>GTM muxed output</b>	
	IOM_REF2_11	O2	<b>Reference input 2</b>	
	—		<b>Reserved</b>	
	QSPI3_MRST	O3	<b>Slave SPI data output</b>	
	IOM_MON2_3		<b>Monitor input 2</b>	
	IOM_REF2_3		<b>Reference input 2</b>	
	—	O4	<b>Reserved</b>	
	CAN20_TXD	O5	<b>CAN transmit output node 0</b>	
	CAN12_TXD	O6	<b>CAN transmit output node 2</b>	
	—	O7	<b>Reserved</b>	

表 2-4 端口 P10 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
G9	P10.8	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM4_IN0_13			<b>Mux input channel 0 of TIM module 4</b>
	GTM_TIM1_IN5_2			<b>Mux input channel 5 of TIM module 1</b>
	GTM_TIM0_IN5_2			<b>Mux input channel 5 of TIM module 0</b>
	CAN12_RXDB			<b>CAN receive input node 2</b>
	GPT120_T4INB			<b>Trigger/gate input of timer T4</b>
	QSPI3_SCLKB			<b>Slave SPI clock inputs</b>
	SCU_E_REQ1_2			<b>ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	CCU60_CCPOS2C			<b>Hall capture input 2</b>
	CAN20_RXDB			<b>CAN receive input node 0</b>
	RIF1_RAMP1B	<b>External RAMP B input</b>		
	P10.8	O0	<b>General-purpose output</b>	
	GTM_TOUT110	O1	<b>GTM muxed output</b>	
	ASCLIN2_ARTS	O2	<b>Ready to send output</b>	
	QSPI3_SCLK	O3	<b>Master SPI clock output</b>	
	—	O4	<b>Reserved</b>	
	—	O5	<b>Reserved</b>	
—	O6	<b>Reserved</b>		
—	O7	<b>Reserved</b>		
B8	P10.9	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM6_IN0_5			<b>Mux input channel 0 of TIM module 6</b>
	GTM_TIM4_IN1_4			<b>Mux input channel 1 of TIM module 4</b>
	GTM_TIM0_IN1_10			<b>Mux input channel 1 of TIM module 0</b>
	SENT_SENT15C			<b>Receive input channel 15</b>
	ASCLIN6_ARXD			<b>Receive input</b>
	P10.9	O0	<b>General-purpose output</b>	
	GTM_TOUT265	O1	<b>GTM muxed output</b>	
	—	O2	<b>Reserved</b>	
	—	O3	<b>Reserved</b>	
	—	O4	<b>Reserved</b>	
	—	O5	<b>Reserved</b>	
	—	O6	<b>Reserved</b>	
	—	O7	<b>Reserved</b>	

表 2-4 端口 P10 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
B7	P10.10	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM6_IN1_5			<b>Mux input channel 1 of TIM module 6</b>
	GTM_TIM4_IN2_4			<b>Mux input channel 2 of TIM module 4</b>
	GTM_TIM0_IN2_11			<b>Mux input channel 2 of TIM module 0</b>
	SENT_SENT16C			<b>Receive input channel 16</b>
	P10.10	O0		<b>General-purpose output</b>
	GTM_TOUT266	O1		<b>GTM muxed output</b>
	ASCLIN6_ATX	O2		<b>Transmit output</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
—	O7	<b>Reserved</b>		
A7	P10.11	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM6_IN2_5			<b>Mux input channel 2 of TIM module 6</b>
	GTM_TIM4_IN5_4			<b>Mux input channel 5 of TIM module 4</b>
	GTM_TIM0_IN5_9			<b>Mux input channel 5 of TIM module 0</b>
	SENT_SENT19C			<b>Receive input channel 19</b>
	P10.11	O0		<b>General-purpose output</b>
	GTM_TOUT269	O1		<b>GTM muxed output</b>
	ASCLIN6_ASCLK	O2		<b>Shift clock output</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
—	O7	<b>Reserved</b>		

表 2-4 端口 P10 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A6	P10.13	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM6_IN3_5			Mux input channel 3 of TIM module 6
	GTM_TIM4_IN4_4			Mux input channel 4 of TIM module 4
	GTM_TIM0_IN4_9			Mux input channel 4 of TIM module 0
	SENT_SENT18C			Receive input channel 18
	P10.13	O0		General-purpose output
	GTM_TOUT268	O1		GTM muxed output
	ASCLIN6_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
—	O7	Reserved		
B5	P10.14	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM7_IN0_4			Mux input channel 0 of TIM module 7
	GTM_TIM4_IN3_4			Mux input channel 3 of TIM module 4
	GTM_TIM0_IN3_11			Mux input channel 3 of TIM module 0
	SENT_SENT17C			Receive input channel 17
	P10.14	O0		General-purpose output
	GTM_TOUT267	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
—	O7	Reserved		
A5	P10.15	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM7_IN1_4			Mux input channel 1 of TIM module 7
	GTM_TIM4_IN6_4			Mux input channel 6 of TIM module 4
	GTM_TIM0_IN6_9			Mux input channel 6 of TIM module 0
	P10.15			O0
	GTM_TOUT270	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-5 端口 P11 的功能

Ball	Symbol	Ctrl.	Buffer Type	Function
K15	P11.0	I	RFAST / PU1 / VFLEX / ES	<b>General-purpose input</b>
	GTM_TIM7_IN5_1			<b>Mux input channel 5 of TIM module 7</b>
	GTM_TIM4_IN0_4			<b>Mux input channel 0 of TIM module 4</b>
	GTM_TIM2_IN0_7			<b>Mux input channel 0 of TIM module 2</b>
	ASCLIN3_ARXB			<b>Receive input</b>
	GTM_DTMA2_1			<b>CDTM2_DTM4</b>
	P11.0	O0		<b>General-purpose output</b>
	GTM_TOUT119	O1		<b>GTM muxed output</b>
	ASCLIN3_ATX	O2		<b>Transmit output</b>
	IOM_MON2_15			<b>Monitor input 2</b>
	IOM_REF2_15			<b>Reference input 2</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	CAN11_TXD	O5		<b>CAN transmit output node 1</b>
	GETH_TXD3	O6		<b>Transmit Data</b>
—	O7	<b>Reserved</b>		
K14	P11.1	I	RFAST / PU1 / VFLEX / ES	<b>General-purpose input</b>
	GTM_TIM7_IN6_1			<b>Mux input channel 6 of TIM module 7</b>
	GTM_TIM4_IN1_5			<b>Mux input channel 1 of TIM module 4</b>
	GTM_TIM2_IN1_6			<b>Mux input channel 1 of TIM module 2</b>
	P11.1	O0		<b>General-purpose output</b>
	GTM_TOUT120	O1		<b>GTM muxed output</b>
	ASCLIN3_ASCLK	O2		<b>Shift clock output</b>
	ASCLIN3_ATX	O3		<b>Transmit output</b>
	IOM_MON2_15			<b>Monitor input 2</b>
	IOM_REF2_15			<b>Reference input 2</b>
	—	O4		<b>Reserved</b>
	CAN12_TXD	O5		<b>CAN transmit output node 2</b>
	GETH_TXD2	O6		<b>Transmit Data</b>
	—	O7		<b>Reserved</b>

表 2-5 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
F15	P11.2	I	RFAST / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM3_IN1_3			Mux input channel 1 of TIM module 3
	GTM_TIM2_IN1_3			Mux input channel 1 of TIM module 2
	P11.2	O0		General-purpose output
	GTM_TOUT95	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO5	O3		Master slave select output
	QSPI1_SLSO5	O4		Master slave select output
	MSC0_EN1	O5		Chip Select
	GETH_TXD1	O6		Transmit Data
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1
	G15	P11.3		I
GTM_TIM3_IN2_2		Mux input channel 2 of TIM module 3		
GTM_TIM2_IN2_2		Mux input channel 2 of TIM module 2		
MSC0_SDI3		Upstream asynchronous input signal		
QSPI1_MRSTB		Master SPI data input		
P11.3		O0	General-purpose output	
GTM_TOUT96		O1	GTM muxed output	
—		O2	Reserved	
QSPI1_MRST		O3	Slave SPI data output	
IOM_MON2_1			Monitor input 2	
IOM_REF2_1			Reference input 2	
ERAY0_TXDA			O4	Transmit Channel A
—		O5	Reserved	
GETH_TXD0		O6	Transmit Data	
CCU60_COUT62		O7	T12 PWM channel 62	
IOM_MON1_5			Monitor input 1	
IOM_REF1_1			Reference input 1	

表 2-5 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
J15	P11.4	I	RFAST / PU1 / VFLEX / ES	<b>General-purpose input</b>
	GTM_TIM7_IN7_1			<b>Mux input channel 7 of TIM module 7</b>
	GTM_TIM4_IN2_5			<b>Mux input channel 2 of TIM module 4</b>
	GTM_TIM2_IN2_6			<b>Mux input channel 2 of TIM module 2</b>
	GETH_RXCLKB			<b>Receive Clock MII</b>
	P11.4	O0		<b>General-purpose output</b>
	GTM_TOUT121	O1		<b>GTM muxed output</b>
	ASCLIN3_ASCLK	O2		<b>Shift clock output</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	CAN13_TXD	O5		<b>CAN transmit output node 3</b>
	GETH_TXER	O6		<b>Transmit Error MII</b>
	GETH_TXCLK	O7		<b>Transmit Clock Output for RGMII</b>
J13	P11.5	I	SLOW / RGMII_In put / PU1 / VFLEX / ES	<b>General-purpose input</b>
	GTM_TIM4_IN3_5			<b>Mux input channel 3 of TIM module 4</b>
	GTM_TIM2_IN3_8			<b>Mux input channel 3 of TIM module 2</b>
	GETH_TXCLKA			<b>Transmit Clock Input for MII</b>
	GETH_GREFCLK			<b>Gigabit Reference Clock input for RGMII (125 MHz high precision)</b>
	P11.5	O0		<b>General-purpose output</b>
	GTM_TOUT122	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	CAN20_TXD	O5		<b>CAN transmit output node 0</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>

表 2-5 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
J14	P11.6	I	RFAST / PU1 / VFLEX / ES	<b>General-purpose input</b>
	GTM_TIM3_IN3_2			<b>Mux input channel 3 of TIM module 3</b>
	GTM_TIM2_IN3_2			<b>Mux input channel 3 of TIM module 2</b>
	QSPI1_SCLKB			<b>Slave SPI clock inputs</b>
	P11.6	O0		<b>General-purpose output</b>
	GTM_TOUT97	O1		<b>GTM muxed output</b>
	ERAY0_TXENB	O2		<b>Transmit Enable Channel B</b>
	QSPI1_SCLK	O3		<b>Master SPI clock output</b>
	ERAY0_TXENA	O4		<b>Transmit Enable Channel A</b>
	MSC0_FCLP	O5		<b>Shift-clock direct part of the differential signal</b>
	GETH_TXEN	O6		<b>Transmit Enable MII and RMII</b>
	GETH_TCTL			<b>Transmit Control for RGMII</b>
	CCU60_COUT61	O7		<b>T12 PWM channel 61</b>
	IOM_MON1_4			<b>Monitor input 1</b>
IOM_REF1_2	<b>Reference input 1</b>			
K13	P11.7	I	SLOW / RGMII_In put / PU1 / VFLEX / ES	<b>General-purpose input</b>
	GTM_TIM4_IN4_5			<b>Mux input channel 4 of TIM module 4</b>
	GTM_TIM2_IN4_7			<b>Mux input channel 4 of TIM module 2</b>
	GETH_RXD3A			<b>Receive Data 3 MII and RGMII (RGMII can use RXD3A only)</b>
	CAN11_RXDD			<b>CAN receive input node 1</b>
	P11.7	O0		<b>General-purpose output</b>
	GTM_TOUT123	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>

表 2-5 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
K12	P11.8	I	SLOW / RGMII_In put / PU1 / VFLEX / ES	<b>General-purpose input</b>
	GTM_TIM4_IN5_5			<b>Mux input channel 5 of TIM module 4</b>
	GTM_TIM2_IN5_8			<b>Mux input channel 5 of TIM module 2</b>
	GETH_RXD2A			<b>Receive Data 2 MII and RGMII (RGMII can use RXD2A only)</b>
	CAN12_RXDD			<b>CAN receive input node 2</b>
	P11.8	O0		<b>General-purpose output</b>
	GTM_TOUT124	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
F14	P11.9	I	FAST / RGMII_In put / PU1 / VFLEX / ES	<b>General-purpose input</b>
	GTM_TIM3_IN4_2			<b>Mux input channel 4 of TIM module 3</b>
	GTM_TIM2_IN4_2			<b>Mux input channel 4 of TIM module 2</b>
	QSPI1_MTSRB			<b>Slave SPI data input</b>
	ERAY0_RXDA1			<b>Receive Channel A1</b>
	GETH_RXD1A			<b>Receive Data 1 MII, RMII and RGMII (RGMII can use RXD1A only)</b>
	P11.9	O0		<b>General-purpose output</b>
	GTM_TOUT98	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	QSPI1_MTSR	O3		<b>Master SPI data output</b>
	—	O4		<b>Reserved</b>
	MSC0_SOP	O5		<b>Data output - direct part of the differential signal</b>
	—	O6		<b>Reserved</b>
	CCU60_COUT60	O7		<b>T12 PWM channel 60</b>
IOM_MON1_3		<b>Monitor input 1</b>		
IOM_REF1_3		<b>Reference input 1</b>		

表 2-5 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
G14	P11.10	I	FAST / RGMII_Input / PU1 / VFLEX / ES	<b>General-purpose input</b>	
	GTM_TIM3_IN5_2			<b>Mux input channel 5 of TIM module 3</b>	
	GTM_TIM2_IN5_2			<b>Mux input channel 5 of TIM module 2</b>	
	GTM_TIM2_IN0_9			<b>Mux input channel 0 of TIM module 2</b>	
	CAN03_RXDD			<b>CAN receive input node 3</b>	
	ERAY0_RXDB1			<b>Receive Channel B1</b>	
	ASCLIN1_ARXE			<b>Receive input</b>	
	SCU_E_REQ6_3			<b>ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>	
	MSC0_SDI0			<b>Upstream asynchronous input signal</b>	
	GETH_RXD0A			<b>Receive Data 0 MII, RMII and RGMII (RGMII can use RXD0A only)</b>	
	QSPI1_SLSIA			<b>Slave select input</b>	
	P11.10			O0	<b>General-purpose output</b>
	GTM_TOUT99			O1	<b>GTM muxed output</b>
	—	O2	<b>Reserved</b>		
	QSPI0_SLSO3	O3	<b>Master slave select output</b>		
	QSPI1_SLSO3	O4	<b>Master slave select output</b>		
	—	O5	<b>Reserved</b>		
	—	O6	<b>Reserved</b>		
	CCU60_CC62	O7	<b>T12 PWM channel 62</b>		
	IOM_MON1_0		<b>Monitor input 1</b>		
IOM_REF1_4	<b>Reference input 1</b>				

表 2-5 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
F13	P11.11	I	FAST / RGMII_In put / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM3_IN6_2			Mux input channel 6 of TIM module 3
	GTM_TIM3_IN0_14			Mux input channel 0 of TIM module 3
	GTM_TIM2_IN6_2			Mux input channel 6 of TIM module 2
	GETH_CRSDVA			Carrier Sense / Data Valid combi-signal for RMII
	GETH_RXDVA			Receive Data Valid MII
	GETH_CRSB			Carrier Sense MII
	GETH_RCTLA			Receive Control for RGMII
	P11.11			O0
	GTM_TOUT100	O1	GTM muxed output	
	—	O2	Reserved	
	QSPI0_SLSO4	O3	Master slave select output	
	QSPI1_SLSO4	O4	Master slave select output	
	MSC0_EN0	O5	Chip Select	
	ERAY0_TXENB	O6	Transmit Enable Channel B	
	CCU60_CC61	O7	T12 PWM channel 61	
	IOM_MON1_1		Monitor input 1	
	IOM_REF1_5		Reference input 1	
G13	P11.12	I	FAST / RGMII_In put / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM3_IN7_2			Mux input channel 7 of TIM module 3
	GTM_TIM2_IN7_2			Mux input channel 7 of TIM module 2
	GETH_REFCLKA			Reference Clock input for RMII (50 MHz)
	GETH_TXCLKB			Transmit Clock Input for MII
	GETH_RXCLKA			Receive Clock MII
	P11.12	O0	General-purpose output	
	GTM_TOUT101	O1	GTM muxed output	
	ASCLIN1_ATX	O2	Transmit output	
	IOM_MON2_13		Monitor input 2	
	IOM_REF2_13		Reference input 2	
	GTM_CLK2	O3	CGM generated clock	
	ERAY0_TXDB	O4	Transmit Channel B	
	CAN03_TXD	O5	CAN transmit output node 3	
	IOM_MON2_8		Monitor input 2	
	IOM_REF2_8		Reference input 2	
	CCU_EXTCLK1	O6	External Clock 1	
	CCU60_CC60	O7	T12 PWM channel 60	
	IOM_MON1_2		Monitor input 1	
	IOM_REF1_6		Reference input 1	

表 2-5 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
K11	P11.13	I	SLOW / PU1 / VFLEX / ES	General-purpose input	
	GTM_TIM4_IN6_5			Mux input channel 6 of TIM module 4	
	GTM_TIM2_IN6_7			Mux input channel 6 of TIM module 2	
	GETH_RXERA			Receive Error MII	
	I2C1_SDAA			Serial Data Input 0	
	CAN13_RXDD			CAN receive input node 3	
	P11.13			00	General-purpose output
	GTM_TOUT125			01	GTM muxed output
	—			02	Reserved
	—			03	Reserved
	—			04	Reserved
	—			05	Reserved
	I2C1_SDA			06	Serial Data Output
	—			07	Reserved
J12	P11.14	I	SLOW / PU1 / VFLEX / ES	General-purpose input	
	GTM_TIM4_IN7_4			Mux input channel 7 of TIM module 4	
	GTM_TIM2_IN7_8			Mux input channel 7 of TIM module 2	
	GETH_CRSDVB			Carrier Sense / Data Valid combi-signal for RMII	
	GETH_RXDVB			Receive Data Valid MII	
	GETH_CRSA			Carrier Sense MII	
	I2C1_SCLA			Serial Clock Input 0	
	CAN20_RXDF			CAN receive input node 0	
	P11.14			00	General-purpose output
	GTM_TOUT126			01	GTM muxed output
	—			02	Reserved
	—			03	Reserved
	—			04	Reserved
	—			05	Reserved
I2C1_SCL	06	Serial Clock Output			
—	07	Reserved			

表 2-5 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
J11	P11.15	I	SLOW / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM4_IN7_5			Mux input channel 7 of TIM module 4
	GTM_TIM0_IN7_8			Mux input channel 7 of TIM module 0
	GETH_COLA			Collision MII
	P11.15	O0		General-purpose output
	GTM_TOUT127	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-6 端口 P12 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
K17	P12.0	I	SLOW / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM7_IN3_2			Mux input channel 3 of TIM module 7
	GTM_TIM4_IN0_5			Mux input channel 0 of TIM module 4
	GTM_TIM3_IN0_7			Mux input channel 0 of TIM module 3
	CAN00_RXDC			CAN receive input node 0
	GETH_RXCLKC			Receive Clock MII
	GTM_DTMA4_0			CDTM4_DTM4
	P12.0	O0		General-purpose output
	GTM_TOUT128	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
GETH_MDC	O6	MDIO clock		
—	O7	Reserved		

表 2-6 端口 P12 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
K16	P12.1	I	SLOW / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM7_IN4_1			Mux input channel 4 of TIM module 7
	GTM_TIM4_IN1_6			Mux input channel 1 of TIM module 4
	GTM_TIM3_IN1_6			Mux input channel 1 of TIM module 3
	GETH_MDIOC			MDIO Input
	P12.1	O0		General-purpose output
	GTM_TOUT129	O1		GTM muxed output
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	CAN00_TXD	O5		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	—	O6		Reserved
	—	O7		Reserved
	GETH_MDIO	O		MDIO Output

表 2-7 端口 P13 的功能

Ball	Symbol	Ctrl.	Buffer Type	Function
G17	P13.0	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM3_IN5_3			Mux input channel 5 of TIM module 3
	GTM_TIM2_IN5_3			Mux input channel 5 of TIM module 2
	ASCLIN10_ARXC			Receive input
	P13.0	O0		General-purpose output
	GTM_TOUT91	O1		GTM muxed output
	ASCLIN10_ATX	O2		Transmit output
	QSPI2_SCLKN	O3		Master SPI clock output (LVDS N line)
	MSC0_EN1	O4		Chip Select
	MSC0_FCLN	O5		Shift-clock inverted part of the differential signal
	—	O6		Reserved
	CAN10_TXD	O7		CAN transmit output node 0

表 2-7 端口 P13 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
F17	P13.1	I	LVDS_TX / FAST / PU1 / VEXT / ES6	<b>General-purpose input</b>	
	GTM_TIM3_IN6_3			<b>Mux input channel 6 of TIM module 3</b>	
	GTM_TIM2_IN6_3			<b>Mux input channel 6 of TIM module 2</b>	
	I2C0_SCLB			<b>Serial Clock Input 1</b>	
	CAN10_RXDD			<b>CAN receive input node 0</b>	
	ASCLIN10_ARXD			<b>Receive input</b>	
	P13.1			O0	<b>General-purpose output</b>
	GTM_TOUT92	O1		<b>GTM muxed output</b>	
	—	O2		<b>Reserved</b>	
	QSPI2_SCLKP	O3		<b>Master SPI clock output (LVDS P line)</b>	
	—	O4		<b>Reserved</b>	
	MSC0_FCLP	O5		<b>Shift-clock direct part of the differential signal</b>	
	I2C0_SCL	O6		<b>Serial Clock Output</b>	
	—	O7		<b>Reserved</b>	
G16	P13.2	I	LVDS_TX / FAST / PU1 / VEXT / ES6	<b>General-purpose input</b>	
	GTM_TIM3_IN7_3			<b>Mux input channel 7 of TIM module 3</b>	
	GTM_TIM2_IN7_3			<b>Mux input channel 7 of TIM module 2</b>	
	GPT120_CAPINA			<b>Trigger input to capture value of timer T5 into CAPREL register</b>	
	I2C0_SDAB			<b>Serial Data Input 1</b>	
	P13.2			O0	<b>General-purpose output</b>
	GTM_TOUT93			O1	<b>GTM muxed output</b>
	ASCLIN10_ASCLK	O2		<b>Shift clock output</b>	
	QSPI2_MTSRN	O3		<b>Master SPI data output (LVDS N line)</b>	
	MSC0_FCLP	O4		<b>Shift-clock direct part of the differential signal</b>	
	MSC0_SON	O5		<b>Data output - inverted part of the differential signal</b>	
	I2C0_SDA	O6		<b>Serial Data Output</b>	
	—	O7		<b>Reserved</b>	

表 2-7 端口 P13 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
F16	P13.3	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input	
	GTM_TIM3_IN0_3			Mux input channel 0 of TIM module 3	
	GTM_TIM2_IN0_3			Mux input channel 0 of TIM module 2	
	P13.3			O0	General-purpose output
	GTM_TOUT94	O1		GTM muxed output	
	ASCLIN10_ASLSO	O2		Slave select signal output	
	QSPI2_MTSRP	O3		Master SPI data output (LVDS P line)	
	—	O4		Reserved	
	MSC0_SOP	O5		Data output - direct part of the differential signal	
	—	O6		Reserved	
	—	O7		Reserved	
B16	P13.4	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input	
	GTM_TIM6_IN0_4			Mux input channel 0 of TIM module 6	
	GTM_TIM5_IN3_4			Mux input channel 3 of TIM module 5	
	GTM_TIM3_IN3_8			Mux input channel 3 of TIM module 3	
	P13.4	O0		General-purpose output	
	GTM_TOUT253	O1		GTM muxed output	
	—	O2		Reserved	
	—	O3		Reserved	
	MSC2_EN0	O4		Chip Select	
	MSC2_FCLN	O5		Shift-clock inverted part of the differential signal	
	—	O6		Reserved	
CAN23_TXD	O7	CAN transmit output node 3			
A16	P13.5	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input	
	GTM_TIM6_IN1_4			Mux input channel 1 of TIM module 6	
	GTM_TIM5_IN4_4			Mux input channel 4 of TIM module 5	
	GTM_TIM3_IN4_9			Mux input channel 4 of TIM module 3	
	CAN23_RXDD	O0		CAN receive input node 3	
	P13.5			General-purpose output	
	GTM_TOUT254			O1	GTM muxed output
	—			O2	Reserved
	—			O3	Reserved
	—			O4	Reserved
	MSC2_FCLP			O5	Shift-clock direct part of the differential signal
—	O6	Reserved			
—	O7	Reserved			

表 2-7 端口 P13 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
B15	P13.6	I	LVDS_TX / FAST / PU1 / VEXT / ES6	<b>General-purpose input</b>
	GTM_TIM6_IN2_4			<b>Mux input channel 2 of TIM module 6</b>
	GTM_TIM5_IN5_4			<b>Mux input channel 5 of TIM module 5</b>
	GTM_TIM3_IN5_10			<b>Mux input channel 5 of TIM module 3</b>
	P13.6	O0		<b>General-purpose output</b>
	GTM_TOUT255	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	MSC2_SON	O5		<b>Data output - inverted part of the differential signal</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
A15	P13.7	I	LVDS_TX / FAST / PU1 / VEXT / ES6	<b>General-purpose input</b>
	GTM_TIM6_IN3_4			<b>Mux input channel 3 of TIM module 6</b>
	GTM_TIM5_IN6_4			<b>Mux input channel 6 of TIM module 5</b>
	GTM_TIM3_IN6_10			<b>Mux input channel 6 of TIM module 3</b>
	P13.7	O0		<b>General-purpose output</b>
	GTM_TOUT256	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	MSC2_SOP	O5		<b>Data output - direct part of the differential signal</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>

表 2-7 端口 P13 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A14	P13.9	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM6_IN4_4			<b>Mux input channel 4 of TIM module 6</b>
	GTM_TIM4_IN7_6			<b>Mux input channel 7 of TIM module 4</b>
	GTM_TIM2_IN7_12			<b>Mux input channel 7 of TIM module 2</b>
	I2C1_SCLB			<b>Serial Clock Input 1</b>
	P13.9	O0		<b>General-purpose output</b>
	GTM_TOUT248	O1		<b>GTM muxed output</b>
	ASCLIN3_ATX	O2		<b>Transmit output</b>
	IOM_MON2_15			<b>Monitor input 2</b>
	IOM_REF2_15			<b>Reference input 2</b>
	QSPI5_SLSO5	O3		<b>Master slave select output</b>
	—	O4		<b>Reserved</b>
	CAN21_TXD	O5		<b>CAN transmit output node 1</b>
	I2C1_SCL	O6		<b>Serial Clock Output</b>
—	O7	<b>Reserved</b>		
B13	P13.10	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM6_IN5_4			<b>Mux input channel 5 of TIM module 6</b>
	GTM_TIM5_IN1_5			<b>Mux input channel 1 of TIM module 5</b>
	GTM_TIM3_IN1_8			<b>Mux input channel 1 of TIM module 3</b>
	PSI5_RX3A			<b>RXD inputs (receive data) channel 3</b>
	MSC3_SDIO			<b>Upstream asynchronous input signal</b>
	P13.10	O0		<b>General-purpose output</b>
	GTM_TOUT251	O1		<b>GTM muxed output</b>
	ASCLIN0_ATX	O2		<b>Transmit output</b>
	IOM_MON2_12			<b>Monitor input 2</b>
	IOM_REF2_12			<b>Reference input 2</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
—	O6	<b>Reserved</b>		
—	O7	<b>Reserved</b>		

表 2-7 端口 P13 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A13	P13.11	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM6_IN6_4			<b>Mux input channel 6 of TIM module 6</b>
	GTM_TIM5_IN0_9			<b>Mux input channel 0 of TIM module 5</b>
	GTM_TIM3_IN0_9			<b>Mux input channel 0 of TIM module 3</b>
	ASCLIN0_ARXE			<b>Receive input</b>
	ASCLIN7_ARXD			<b>Receive input</b>
	MSC3_INJ0			<b>Injection signal from port</b>
	P13.11	O0		<b>General-purpose output</b>
	GTM_TOUT250	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	PSI5_TX3	O4		<b>TXD outputs (send data)</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
—	O7	<b>Reserved</b>		
B12	P13.12	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM6_IN7_4			<b>Mux input channel 7 of TIM module 6</b>
	GTM_TIM4_IN0_6			<b>Mux input channel 0 of TIM module 4</b>
	GTM_TIM0_IN0_11			<b>Mux input channel 0 of TIM module 0</b>
	ASCLIN3_ARXH			<b>Receive input</b>
	I2C1_SDAB			<b>Serial Data Input 1</b>
	CAN21_RXDB			<b>CAN receive input node 1</b>
	P13.12	O0		<b>General-purpose output</b>
	GTM_TOUT249	O1		<b>GTM muxed output</b>
	ASCLIN7_ATX	O2		<b>Transmit output</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	I2C1_SDA	O6		<b>Serial Data Output</b>
—	O7	<b>Reserved</b>		

表 2-7 端口 P13 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A12	P13.13	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM7_IN0_3			Mux input channel 0 of TIM module 7
	GTM_TIM5_IN5_5			Mux input channel 5 of TIM module 5
	GTM_TIM3_IN5_9			Mux input channel 5 of TIM module 3
	MSC2_INJ0			Injection signal from port
	PSI5_RX3B			RXD inputs (receive data) channel 3
	P13.13	O0		General-purpose output
	GTM_TOUT262	O1		GTM muxed output
	ASCLIN7_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
—	O7	Reserved		
B11	P13.14	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM7_IN1_3			Mux input channel 1 of TIM module 7
	GTM_TIM5_IN2_4			Mux input channel 2 of TIM module 5
	GTM_TIM3_IN2_7			Mux input channel 2 of TIM module 3
	P13.14	O0		General-purpose output
	GTM_TOUT252	O1		GTM muxed output
	—	O2		Reserved
	QSPI5_SLSO4	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	A11	P13.15		I
GTM_TIM7_IN2_3		Mux input channel 2 of TIM module 7		
GTM_TIM5_IN7_4		Mux input channel 7 of TIM module 5		
GTM_TIM3_IN7_9		Mux input channel 7 of TIM module 3		
P13.15		O0	General-purpose output	
GTM_TOUT264		O1	GTM muxed output	
ASCLIN7_ASLSO		O2	Slave select signal output	
—		O3	Reserved	
PSI5_TX3		O4	TXD outputs (send data)	
—		O5	Reserved	
—		O6	Reserved	
—		O7	Reserved	

表 2-8 端口 P14 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
G21	P14.0	I	FAST / PU1 / VEXT / ES2	<b>General-purpose input</b>
	GTM_TIM1_IN3_5			<b>Mux input channel 3 of TIM module 1</b>
	GTM_TIM0_IN3_5			<b>Mux input channel 3 of TIM module 0</b>
	SENT_SENT17D			<b>Receive input channel 17</b>
	P14.0	O0		<b>General-purpose output</b>
	GTM_TOUT80	O1		<b>GTM muxed output</b>
	ASCLIN0_ATX	O2		<b>Transmit output</b>
	IOM_MON2_12			<b>Monitor input 2</b>
	IOM_REF2_12			<b>Reference input 2</b>
	ERAY0_TXDA	O3		<b>Transmit Channel A</b>
	ERAY0_TXDB	O4		<b>Transmit Channel B</b>
	CAN01_TXD	O5		<b>CAN transmit output node 1</b>
	IOM_MON2_6			<b>Monitor input 2</b>
	IOM_REF2_6			<b>Reference input 2</b>
	ASCLIN0_ASCLK	O6		<b>Shift clock output</b>
	CCU60_COUT62	O7		<b>T12 PWM channel 62</b>
	IOM_MON1_5			<b>Monitor input 1</b>
	IOM_REF1_1			<b>Reference input 1</b>

表 2-8 端口 P14 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
F20	P14.1	I	FAST / PU1 / VEXT / ES2	<b>General-purpose input</b>
	GTM_TIM1_IN4_3			<b>Mux input channel 4 of TIM module 1</b>
	GTM_TIM0_IN4_3			<b>Mux input channel 4 of TIM module 0</b>
	ERAY0_RXDA3			<b>Receive Channel A3</b>
	ASCLIN0_ARXA			<b>Receive input</b>
	SENT_SENT18D			<b>Receive input channel 18</b>
	ERAY0_RXDB3			<b>Receive Channel B3</b>
	CAN01_RXDB			<b>CAN receive input node 1</b>
	SCU_E_REQ3_1			<b>ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	PMS_PINAWKP			<b>PINA ( P14.1) pin input</b>
	P14.1	00	<b>General-purpose output</b>	
	GTM_TOUT81	01	<b>GTM muxed output</b>	
	ASCLIN0_ATX	02	<b>Transmit output</b>	
	IOM_MON2_12		<b>Monitor input 2</b>	
	IOM_REF2_12	<b>Reference input 2</b>		
	—	03	<b>Reserved</b>	
	—	04	<b>Reserved</b>	
	—	05	<b>Reserved</b>	
	—	06	<b>Reserved</b>	
	CCU60_COUT63	07	<b>T13 PWM channel 63</b>	
IOM_MON1_6	<b>Monitor input 1</b>			
IOM_REF1_0	<b>Reference input 1</b>			
K18	P14.2	I	SLOW / PU2 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN5_3			<b>Mux input channel 5 of TIM module 1</b>
	GTM_TIM0_IN5_3			<b>Mux input channel 5 of TIM module 0</b>
	PMS_HWCFG2IN			<b>HWCFG2 pin input</b>
	P14.2	00	<b>General-purpose output</b>	
	GTM_TOUT82	01	<b>GTM muxed output</b>	
	ASCLIN2_ATX	02	<b>Transmit output</b>	
	IOM_MON2_14		<b>Monitor input 2</b>	
	IOM_REF2_14		<b>Reference input 2</b>	
	QSPI2_SLSO1	03	<b>Master slave select output</b>	
	—	04	<b>Reserved</b>	
	—	05	<b>Reserved</b>	
	ASCLIN2_ASCLK	06	<b>Shift clock output</b>	
	—	07	<b>Reserved</b>	

表 2-8 端口 P14 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
G19	P14.3	I	SLOW / PU2 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN6_3			<b>Mux input channel 6 of TIM module 1</b>
	GTM_TIM0_IN6_3			<b>Mux input channel 6 of TIM module 0</b>
	PMS_HWCFG3IN			<b>HWCFG3 pin input</b>
	ASCLIN2_ARXA			<b>Receive input</b>
	MSC0_SDI2			<b>Upstream asynchronous input signal</b>
	SCU_E_REQ1_0			<b>ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	P14.3	O0	<b>General-purpose output</b>	
	GTM_TOUT83	O1	<b>GTM muxed output</b>	
	ASCLIN2_ATX	O2	<b>Transmit output</b>	
	IOM_MON2_14		<b>Monitor input 2</b>	
	IOM_REF2_14		<b>Reference input 2</b>	
	QSPI2_SLSO3	O3	<b>Master slave select output</b>	
	ASCLIN1_ASLSO	O4	<b>Slave select signal output</b>	
	ASCLIN3_ASLSO	O5	<b>Slave select signal output</b>	
	—	O6	<b>Reserved</b>	
	—	O7	<b>Reserved</b>	
G20	P14.4	I	SLOW / PU2 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN7_2			<b>Mux input channel 7 of TIM module 1</b>
	GTM_TIM0_IN7_2			<b>Mux input channel 7 of TIM module 0</b>
	PMS_HWCFG6IN			<b>HWCFG6 pin input</b>
	GTM_DTMT0_0			<b>CDTMO_DTM0</b>
	P14.4	O0	<b>General-purpose output</b>	
	GTM_TOUT84	O1	<b>GTM muxed output</b>	
	—	O2	<b>Reserved</b>	
	—	O3	<b>Reserved</b>	
	—	O4	<b>Reserved</b>	
	—	O5	<b>Reserved</b>	
	GETH_PPS	O6	<b>Pulse Per Second</b>	
	—	O7	<b>Reserved</b>	

表 2-8 端口 P14 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
F19	P14.5	I	FAST / PU2 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN0_4			<b>Mux input channel 0 of TIM module 1</b>
	GTM_TIM0_IN0_4			<b>Mux input channel 0 of TIM module 0</b>
	PMS_HWCFG1IN			<b>HWCFG1 pin input</b>
	QSPI5_MRSTB			<b>Master SPI data input</b>
	GTM_DTMA2_0			<b>CDTM2_DTM4</b>
	P14.5			00
	GTM_TOUT85	01		<b>GTM muxed output</b>
	—	02		<b>Reserved</b>
	QSPI5_MRST	03		<b>Slave SPI data output</b>
	—	04		<b>Reserved</b>
	—	05		<b>Reserved</b>
	ERAY0_TXDB	06		<b>Transmit Channel B</b>
	ERAY1_TXDB	07		<b>Transmit Channel B</b>
G18	P14.6	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN1_4			<b>Mux input channel 1 of TIM module 1</b>
	GTM_TIM0_IN1_4			<b>Mux input channel 1 of TIM module 0</b>
	QSPI5_MTSRB			<b>Slave SPI data input</b>
	P14.6	00		<b>General-purpose output</b>
	GTM_TOUT86	01		<b>GTM muxed output</b>
	QSPI5_MTSR	02		<b>Master SPI data output</b>
	QSPI2_SLSO2	03		<b>Master slave select output</b>
	CAN13_TXD	04		<b>CAN transmit output node 3</b>
	—	05		<b>Reserved</b>
	ERAY0_TXENB	06		<b>Transmit Enable Channel B</b>
	ERAY1_TXENB	07		<b>Transmit Enable Channel B</b>

表 2-8 端口 P14 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
J18	P14.7	I	SLOW / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM4_IN7_10			Mux input channel 7 of TIM module 4	
	GTM_TIM1_IN0_5			Mux input channel 0 of TIM module 1	
	GTM_TIM0_IN0_5			Mux input channel 0 of TIM module 0	
	ERAY0_RXDB0			Receive Channel B0	
	ERAY1_RXDB0			Receive Channel B0	
	CAN10_RXDB			CAN receive input node 0	
	CAN13_RXDA			CAN receive input node 3	
	ASCLIN9_ARXC			Receive input	
	P14.7	O0	General-purpose output		
	GTM_TOUT87	O1	GTM muxed output		
	ASCLIN0_ARTS	O2	Ready to send output		
	QSPI2_SLSO4	O3	Master slave select output		
	ASCLIN9_ATX	O4	Transmit output		
	—	O5	Reserved		
	—	O6	Reserved		
	—	O7	Reserved		
F18	P14.8	I	SLOW / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM3_IN2_3			Mux input channel 2 of TIM module 3	
	GTM_TIM2_IN2_3			Mux input channel 2 of TIM module 2	
	ERAY0_RXDA0			Receive Channel A0	
	CAN02_RXDD			CAN receive input node 2	
	ASCLIN1_ARXD			Receive input	
	ERAY1_RXDA0			Receive Channel A0	
	P14.8			O0	General-purpose output
	GTM_TOUT88			O1	GTM muxed output
	ASCLIN5_ASLSO	O2	Slave select signal output		
	ASCLIN7_ASLSO	O3	Slave select signal output		
	—	O4	Reserved		
	—	O5	Reserved		
	—	O6	Reserved		
	—	O7	Reserved		

表 2-8 端口 P14 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
J17	P14.9	I	LVDS_RX / FAST / PU1 / VEXT / ES	<b>General-purpose input</b>	
	GTM_TIM3_IN3_3			<b>Mux input channel 3 of TIM module 3</b>	
	GTM_TIM2_IN3_3			<b>Mux input channel 3 of TIM module 2</b>	
	ASCLIN0_ACTSA			<b>Clear to send input</b>	
	QSPI2_MRSTFN			<b>Master SPI data input (LVDS N line)</b>	
	ASCLIN9_ARXD			<b>Receive input</b>	
	P14.9			O0	<b>General-purpose output</b>
	GTM_TOUT89	O1	<b>GTM muxed output</b>		
	CAN23_TXD	O2	<b>CAN transmit output node 3</b>		
	MSC0_EN1	O3	<b>Chip Select</b>		
	CAN10_TXD	O4	<b>CAN transmit output node 0</b>		
	ERAY0_TXENB	O5	<b>Transmit Enable Channel B</b>		
	ERAY0_TXENA	O6	<b>Transmit Enable Channel A</b>		
	ERAY1_TXENA	O7	<b>Transmit Enable Channel A</b>		
J16	P14.10	I	LVDS_RX / FAST / PU1 / VEXT / ES	<b>General-purpose input</b>	
	GTM_TIM3_IN4_3			<b>Mux input channel 4 of TIM module 3</b>	
	GTM_TIM2_IN4_3			<b>Mux input channel 4 of TIM module 2</b>	
	CAN23_RXDA			<b>CAN receive input node 3</b>	
	QSPI2_MRSTFP			<b>Master SPI data input (LVDS P line)</b>	
	P14.10			O0	<b>General-purpose output</b>
	GTM_TOUT90			O1	<b>GTM muxed output</b>
	QSPI5_SCLK	O2	<b>Master SPI clock output</b>		
	MSC0_EN0	O3	<b>Chip Select</b>		
	ASCLIN1_ATX	O4	<b>Transmit output</b>		
	IOM_MON2_13		<b>Monitor input 2</b>		
	IOM_REF2_13		<b>Reference input 2</b>		
	CAN02_TXD	O5	<b>CAN transmit output node 2</b>		
	IOM_MON2_7		<b>Monitor input 2</b>		
	IOM_REF2_7		<b>Reference input 2</b>		
	ERAY0_TXDA	O6	<b>Transmit Channel A</b>		
	ERAY1_TXDA	O7	<b>Transmit Channel A</b>		

表 2-8 端口 P14 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A20	P14.11	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM7_IN6_2			Mux input channel 6 of TIM module 7
	GTM_TIM5_IN1_4			Mux input channel 1 of TIM module 5
	GTM_TIM3_IN1_9			Mux input channel 1 of TIM module 3
	MSC2_SDI1			Upstream asynchronous input signal
	P14.11	O0		General-purpose output
	GTM_TOUT258	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	MSC2_EN2	O4		Chip Select
	MSC2_SOP	O5		Data output - direct part of the differential signal
	—	O6		Reserved
	—	O7		Reserved
	B19	P14.12		I
GTM_TIM6_IN4_3		Mux input channel 4 of TIM module 6		
GTM_TIM5_IN4_5		Mux input channel 4 of TIM module 5		
GTM_TIM3_IN4_8		Mux input channel 4 of TIM module 3		
MSC2_SDI0		Upstream asynchronous input signal		
P14.12		O0	General-purpose output	
GTM_TOUT261		O1	GTM muxed output	
ASCLIN5_ASCLK		O2	Shift clock output	
ASCLIN7_ASCLK		O3	Shift clock output	
—		O4	Reserved	
—		O5	Reserved	
QSPI5_SLSO6		O6	Master slave select output	
—		O7	Reserved	

表 2-8 端口 P14 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A19	P14.13	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM6_IN5_3			<b>Mux input channel 5 of TIM module 6</b>
	GTM_TIM5_IN3_5			<b>Mux input channel 3 of TIM module 5</b>
	GTM_TIM3_IN3_6			<b>Mux input channel 3 of TIM module 3</b>
	QSPI5_SCLKB			<b>Slave SPI clock inputs</b>
	P14.13	O0		<b>General-purpose output</b>
	GTM_TOUT260	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	QSPI5_SCLK	O3		<b>Master SPI clock output</b>
	MSC2_EN1	O4		<b>Chip Select</b>
	CAN22_TXD	O5		<b>CAN transmit output node 2</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
B18	P14.14	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM6_IN6_3			<b>Mux input channel 6 of TIM module 6</b>
	GTM_TIM5_IN2_3			<b>Mux input channel 2 of TIM module 5</b>
	GTM_TIM3_IN2_8			<b>Mux input channel 2 of TIM module 3</b>
	CAN22_RXDD			<b>CAN receive input node 2</b>
	P14.14	O0		<b>General-purpose output</b>
	GTM_TOUT259	O1		<b>GTM muxed output</b>
	ASCLIN5_ATX	O2		<b>Transmit output</b>
	ASCLIN7_ATX	O3		<b>Transmit output</b>
	MSC2_EN0	O4		<b>Chip Select</b>
	CAN23_TXD	O5		<b>CAN transmit output node 3</b>
	QSPI5_SLSO7	O6		<b>Master slave select output</b>
	—	O7		<b>Reserved</b>

表 2-8 端口 P14 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A18	P14.15	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM6_IN7_3			<b>Mux input channel 7 of TIM module 6</b>
	GTM_TIM5_IN6_5			<b>Mux input channel 6 of TIM module 5</b>
	GTM_TIM3_IN6_9			<b>Mux input channel 6 of TIM module 3</b>
	MSC2_INJ1			<b>Injection signal from port</b>
	ASCLIN5_ARXD			<b>Receive input</b>
	ASCLIN7_ARXA			<b>Receive input</b>
	CAN23_RXDC			<b>CAN receive input node 3</b>
	MSC3_INJ1			<b>Injection signal from port</b>
	P14.15			O0
	GTM_TOUT263	O1	<b>GTM muxed output</b>	
	ASCLIN1_ATX	O2	<b>Transmit output</b>	
	IOM_MON2_13		<b>Monitor input 2</b>	
	IOM_REF2_13		<b>Reference input 2</b>	
	—	O3	<b>Reserved</b>	
	—	O4	<b>Reserved</b>	
	—	O5	<b>Reserved</b>	
	QSPI5_SLSO8	O6	<b>Master slave select output</b>	
	—	O7	<b>Reserved</b>	

表 2-9 端口 P15 功能

Ball	Symbol	Ctrl.	Buffer Type	Function	
G25	P15.0	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>	
	GTM_TIM3_IN3_4			<b>Mux input channel 3 of TIM module 3</b>	
	GTM_TIM2_IN3_4			<b>Mux input channel 3 of TIM module 2</b>	
	SDMMC0_DAT7_IN			<b>read data in</b>	
	P15.0			O0	<b>General-purpose output</b>
	GTM_TOUT71			O1	<b>GTM muxed output</b>
	ASCLIN1_ATX			O2	<b>Transmit output</b>
	IOM_MON2_13				<b>Monitor input 2</b>
	IOM_REF2_13				<b>Reference input 2</b>
	QSPI0_SLSO13			O3	<b>Master slave select output</b>
	—	O4	<b>Reserved</b>		
	CAN02_TXD	O5	<b>CAN transmit output node 2</b>		
	IOM_MON2_7		<b>Monitor input 2</b>		
	IOM_REF2_7		<b>Reference input 2</b>		
	ASCLIN1_ASCLK	O6	<b>Shift clock output</b>		
	—	O7	<b>Reserved</b>		
	SDMMC0_DAT7	O	<b>write data out</b>		
F23	P15.1	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>	
	GTM_TIM3_IN4_4			<b>Mux input channel 4 of TIM module 3</b>	
	GTM_TIM2_IN4_4			<b>Mux input channel 4 of TIM module 2</b>	
	CAN02_RXDA			<b>CAN receive input node 2</b>	
	ASCLIN1_ARXA			<b>Receive input</b>	
	QSPI2_SLSIB			<b>Slave select input</b>	
	SCU_E_REQ7_2			<b>ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>	
	P15.1			O0	<b>General-purpose output</b>
	GTM_TOUT72			O1	<b>GTM muxed output</b>
	ASCLIN1_ATX			O2	<b>Transmit output</b>
	IOM_MON2_13	<b>Monitor input 2</b>			
	IOM_REF2_13	<b>Reference input 2</b>			
	QSPI2_SLSO5	O3	<b>Master slave select output</b>		
	—	O4	<b>Reserved</b>		
	—	O5	<b>Reserved</b>		
	—	O6	<b>Reserved</b>		
	SDMMC0_CLK	O7	<b>card clock</b>		

表 2-9 端口 P15 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
H24	P15.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN5_4			Mux input channel 5 of TIM module 3
	GTM_TIM2_IN5_4			Mux input channel 5 of TIM module 2
	QSPI2_SLSIA			Slave select input
	SENT_SENT10D			Receive input channel 10
	QSPI2_MRSTE			Master SPI data input
	QSPI2_HSICINA			Highspeed capture channel
	P15.2			O0
	GTM_TOUT73	O1	GTM muxed output	
	ASCLIN0_ATX	O2	Transmit output	
	IOM_MON2_12		Monitor input 2	
	IOM_REF2_12		Reference input 2	
	QSPI2_SLSO0	O3	Master slave select output	
	—	O4	Reserved	
	CAN01_TXD	O5	CAN transmit output node 1	
	IOM_MON2_6		Monitor input 2	
	IOM_REF2_6		Reference input 2	
	ASCLIN0_ASCLK	O6	Shift clock output	
	—	O7	Reserved	
G22	P15.3	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN6_4			Mux input channel 6 of TIM module 3
	GTM_TIM2_IN6_4			Mux input channel 6 of TIM module 2
	CAN01_RXDA			CAN receive input node 1
	ASCLIN0_ARXB			Receive input
	QSPI2_SCLKA			Slave SPI clock inputs
	QSPI2_HSICINB			Highspeed capture channel
	SDMMC0_CMD_IN			command in
	P15.3	O0	General-purpose output	
	GTM_TOUT74	O1	GTM muxed output	
	ASCLIN0_ATX	O2	Transmit output	
	IOM_MON2_12		Monitor input 2	
	IOM_REF2_12		Reference input 2	
	QSPI2_SCLK	O3	Master SPI clock output	
	—	O4	Reserved	
	MSC0_EN1	O5	Chip Select	
	—	O6	Reserved	
	—	O7	Reserved	
	SDMMC0_CMD	O	command out	

表 2-9 端口 P15 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
F22	P15.4	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM3_IN7_4			<b>Mux input channel 7 of TIM module 3</b>
	GTM_TIM2_IN7_4			<b>Mux input channel 7 of TIM module 2</b>
	I2C0_SCLC			<b>Serial Clock Input 2</b>
	QSPI2_MRSTA			<b>Master SPI data input</b>
	SCU_E_REQ0_0			<b>ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	SENT_SENT11D			<b>Receive input channel 11</b>
	P15.4	O0	<b>General-purpose output</b>	
	GTM_TOUT75	O1	<b>GTM muxed output</b>	
	ASCLIN1_ATX	O2	<b>Transmit output</b>	
	IOM_MON2_13		<b>Monitor input 2</b>	
	IOM_REF2_13		<b>Reference input 2</b>	
	QSPI2_MRST	O3	<b>Slave SPI data output</b>	
	IOM_MON2_2		<b>Monitor input 2</b>	
	IOM_REF2_2		<b>Reference input 2</b>	
	—	O4	<b>Reserved</b>	
	—	O5	<b>Reserved</b>	
	I2C0_SCL	O6	<b>Serial Clock Output</b>	
	CCU60_CC62	O7	<b>T12 PWM channel 62</b>	
	IOM_MON1_0		<b>Monitor input 1</b>	
IOM_REF1_4	<b>Reference input 1</b>			

表 2-9 端口 P15 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
K19	P15.5	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM3_IN0_4			<b>Mux input channel 0 of TIM module 3</b>
	GTM_TIM2_IN0_4			<b>Mux input channel 0 of TIM module 2</b>
	ASCLIN1_ARXB			<b>Receive input</b>
	I2C0_SDAC			<b>Serial Data Input 2</b>
	QSPI2_MTSRA			<b>Slave SPI data input</b>
	SCU_E_REQ4_3			<b>ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	P15.5	O0	<b>General-purpose output</b>	
	GTM_TOUT76	O1	<b>GTM muxed output</b>	
	ASCLIN1_ATX	O2	<b>Transmit output</b>	
	IOM_MON2_13		<b>Monitor input 2</b>	
	IOM_REF2_13		<b>Reference input 2</b>	
	QSPI2_MTSR	O3	<b>Master SPI data output</b>	
	—	O4	<b>Reserved</b>	
	MSC0_EN0	O5	<b>Chip Select</b>	
	I2C0_SDA	O6	<b>Serial Data Output</b>	
	CCU60_CC61	O7	<b>T12 PWM channel 61</b>	
	IOM_MON1_1		<b>Monitor input 1</b>	
	IOM_REF1_5		<b>Reference input 1</b>	
	F21	P15.6	I	FAST / PU1 / VEXT / ES
GTM_TIM2_IN2_14		<b>Mux input channel 2 of TIM module 2</b>		
GTM_TIM1_IN0_6		<b>Mux input channel 0 of TIM module 1</b>		
GTM_TIM0_IN0_6		<b>Mux input channel 0 of TIM module 0</b>		
QSPI2_MTSRB		<b>Slave SPI data input</b>		
P15.6		O0	<b>General-purpose output</b>	
GTM_TOUT77		O1	<b>GTM muxed output</b>	
ASCLIN3_ATX		O2	<b>Transmit output</b>	
IOM_MON2_15			<b>Monitor input 2</b>	
IOM_REF2_15			<b>Reference input 2</b>	
QSPI2_MTSR		O3	<b>Master SPI data output</b>	
QSPI5_SLSO3		O4	<b>Master slave select output</b>	
QSPI2_SCLK		O5	<b>Master SPI clock output</b>	
ASCLIN3_ASCLK		O6	<b>Shift clock output</b>	
CCU60_CC60		O7	<b>T12 PWM channel 60</b>	
IOM_MON1_2			<b>Monitor input 1</b>	
IOM_REF1_6			<b>Reference input 1</b>	

表 2-9 端口 P15 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
J20	P15.7	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN1_5			<b>Mux input channel 1 of TIM module 1</b>
	GTM_TIM0_IN1_5			<b>Mux input channel 1 of TIM module 0</b>
	ASCLIN3_ARXA			<b>Receive input</b>
	QSPI2_MRSTB			<b>Master SPI data input</b>
	P15.7	O0		<b>General-purpose output</b>
	GTM_TOUT78	O1		<b>GTM muxed output</b>
	ASCLIN3_ATX	O2		<b>Transmit output</b>
	IOM_MON2_15			<b>Monitor input 2</b>
	IOM_REF2_15			<b>Reference input 2</b>
	QSPI2_MRST	O3		<b>Slave SPI data output</b>
	IOM_MON2_2			<b>Monitor input 2</b>
	IOM_REF2_2			<b>Reference input 2</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	CCU60_COUT60	O7		<b>T12 PWM channel 60</b>
	IOM_MON1_3			<b>Monitor input 1</b>
	IOM_REF1_3			<b>Reference input 1</b>
J19	P15.8	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN2_5			<b>Mux input channel 2 of TIM module 1</b>
	GTM_TIM0_IN2_5			<b>Mux input channel 2 of TIM module 0</b>
	QSPI2_SCLKB			<b>Slave SPI clock inputs</b>
	SCU_E_REQ5_0			<b>ERU Channel 5 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	P15.8	O0		<b>General-purpose output</b>
	GTM_TOUT79	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	QSPI2_SCLK	O3		<b>Master SPI clock output</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	ASCLIN3_ASCLK	O6		<b>Shift clock output</b>
	CCU60_COUT61	O7		<b>T12 PWM channel 61</b>
	IOM_MON1_4			<b>Monitor input 1</b>
	IOM_REF1_2			<b>Reference input 1</b>

表 2-9 端口 P15 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
B24	P15.10	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input	
	GTM_TIM7_IN0_2			Mux input channel 0 of TIM module 7	
	GTM_TIM4_IN1_7			Mux input channel 1 of TIM module 4	
	GTM_TIM2_IN1_8			Mux input channel 1 of TIM module 2	
	QSPI5_MRSTA			Master SPI data input	
	P15.10			O0	General-purpose output
	GTM_TOUT242			O1	GTM muxed output
	—			O2	Reserved
	QSPI5_MRST			O3	Slave SPI data output
	MSC3_FCLN			O4	Shift-clock inverted part of the differential signal
	—			O5	Reserved
	—			O6	Reserved
—	O7	Reserved			
A24	P15.11	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input	
	GTM_TIM7_IN1_2			Mux input channel 1 of TIM module 7	
	GTM_TIM4_IN2_6			Mux input channel 2 of TIM module 4	
	GTM_TIM2_IN2_8			Mux input channel 2 of TIM module 2	
	QSPI5_SLSIA			Slave select input	
	P15.11			O0	General-purpose output
	GTM_TOUT243			O1	GTM muxed output
	—			O2	Reserved
	QSPI5_SLSO2			O3	Master slave select output
	MSC3_FCLP			O4	Shift-clock direct part of the differential signal
	—			O5	Reserved
	—			O6	Reserved
—	O7	Reserved			
B23	P15.12	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input	
	GTM_TIM7_IN2_2			Mux input channel 2 of TIM module 7	
	GTM_TIM4_IN3_6			Mux input channel 3 of TIM module 4	
	GTM_TIM2_IN3_6			Mux input channel 3 of TIM module 2	
	P15.12			O0	General-purpose output
	GTM_TOUT244			O1	GTM muxed output
	—			O2	Reserved
	QSPI5_SLSO1			O3	Master slave select output
	MSC3_SON			O4	Data output - inverted part of the differential signal
	—			O5	Reserved
	—			O6	Reserved
	—			O7	Reserved

表 2-9 端口 P15 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A23	P15.13	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM7_IN3_3			Mux input channel 3 of TIM module 7
	GTM_TIM4_IN4_6			Mux input channel 4 of TIM module 4
	GTM_TIM2_IN4_9			Mux input channel 4 of TIM module 2
	P15.13	O0		General-purpose output
	GTM_TOUT245	O1		GTM muxed output
	—	O2		Reserved
	QSPI5_SLSO0	O3		Master slave select output
	MSC3_SOP	O4		Data output - direct part of the differential signal
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
B22	P15.14	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM7_IN4_2			Mux input channel 4 of TIM module 7
	GTM_TIM4_IN5_6			Mux input channel 5 of TIM module 4
	GTM_TIM2_IN5_12			Mux input channel 5 of TIM module 2
	QSPI5_MTSRA	O0		Slave SPI data input
	P15.14			General-purpose output
	GTM_TOUT246			GTM muxed output
	—			Reserved
	QSPI5_MTSR			Master SPI data output
	MSC3_EN0			Chip Select
	—			Reserved
	—			Reserved
—	O7	Reserved		
A22	P15.15	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM7_IN5_2			Mux input channel 5 of TIM module 7
	GTM_TIM4_IN6_6			Mux input channel 6 of TIM module 4
	GTM_TIM2_IN6_9			Mux input channel 6 of TIM module 2
	QSPI5_SCLKA	O0		Slave SPI clock inputs
	P15.15			General-purpose output
	GTM_TOUT247			GTM muxed output
	—			Reserved
	QSPI5_SCLK			Master SPI clock output
	MSC3_EN1			Chip Select
	—			Reserved
	—			Reserved
—	O7	Reserved		

表 2-10 端口 P20 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
N25	P20.0	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN6_7			<b>Mux input channel 6 of TIM module 1</b>
	GTM_TIM1_IN4_9			<b>Mux input channel 4 of TIM module 1</b>
	GTM_TIM0_IN6_7			<b>Mux input channel 6 of TIM module 0</b>
	CAN03_RXDC			<b>CAN receive input node 3</b>
	CCU_PAD_SYSCLK			<b>Sysclk input</b>
	CAN21_RXDC			<b>CAN receive input node 1</b>
	CBS_TGI0			<b>Trigger input</b>
	SCU_E_REQ6_0			<b>ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	GPT120_T6EUDA			<b>Count direction control input of core timer T6</b>
	P20.0	O0	<b>General-purpose output</b>	
	GTM_TOUT59	O1	<b>GTM muxed output</b>	
	ASCLIN3_ATX	O2	<b>Transmit output</b>	
	IOM_MON2_15		<b>Monitor input 2</b>	
	IOM_REF2_15	<b>Reference input 2</b>		
	ASCLIN3_ASCLK	O3	<b>Shift clock output</b>	
	—	O4	<b>Reserved</b>	
	HSCT0_SYSCLK_OUT	O5	<b>sys clock output</b>	
	—	O6	<b>Reserved</b>	
	—	O7	<b>Reserved</b>	
CBS_TGO0	O	<b>Trigger output</b>		
M24	P20.1	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM4_IN4_11			<b>Mux input channel 4 of TIM module 4</b>
	GTM_TIM3_IN3_5			<b>Mux input channel 3 of TIM module 3</b>
	GTM_TIM2_IN3_5			<b>Mux input channel 3 of TIM module 2</b>
	CBS_TGI1			<b>Trigger input</b>
	GTM_DTMA1_1			<b>CDTM1_DTM4</b>
	P20.1	O0	<b>General-purpose output</b>	
	GTM_TOUT60	O1	<b>GTM muxed output</b>	
	—	O2	<b>Reserved</b>	
	—	O3	<b>Reserved</b>	
	—	O4	<b>Reserved</b>	
	—	O5	<b>Reserved</b>	
	—	O6	<b>Reserved</b>	
	—	O7	<b>Reserved</b>	
	CBS_TGO1	O	<b>Trigger output</b>	

表 2-10 端口 P20 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
N24	P20.2	I	S / PU / VEXT	<b>General-purpose input</b> This pin is latched at power on reset release to enter test mode.
	TESTMODE			<b>Testmode Enable Input</b>
M25	P20.3	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM4_IN5_11			<b>Mux input channel 5 of TIM module 4</b>
	GTM_TIM3_IN4_5			<b>Mux input channel 4 of TIM module 3</b>
	GTM_TIM2_IN4_5			<b>Mux input channel 4 of TIM module 2</b>
	ASCLIN3_ARXC			<b>Receive input</b>
	GPT120_T6INA			<b>Trigger/gate input of core timer T6</b>
	P20.3	O0		<b>General-purpose output</b>
	GTM_TOUT61	O1		<b>GTM muxed output</b>
	ASCLIN3_ATX	O2		<b>Transmit output</b>
	IOM_MON2_15			<b>Monitor input 2</b>
	IOM_REF2_15			<b>Reference input 2</b>
	QSPI0_SLSO9	O3		<b>Master slave select output</b>
	QSPI2_SLSO9	O4		<b>Master slave select output</b>
	CAN03_TXD	O5		<b>CAN transmit output node 3</b>
	IOM_MON2_8			<b>Monitor input 2</b>
	IOM_REF2_8			<b>Reference input 2</b>
	CAN21_TXD	O6		<b>CAN transmit output node 1</b>
	—	O7		<b>Reserved</b>
	L22	P20.6	I	SLOW / PU1 / VEXT / ES
GTM_TIM6_IN0_1			<b>Mux input channel 0 of TIM module 6</b>	
GTM_TIM3_IN6_5			<b>Mux input channel 6 of TIM module 3</b>	
GTM_TIM2_IN6_5			<b>Mux input channel 6 of TIM module 2</b>	
CAN12_RXDA			<b>CAN receive input node 2</b>	
ASCLIN9_ARXE			<b>Receive input</b>	
P20.6		O0		<b>General-purpose output</b>
GTM_TOUT62		O1		<b>GTM muxed output</b>
ASCLIN1_ARTS		O2		<b>Ready to send output</b>
QSPI0_SLSO8		O3		<b>Master slave select output</b>
QSPI2_SLSO8		O4		<b>Master slave select output</b>
—		O5		<b>Reserved</b>
—		O6		<b>Reserved</b>
—		O7		<b>Reserved</b>

表 2-10 端口 P20 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
L24	P20.7	I	FAST / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM3_IN7_5			Mux input channel 7 of TIM module 3	
	GTM_TIM2_IN7_5			Mux input channel 7 of TIM module 2	
	GTM_TIM1_IN5_8			Mux input channel 5 of TIM module 1	
	GTM_TIM6_IN1_1			Mux input channel 1 of TIM module 6	
	CAN00_RXDB			CAN receive input node 0	
	ASCLIN1_ACTSA			Clear to send input	
	ASCLIN9_ARXF			Receive input	
	SDMMC0_DAT0_IN			read data in	
	P20.7			O0	General-purpose output
	GTM_TOUT63	O1	GTM muxed output		
	ASCLIN9_ATX	O2	Transmit output		
	—	O3	Reserved		
	—	O4	Reserved		
	CAN12_TXD	O5	CAN transmit output node 2		
	—	O6	Reserved		
	CCU61_COUT63	O7	T13 PWM channel 63		
	IOM_MON1_7		Monitor input 1		
	IOM_REF1_7		Reference input 1		
	SDMMC0_DAT0	O	write data out		
L25	P20.8	I	FAST / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM6_IN2_1			Mux input channel 2 of TIM module 6	
	GTM_TIM1_IN7_3			Mux input channel 7 of TIM module 1	
	GTM_TIM0_IN7_3			Mux input channel 7 of TIM module 0	
	SDMMC0_DAT1_IN			read data in	
	P20.8			O0	General-purpose output
	GTM_TOUT64			O1	GTM muxed output
	ASCLIN1_ASLSO			O2	Slave select signal output
	QSPI0_SLSO0			O3	Master slave select output
	QSPI1_SLSO0			O4	Master slave select output
	CAN00_TXD	O5	CAN transmit output node 0		
	IOM_MON2_5		Monitor input 2		
	IOM_REF2_5		Reference input 2		
	—	O6	Reserved		
	CCU61_CC60	O7	T12 PWM channel 60		
	IOM_MON1_8		Monitor input 1		
	IOM_REF1_13		Reference input 1		
	SDMMC0_DAT1	O	write data out		

表 2-10 端口 P20 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
K22	P20.9	I	FAST / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM6_IN3_1			Mux input channel 3 of TIM module 6	
	GTM_TIM3_IN5_5			Mux input channel 5 of TIM module 3	
	GTM_TIM2_IN5_5			Mux input channel 5 of TIM module 2	
	CAN03_RXDE			CAN receive input node 3	
	ASCLIN1_ARXC			Receive input	
	QSPI0_SLSIB			Slave select input	
	SCU_E_REQ7_0			ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)	
	P20.9			O0	General-purpose output
	GTM_TOUT65	O1	GTM muxed output		
	—	O2	Reserved		
	QSPI0_SLSO1	O3	Master slave select output		
	QSPI1_SLSO1	O4	Master slave select output		
	—	O5	Reserved		
	—	O6	Reserved		
	CCU61_CC61	O7	T12 PWM channel 61		
	IOM_MON1_9		Monitor input 1		
	IOM_REF1_12		Reference input 1		
	K24	P20.10	I	FAST / PU1 / VEXT / ES	General-purpose input
GTM_TIM3_IN6_6		Mux input channel 6 of TIM module 3			
GTM_TIM2_IN6_6		Mux input channel 6 of TIM module 2			
SDMMC0_DAT2_IN		read data in			
P20.10		O0			General-purpose output
GTM_TOUT66		O1			GTM muxed output
ASCLIN1_ATX		O2			Transmit output
IOM_MON2_13					Monitor input 2
IOM_REF2_13					Reference input 2
QSPI0_SLSO6			O3	Master slave select output	
QSPI2_SLSO7		O4	Master slave select output		
CAN03_TXD		O5	CAN transmit output node 3		
IOM_MON2_8			Monitor input 2		
IOM_REF2_8			Reference input 2		
ASCLIN1_ASCLK			O6	Shift clock output	
CCU61_CC62		O7	T12 PWM channel 62		
IOM_MON1_10			Monitor input 1		
IOM_REF1_11			Reference input 1		
SDMMC0_DAT2			O	write data out	

表 2-10 端口 P20 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
K25	P20.11	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN7_6			Mux input channel 7 of TIM module 3
	GTM_TIM2_IN7_6			Mux input channel 7 of TIM module 2
	QSPI0_SCLKA			Slave SPI clock inputs
	SDMMC0_DAT3_IN			read data in
	P20.11	00		General-purpose output
	GTM_TOUT67	01		GTM muxed output
	—	02		Reserved
	QSPI0_SCLK	03		Master SPI clock output
	—	04		Reserved
	—	05		Reserved
	—	06		Reserved
	CCU61_COUT60	07		T12 PWM channel 60
	IOM_MON1_11			Monitor input 1
	IOM_REF1_10			Reference input 1
SDMMC0_DAT3	0	write data out		
J24	P20.12	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN0_5			Mux input channel 0 of TIM module 3
	GTM_TIM2_IN0_5			Mux input channel 0 of TIM module 2
	QSPI0_MRSTA			Master SPI data input
	SDMMC0_DAT4_IN			read data in
	IOM_PIN_13	GPIO pad input to FPC		
	P20.12	00		General-purpose output
	GTM_TOUT68	01		GTM muxed output
	IOM_MON0_13	02		Monitor input 0
	—			Reserved
	QSPI0_MRST			Slave SPI data output
	IOM_MON2_0	03		Monitor input 2
	IOM_REF2_0			Reference input 2
	QSPI0_MTSR			Master SPI data output
	—	05		Reserved
	—	06		Reserved
	CCU61_COUT61	07		T12 PWM channel 61
	IOM_MON1_12			Monitor input 1
IOM_REF1_9	Reference input 1			
SDMMC0_DAT4	0	write data out		

表 2-10 端口 P20 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
J25	P20.13	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM3_IN1_4			<b>Mux input channel 1 of TIM module 3</b>
	GTM_TIM2_IN1_4			<b>Mux input channel 1 of TIM module 2</b>
	QSPI0_SLSIA			<b>Slave select input</b>
	SDMMC0_DAT5_IN			<b>read data in</b>
	IOM_PIN_14			<b>GPIO pad input to FPC</b>
	P20.13			O0
	GTM_TOUT69	O1		<b>GTM muxed output</b>
	IOM_MON0_14			<b>Monitor input 0</b>
	—	O2		<b>Reserved</b>
	QSPI0_SLSO2	O3		<b>Master slave select output</b>
	QSPI1_SLSO2	O4		<b>Master slave select output</b>
	QSPI0_SCLK	O5		<b>Master SPI clock output</b>
	—	O6		<b>Reserved</b>
	CCU61_COUT62	O7		<b>T12 PWM channel 62</b>
	IOM_MON1_13			<b>Monitor input 1</b>
	IOM_REF1_8			<b>Reference input 1</b>
SDMMC0_DAT5	O	<b>write data out</b>		
H25	P20.14	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM3_IN2_4			<b>Mux input channel 2 of TIM module 3</b>
	GTM_TIM2_IN2_4			<b>Mux input channel 2 of TIM module 2</b>
	QSPI0_MTSRA			<b>Slave SPI data input</b>
	SDMMC0_DAT6_IN			<b>read data in</b>
	IOM_PIN_15			<b>GPIO pad input to FPC</b>
	P20.14			O0
	GTM_TOUT70	O1		<b>GTM muxed output</b>
	IOM_MON0_15			<b>Monitor input 0</b>
	—	O2		<b>Reserved</b>
	QSPI0_MTSR	O3		<b>Master SPI data output</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	SDMMC0_DAT6	O		<b>write data out</b>

表 2-11 端口 P21 的功能

Ball	Symbol	Ctrl.	Buffer Type	Function
R22	P21.0	I	LVDS_RX / FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM4_IN0_11			<b>Mux input channel 0 of TIM module 4</b>
	GTM_TIM3_IN4_6			<b>Mux input channel 4 of TIM module 3</b>
	GTM_TIM2_IN4_6			<b>Mux input channel 4 of TIM module 2</b>
	QSPI4_MRSTDN			<b>Master SPI data input (LVDS N line)</b>
	DMU_FDEST			<b>Enter destructive debug mode</b>
	ASCLIN11_ARXC			<b>Receive input</b>
	HSCT1_RXDN			<b>Rx data</b>
	P21.0	O0	<b>General-purpose output</b>	
	GTM_TOUT51	O1	<b>GTM muxed output</b>	
	ASCLIN11_ATX	O2	<b>Transmit output</b>	
	—	O3	<b>Reserved</b>	
	—	O4	<b>Reserved</b>	
	—	O5	<b>Reserved</b>	
	—	O6	<b>Reserved</b>	
	—	O7	<b>Reserved</b>	
HSM_HSM1	O	<b>Pin Output Value</b>		
P22	P21.1	I	LVDS_RX / FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM4_IN1_13			<b>Mux input channel 1 of TIM module 4</b>
	GTM_TIM3_IN5_6			<b>Mux input channel 5 of TIM module 3</b>
	GTM_TIM2_IN5_6			<b>Mux input channel 5 of TIM module 2</b>
	QSPI4_MRSTDP			<b>Master SPI data input (LVDS P line)</b>
	ASCLIN11_ARXD			<b>Receive input</b>
	HSCT1_RXDP			<b>Rx data</b>
	GTM_DTMA4_1			<b>CDTM4_DTM4</b>
	P21.1	O0	<b>General-purpose output</b>	
	GTM_TOUT52	O1	<b>GTM muxed output</b>	
	—	O2	<b>Reserved</b>	
	—	O3	<b>Reserved</b>	
	—	O4	<b>Reserved</b>	
	—	O5	<b>Reserved</b>	
	—	O6	<b>Reserved</b>	
	—	O7	<b>Reserved</b>	
HSM_HSM2	O	<b>Pin Output Value</b>		

表 2-11 端口 P21 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
R24	P21.2	I	LVDS_RX / FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM5_IN4_11			<b>Mux input channel 4 of TIM module 5</b>
	GTM_TIM1_IN0_7			<b>Mux input channel 0 of TIM module 1</b>
	GTM_TIM0_IN0_7			<b>Mux input channel 0 of TIM module 0</b>
	QSPI2_MRSTCN			<b>Master SPI data input (LVDS N line)</b>
	SCU_EMGSTOP_POR T_B			<b>Emergency stop Port Pin B input request</b>
	ASCLIN3_ARXGN			<b>Differential Receive input (low active)</b>
	HSCT0_RXDN			<b>Rx data</b>
	QSPI4_MRSTCN			<b>Master SPI data input (LVDS N line)</b>
	ASCLIN11_ARXE			<b>Receive input</b>
	GTM_DTMA1_0			<b>CDTM1_DTM4</b>
	P21.2	O0		<b>General-purpose output</b>
	GTM_TOUT53	O1		<b>GTM muxed output</b>
	ASCLIN3_ASLSO	O2		<b>Slave select signal output</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	GETH_MDC	O5		<b>MDIO clock</b>
—	O6	<b>Reserved</b>		
—	O7	<b>Reserved</b>		
P24	P21.3	I	LVDS_RX / FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM5_IN5_12			<b>Mux input channel 5 of TIM module 5</b>
	GTM_TIM1_IN1_6			<b>Mux input channel 1 of TIM module 1</b>
	GTM_TIM0_IN1_6			<b>Mux input channel 1 of TIM module 0</b>
	QSPI2_MRSTCP			<b>Master SPI data input (LVDS P line)</b>
	ASCLIN3_ARXGP			<b>Differential Receive input (high active)</b>
	GETH_MDIOD			<b>MDIO Input</b>
	HSCT0_RXDP			<b>Rx data</b>
	QSPI4_MRSTCP			<b>Master SPI data input (LVDS P line)</b>
	P21.3	O0		<b>General-purpose output</b>
	GTM_TOUT54	O1		<b>GTM muxed output</b>
	ASCLIN11_ASCLK	O2		<b>Shift clock output</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
GETH_MDIO	O	<b>MDIO Output</b>		

表 2-11 端口 P21 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
R25	P21.4	I	LVDS_TX / FAST / PU1 / VEXT / ES6	<b>General-purpose input</b>
	GTM_TIM5_IN6_12			<b>Mux input channel 6 of TIM module 5</b>
	GTM_TIM1_IN2_6			<b>Mux input channel 2 of TIM module 1</b>
	GTM_TIM0_IN2_6			<b>Mux input channel 2 of TIM module 0</b>
	P21.4	O0		<b>General-purpose output</b>
	GTM_TOUT55	O1		<b>GTM muxed output</b>
	ASCLIN11_ASLSO	O2		<b>Slave select signal output</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	HSCT0_TXDN	O		<b>Tx data</b>
P25	P21.5	I	LVDS_TX / FAST / PU1 / VEXT / ES6	<b>General-purpose input</b>
	GTM_TIM5_IN7_11			<b>Mux input channel 7 of TIM module 5</b>
	GTM_TIM1_IN3_6			<b>Mux input channel 3 of TIM module 1</b>
	GTM_TIM0_IN3_6			<b>Mux input channel 3 of TIM module 0</b>
	ASCLIN11_ARXF			<b>Receive input</b>
	P21.5	O0		<b>General-purpose output</b>
	GTM_TOUT56	O1		<b>GTM muxed output</b>
	ASCLIN3_ASCLK	O2		<b>Shift clock output</b>
	ASCLIN11_ATX	O3		<b>Transmit output</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
HSCT0_TXDP	O	<b>Tx data</b>		

表 2-11 端口 P21 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
N22	P21.6/TDI	I	FAST / PD / PU2 / VEXT / ES3	<b>General-purpose input</b> PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ.
	GTM_TIM4_IN2_12			<b>Mux input channel 2 of TIM module 4</b>
	GTM_TIM1_IN4_8			<b>Mux input channel 4 of TIM module 1</b>
	GTM_TIM0_IN4_8			<b>Mux input channel 4 of TIM module 0</b>
	GPT120_T5EUDA			<b>Count direction control input of timer T5</b>
	ASCLIN3_ARXF			<b>Receive input</b>
	CBS_TGI2			<b>Trigger input</b>
	TDI			<b>JTAG Module Data Input</b>
	P21.6	O0	<b>General-purpose output</b>	
	GTM_TOUT57	O1	<b>GTM muxed output</b>	
	ASCLIN3_ASLSO	O2	<b>Slave select signal output</b>	
	—	O3	<b>Reserved</b>	
	—	O4	<b>Reserved</b>	
	—	O5	<b>Reserved</b>	
	—	O6	<b>Reserved</b>	
	GPT120_T3OUT	O7	<b>External output for overflow/underflow detection of core timer T3</b>	
	CBS_TGO2	O	<b>Trigger output</b>	
	DAP3	I/O	<b>DAP: DAP3 Data I/O</b>	
	DAPE1	I/O	<b>DAPE: DAPE1 Data I/O</b>	

表 2-11 端口 P21 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
N21	P21.7/TDO	I	FAST / PU2 / VEXT / ES4	<b>General-purpose input</b>
	GTM_TIM4_IN3_12			<b>Mux input channel 3 of TIM module 4</b>
	GTM_TIM1_IN5_7			<b>Mux input channel 5 of TIM module 1</b>
	GTM_TIM0_IN5_7			<b>Mux input channel 5 of TIM module 0</b>
	GPT120_T5INA			<b>Trigger/gate input of timer T5</b>
	CBS_TGI3			<b>Trigger input</b>
	GETH_RXERB			<b>Receive Error MII</b>
	P21.7	O0		<b>General-purpose output</b>
	GTM_TOUT58	O1		<b>GTM muxed output</b>
	ASCLIN3_ATX	O2		<b>Transmit output</b>
	IOM_MON2_15			<b>Monitor input 2</b>
	IOM_REF2_15			<b>Reference input 2</b>
	ASCLIN3_ASCLK	O3		<b>Shift clock output</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	GPT120_T6OUT	O7		<b>External output for overflow/underflow detection of core timer T6</b>
	CBS_TGO3	O		<b>Trigger output</b>
	DAP2	I/O		<b>DAP: DAP2 Data I/O</b>
	DAPE2	I/O		<b>DAPE: DAPE2 Data I/O</b>
TDO	O	<b>JTAG Module Data Output</b>		

表 2-12 端口 P22 的功能

Ball	Symbol	Ctrl.	Buffer Type	Function	
W25	P22.0	I	LVDS_TX / FAST / PU1 / VEXT / ES6	<b>General-purpose input</b>	
	GTM_TIM7_IN3_1			<b>Mux input channel 3 of TIM module 7</b>	
	GTM_TIM1_IN1_7			<b>Mux input channel 1 of TIM module 1</b>	
	GTM_TIM0_IN1_7			<b>Mux input channel 1 of TIM module 0</b>	
	QSPI4_MTSRB			<b>Slave SPI data input</b>	
	ASCLIN6_ARXE			<b>Receive input</b>	
	P22.0			O0	<b>General-purpose output</b>
	GTM_TOUT47			O1	<b>GTM muxed output</b>
	ASCLIN3_ATXN			O2	<b>Differential Transmit output (low active)</b>
	QSPI4_MTSR			O3	<b>Master SPI data output</b>
	QSPI4_SCLKN			O4	<b>Master SPI clock output (LVDS N line)</b>
	MSC1_FCLN			O5	<b>Shift-clock inverted part of the differential signal</b>
	—	O6	<b>Reserved</b>		
ASCLIN6_ATX	O7	<b>Transmit output</b>			
W24	P22.1	I	LVDS_TX / FAST / PU1 / VEXT / ES6	<b>General-purpose input</b>	
	GTM_TIM7_IN2_1			<b>Mux input channel 2 of TIM module 7</b>	
	GTM_TIM1_IN0_8			<b>Mux input channel 0 of TIM module 1</b>	
	GTM_TIM0_IN0_8			<b>Mux input channel 0 of TIM module 0</b>	
	QSPI4_MRSTB			<b>Master SPI data input</b>	
	ASCLIN7_ARXE			<b>Receive input</b>	
	P22.1			O0	<b>General-purpose output</b>
	GTM_TOUT48			O1	<b>GTM muxed output</b>
	ASCLIN3_ATXP			O2	<b>Differential Transmit output (high active)</b>
	QSPI4_MRST			O3	<b>Slave SPI data output</b>
	IOM_MON2_4				<b>Monitor input 2</b>
	IOM_REF2_4				<b>Reference input 2</b>
	QSPI4_SCLKP	O4	<b>Master SPI clock output (LVDS P line)</b>		
MSC1_FCLP	O5	<b>Shift-clock direct part of the differential signal</b>			
—	O6	<b>Reserved</b>			
ASCLIN7_ATX	O7	<b>Transmit output</b>			

表 2-12 端口 P22 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y25	P22.2	I	LVDS_TX / FAST / PU1 / VEXT / ES6	<b>General-purpose input</b>
	GTM_TIM7_IN1_1			<b>Mux input channel 1 of TIM module 7</b>
	GTM_TIM1_IN3_7			<b>Mux input channel 3 of TIM module 1</b>
	GTM_TIM0_IN3_7			<b>Mux input channel 3 of TIM module 0</b>
	QSPI4_SLSIB			<b>Slave select input</b>
	P22.2	O0		<b>General-purpose output</b>
	GTM_TOUT49	O1		<b>GTM muxed output</b>
	ASCLIN5_ATX	O2		<b>Transmit output</b>
	QSPI4_SLSO3	O3		<b>Master slave select output</b>
	QSPI4_MTSRN	O4		<b>Master SPI data output (LVDS N line)</b>
	MSC1_SON	O5		<b>Data output - inverted part of the differential signal</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	HSCT1_TXDN	O		<b>Tx data</b>
Y24	P22.3	I	LVDS_TX / FAST / PU1 / VEXT / ES6	<b>General-purpose input</b>
	GTM_TIM7_IN0_1			<b>Mux input channel 0 of TIM module 7</b>
	GTM_TIM1_IN4_4			<b>Mux input channel 4 of TIM module 1</b>
	GTM_TIM0_IN4_4			<b>Mux input channel 4 of TIM module 0</b>
	QSPI4_SCLKB			<b>Slave SPI clock inputs</b>
	ASCLIN5_ARXC			<b>Receive input</b>
	P22.3	O0		<b>General-purpose output</b>
	GTM_TOUT50	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	QSPI4_SCLK	O3		<b>Master SPI clock output</b>
	QSPI4_MTSRP	O4		<b>Master SPI data output (LVDS P line)</b>
	MSC1_SOP	O5		<b>Data output - direct part of the differential signal</b>
	—	O6		<b>Reserved</b>
	HSPDM_MUTE	O7		<b>Mute output from the micro controller which could be used to control an external Transmitter</b>
HSCT1_TXDP	O		<b>Tx data</b>	

表 2-12 端口 P22 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
W21	P22.4	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM3_IN0_8			<b>Mux input channel 0 of TIM module 3</b>
	ASCLIN7_ARXF			<b>Receive input</b>
	GTM_DTMA3_0			<b>CDTM3_DTM4</b>
	P22.4	O0		<b>General-purpose output</b>
	GTM_TOUT130	O1		<b>GTM muxed output</b>
	ASCLIN4_ASLSO	O2		<b>Slave select signal output</b>
	—	O3		<b>Reserved</b>
	QSPI0_SLSO12	O4		<b>Master slave select output</b>
	—	O5		<b>Reserved</b>
	CAN13_TXD	O6		<b>CAN transmit output node 3</b>
	HSPDM_BS0_OUT	O7		<b>Bit stream 0 output to the pad</b>
W22	P22.5	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM3_IN1_7			<b>Mux input channel 1 of TIM module 3</b>
	QSPI0_MTSRC			<b>Slave SPI data input</b>
	CAN13_RXDC			<b>CAN receive input node 3</b>
	P22.5	O0		<b>General-purpose output</b>
	GTM_TOUT131	O1		<b>GTM muxed output</b>
	ASCLIN4_ATX	O2		<b>Transmit output</b>
	—	O3		<b>Reserved</b>
	QSPI0_MTSR	O4		<b>Master SPI data output</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	HSPDM_BS1_OUT	O7		<b>Bit stream 1 output to the pad</b>

表 2-12 端口 P22 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
V21	P22.6	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN2_6			Mux input channel 2 of TIM module 3
	GTM_TIM2_IN6_14			Mux input channel 6 of TIM module 2
	QSPI0_MRSTC			Master SPI data input
	ASCLIN4_ARXC			Receive input
	P22.6	O0		General-purpose output
	GTM_TOUT132	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	QSPI0_MRST	O4		Slave SPI data output
	IOM_MON2_0			Monitor input 2
	IOM_REF2_0			Reference input 2
	CAN21_TXD	O5		CAN transmit output node 1
	—	O6		Reserved
—	O7	Reserved		
V22	P22.7	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN3_7			Mux input channel 3 of TIM module 3
	QSPI0_SCLKC			Slave SPI clock inputs
	CAN21_RXDF			CAN receive input node 1
	P22.7	O0		General-purpose output
	GTM_TOUT133	O1		GTM muxed output
	ASCLIN4_ASCLK	O2		Shift clock output
	—	O3		Reserved
	QSPI0_SCLK	O4		Master SPI clock output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-12 端口 P22 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
U21	P22.8	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN0_4			Mux input channel 0 of TIM module 5
	GTM_TIM3_IN4_7			Mux input channel 4 of TIM module 3
	QSPI0_SCLKB			Slave SPI clock inputs
	P22.8	O0		General-purpose output
	GTM_TOUT134	O1		GTM muxed output
	ASCLIN5_ASCLK	O2		Shift clock output
	—	O3		Reserved
	QSPI0_SCLK	O4		Master SPI clock output
	CAN22_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	—	O7		Reserved
U22	P22.9	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN1_10			Mux input channel 1 of TIM module 5
	GTM_TIM3_IN5_7			Mux input channel 5 of TIM module 3
	QSPI0_MRSTB			Master SPI data input
	ASCLIN4_ARXD			Receive input
	CAN22_RXDE			CAN receive input node 2
	GTM_DTMA3_1			CDTM3_DTM4
	P22.9	O0		General-purpose output
	GTM_TOUT135	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	QSPI0_MRST	O4		Slave SPI data output
	IOM_MON2_0			Monitor input 2
	IOM_REF2_0			Reference input 2
	—	O5		Reserved
	—	O6		Reserved
—	O7	Reserved		

表 2-12 端口 P22 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
T21	P22.10	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN2_8			Mux input channel 2 of TIM module 5
	GTM_TIM3_IN6_7			Mux input channel 6 of TIM module 3
	QSPI0_MTSRB			Slave SPI data input
	P22.10	O0		General-purpose output
	GTM_TOUT136	O1		GTM muxed output
	ASCLIN4_ATX	O2		Transmit output
	—	O3		Reserved
	QSPI0_MTSR	O4		Master SPI data output
	CAN23_TXD	O5		CAN transmit output node 3
	—	O6		Reserved
	—	O7		Reserved
T22	P22.11	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN3_10			Mux input channel 3 of TIM module 5
	GTM_TIM3_IN7_7			Mux input channel 7 of TIM module 3
	CAN23_RXDE			CAN receive input node 3
	P22.11	O0		General-purpose output
	GTM_TOUT137	O1		GTM muxed output
	ASCLIN4_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	QSPI0_SLSO10	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-13 端口 P23 的功能

Ball	Symbol	Ctrl.	Buffer Type	Function
AC25	P23.0	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM6_IN7_1			<b>Mux input channel 7 of TIM module 6</b>
	GTM_TIM1_IN5_4			<b>Mux input channel 5 of TIM module 1</b>
	GTM_TIM0_IN5_4			<b>Mux input channel 5 of TIM module 0</b>
	CAN10_RXDC			<b>CAN receive input node 0</b>
	P23.0	O0		<b>General-purpose output</b>
	GTM_TOUT41	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
AB24	P23.1	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM6_IN6_1			<b>Mux input channel 6 of TIM module 6</b>
	GTM_TIM1_IN6_4			<b>Mux input channel 6 of TIM module 1</b>
	GTM_TIM0_IN6_4			<b>Mux input channel 6 of TIM module 0</b>
	MSC1_SDIO			<b>Upstream asynchronous input signal</b>
	ASCLIN6_ARXF			<b>Receive input</b>
	P23.1	O0		<b>General-purpose output</b>
	GTM_TOUT42	O1		<b>GTM muxed output</b>
	ASCLIN1_ARTS	O2		<b>Ready to send output</b>
	QSPI4_SLSO6	O3		<b>Master slave select output</b>
	GTM_CLK0	O4		<b>CGM generated clock</b>
	CAN10_TXD	O5		<b>CAN transmit output node 0</b>
	CCU_EXTCLK0	O6		<b>External Clock 0</b>
	ASCLIN6_ASCLK	O7		<b>Shift clock output</b>

表 2-13 端口 P23 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AB25	P23.2	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM6_IN5_1			Mux input channel 5 of TIM module 6
	GTM_TIM1_IN6_5			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_5			Mux input channel 6 of TIM module 0
	ASCLIN7_ARXC			Receive input
	P23.2	O0		General-purpose output
	GTM_TOUT43	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	CAN23_TXD	O4		CAN transmit output node 3
	CAN12_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	—	O7		Reserved
	AA24	P23.3		I
GTM_TIM6_IN4_2		Mux input channel 4 of TIM module 6		
GTM_TIM1_IN7_4		Mux input channel 7 of TIM module 1		
GTM_TIM0_IN7_4		Mux input channel 7 of TIM module 0		
MSC1_INJ0		Injection signal from port		
ASCLIN6_ARXA		Receive input		
CAN12_RXDC		CAN receive input node 2		
CAN23_RXDB		CAN receive input node 3		
P23.3		O0	General-purpose output	
GTM_TOUT44		O1	GTM muxed output	
ASCLIN7_ATX		O2	Transmit output	
—		O3	Reserved	
—		O4	Reserved	
—		O5	Reserved	
—		O6	Reserved	
—		O7	Reserved	

表 2-13 端口 P23 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AA25	P23.4	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM6_IN3_2			Mux input channel 3 of TIM module 6
	GTM_TIM1_IN7_5			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_5			Mux input channel 7 of TIM module 0
	P23.4	O0		General-purpose output
	GTM_TOUT45	O1		GTM muxed output
	ASCLIN6_ASLSO	O2		Slave select signal output
	QSPI4_SLSO5	O3		Master slave select output
	—	O4		Reserved
	MSC1_EN0	O5		Chip Select
	—	O6		Reserved
	—	O7		Reserved
AA22	P23.5	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM6_IN2_2			Mux input channel 2 of TIM module 6
	GTM_TIM1_IN2_7			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_7			Mux input channel 2 of TIM module 0
	P23.5	O0		General-purpose output
	GTM_TOUT46	O1		GTM muxed output
	ASCLIN6_ATX	O2		Transmit output
	QSPI4_SLSO4	O3		Master slave select output
	—	O4		Reserved
	MSC1_EN1	O5		Chip Select
	CAN22_TXD	O6		CAN transmit output node 2
	—	O7		Reserved
Y22	P23.6	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM6_IN1_2			Mux input channel 1 of TIM module 6
	GTM_TIM4_IN2_7			Mux input channel 2 of TIM module 4
	GTM_TIM1_IN2_10			Mux input channel 2 of TIM module 1
	CAN22_RXDC			CAN receive input node 2
	P23.6	O0		General-purpose output
	GTM_TOUT138	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	QSPI0_SLSO11	O4		Master slave select output
	CAN11_TXD	O5		CAN transmit output node 1
	—	O6		Reserved
—	O7	Reserved		

表 2-13 端口 P23 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y21	P23.7	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM6_IN0_2			Mux input channel 0 of TIM module 6
	GTM_TIM4_IN3_7			Mux input channel 3 of TIM module 4
	GTM_TIM1_IN3_10			Mux input channel 3 of TIM module 1
	CAN11_RXDC			CAN receive input node 1
	P23.7	O0		General-purpose output
	GTM_TOUT139	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-14 端口 P24 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
U29	P24.0	I	FAST / PU1 / VEBU / ES	General-purpose input
	GTM_TIM6_IN0_6			Mux input channel 0 of TIM module 6
	GTM_TIM4_IN0_8			Mux input channel 0 of TIM module 4
	EBU_A_IN11			Address Input
	P24.0	O0		General-purpose output
	GTM_TOUT222	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	EBU_A11	O		Address Output

表 2-14 端口 P24 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
U30	P24.1	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM6_IN1_6			<b>Mux input channel 1 of TIM module 6</b>
	GTM_TIM4_IN1_8			<b>Mux input channel 1 of TIM module 4</b>
	EBU_A_IN15			<b>Address Input</b>
	P24.1	O0		<b>General-purpose output</b>
	GTM_TOUT223	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_A15	O		<b>Address Output</b>
T29	P24.2	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM6_IN2_6			<b>Mux input channel 2 of TIM module 6</b>
	GTM_TIM4_IN2_8			<b>Mux input channel 2 of TIM module 4</b>
	EBU_A_IN14			<b>Address Input</b>
	P24.2	O0		<b>General-purpose output</b>
	GTM_TOUT224	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_A14	O		<b>Address Output</b>

表 2-14 端口 P24 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
T30	P24.3	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM6_IN3_6			<b>Mux input channel 3 of TIM module 6</b>
	GTM_TIM4_IN3_8			<b>Mux input channel 3 of TIM module 4</b>
	EBU_A_IN13			<b>Address Input</b>
	P24.3	O0		<b>General-purpose output</b>
	GTM_TOUT225	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_A13	O		<b>Address Output</b>
R29	P24.4	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM6_IN4_5			<b>Mux input channel 4 of TIM module 6</b>
	GTM_TIM4_IN4_7			<b>Mux input channel 4 of TIM module 4</b>
	EBU_A_IN9			<b>Address Input</b>
	P24.4	O0		<b>General-purpose output</b>
	GTM_TOUT226	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_A9	O		<b>Address Output</b>

表 2-14 端口 P24 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
R30	P24.5	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM6_IN5_5			<b>Mux input channel 5 of TIM module 6</b>
	GTM_TIM4_IN5_7			<b>Mux input channel 5 of TIM module 4</b>
	EBU_A_IN12			<b>Address Input</b>
	P24.5	O0		<b>General-purpose output</b>
	GTM_TOUT227	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_A12	O		<b>Address Output</b>
P29	P24.6	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM6_IN6_5			<b>Mux input channel 6 of TIM module 6</b>
	GTM_TIM4_IN6_7			<b>Mux input channel 6 of TIM module 4</b>
	EBU_A_IN5			<b>Address Input</b>
	P24.6	O0		<b>General-purpose output</b>
	GTM_TOUT228	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_A5	O		<b>Address Output</b>

表 2-14 端口 P24 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
P30	P24.7	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM6_IN7_5			<b>Mux input channel 7 of TIM module 6</b>
	GTM_TIM4_IN7_7			<b>Mux input channel 7 of TIM module 4</b>
	EBU_A_IN8			<b>Address Input</b>
	P24.7	O0		<b>General-purpose output</b>
	GTM_TOUT229	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_A8	O		<b>Address Output</b>
N29	P24.8	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM7_IN0_5			<b>Mux input channel 0 of TIM module 7</b>
	GTM_TIM5_IN0_5			<b>Mux input channel 0 of TIM module 5</b>
	EBU_A_IN10			<b>Address Input</b>
	P24.8	O0		<b>General-purpose output</b>
	GTM_TOUT230	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_A10	O		<b>Address Output</b>

表 2-14 端口 P24 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
N30	P24.9	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM7_IN1_5			<b>Mux input channel 1 of TIM module 7</b>
	GTM_TIM5_IN1_6			<b>Mux input channel 1 of TIM module 5</b>
	EBU_A_IN6			<b>Address Input</b>
	P24.9	O0		<b>General-purpose output</b>
	GTM_TOUT231	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_A6	O		<b>Address Output</b>
M29	P24.10	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM7_IN2_4			<b>Mux input channel 2 of TIM module 7</b>
	GTM_TIM5_IN2_5			<b>Mux input channel 2 of TIM module 5</b>
	EBU_A_IN4			<b>Address Input</b>
	P24.10	O0		<b>General-purpose output</b>
	GTM_TOUT232	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_A4	O		<b>Address Output</b>

表 2-14 端口 P24 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
M30	P24.11	I	FAST / PU1 / VEBU / ES	General-purpose input
	GTM_TIM7_IN3_4			Mux input channel 3 of TIM module 7
	GTM_TIM5_IN3_6			Mux input channel 3 of TIM module 5
	EBU_A_IN3			Address Input
	P24.11	O0		General-purpose output
	GTM_TOUT233	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	EBU_A3	O		Address Output
L29	P24.12	I	FAST / PU1 / VEBU / ES	General-purpose input
	GTM_TIM7_IN4_3			Mux input channel 4 of TIM module 7
	GTM_TIM5_IN4_6			Mux input channel 4 of TIM module 5
	EBU_A_IN1			Address Input
	P24.12	O0		General-purpose output
	GTM_TOUT234	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	EBU_A1	O		Address Output

表 2-14 端口 P24 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
L30	P24.13	I	FAST / PU1 / VEBU / ES	General-purpose input
	GTM_TIM7_IN5_3			Mux input channel 5 of TIM module 7
	GTM_TIM5_IN5_6			Mux input channel 5 of TIM module 5
	EBU_A_IN2			Address Input
	P24.13	O0		General-purpose output
	GTM_TOUT235	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	EBU_A2	O		Address Output
K29	P24.14	I	FAST / PU1 / VEBU / ES	General-purpose input
	GTM_TIM7_IN7_3			Mux input channel 7 of TIM module 7
	GTM_TIM7_IN6_3			Mux input channel 6 of TIM module 7
	GTM_TIM5_IN6_6			Mux input channel 6 of TIM module 5
	EBU_A_IN0			Address Input
	P24.14	O0		General-purpose output
	GTM_TOUT236	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
EBU_A0	O	Address Output		

表 2-14 端口 P24 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
K30	P24.15	I	FAST / PU1 / VEBU / ES	General-purpose input
	GTM_TIM7_IN7_2			Mux input channel 7 of TIM module 7
	GTM_TIM5_IN7_5			Mux input channel 7 of TIM module 5
	EBU_A_IN7			Address Input
	P24.15	O0		General-purpose output
	GTM_TOUT237	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	EBU_A7	O		Address Output

表 2-15 端口 P25 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
AG30	P25.0	I	FAST / PU1 / VEBU / ES	General-purpose input
	GTM_TIM6_IN0_7			Mux input channel 0 of TIM module 6
	GTM_TIM3_IN0_12			Mux input channel 0 of TIM module 3
	P25.0	O0		General-purpose output
	GTM_TOUT206	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	EBU_BFCLKO	O		Burst Flash Clock Output

表 2-15 端口 P25 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AF30	P25.1	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM6_IN1_7			<b>Mux input channel 1 of TIM module 6</b>
	GTM_TIM3_IN1_11			<b>Mux input channel 1 of TIM module 3</b>
	EBU_RD_FDBK			<b>Read Feedback</b>
	P25.1	O0		<b>General-purpose output</b>
	GTM_TOUT207	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_RD	O		<b>Read Control</b>
AF29	P25.2	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM6_IN2_7			<b>Mux input channel 2 of TIM module 6</b>
	GTM_TIM3_IN2_9			<b>Mux input channel 2 of TIM module 3</b>
	EBU_WR_FDBK			<b>Write Feedback</b>
	P25.2	O0		<b>General-purpose output</b>
	GTM_TOUT208	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_WR	O		<b>Write Control</b>

表 2-15 端口 P25 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AE30	P25.3	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM6_IN3_7			<b>Mux input channel 3 of TIM module 6</b>
	GTM_TIM3_IN3_9			<b>Mux input channel 3 of TIM module 3</b>
	EBU_CS_FDBK2			<b>Chip Select Feedback</b>
	P25.3	O0		<b>General-purpose output</b>
	GTM_TOUT209	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	EBU_BAA	O7		<b>Burst Address Advance</b>
	EBU_CS2	O		<b>Chip Select</b>
	AE29	P25.4		I
GTM_TIM6_IN4_6		<b>Mux input channel 4 of TIM module 6</b>		
GTM_TIM3_IN4_10		<b>Mux input channel 4 of TIM module 3</b>		
EBU_CS_FDBK1		<b>Chip Select Feedback</b>		
P25.4		O0	<b>General-purpose output</b>	
GTM_TOUT210		O1	<b>GTM muxed output</b>	
—		O2	<b>Reserved</b>	
—		O3	<b>Reserved</b>	
—		O4	<b>Reserved</b>	
—		O5	<b>Reserved</b>	
—		O6	<b>Reserved</b>	
—		O7	<b>Reserved</b>	
EBU_CS1		O	<b>Chip Select</b>	

表 2-15 端口 P25 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AD30	P25.5	I	FAST / PU1 / VEBU / ES	General-purpose input
	GTM_TIM6_IN5_6			Mux input channel 5 of TIM module 6
	GTM_TIM3_IN5_11			Mux input channel 5 of TIM module 3
	EBU_CS_FDBK0			Chip Select Feedback
	P25.5	O0		General-purpose output
	GTM_TOUT211	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	EBU_CS0	O		Chip Select
W29	P25.6	I	FAST / PU1 / VEBU / ES	General-purpose input
	GTM_TIM6_IN6_6			Mux input channel 6 of TIM module 6
	GTM_TIM3_IN6_14			Mux input channel 6 of TIM module 3
	EBU_WAIT			Wait Input
	P25.6	O0		General-purpose output
	GTM_TOUT212	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	AD29	P25.7		I
GTM_TIM6_IN7_6		Mux input channel 7 of TIM module 6		
GTM_TIM3_IN7_10		Mux input channel 7 of TIM module 3		
EBU_ADV_FDBK		ADV Control Signal Feedback		
P25.7		O0	General-purpose output	
GTM_TOUT213		O1	GTM muxed output	
—		O2	Reserved	
—		O3	Reserved	
—		O4	Reserved	
—		O5	Reserved	
—		O6	Reserved	
—		O7	Reserved	
EBU_ADV		O	Address Valid Control Signal	

表 2-15 端口 P25 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AC29	P25.8	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM7_IN0_6			<b>Mux input channel 0 of TIM module 7</b>
	GTM_TIM4_IN0_9			<b>Mux input channel 0 of TIM module 4</b>
	P25.8	O0		<b>General-purpose output</b>
	GTM_TOUT214	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	EBU_A23	O5		<b>Address Output</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_BC0	0		<b>Byte Control</b>
AC30	P25.9	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM7_IN1_6			<b>Mux input channel 1 of TIM module 7</b>
	GTM_TIM4_IN1_9			<b>Mux input channel 1 of TIM module 4</b>
	P25.9	O0		<b>General-purpose output</b>
	GTM_TOUT215	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	EBU_A22	O5		<b>Address Output</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_BC1	0		<b>Byte Control</b>
AB29	P25.10	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM7_IN2_5			<b>Mux input channel 2 of TIM module 7</b>
	GTM_TIM4_IN2_9			<b>Mux input channel 2 of TIM module 4</b>
	P25.10	O0		<b>General-purpose output</b>
	GTM_TOUT216	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	EBU_A21	O5		<b>Address Output</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_BC2	0		<b>Byte Control</b>

表 2-15 端口 P25 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AB30	P25.11	I	FAST / PU1 / VEBU / ES	General-purpose input
	GTM_TIM7_IN3_5			Mux input channel 3 of TIM module 7
	GTM_TIM4_IN3_9			Mux input channel 3 of TIM module 4
	P25.11	O0		General-purpose output
	GTM_TOUT217	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	EBU_A20	O5		Address Output
	—	O6		Reserved
	—	O7		Reserved
	EBU_BC3	O		Byte Control
AA29	P25.12	I	FAST / PU1 / VEBU / ES	General-purpose input
	GTM_TIM7_IN4_4			Mux input channel 4 of TIM module 7
	GTM_TIM4_IN4_8			Mux input channel 4 of TIM module 4
	P25.12	O0		General-purpose output
	GTM_TOUT218	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	EBU_A19	O		Address Output
AA30	P25.13	I	FAST / PU1 / VEBU / ES	General-purpose input
	GTM_TIM7_IN5_4			Mux input channel 5 of TIM module 7
	GTM_TIM4_IN5_8			Mux input channel 5 of TIM module 4
	P25.13	O0		General-purpose output
	GTM_TOUT219	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	EBU_A17	O		Address Output

表 2-15 端口 P25 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y29	P25.14	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM7_IN6_4			<b>Mux input channel 6 of TIM module 7</b>
	GTM_TIM4_IN6_8			<b>Mux input channel 6 of TIM module 4</b>
	P25.14	O0		<b>General-purpose output</b>
	GTM_TOUT220	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_A18	O		<b>Address Output</b>
Y30	P25.15	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM4_IN7_8			<b>Mux input channel 7 of TIM module 4</b>
	P25.15			O0
	GTM_TOUT221	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_A16	O		<b>Address Output</b>

表 2-16 端口 P26 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
AG29	P26.0	I	SLOW / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM6_IN6_9			<b>Mux input channel 6 of TIM module 6</b>
	GTM_TIM3_IN6_11			<b>Mux input channel 6 of TIM module 3</b>
	EBU_BFCLKI			<b>Burst Flash Clock Feedback</b>
	P26.0	O0		<b>General-purpose output</b>
	GTM_TOUT212	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>

表 2-17 端口 P30 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
AJ21	P30.0	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM7_IN0_7			<b>Mux input channel 0 of TIM module 7</b>
	GTM_TIM4_IN0_10			<b>Mux input channel 0 of TIM module 4</b>
	EBU_AD_IN14			<b>Data Bus Input</b>
	P30.0	O0		<b>General-purpose output</b>
	GTM_TOUT190	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_AD14	O		<b>Data Bus Output</b>

表 2-17 端口 P30 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AK21	P30.1	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM7_IN1_7			<b>Mux input channel 1 of TIM module 7</b>
	GTM_TIM4_IN1_10			<b>Mux input channel 1 of TIM module 4</b>
	EBU_AD_IN11			<b>Data Bus Input</b>
	P30.1	O0		<b>General-purpose output</b>
	GTM_TOUT191	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_AD11	O		<b>Data Bus Output</b>
AJ22	P30.2	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM7_IN2_6			<b>Mux input channel 2 of TIM module 7</b>
	GTM_TIM4_IN2_10			<b>Mux input channel 2 of TIM module 4</b>
	EBU_AD_IN12			<b>Data Bus Input</b>
	P30.2	O0		<b>General-purpose output</b>
	GTM_TOUT192	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_AD12	O		<b>Data Bus Output</b>

表 2-17 端口 P30 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AK22	P30.3	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM7_IN3_6			<b>Mux input channel 3 of TIM module 7</b>
	GTM_TIM4_IN3_10			<b>Mux input channel 3 of TIM module 4</b>
	EBU_AD_IN15			<b>Data Bus Input</b>
	P30.3	O0		<b>General-purpose output</b>
	GTM_TOUT193	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_AD15	O		<b>Data Bus Output</b>
AJ23	P30.4	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM7_IN4_5			<b>Mux input channel 4 of TIM module 7</b>
	GTM_TIM4_IN4_9			<b>Mux input channel 4 of TIM module 4</b>
	EBU_AD_IN8			<b>Data Bus Input</b>
	P30.4	O0		<b>General-purpose output</b>
	GTM_TOUT194	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_AD8	O		<b>Data Bus Output</b>

表 2-17 端口 P30 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AK23	P30.5	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM7_IN5_5			<b>Mux input channel 5 of TIM module 7</b>
	GTM_TIM4_IN5_9			<b>Mux input channel 5 of TIM module 4</b>
	EBU_AD_IN13			<b>Data Bus Input</b>
	P30.5	O0		<b>General-purpose output</b>
	GTM_TOUT195	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_AD13	O		<b>Data Bus Output</b>
AJ24	P30.6	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM7_IN6_5			<b>Mux input channel 6 of TIM module 7</b>
	GTM_TIM4_IN6_9			<b>Mux input channel 6 of TIM module 4</b>
	EBU_AD_IN4			<b>Data Bus Input</b>
	P30.6	O0		<b>General-purpose output</b>
	GTM_TOUT196	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_AD4	O		<b>Data Bus Output</b>

表 2-17 端口 P30 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AK24	P30.7	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM7_IN7_4			<b>Mux input channel 7 of TIM module 7</b>
	GTM_TIM4_IN7_9			<b>Mux input channel 7 of TIM module 4</b>
	EBU_AD_IN7			<b>Data Bus Input</b>
	P30.7	O0		<b>General-purpose output</b>
	GTM_TOUT197	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_AD7	O		<b>Data Bus Output</b>
AJ25	P30.8	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM6_IN0_8			<b>Mux input channel 0 of TIM module 6</b>
	GTM_TIM5_IN0_6			<b>Mux input channel 0 of TIM module 5</b>
	EBU_AD_IN3			<b>Data Bus Input</b>
	P30.8	O0		<b>General-purpose output</b>
	GTM_TOUT198	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_AD3	O		<b>Data Bus Output</b>

表 2-17 端口 P30 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AK25	P30.9	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM6_IN1_8			<b>Mux input channel 1 of TIM module 6</b>
	GTM_TIM5_IN1_7			<b>Mux input channel 1 of TIM module 5</b>
	EBU_AD_IN0			<b>Data Bus Input</b>
	P30.9	O0		<b>General-purpose output</b>
	GTM_TOUT199	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_AD0	O		<b>Data Bus Output</b>
AJ26	P30.10	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM6_IN2_8			<b>Mux input channel 2 of TIM module 6</b>
	GTM_TIM5_IN2_6			<b>Mux input channel 2 of TIM module 5</b>
	EBU_AD_IN5			<b>Data Bus Input</b>
	P30.10	O0		<b>General-purpose output</b>
	GTM_TOUT200	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_AD5	O		<b>Data Bus Output</b>

表 2-17 端口 P30 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AK26	P30.11	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM6_IN3_8			<b>Mux input channel 3 of TIM module 6</b>
	GTM_TIM5_IN3_7			<b>Mux input channel 3 of TIM module 5</b>
	EBU_AD_IN10			<b>Data Bus Input</b>
	P30.11	O0		<b>General-purpose output</b>
	GTM_TOUT201	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_AD10	O		<b>Data Bus Output</b>
AJ27	P30.12	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM6_IN4_7			<b>Mux input channel 4 of TIM module 6</b>
	GTM_TIM5_IN4_7			<b>Mux input channel 4 of TIM module 5</b>
	EBU_AD_IN9			<b>Data Bus Input</b>
	P30.12	O0		<b>General-purpose output</b>
	GTM_TOUT202	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_AD9	O		<b>Data Bus Output</b>

表 2-17 端口 P30 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AK27	P30.13	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM6_IN5_7			<b>Mux input channel 5 of TIM module 6</b>
	GTM_TIM5_IN5_7			<b>Mux input channel 5 of TIM module 5</b>
	EBU_AD_IN2			<b>Data Bus Input</b>
	P30.13	O0		<b>General-purpose output</b>
	GTM_TOUT203	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_AD2	O		<b>Data Bus Output</b>
AJ28	P30.14	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM6_IN6_7			<b>Mux input channel 6 of TIM module 6</b>
	GTM_TIM5_IN6_7			<b>Mux input channel 6 of TIM module 5</b>
	EBU_AD_IN1			<b>Data Bus Input</b>
	P30.14	O0		<b>General-purpose output</b>
	GTM_TOUT204	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_AD1	O		<b>Data Bus Output</b>

表 2-17 端口 P30 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AK28	P30.15	I	FAST / PU1 / VEBU / ES	General-purpose input
	GTM_TIM6_IN7_7			Mux input channel 7 of TIM module 6
	GTM_TIM5_IN7_6			Mux input channel 7 of TIM module 5
	EBU_AD_IN6			Data Bus Input
	P30.15	O0		General-purpose output
	GTM_TOUT205	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	EBU_AD6	O		Data Bus Output

表 2-18 端口 P31 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
AJ12	P31.0	I	FAST / PU1 / VEBU / ES	General-purpose input
	GTM_TIM7_IN0_8			Mux input channel 0 of TIM module 7
	GTM_TIM2_IN0_13			Mux input channel 0 of TIM module 2
	EBU_AD_IN30			Data Bus Input
	P31.0	O0		General-purpose output
	GTM_TOUT174	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	EBU_AD30	O		Data Bus Output

表 2-18 端口 P31 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AK12	P31.1	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM7_IN1_8			<b>Mux input channel 1 of TIM module 7</b>
	GTM_TIM2_IN1_9			<b>Mux input channel 1 of TIM module 2</b>
	EBU_AD_IN29			<b>Data Bus Input</b>
	P31.1	O0		<b>General-purpose output</b>
	GTM_TOUT175	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_AD29	O		<b>Data Bus Output</b>
AJ13	P31.2	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM7_IN2_7			<b>Mux input channel 2 of TIM module 7</b>
	GTM_TIM2_IN2_9			<b>Mux input channel 2 of TIM module 2</b>
	EBU_AD_IN28			<b>Data Bus Input</b>
	P31.2	O0		<b>General-purpose output</b>
	GTM_TOUT176	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_AD28	O		<b>Data Bus Output</b>

表 2-18 端口 P31 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AK13	P31.3	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM7_IN3_7			<b>Mux input channel 3 of TIM module 7</b>
	GTM_TIM2_IN3_14			<b>Mux input channel 3 of TIM module 2</b>
	EBU_AD_IN26			<b>Data Bus Input</b>
	P31.3	O0		<b>General-purpose output</b>
	GTM_TOUT177	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_AD26	O		<b>Data Bus Output</b>
AJ14	P31.4	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM7_IN4_6			<b>Mux input channel 4 of TIM module 7</b>
	GTM_TIM2_IN4_12			<b>Mux input channel 4 of TIM module 2</b>
	EBU_AD_IN24			<b>Data Bus Input</b>
	P31.4	O0		<b>General-purpose output</b>
	GTM_TOUT178	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_AD24	O		<b>Data Bus Output</b>

表 2-18 端口 P31 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AK14	P31.5	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM7_IN5_6			<b>Mux input channel 5 of TIM module 7</b>
	GTM_TIM2_IN5_13			<b>Mux input channel 5 of TIM module 2</b>
	EBU_AD_IN23			<b>Data Bus Input</b>
	P31.5	O0		<b>General-purpose output</b>
	GTM_TOUT179	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_AD23	O		<b>Data Bus Output</b>
AJ15	P31.6	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM7_IN6_6			<b>Mux input channel 6 of TIM module 7</b>
	GTM_TIM2_IN6_12			<b>Mux input channel 6 of TIM module 2</b>
	EBU_AD_IN20			<b>Data Bus Input</b>
	P31.6	O0		<b>General-purpose output</b>
	GTM_TOUT180	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_AD20	O		<b>Data Bus Output</b>

表 2-18 端口 P31 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AK15	P31.7	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM7_IN7_5			<b>Mux input channel 7 of TIM module 7</b>
	GTM_TIM2_IN7_14			<b>Mux input channel 7 of TIM module 2</b>
	EBU_AD_IN16			<b>Data Bus Input</b>
	P31.7	O0		<b>General-purpose output</b>
	GTM_TOUT181	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_AD16	O		<b>Data Bus Output</b>
AJ16	P31.8	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM6_IN0_9			<b>Mux input channel 0 of TIM module 6</b>
	GTM_TIM5_IN0_7			<b>Mux input channel 0 of TIM module 5</b>
	EBU_AD_IN31			<b>Data Bus Input</b>
	SENT_SENT20C			<b>Receive input channel 20</b>
	P31.8	O0		<b>General-purpose output</b>
	GTM_TOUT182	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
EBU_AD31	O	<b>Data Bus Output</b>		

表 2-18 端口 P31 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AK16	P31.9	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM6_IN1_9			<b>Mux input channel 1 of TIM module 6</b>
	GTM_TIM5_IN1_8			<b>Mux input channel 1 of TIM module 5</b>
	EBU_AD_IN27			<b>Data Bus Input</b>
	SENT_SENT21C			<b>Receive input channel 21</b>
	P31.9	O0		<b>General-purpose output</b>
	GTM_TOUT183	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_AD27	O		<b>Data Bus Output</b>
AJ17	P31.10	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM6_IN2_9			<b>Mux input channel 2 of TIM module 6</b>
	GTM_TIM5_IN2_7			<b>Mux input channel 2 of TIM module 5</b>
	EBU_AD_IN21			<b>Data Bus Input</b>
	SENT_SENT22C			<b>Receive input channel 22</b>
	P31.10	O0		<b>General-purpose output</b>
	GTM_TOUT184	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_AD21	O		<b>Data Bus Output</b>

表 2-18 端口 P31 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AK17	P31.11	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM6_IN3_9			<b>Mux input channel 3 of TIM module 6</b>
	GTM_TIM5_IN3_8			<b>Mux input channel 3 of TIM module 5</b>
	EBU_AD_IN25			<b>Data Bus Input</b>
	SENT_SENT23C			<b>Receive input channel 23</b>
	P31.11	O0		<b>General-purpose output</b>
	GTM_TOUT185	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_AD25	O		<b>Data Bus Output</b>
AJ18	P31.12	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM6_IN4_8			<b>Mux input channel 4 of TIM module 6</b>
	GTM_TIM5_IN4_8			<b>Mux input channel 4 of TIM module 5</b>
	EBU_AD_IN19			<b>Data Bus Input</b>
	SENT_SENT24C			<b>Receive input channel 24</b>
	P31.12	O0		<b>General-purpose output</b>
	GTM_TOUT186	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_AD19	O		<b>Data Bus Output</b>

表 2-18 端口 P31 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AK18	P31.13	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM6_IN5_8			<b>Mux input channel 5 of TIM module 6</b>
	GTM_TIM5_IN5_8			<b>Mux input channel 5 of TIM module 5</b>
	EBU_AD_IN22			<b>Data Bus Input</b>
	P31.13	O0		<b>General-purpose output</b>
	GTM_TOUT187	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_AD22	O		<b>Data Bus Output</b>
AJ19	P31.14	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM6_IN6_8			<b>Mux input channel 6 of TIM module 6</b>
	GTM_TIM5_IN6_8			<b>Mux input channel 6 of TIM module 5</b>
	EBU_AD_IN18			<b>Data Bus Input</b>
	P31.14	O0		<b>General-purpose output</b>
	GTM_TOUT188	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_AD18	O		<b>Data Bus Output</b>

表 2-18 端口 P31 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AK19	P31.15	I	FAST / PU1 / VEBU / ES	<b>General-purpose input</b>
	GTM_TIM6_IN7_8			<b>Mux input channel 7 of TIM module 6</b>
	GTM_TIM5_IN7_7			<b>Mux input channel 7 of TIM module 5</b>
	EBU_AD_IN17			<b>Data Bus Input</b>
	P31.15	O0		<b>General-purpose output</b>
	GTM_TOUT189	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	EBU_AD17	O		<b>Data Bus Output</b>

表 2-19 端口 P32 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
AE22	P32.0	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b> P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
	GTM_TIM3_IN2_5			<b>Mux input channel 2 of TIM module 3</b>
	GTM_TIM2_IN2_5			<b>Mux input channel 2 of TIM module 2</b>
	P32.0	O0		<b>General-purpose output</b>
	GTM_TOUT36	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>

表 2-19 端口 P32 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AD22	P32.1	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b> P32.1 / External Pass Device gate control for EVRC
	GTM_TIM3_IN3_15			<b>Mux input channel 3 of TIM module 3</b>
	P32.1	O0		<b>General-purpose output</b>
	GTM_TOUT37	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
AE23	P32.2	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN3_8			<b>Mux input channel 3 of TIM module 1</b>
	GTM_TIM0_IN3_8			<b>Mux input channel 3 of TIM module 0</b>
	CAN03_RXDB			<b>CAN receive input node 3</b>
	ASCLIN3_ARXD			<b>Receive input</b>
	CAN21_RXDD			<b>CAN receive input node 1</b>
	P32.2	O0		<b>General-purpose output</b>
	GTM_TOUT38	O1		<b>GTM muxed output</b>
	ASCLIN3_ATX	O2		<b>Transmit output</b>
	IOM_MON2_15			<b>Monitor input 2</b>
	IOM_REF2_15			<b>Reference input 2</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	PMS_DCDCSYNCO	O6		<b>DC-DC synchronization output</b>
	—	O7		<b>Reserved</b>

表 2-19 端口 P32 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AE24	P32.3	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN4_5			<b>Mux input channel 4 of TIM module 1</b>
	GTM_TIM0_IN4_5			<b>Mux input channel 4 of TIM module 0</b>
	P32.3	O0		<b>General-purpose output</b>
	GTM_TOUT39	O1		<b>GTM muxed output</b>
	ASCLIN3_ATX	O2		<b>Transmit output</b>
	IOM_MON2_15			<b>Monitor input 2</b>
	IOM_REF2_15	O3		<b>Reference input 2</b>
	—			<b>Reserved</b>
	ASCLIN3_ASCLK			<b>Shift clock output</b>
	CAN03_TXD	O5		<b>CAN transmit output node 3</b>
	IOM_MON2_8			<b>Monitor input 2</b>
	IOM_REF2_8			<b>Reference input 2</b>
	CAN21_TXD	O6		<b>CAN transmit output node 1</b>
	—	O7		<b>Reserved</b>
AD23	P32.4	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN5_5			<b>Mux input channel 5 of TIM module 1</b>
	GTM_TIM0_IN5_5			<b>Mux input channel 5 of TIM module 0</b>
	ASCLIN1_ACTSB			<b>Clear to send input</b>
	MSC1_SDI2			<b>Upstream asynchronous input signal</b>
	P32.4	O0		<b>General-purpose output</b>
	GTM_TOUT40	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	GTM_CLK1	O4		<b>CGM generated clock</b>
	MSC1_EN0	O5		<b>Chip Select</b>
	CCU_EXTCLK1	O6		<b>External Clock 1</b>
	CCU60_COUT63			<b>T13 PWM channel 63</b>
	IOM_MON1_6	O7		<b>Monitor input 1</b>
	IOM_REF1_0			<b>Reference input 1</b>
PMS_DCDCSYNCO	O		<b>DC-DC synchronization output</b>	

表 2-19 端口 P32 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
AA20	P32.5	I	SLOW / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM5_IN5_9			Mux input channel 5 of TIM module 5	
	GTM_TIM4_IN1_14			Mux input channel 1 of TIM module 4	
	GTM_TIM3_IN5_8			Mux input channel 5 of TIM module 3	
	SENT_SENT10C			Receive input channel 10	
	P32.5	O0		General-purpose output	
	GTM_TOUT140	O1		GTM muxed output	
	ASCLIN2_ATX	O2		Transmit output	
	IOM_MON2_14			Monitor input 2	
	IOM_REF2_14			Reference input 2	
	—	O3		Reserved	
	—	O4		Reserved	
	—	O5		Reserved	
	CAN02_TXD	O6		CAN transmit output node 2	
	IOM_MON2_7			Monitor input 2	
	IOM_REF2_7			Reference input 2	
	—	O7		Reserved	
AB20	P32.6	I	SLOW / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM5_IN6_9			Mux input channel 6 of TIM module 5	
	GTM_TIM4_IN4_15			Mux input channel 4 of TIM module 4	
	GTM_TIM3_IN6_8			Mux input channel 6 of TIM module 3	
	CAN02_RXDC			CAN receive input node 2	
	CBS_TGI4			Trigger input	
	ASCLIN2_ARXF			Receive input	
	ASCLIN6_ARXC			Receive input	
	SENT_SENT11C			Receive input channel 11	
	P32.6			O0	General-purpose output
	GTM_TOUT141			O1	GTM muxed output
	—			O2	Reserved
	—			O3	Reserved
	QSPI2_SLSO12			O4	Master slave select output
	CAN22_TXD			O5	CAN transmit output node 2
	—			O6	Reserved
	—			O7	Reserved
CBS_TGO4	O	Trigger output			

表 2-19 端口 P32 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AB21	P32.7	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM5_IN7_8			<b>Mux input channel 7 of TIM module 5</b>
	GTM_TIM4_IN0_15			<b>Mux input channel 0 of TIM module 4</b>
	GTM_TIM3_IN7_8			<b>Mux input channel 7 of TIM module 3</b>
	CBS_TGI5			<b>Trigger input</b>
	CAN22_RXDB			<b>CAN receive input node 2</b>
	SENT_SENT12C			<b>Receive input channel 12</b>
	P32.7			O0
	GTM_TOUT142	O1		<b>GTM muxed output</b>
	ASCLIN6_ATX	O2		<b>Transmit output</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	CBS_TGO5	O		<b>Trigger output</b>

表 2-20 端口 P33 功能

Ball	Symbol	Ctrl.	Buffer Type	Function	
AD15	P33.0	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>	
	GTM_TIM3_IN0_13			<b>Mux input channel 0 of TIM module 3</b>	
	GTM_TIM1_IN4_6			<b>Mux input channel 4 of TIM module 1</b>	
	GTM_TIM0_IN4_6			<b>Mux input channel 4 of TIM module 0</b>	
	EDSADC_ITR0E			<b>Trigger/Gate input, channel 0</b>	
	SENT_SENT13C			<b>Receive input channel 13</b>	
	IOM_PIN_0			<b>GPIO pad input to FPC</b>	
	GTM_DTMT1_2			<b>CDTM1_DTM0</b>	
	EVADC_G10CH7			AI	<b>Analog input channel 7, group 10</b>
	EVADC_FC7CH0				<b>Analog input FC channel 7</b>
	P33.0	O0	<b>General-purpose output</b>		
	GTM_TOUT22	O1	<b>GTM muxed output</b>		
	IOM_MON0_0		<b>Monitor input 0</b>		
	IOM_GTM_0		<b>GTM-provided inputs to EXOR combiner</b>		
	ASCLIN5_ATX	O2	<b>Transmit output</b>		
	—	O3	<b>Reserved</b>		
	—	O4	<b>Reserved</b>		
	—	O5	<b>Reserved</b>		
	EVADC_FC2BFLOUT	O6	<b>Boundary flag output, FC channel 2</b>		
	—	O7	<b>Reserved</b>		

表 2-20 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AE15	P33.1	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM3_IN1_15			<b>Mux input channel 1 of TIM module 3</b>
	GTM_TIM1_IN5_6			<b>Mux input channel 5 of TIM module 1</b>
	GTM_TIM0_IN5_6			<b>Mux input channel 5 of TIM module 0</b>
	EDSADC_ITR1E			<b>Trigger/Gate input, channel 1</b>
	PSI5_RX0C			<b>RXD inputs (receive data) channel 0</b>
	EDSADC_DSCIN2B			<b>Modulator clock input, channel 2</b>
	SENT_SENT9C			<b>Receive input channel 9</b>
	ASCLIN8_ARXC			<b>Receive input</b>
	IOM_PIN_1			<b>GPIO pad input to FPC</b>
	EVADC_G10CH6			AI
	EVADC_FC6CH0	<b>Analog input FC channel 6</b>		
	P33.1	O0	<b>General-purpose output</b>	
	GTM_TOUT23	O1	<b>GTM muxed output</b>	
	IOM_MON0_1		<b>Monitor input 0</b>	
	IOM_GTM_1		<b>GTM-provided inputs to EXOR combiner</b>	
	ASCLIN3_ASLSO	O2	<b>Slave select signal output</b>	
	QSPI2_SCLK	O3	<b>Master SPI clock output</b>	
	EDSADC_DSCOUT2	O4	<b>Modulator clock output</b>	
	EVADC_EMUX02	O5	<b>Control of external analog multiplexer interface 0</b>	
	EVADC_FC4BFLOUT	O6	<b>Boundary flag output, FC channel 4</b>	
	—	O7	<b>Reserved</b>	

表 2-20 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AD16	P33.2	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM3_IN2_14			<b>Mux input channel 2 of TIM module 3</b>
	GTM_TIM1_IN6_6			<b>Mux input channel 6 of TIM module 1</b>
	GTM_TIM0_IN6_6			<b>Mux input channel 6 of TIM module 0</b>
	EDSADC_ITR2E			<b>Trigger/Gate input, channel 2</b>
	SENT_SENT8C			<b>Receive input channel 8</b>
	EDSADC_DSDIN2B			<b>Digital datastream input, channel 2</b>
	IOM_PIN_2			<b>GPIO pad input to FPC</b>
	EVADC_G10CH5			AI
	EVADC_FC5CH0	<b>Analog input FC channel 5</b>		
	P33.2	O0	<b>General-purpose output</b>	
	GTM_TOUT24	O1	<b>GTM muxed output</b>	
	IOM_MON0_2		<b>Monitor input 0</b>	
	IOM_GTM_2		<b>GTM-provided inputs to EXOR combiner</b>	
	ASCLIN3_ASCLK	O2	<b>Shift clock output</b>	
	QSPI2_SLSO10	O3	<b>Master slave select output</b>	
	PSI5_TX0	O4	<b>TXD outputs (send data)</b>	
	IOM_MON1_14		<b>Monitor input 1</b>	
	IOM_REF1_14		<b>Reference input 1</b>	
	EVADC_EMUX01	O5	<b>Control of external analog multiplexer interface 0</b>	
	EVADC_FC3BFLOUT	O6	<b>Boundary flag output, FC channel 3</b>	
—	O7	<b>Reserved</b>		

表 2-20 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AE16	P33.3	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM3_IN3_12			<b>Mux input channel 3 of TIM module 3</b>
	GTM_TIM1_IN7_6			<b>Mux input channel 7 of TIM module 1</b>
	GTM_TIM0_IN7_6			<b>Mux input channel 7 of TIM module 0</b>
	PSI5_RX1C			<b>RXD inputs (receive data) channel 1</b>
	SENT_SENT7C			<b>Receive input channel 7</b>
	EDSADC_DSCIN1B			<b>Modulator clock input, channel 1</b>
	IOM_PIN_3			<b>GPIO pad input to FPC</b>
	EVADC_G10CH4			AI
	EVADC_FC4CH0	<b>Analog input FC channel 4</b>		
	P33.3	O0	<b>General-purpose output</b>	
	GTM_TOUT25	O1	<b>GTM muxed output</b>	
	IOM_MON0_3		<b>Monitor input 0</b>	
	IOM_GTM_3		<b>GTM-provided inputs to EXOR combiner</b>	
	ASCLIN5_ASCLK	O2	<b>Shift clock output</b>	
	QSPI4_SLSO2	O3	<b>Master slave select output</b>	
	EDSADC_DSCOUT1	O4	<b>Modulator clock output</b>	
	EVADC_EMUX00	O5	<b>Control of external analog multiplexer interface 0</b>	
	EVADC_FC5BFLOUT	O6	<b>Boundary flag output, FC channel 5</b>	
	—	O7	<b>Reserved</b>	

表 2-20 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AD17	P33.4	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM4_IN4_10			<b>Mux input channel 4 of TIM module 4</b>
	GTM_TIM1_IN0_10			<b>Mux input channel 0 of TIM module 1</b>
	GTM_TIM0_IN0_10			<b>Mux input channel 0 of TIM module 0</b>
	EDSADC_ITR0F			<b>Trigger/Gate input, channel 0</b>
	SENT_SENT6C			<b>Receive input channel 6</b>
	EDSADC_DSDIN1B			<b>Digital datastream input, channel 1</b>
	CCU61_CTRAPC			<b>Trap input capture</b>
	ASCLIN5_ARXB			<b>Receive input</b>
	IOM_PIN_4			<b>GPIO pad input to FPC</b>
	GTM_DTMT2_0			<b>CDTM2_DTM0</b>
	EVADC_G10CH3	AI	<b>Analog input channel 3, group 10</b>	
	P33.4	O0	<b>General-purpose output</b>	
	GTM_TOUT26	O1	<b>GTM muxed output</b>	
	IOM_MON0_4		<b>Monitor input 0</b>	
	IOM_GTM_4		<b>GTM-provided inputs to EXOR combiner</b>	
	ASCLIN2_ARTS	O2	<b>Ready to send output</b>	
	QSPI2_SLSO12	O3	<b>Master slave select output</b>	
	PSI5_TX1	O4	<b>TXD outputs (send data)</b>	
	IOM_MON1_15		<b>Monitor input 1</b>	
EVADC_EMUX12	<b>Control of external analog multiplexer interface 1</b>			
EVADC_FC0BFLOUT	<b>Boundary flag output, FC channel 0</b>			
CAN13_TXD	O7	<b>CAN transmit output node 3</b>		

表 2-20 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AE17	P33.5	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM4_IN5_10			<b>Mux input channel 5 of TIM module 4</b>
	GTM_TIM1_IN1_8			<b>Mux input channel 1 of TIM module 1</b>
	GTM_TIM0_IN1_8			<b>Mux input channel 1 of TIM module 0</b>
	EDSADC_DSCIN0B			<b>Modulator clock input, channel 0</b>
	EDSADC_ITR1F			<b>Trigger/Gate input, channel 1</b>
	GPT120_T4EUDB			<b>Count direction control input of timer T4</b>
	PSI5S_RXC			<b>RX data input</b>
	ASCLIN2_ACTSB			<b>Clear to send input</b>
	CCU61_CCPOS2C			<b>Hall capture input 2</b>
	PSI5_RX2C			<b>RXD inputs (receive data) channel 2</b>
	SENT_SENT5C			<b>Receive input channel 5</b>
	CAN13_RXDB			<b>CAN receive input node 3</b>
	IOM_PIN_5			<b>GPIO pad input to FPC</b>
	EVADC_G10CH2	AI	<b>Analog input channel 2, group 10</b>	
	P33.5	O0	<b>General-purpose output</b>	
	GTM_TOUT27	O1	<b>GTM muxed output</b>	
	IOM_MON0_5	O1	<b>Monitor input 0</b>	
	IOM_GTM_5		<b>GTM-provided inputs to EXOR combiner</b>	
	QSPI0_SLSO7	O2	<b>Master slave select output</b>	
QSPI1_SLSO7	O3	<b>Master slave select output</b>		
EDSADC_DSCOUT0	O4	<b>Modulator clock output</b>		
EVADC_EMUX11	O5	<b>Control of external analog multiplexer interface 1</b>		
EVADC_FC2BFLOUT	O6	<b>Boundary flag output, FC channel 2</b>		
ASCLIN5_ASLSO	O7	<b>Slave select signal output</b>		

表 2-20 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AD18	P33.6	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM1_IN2_9			<b>Mux input channel 2 of TIM module 1</b>
	GTM_TIM0_IN2_9			<b>Mux input channel 2 of TIM module 0</b>
	EDSADC_ITR2F			<b>Trigger/Gate input, channel 2</b>
	GPT120_T2EUDB			<b>Count direction control input of timer T2</b>
	SENT_SENT4C			<b>Receive input channel 4</b>
	CCU61_CCPOS1C			<b>Hall capture input 1</b>
	EDSADC_DSDIN0B			<b>Digital datastream input, channel 0</b>
	ASCLIN8_ARXD			<b>Receive input</b>
	IOM_PIN_6			<b>GPIO pad input to FPC</b>
	GTM_DTMT2_1			<b>CDTM2_DTM0</b>
	EVADC_G10CH1			AI
	P33.6	O0	<b>General-purpose output</b>	
	GTM_TOUT28	O1	<b>GTM muxed output</b>	
	IOM_MON0_6		<b>Monitor input 0</b>	
	IOM_GTM_6		<b>GTM-provided inputs to EXOR combiner</b>	
	ASCLIN2_ASLSO	O2	<b>Slave select signal output</b>	
	QSPI2_SLSO11	O3	<b>Master slave select output</b>	
	PSI5_TX2	O4	<b>TXD outputs (send data)</b>	
	IOM_REF1_15		<b>Reference input 1</b>	
	EVADC_EMUX10		<b>Control of external analog multiplexer interface 1</b>	
	EVADC_FC1BFLOUT	O6	<b>Boundary flag output, FC channel 1</b>	
	PSI5_TX	O7	<b>TX data output</b>	

表 2-20 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AE18	P33.7	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM1_IN3_9			<b>Mux input channel 3 of TIM module 1</b>
	GTM_TIM0_IN3_9			<b>Mux input channel 3 of TIM module 0</b>
	CAN00_RXDE			<b>CAN receive input node 0</b>
	GPT120_T2INB			<b>Trigger/gate input of timer T2</b>
	CCU61_CCPOS0C			<b>Hall capture input 0</b>
	SCU_E_REQ4_0			<b>ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	SENT_SENT14C			<b>Receive input channel 14</b>
	IOM_PIN_7			<b>GPIO pad input to FPC</b>
	EVADC_G10CH0			AI
	P33.7	O0	<b>General-purpose output</b>	
	GTM_TOUT29	O1	<b>GTM muxed output</b>	
	IOM_MON0_7		<b>Monitor input 0</b>	
	IOM_GTM_7		<b>GTM-provided inputs to EXOR combiner</b>	
	ASCLIN2_ASCLK	O2	<b>Shift clock output</b>	
	QSPI4_SLSO7	O3	<b>Master slave select output</b>	
	ASCLIN8_ATX	O4	<b>Transmit output</b>	
	—	O5	<b>Reserved</b>	
	EVADC_FC3BFLOUT	O6	<b>Boundary flag output, FC channel 3</b>	
	—	O7	<b>Reserved</b>	

表 2-20 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AD19	P33.8	I	FAST / HighZ / VEVR SB	<b>General-purpose input</b>
	GTM_TIM1_IN4_7			<b>Mux input channel 4 of TIM module 1</b>
	GTM_TIM0_IN4_7			<b>Mux input channel 4 of TIM module 0</b>
	ASCLIN2_ARXE			<b>Receive input</b>
	SCU_EMGSTOP_POR T_A			<b>Emergency stop Port Pin A input request</b>
	IOM_PIN_8			<b>GPIO pad input to FPC</b>
	P33.8			O0
	GTM_TOUT30	O1		<b>GTM muxed output</b>
	IOM_MON0_8			<b>Monitor input 0</b>
	ASCLIN2_ATX	O2		<b>Transmit output</b>
	IOM_MON2_14			<b>Monitor input 2</b>
	IOM_REF2_14			<b>Reference input 2</b>
	QSPI4_SLSO2	O3		<b>Master slave select output</b>
	—	O4		<b>Reserved</b>
	CAN00_TXD	O5		<b>CAN transmit output node 0</b>
	IOM_MON2_5			<b>Monitor input 2</b>
	IOM_REF2_5			<b>Reference input 2</b>
	—	O6		<b>Reserved</b>
	CCU61_COUT62	O7		<b>T12 PWM channel 62</b>
	IOM_MON1_13			<b>Monitor input 1</b>
IOM_REF1_8		<b>Reference input 1</b>		
SMU_FSP0	O	<b>FSP[1..0] Output Signals - Generated by SMU_core</b>		

表 2-20 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AE19	P33.9	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM1_IN1_9			<b>Mux input channel 1 of TIM module 1</b>
	GTM_TIM0_IN1_9			<b>Mux input channel 1 of TIM module 0</b>
	QSPI3_HSICINA			<b>Highspeed capture channel</b>
	IOM_PIN_9			<b>GPIO pad input to FPC</b>
	P33.9	O0		<b>General-purpose output</b>
	GTM_TOUT31	O1		<b>GTM muxed output</b>
	IOM_MON0_9			<b>Monitor input 0</b>
	ASCLIN2_ATX	O2		<b>Transmit output</b>
	IOM_MON2_14			<b>Monitor input 2</b>
	IOM_REF2_14			<b>Reference input 2</b>
	QSPI4_SLSO1	O3		<b>Master slave select output</b>
	ASCLIN2_ASCLK	O4		<b>Shift clock output</b>
	CAN01_TXD	O5		<b>CAN transmit output node 1</b>
	IOM_MON2_6			<b>Monitor input 2</b>
	IOM_REF2_6			<b>Reference input 2</b>
	ASCLIN0_ATX	O6		<b>Transmit output</b>
	IOM_MON2_12			<b>Monitor input 2</b>
	IOM_REF2_12			<b>Reference input 2</b>
	CCU61_CC62	O7		<b>T12 PWM channel 62</b>
	IOM_MON1_10			<b>Monitor input 1</b>
	IOM_REF1_11			<b>Reference input 1</b>

表 2-20 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AD20	P33.10	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM4_IN4_14			Mux input channel 4 of TIM module 4
	GTM_TIM1_IN0_9			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_9			Mux input channel 0 of TIM module 0
	QSPI4_SLSIA			Slave select input
	QSPI3_HSICINB			Highspeed capture channel
	CAN01_RXDD			CAN receive input node 1
	ASCLIN0_ARXD			Receive input
	IOM_PIN_10			GPIO pad input to FPC
	P33.10			00
	GTM_TOUT32	01	GTM muxed output	
	IOM_MON0_10	02	Monitor input 0	
	QSPI1_SLSO6		Master slave select output	
	QSPI4_SLSO0	03	Master slave select output	
	ASCLIN1_ASLSO	04	Slave select signal output	
	PSI5S_CLK	05	PSI5S CLK is a clock that can be used on a pin to drive the external PHY.	
	—	06	Reserved	
	CCU61_COUT61	07	T12 PWM channel 61	
	IOM_MON1_12	0	Monitor input 1	
	IOM_REF1_9		Reference input 1	
SMU_FSP1		FSP[1..0] Output Signals - Generated by SMU_core		
AE20	P33.11	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN2_8			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_8			Mux input channel 2 of TIM module 0
	QSPI4_SCLKA			Slave SPI clock inputs
	IOM_PIN_11			GPIO pad input to FPC
	P33.11	00	General-purpose output	
	GTM_TOUT33	01	GTM muxed output	
	IOM_MON0_11	02	Monitor input 0	
	ASCLIN1_ASCLK		Shift clock output	
	QSPI4_SCLK	03	Master SPI clock output	
	—	04	Reserved	
	—	05	Reserved	
	EDSADC_CGPWMN	06	Negative carrier generator output	
	CCU61_CC61	07	T12 PWM channel 61	
	IOM_MON1_9	0	Monitor input 1	
	IOM_REF1_12		Reference input 1	

表 2-20 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AD21	P33.12	I	FAST / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM3_IN0_6			<b>Mux input channel 0 of TIM module 3</b>
	GTM_TIM2_IN0_6			<b>Mux input channel 0 of TIM module 2</b>
	QSPI4_MTSRA			<b>Slave SPI data input</b>
	CAN00_RXDD			<b>CAN receive input node 0</b>
	PMS_PINBWKP			<b>PINB (P33.12) pin input</b>
	IOM_PIN_12			<b>GPIO pad input to FPC</b>
	P33.12			O0
	GTM_TOUT34	O1		<b>GTM muxed output</b>
	IOM_MON0_12			<b>Monitor input 0</b>
	ASCLIN1_ATX	O2		<b>Transmit output</b>
	IOM_MON2_13			<b>Monitor input 2</b>
	IOM_REF2_13			<b>Reference input 2</b>
	QSPI4_MTSR	O3		<b>Master SPI data output</b>
	ASCLIN1_ASCLK	O4		<b>Shift clock output</b>
	CAN22_TXD	O5		<b>CAN transmit output node 2</b>
	EDSADC_CGPWMP	O6		<b>Positive carrier generator output</b>
	CCU61_COUT60	O7		<b>T12 PWM channel 60</b>
	IOM_MON1_11			<b>Monitor input 1</b>
	IOM_REF1_10			<b>Reference input 1</b>

表 2-20 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AE21	P33.13	I	FAST / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM3_IN1_5			<b>Mux input channel 1 of TIM module 3</b>
	GTM_TIM2_IN1_5			<b>Mux input channel 1 of TIM module 2</b>
	ASCLIN1_ARXF			<b>Receive input</b>
	EDSADC_SGNB			<b>Carrier sign signal input</b>
	QSPI4_MRSTA			<b>Master SPI data input</b>
	MSC1_INJ1			<b>Injection signal from port</b>
	CAN22_RXDA			<b>CAN receive input node 2</b>
	P33.13			O0
	GTM_TOUT35	O1	<b>GTM muxed output</b>	
	ASCLIN1_ATX	O2	<b>Transmit output</b>	
	IOM_MON2_13		<b>Monitor input 2</b>	
	IOM_REF2_13		<b>Reference input 2</b>	
	QSPI4_MRST	O3	<b>Slave SPI data output</b>	
	IOM_MON2_4		<b>Monitor input 2</b>	
	IOM_REF2_4		<b>Reference input 2</b>	
	QSPI2_SLSO6	O4	<b>Master slave select output</b>	
	CAN00_TXD	O5	<b>CAN transmit output node 0</b>	
	IOM_MON2_5		<b>Monitor input 2</b>	
	IOM_REF2_5		<b>Reference input 2</b>	
	—	O6	<b>Reserved</b>	
	CCU61_CC60	O7	<b>T12 PWM channel 60</b>	
	IOM_MON1_8		<b>Monitor input 1</b>	
	IOM_REF1_13		<b>Reference input 1</b>	

表 2-20 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AA19	P33.14	I	FAST / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM5_IN0_8			<b>Mux input channel 0 of TIM module 5</b>
	GTM_TIM4_IN5_14			<b>Mux input channel 5 of TIM module 4</b>
	GTM_TIM2_IN0_8			<b>Mux input channel 0 of TIM module 2</b>
	QSPI2_SCLKD			<b>Slave SPI clock inputs</b>
	CBS_TGI6			<b>Trigger input</b>
	P33.14	O0		<b>General-purpose output</b>
	GTM_TOUT143	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	QSPI2_SCLK	O3		<b>Master SPI clock output</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	CCU60_CC62	O7		<b>T12 PWM channel 62</b>
	IOM_MON1_0			<b>Monitor input 1</b>
	IOM_REF1_4			<b>Reference input 1</b>
CBS_TGO6	O	<b>Trigger output</b>		
AB19	P33.15	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM5_IN1_9			<b>Mux input channel 1 of TIM module 5</b>
	GTM_TIM4_IN6_12			<b>Mux input channel 6 of TIM module 4</b>
	GTM_TIM2_IN1_7			<b>Mux input channel 1 of TIM module 2</b>
	CBS_TGI7			<b>Trigger input</b>
	P33.15	O0		<b>General-purpose output</b>
	GTM_TOUT144	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	QSPI2_SLSO11	O3		<b>Master slave select output</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	CCU60_COUT62	O7		<b>T12 PWM channel 62</b>
	IOM_MON1_5			<b>Monitor input 1</b>
	IOM_REF1_1			<b>Reference input 1</b>
	CBS_TGO7	O		<b>Trigger output</b>

表 2-21 端口 P34 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
AB16	P34.1	I	SLOW / PU1 / VEVR SB / ES5	<b>General-purpose input</b>
	GTM_TIM5_IN3_9			<b>Mux input channel 3 of TIM module 5</b>
	GTM_TIM3_IN4_12			<b>Mux input channel 4 of TIM module 3</b>
	GTM_TIM2_IN3_9			<b>Mux input channel 3 of TIM module 2</b>
	EVADC_G10CH11	AI		<b>Analog input channel 11, group 10</b>
	P34.1	O0		<b>General-purpose output</b>
	GTM_TOUT146	O1		<b>GTM muxed output</b>
	ASCLIN4_ATX	O2		<b>Transmit output</b>
	—	O3		<b>Reserved</b>
	CAN00_TXD	O4		<b>CAN transmit output node 0</b>
	IOM_MON2_5			<b>Monitor input 2</b>
	IOM_REF2_5			<b>Reference input 2</b>
	CAN20_TXD	O5		<b>CAN transmit output node 0</b>
	—	O6		<b>Reserved</b>
	CCU60_COUT63	O7		<b>T13 PWM channel 63</b>
	IOM_MON1_6		<b>Monitor input 1</b>	
IOM_REF1_0		<b>Reference input 1</b>		
AA17	P34.2	I	SLOW / PU1 / VEVR SB / ES	<b>General-purpose input</b>
	GTM_TIM5_IN4_9			<b>Mux input channel 4 of TIM module 5</b>
	GTM_TIM3_IN5_13			<b>Mux input channel 5 of TIM module 3</b>
	GTM_TIM2_IN4_8			<b>Mux input channel 4 of TIM module 2</b>
	ASCLIN4_ARXB			<b>Receive input</b>
	CAN00_RXDG			<b>CAN receive input node 0</b>
	CAN20_RXDC			<b>CAN receive input node 0</b>
	EVADC_G10CH10	AI		<b>Analog input channel 10, group 10</b>
	P34.2	O0		<b>General-purpose output</b>
	GTM_TOUT147	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	CCU60_CC60	O7	<b>T12 PWM channel 60</b>	
IOM_MON1_2		<b>Monitor input 1</b>		
IOM_REF1_6		<b>Reference input 1</b>		

表 2-21 端口 P34 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AB17	P34.3	I	SLOW / PU1 / VEVRSB / ES	General-purpose input
	GTM_TIM5_IN5_10			Mux input channel 5 of TIM module 5
	GTM_TIM3_IN6_13			Mux input channel 6 of TIM module 3
	GTM_TIM2_IN5_9			Mux input channel 5 of TIM module 2
	EVADC_G10CH9	AI		Analog input channel 9, group 10
	P34.3	O0		General-purpose output
	GTM_TOUT148	O1		GTM muxed output
	ASCLIN4_ASCLK	O2		Shift clock output
	—	O3		Reserved
	QSPI2_SLSO10	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT60	O7		T12 PWM channel 60
	IOM_MON1_3			Monitor input 1
IOM_REF1_3	Reference input 1			
AA18	P34.4	I	SLOW / PU1 / VEVRSB / ES	General-purpose input
	GTM_TIM5_IN6_10			Mux input channel 6 of TIM module 5
	GTM_TIM3_IN7_12			Mux input channel 7 of TIM module 3
	GTM_TIM2_IN6_8			Mux input channel 6 of TIM module 2
	QSPI2_MRSTD			Master SPI data input
	EVADC_G10CH8	AI		Analog input channel 8, group 10
	P34.4	O0		General-purpose output
	GTM_TOUT149	O1		GTM muxed output
	ASCLIN4_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	QSPI2_MRST	O4		Slave SPI data output
	IOM_MON2_2			Monitor input 2
	IOM_REF2_2			Reference input 2
	—			O5
	EVADC_FC6BFLOUT	O6		Boundary flag output, FC channel 6
	CCU60_CC61	O7		T12 PWM channel 61
IOM_MON1_1	Monitor input 1			
IOM_REF1_5	Reference input 1			

表 2-21 端口 P34 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AB18	P34.5	I	FAST / PU1 / VEVRSB / ES	General-purpose input
	GTM_TIM5_IN7_9			Mux input channel 7 of TIM module 5
	GTM_TIM4_IN7_12			Mux input channel 7 of TIM module 4
	GTM_TIM2_IN7_9			Mux input channel 7 of TIM module 2
	QSPI2_MTSRD			Slave SPI data input
	ASCLIN8_ARXE			Receive input
	P34.5	O0		General-purpose output
	GTM_TOUT150	O1		GTM muxed output
	ASCLIN8_ATX	O2		Transmit output
	—	O3		Reserved
	QSPI2_MTSR	O4		Master SPI data output
	—	O5		Reserved
	EVADC_FC7BFLOUT	O6		Boundary flag output, FC channel 7
	CCU60_COUT61	O7		T12 PWM channel 61
	IOM_MON1_4			Monitor input 1
IOM_REF1_2		Reference input 1		

表 2-22 模拟输入

Ball	Symbol	Ctrl.	Buffer Type	Function
AA15	AN0	I	D / HighZ / VDDM	Analog Input 0
	EVADC_G0CH0			Analog input channel 0, group 0
	EDSADC_EDS3PA			Positive analog input channel 3, pin A
AB15	AN1	I	D / HighZ / VDDM	Analog Input 1
	EVADC_G0CH1			Analog input channel 1, group 0
	EDSADC_EDS3NA			Negative analog input channel 3, pin A
AD14	AN2	I	D / HighZ / VDDM	Analog Input 2
	EVADC_G0CH2			Analog input channel 2, group 0
	EDSADC_EDS0PA			Positive analog input channel 0, pin A
AB14	AN3	I	D / HighZ / VDDM	Analog Input 3
	EVADC_G0CH3			Analog input channel 3, group 0
	EDSADC_EDS0NA			Negative analog input channel 0, pin A
AA14	AN4	I	D / HighZ / VDDM	Analog Input 4
	EVADC_G11CH0			Analog input channel 0, group 11
	EVADC_G0CH4			Analog input channel 4, group 0
AE14	AN5	I	D / HighZ / VDDM	Analog Input 5
	EVADC_G11CH1			Analog input channel 1, group 11
	EVADC_G0CH5			Analog input channel 5, group 0

表 2-22 模拟输入 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AA13	AN6	I	D / HighZ / VDDM	<b>Analog Input 6</b>
	EVADC_G11CH2			<b>Analog input channel 2, group 11</b>
	EVADC_G0CH6			<b>Analog input channel 6, group 0</b>
AB13	AN7	I	D / HighZ / VDDM	<b>Analog Input 7</b>
	EVADC_G11CH3			<b>Analog input channel 3, group 11</b>
	EVADC_G0CH7			<b>Analog input channel 7, group 0</b>
AD13	AN8	I	D / HighZ / VDDM	<b>Analog Input 8</b>
	EVADC_G11CH4			<b>Analog input channel 4, group 11</b>
	EVADC_G1CH0			<b>Analog input channel 0, group 1</b>
AB12	AN9	I	D / HighZ / VDDM	<b>Analog Input 9</b>
	EVADC_G11CH5			<b>Analog input channel 5, group 11</b>
	EVADC_G1CH1			<b>Analog input channel 1, group 1</b>
AE13	AN10	I	D / HighZ / VDDM	<b>Analog Input 10</b>
	EVADC_G11CH6			<b>Analog input channel 6, group 11</b>
	EVADC_G1CH2			<b>Analog input channel 2, group 1</b>
AD12	AN11	I	D / HighZ / VDDM	<b>Analog Input 11</b>
	EVADC_G11CH7			<b>Analog input channel 7, group 11</b>
	EVADC_G1CH3			<b>Analog input channel 3, group 1</b>
AA12	AN12	I	D / HighZ / VDDM	<b>Analog Input 12</b>
	EVADC_G1CH4			<b>Analog input channel 4, group 1</b>
	EDSADC_EDS0PB			<b>Positive analog input channel 0, pin B</b>
AD11	AN13	I	D / HighZ / VDDM	<b>Analog Input 13</b>
	EVADC_G1CH5			<b>Analog input channel 5, group 1</b>
	EDSADC_EDS0NB			<b>Negative analog input channel 0, pin B</b>
AB11	AN14	I	D / HighZ / VDDM	<b>Analog Input 14</b>
	EVADC_G1CH6			<b>Analog input channel 6, group 1</b>
	EDSADC_EDS3PB			<b>Positive analog input channel 3, pin B</b>
AA11	AN15	I	D / HighZ / VDDM	<b>Analog Input 15</b>
	EVADC_G1CH7			<b>Analog input channel 7, group 1</b>
	EDSADC_EDS3NB			<b>Negative analog input channel 3, pin N</b>
AD10	AN16	I	D / HighZ / VDDM	<b>Analog Input 16</b>
	EVADC_G2CH0			<b>Analog input channel 0, group 2</b>
	EVADC_FC0CH0			<b>Analog input FC channel 0</b>
AB10	AN17/P40.10	I	S / HighZ / VDDM	<b>Analog Input 17</b>
	SENT_SENT10A			<b>Receive input channel 10</b>
	EVADC_G2CH1			<b>Analog input channel 1, group 2</b>
	EVADC_FC1CH0			<b>Analog input FC channel 1</b>

表 2-22 模拟输入 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AD9	AN18/P40.11	I	S / HighZ / VDDM	Analog Input 18
	SENT_SENT11A			Receive input channel 11
	EVADC_G11CH8			Analog input channel 8, group 11
	EVADC_G2CH2			Analog input channel 2, group 2
AD8	AN19/P40.12	I	S / HighZ / VDDM	Analog Input 19
	SENT_SENT12A			Receive input channel 12
	EVADC_G11CH9			Analog input channel 9, group 11
	EVADC_G2CH3			Analog input channel 3, group 2
AE8	AN20	I	D / HighZ / VDDM	Analog Input 20
	EVADC_G2CH4			Analog input channel 4, group 2
	EDSADC_EDS2PA			Positive analog input channel 2, pin A
AE7	AN21	I	D / HighZ / VDDM	Analog Input 21
	EVADC_G2CH5			Analog input channel 5, group 2
	EDSADC_EDS2NA			Negative analog input channel 2, pin A
AA10	AN22	I	D / HighZ / VDDM	Analog Input 22
	EVADC_G2CH6			Analog input channel 6, group 2
Y10	AN23	I	D / HighZ / VDDM	Analog Input 23
	EVADC_G2CH7			Analog input channel 7, group 2
AD7	AN24/P40.0	I	S / HighZ / VDDM	Analog Input 24
	SENT_SENT0A			Receive input channel 0
	EVADC_G3CH0			Analog input channel 0, group 3
	CCU60_CCPOS0D			Hall capture input 0
	EDSADC_EDS2PB			Positive analog input channel 2, pin B
AD6	AN25/P40.1	I	S / HighZ / VDDM	Analog Input 25
	SENT_SENT1A			Receive input channel 1
	EVADC_G3CH1			Analog input channel 1, group 3
	CCU60_CCPOS1B			Hall capture input 1
	EDSADC_EDS2NB			Negative analog input channel 2, pin B
AC7	AN26/P40.2	I	S / HighZ / VDDM	Analog Input 26
	SENT_SENT2A			Receive input channel 2
	EVADC_G3CH2			Analog input channel 2, group 3
	CCU60_CCPOS1D			Hall capture input 1
	EVADC_G11CH10			Analog input channel 10, group 11
AC6	AN27/P40.3	I	S / HighZ / VDDM	Analog Input 27
	SENT_SENT3A			Receive input channel 3
	EVADC_G3CH3			Analog input channel 3, group 3
	CCU60_CCPOS2B			Hall capture input 2
	EVADC_G11CH11			Analog input channel 11, group 11

表 2-22 模拟输入 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AB7	AN28/P40.13	I	S / HighZ / VDDM	Analog Input 28
	SENT_SENT13A			Receive input channel 13
	EVADC_G3CH4			Analog input channel 4, group 3
	EVADC_G4CH4			Analog input channel 4, group 4
AB6	AN29/P40.14	I	S / HighZ / VDDM	Analog Input 29
	SENT_SENT14A			Receive input channel 14
	EVADC_G3CH5			Analog input channel 5, group 3
	EVADC_G4CH5			Analog input channel 5, group 4
AA9	AN30	I	D / HighZ / VDDM	Analog Input 30
	EVADC_G3CH6			Analog input channel 6, group 3
	EVADC_G4CH6			Analog input channel 6, group 4
Y9	AN31	I	D / HighZ / VDDM	Analog Input 31
	EVADC_G3CH7			Analog input channel 7, group 3
	EVADC_G4CH7			Analog input channel 7, group 4
W9	AN32/P40.4	I	S / HighZ / VDDM	Analog Input 32
	SENT_SENT4A			Receive input channel 4
	EVADC_G8CH0			Analog input channel 0, group 8
	CCU60_CCPOS2D			Hall capture input 2
	EVADC_G11CH12			Analog input channel 12, group 11
Y6	AN33/P40.5	I	S / HighZ / VDDM	Analog Input 33
	SENT_SENT5A			Receive input channel 5
	EVADC_G8CH1			Analog input channel 1, group 8
	CCU61_CCPOS0D			Hall capture input 0
	EVADC_G11CH13			Analog input channel 13, group 11
W10	AN34	I	D / HighZ / VDDM	Analog Input 34
	EVADC_G8CH2			Analog input channel 2, group 8
	EVADC_G11CH14			Analog input channel 14, group 11
Y7	AN35	I	D / HighZ / VDDM	Analog Input 35
	EVADC_G8CH3			Analog input channel 3, group 8
	EVADC_G11CH15			Analog input channel 15, group 11
V9	AN36/P40.6	I	S / HighZ / VDDM	Analog Input 36
	SENT_SENT6A			Receive input channel 6
	EVADC_G8CH4			Analog input channel 4, group 8
	CCU61_CCPOS1B			Hall capture input 1
	EDSADC_EDS1PA			Positive analog input channel 1, pin A

表 2-22 模拟输入 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
W7	AN37/P40.7	I	S / HighZ / VDDM	Analog Input 37
	SENT_SENT7A			Receive input channel 7
	EVADC_G8CH5			Analog input channel 5, group 8
	CCU61_CCPOS1D			Hall capture input 1
	EDSADC_EDS1NA			Negative analog input channel 1, pin A
V10	AN38/P40.8	I	S / HighZ / VDDM	Analog Input 38
	SENT_SENT8A			Receive input channel 8
	EVADC_G8CH6			Analog input channel 6, group 8
	CCU61_CCPOS2B			Hall capture input 2
	EDSADC_EDS1PB			Positive analog input channel 1, pin B
W6	AN39/P40.9	I	S / HighZ / VDDM	Analog Input 39
	SENT_SENT9A			Receive input channel 9
	EVADC_G8CH7			Analog input channel 7, group 8
	CCU61_CCPOS2D			Hall capture input 2
	EDSADC_EDS1NB			Negative analog input channel 1, pin B
U10	AN40	I	D / HighZ / VDDM	Analog Input 40
	EVADC_G8CH8			Analog input channel 8, group 8
	EVADC_G4CH0			Analog input channel 0, group 4
U9	AN41	I	D / HighZ / VDDM	Analog Input 41
	EVADC_G8CH9			Analog input channel 9, group 8
	EVADC_G4CH1			Analog input channel 1, group 4
T10	AN42	I	D / HighZ / VDDM	Analog Input 42
	EVADC_G8CH10			Analog input channel 10, group 8
	EVADC_G4CH2			Analog input channel 2, group 4
T9	AN43	I	D / HighZ / VDDM	Analog Input 43
	EVADC_G8CH11			Analog input channel 11, group 8
	EVADC_G4CH3			Analog input channel 3, group 4
V6	AN44	I	D / HighZ / VDDM	Analog Input 44
	EVADC_G8CH12			Analog input channel 12, group 8
	EDSADC_EDS1PC			Positive analog input channel 1, pin C
V7	AN45	I	D / HighZ / VDDM	Analog Input 45
	EVADC_G8CH13			Analog input channel 13, group 8
	EDSADC_EDS1NC			Negative analog input channel 1, pin C
U6	AN46	I	D / HighZ / VDDM	Analog Input 46
	EVADC_G8CH14			Analog input channel 14, group 8
	EDSADC_EDS1PD			Positive analog input channel 1, pin D

表 2-22 模拟输入 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
U7	AN47	I	D / HighZ / VDDM	Analog Input 47
	EVADC_G8CH15			Analog input channel 15, group 8
	EDSADC_EDS1ND			Negative analog input channel 1, pin D
AK7	AN48	I	D / HighZ / VDDM	Analog Input 48
	EVADC_G5CH0			Analog input channel 0, group 5
AJ7	AN49	I	D / HighZ / VDDM	Analog Input 49
	EVADC_G5CH1			Analog input channel 1, group 5
AJ6	AN50	I	D / HighZ / VDDM	Analog Input 50
	EVADC_G5CH2			Analog input channel 2, group 5
	EDSADC_EDS9PA			Positive analog input channel 9, pin A
AK6	AN51	I	D / HighZ / VDDM	Analog Input 51
	EVADC_G5CH3			Analog input channel 3, group 5
	EDSADC_EDS9NA			Negative analog input channel 9, pin A
AJ5	AN52	I	D / HighZ / VDDM	Analog Input 52
	EVADC_G5CH4			Analog input channel 4, group 5
	EDSADC_EDS6PA			Positive analog input channel 6, pin A
AK5	AN53	I	D / HighZ / VDDM	Analog Input 53
	EVADC_G5CH5			Analog input channel 5, group 5
	EDSADC_EDS6NA			Negative analog input channel 6, pin A
AJ4	AN54/P41.4	I	S / HighZ / VDDM	Analog Input 54
	SENT_SENT20A			Receive input channel 20
	EVADC_G5CH6			Analog input channel 6, group 5
	EDSADC_EDS6PB			Positive analog input channel 6, pin B
AK4	AN55/P41.5	I	S / HighZ / VDDM	Analog Input 55
	SENT_SENT21A			Receive input channel 21
	EVADC_G5CH7			Analog input channel 7, group 5
	EDSADC_EDS6NB			Negative analog input channel 6, pin B
AF1	AN56	I	D / HighZ / VDDM	Analog Input 56
	EVADC_G6CH0			Analog input channel 0, group 6
AF2	AN57	I	D / HighZ / VDDM	Analog Input 57
	EVADC_G6CH1			Analog input channel 1, group 6
AE2	AN58	I	D / HighZ / VDDM	Analog Input 58
	EVADC_G6CH2			Analog input channel 2, group 6
	EDSADC_EDS10PA			Positive analog input channel 10, pin A
AE1	AN59	I	D / HighZ / VDDM	Analog Input 59
	EVADC_G6CH3			Analog input channel 3, group 6
	EDSADC_EDS10NA			Negative analog input channel 10, pin A

表 2-22 模拟输入 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AD1	AN60	I	D / HighZ / VDDM	<b>Analog Input 60</b>
	EVADC_G6CH4			<b>Analog input channel 4, group 6</b>
	EDSADC_EDS7PA			<b>Positive analog input channel 7, pin A</b>
AD2	AN61	I	D / HighZ / VDDM	<b>Analog Input 61</b>
	EVADC_G6CH5			<b>Analog input channel 5, group 6</b>
	EDSADC_EDS7NA			<b>Negative analog input channel 7, pin A</b>
AC2	AN62/P41.6	I	S / HighZ / VDDM	<b>Analog Input 62</b>
	SENT_SENT22A			<b>Receive input channel 22</b>
	EVADC_G6CH6			<b>Analog input channel 6, group 6</b>
	EDSADC_EDS7PB			<b>Positive analog input channel 7, pin B</b>
AC1	AN63/P41.7	I	S / HighZ / VDDM	<b>Analog Input 63</b>
	SENT_SENT23A			<b>Receive input channel 23</b>
	EVADC_G6CH7			<b>Analog input channel 7, group 6</b>
	EDSADC_EDS7NB			<b>Negative analog input channel 7, pin B</b>
AB2	AN64/P41.8	I	S / HighZ / VDDM	<b>Analog Input 64</b>
	SENT_SENT24A			<b>Receive input channel 24</b>
	EVADC_G7CH0			<b>Analog input channel 0, group 7</b>
AB1	AN65	I	D / HighZ / VDDM	<b>Analog Input 65</b>
	EVADC_G7CH1			<b>Analog input channel 1, group 7</b>
AA2	AN66	I	D / HighZ / VDDM	<b>Analog Input 66</b>
	EVADC_G7CH2			<b>Analog input channel 2, group 7</b>
	EDSADC_EDS11PA			<b>Positive analog input channel 11, pin A</b>
AA1	AN67/P40.15	I	S / HighZ / VDDM	<b>Analog Input 67</b>
	SENT_SENT15A			<b>Receive input channel 15</b>
	EVADC_G7CH3			<b>Analog input channel 3, group 7</b>
	EDSADC_EDS11NA			<b>Negative analog input channel 11, pin A</b>
Y1	AN68/P41.0	I	S / HighZ / VDDM	<b>Analog Input 68</b>
	SENT_SENT16A			<b>Receive input channel 16</b>
	EVADC_G7CH4			<b>Analog input channel 4, group 7</b>
	EDSADC_EDS8PA			<b>Positive analog input channel 8, pin A</b>
Y2	AN69/P41.1	I	S / HighZ / VDDM	<b>Analog Input 69</b>
	SENT_SENT17A			<b>Receive input channel 17</b>
	EVADC_G7CH5			<b>Analog input channel 5, group 7</b>
	EDSADC_EDS8NA			<b>Negative analog input channel 8, pin A</b>

表 2-22 模拟输入 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
W1	AN70/P41.2	I	S / HighZ / VDDM	<b>Analog Input 70</b>
	SENT_SENT18A			<b>Receive input channel 18</b>
	EVADC_G7CH6			<b>Analog input channel 6, group 7</b>
	EDSADC_EDS12PA			<b>Positive analog input channel 12, pin A</b>
	EDSADC_EDS9PB			<b>Positive analog input channel 9, pin B</b>
W2	AN71/P41.3	I	S / HighZ / VDDM	<b>Analog Input 71</b>
	SENT_SENT19A			<b>Receive input channel 19</b>
	EVADC_G7CH7			<b>Analog input channel 7, group 7</b>
	EDSADC_EDS12NA			<b>Negative analog input channel 12, pin A</b>
	EDSADC_EDS9NB			<b>Negative analog input channel 9, pin B</b>
V1	AN72	I	D / HighZ / VDDM	<b>Analog Input 72</b>
	EDSADC_EDS13PA			<b>Positive analog input channel 13, pin A</b>
V2	AN73	I	D / HighZ / VDDM	<b>Analog Input 73</b>
	EDSADC_EDS13NA			<b>Negative analog input channel 13, pin A</b>

注释：端口引脚P32.0和P32.1是双向引脚，具有以下两个功能：

1. 如果将这些引脚用作标准GPIO，则可以使用P32.0和P32.1引脚配置表中定义的功能。
2. 如果引脚用作外部MOSFET的预驱动器（内部DCDC情况），P32.0和P32.1将充当名为VGATE1N和VGATE1P的模拟IO。

表 2-23 系统 I/O

Ball	Symbol	Ctrl.	Buffer Type	Function
T12	AGBTCLKN (VSS)	I	AGBT_C LK / VEXT	<b>Input PAD (negative pole) for the external 100 MHz differential clock.</b> AGBT Input; (TC3xx devices without AGBT: VSS)
R12	AGBTCLKP (VSS)	I	AGBT_C LK / VEXT	<b>Input PAD (positive pole) for the external 100 MHz differential clock.</b> AGBT Input; (TC3xx devices without AGBT: VSS)
W15	AGBTTXN (VSS)	O	AGBT_T X / VEXT	<b>Off-chip driver output PAD of the 2.5Gbps transmitter, negative pole</b> AGBT Output; (TC3xx devices without AGBT: VSS)
W16	AGBTTXP (VSS)	O	AGBT_T X / VEXT	<b>Off-chip driver output PAD of the 2.5Gbps transmitter, positive pole</b> AGBT Output; (TC3xx devices without AGBT: VSS)
T19	AGBTERR (VSS)	I	FAST / PD / VEXT	<b>Input PAD for CRC error from FPGA.</b> AGBT Input; (TC3xx devices without AGBT: VSS)

表 2-23 系统 I/O (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AD22	VGATE1P	O	—	<b>DCDC P ch. MOSFET gate driver output</b> P32.1 / External Pass Device gate control for EVRC
AE22	VGATE1N	O	—	<b>DCDC N ch. MOSFET gate driver output</b> P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
U25	XTAL1	I	XTAL / VEXT	<b>XTAL pad1</b> XTAL1. Main Oscillator/PLL/Clock Generator Input.
U24	XTAL2	O	XTAL / VEXT	<b>XTAL pad2</b> XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT
R19	DAPE0	I	FAST / PD2 / VEXT	<b>DAPE: DAPE0 Clock Input</b> DAPE: DAPE0 clock input (PD Devices: NC)
T24	TRST	I	FAST /	<b>JTAG Module Reset/Enable Input</b>
	DAPE0	I	PU2 / VEXT	<b>DAPE: DAPE0 Clock Input</b>
R21	TMS	I	FAST /	<b>JTAG Module State Machine Control Input</b>
	DAP1	I/O	PD2 / VEXT	<b>DAP: DAP1 Data I/O</b>
P21	TCK	I	FAST /	<b>JTAG Module Clock Input</b>
	DAP0	I	PD2 / VEXT	<b>DAP: DAP0 Clock Input</b>
M16	DAPE1	I/O	FAST / PD2 / VEXT	<b>DAPE: DAPE1 Data I/O</b> DAPE: DAPE1 Data I/O (PD Devices: VSS)
M15	DAPE2	I/O	FAST / PD2 / VEXT	<b>DAPE: DAPE2 Data I/O</b> DAPE: DAPE2 Data I/O (PD Devices: VSS)
M21	ESR1	I/O	FAST / PU1 / VEXT	<b>ESR1 Port Pin input - can be used to trigger a reset or an NMI</b> ESR1: External System Request Reset 1. Default NMI function. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter 'Reset Control Unit' and SCU_IOCR register description. PMS_EVRWUP: EVR Wakeup Pin
	PMS_ESR1WKP	I		<b>ESR1 pin input</b>

表 2-23 系统 I/O (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
L21	ESR0	I/O	FAST / OD / VEXT	<b>ESR0 Port Pin input - can be used to trigger a reset or an NMI</b> ESR0: External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter 'Reset Control Unit' and SCU_IOCRR register description. PMS_EVRWUP: EVR Wakeup Pin
	PMS_ESR0WKP	I		<b>ESR0 pin input</b>
M22	PORST	I/O	PORST / PD / VEXT	<b>PORST pin</b> Power On Reset Input. Additional strong PD in case of power fail.

表 2-24 供电

Ball	Symbol	Ctrl.	Buffer Type	Function
N19, V19, M18, W18, W13, V12, J21, K20	VDD	I	—	<b>Digital Core Power Supply (1.25V)</b>
AJ30, AH29, AD25, AC24, G8, F7, B3, A2	VEXT	I	—	<b>External Power Supply (5V / 3.3V)</b>
J10	VFLEX	I	—	<b>Digital Power Supply for Flex Port Pads (5V / 3.3V)</b>
AE10, AJ9, AK9	VDDM	I	—	<b>ADC Analog Power Supply (5V / 3.3V)</b>
A29, B28, F24, G23	VDDP3	I	—	<b>Flash Power Supply (3.3V)</b>
AK30, AJ29, AE25, AD24, AB22, AA21, K10, J9, G7, B2, A30, B30, B29, F25, G24, J22, K21	VSS	I	—	<b>Digital Ground</b>
AE9, AJ8, AK8	VSSM	I	—	<b>Analog Ground for VDDM</b>

表 2-24 供电 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
P19, U19, P18, R18, T18, U18, M17, N17, R17, T17, V17, W17, N16, P16, R16, T16, U16, V16, N15, P15, R15, T15, U15, V15, M14, N14, R14, T14, V14, W14, P13, R13, T13, U13, P12, U12	VSS	I	—	<b>Digital Ground</b>
T25	VSS	I	—	<b>Oscillator Ground, VSS(OSC)</b>
AE11	VAREF1	I	—	<b>Positive Analog Reference Voltage 1</b>
AE12	VAGND1	I	—	<b>Negative Analog Reference Voltage 1</b>
AA6	VAREF2	I	—	<b>Positive Analog Reference Voltage 2</b>
AA7	VAGND2	I	—	<b>Negative Analog Reference Voltage 2</b>
C30, D30, E30, F30, G30, W30, C29, D29, E29, F29, G29, A28, A27, B27, A26, B26, A25, A21, AJ20, B21, B20, A17, B17, A10, B10, A9, B9, A8, A4, B4, A3, AJ3, AK3, C2, D2, E2, H2, R2, AH2, AJ2, AK2, B1, C1, D1, E1, H1, J1, R1, T1, AH1, AJ1, B6, B14, B25	NC	I	—	<b>Not connected. These pins are reserved for future extensions and shall not be connected externally</b>

表 2-24 供电 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
AB9, F6, AE6, A1, AK1, V30, V29	NC1		—	<b>Not connected. These pins are not connected on package level and will not be used for future extensions</b>
H30, H29, AJ10, AK10	VSS		—	<b>Digital Ground for EBU</b>
N12, M13	VDDSB (VDD)		—	<b>Devices with integrated EMEM: EMEM SRAM Standby Power Supply, VDDSB (1.25V); Devices without integrated EMEM: VDD (1.25V)</b>
J29, J30, AH30, AK29, AK20, AJ11, AK11	VEBU		—	<b>Digital Power Supply for EBU (5V / 3.3V)</b>
AA16	VEVRSB		—	<b>Standby Power Supply (5V / 3.3V) for the Standby SRAM</b>
V24	VDD		—	<b>Digital Power Supply for Oscillator (1.25V), VDD(OSC)</b>
V25	VEXT		—	<b>Digital Power Supply for Oscillator (shall be supplied with same level as used for VEXT), VEXT(OSC)</b>
AG1	VAREF3		—	<b>Positive Analog Reference Voltage 3</b>
AG2	VAGND3		—	<b>Negative Analog Reference Voltage 3</b>

## 2.2 LFBGA-292 封装变体引脚配置

表 2-25 端口 P00 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
G1	P00.0	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM5_IN4_10			<b>Mux input channel 4 of TIM module 5</b>
	GTM_TIM3_IN0_1			<b>Mux input channel 0 of TIM module 3</b>
	GTM_TIM2_IN0_1			<b>Mux input channel 0 of TIM module 2</b>
	CCU61_CTRAPA			<b>Trap input capture</b>
	CCU60_T12HRE			<b>External timer start 12</b>
	MSC0_INJ0			<b>Injection signal from port</b>
	GETH_MDIOA			<b>MDIO Input</b>
	P00.0			O0
	GTM_TOUT9	O1	<b>GTM muxed output</b>	
	IOM_REF0_9		<b>Reference input 0</b>	
	ASCLIN3_ASCLK	O2	<b>Shift clock output</b>	
	ASCLIN3_ATX	O3	<b>Transmit output</b>	
	IOM_MON2_15		<b>Monitor input 2</b>	
	IOM_REF2_15		<b>Reference input 2</b>	
	—	O4	<b>Reserved</b>	
	CAN10_TXD	O5	<b>CAN transmit output node 0</b>	
	—	O6	<b>Reserved</b>	
	CCU60_COUT63	O7	<b>T13 PWM channel 63</b>	
	IOM_MON1_6		<b>Monitor input 1</b>	
IOM_REF1_0	<b>Reference input 1</b>			
GETH_MDIO	O	<b>MDIO Output</b>		

表 2-25 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
G2	P00.1	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM5_IN5_11			<b>Mux input channel 5 of TIM module 5</b>
	GTM_TIM3_IN1_1			<b>Mux input channel 1 of TIM module 3</b>
	GTM_TIM2_IN1_1			<b>Mux input channel 1 of TIM module 2</b>
	CCU60_CC60INB			<b>T12 capture input 60</b>
	ASCLIN3_ARXE			<b>Receive input</b>
	EDSADC_DSCIN5A			<b>Modulator clock input, channel 5</b>
	CAN10_RXDA			<b>CAN receive input node 0</b>
	PSI5_RX0A			<b>RXD inputs (receive data) channel 0</b>
	CCU61_CC60INA			<b>T12 capture input 60</b>
	SENT_SENT0B			<b>Receive input channel 0</b>
	EDSADC_DSCIN7B			<b>Modulator clock input, channel 7</b>
	EVADC_G9CH11			AI
	EDSADC_EDS5NA	<b>Negative analog input channel 5, pin A</b>		
	P00.1	O0	<b>General-purpose output</b>	
	GTM_TOUT10	O1	<b>GTM muxed output</b>	
	IOM_REF0_10	O2	<b>Reference input 0</b>	
	ASCLIN3_ATX		<b>Transmit output</b>	
	IOM_MON2_15		<b>Monitor input 2</b>	
	IOM_REF2_15	O3	<b>Reference input 2</b>	
	—		<b>Reserved</b>	
	EDSADC_DSCOUT5	O4	<b>Modulator clock output</b>	
	EDSADC_DSCOUT7	O5	<b>Modulator clock output</b>	
	SENT_SPC0	O6	<b>Transmit output</b>	
	CCU61_CC60	O7	<b>T12 PWM channel 60</b>	
	IOM_MON1_8		<b>Monitor input 1</b>	
IOM_REF1_13	<b>Reference input 1</b>			

表 2-25 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
H1	P00.2	I	SLOW / PU1 / VEXT / ES1	<b>General-purpose input</b>
	GTM_TIM5_IN6_11			<b>Mux input channel 6 of TIM module 5</b>
	GTM_TIM3_IN1_2			<b>Mux input channel 1 of TIM module 3</b>
	GTM_TIM2_IN1_2			<b>Mux input channel 1 of TIM module 2</b>
	EDSADC_DSDIN7B			<b>Digital datastream input, channel 7</b>
	EDSADC_DSDIN5A			<b>Digital datastream input, channel 5</b>
	SENT_SENT1B			<b>Receive input channel 1</b>
	EVADC_G9CH10	AI	<b>Analog input channel 10, group 9</b>	
	EDSADC_EDS5PA		<b>Positive analog input channel 5, pin A</b>	
	P00.2	O0	<b>General-purpose output</b>	
	GTM_TOUT11	O1	<b>GTM muxed output</b>	
	IOM_REF0_11		<b>Reference input 0</b>	
	ASCLIN3_ASCLK	O2	<b>Shift clock output</b>	
	CAN21_TXD	O3	<b>CAN transmit output node 1</b>	
	PSI5_TX0	O4	<b>TXD outputs (send data)</b>	
	IOM_MON1_14		<b>Monitor input 1</b>	
	IOM_REF1_14		<b>Reference input 1</b>	
	CAN03_TXD	O5	<b>CAN transmit output node 3</b>	
	IOM_MON2_8		<b>Monitor input 2</b>	
	IOM_REF2_8		<b>Reference input 2</b>	
	QSPI3_SLSO4	O6	<b>Master slave select output</b>	
	CCU61_COUT60	O7	<b>T12 PWM channel 60</b>	
	IOM_MON1_11		<b>Monitor input 1</b>	
	IOM_REF1_10		<b>Reference input 1</b>	

表 2-25 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
H2	P00.3	I	SLOW / PU1 / VEXT / ES1	<b>General-purpose input</b>	
	GTM_TIM5_IN7_10			<b>Mux input channel 7 of TIM module 5</b>	
	GTM_TIM3_IN2_1			<b>Mux input channel 2 of TIM module 3</b>	
	GTM_TIM2_IN2_1			<b>Mux input channel 2 of TIM module 2</b>	
	CCU60_CC61INB			<b>T12 capture input 61</b>	
	EDSADC_DSCIN3A			<b>Modulator clock input, channel 3</b>	
	EDSADC_ITR5F			<b>Trigger/Gate input, channel 5</b>	
	PSI5_RX1A			<b>RXD inputs (receive data) channel 1</b>	
	CAN03_RXDA			<b>CAN receive input node 3</b>	
	CAN21_RXDA			<b>CAN receive input node 1</b>	
	PSI5S_RXA			<b>RX data input</b>	
	SENT_SENT2B			<b>Receive input channel 2</b>	
	CCU61_CC61INA			<b>T12 capture input 61</b>	
	EVADC_G9CH9			AI	<b>Analog input channel 9, group 9</b>
	EDSADC_EDS5NB				<b>Negative analog input channel 5, pin B</b>
	P00.3	O0	<b>General-purpose output</b>		
	GTM_TOUT12	O1	<b>GTM muxed output</b>		
	IOM_REF0_12		<b>Reference input 0</b>		
	ASCLIN3_ASLSO	O2	<b>Slave select signal output</b>		
	—	O3	<b>Reserved</b>		
	EDSADC_DSCOUT3	O4	<b>Modulator clock output</b>		
	—	O5	<b>Reserved</b>		
	SENT_SPC2	O6	<b>Transmit output</b>		
	CCU61_CC61	O7	<b>T12 PWM channel 61</b>		
	IOM_MON1_9		<b>Monitor input 1</b>		
	IOM_REF1_12		<b>Reference input 1</b>		

表 2-25 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
J1	P00.4	I	SLOW / PU1 / VEXT / ES1	<b>General-purpose input</b>	
	GTM_TIM6_IN4_1			<b>Mux input channel 4 of TIM module 6</b>	
	GTM_TIM3_IN3_1			<b>Mux input channel 3 of TIM module 3</b>	
	GTM_TIM2_IN3_1			<b>Mux input channel 3 of TIM module 2</b>	
	SCU_E_REQ2_2			<b>ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>	
	SENT_SENT3B			<b>Receive input channel 3</b>	
	EDSADC_DSDIN3A			<b>Digital datastream input, channel 3</b>	
	EDSADC_SGNA			<b>Carrier sign signal input</b>	
	ASCLIN10_ARXA			<b>Receive input</b>	
	GTM_DTMA5_0			<b>CDTM5_DTM4</b>	
	GTM_DTMT3_0			<b>CDTM3_DTM0</b>	
	EVADC_G9CH8			AI	<b>Analog input channel 8, group 9</b>
	EDSADC_EDS5PB				<b>Positive analog input channel 5, pin B</b>
	P00.4	O0	<b>General-purpose output</b>		
	GTM_TOUT13	O1	<b>GTM muxed output</b>		
	IOM_REF0_13		<b>Reference input 0</b>		
	PSI5S_TX	O2	<b>TX data output</b>		
	CAN11_TXD	O3	<b>CAN transmit output node 1</b>		
	PSI5_TX1	O4	<b>TXD outputs (send data)</b>		
	IOM_MON1_15		<b>Monitor input 1</b>		
	EVADC_FC4BFLOUT	O5	<b>Boundary flag output, FC channel 4</b>		
	SENT_SPC3	O6	<b>Transmit output</b>		
	CCU61_COUT61	O7	<b>T12 PWM channel 61</b>		
IOM_MON1_12	<b>Monitor input 1</b>				
IOM_REF1_9	<b>Reference input 1</b>				

表 2-25 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
J2	P00.5	I	SLOW / PU1 / VEXT / ES1	<b>General-purpose input</b>
	GTM_TIM3_IN4_1			<b>Mux input channel 4 of TIM module 3</b>
	GTM_TIM3_IN0_11			<b>Mux input channel 0 of TIM module 3</b>
	GTM_TIM2_IN4_1			<b>Mux input channel 4 of TIM module 2</b>
	CCU60_CC62INB			<b>T12 capture input 62</b>
	EDSADC_DSCIN2A			<b>Modulator clock input, channel 2</b>
	PSI5_RX2A			<b>RXD inputs (receive data) channel 2</b>
	CCU61_CC62INA			<b>T12 capture input 62</b>
	SENT_SENT4B			<b>Receive input channel 4</b>
	CAN11_RXDB			<b>CAN receive input node 1</b>
	GTM_DTMT1_1			<b>CDTM1_DTM0</b>
	GTM_DTMT4_2			<b>CDTM4_DTM0</b>
	EVADC_G9CH7			AI
	P00.5	O0	<b>General-purpose output</b>	
	GTM_TOUT14	O1	<b>GTM muxed output</b>	
	IOM_REF0_14		<b>Reference input 0</b>	
	EDSADC_CGPWMN	O2	<b>Negative carrier generator output</b>	
	QSPI3_SLSO3	O3	<b>Master slave select output</b>	
	EDSADC_DSCOUT2	O4	<b>Modulator clock output</b>	
	EVADC_FC0BFLOUT	O5	<b>Boundary flag output, FC channel 0</b>	
	SENT_SPC4	O6	<b>Transmit output</b>	
	CCU61_CC62	O7	<b>T12 PWM channel 62</b>	
	IOM_MON1_10		<b>Monitor input 1</b>	
IOM_REF1_11		<b>Reference input 1</b>		

表 2-25 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
J4	P00.6	I	SLOW / PU1 / VEXT / ES1	<b>General-purpose input</b>
	GTM_TIM3_IN5_1			<b>Mux input channel 5 of TIM module 3</b>
	GTM_TIM3_IN1_14			<b>Mux input channel 1 of TIM module 3</b>
	GTM_TIM2_IN5_1			<b>Mux input channel 5 of TIM module 2</b>
	EDSADC_ITR4F			<b>Trigger/Gate input, channel 4</b>
	EDSADC_DSDIN2A			<b>Digital datastream input, channel 2</b>
	SENT_SENT5B			<b>Receive input channel 5</b>
	ASCLIN5_ARXA			<b>Receive input</b>
	GTM_DTMA6_0			<b>CDTM6_DTM4</b>
	GTM_DTMT3_1			<b>CDTM3_DTM0</b>
	EVADC_G9CH6	AI	<b>Analog input channel 6, group 9</b>	
	P00.6	O0	<b>General-purpose output</b>	
	GTM_TOUT15	O1	<b>GTM muxed output</b>	
	IOM_REF0_15		<b>Reference input 0</b>	
	EDSADC_CGPWMP	O2	<b>Positive carrier generator output</b>	
	EVADC_FC5BFLOUT	O3	<b>Boundary flag output, FC channel 5</b>	
	PSI5_TX2	O4	<b>TXD outputs (send data)</b>	
	IOM_REF1_15		<b>Reference input 1</b>	
	EVADC_EMUX10	O5	<b>Control of external analog multiplexer interface 1</b>	
	SENT_SPC5	O6	<b>Transmit output</b>	
	CCU61_COUT62	O7	<b>T12 PWM channel 62</b>	
	IOM_MON1_13		<b>Monitor input 1</b>	
	IOM_REF1_8		<b>Reference input 1</b>	

表 2-25 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
K1	P00.7	I	SLOW / PU1 / VEXT / ES1	<b>General-purpose input</b>
	GTM_TIM3_IN6_1			<b>Mux input channel 6 of TIM module 3</b>
	GTM_TIM3_IN2_11			<b>Mux input channel 2 of TIM module 3</b>
	GTM_TIM2_IN6_1			<b>Mux input channel 6 of TIM module 2</b>
	CCU61_CC60INC			<b>T12 capture input 60</b>
	SENT_SENT6B			<b>Receive input channel 6</b>
	EDSADC_DSCIN4A			<b>Modulator clock input, channel 4</b>
	GPT120_T2INA			<b>Trigger/gate input of timer T2</b>
	CCU61_CCPOS0A			<b>Hall capture input 0</b>
	CCU60_T12HRB			<b>External timer start 12</b>
	GTM_DTMT0_2			<b>CDTM0_DTM0</b>
	EVADC_G9CH5	AI	<b>Analog input channel 5, group 9</b>	
	EDSADC_EDS4NA		<b>Negative analog input channel 4, pin A</b>	
	P00.7	O0	<b>General-purpose output</b>	
	GTM_TOUT16	O1	<b>GTM muxed output</b>	
	ASCLIN5_ATX	O2	<b>Transmit output</b>	
	EVADC_FC2BFLOUT	O3	<b>Boundary flag output, FC channel 2</b>	
	EDSADC_DSCOUT4	O4	<b>Modulator clock output</b>	
	EVADC_EMUX11	O5	<b>Control of external analog multiplexer interface 1</b>	
	SENT_SPC6	O6	<b>Transmit output</b>	
	CCU61_CC60	O7	<b>T12 PWM channel 60</b>	
	IOM_MON1_8		<b>Monitor input 1</b>	
	IOM_REF1_13		<b>Reference input 1</b>	

表 2-25 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
K4	P00.8	I	SLOW / PU1 / VEXT / ES1	<b>General-purpose input</b>
	GTM_TIM3_IN7_1			<b>Mux input channel 7 of TIM module 3</b>
	GTM_TIM3_IN3_11			<b>Mux input channel 3 of TIM module 3</b>
	GTM_TIM2_IN7_1			<b>Mux input channel 7 of TIM module 2</b>
	CCU61_CC61INC			<b>T12 capture input 61</b>
	SENT_SENT7B			<b>Receive input channel 7</b>
	EDSADC_DSDIN4A			<b>Digital datastream input, channel 4</b>
	GPT120_T2EUDA			<b>Count direction control input of timer T2</b>
	CCU61_CCPOS1A			<b>Hall capture input 1</b>
	CCU60_T13HRB			<b>External timer start 13</b>
	ASCLIN10_ARXB			<b>Receive input</b>
	EVADC_G9CH4			AI
	EDSADC_EDS4PA		<b>Positive analog input channel 4, pin A</b>	
	P00.8	O0	<b>General-purpose output</b>	
	GTM_TOUT17	O1	<b>GTM muxed output</b>	
	QSPI3_SLSO6	O2	<b>Master slave select output</b>	
	ASCLIN10_ATX	O3	<b>Transmit output</b>	
	—	O4	<b>Reserved</b>	
	EVADC_EMUX12	O5	<b>Control of external analog multiplexer interface 1</b>	
	SENT_SPC7	O6	<b>Transmit output</b>	
	CCU61_CC61	O7	<b>T12 PWM channel 61</b>	
	IOM_MON1_9		<b>Monitor input 1</b>	
	IOM_REF1_12		<b>Reference input 1</b>	

表 2-25 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
K2	P00.9	I	SLOW / PU1 / VEXT / ES1	<b>General-purpose input</b>
	GTM_TIM4_IN0_7			<b>Mux input channel 0 of TIM module 4</b>
	GTM_TIM1_IN0_1			<b>Mux input channel 0 of TIM module 1</b>
	GTM_TIM0_IN0_1			<b>Mux input channel 0 of TIM module 0</b>
	CCU61_CC62INC			<b>T12 capture input 62</b>
	SENT_SENT8B			<b>Receive input channel 8</b>
	CCU61_CCPOS2A			<b>Hall capture input 2</b>
	EDSADC_DSCIN1A			<b>Modulator clock input, channel 1</b>
	EDSADC_ITR3F			<b>Trigger/Gate input, channel 3</b>
	GPT120_T4EUDA			<b>Count direction control input of timer T4</b>
	CCU60_T13HRC			<b>External timer start 13</b>
	CCU60_T12HRC			<b>External timer start 12</b>
	EVADC_G9CH3			AI
	EDSADC_EDS4NB	<b>Negative analog input channel 4, pin B</b>		
	P00.9	O0	<b>General-purpose output</b>	
	GTM_TOUT18	O1	<b>GTM muxed output</b>	
	QSPI3_SLSO7	O2	<b>Master slave select output</b>	
	ASCLIN3_ARTS	O3	<b>Ready to send output</b>	
	EDSADC_DSCOUT1	O4	<b>Modulator clock output</b>	
	ASCLIN4_ATX	O5	<b>Transmit output</b>	
	SENT_SPC8	O6	<b>Transmit output</b>	
	CCU61_CC62	O7	<b>T12 PWM channel 62</b>	
	IOM_MON1_10		<b>Monitor input 1</b>	
IOM_REF1_11	<b>Reference input 1</b>			

表 2-25 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
K5	P00.10	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM4_IN1_11			Mux input channel 1 of TIM module 4
	GTM_TIM1_IN1_1			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_1			Mux input channel 1 of TIM module 0
	SENT_SENT9B			Receive input channel 9
	EDSADC_DSDIN1A			Digital datastream input, channel 1
	EVADC_G9CH2			Analog input channel 2, group 9
	EDSADC_EDS4PB	AI	Positive analog input channel 4, pin B	
	P00.10		O0	General-purpose output
	GTM_TOUT19	O1	GTM muxed output	
	ASCLIN4_ASCLK	O2	Shift clock output	
	—	O3	Reserved	
	—	O4	Reserved	
	—	O5	Reserved	
	SENT_SPC9	O6	Transmit output	
	CCU61_COUT63	O7	T13 PWM channel 63	
	IOM_MON1_7		Monitor input 1	
IOM_REF1_7	Reference input 1			
L1	P00.11	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM4_IN2_11			Mux input channel 2 of TIM module 4
	GTM_TIM1_IN2_1			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_1			Mux input channel 2 of TIM module 0
	CCU60_CTRAPA			Trap input capture
	EDSADC_DSCIN0A			Modulator clock input, channel 0
	CCU61_T12HRE			External timer start 12
	SENT_SENT10B	Receive input channel 10		
	EVADC_G9CH1	AI	Analog input channel 1, group 9	
	EVADC_FC3CH0		Analog input FC channel 3	
	P00.11	O0	General-purpose output	
	GTM_TOUT20	O1	GTM muxed output	
	ASCLIN4_ASLSO	O2	Slave select signal output	
	—	O3	Reserved	
	EDSADC_DSCOUT0	O4	Modulator clock output	
	—	O5	Reserved	
	—	O6	Reserved	
—	O7	Reserved		

表 2-25 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
L2	P00.12	I	SLOW / PU1 / VEXT / ES1	<b>General-purpose input</b>
	GTM_TIM4_IN3_11			<b>Mux input channel 3 of TIM module 4</b>
	GTM_TIM1_IN3_1			<b>Mux input channel 3 of TIM module 1</b>
	GTM_TIM0_IN3_1			<b>Mux input channel 3 of TIM module 0</b>
	ASCLIN3_ACTSA			<b>Clear to send input</b>
	EDSADC_DSDIN0A			<b>Digital datastream input, channel 0</b>
	ASCLIN4_ARXA			<b>Receive input</b>
	SENT_SENT11B			<b>Receive input channel 11</b>
	EVADC_G9CH0			Ai
	EVADC_FC2CH0		<b>Analog input FC channel 2</b>	
	P00.12	O0	<b>General-purpose output</b>	
	GTM_TOUT21	O1	<b>GTM muxed output</b>	
	—	O2	<b>Reserved</b>	
	—	O3	<b>Reserved</b>	
	—	O4	<b>Reserved</b>	
	—	O5	<b>Reserved</b>	
	—	O6	<b>Reserved</b>	
	CCU61_COUT63	O7	<b>T13 PWM channel 63</b>	
	IOM_MON1_7		<b>Monitor input 1</b>	
	IOM_REF1_7		<b>Reference input 1</b>	

表 2-26 端口 P01 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
G5	P01.3	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN5_2			Mux input channel 5 of TIM module 4
	GTM_TIM2_IN0_14			Mux input channel 0 of TIM module 2
	GTM_TIM0_IN5_8			Mux input channel 5 of TIM module 0
	QSPI3_SLSIB			Slave select input
	EDSADC_ITR7F			Trigger/Gate input, channel 7
	EVADC_G9CH14	AI	Analog input channel 14, group 9	
	P01.3	O0	General-purpose output	
	GTM_TOUT111	O1	GTM muxed output	
	—	O2	Reserved	
	—	O3	Reserved	
	QSPI3_SLSO9	O4	Master slave select output	
	CAN01_TXD	O5	CAN transmit output node 1	
	IOM_MON2_6		Monitor input 2	
	IOM_REF2_6		Reference input 2	
	—	O6	Reserved	
	—	O7	Reserved	
G4	P01.4	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN6_2			Mux input channel 6 of TIM module 4
	GTM_TIM2_IN1_14			Mux input channel 1 of TIM module 2
	GTM_TIM0_IN6_8			Mux input channel 6 of TIM module 0
	CAN01_RXDC			CAN receive input node 1
	EDSADC_ITR7E			Trigger/Gate input, channel 7
	EVADC_G9CH13	AI	Analog input channel 13, group 9	
	P01.4	O0	General-purpose output	
	GTM_TOUT112	O1	GTM muxed output	
	—	O2	Reserved	
	ASCLIN9_ASLSO	O3	Slave select signal output	
	QSPI3_SLSO10	O4	Master slave select output	
	—	O5	Reserved	
	—	O6	Reserved	
	—	O7	Reserved	

表 2-26 端口 P01 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
H5	P01.5	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN3_2			Mux input channel 3 of TIM module 5
	GTM_TIM2_IN3_7			Mux input channel 3 of TIM module 2
	GTM_TIM2_IN2_7			Mux input channel 2 of TIM module 2
	QSPI3_MRSTC			Master SPI data input
	EDSADC_DSCIN8A			Modulator clock input, channel 8
	ASCLIN9_ARXA			Receive input
	EVADC_G9CH12	AI	Analog input channel 12, group 9	
	P01.5	O0	General-purpose output	
	GTM_TOUT113	O1	GTM muxed output	
	—	O2	Reserved	
	—	O3	Reserved	
	QSPI3_MRST	O4	Slave SPI data output	
	IOM_MON2_3		Monitor input 2	
	IOM_REF2_3		Reference input 2	
	—	O5	Reserved	
	EDSADC_DSCOUT8	O6	Modulator clock output	
—	O7	Reserved		
H4	P01.6	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN6_2			Mux input channel 6 of TIM module 5
	GTM_TIM5_IN5_3			Mux input channel 5 of TIM module 5
	GTM_TIM2_IN5_7			Mux input channel 5 of TIM module 2
	QSPI3_MTSRC			Slave SPI data input
	EDSADC_DSDIN8A			Digital datastream input, channel 8
	P01.6	O0	General-purpose output	
	GTM_TOUT114	O1	GTM muxed output	
	—	O2	Reserved	
	ASCLIN9_ASCLK	O3	Shift clock output	
	QSPI3_MTSR	O4	Master SPI data output	
	—	O5	Reserved	
	—	O6	Reserved	
	—	O7	Reserved	

表 2-26 端口 P01 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
J5	P01.7	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM5_IN7_2			<b>Mux input channel 7 of TIM module 5</b>
	GTM_TIM2_IN7_7			<b>Mux input channel 7 of TIM module 2</b>
	QSPI3_SCLKC			<b>Slave SPI clock inputs</b>
	EDSADC_ITR8F			<b>Trigger/Gate input, channel 8</b>
	ASCLIN9_ARXB			<b>Receive input</b>
	P01.7	O0		<b>General-purpose output</b>
	GTM_TOUT115	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	ASCLIN9_ATX	O3		<b>Transmit output</b>
	QSPI3_SCLK	O4		<b>Master SPI clock output</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>

表 2-27 端口 P02 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
B1	P02.0	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN0_2			<b>Mux input channel 0 of TIM module 1</b>
	GTM_TIM0_IN0_2			<b>Mux input channel 0 of TIM module 0</b>
	CCU61_CC60INB			<b>T12 capture input 60</b>
	ASCLIN2_ARXG			<b>Receive input</b>
	CCU60_CC60INA			<b>T12 capture input 60</b>
	SCU_E_REQ3_2			<b>ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	GTM_DTMA0_0			<b>CDTM0_DTM4</b>
	P02.0			O0
	GTM_TOUT0	O1	<b>GTM muxed output</b>	
	IOM_REF0_0		<b>Reference input 0</b>	
	ASCLIN2_ATX	O2	<b>Transmit output</b>	
	IOM_MON2_14		<b>Monitor input 2</b>	
	IOM_REF2_14		<b>Reference input 2</b>	
	QSPI3_SLSO1	O3	<b>Master slave select output</b>	
	EDSADC_CGPWMN	O4	<b>Negative carrier generator output</b>	
	CAN00_TXD	O5	<b>CAN transmit output node 0</b>	
	IOM_MON2_5		<b>Monitor input 2</b>	
	IOM_REF2_5		<b>Reference input 2</b>	
	ERAY0_TXDA	O6	<b>Transmit Channel A</b>	
	CCU60_CC60	O7	<b>T12 PWM channel 60</b>	
	IOM_MON1_2		<b>Monitor input 1</b>	
	IOM_REF1_6		<b>Reference input 1</b>	

表 2-27 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
C2	P02.1	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN1_2			<b>Mux input channel 1 of TIM module 1</b>
	GTM_TIM0_IN1_2			<b>Mux input channel 1 of TIM module 0</b>
	ERAY0_RXDA2			<b>Receive Channel A2</b>
	ASCLIN2_ARXB			<b>Receive input</b>
	CAN00_RXDA			<b>CAN receive input node 0</b>
	SCU_E_REQ2_1			<b>ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	P02.1	O0	<b>General-purpose output</b>	
	GTM_TOUT1	O1	<b>GTM muxed output</b>	
	IOM_REF0_1		<b>Reference input 0</b>	
	QSPI4_SLSO7	O2	<b>Master slave select output</b>	
	QSPI3_SLSO2	O3	<b>Master slave select output</b>	
	EDSADC_CGPWMP	O4	<b>Positive carrier generator output</b>	
	—	O5	<b>Reserved</b>	
	—	O6	<b>Reserved</b>	
	CCU60_COUT60	O7	<b>T12 PWM channel 60</b>	
	IOM_MON1_3		<b>Monitor input 1</b>	
	IOM_REF1_3		<b>Reference input 1</b>	

表 2-27 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
C1	P02.2	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN2_2			<b>Mux input channel 2 of TIM module 1</b>
	GTM_TIM0_IN2_2			<b>Mux input channel 2 of TIM module 0</b>
	CCU61_CC61INB			<b>T12 capture input 61</b>
	CCU60_CC61INA			<b>T12 capture input 61</b>
	SENT_SENT14B			<b>Receive input channel 14</b>
	P02.2	O0		<b>General-purpose output</b>
	GTM_TOUT2	O1		<b>GTM muxed output</b>
	IOM_REF0_2	O2		<b>Reference input 0</b>
	ASCLIN1_ATX			<b>Transmit output</b>
	IOM_MON2_13			<b>Monitor input 2</b>
	IOM_REF2_13	O3		<b>Reference input 2</b>
	QSPI3_SLSO3			<b>Master slave select output</b>
	PSI5_TX0	O4		<b>TXD outputs (send data)</b>
	IOM_MON1_14	O5		<b>Monitor input 1</b>
	IOM_REF1_14			<b>Reference input 1</b>
	CAN02_TXD			<b>CAN transmit output node 2</b>
	IOM_MON2_7	O6		<b>Monitor input 2</b>
	IOM_REF2_7			<b>Reference input 2</b>
	ERAY0_TXDB	O7		<b>Transmit Channel B</b>
	CCU60_CC61	O7		<b>T12 PWM channel 61</b>
	IOM_MON1_1			<b>Monitor input 1</b>
	IOM_REF1_5			<b>Reference input 1</b>

表 2-27 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
D2	P02.3	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN3_2			<b>Mux input channel 3 of TIM module 1</b>
	GTM_TIM0_IN3_2			<b>Mux input channel 3 of TIM module 0</b>
	EDSADC_DSCIN5B			<b>Modulator clock input, channel 5</b>
	ERAY0_RXDB2			<b>Receive Channel B2</b>
	CAN02_RXDB			<b>CAN receive input node 2</b>
	ASCLIN1_ARXG			<b>Receive input</b>
	MSC1_SDI1			<b>Upstream asynchronous input signal</b>
	PSI5_RX0B			<b>RXD inputs (receive data) channel 0</b>
	SENT_SENT13B			<b>Receive input channel 13</b>
	P02.3	O0	<b>General-purpose output</b>	
	GTM_TOUT3	O1	<b>GTM muxed output</b>	
	IOM_REF0_3		<b>Reference input 0</b>	
	ASCLIN2_ASLSO	O2	<b>Slave select signal output</b>	
	QSPI3_SLSO4	O3	<b>Master slave select output</b>	
	EDSADC_DSCOUT5	O4	<b>Modulator clock output</b>	
	—	O5	<b>Reserved</b>	
	—	O6	<b>Reserved</b>	
	CCU60_COUT61	O7	<b>T12 PWM channel 61</b>	
	IOM_MON1_4		<b>Monitor input 1</b>	
IOM_REF1_2	<b>Reference input 1</b>			

表 2-27 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
D1	P02.4	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN4_1			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_1			Mux input channel 4 of TIM module 0
	CCU61_CC62INB			T12 capture input 62
	EDSADC_DSDIN5B			Digital datastream input, channel 5
	QSPI3_SLSIA			Slave select input
	CCU60_CC62INA			T12 capture input 62
	I2C0_SDAA			Serial Data Input 0
	CAN11_RXDA			CAN receive input node 1
	CAN0_ECTT1			External CAN time trigger input
	SENT_SENT12B			Receive input channel 12
	P02.4	O0	General-purpose output	
	GTM_TOUT4	O1	GTM muxed output	
	IOM_REF0_4		Reference input 0	
	ASCLIN2_ASCLK	O2	Shift clock output	
	QSPI3_SLSO0	O3	Master slave select output	
	PSI5S_CLK	O4	PSI5S CLK is a clock that can be used on a pin to drive the external PHY.	
	I2C0_SDA	O5	Serial Data Output	
	ERAY0_TXENA	O6	Transmit Enable Channel A	
	CCU60_CC62	O7	T12 PWM channel 62	
IOM_MON1_0	Monitor input 1			
IOM_REF1_4	Reference input 1			

表 2-27 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
E2	P02.5	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN5_1			<b>Mux input channel 5 of TIM module 1</b>
	GTM_TIM0_IN5_1			<b>Mux input channel 5 of TIM module 0</b>
	EDSADC_DSCIN4B			<b>Modulator clock input, channel 4</b>
	I2C0_SCLA			<b>Serial Clock Input 0</b>
	PSI5_RX1B			<b>RXD inputs (receive data) channel 1</b>
	PSI5S_RXB			<b>RX data input</b>
	QSPI3_MRSTA			<b>Master SPI data input</b>
	SENT_SENT3C			<b>Receive input channel 3</b>
	CAN0_ECTT2			<b>External CAN time trigger input</b>
	P02.5	O0	<b>General-purpose output</b>	
	GTM_TOUT5	O1	<b>GTM muxed output</b>	
	IOM_REF0_5	O2	<b>Reference input 0</b>	
	CAN11_TXD		<b>CAN transmit output node 1</b>	
	QSPI3_MRST	O3	<b>Slave SPI data output</b>	
	IOM_MON2_3	O4	<b>Monitor input 2</b>	
	IOM_REF2_3		<b>Reference input 2</b>	
	EDSADC_DSCOUT4	O5	<b>Modulator clock output</b>	
	I2C0_SCL	O6	<b>Serial Clock Output</b>	
	ERAY0_TXENB	O7	<b>Transmit Enable Channel B</b>	
CCU60_COUT62	O7	<b>T12 PWM channel 62</b>		
IOM_MON1_5		<b>Monitor input 1</b>		
IOM_REF1_1		<b>Reference input 1</b>		

表 2-27 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
E1	P02.6	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM3_IN0_10			<b>Mux input channel 0 of TIM module 3</b>
	GTM_TIM1_IN6_1			<b>Mux input channel 6 of TIM module 1</b>
	GTM_TIM0_IN6_1			<b>Mux input channel 6 of TIM module 0</b>
	CCU60_CC60INC			<b>T12 capture input 60</b>
	SENT_SENT2C			<b>Receive input channel 2</b>
	EDSADC_DSDIN4B			<b>Digital datastream input, channel 4</b>
	EDSADC_ITR5E			<b>Trigger/Gate input, channel 5</b>
	GPT120_T3INA			<b>Trigger/gate input of core timer T3</b>
	CCU60_CCPOS0A			<b>Hall capture input 0</b>
	CCU61_T12HRB			<b>External timer start 12</b>
	QSPI3_MTSRA			<b>Slave SPI data input</b>
	RIF0_RAMP1B			<b>External RAMP B input</b>
	P02.6			O0
	GTM_TOUT6	O1	<b>GTM muxed output</b>	
	IOM_REF0_6		<b>Reference input 0</b>	
	PSI5S_TX	O2	<b>TX data output</b>	
	QSPI3_MTSR	O3	<b>Master SPI data output</b>	
	PSI5_TX1	O4	<b>TXD outputs (send data)</b>	
	IOM_MON1_15		<b>Monitor input 1</b>	
	EVADC_EMUX00	O5	<b>Control of external analog multiplexer interface 0</b>	
	—	O6	<b>Reserved</b>	
	CCU60_CC60	O7	<b>T12 PWM channel 60</b>	
	IOM_MON1_2		<b>Monitor input 1</b>	
IOM_REF1_6	<b>Reference input 1</b>			

表 2-27 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
F2	P02.7	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM3_IN1_10			<b>Mux input channel 1 of TIM module 3</b>
	GTM_TIM1_IN7_1			<b>Mux input channel 7 of TIM module 1</b>
	GTM_TIM0_IN7_1			<b>Mux input channel 7 of TIM module 0</b>
	CCU60_CC61INC			<b>T12 capture input 61</b>
	SENT_SENT1C			<b>Receive input channel 1</b>
	EDSADC_DSCIN3B			<b>Modulator clock input, channel 3</b>
	EDSADC_ITR4E			<b>Trigger/Gate input, channel 4</b>
	GPT120_T3EUDA			<b>Count direction control input of core timer T3</b>
	PSI5_RX2B			<b>RXD inputs (receive data) channel 2</b>
	CCU60_CCPOS1A			<b>Hall capture input 1</b>
	QSPI3_SCLKA			<b>Slave SPI clock inputs</b>
	CCU61_T13HRB			<b>External timer start 13</b>
	P02.7			O0
	GTM_TOUT7	O1	<b>GTM muxed output</b>	
	IOM_REF0_7	O2	<b>Reference input 0</b>	
	—		<b>Reserved</b>	
	QSPI3_SCLK	O3	<b>Master SPI clock output</b>	
	EDSADC_DSCOUT3	O4	<b>Modulator clock output</b>	
	EVADC_EMUX01	O5	<b>Control of external analog multiplexer interface 0</b>	
SENT_SPC1	O6	<b>Transmit output</b>		
CCU60_CC61	O7	<b>T12 PWM channel 61</b>		
IOM_MON1_1		<b>Monitor input 1</b>		
IOM_REF1_5		<b>Reference input 1</b>		

表 2-27 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
F1	P02.8	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM3_IN2_10			<b>Mux input channel 2 of TIM module 3</b>
	GTM_TIM3_IN0_2			<b>Mux input channel 0 of TIM module 3</b>
	GTM_TIM2_IN0_2			<b>Mux input channel 0 of TIM module 2</b>
	CCU60_CC62INC			<b>T12 capture input 62</b>
	SENT_SENT0C			<b>Receive input channel 0</b>
	CCU60_CCPOS2A			<b>Hall capture input 2</b>
	EDSADC_DSDIN3B			<b>Digital datastream input, channel 3</b>
	EDSADC_ITR3E			<b>Trigger/Gate input, channel 3</b>
	GPT120_T4INA			<b>Trigger/gate input of timer T4</b>
	CCU61_T12HRC			<b>External timer start 12</b>
	CCU61_T13HRC			<b>External timer start 13</b>
	GTM_DTMA0_1			<b>CDTM0_DTM4</b>
	P02.8			O0
	GTM_TOUT8	O1	<b>GTM muxed output</b>	
	IOM_REF0_8		<b>Reference input 0</b>	
	QSPI3_SLSO5	O2	<b>Master slave select output</b>	
	ASCLIN8_ASCLK	O3	<b>Shift clock output</b>	
	PSI5_TX2	O4	<b>TXD outputs (send data)</b>	
	IOM_REF1_15		<b>Reference input 1</b>	
EVADC_EMUX02	O5	<b>Control of external analog multiplexer interface 0</b>		
GETH_MDC	O6	<b>MDIO clock</b>		
CCU60_CC62	O7	<b>T12 PWM channel 62</b>		
IOM_MON1_0		<b>Monitor input 1</b>		
IOM_REF1_4		<b>Reference input 1</b>		

表 2-27 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
E4	P02.9	I	SLOW / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM4_IN2_2			Mux input channel 2 of TIM module 4	
	GTM_TIM3_IN3_10			Mux input channel 3 of TIM module 3	
	GTM_TIM0_IN2_10			Mux input channel 2 of TIM module 0	
	SENT_SENT20B			Receive input channel 20	
	ASCLIN8_ARXA			Receive input	
	P02.9			O0	General-purpose output
	GTM_TOUT116			O1	GTM muxed output
	ASCLIN2_ATX			O2	Transmit output
	IOM_MON2_14				Monitor input 2
	IOM_REF2_14				Reference input 2
	ASCLIN8_ATX			O3	Transmit output
	—			O4	Reserved
	CAN01_TXD			O5	CAN transmit output node 1
	IOM_MON2_6				Monitor input 2
	IOM_REF2_6				Reference input 2
	—			O6	Reserved
—	O7	Reserved			
F5	P02.10	I	SLOW / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM4_IN3_2			Mux input channel 3 of TIM module 4	
	GTM_TIM3_IN4_11			Mux input channel 4 of TIM module 3	
	GTM_TIM0_IN3_10			Mux input channel 3 of TIM module 0	
	ASCLIN2_ARXC			Receive input	
	CAN01_RXDE			CAN receive input node 1	
	SENT_SENT21B			Receive input channel 21	
	ASCLIN8_ARXB			Receive input	
	P02.10			O0	General-purpose output
	GTM_TOUT117			O1	GTM muxed output
	—			O2	Reserved
	—			O3	Reserved
	—			O4	Reserved
	—			O5	Reserved
	—			O6	Reserved
	—			O7	Reserved

表 2-27 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
F4	P02.11	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN4_3			Mux input channel 4 of TIM module 4
	GTM_TIM3_IN5_12			Mux input channel 5 of TIM module 3
	GTM_TIM0_IN7_7			Mux input channel 7 of TIM module 0
	SENT_SENT22B			Receive input channel 22
	EVADC_G9CH15			Analog input channel 15, group 9
	P02.11	O0		General-purpose output
	GTM_TOUT118	O1		GTM muxed output
	—	O2		Reserved
	ASCLIN8_ASLSO	O3		Slave select signal output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-28 端口 P10 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
A7	P10.0	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN0_12			Mux input channel 0 of TIM module 4
	GTM_TIM1_IN4_2			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_2			Mux input channel 4 of TIM module 0
	GPT120_T6EUDB			Count direction control input of core timer T6
	ASCLIN11_ARXA			Receive input
	GETH_RXERC			Receive Error MII
	GTM_DTMA5_2			CDTM5_DTM4
	P10.0	O0		General-purpose output
	GTM_TOUT102	O1		GTM muxed output
	ASCLIN11_ATX	O2		Transmit output
	QSPI1_SLSO10	O3		Master slave select output
	—	O4		Reserved
	EVADC_FC6BFLOUT	O5		Boundary flag output, FC channel 6
—	O6	Reserved		
—	O7	Reserved		

表 2-28 端口 P10 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
B7	P10.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN4_12			Mux input channel 4 of TIM module 4
	GTM_TIM1_IN1_3			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_3			Mux input channel 1 of TIM module 0
	GPT120_T5EUDB			Count direction control input of timer T5
	QSPI1_MRSTA			Master SPI data input
	GTM_DTMT0_1			CDTM0_DTM0
	P10.1	O0	General-purpose output	
	GTM_TOUT103	O1	GTM muxed output	
	QSPI1_MTSR	O2	Master SPI data output	
	QSPI1_MRST	O3	Slave SPI data output	
	IOM_MON2_1		Monitor input 2	
	IOM_REF2_1		Reference input 2	
	MSC0_EN1	O4	Chip Select	
	EVADC_FC1BFLOUT	O5	Boundary flag output, FC channel 1	
	—	O6	Reserved	
	—	O7	Reserved	
A5	P10.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN5_12			Mux input channel 5 of TIM module 4
	GTM_TIM1_IN2_3			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_3			Mux input channel 2 of TIM module 0
	CAN02_RXDE			CAN receive input node 2
	MSC0_SDI1			Upstream asynchronous input signal
	QSPI1_SCLKA			Slave SPI clock inputs
	GPT120_T6INB			Trigger/gate input of core timer T6
	SCU_E_REQ2_0			ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	GTM_DTMT2_2	CDTM2_DTM0		
	P10.2	O0	General-purpose output	
	GTM_TOUT104	O1	GTM muxed output	
	IOM_MON2_9		Monitor input 2	
	—		Reserved	
	QSPI1_SCLK	O3	Master SPI clock output	
	MSC0_EN0	O4	Chip Select	
	EVADC_FC3BFLOUT	O5	Boundary flag output, FC channel 3	
—	O6	Reserved		
—	O7	Reserved		

表 2-28 端口 P10 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A6	P10.3	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN6_10			Mux input channel 6 of TIM module 4
	GTM_TIM1_IN3_3			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_3			Mux input channel 3 of TIM module 0
	QSPI1_MTSRA			Slave SPI data input
	SCU_E_REQ3_0			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	GPT120_T5INB			Trigger/gate input of timer T5
	P10.3	O0	General-purpose output	
	GTM_TOUT105	O1	GTM muxed output	
	IOM_MON2_10	O2	Monitor input 2	
	—		Reserved	
	QSPI1_MTSR	O3	Master SPI data output	
	MSC0_EN0	O4	Chip Select	
	—	O5	Reserved	
	CAN02_TXD	O6	CAN transmit output node 2	
	IOM_MON2_7	O7	Monitor input 2	
	IOM_REF2_7		Reference input 2	
—	Reserved			
B6	P10.4	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN7_3			Mux input channel 7 of TIM module 4
	GTM_TIM1_IN6_2			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_2			Mux input channel 6 of TIM module 0
	QSPI1_MTSRC			Slave SPI data input
	CCU60_CCPOS0C			Hall capture input 0
	GPT120_T3INB			Trigger/gate input of core timer T3
	ASCLIN11_ARXB	Receive input		
	P10.4	O0	General-purpose output	
	GTM_TOUT106	O1	GTM muxed output	
	IOM_MON2_11	O2	Monitor input 2	
	—		Reserved	
	QSPI1_SLSO8	O3	Master slave select output	
	QSPI1_MTSR	O4	Master SPI data output	
	MSC0_EN0	O5	Chip Select	
	—	O6	Reserved	
	—	O7	Reserved	

表 2-28 端口 P10 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
B5	P10.5	I	SLOW / PU2 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM4_IN3_13			<b>Mux input channel 3 of TIM module 4</b>
	GTM_TIM1_IN2_4			<b>Mux input channel 2 of TIM module 1</b>
	GTM_TIM0_IN2_4			<b>Mux input channel 2 of TIM module 0</b>
	PMS_HWCFG4IN			<b>HWCFG4 pin input</b>
	CAN20_RXDA			<b>CAN receive input node 0</b>
	MSC0_INJ1			<b>Injection signal from port</b>
	P10.5	O0		<b>General-purpose output</b>
	GTM_TOUT107	O1		<b>GTM muxed output</b>
	IOM_REF2_9	O2		<b>Reference input 2</b>
	ASCLIN2_ATX			<b>Transmit output</b>
	IOM_MON2_14			<b>Monitor input 2</b>
	IOM_REF2_14	O3		<b>Reference input 2</b>
	QSPI3_SLSO8			<b>Master slave select output</b>
	QSPI1_SLSO9	O4		<b>Master slave select output</b>
	GPT120_T6OUT	O5		<b>External output for overflow/underflow detection of core timer T6</b>
	ASCLIN2_ASLSO	O6		<b>Slave select signal output</b>
	PSI5_TX3	O7		<b>TXD outputs (send data)</b>

表 2-28 端口 P10 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A4	P10.6	I	SLOW / PU2 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM4_IN2_13			<b>Mux input channel 2 of TIM module 4</b>
	GTM_TIM1_IN3_4			<b>Mux input channel 3 of TIM module 1</b>
	GTM_TIM0_IN3_4			<b>Mux input channel 3 of TIM module 0</b>
	PSI5_RX3C			<b>RXD inputs (receive data) channel 3</b>
	ASCLIN2_ARXD			<b>Receive input</b>
	QSPI3_MTSRB			<b>Slave SPI data input</b>
	PMS_HWCFG5IN			<b>HWCFG5 pin input</b>
	P10.6	O0		<b>General-purpose output</b>
	GTM_TOUT108	O1		<b>GTM muxed output</b>
	IOM_REF2_10			<b>Reference input 2</b>
	ASCLIN2_ASCLK	O2		<b>Shift clock output</b>
	QSPI3_MTSR	O3		<b>Master SPI data output</b>
	GPT120_T3OUT	O4		<b>External output for overflow/underflow detection of core timer T3</b>
	CAN20_TXD	O5		<b>CAN transmit output node 0</b>
	QSPI1_MRST	O6		<b>Slave SPI data output</b>
	IOM_MON2_1			<b>Monitor input 2</b>
	IOM_REF2_1			<b>Reference input 2</b>
	EVADC_FC7BFLOUT	O7		<b>Boundary flag output, FC channel 7</b>

表 2-28 端口 P10 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A3	P10.7	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN0_3			<b>Mux input channel 0 of TIM module 1</b>
	GTM_TIM0_IN0_3			<b>Mux input channel 0 of TIM module 0</b>
	GPT120_T3EUIDB			<b>Count direction control input of core timer T3</b>
	ASCLIN2_ACTSA			<b>Clear to send input</b>
	QSPI3_MRSTB			<b>Master SPI data input</b>
	SCU_E_REQ0_2			<b>ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	CCU60_CCPOS1C			<b>Hall capture input 1</b>
	P10.7	O0	<b>General-purpose output</b>	
	GTM_TOUT109	O1	<b>GTM muxed output</b>	
	IOM_REF2_11	O2	<b>Reference input 2</b>	
	—		<b>Reserved</b>	
	QSPI3_MRST	O3	<b>Slave SPI data output</b>	
	IOM_MON2_3		<b>Monitor input 2</b>	
	IOM_REF2_3		<b>Reference input 2</b>	
	—	O4	<b>Reserved</b>	
	CAN20_TXD	O5	<b>CAN transmit output node 0</b>	
	CAN12_TXD	O6	<b>CAN transmit output node 2</b>	
	—	O7	<b>Reserved</b>	

表 2-28 端口 P10 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
B4	P10.8	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>	
	GTM_TIM4_IN0_13			<b>Mux input channel 0 of TIM module 4</b>	
	GTM_TIM1_IN5_2			<b>Mux input channel 5 of TIM module 1</b>	
	GTM_TIM0_IN5_2			<b>Mux input channel 5 of TIM module 0</b>	
	CAN12_RXDB			<b>CAN receive input node 2</b>	
	GPT120_T4INB			<b>Trigger/gate input of timer T4</b>	
	QSPI3_SCLKB			<b>Slave SPI clock inputs</b>	
	SCU_E_REQ1_2			<b>ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>	
	CCU60_CCPOS2C			<b>Hall capture input 2</b>	
	CAN20_RXDB			<b>CAN receive input node 0</b>	
	RIF1_RAMP1B			<b>External RAMP B input</b>	
	P10.8			O0	<b>General-purpose output</b>
	GTM_TOUT110			O1	<b>GTM muxed output</b>
	ASCLIN2_ARTS	O2	<b>Ready to send output</b>		
	QSPI3_SCLK	O3	<b>Master SPI clock output</b>		
	—	O4	<b>Reserved</b>		
	—	O5	<b>Reserved</b>		
	—	O6	<b>Reserved</b>		
	—	O7	<b>Reserved</b>		

表 2-29 端口 P11 的功能

Ball	Symbol	Ctrl.	Buffer Type	Function	
E10	P11.0	I	RFAST / PU1 / VFLEX / ES	<b>General-purpose input</b>	
	GTM_TIM7_IN5_1			<b>Mux input channel 5 of TIM module 7</b>	
	GTM_TIM4_IN0_4			<b>Mux input channel 0 of TIM module 4</b>	
	GTM_TIM2_IN0_7			<b>Mux input channel 0 of TIM module 2</b>	
	ASCLIN3_ARXB			<b>Receive input</b>	
	GTM_DTMA2_1			<b>CDTM2_DTM4</b>	
	P11.0			O0	<b>General-purpose output</b>
	GTM_TOUT119			O1	<b>GTM muxed output</b>
	ASCLIN3_ATX			O2	<b>Transmit output</b>
	IOM_MON2_15				<b>Monitor input 2</b>
	IOM_REF2_15	<b>Reference input 2</b>			
	—	O3	<b>Reserved</b>		
	—	O4	<b>Reserved</b>		
	CAN11_TXD	O5	<b>CAN transmit output node 1</b>		
	GETH_TXD3	O6	<b>Transmit Data</b>		
—	O7	<b>Reserved</b>			
E9	P11.1	I	RFAST / PU1 / VFLEX / ES	<b>General-purpose input</b>	
	GTM_TIM7_IN6_1			<b>Mux input channel 6 of TIM module 7</b>	
	GTM_TIM4_IN1_5			<b>Mux input channel 1 of TIM module 4</b>	
	GTM_TIM2_IN1_6			<b>Mux input channel 1 of TIM module 2</b>	
	P11.1			O0	<b>General-purpose output</b>
	GTM_TOUT120			O1	<b>GTM muxed output</b>
	ASCLIN3_ASCLK			O2	<b>Shift clock output</b>
	ASCLIN3_ATX			O3	<b>Transmit output</b>
	IOM_MON2_15				<b>Monitor input 2</b>
	IOM_REF2_15				<b>Reference input 2</b>
	—	O4	<b>Reserved</b>		
	CAN12_TXD	O5	<b>CAN transmit output node 2</b>		
	GETH_TXD2	O6	<b>Transmit Data</b>		
	—	O7	<b>Reserved</b>		

表 2-29 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A10	P11.2	I	RFAST / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM3_IN1_3			Mux input channel 1 of TIM module 3
	GTM_TIM2_IN1_3			Mux input channel 1 of TIM module 2
	P11.2	00		General-purpose output
	GTM_TOUT95	01		GTM muxed output
	—	02		Reserved
	QSPI0_SLSO5	03		Master slave select output
	QSPI1_SLSO5	04		Master slave select output
	MSC0_EN1	05		Chip Select
	GETH_TXD1	06		Transmit Data
	CCU60_COUT63	07		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1
B10	P11.3	I	RFAST / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM3_IN2_2			Mux input channel 2 of TIM module 3
	GTM_TIM2_IN2_2			Mux input channel 2 of TIM module 2
	MSC0_SDI3			Upstream asynchronous input signal
	QSPI1_MRSTB			Master SPI data input
	P11.3	00		General-purpose output
	GTM_TOUT96	01		GTM muxed output
	—	02		Reserved
	QSPI1_MRST	03		Slave SPI data output
	IOM_MON2_1			Monitor input 2
	IOM_REF2_1			Reference input 2
	ERAY0_TXDA	04		Transmit Channel A
	—	05		Reserved
	GETH_TXD0	06		Transmit Data
	CCU60_COUT62	07		T12 PWM channel 62
	IOM_MON1_5			Monitor input 1
	IOM_REF1_1			Reference input 1

表 2-29 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
D10	P11.4	I	RFAST / PU1 / VFLEX / ES	<b>General-purpose input</b>
	GTM_TIM7_IN7_1			<b>Mux input channel 7 of TIM module 7</b>
	GTM_TIM4_IN2_5			<b>Mux input channel 2 of TIM module 4</b>
	GTM_TIM2_IN2_6			<b>Mux input channel 2 of TIM module 2</b>
	GETH_RXCLKB			<b>Receive Clock MII</b>
	P11.4	O0		<b>General-purpose output</b>
	GTM_TOUT121	O1		<b>GTM muxed output</b>
	ASCLIN3_ASCLK	O2		<b>Shift clock output</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	CAN13_TXD	O5		<b>CAN transmit output node 3</b>
	GETH_TXER	O6		<b>Transmit Error MII</b>
	GETH_TXCLK	O7		<b>Transmit Clock Output for RGMII</b>
D8	P11.5	I	SLOW / RGMII_In put / PU1 / VFLEX / ES	<b>General-purpose input</b>
	GTM_TIM4_IN3_5			<b>Mux input channel 3 of TIM module 4</b>
	GTM_TIM2_IN3_8			<b>Mux input channel 3 of TIM module 2</b>
	GETH_TXCLKA			<b>Transmit Clock Input for MII</b>
	GETH_GREFCLK			<b>Gigabit Reference Clock input for RGMII (125 MHz high precision)</b>
	P11.5	O0		<b>General-purpose output</b>
	GTM_TOUT122	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	CAN20_TXD	O5		<b>CAN transmit output node 0</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>

表 2-29 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
D9	P11.6	I	RFAST / PU1 / VFLEX / ES	<b>General-purpose input</b>
	GTM_TIM3_IN3_2			<b>Mux input channel 3 of TIM module 3</b>
	GTM_TIM2_IN3_2			<b>Mux input channel 3 of TIM module 2</b>
	QSPI1_SCLKB			<b>Slave SPI clock inputs</b>
	P11.6	O0		<b>General-purpose output</b>
	GTM_TOUT97	O1		<b>GTM muxed output</b>
	ERAY0_TXENB	O2		<b>Transmit Enable Channel B</b>
	QSPI1_SCLK	O3		<b>Master SPI clock output</b>
	ERAY0_TXENA	O4		<b>Transmit Enable Channel A</b>
	MSC0_FCLP	O5		<b>Shift-clock direct part of the differential signal</b>
	GETH_TXEN	O6		<b>Transmit Enable MII and RMII</b>
	GETH_TCTL			<b>Transmit Control for RGMII</b>
	CCU60_COUT61	O7		<b>T12 PWM channel 61</b>
	IOM_MON1_4			<b>Monitor input 1</b>
IOM_REF1_2	<b>Reference input 1</b>			
E8	P11.7	I	SLOW / RGMII_In put / PU1 / VFLEX / ES	<b>General-purpose input</b>
	GTM_TIM4_IN4_5			<b>Mux input channel 4 of TIM module 4</b>
	GTM_TIM2_IN4_7			<b>Mux input channel 4 of TIM module 2</b>
	GETH_RXD3A			<b>Receive Data 3 MII and RGMII (RGMII can use RXD3A only)</b>
	CAN11_RXDD			<b>CAN receive input node 1</b>
	P11.7	O0		<b>General-purpose output</b>
	GTM_TOUT123	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>

表 2-29 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
E7	P11.8	I	SLOW / RGMII_In put / PU1 / VFLEX / ES	<b>General-purpose input</b>
	GTM_TIM4_IN5_5			<b>Mux input channel 5 of TIM module 4</b>
	GTM_TIM2_IN5_8			<b>Mux input channel 5 of TIM module 2</b>
	GETH_RXD2A			<b>Receive Data 2 MII and RGMII (RGMII can use RXD2A only)</b>
	CAN12_RXDD			<b>CAN receive input node 2</b>
	P11.8	O0		<b>General-purpose output</b>
	GTM_TOUT124	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
—	O7	<b>Reserved</b>		
A9	P11.9	I	FAST / RGMII_In put / PU1 / VFLEX / ES	<b>General-purpose input</b>
	GTM_TIM3_IN4_2			<b>Mux input channel 4 of TIM module 3</b>
	GTM_TIM2_IN4_2			<b>Mux input channel 4 of TIM module 2</b>
	QSPI1_MTSRB			<b>Slave SPI data input</b>
	ERAY0_RXDA1			<b>Receive Channel A1</b>
	GETH_RXD1A			<b>Receive Data 1 MII, RMII and RGMII (RGMII can use RXD1A only)</b>
	P11.9	O0		<b>General-purpose output</b>
	GTM_TOUT98	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	QSPI1_MTSR	O3		<b>Master SPI data output</b>
	—	O4		<b>Reserved</b>
	MSC0_SOP	O5		<b>Data output - direct part of the differential signal</b>
	—	O6		<b>Reserved</b>
	CCU60_COUT60	O7		<b>T12 PWM channel 60</b>
IOM_MON1_3		<b>Monitor input 1</b>		
IOM_REF1_3		<b>Reference input 1</b>		

表 2-29 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
B9	P11.10	I	FAST / RGMII_Input / PU1 / VFLEX / ES	<b>General-purpose input</b>	
	GTM_TIM3_IN5_2			<b>Mux input channel 5 of TIM module 3</b>	
	GTM_TIM2_IN5_2			<b>Mux input channel 5 of TIM module 2</b>	
	GTM_TIM2_IN0_9			<b>Mux input channel 0 of TIM module 2</b>	
	CAN03_RXDD			<b>CAN receive input node 3</b>	
	ERAY0_RXDB1			<b>Receive Channel B1</b>	
	ASCLIN1_ARXE			<b>Receive input</b>	
	SCU_E_REQ6_3			<b>ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>	
	MSC0_SDI0			<b>Upstream asynchronous input signal</b>	
	GETH_RXD0A			<b>Receive Data 0 MII, RMII and RGMII (RGMII can use RXD0A only)</b>	
	QSPI1_SLSIA			<b>Slave select input</b>	
	P11.10			O0	<b>General-purpose output</b>
	GTM_TOUT99			O1	<b>GTM muxed output</b>
	—	O2	<b>Reserved</b>		
	QSPI0_SLSO3	O3	<b>Master slave select output</b>		
	QSPI1_SLSO3	O4	<b>Master slave select output</b>		
	—	O5	<b>Reserved</b>		
	—	O6	<b>Reserved</b>		
	CCU60_CC62	O7	<b>T12 PWM channel 62</b>		
	IOM_MON1_0		<b>Monitor input 1</b>		
IOM_REF1_4	<b>Reference input 1</b>				

表 2-29 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A8	P11.11	I	FAST / RGMII_In put / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM3_IN6_2			Mux input channel 6 of TIM module 3
	GTM_TIM3_IN0_14			Mux input channel 0 of TIM module 3
	GTM_TIM2_IN6_2			Mux input channel 6 of TIM module 2
	GETH_CRSDVA			Carrier Sense / Data Valid combi-signal for RMII
	GETH_RXDVA			Receive Data Valid MII
	GETH_CRSB			Carrier Sense MII
	GETH_RCTLA			Receive Control for RGMII
	P11.11			O0
	GTM_TOUT100	O1	GTM muxed output	
	—	O2	Reserved	
	QSPI0_SLSO4	O3	Master slave select output	
	QSPI1_SLSO4	O4	Master slave select output	
	MSC0_EN0	O5	Chip Select	
	ERAY0_TXENB	O6	Transmit Enable Channel B	
	CCU60_CC61	O7	T12 PWM channel 61	
	IOM_MON1_1		Monitor input 1	
IOM_REF1_5	Reference input 1			
B8	P11.12	I	FAST / RGMII_In put / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM3_IN7_2			Mux input channel 7 of TIM module 3
	GTM_TIM2_IN7_2			Mux input channel 7 of TIM module 2
	GETH_REFCLKA			Reference Clock input for RMII (50 MHz)
	GETH_TXCLKB			Transmit Clock Input for MII
	GETH_RXCLKA			Receive Clock MII
	P11.12	O0	General-purpose output	
	GTM_TOUT101	O1	GTM muxed output	
	ASCLIN1_ATX	O2	Transmit output	
	IOM_MON2_13		Monitor input 2	
	IOM_REF2_13		Reference input 2	
	GTM_CLK2	O3	CGM generated clock	
	ERAY0_TXDB	O4	Transmit Channel B	
	CAN03_TXD	O5	CAN transmit output node 3	
	IOM_MON2_8		Monitor input 2	
	IOM_REF2_8	O6	Reference input 2	
	CCU_EXTCLK1		External Clock 1	
	CCU60_CC60		T12 PWM channel 60	
	IOM_MON1_2	O7	Monitor input 1	
IOM_REF1_6	Reference input 1			

表 2-29 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
E6	P11.13	I	SLOW / PU1 / VFLEX / ES	<b>General-purpose input</b>
	GTM_TIM4_IN6_5			<b>Mux input channel 6 of TIM module 4</b>
	GTM_TIM2_IN6_7			<b>Mux input channel 6 of TIM module 2</b>
	GETH_RXERA			<b>Receive Error MII</b>
	I2C1_SDAA			<b>Serial Data Input 0</b>
	CAN13_RXDD			<b>CAN receive input node 3</b>
	P11.13			O0
	GTM_TOUT125	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	I2C1_SDA	O6		<b>Serial Data Output</b>
	—	O7		<b>Reserved</b>
D7	P11.14	I	SLOW / PU1 / VFLEX / ES	<b>General-purpose input</b>
	GTM_TIM4_IN7_4			<b>Mux input channel 7 of TIM module 4</b>
	GTM_TIM2_IN7_8			<b>Mux input channel 7 of TIM module 2</b>
	GETH_CRSDVB			<b>Carrier Sense / Data Valid combi-signal for RMII</b>
	GETH_RXDVB			<b>Receive Data Valid MII</b>
	GETH_CRSA			<b>Carrier Sense MII</b>
	I2C1_SCLA			<b>Serial Clock Input 0</b>
	CAN20_RXDF	<b>CAN receive input node 0</b>		
	P11.14	O0		<b>General-purpose output</b>
	GTM_TOUT126	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
I2C1_SCL	O6	<b>Serial Clock Output</b>		
—	O7	<b>Reserved</b>		

表 2-29 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
D6	P11.15	I	SLOW / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM4_IN7_5			Mux input channel 7 of TIM module 4
	GTM_TIM0_IN7_8			Mux input channel 7 of TIM module 0
	GETH_COLA			Collision MII
	P11.15	O0		General-purpose output
	GTM_TOUT127	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-30 端口 P12 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
E12	P12.0	I	SLOW / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM7_IN3_2			Mux input channel 3 of TIM module 7
	GTM_TIM4_IN0_5			Mux input channel 0 of TIM module 4
	GTM_TIM3_IN0_7			Mux input channel 0 of TIM module 3
	CAN00_RXDC			CAN receive input node 0
	GETH_RXCLKC			Receive Clock MII
	GTM_DTMA4_0			CDTM4_DTM4
	P12.0	O0		General-purpose output
	GTM_TOUT128	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
GETH_MDC	O6	MDIO clock		
—	O7	Reserved		

表 2-30 端口 P12 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
E11	P12.1	I	SLOW / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM7_IN4_1			Mux input channel 4 of TIM module 7
	GTM_TIM4_IN1_6			Mux input channel 1 of TIM module 4
	GTM_TIM3_IN1_6			Mux input channel 1 of TIM module 3
	GETH_MDIOC			MDIO Input
	P12.1	O0		General-purpose output
	GTM_TOUT129	O1		GTM muxed output
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	CAN00_TXD	O5		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	—	O6		Reserved
	—	O7		Reserved
GETH_MDIO	O	MDIO Output		

表 2-31 端口 P13 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
B12	P13.0	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM3_IN5_3			Mux input channel 5 of TIM module 3
	GTM_TIM2_IN5_3			Mux input channel 5 of TIM module 2
	ASCLIN10_ARXC			Receive input
	P13.0	O0		General-purpose output
	GTM_TOUT91	O1		GTM muxed output
	ASCLIN10_ATX	O2		Transmit output
	QSPI2_SCLKN	O3		Master SPI clock output (LVDS N line)
	MSC0_EN1	O4		Chip Select
	MSC0_FCLN	O5		Shift-clock inverted part of the differential signal
	—	O6		Reserved
	CAN10_TXD	O7		CAN transmit output node 0

表 2-31 端口 P13 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
A12	P13.1	I	LVDS_TX / FAST / PU1 / VEXT / ES6	<b>General-purpose input</b>	
	GTM_TIM3_IN6_3			<b>Mux input channel 6 of TIM module 3</b>	
	GTM_TIM2_IN6_3			<b>Mux input channel 6 of TIM module 2</b>	
	I2C0_SCLB			<b>Serial Clock Input 1</b>	
	CAN10_RXDD			<b>CAN receive input node 0</b>	
	ASCLIN10_ARXD			<b>Receive input</b>	
	P13.1			O0	<b>General-purpose output</b>
	GTM_TOUT92	O1		<b>GTM muxed output</b>	
	—	O2		<b>Reserved</b>	
	QSPI2_SCLKP	O3		<b>Master SPI clock output (LVDS P line)</b>	
	—	O4		<b>Reserved</b>	
	MSC0_FCLP	O5		<b>Shift-clock direct part of the differential signal</b>	
	I2C0_SCL	O6		<b>Serial Clock Output</b>	
	—	O7		<b>Reserved</b>	
B11	P13.2	I	LVDS_TX / FAST / PU1 / VEXT / ES6	<b>General-purpose input</b>	
	GTM_TIM3_IN7_3			<b>Mux input channel 7 of TIM module 3</b>	
	GTM_TIM2_IN7_3			<b>Mux input channel 7 of TIM module 2</b>	
	GPT120_CAPINA			<b>Trigger input to capture value of timer T5 into CAPREL register</b>	
	I2C0_SDAB			<b>Serial Data Input 1</b>	
	P13.2			O0	<b>General-purpose output</b>
	GTM_TOUT93			O1	<b>GTM muxed output</b>
	ASCLIN10_ASCLK	O2		<b>Shift clock output</b>	
	QSPI2_MTSRN	O3		<b>Master SPI data output (LVDS N line)</b>	
	MSC0_FCLP	O4		<b>Shift-clock direct part of the differential signal</b>	
	MSC0_SON	O5		<b>Data output - inverted part of the differential signal</b>	
	I2C0_SDA	O6		<b>Serial Data Output</b>	
	—	O7		<b>Reserved</b>	

表 2-31 端口 P13 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A11	P13.3	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM3_IN0_3			Mux input channel 0 of TIM module 3
	GTM_TIM2_IN0_3			Mux input channel 0 of TIM module 2
	P13.3	O0		General-purpose output
	GTM_TOUT94	O1		GTM muxed output
	ASCLIN10_ASLSO	O2		Slave select signal output
	QSPI2_MTSRP	O3		Master SPI data output (LVDS P line)
	—	O4		Reserved
	MSC0_SOP	O5		Data output - direct part of the differential signal
	—	O6		Reserved
	—	O7		Reserved

表 2-32 端口 P14 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
B16	P14.0	I	FAST / PU1 / VEXT / ES2	General-purpose input
	GTM_TIM1_IN3_5			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_5			Mux input channel 3 of TIM module 0
	SENT_SENT17D			Receive input channel 17
	P14.0	O0		General-purpose output
	GTM_TOUT80	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	ERAY0_TXDA			O3
	ERAY0_TXDB	O4		Transmit Channel B
	CAN01_TXD	O5		CAN transmit output node 1
	IOM_MON2_6			Monitor input 2
	IOM_REF2_6			Reference input 2
	ASCLIN0_ASCLK			O6
	CCU60_COUT62	O7		T12 PWM channel 62
	IOM_MON1_5			Monitor input 1
	IOM_REF1_1			Reference input 1

表 2-32 端口 P14 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A15	P14.1	I	FAST / PU1 / VEXT / ES2	<b>General-purpose input</b>
	GTM_TIM1_IN4_3			<b>Mux input channel 4 of TIM module 1</b>
	GTM_TIM0_IN4_3			<b>Mux input channel 4 of TIM module 0</b>
	ERAY0_RXDA3			<b>Receive Channel A3</b>
	ASCLIN0_ARXA			<b>Receive input</b>
	SENT_SENT18D			<b>Receive input channel 18</b>
	ERAY0_RXDB3			<b>Receive Channel B3</b>
	CAN01_RXDB			<b>CAN receive input node 1</b>
	SCU_E_REQ3_1			<b>ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	PMS_PINAWKP			<b>PINA ( P14.1) pin input</b>
	P14.1	O0	<b>General-purpose output</b>	
	GTM_TOUT81	O1	<b>GTM muxed output</b>	
	ASCLIN0_ATX	O2	<b>Transmit output</b>	
	IOM_MON2_12		<b>Monitor input 2</b>	
	IOM_REF2_12	<b>Reference input 2</b>		
	—	O3	<b>Reserved</b>	
	—	O4	<b>Reserved</b>	
	—	O5	<b>Reserved</b>	
	—	O6	<b>Reserved</b>	
	CCU60_COUT63	O7	<b>T13 PWM channel 63</b>	
IOM_MON1_6	<b>Monitor input 1</b>			
IOM_REF1_0	<b>Reference input 1</b>			
E13	P14.2	I	SLOW / PU2 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN5_3			<b>Mux input channel 5 of TIM module 1</b>
	GTM_TIM0_IN5_3			<b>Mux input channel 5 of TIM module 0</b>
	PMS_HWCFG2IN			<b>HWCFG2 pin input</b>
	P14.2	O0	<b>General-purpose output</b>	
	GTM_TOUT82	O1	<b>GTM muxed output</b>	
	ASCLIN2_ATX	O2	<b>Transmit output</b>	
	IOM_MON2_14		<b>Monitor input 2</b>	
	IOM_REF2_14	<b>Reference input 2</b>		
	QSPI2_SLSO1	O3	<b>Master slave select output</b>	
	—	O4	<b>Reserved</b>	
	—	O5	<b>Reserved</b>	
	ASCLIN2_ASCLK	O6	<b>Shift clock output</b>	
	—	O7	<b>Reserved</b>	

表 2-32 端口 P14 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
B14	P14.3	I	SLOW / PU2 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN6_3			<b>Mux input channel 6 of TIM module 1</b>
	GTM_TIM0_IN6_3			<b>Mux input channel 6 of TIM module 0</b>
	PMS_HWCFG3IN			<b>HWCFG3 pin input</b>
	ASCLIN2_ARXA			<b>Receive input</b>
	MSC0_SDI2			<b>Upstream asynchronous input signal</b>
	SCU_E_REQ1_0			<b>ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	P14.3	O0	<b>General-purpose output</b>	
	GTM_TOUT83	O1	<b>GTM muxed output</b>	
	ASCLIN2_ATX	O2	<b>Transmit output</b>	
	IOM_MON2_14		<b>Monitor input 2</b>	
	IOM_REF2_14		<b>Reference input 2</b>	
	QSPI2_SLSO3	O3	<b>Master slave select output</b>	
	ASCLIN1_ASLSO	O4	<b>Slave select signal output</b>	
	ASCLIN3_ASLSO	O5	<b>Slave select signal output</b>	
	—	O6	<b>Reserved</b>	
	—	O7	<b>Reserved</b>	
B15	P14.4	I	SLOW / PU2 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN7_2			<b>Mux input channel 7 of TIM module 1</b>
	GTM_TIM0_IN7_2			<b>Mux input channel 7 of TIM module 0</b>
	PMS_HWCFG6IN			<b>HWCFG6 pin input</b>
	GTM_DTMT0_0			<b>CDTMO_DTM0</b>
	P14.4	O0	<b>General-purpose output</b>	
	GTM_TOUT84	O1	<b>GTM muxed output</b>	
	—	O2	<b>Reserved</b>	
	—	O3	<b>Reserved</b>	
	—	O4	<b>Reserved</b>	
	—	O5	<b>Reserved</b>	
	GETH_PPS	O6	<b>Pulse Per Second</b>	
	—	O7	<b>Reserved</b>	

表 2-32 端口 P14 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A14	P14.5	I	FAST / PU2 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN0_4			<b>Mux input channel 0 of TIM module 1</b>
	GTM_TIM0_IN0_4			<b>Mux input channel 0 of TIM module 0</b>
	PMS_HWCFG1IN			<b>HWCFG1 pin input</b>
	QSPI5_MRSTB			<b>Master SPI data input</b>
	GTM_DTMA2_0			<b>CDTM2_DTM4</b>
	P14.5			O0
	GTM_TOUT85	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	QSPI5_MRST	O3		<b>Slave SPI data output</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	ERAY0_TXDB	O6		<b>Transmit Channel B</b>
	ERAY1_TXDB	O7		<b>Transmit Channel B</b>
B13	P14.6	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN1_4			<b>Mux input channel 1 of TIM module 1</b>
	GTM_TIM0_IN1_4			<b>Mux input channel 1 of TIM module 0</b>
	QSPI5_MTSRB			<b>Slave SPI data input</b>
	P14.6	O0		<b>General-purpose output</b>
	GTM_TOUT86	O1		<b>GTM muxed output</b>
	QSPI5_MTSR	O2		<b>Master SPI data output</b>
	QSPI2_SLSO2	O3		<b>Master slave select output</b>
	CAN13_TXD	O4		<b>CAN transmit output node 3</b>
	—	O5		<b>Reserved</b>
	ERAY0_TXENB	O6		<b>Transmit Enable Channel B</b>
	ERAY1_TXENB	O7		<b>Transmit Enable Channel B</b>

表 2-32 端口 P14 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
D13	P14.7	I	SLOW / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM4_IN7_10			Mux input channel 7 of TIM module 4	
	GTM_TIM1_IN0_5			Mux input channel 0 of TIM module 1	
	GTM_TIM0_IN0_5			Mux input channel 0 of TIM module 0	
	ERAY0_RXDB0			Receive Channel B0	
	ERAY1_RXDB0			Receive Channel B0	
	CAN10_RXDB			CAN receive input node 0	
	CAN13_RXDA			CAN receive input node 3	
	ASCLIN9_ARXC			Receive input	
	P14.7	O0	General-purpose output		
	GTM_TOUT87	O1	GTM muxed output		
	ASCLIN0_ARTS	O2	Ready to send output		
	QSPI2_SLSO4	O3	Master slave select output		
	ASCLIN9_ATX	O4	Transmit output		
	—	O5	Reserved		
	—	O6	Reserved		
	—	O7	Reserved		
A13	P14.8	I	SLOW / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM3_IN2_3			Mux input channel 2 of TIM module 3	
	GTM_TIM2_IN2_3			Mux input channel 2 of TIM module 2	
	ERAY0_RXDA0			Receive Channel A0	
	CAN02_RXDD			CAN receive input node 2	
	ASCLIN1_ARXD			Receive input	
	ERAY1_RXDA0			Receive Channel A0	
	P14.8			O0	General-purpose output
	GTM_TOUT88			O1	GTM muxed output
	ASCLIN5_ASLSO	O2	Slave select signal output		
	ASCLIN7_ASLSO	O3	Slave select signal output		
	—	O4	Reserved		
	—	O5	Reserved		
	—	O6	Reserved		
	—	O7	Reserved		

表 2-32 端口 P14 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
D12	P14.9	I	LVDS_RX / FAST / PU1 / VEXT / ES	<b>General-purpose input</b>	
	GTM_TIM3_IN3_3			<b>Mux input channel 3 of TIM module 3</b>	
	GTM_TIM2_IN3_3			<b>Mux input channel 3 of TIM module 2</b>	
	ASCLIN0_ACTSA			<b>Clear to send input</b>	
	QSPI2_MRSTFN			<b>Master SPI data input (LVDS N line)</b>	
	ASCLIN9_ARXD			<b>Receive input</b>	
	P14.9			O0	<b>General-purpose output</b>
	GTM_TOUT89	O1	<b>GTM muxed output</b>		
	CAN23_TXD	O2	<b>CAN transmit output node 3</b>		
	MSC0_EN1	O3	<b>Chip Select</b>		
	CAN10_TXD	O4	<b>CAN transmit output node 0</b>		
	ERAY0_TXENB	O5	<b>Transmit Enable Channel B</b>		
	ERAY0_TXENA	O6	<b>Transmit Enable Channel A</b>		
	ERAY1_TXENA	O7	<b>Transmit Enable Channel A</b>		
D11	P14.10	I	LVDS_RX / FAST / PU1 / VEXT / ES	<b>General-purpose input</b>	
	GTM_TIM3_IN4_3			<b>Mux input channel 4 of TIM module 3</b>	
	GTM_TIM2_IN4_3			<b>Mux input channel 4 of TIM module 2</b>	
	CAN23_RXDA			<b>CAN receive input node 3</b>	
	QSPI2_MRSTFP			<b>Master SPI data input (LVDS P line)</b>	
	P14.10			O0	<b>General-purpose output</b>
	GTM_TOUT90			O1	<b>GTM muxed output</b>
	QSPI5_SCLK	O2	<b>Master SPI clock output</b>		
	MSC0_EN0	O3	<b>Chip Select</b>		
	ASCLIN1_ATX	O4	<b>Transmit output</b>		
	IOM_MON2_13		<b>Monitor input 2</b>		
	IOM_REF2_13		<b>Reference input 2</b>		
	CAN02_TXD	O5	<b>CAN transmit output node 2</b>		
	IOM_MON2_7		<b>Monitor input 2</b>		
	IOM_REF2_7		<b>Reference input 2</b>		
	ERAY0_TXDA	O6	<b>Transmit Channel A</b>		
ERAY1_TXDA	O7	<b>Transmit Channel A</b>			

表 2-33 端口 P15 功能

Ball	Symbol	Ctrl.	Buffer Type	Function	
B20	P15.0	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>	
	GTM_TIM3_IN3_4			<b>Mux input channel 3 of TIM module 3</b>	
	GTM_TIM2_IN3_4			<b>Mux input channel 3 of TIM module 2</b>	
	SDMMC0_DAT7_IN			<b>read data in</b>	
	P15.0			O0	<b>General-purpose output</b>
	GTM_TOUT71			O1	<b>GTM muxed output</b>
	ASCLIN1_ATX			O2	<b>Transmit output</b>
	IOM_MON2_13				<b>Monitor input 2</b>
	IOM_REF2_13				<b>Reference input 2</b>
	QSPI0_SLSO13			O3	<b>Master slave select output</b>
	—	O4	<b>Reserved</b>		
	CAN02_TXD	O5	<b>CAN transmit output node 2</b>		
	IOM_MON2_7		<b>Monitor input 2</b>		
	IOM_REF2_7		<b>Reference input 2</b>		
	ASCLIN1_ASCLK	O6	<b>Shift clock output</b>		
	—	O7	<b>Reserved</b>		
	SDMMC0_DAT7	O	<b>write data out</b>		
A18	P15.1	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>	
	GTM_TIM3_IN4_4			<b>Mux input channel 4 of TIM module 3</b>	
	GTM_TIM2_IN4_4			<b>Mux input channel 4 of TIM module 2</b>	
	CAN02_RXDA			<b>CAN receive input node 2</b>	
	ASCLIN1_ARXA			<b>Receive input</b>	
	QSPI2_SLSIB			<b>Slave select input</b>	
	SCU_E_REQ7_2			<b>ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>	
	P15.1			O0	<b>General-purpose output</b>
	GTM_TOUT72			O1	<b>GTM muxed output</b>
	ASCLIN1_ATX			O2	<b>Transmit output</b>
	IOM_MON2_13	<b>Monitor input 2</b>			
	IOM_REF2_13	<b>Reference input 2</b>			
	QSPI2_SLSO5	O3	<b>Master slave select output</b>		
	—	O4	<b>Reserved</b>		
	—	O5	<b>Reserved</b>		
	—	O6	<b>Reserved</b>		
	SDMMC0_CLK	O7	<b>card clock</b>		

表 2-33 端口 P15 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
C19	P15.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN5_4			Mux input channel 5 of TIM module 3
	GTM_TIM2_IN5_4			Mux input channel 5 of TIM module 2
	QSPI2_SLSIA			Slave select input
	SENT_SENT10D			Receive input channel 10
	QSPI2_MRSTE			Master SPI data input
	QSPI2_HSICINA			Highspeed capture channel
	P15.2			O0
	GTM_TOUT73	O1	GTM muxed output	
	ASCLIN0_ATX	O2	Transmit output	
	IOM_MON2_12		Monitor input 2	
	IOM_REF2_12		Reference input 2	
	QSPI2_SLSO0	O3	Master slave select output	
	—	O4	Reserved	
	CAN01_TXD	O5	CAN transmit output node 1	
	IOM_MON2_6		Monitor input 2	
	IOM_REF2_6		Reference input 2	
	ASCLIN0_ASCLK	O6	Shift clock output	
	—	O7	Reserved	
B17	P15.3	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN6_4			Mux input channel 6 of TIM module 3
	GTM_TIM2_IN6_4			Mux input channel 6 of TIM module 2
	CAN01_RXDA			CAN receive input node 1
	ASCLIN0_ARXB			Receive input
	QSPI2_SCLKA			Slave SPI clock inputs
	QSPI2_HSICINB			Highspeed capture channel
	SDMMC0_CMD_IN			command in
	P15.3	O0	General-purpose output	
	GTM_TOUT74	O1	GTM muxed output	
	ASCLIN0_ATX	O2	Transmit output	
	IOM_MON2_12		Monitor input 2	
	IOM_REF2_12		Reference input 2	
	QSPI2_SCLK	O3	Master SPI clock output	
	—	O4	Reserved	
	MSC0_EN1	O5	Chip Select	
	—	O6	Reserved	
	—	O7	Reserved	
	SDMMC0_CMD	O	command out	

表 2-33 端口 P15 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A17	P15.4	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM3_IN7_4			<b>Mux input channel 7 of TIM module 3</b>
	GTM_TIM2_IN7_4			<b>Mux input channel 7 of TIM module 2</b>
	I2C0_SCLC			<b>Serial Clock Input 2</b>
	QSPI2_MRSTA			<b>Master SPI data input</b>
	SCU_E_REQ0_0			<b>ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	SENT_SENT11D			<b>Receive input channel 11</b>
	P15.4			O0
	GTM_TOUT75	O1	<b>GTM muxed output</b>	
	ASCLIN1_ATX	O2	<b>Transmit output</b>	
	IOM_MON2_13		<b>Monitor input 2</b>	
	IOM_REF2_13		<b>Reference input 2</b>	
	QSPI2_MRST	O3	<b>Slave SPI data output</b>	
	IOM_MON2_2		<b>Monitor input 2</b>	
	IOM_REF2_2		<b>Reference input 2</b>	
	—	O4	<b>Reserved</b>	
	—	O5	<b>Reserved</b>	
	I2C0_SCL	O6	<b>Serial Clock Output</b>	
	CCU60_CC62	O7	<b>T12 PWM channel 62</b>	
	IOM_MON1_0		<b>Monitor input 1</b>	
IOM_REF1_4	<b>Reference input 1</b>			

表 2-33 端口 P15 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
E14	P15.5	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM3_IN0_4			<b>Mux input channel 0 of TIM module 3</b>
	GTM_TIM2_IN0_4			<b>Mux input channel 0 of TIM module 2</b>
	ASCLIN1_ARXB			<b>Receive input</b>
	I2C0_SDAC			<b>Serial Data Input 2</b>
	QSPI2_MTSRA			<b>Slave SPI data input</b>
	SCU_E_REQ4_3			<b>ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	P15.5	O0	<b>General-purpose output</b>	
	GTM_TOUT76	O1	<b>GTM muxed output</b>	
	ASCLIN1_ATX	O2	<b>Transmit output</b>	
	IOM_MON2_13		<b>Monitor input 2</b>	
	IOM_REF2_13		<b>Reference input 2</b>	
	QSPI2_MTSR	O3	<b>Master SPI data output</b>	
	—	O4	<b>Reserved</b>	
	MSC0_EN0	O5	<b>Chip Select</b>	
	I2C0_SDA	O6	<b>Serial Data Output</b>	
	CCU60_CC61	O7	<b>T12 PWM channel 61</b>	
	IOM_MON1_1		<b>Monitor input 1</b>	
	IOM_REF1_5		<b>Reference input 1</b>	
A16	P15.6	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM2_IN2_14			<b>Mux input channel 2 of TIM module 2</b>
	GTM_TIM1_IN0_6			<b>Mux input channel 0 of TIM module 1</b>
	GTM_TIM0_IN0_6			<b>Mux input channel 0 of TIM module 0</b>
	QSPI2_MTSRB			<b>Slave SPI data input</b>
	P15.6	O0	<b>General-purpose output</b>	
	GTM_TOUT77	O1	<b>GTM muxed output</b>	
	ASCLIN3_ATX	O2	<b>Transmit output</b>	
	IOM_MON2_15		<b>Monitor input 2</b>	
	IOM_REF2_15		<b>Reference input 2</b>	
	QSPI2_MTSR	O3	<b>Master SPI data output</b>	
	QSPI5_SLSO3	O4	<b>Master slave select output</b>	
	QSPI2_SCLK	O5	<b>Master SPI clock output</b>	
	ASCLIN3_ASCLK	O6	<b>Shift clock output</b>	
	CCU60_CC60	O7	<b>T12 PWM channel 60</b>	
	IOM_MON1_2		<b>Monitor input 1</b>	
	IOM_REF1_6		<b>Reference input 1</b>	

表 2-33 端口 P15 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
D15	P15.7	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN1_5			<b>Mux input channel 1 of TIM module 1</b>
	GTM_TIM0_IN1_5			<b>Mux input channel 1 of TIM module 0</b>
	ASCLIN3_ARXA			<b>Receive input</b>
	QSPI2_MRSTB			<b>Master SPI data input</b>
	P15.7	O0		<b>General-purpose output</b>
	GTM_TOUT78	O1		<b>GTM muxed output</b>
	ASCLIN3_ATX	O2		<b>Transmit output</b>
	IOM_MON2_15			<b>Monitor input 2</b>
	IOM_REF2_15			<b>Reference input 2</b>
	QSPI2_MRST	O3		<b>Slave SPI data output</b>
	IOM_MON2_2			<b>Monitor input 2</b>
	IOM_REF2_2			<b>Reference input 2</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	CCU60_COUT60	O7		<b>T12 PWM channel 60</b>
	IOM_MON1_3			<b>Monitor input 1</b>
IOM_REF1_3	<b>Reference input 1</b>			
D14	P15.8	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN2_5			<b>Mux input channel 2 of TIM module 1</b>
	GTM_TIM0_IN2_5			<b>Mux input channel 2 of TIM module 0</b>
	QSPI2_SCLKB			<b>Slave SPI clock inputs</b>
	SCU_E_REQ5_0			<b>ERU Channel 5 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	P15.8	O0		<b>General-purpose output</b>
	GTM_TOUT79	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	QSPI2_SCLK	O3		<b>Master SPI clock output</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	ASCLIN3_ASCLK	O6		<b>Shift clock output</b>
	CCU60_COUT61	O7		<b>T12 PWM channel 61</b>
	IOM_MON1_4			<b>Monitor input 1</b>
	IOM_REF1_2			<b>Reference input 1</b>

表 2-34 端口 P20 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
H20	P20.0	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN6_7			<b>Mux input channel 6 of TIM module 1</b>
	GTM_TIM1_IN4_9			<b>Mux input channel 4 of TIM module 1</b>
	GTM_TIM0_IN6_7			<b>Mux input channel 6 of TIM module 0</b>
	CAN03_RXDC			<b>CAN receive input node 3</b>
	CCU_PAD_SYSCLK			<b>Sysclk input</b>
	CAN21_RXDC			<b>CAN receive input node 1</b>
	CBS_TGI0			<b>Trigger input</b>
	SCU_E_REQ6_0			<b>ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	GPT120_T6EUDA			<b>Count direction control input of core timer T6</b>
	P20.0	O0	<b>General-purpose output</b>	
	GTM_TOUT59	O1	<b>GTM muxed output</b>	
	ASCLIN3_ATX	O2	<b>Transmit output</b>	
	IOM_MON2_15		<b>Monitor input 2</b>	
	IOM_REF2_15	<b>Reference input 2</b>		
	ASCLIN3_ASCLK	O3	<b>Shift clock output</b>	
	—	O4	<b>Reserved</b>	
	HSCT0_SYSCLK_OUT	O5	<b>sys clock output</b>	
	—	O6	<b>Reserved</b>	
	—	O7	<b>Reserved</b>	
CBS_TGO0	O	<b>Trigger output</b>		
G19	P20.1	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM4_IN4_11			<b>Mux input channel 4 of TIM module 4</b>
	GTM_TIM3_IN3_5			<b>Mux input channel 3 of TIM module 3</b>
	GTM_TIM2_IN3_5			<b>Mux input channel 3 of TIM module 2</b>
	CBS_TGI1			<b>Trigger input</b>
	GTM_DTMA1_1			<b>CDTM1_DTM4</b>
	P20.1	O0	<b>General-purpose output</b>	
	GTM_TOUT60	O1	<b>GTM muxed output</b>	
	—	O2	<b>Reserved</b>	
	—	O3	<b>Reserved</b>	
	—	O4	<b>Reserved</b>	
	—	O5	<b>Reserved</b>	
	—	O6	<b>Reserved</b>	
	—	O7	<b>Reserved</b>	
	CBS_TGO1	O	<b>Trigger output</b>	

表 2-34 端口 P20 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
H19	P20.2	I	S / PU / VEXT	<b>General-purpose input</b> This pin is latched at power on reset release to enter test mode.
	TESTMODE			<b>Testmode Enable Input</b>
G20	P20.3	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM4_IN5_11			<b>Mux input channel 5 of TIM module 4</b>
	GTM_TIM3_IN4_5			<b>Mux input channel 4 of TIM module 3</b>
	GTM_TIM2_IN4_5			<b>Mux input channel 4 of TIM module 2</b>
	ASCLIN3_ARXC			<b>Receive input</b>
	GPT120_T6INA			<b>Trigger/gate input of core timer T6</b>
	P20.3	O0		<b>General-purpose output</b>
	GTM_TOUT61	O1		<b>GTM muxed output</b>
	ASCLIN3_ATX	O2		<b>Transmit output</b>
	IOM_MON2_15			<b>Monitor input 2</b>
	IOM_REF2_15			<b>Reference input 2</b>
	QSPI0_SLSO9	O3		<b>Master slave select output</b>
	QSPI2_SLSO9	O4		<b>Master slave select output</b>
	CAN03_TXD	O5		<b>CAN transmit output node 3</b>
	IOM_MON2_8			<b>Monitor input 2</b>
	IOM_REF2_8			<b>Reference input 2</b>
	CAN21_TXD	O6		<b>CAN transmit output node 1</b>
	—	O7		<b>Reserved</b>
	F17	P20.6	I	SLOW / PU1 / VEXT / ES
GTM_TIM6_IN0_1			<b>Mux input channel 0 of TIM module 6</b>	
GTM_TIM3_IN6_5			<b>Mux input channel 6 of TIM module 3</b>	
GTM_TIM2_IN6_5			<b>Mux input channel 6 of TIM module 2</b>	
CAN12_RXDA			<b>CAN receive input node 2</b>	
ASCLIN9_ARXE			<b>Receive input</b>	
P20.6		O0		<b>General-purpose output</b>
GTM_TOUT62		O1		<b>GTM muxed output</b>
ASCLIN1_ARTS		O2		<b>Ready to send output</b>
QSPI0_SLSO8		O3		<b>Master slave select output</b>
QSPI2_SLSO8		O4		<b>Master slave select output</b>
—		O5		<b>Reserved</b>
—		O6		<b>Reserved</b>
—		O7		<b>Reserved</b>

表 2-34 端口 P20 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
F19	P20.7	I	FAST / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM3_IN7_5			Mux input channel 7 of TIM module 3	
	GTM_TIM2_IN7_5			Mux input channel 7 of TIM module 2	
	GTM_TIM1_IN5_8			Mux input channel 5 of TIM module 1	
	GTM_TIM6_IN1_1			Mux input channel 1 of TIM module 6	
	CAN00_RXDB			CAN receive input node 0	
	ASCLIN1_ACTSA			Clear to send input	
	ASCLIN9_ARXF			Receive input	
	SDMMC0_DAT0_IN			read data in	
	P20.7			O0	General-purpose output
	GTM_TOUT63	O1	GTM muxed output		
	ASCLIN9_ATX	O2	Transmit output		
	—	O3	Reserved		
	—	O4	Reserved		
	CAN12_TXD	O5	CAN transmit output node 2		
	—	O6	Reserved		
	CCU61_COUT63	O7	T13 PWM channel 63		
	IOM_MON1_7		Monitor input 1		
	IOM_REF1_7		Reference input 1		
SDMMC0_DAT0	O	write data out			
F20	P20.8	I	FAST / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM6_IN2_1			Mux input channel 2 of TIM module 6	
	GTM_TIM1_IN7_3			Mux input channel 7 of TIM module 1	
	GTM_TIM0_IN7_3			Mux input channel 7 of TIM module 0	
	SDMMC0_DAT1_IN			read data in	
	P20.8			O0	General-purpose output
	GTM_TOUT64			O1	GTM muxed output
	ASCLIN1_ASLSO			O2	Slave select signal output
	QSPI0_SLSO0			O3	Master slave select output
	QSPI1_SLSO0			O4	Master slave select output
	CAN00_TXD	O5	CAN transmit output node 0		
	IOM_MON2_5		Monitor input 2		
	IOM_REF2_5		Reference input 2		
	—	O6	Reserved		
	CCU61_CC60	O7	T12 PWM channel 60		
	IOM_MON1_8		Monitor input 1		
	IOM_REF1_13		Reference input 1		
	SDMMC0_DAT1	O	write data out		

表 2-34 端口 P20 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
E17	P20.9	I	FAST / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM6_IN3_1			Mux input channel 3 of TIM module 6	
	GTM_TIM3_IN5_5			Mux input channel 5 of TIM module 3	
	GTM_TIM2_IN5_5			Mux input channel 5 of TIM module 2	
	CAN03_RXDE			CAN receive input node 3	
	ASCLIN1_ARXC			Receive input	
	QSPI0_SLSIB			Slave select input	
	SCU_E_REQ7_0			ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)	
	P20.9			O0	General-purpose output
	GTM_TOUT65	O1	GTM muxed output		
	—	O2	Reserved		
	QSPI0_SLSO1	O3	Master slave select output		
	QSPI1_SLSO1	O4	Master slave select output		
	—	O5	Reserved		
	—	O6	Reserved		
	CCU61_CC61	O7	T12 PWM channel 61		
	IOM_MON1_9		Monitor input 1		
	IOM_REF1_12		Reference input 1		
	E19	P20.10	I	FAST / PU1 / VEXT / ES	General-purpose input
GTM_TIM3_IN6_6		Mux input channel 6 of TIM module 3			
GTM_TIM2_IN6_6		Mux input channel 6 of TIM module 2			
SDMMC0_DAT2_IN		read data in			
P20.10		O0			General-purpose output
GTM_TOUT66		O1			GTM muxed output
ASCLIN1_ATX		O2			Transmit output
IOM_MON2_13					Monitor input 2
IOM_REF2_13					Reference input 2
QSPI0_SLSO6			O3	Master slave select output	
QSPI2_SLSO7		O4	Master slave select output		
CAN03_TXD		O5	CAN transmit output node 3		
IOM_MON2_8			Monitor input 2		
IOM_REF2_8			Reference input 2		
ASCLIN1_ASCLK			O6	Shift clock output	
CCU61_CC62		O7	T12 PWM channel 62		
IOM_MON1_10			Monitor input 1		
IOM_REF1_11			Reference input 1		
SDMMC0_DAT2			O	write data out	

表 2-34 端口 P20 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
E20	P20.11	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN7_6			Mux input channel 7 of TIM module 3
	GTM_TIM2_IN7_6			Mux input channel 7 of TIM module 2
	QSPI0_SCLKA			Slave SPI clock inputs
	SDMMC0_DAT3_IN			read data in
	P20.11	00		General-purpose output
	GTM_TOUT67	01		GTM muxed output
	—	02		Reserved
	QSPI0_SCLK	03		Master SPI clock output
	—	04		Reserved
	—	05		Reserved
	—	06		Reserved
	CCU61_COUT60	07		T12 PWM channel 60
	IOM_MON1_11			Monitor input 1
	IOM_REF1_10			Reference input 1
SDMMC0_DAT3	0	write data out		
D19	P20.12	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN0_5			Mux input channel 0 of TIM module 3
	GTM_TIM2_IN0_5			Mux input channel 0 of TIM module 2
	QSPI0_MRSTA			Master SPI data input
	SDMMC0_DAT4_IN			read data in
	IOM_PIN_13	GPIO pad input to FPC		
	P20.12	00		General-purpose output
	GTM_TOUT68	01		GTM muxed output
	IOM_MON0_13	02		Monitor input 0
	—			Reserved
	QSPI0_MRST			Slave SPI data output
	IOM_MON2_0	03		Monitor input 2
	IOM_REF2_0			Reference input 2
	QSPI0_MTSR			Master SPI data output
	—	05		Reserved
	—	06		Reserved
	CCU61_COUT61	07		T12 PWM channel 61
	IOM_MON1_12			Monitor input 1
IOM_REF1_9	Reference input 1			
SDMMC0_DAT4	0	write data out		

表 2-34 端口 P20 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
D20	P20.13	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM3_IN1_4			<b>Mux input channel 1 of TIM module 3</b>
	GTM_TIM2_IN1_4			<b>Mux input channel 1 of TIM module 2</b>
	QSPI0_SLSIA			<b>Slave select input</b>
	SDMMC0_DAT5_IN			<b>read data in</b>
	IOM_PIN_14			<b>GPIO pad input to FPC</b>
	P20.13			O0
	GTM_TOUT69	O1		<b>GTM muxed output</b>
	IOM_MON0_14			<b>Monitor input 0</b>
	—	O2		<b>Reserved</b>
	QSPI0_SLSO2	O3		<b>Master slave select output</b>
	QSPI1_SLSO2	O4		<b>Master slave select output</b>
	QSPI0_SCLK	O5		<b>Master SPI clock output</b>
	—	O6		<b>Reserved</b>
	CCU61_COUT62	O7		<b>T12 PWM channel 62</b>
	IOM_MON1_13			<b>Monitor input 1</b>
	IOM_REF1_8			<b>Reference input 1</b>
SDMMC0_DAT5	O	<b>write data out</b>		
C20	P20.14	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM3_IN2_4			<b>Mux input channel 2 of TIM module 3</b>
	GTM_TIM2_IN2_4			<b>Mux input channel 2 of TIM module 2</b>
	QSPI0_MTSRA			<b>Slave SPI data input</b>
	SDMMC0_DAT6_IN			<b>read data in</b>
	IOM_PIN_15			<b>GPIO pad input to FPC</b>
	P20.14			O0
	GTM_TOUT70	O1		<b>GTM muxed output</b>
	IOM_MON0_15			<b>Monitor input 0</b>
	—	O2		<b>Reserved</b>
	QSPI0_MTSR	O3		<b>Master SPI data output</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	SDMMC0_DAT6	O		<b>write data out</b>

表 2-35 端口 P21 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
K17	P21.0	I	LVDS_RX / FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM4_IN0_11			<b>Mux input channel 0 of TIM module 4</b>
	GTM_TIM3_IN4_6			<b>Mux input channel 4 of TIM module 3</b>
	GTM_TIM2_IN4_6			<b>Mux input channel 4 of TIM module 2</b>
	QSPI4_MRSTDN			<b>Master SPI data input (LVDS N line)</b>
	DMU_FDEST			<b>Enter destructive debug mode</b>
	ASCLIN11_ARXC			<b>Receive input</b>
	HSCT1_RXDN			<b>Rx data</b>
	P21.0	O0	<b>General-purpose output</b>	
	GTM_TOUT51	O1	<b>GTM muxed output</b>	
	ASCLIN11_ATX	O2	<b>Transmit output</b>	
	—	O3	<b>Reserved</b>	
	—	O4	<b>Reserved</b>	
	—	O5	<b>Reserved</b>	
	—	O6	<b>Reserved</b>	
	—	O7	<b>Reserved</b>	
HSM_HSM1	O	<b>Pin Output Value</b>		
J17	P21.1	I	LVDS_RX / FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM4_IN1_13			<b>Mux input channel 1 of TIM module 4</b>
	GTM_TIM3_IN5_6			<b>Mux input channel 5 of TIM module 3</b>
	GTM_TIM2_IN5_6			<b>Mux input channel 5 of TIM module 2</b>
	QSPI4_MRSTDP			<b>Master SPI data input (LVDS P line)</b>
	ASCLIN11_ARXD			<b>Receive input</b>
	HSCT1_RXDP			<b>Rx data</b>
	GTM_DTMA4_1			<b>CDTM4_DTM4</b>
	P21.1	O0	<b>General-purpose output</b>	
	GTM_TOUT52	O1	<b>GTM muxed output</b>	
	—	O2	<b>Reserved</b>	
	—	O3	<b>Reserved</b>	
	—	O4	<b>Reserved</b>	
	—	O5	<b>Reserved</b>	
	—	O6	<b>Reserved</b>	
	—	O7	<b>Reserved</b>	
HSM_HSM2	O	<b>Pin Output Value</b>		

表 2-35 端口 P21 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
K19	P21.2	I	LVDS_RX / FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM5_IN4_11			<b>Mux input channel 4 of TIM module 5</b>
	GTM_TIM1_IN0_7			<b>Mux input channel 0 of TIM module 1</b>
	GTM_TIM0_IN0_7			<b>Mux input channel 0 of TIM module 0</b>
	QSPI2_MRSTCN			<b>Master SPI data input (LVDS N line)</b>
	SCU_EMGSTOP_POR T_B			<b>Emergency stop Port Pin B input request</b>
	ASCLIN3_ARXGN			<b>Differential Receive input (low active)</b>
	HSCT0_RXDN			<b>Rx data</b>
	QSPI4_MRSTCN			<b>Master SPI data input (LVDS N line)</b>
	ASCLIN11_ARXE			<b>Receive input</b>
	GTM_DTMA1_0			<b>CDTM1_DTM4</b>
	P21.2	O0		<b>General-purpose output</b>
	GTM_TOUT53	O1		<b>GTM muxed output</b>
	ASCLIN3_ASLSO	O2		<b>Slave select signal output</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	GETH_MDC	O5		<b>MDIO clock</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
J19	P21.3	I	LVDS_RX / FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM5_IN5_12			<b>Mux input channel 5 of TIM module 5</b>
	GTM_TIM1_IN1_6			<b>Mux input channel 1 of TIM module 1</b>
	GTM_TIM0_IN1_6			<b>Mux input channel 1 of TIM module 0</b>
	QSPI2_MRSTCP			<b>Master SPI data input (LVDS P line)</b>
	ASCLIN3_ARXGP			<b>Differential Receive input (high active)</b>
	GETH_MDIOD			<b>MDIO Input</b>
	HSCT0_RXDP			<b>Rx data</b>
	QSPI4_MRSTCP			<b>Master SPI data input (LVDS P line)</b>
	P21.3	O0		<b>General-purpose output</b>
	GTM_TOUT54	O1		<b>GTM muxed output</b>
	ASCLIN11_ASCLK	O2		<b>Shift clock output</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	GETH_MDIO	O		<b>MDIO Output</b>

表 2-35 端口 P21 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
K20	P21.4	I	LVDS_TX / FAST / PU1 / VEXT / ES6	<b>General-purpose input</b>
	GTM_TIM5_IN6_12			<b>Mux input channel 6 of TIM module 5</b>
	GTM_TIM1_IN2_6			<b>Mux input channel 2 of TIM module 1</b>
	GTM_TIM0_IN2_6			<b>Mux input channel 2 of TIM module 0</b>
	P21.4	O0		<b>General-purpose output</b>
	GTM_TOUT55	O1		<b>GTM muxed output</b>
	ASCLIN11_ASLSO	O2		<b>Slave select signal output</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	HSCT0_TXDN	O		<b>Tx data</b>
J20	P21.5	I	LVDS_TX / FAST / PU1 / VEXT / ES6	<b>General-purpose input</b>
	GTM_TIM5_IN7_11			<b>Mux input channel 7 of TIM module 5</b>
	GTM_TIM1_IN3_6			<b>Mux input channel 3 of TIM module 1</b>
	GTM_TIM0_IN3_6			<b>Mux input channel 3 of TIM module 0</b>
	ASCLIN11_ARXF			<b>Receive input</b>
	P21.5	O0		<b>General-purpose output</b>
	GTM_TOUT56	O1		<b>GTM muxed output</b>
	ASCLIN3_ASCLK	O2		<b>Shift clock output</b>
	ASCLIN11_ATX	O3		<b>Transmit output</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
HSCT0_TXDP	O	<b>Tx data</b>		

表 2-35 端口 P21 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
H17	P21.6/TDI	I	FAST / PD / PU2 / VEXT / ES3	<b>General-purpose input</b> PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ.
	GTM_TIM4_IN2_12			<b>Mux input channel 2 of TIM module 4</b>
	GTM_TIM1_IN4_8			<b>Mux input channel 4 of TIM module 1</b>
	GTM_TIM0_IN4_8			<b>Mux input channel 4 of TIM module 0</b>
	GPT120_T5EUDA			<b>Count direction control input of timer T5</b>
	ASCLIN3_ARXF			<b>Receive input</b>
	CBS_TGI2			<b>Trigger input</b>
	TDI			<b>JTAG Module Data Input</b>
	P21.6	O0	<b>General-purpose output</b>	
	GTM_TOUT57	O1	<b>GTM muxed output</b>	
	ASCLIN3_ASLSO	O2	<b>Slave select signal output</b>	
	—	O3	<b>Reserved</b>	
	—	O4	<b>Reserved</b>	
	—	O5	<b>Reserved</b>	
	—	O6	<b>Reserved</b>	
	GPT120_T3OUT	O7	<b>External output for overflow/underflow detection of core timer T3</b>	
	CBS_TGO2	O	<b>Trigger output</b>	
	DAP3	I/O	<b>DAP: DAP3 Data I/O</b>	
	DAPE1	I/O	<b>DAPE: DAPE1 Data I/O</b>	

表 2-35 端口 P21 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
H16	P21.7/TDO	I	FAST / PU2 / VEXT / ES4	<b>General-purpose input</b>
	GTM_TIM4_IN3_12			<b>Mux input channel 3 of TIM module 4</b>
	GTM_TIM1_IN5_7			<b>Mux input channel 5 of TIM module 1</b>
	GTM_TIM0_IN5_7			<b>Mux input channel 5 of TIM module 0</b>
	GPT120_T5INA			<b>Trigger/gate input of timer T5</b>
	CBS_TGI3			<b>Trigger input</b>
	GETH_RXERB			<b>Receive Error MII</b>
	P21.7	O0		<b>General-purpose output</b>
	GTM_TOUT58	O1		<b>GTM muxed output</b>
	ASCLIN3_ATX	O2		<b>Transmit output</b>
	IOM_MON2_15			<b>Monitor input 2</b>
	IOM_REF2_15			<b>Reference input 2</b>
	ASCLIN3_ASCLK	O3		<b>Shift clock output</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	GPT120_T6OUT	O7		<b>External output for overflow/underflow detection of core timer T6</b>
	CBS_TGO3	O		<b>Trigger output</b>
	DAP2	I/O		<b>DAP: DAP2 Data I/O</b>
	DAPE2	I/O		<b>DAPE: DAPE2 Data I/O</b>
TDO	O	<b>JTAG Module Data Output</b>		

表 2-36 端口 P22 功能

Ball	Symbol	Ctrl.	Buffer Type	Function	
P20	P22.0	I	LVDS_TX / FAST / PU1 / VEXT / ES6	<b>General-purpose input</b>	
	GTM_TIM7_IN3_1			<b>Mux input channel 3 of TIM module 7</b>	
	GTM_TIM1_IN1_7			<b>Mux input channel 1 of TIM module 1</b>	
	GTM_TIM0_IN1_7			<b>Mux input channel 1 of TIM module 0</b>	
	QSPI4_MTSRB			<b>Slave SPI data input</b>	
	ASCLIN6_ARXE			<b>Receive input</b>	
	P22.0			O0	<b>General-purpose output</b>
	GTM_TOUT47			O1	<b>GTM muxed output</b>
	ASCLIN3_ATXN			O2	<b>Differential Transmit output (low active)</b>
	QSPI4_MTSR			O3	<b>Master SPI data output</b>
	QSPI4_SCLKN			O4	<b>Master SPI clock output (LVDS N line)</b>
	MSC1_FCLN			O5	<b>Shift-clock inverted part of the differential signal</b>
	—			O6	<b>Reserved</b>
	ASCLIN6_ATX	O7	<b>Transmit output</b>		
P19	P22.1	I	LVDS_TX / FAST / PU1 / VEXT / ES6	<b>General-purpose input</b>	
	GTM_TIM7_IN2_1			<b>Mux input channel 2 of TIM module 7</b>	
	GTM_TIM1_IN0_8			<b>Mux input channel 0 of TIM module 1</b>	
	GTM_TIM0_IN0_8			<b>Mux input channel 0 of TIM module 0</b>	
	QSPI4_MRSTB			<b>Master SPI data input</b>	
	ASCLIN7_ARXE			<b>Receive input</b>	
	P22.1			O0	<b>General-purpose output</b>
	GTM_TOUT48			O1	<b>GTM muxed output</b>
	ASCLIN3_ATXP			O2	<b>Differential Transmit output (high active)</b>
	QSPI4_MRST			O3	<b>Slave SPI data output</b>
	IOM_MON2_4				<b>Monitor input 2</b>
	IOM_REF2_4				<b>Reference input 2</b>
	QSPI4_SCLKP			O4	<b>Master SPI clock output (LVDS P line)</b>
	MSC1_FCLP	O5	<b>Shift-clock direct part of the differential signal</b>		
—	O6	<b>Reserved</b>			
ASCLIN7_ATX	O7	<b>Transmit output</b>			

表 2-36 端口 P22 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
R20	P22.2	I	LVDS_TX / FAST / PU1 / VEXT / ES6	<b>General-purpose input</b>
	GTM_TIM7_IN1_1			<b>Mux input channel 1 of TIM module 7</b>
	GTM_TIM1_IN3_7			<b>Mux input channel 3 of TIM module 1</b>
	GTM_TIM0_IN3_7			<b>Mux input channel 3 of TIM module 0</b>
	QSPI4_SLSIB			<b>Slave select input</b>
	P22.2	O0		<b>General-purpose output</b>
	GTM_TOUT49	O1		<b>GTM muxed output</b>
	ASCLIN5_ATX	O2		<b>Transmit output</b>
	QSPI4_SLSO3	O3		<b>Master slave select output</b>
	QSPI4_MTSRN	O4		<b>Master SPI data output (LVDS N line)</b>
	MSC1_SON	O5		<b>Data output - inverted part of the differential signal</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	HSCT1_TXDN	O		<b>Tx data</b>
R19	P22.3	I	LVDS_TX / FAST / PU1 / VEXT / ES6	<b>General-purpose input</b>
	GTM_TIM7_IN0_1			<b>Mux input channel 0 of TIM module 7</b>
	GTM_TIM1_IN4_4			<b>Mux input channel 4 of TIM module 1</b>
	GTM_TIM0_IN4_4			<b>Mux input channel 4 of TIM module 0</b>
	QSPI4_SCLKB			<b>Slave SPI clock inputs</b>
	ASCLIN5_ARXC			<b>Receive input</b>
	P22.3	O0		<b>General-purpose output</b>
	GTM_TOUT50	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	QSPI4_SCLK	O3		<b>Master SPI clock output</b>
	QSPI4_MTSRP	O4		<b>Master SPI data output (LVDS P line)</b>
	MSC1_SOP	O5		<b>Data output - direct part of the differential signal</b>
	—	O6		<b>Reserved</b>
	HSPDM_MUTE	O7		<b>Mute output from the micro controller which could be used to control an external Transmitter</b>
HSCT1_TXDP	O		<b>Tx data</b>	

表 2-36 端口 P22 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
P16	P22.4	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM3_IN0_8			<b>Mux input channel 0 of TIM module 3</b>
	ASCLIN7_ARXF			<b>Receive input</b>
	GTM_DTMA3_0			<b>CDTM3_DTM4</b>
	P22.4	O0		<b>General-purpose output</b>
	GTM_TOUT130	O1		<b>GTM muxed output</b>
	ASCLIN4_ASLSO	O2		<b>Slave select signal output</b>
	—	O3		<b>Reserved</b>
	QSPI0_SLSO12	O4		<b>Master slave select output</b>
	—	O5		<b>Reserved</b>
	CAN13_TXD	O6		<b>CAN transmit output node 3</b>
	HSPDM_BS0_OUT	O7		<b>Bit stream 0 output to the pad</b>
P17	P22.5	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM3_IN1_7			<b>Mux input channel 1 of TIM module 3</b>
	QSPI0_MTSRC			<b>Slave SPI data input</b>
	CAN13_RXDC			<b>CAN receive input node 3</b>
	P22.5	O0		<b>General-purpose output</b>
	GTM_TOUT131	O1		<b>GTM muxed output</b>
	ASCLIN4_ATX	O2		<b>Transmit output</b>
	—	O3		<b>Reserved</b>
	QSPI0_MTSR	O4		<b>Master SPI data output</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	HSPDM_BS1_OUT	O7		<b>Bit stream 1 output to the pad</b>

表 2-36 端口 P22 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
N16	P22.6	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN2_6			Mux input channel 2 of TIM module 3
	GTM_TIM2_IN6_14			Mux input channel 6 of TIM module 2
	QSPI0_MRSTC			Master SPI data input
	ASCLIN4_ARXC			Receive input
	P22.6	O0		General-purpose output
	GTM_TOUT132	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	QSPI0_MRST	O4		Slave SPI data output
	IOM_MON2_0			Monitor input 2
	IOM_REF2_0			Reference input 2
	CAN21_TXD	O5		CAN transmit output node 1
	—	O6		Reserved
—	O7	Reserved		
N17	P22.7	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN3_7			Mux input channel 3 of TIM module 3
	QSPI0_SCLKC			Slave SPI clock inputs
	CAN21_RXDF			CAN receive input node 1
	P22.7	O0		General-purpose output
	GTM_TOUT133	O1		GTM muxed output
	ASCLIN4_ASCLK	O2		Shift clock output
	—	O3		Reserved
	QSPI0_SCLK	O4		Master SPI clock output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-36 端口 P22 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
M16	P22.8	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN0_4			Mux input channel 0 of TIM module 5
	GTM_TIM3_IN4_7			Mux input channel 4 of TIM module 3
	QSPI0_SCLKB			Slave SPI clock inputs
	P22.8	O0		General-purpose output
	GTM_TOUT134	O1		GTM muxed output
	ASCLIN5_ASCLK	O2		Shift clock output
	—	O3		Reserved
	QSPI0_SCLK	O4		Master SPI clock output
	CAN22_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
—	O7	Reserved		
M17	P22.9	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN1_10			Mux input channel 1 of TIM module 5
	GTM_TIM3_IN5_7			Mux input channel 5 of TIM module 3
	QSPI0_MRSTB			Master SPI data input
	ASCLIN4_ARXD			Receive input
	CAN22_RXDE			CAN receive input node 2
	GTM_DTMA3_1			CDTM3_DTM4
	P22.9	O0		General-purpose output
	GTM_TOUT135	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	QSPI0_MRST	O4		Slave SPI data output
	IOM_MON2_0			Monitor input 2
	IOM_REF2_0			Reference input 2
	—	O5		Reserved
—	O6	Reserved		
—	O7	Reserved		

表 2-36 端口 P22 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
L16	P22.10	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM5_IN2_8			<b>Mux input channel 2 of TIM module 5</b>
	GTM_TIM3_IN6_7			<b>Mux input channel 6 of TIM module 3</b>
	QSPI0_MTSRB			<b>Slave SPI data input</b>
	P22.10	O0		<b>General-purpose output</b>
	GTM_TOUT136	O1		<b>GTM muxed output</b>
	ASCLIN4_ATX	O2		<b>Transmit output</b>
	—	O3		<b>Reserved</b>
	QSPI0_MTSR	O4		<b>Master SPI data output</b>
	CAN23_TXD	O5		<b>CAN transmit output node 3</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
L17	P22.11	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM5_IN3_10			<b>Mux input channel 3 of TIM module 5</b>
	GTM_TIM3_IN7_7			<b>Mux input channel 7 of TIM module 3</b>
	CAN23_RXDE			<b>CAN receive input node 3</b>
	P22.11	O0		<b>General-purpose output</b>
	GTM_TOUT137	O1		<b>GTM muxed output</b>
	ASCLIN4_ASLSO	O2		<b>Slave select signal output</b>
	—	O3		<b>Reserved</b>
	QSPI0_SLSO10	O4		<b>Master slave select output</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>

表 2-37 端口 P23 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
V20	P23.0	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM6_IN7_1			<b>Mux input channel 7 of TIM module 6</b>
	GTM_TIM1_IN5_4			<b>Mux input channel 5 of TIM module 1</b>
	GTM_TIM0_IN5_4			<b>Mux input channel 5 of TIM module 0</b>
	CAN10_RXDC			<b>CAN receive input node 0</b>
	P23.0	O0		<b>General-purpose output</b>
	GTM_TOUT41	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
U19	P23.1	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM6_IN6_1			<b>Mux input channel 6 of TIM module 6</b>
	GTM_TIM1_IN6_4			<b>Mux input channel 6 of TIM module 1</b>
	GTM_TIM0_IN6_4			<b>Mux input channel 6 of TIM module 0</b>
	MSC1_SDIO			<b>Upstream asynchronous input signal</b>
	ASCLIN6_ARXF			<b>Receive input</b>
	P23.1	O0		<b>General-purpose output</b>
	GTM_TOUT42	O1		<b>GTM muxed output</b>
	ASCLIN1_ARTS	O2		<b>Ready to send output</b>
	QSPI4_SLSO6	O3		<b>Master slave select output</b>
	GTM_CLK0	O4		<b>CGM generated clock</b>
	CAN10_TXD	O5		<b>CAN transmit output node 0</b>
	CCU_EXTCLK0	O6		<b>External Clock 0</b>
	ASCLIN6_ASCLK	O7		<b>Shift clock output</b>

表 2-37 端口 P23 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
U20	P23.2	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM6_IN5_1			Mux input channel 5 of TIM module 6
	GTM_TIM1_IN6_5			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_5			Mux input channel 6 of TIM module 0
	ASCLIN7_ARXC			Receive input
	P23.2	O0		General-purpose output
	GTM_TOUT43	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	CAN23_TXD	O4		CAN transmit output node 3
	CAN12_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	—	O7		Reserved
T19	P23.3	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM6_IN4_2			Mux input channel 4 of TIM module 6
	GTM_TIM1_IN7_4			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_4			Mux input channel 7 of TIM module 0
	MSC1_INJ0			Injection signal from port
	ASCLIN6_ARXA			Receive input
	CAN12_RXDC			CAN receive input node 2
	CAN23_RXDB			CAN receive input node 3
	P23.3	O0		General-purpose output
	GTM_TOUT44	O1		GTM muxed output
	ASCLIN7_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
—	O7	Reserved		

表 2-37 端口 P23 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
T20	P23.4	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM6_IN3_2			<b>Mux input channel 3 of TIM module 6</b>
	GTM_TIM1_IN7_5			<b>Mux input channel 7 of TIM module 1</b>
	GTM_TIM0_IN7_5			<b>Mux input channel 7 of TIM module 0</b>
	P23.4	O0		<b>General-purpose output</b>
	GTM_TOUT45	O1		<b>GTM muxed output</b>
	ASCLIN6_ASLSO	O2		<b>Slave select signal output</b>
	QSPI4_SLSO5	O3		<b>Master slave select output</b>
	—	O4		<b>Reserved</b>
	MSC1_EN0	O5		<b>Chip Select</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
T17	P23.5	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM6_IN2_2			<b>Mux input channel 2 of TIM module 6</b>
	GTM_TIM1_IN2_7			<b>Mux input channel 2 of TIM module 1</b>
	GTM_TIM0_IN2_7			<b>Mux input channel 2 of TIM module 0</b>
	P23.5	O0		<b>General-purpose output</b>
	GTM_TOUT46	O1		<b>GTM muxed output</b>
	ASCLIN6_ATX	O2		<b>Transmit output</b>
	QSPI4_SLSO4	O3		<b>Master slave select output</b>
	—	O4		<b>Reserved</b>
	MSC1_EN1	O5		<b>Chip Select</b>
	CAN22_TXD	O6		<b>CAN transmit output node 2</b>
	—	O7		<b>Reserved</b>
R17	P23.6	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM6_IN1_2			<b>Mux input channel 1 of TIM module 6</b>
	GTM_TIM4_IN2_7			<b>Mux input channel 2 of TIM module 4</b>
	GTM_TIM1_IN2_10			<b>Mux input channel 2 of TIM module 1</b>
	CAN22_RXDC			<b>CAN receive input node 2</b>
	P23.6	O0		<b>General-purpose output</b>
	GTM_TOUT138	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	QSPI0_SLSO11	O4		<b>Master slave select output</b>
	CAN11_TXD	O5		<b>CAN transmit output node 1</b>
	—	O6		<b>Reserved</b>
—	O7	<b>Reserved</b>		

表 2-37 端口 P23 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
R16	P23.7	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM6_IN0_2			<b>Mux input channel 0 of TIM module 6</b>
	GTM_TIM4_IN3_7			<b>Mux input channel 3 of TIM module 4</b>
	GTM_TIM1_IN3_10			<b>Mux input channel 3 of TIM module 1</b>
	CAN11_RXDC			<b>CAN receive input node 1</b>
	P23.7	O0		<b>General-purpose output</b>
	GTM_TOUT139	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>

表 2-38 端口 P32 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
Y17	P32.0	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b> P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
	GTM_TIM3_IN2_5			<b>Mux input channel 2 of TIM module 3</b>
	GTM_TIM2_IN2_5			<b>Mux input channel 2 of TIM module 2</b>
	P32.0	O0		<b>General-purpose output</b>
	GTM_TOUT36	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>

表 2-38 端口 P32 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
W17	P32.1	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b> P32.1 / External Pass Device gate control for EVRC
	GTM_TIM3_IN3_15			<b>Mux input channel 3 of TIM module 3</b>
	P32.1	O0		<b>General-purpose output</b>
	GTM_TOUT37	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
—	O7	<b>Reserved</b>		
Y18	P32.2	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN3_8			<b>Mux input channel 3 of TIM module 1</b>
	GTM_TIM0_IN3_8			<b>Mux input channel 3 of TIM module 0</b>
	CAN03_RXDB			<b>CAN receive input node 3</b>
	ASCLIN3_ARXD			<b>Receive input</b>
	CAN21_RXDD			<b>CAN receive input node 1</b>
	P32.2	O0		<b>General-purpose output</b>
	GTM_TOUT38	O1		<b>GTM muxed output</b>
	ASCLIN3_ATX	O2		<b>Transmit output</b>
	IOM_MON2_15			<b>Monitor input 2</b>
	IOM_REF2_15			<b>Reference input 2</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	PMS_DCDCSYNCO	O6		<b>DC-DC synchronization output</b>
—	O7	<b>Reserved</b>		

表 2-38 端口 P32 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y19	P32.3	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN4_5			<b>Mux input channel 4 of TIM module 1</b>
	GTM_TIM0_IN4_5			<b>Mux input channel 4 of TIM module 0</b>
	P32.3	O0		<b>General-purpose output</b>
	GTM_TOUT39	O1		<b>GTM muxed output</b>
	ASCLIN3_ATX	O2		<b>Transmit output</b>
	IOM_MON2_15			<b>Monitor input 2</b>
	IOM_REF2_15	O3		<b>Reference input 2</b>
	—			<b>Reserved</b>
	ASCLIN3_ASCLK			<b>Shift clock output</b>
	CAN03_TXD	O5		<b>CAN transmit output node 3</b>
	IOM_MON2_8			<b>Monitor input 2</b>
	IOM_REF2_8			<b>Reference input 2</b>
	CAN21_TXD	O6		<b>CAN transmit output node 1</b>
	—	O7		<b>Reserved</b>
W18	P32.4	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN5_5			<b>Mux input channel 5 of TIM module 1</b>
	GTM_TIM0_IN5_5			<b>Mux input channel 5 of TIM module 0</b>
	ASCLIN1_ACTSB			<b>Clear to send input</b>
	MSC1_SDI2			<b>Upstream asynchronous input signal</b>
	P32.4	O0		<b>General-purpose output</b>
	GTM_TOUT40	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	GTM_CLK1	O4		<b>CGM generated clock</b>
	MSC1_EN0	O5		<b>Chip Select</b>
	CCU_EXTCLK1	O6		<b>External Clock 1</b>
	CCU60_COUT63			<b>T13 PWM channel 63</b>
	IOM_MON1_6	O7		<b>Monitor input 1</b>
	IOM_REF1_0			<b>Reference input 1</b>
PMS_DCDCSYNCO	O		<b>DC-DC synchronization output</b>	

表 2-38 端口 P32 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
T15	P32.5	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN5_9			Mux input channel 5 of TIM module 5
	GTM_TIM4_IN1_14			Mux input channel 1 of TIM module 4
	GTM_TIM3_IN5_8			Mux input channel 5 of TIM module 3
	SENT_SENT10C			Receive input channel 10
	P32.5	O0		General-purpose output
	GTM_TOUT140	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	CAN02_TXD	O6		CAN transmit output node 2
	IOM_MON2_7			Monitor input 2
	IOM_REF2_7			Reference input 2
—	O7	Reserved		
U15	P32.6	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN6_9			Mux input channel 6 of TIM module 5
	GTM_TIM4_IN4_15			Mux input channel 4 of TIM module 4
	GTM_TIM3_IN6_8			Mux input channel 6 of TIM module 3
	CAN02_RXDC			CAN receive input node 2
	CBS_TGI4			Trigger input
	ASCLIN2_ARXF			Receive input
	ASCLIN6_ARXC			Receive input
	SENT_SENT11C			Receive input channel 11
	P32.6			O0
	GTM_TOUT141	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	QSPI2_SLSO12	O4		Master slave select output
	CAN22_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
—	O7	Reserved		
CBS_TGO4	O	Trigger output		

表 2-38 端口 P32 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
U16	P32.7	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM5_IN7_8			<b>Mux input channel 7 of TIM module 5</b>
	GTM_TIM4_IN0_15			<b>Mux input channel 0 of TIM module 4</b>
	GTM_TIM3_IN7_8			<b>Mux input channel 7 of TIM module 3</b>
	CBS_TGI5			<b>Trigger input</b>
	CAN22_RXDB			<b>CAN receive input node 2</b>
	SENT_SENT12C			<b>Receive input channel 12</b>
	P32.7			O0
	GTM_TOUT142	O1		<b>GTM muxed output</b>
	ASCLIN6_ATX	O2		<b>Transmit output</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	CBS_TGO5	O		<b>Trigger output</b>

表 2-39 端口 P33 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
W10	P33.0	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM3_IN0_13			<b>Mux input channel 0 of TIM module 3</b>
	GTM_TIM1_IN4_6			<b>Mux input channel 4 of TIM module 1</b>
	GTM_TIM0_IN4_6			<b>Mux input channel 4 of TIM module 0</b>
	EDSADC_ITR0E			<b>Trigger/Gate input, channel 0</b>
	SENT_SENT13C			<b>Receive input channel 13</b>
	IOM_PIN_0			<b>GPIO pad input to FPC</b>
	GTM_DTMT1_2			<b>CDTM1_DTM0</b>
	EVADC_G10CH7	AI		<b>Analog input channel 7, group 10</b>
	EVADC_FC7CH0			<b>Analog input FC channel 7</b>
	P33.0	O0		<b>General-purpose output</b>
	GTM_TOUT22	O1		<b>GTM muxed output</b>
	IOM_MON0_0			<b>Monitor input 0</b>
	IOM_GTM_0		<b>GTM-provided inputs to EXOR combiner</b>	
	ASCLIN5_ATX	O2	<b>Transmit output</b>	
	—	O3	<b>Reserved</b>	
	—	O4	<b>Reserved</b>	
	—	O5	<b>Reserved</b>	
	EVADC_FC2BFLOUT	O6	<b>Boundary flag output, FC channel 2</b>	
	—	O7	<b>Reserved</b>	

表 2-39 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y10	P33.1	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM3_IN1_15			<b>Mux input channel 1 of TIM module 3</b>
	GTM_TIM1_IN5_6			<b>Mux input channel 5 of TIM module 1</b>
	GTM_TIM0_IN5_6			<b>Mux input channel 5 of TIM module 0</b>
	EDSADC_ITR1E			<b>Trigger/Gate input, channel 1</b>
	PSI5_RX0C			<b>RXD inputs (receive data) channel 0</b>
	EDSADC_DSCIN2B			<b>Modulator clock input, channel 2</b>
	SENT_SENT9C			<b>Receive input channel 9</b>
	ASCLIN8_ARXC			<b>Receive input</b>
	IOM_PIN_1			<b>GPIO pad input to FPC</b>
	EVADC_G10CH6			AI
	EVADC_FC6CH0	<b>Analog input FC channel 6</b>		
	P33.1	O0	<b>General-purpose output</b>	
	GTM_TOUT23	O1	<b>GTM muxed output</b>	
	IOM_MON0_1		<b>Monitor input 0</b>	
	IOM_GTM_1		<b>GTM-provided inputs to EXOR combiner</b>	
	ASCLIN3_ASLSO	O2	<b>Slave select signal output</b>	
	QSPI2_SCLK	O3	<b>Master SPI clock output</b>	
	EDSADC_DSCOUT2	O4	<b>Modulator clock output</b>	
	EVADC_EMUX02	O5	<b>Control of external analog multiplexer interface 0</b>	
	EVADC_FC4BFLOUT	O6	<b>Boundary flag output, FC channel 4</b>	
	—	O7	<b>Reserved</b>	

表 2-39 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
W11	P33.2	I	SLOW / PU1 / VEVR SB / ES5	<b>General-purpose input</b>
	GTM_TIM3_IN2_14			<b>Mux input channel 2 of TIM module 3</b>
	GTM_TIM1_IN6_6			<b>Mux input channel 6 of TIM module 1</b>
	GTM_TIM0_IN6_6			<b>Mux input channel 6 of TIM module 0</b>
	EDSADC_ITR2E			<b>Trigger/Gate input, channel 2</b>
	SENT_SENT8C			<b>Receive input channel 8</b>
	EDSADC_DSDIN2B			<b>Digital datastream input, channel 2</b>
	IOM_PIN_2			<b>GPIO pad input to FPC</b>
	EVADC_G10CH5			AI
	EVADC_FC5CH0	<b>Analog input FC channel 5</b>		
	P33.2	O0	<b>General-purpose output</b>	
	GTM_TOUT24	O1	<b>GTM muxed output</b>	
	IOM_MON0_2		<b>Monitor input 0</b>	
	IOM_GTM_2		<b>GTM-provided inputs to EXOR combiner</b>	
	ASCLIN3_ASCLK	O2	<b>Shift clock output</b>	
	QSPI2_SLSO10	O3	<b>Master slave select output</b>	
	PSI5_TX0	O4	<b>TXD outputs (send data)</b>	
	IOM_MON1_14		<b>Monitor input 1</b>	
	IOM_REF1_14		<b>Reference input 1</b>	
	EVADC_EMUX01	O5	<b>Control of external analog multiplexer interface 0</b>	
	EVADC_FC3BFLOUT	O6	<b>Boundary flag output, FC channel 3</b>	
	—	O7	<b>Reserved</b>	

表 2-39 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y11	P33.3	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM3_IN3_12			<b>Mux input channel 3 of TIM module 3</b>
	GTM_TIM1_IN7_6			<b>Mux input channel 7 of TIM module 1</b>
	GTM_TIM0_IN7_6			<b>Mux input channel 7 of TIM module 0</b>
	PSI5_RX1C			<b>RXD inputs (receive data) channel 1</b>
	SENT_SENT7C			<b>Receive input channel 7</b>
	EDSADC_DSCIN1B			<b>Modulator clock input, channel 1</b>
	IOM_PIN_3			<b>GPIO pad input to FPC</b>
	EVADC_G10CH4			AI
	EVADC_FC4CH0	<b>Analog input FC channel 4</b>		
	P33.3	O0	<b>General-purpose output</b>	
	GTM_TOUT25	O1	<b>GTM muxed output</b>	
	IOM_MON0_3		<b>Monitor input 0</b>	
	IOM_GTM_3		<b>GTM-provided inputs to EXOR combiner</b>	
	ASCLIN5_ASCLK	O2	<b>Shift clock output</b>	
	QSPI4_SLSO2	O3	<b>Master slave select output</b>	
	EDSADC_DSCOUT1	O4	<b>Modulator clock output</b>	
	EVADC_EMUX00	O5	<b>Control of external analog multiplexer interface 0</b>	
	EVADC_FC5BFLOUT	O6	<b>Boundary flag output, FC channel 5</b>	
	—	O7	<b>Reserved</b>	

表 2-39 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
W12	P33.4	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM4_IN4_10			<b>Mux input channel 4 of TIM module 4</b>
	GTM_TIM1_IN0_10			<b>Mux input channel 0 of TIM module 1</b>
	GTM_TIM0_IN0_10			<b>Mux input channel 0 of TIM module 0</b>
	EDSADC_ITR0F			<b>Trigger/Gate input, channel 0</b>
	SENT_SENT6C			<b>Receive input channel 6</b>
	EDSADC_DSDIN1B			<b>Digital datastream input, channel 1</b>
	CCU61_CTRAPC			<b>Trap input capture</b>
	ASCLIN5_ARXB			<b>Receive input</b>
	IOM_PIN_4			<b>GPIO pad input to FPC</b>
	GTM_DTMT2_0			<b>CDTM2_DTM0</b>
	EVADC_G10CH3	AI	<b>Analog input channel 3, group 10</b>	
	P33.4	O0	<b>General-purpose output</b>	
	GTM_TOUT26	O1	<b>GTM muxed output</b>	
	IOM_MON0_4		<b>Monitor input 0</b>	
	IOM_GTM_4		<b>GTM-provided inputs to EXOR combiner</b>	
	ASCLIN2_ARTS	O2	<b>Ready to send output</b>	
	QSPI2_SLSO12	O3	<b>Master slave select output</b>	
	PSI5_TX1	O4	<b>TXD outputs (send data)</b>	
	IOM_MON1_15		<b>Monitor input 1</b>	
	EVADC_EMUX12		<b>Control of external analog multiplexer interface 1</b>	
	EVADC_FC0BFLOUT	O6	<b>Boundary flag output, FC channel 0</b>	
	CAN13_TXD	O7	<b>CAN transmit output node 3</b>	

表 2-39 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y12	P33.5	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM4_IN5_10			<b>Mux input channel 5 of TIM module 4</b>
	GTM_TIM1_IN1_8			<b>Mux input channel 1 of TIM module 1</b>
	GTM_TIM0_IN1_8			<b>Mux input channel 1 of TIM module 0</b>
	EDSADC_DSCIN0B			<b>Modulator clock input, channel 0</b>
	EDSADC_ITR1F			<b>Trigger/Gate input, channel 1</b>
	GPT120_T4EUDB			<b>Count direction control input of timer T4</b>
	PSI5S_RXC			<b>RX data input</b>
	ASCLIN2_ACTSB			<b>Clear to send input</b>
	CCU61_CCPOS2C			<b>Hall capture input 2</b>
	PSI5_RX2C			<b>RXD inputs (receive data) channel 2</b>
	SENT_SENT5C			<b>Receive input channel 5</b>
	CAN13_RXDB			<b>CAN receive input node 3</b>
	IOM_PIN_5			<b>GPIO pad input to FPC</b>
	EVADC_G10CH2	AI	<b>Analog input channel 2, group 10</b>	
	P33.5	O0	<b>General-purpose output</b>	
	GTM_TOUT27	O1	<b>GTM muxed output</b>	
	IOM_MON0_5	O1	<b>Monitor input 0</b>	
	IOM_GTM_5		<b>GTM-provided inputs to EXOR combiner</b>	
	QSPI0_SLSO7	O2	<b>Master slave select output</b>	
	QSPI1_SLSO7	O3	<b>Master slave select output</b>	
	EDSADC_DSCOUT0	O4	<b>Modulator clock output</b>	
	EVADC_EMUX11	O5	<b>Control of external analog multiplexer interface 1</b>	
EVADC_FC2BFLOUT	O6	<b>Boundary flag output, FC channel 2</b>		
ASCLIN5_ASLSO	O7	<b>Slave select signal output</b>		

表 2-39 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
W13	P33.6	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM1_IN2_9			<b>Mux input channel 2 of TIM module 1</b>
	GTM_TIM0_IN2_9			<b>Mux input channel 2 of TIM module 0</b>
	EDSADC_ITR2F			<b>Trigger/Gate input, channel 2</b>
	GPT120_T2EUDB			<b>Count direction control input of timer T2</b>
	SENT_SENT4C			<b>Receive input channel 4</b>
	CCU61_CCPOS1C			<b>Hall capture input 1</b>
	EDSADC_DSDIN0B			<b>Digital datastream input, channel 0</b>
	ASCLIN8_ARXD			<b>Receive input</b>
	IOM_PIN_6			<b>GPIO pad input to FPC</b>
	GTM_DTMT2_1			<b>CDTM2_DTM0</b>
	EVADC_G10CH1			AI
	P33.6	O0	<b>General-purpose output</b>	
	GTM_TOUT28	O1	<b>GTM muxed output</b>	
	IOM_MON0_6		<b>Monitor input 0</b>	
	IOM_GTM_6		<b>GTM-provided inputs to EXOR combiner</b>	
	ASCLIN2_ASLSO	O2	<b>Slave select signal output</b>	
	QSPI2_SLSO11	O3	<b>Master slave select output</b>	
	PSI5_TX2	O4	<b>TXD outputs (send data)</b>	
	IOM_REF1_15		<b>Reference input 1</b>	
	EVADC_EMUX10	O5	<b>Control of external analog multiplexer interface 1</b>	
	EVADC_FC1BFLOUT	O6	<b>Boundary flag output, FC channel 1</b>	
	PSI5S_TX	O7	<b>TX data output</b>	

表 2-39 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y13	P33.7	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM1_IN3_9			<b>Mux input channel 3 of TIM module 1</b>
	GTM_TIM0_IN3_9			<b>Mux input channel 3 of TIM module 0</b>
	CAN00_RXDE			<b>CAN receive input node 0</b>
	GPT120_T2INB			<b>Trigger/gate input of timer T2</b>
	CCU61_CCPOS0C			<b>Hall capture input 0</b>
	SCU_E_REQ4_0			<b>ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	SENT_SENT14C			<b>Receive input channel 14</b>
	IOM_PIN_7			<b>GPIO pad input to FPC</b>
	EVADC_G10CH0	AI	<b>Analog input channel 0, group 10</b>	
	P33.7	O0	<b>General-purpose output</b>	
	GTM_TOUT29	O1	<b>GTM muxed output</b>	
	IOM_MON0_7		<b>Monitor input 0</b>	
	IOM_GTM_7		<b>GTM-provided inputs to EXOR combiner</b>	
	ASCLIN2_ASCLK	O2	<b>Shift clock output</b>	
	QSPI4_SLSO7	O3	<b>Master slave select output</b>	
	ASCLIN8_ATX	O4	<b>Transmit output</b>	
	—	O5	<b>Reserved</b>	
	EVADC_FC3BFLOUT	O6	<b>Boundary flag output, FC channel 3</b>	
	—	O7	<b>Reserved</b>	

表 2-39 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
W14	P33.8	I	FAST / HighZ / VEVR SB	<b>General-purpose input</b>
	GTM_TIM1_IN4_7			<b>Mux input channel 4 of TIM module 1</b>
	GTM_TIM0_IN4_7			<b>Mux input channel 4 of TIM module 0</b>
	ASCLIN2_ARXE			<b>Receive input</b>
	SCU_EMGSTOP_POR T_A			<b>Emergency stop Port Pin A input request</b>
	IOM_PIN_8			<b>GPIO pad input to FPC</b>
	P33.8	O0		<b>General-purpose output</b>
	GTM_TOUT30	O1		<b>GTM muxed output</b>
	IOM_MON0_8			<b>Monitor input 0</b>
	ASCLIN2_ATX	O2		<b>Transmit output</b>
	IOM_MON2_14			<b>Monitor input 2</b>
	IOM_REF2_14			<b>Reference input 2</b>
	QSPI4_SLSO2	O3		<b>Master slave select output</b>
	—	O4		<b>Reserved</b>
	CAN00_TXD	O5		<b>CAN transmit output node 0</b>
	IOM_MON2_5			<b>Monitor input 2</b>
	IOM_REF2_5			<b>Reference input 2</b>
	—	O6		<b>Reserved</b>
	CCU61_COUT62	O7		<b>T12 PWM channel 62</b>
	IOM_MON1_13			<b>Monitor input 1</b>
IOM_REF1_8	<b>Reference input 1</b>			
SMU_FSP0	O	<b>FSP[1..0] Output Signals - Generated by SMU_core</b>		

表 2-39 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y14	P33.9	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM1_IN1_9			<b>Mux input channel 1 of TIM module 1</b>
	GTM_TIM0_IN1_9			<b>Mux input channel 1 of TIM module 0</b>
	QSPI3_HSICINA			<b>Highspeed capture channel</b>
	IOM_PIN_9			<b>GPIO pad input to FPC</b>
	P33.9	O0		<b>General-purpose output</b>
	GTM_TOUT31	O1		<b>GTM muxed output</b>
	IOM_MON0_9			<b>Monitor input 0</b>
	ASCLIN2_ATX	O2		<b>Transmit output</b>
	IOM_MON2_14			<b>Monitor input 2</b>
	IOM_REF2_14			<b>Reference input 2</b>
	QSPI4_SLSO1	O3		<b>Master slave select output</b>
	ASCLIN2_ASCLK	O4		<b>Shift clock output</b>
	CAN01_TXD	O5		<b>CAN transmit output node 1</b>
	IOM_MON2_6			<b>Monitor input 2</b>
	IOM_REF2_6			<b>Reference input 2</b>
	ASCLIN0_ATX	O6		<b>Transmit output</b>
	IOM_MON2_12			<b>Monitor input 2</b>
	IOM_REF2_12			<b>Reference input 2</b>
	CCU61_CC62	O7		<b>T12 PWM channel 62</b>
	IOM_MON1_10			<b>Monitor input 1</b>
	IOM_REF1_11			<b>Reference input 1</b>

表 2-39 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
W15	P33.10	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM4_IN4_14			Mux input channel 4 of TIM module 4
	GTM_TIM1_IN0_9			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_9			Mux input channel 0 of TIM module 0
	QSPI4_SLSIA			Slave select input
	QSPI3_HSICINB			Highspeed capture channel
	CAN01_RXDD			CAN receive input node 1
	ASCLIN0_ARXD			Receive input
	IOM_PIN_10			GPIO pad input to FPC
	P33.10			O0
	GTM_TOUT32	O1	GTM muxed output	
	IOM_MON0_10	O2	Monitor input 0	
	QSPI1_SLSO6		Master slave select output	
	QSPI4_SLSO0	O3	Master slave select output	
	ASCLIN1_ASLSO	O4	Slave select signal output	
	PSI5S_CLK	O5	PSI5S CLK is a clock that can be used on a pin to drive the external PHY.	
	—	O6	Reserved	
	CCU61_COUT61	O7	T12 PWM channel 61	
	IOM_MON1_12	O	Monitor input 1	
	IOM_REF1_9		Reference input 1	
SMU_FSP1		FSP[1..0] Output Signals - Generated by SMU_core		
Y15	P33.11	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN2_8			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_8			Mux input channel 2 of TIM module 0
	QSPI4_SCLKA			Slave SPI clock inputs
	IOM_PIN_11			GPIO pad input to FPC
	P33.11	O0	General-purpose output	
	GTM_TOUT33	O1	GTM muxed output	
	IOM_MON0_11	O2	Monitor input 0	
	ASCLIN1_ASCLK		Shift clock output	
	QSPI4_SCLK	O3	Master SPI clock output	
	—	O4	Reserved	
	—	O5	Reserved	
	EDSADC_CGPWMN	O6	Negative carrier generator output	
	CCU61_CC61	O7	T12 PWM channel 61	
	IOM_MON1_9	O	Monitor input 1	
IOM_REF1_12	Reference input 1			

表 2-39 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
W16	P33.12	I	FAST / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM3_IN0_6			<b>Mux input channel 0 of TIM module 3</b>
	GTM_TIM2_IN0_6			<b>Mux input channel 0 of TIM module 2</b>
	QSPI4_MTSRA			<b>Slave SPI data input</b>
	CAN00_RXDD			<b>CAN receive input node 0</b>
	PMS_PINBWKP			<b>PINB (P33.12) pin input</b>
	IOM_PIN_12			<b>GPIO pad input to FPC</b>
	P33.12			O0
	GTM_TOUT34	O1		<b>GTM muxed output</b>
	IOM_MON0_12			<b>Monitor input 0</b>
	ASCLIN1_ATX	O2		<b>Transmit output</b>
	IOM_MON2_13			<b>Monitor input 2</b>
	IOM_REF2_13			<b>Reference input 2</b>
	QSPI4_MTSR	O3		<b>Master SPI data output</b>
	ASCLIN1_ASCLK	O4		<b>Shift clock output</b>
	CAN22_TXD	O5		<b>CAN transmit output node 2</b>
	EDSADC_CGPWMP	O6		<b>Positive carrier generator output</b>
	CCU61_COUT60	O7		<b>T12 PWM channel 60</b>
	IOM_MON1_11			<b>Monitor input 1</b>
	IOM_REF1_10			<b>Reference input 1</b>

表 2-39 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y16	P33.13	I	FAST / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM3_IN1_5			<b>Mux input channel 1 of TIM module 3</b>
	GTM_TIM2_IN1_5			<b>Mux input channel 1 of TIM module 2</b>
	ASCLIN1_ARXF			<b>Receive input</b>
	EDSADC_SGNB			<b>Carrier sign signal input</b>
	QSPI4_MRSTA			<b>Master SPI data input</b>
	MSC1_INJ1			<b>Injection signal from port</b>
	CAN22_RXDA			<b>CAN receive input node 2</b>
	P33.13			O0
	GTM_TOUT35	O1	<b>GTM muxed output</b>	
	ASCLIN1_ATX	O2	<b>Transmit output</b>	
	IOM_MON2_13		<b>Monitor input 2</b>	
	IOM_REF2_13		<b>Reference input 2</b>	
	QSPI4_MRST	O3	<b>Slave SPI data output</b>	
	IOM_MON2_4		<b>Monitor input 2</b>	
	IOM_REF2_4		<b>Reference input 2</b>	
	QSPI2_SLSO6	O4	<b>Master slave select output</b>	
	CAN00_TXD	O5	<b>CAN transmit output node 0</b>	
	IOM_MON2_5		<b>Monitor input 2</b>	
	IOM_REF2_5		<b>Reference input 2</b>	
	—	O6	<b>Reserved</b>	
	CCU61_CC60	O7	<b>T12 PWM channel 60</b>	
	IOM_MON1_8		<b>Monitor input 1</b>	
	IOM_REF1_13		<b>Reference input 1</b>	

表 2-39 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
T14	P33.14	I	FAST / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM5_IN0_8			<b>Mux input channel 0 of TIM module 5</b>
	GTM_TIM4_IN5_14			<b>Mux input channel 5 of TIM module 4</b>
	GTM_TIM2_IN0_8			<b>Mux input channel 0 of TIM module 2</b>
	QSPI2_SCLKD			<b>Slave SPI clock inputs</b>
	CBS_TGI6			<b>Trigger input</b>
	P33.14	O0		<b>General-purpose output</b>
	GTM_TOUT143	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	QSPI2_SCLK	O3		<b>Master SPI clock output</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	CCU60_CC62	O7		<b>T12 PWM channel 62</b>
	IOM_MON1_0			<b>Monitor input 1</b>
	IOM_REF1_4			<b>Reference input 1</b>
CBS_TGO6	O	<b>Trigger output</b>		
U14	P33.15	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM5_IN1_9			<b>Mux input channel 1 of TIM module 5</b>
	GTM_TIM4_IN6_12			<b>Mux input channel 6 of TIM module 4</b>
	GTM_TIM2_IN1_7			<b>Mux input channel 1 of TIM module 2</b>
	CBS_TGI7			<b>Trigger input</b>
	P33.15	O0		<b>General-purpose output</b>
	GTM_TOUT144	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	QSPI2_SLSO11	O3		<b>Master slave select output</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	CCU60_COUT62	O7		<b>T12 PWM channel 62</b>
	IOM_MON1_5			<b>Monitor input 1</b>
	IOM_REF1_1			<b>Reference input 1</b>
	CBS_TGO7	O		<b>Trigger output</b>

表 2-40 端口 P34 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
U11	P34.1	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM5_IN3_9			<b>Mux input channel 3 of TIM module 5</b>
	GTM_TIM3_IN4_12			<b>Mux input channel 4 of TIM module 3</b>
	GTM_TIM2_IN3_9			<b>Mux input channel 3 of TIM module 2</b>
	EVADC_G10CH11	AI		<b>Analog input channel 11, group 10</b>
	P34.1	O0		<b>General-purpose output</b>
	GTM_TOUT146	O1		<b>GTM muxed output</b>
	ASCLIN4_ATX	O2		<b>Transmit output</b>
	—	O3		<b>Reserved</b>
	CAN00_TXD	O4		<b>CAN transmit output node 0</b>
	IOM_MON2_5			<b>Monitor input 2</b>
	IOM_REF2_5			<b>Reference input 2</b>
	CAN20_TXD	O5		<b>CAN transmit output node 0</b>
	—	O6		<b>Reserved</b>
	CCU60_COUT63	O7		<b>T13 PWM channel 63</b>
	IOM_MON1_6		<b>Monitor input 1</b>	
IOM_REF1_0		<b>Reference input 1</b>		
T12	P34.2	I	SLOW / PU1 / VEVRSB / ES	<b>General-purpose input</b>
	GTM_TIM5_IN4_9			<b>Mux input channel 4 of TIM module 5</b>
	GTM_TIM3_IN5_13			<b>Mux input channel 5 of TIM module 3</b>
	GTM_TIM2_IN4_8			<b>Mux input channel 4 of TIM module 2</b>
	ASCLIN4_ARXB			<b>Receive input</b>
	CAN00_RXDG			<b>CAN receive input node 0</b>
	CAN20_RXDC			<b>CAN receive input node 0</b>
	EVADC_G10CH10	AI		<b>Analog input channel 10, group 10</b>
	P34.2	O0		<b>General-purpose output</b>
	GTM_TOUT147	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	CCU60_CC60	O7	<b>T12 PWM channel 60</b>	
IOM_MON1_2		<b>Monitor input 1</b>		
IOM_REF1_6		<b>Reference input 1</b>		

表 2-40 端口 P34 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
U12	P34.3	I	SLOW / PU1 / VEVRSB / ES	<b>General-purpose input</b>
	GTM_TIM5_IN5_10			<b>Mux input channel 5 of TIM module 5</b>
	GTM_TIM3_IN6_13			<b>Mux input channel 6 of TIM module 3</b>
	GTM_TIM2_IN5_9			<b>Mux input channel 5 of TIM module 2</b>
	EVADC_G10CH9	AI		<b>Analog input channel 9, group 10</b>
	P34.3	O0		<b>General-purpose output</b>
	GTM_TOUT148	O1		<b>GTM muxed output</b>
	ASCLIN4_ASCLK	O2		<b>Shift clock output</b>
	—	O3		<b>Reserved</b>
	QSPI2_SLSO10	O4		<b>Master slave select output</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	CCU60_COUT60	O7		<b>T12 PWM channel 60</b>
	IOM_MON1_3			<b>Monitor input 1</b>
IOM_REF1_3	<b>Reference input 1</b>			
T13	P34.4	I	SLOW / PU1 / VEVRSB / ES	<b>General-purpose input</b>
	GTM_TIM5_IN6_10			<b>Mux input channel 6 of TIM module 5</b>
	GTM_TIM3_IN7_12			<b>Mux input channel 7 of TIM module 3</b>
	GTM_TIM2_IN6_8			<b>Mux input channel 6 of TIM module 2</b>
	QSPI2_MRSTD			<b>Master SPI data input</b>
	EVADC_G10CH8	AI		<b>Analog input channel 8, group 10</b>
	P34.4	O0		<b>General-purpose output</b>
	GTM_TOUT149	O1		<b>GTM muxed output</b>
	ASCLIN4_ASLSO	O2		<b>Slave select signal output</b>
	—	O3		<b>Reserved</b>
	QSPI2_MRST	O4		<b>Slave SPI data output</b>
	IOM_MON2_2			<b>Monitor input 2</b>
	IOM_REF2_2			<b>Reference input 2</b>
	—	O5		<b>Reserved</b>
	EVADC_FC6BFLOUT	O6		<b>Boundary flag output, FC channel 6</b>
	CCU60_CC61	O7		<b>T12 PWM channel 61</b>
IOM_MON1_1	<b>Monitor input 1</b>			
IOM_REF1_5	<b>Reference input 1</b>			

表 2-40 端口 P34 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
U13	P34.5	I	FAST / PU1 / VEVRSB / ES	General-purpose input
	GTM_TIM5_IN7_9			Mux input channel 7 of TIM module 5
	GTM_TIM4_IN7_12			Mux input channel 7 of TIM module 4
	GTM_TIM2_IN7_9			Mux input channel 7 of TIM module 2
	QSPI2_MTSRD			Slave SPI data input
	ASCLIN8_ARXE			Receive input
	P34.5	O0	FAST / PU1 / VEVRSB / ES	General-purpose output
	GTM_TOUT150	O1		GTM muxed output
	ASCLIN8_ATX	O2		Transmit output
	—	O3		Reserved
	QSPI2_MTSR	O4		Master SPI data output
	—	O5		Reserved
	EVADC_FC7BFLOUT	O6		Boundary flag output, FC channel 7
	CCU60_COUT61	O7		T12 PWM channel 61
IOM_MON1_4		Monitor input 1		
IOM_REF1_2		Reference input 1		

表 2-41 模拟输入

Ball	Symbol	Ctrl.	Buffer Type	Function
T10	AN0	I	D / HighZ / VDDM	Analog Input 0
	EVADC_G0CH0			Analog input channel 0, group 0
	EDSADC_EDS3PA			Positive analog input channel 3, pin A
U10	AN1	I	D / HighZ / VDDM	Analog Input 1
	EVADC_G0CH1			Analog input channel 1, group 0
	EDSADC_EDS3NA			Negative analog input channel 3, pin A
W9	AN2	I	D / HighZ / VDDM	Analog Input 2
	EVADC_G0CH2			Analog input channel 2, group 0
	EDSADC_EDS0PA			Positive analog input channel 0, pin A
U9	AN3	I	D / HighZ / VDDM	Analog Input 3
	EVADC_G0CH3			Analog input channel 3, group 0
	EDSADC_EDS0NA			Negative analog input channel 0, pin A
T9	AN4	I	D / HighZ / VDDM	Analog Input 4
	EVADC_G11CH0			Analog input channel 0, group 11
	EVADC_G0CH4			Analog input channel 4, group 0
Y9	AN5	I	D / HighZ / VDDM	Analog Input 5
	EVADC_G11CH1			Analog input channel 1, group 11
	EVADC_G0CH5			Analog input channel 5, group 0

表 2-41 模拟输入 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
T8	AN6	I	D / HighZ / VDDM	<b>Analog Input 6</b>
	EVADC_G11CH2			<b>Analog input channel 2, group 11</b>
	EVADC_G0CH6			<b>Analog input channel 6, group 0</b>
U8	AN7	I	D / HighZ / VDDM	<b>Analog Input 7</b>
	EVADC_G11CH3			<b>Analog input channel 3, group 11</b>
	EVADC_G0CH7			<b>Analog input channel 7, group 0</b>
W8	AN8	I	D / HighZ / VDDM	<b>Analog Input 8</b>
	EVADC_G11CH4			<b>Analog input channel 4, group 11</b>
	EVADC_G1CH0			<b>Analog input channel 0, group 1</b>
U7	AN9	I	D / HighZ / VDDM	<b>Analog Input 9</b>
	EVADC_G11CH5			<b>Analog input channel 5, group 11</b>
	EVADC_G1CH1			<b>Analog input channel 1, group 1</b>
Y8	AN10	I	D / HighZ / VDDM	<b>Analog Input 10</b>
	EVADC_G11CH6			<b>Analog input channel 6, group 11</b>
	EVADC_G1CH2			<b>Analog input channel 2, group 1</b>
W7	AN11	I	D / HighZ / VDDM	<b>Analog Input 11</b>
	EVADC_G11CH7			<b>Analog input channel 7, group 11</b>
	EVADC_G1CH3			<b>Analog input channel 3, group 1</b>
T7	AN12	I	D / HighZ / VDDM	<b>Analog Input 12</b>
	EVADC_G1CH4			<b>Analog input channel 4, group 1</b>
	EDSADC_EDS0PB			<b>Positive analog input channel 0, pin B</b>
W6	AN13	I	D / HighZ / VDDM	<b>Analog Input 13</b>
	EVADC_G1CH5			<b>Analog input channel 5, group 1</b>
	EDSADC_EDS0NB			<b>Negative analog input channel 0, pin B</b>
U6	AN14	I	D / HighZ / VDDM	<b>Analog Input 14</b>
	EVADC_G1CH6			<b>Analog input channel 6, group 1</b>
	EDSADC_EDS3PB			<b>Positive analog input channel 3, pin B</b>
T6	AN15	I	D / HighZ / VDDM	<b>Analog Input 15</b>
	EVADC_G1CH7			<b>Analog input channel 7, group 1</b>
	EDSADC_EDS3NB			<b>Negative analog input channel 3, pin N</b>
W5	AN16	I	D / HighZ / VDDM	<b>Analog Input 16</b>
	EVADC_G2CH0			<b>Analog input channel 0, group 2</b>
	EVADC_FC0CH0			<b>Analog input FC channel 0</b>
U5	AN17/P40.10	I	S / HighZ / VDDM	<b>Analog Input 17</b>
	SENT_SENT10A			<b>Receive input channel 10</b>
	EVADC_G2CH1			<b>Analog input channel 1, group 2</b>
	EVADC_FC1CH0			<b>Analog input FC channel 1</b>

表 2-41 模拟输入 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
W4	AN18/P40.11	I	S / HighZ / VDDM	Analog Input 18
	SENT_SENT11A			Receive input channel 11
	EVADC_G11CH8			Analog input channel 8, group 11
	EVADC_G2CH2			Analog input channel 2, group 2
W3	AN19/P40.12	I	S / HighZ / VDDM	Analog Input 19
	SENT_SENT12A			Receive input channel 12
	EVADC_G11CH9			Analog input channel 9, group 11
	EVADC_G2CH3			Analog input channel 3, group 2
Y3	AN20	I	D / HighZ / VDDM	Analog Input 20
	EVADC_G2CH4			Analog input channel 4, group 2
	EDSADC_EDS2PA			Positive analog input channel 2, pin A
Y2	AN21	I	D / HighZ / VDDM	Analog Input 21
	EVADC_G2CH5			Analog input channel 5, group 2
	EDSADC_EDS2NA			Negative analog input channel 2, pin A
T5	AN22	I	D / HighZ / VDDM	Analog Input 22
	EVADC_G2CH6			Analog input channel 6, group 2
R5	AN23	I	D / HighZ / VDDM	Analog Input 23
	EVADC_G2CH7			Analog input channel 7, group 2
W2	AN24/P40.0	I	S / HighZ / VDDM	Analog Input 24
	SENT_SENT0A			Receive input channel 0
	EVADC_G3CH0			Analog input channel 0, group 3
	CCU60_CCPOS0D			Hall capture input 0
	EDSADC_EDS2PB			Positive analog input channel 2, pin B
W1	AN25/P40.1	I	S / HighZ / VDDM	Analog Input 25
	SENT_SENT1A			Receive input channel 1
	EVADC_G3CH1			Analog input channel 1, group 3
	CCU60_CCPOS1B			Hall capture input 1
	EDSADC_EDS2NB			Negative analog input channel 2, pin B
V2	AN26/P40.2	I	S / HighZ / VDDM	Analog Input 26
	SENT_SENT2A			Receive input channel 2
	EVADC_G3CH2			Analog input channel 2, group 3
	CCU60_CCPOS1D			Hall capture input 1
	EVADC_G11CH10			Analog input channel 10, group 11
V1	AN27/P40.3	I	S / HighZ / VDDM	Analog Input 27
	SENT_SENT3A			Receive input channel 3
	EVADC_G3CH3			Analog input channel 3, group 3
	CCU60_CCPOS2B			Hall capture input 2
	EVADC_G11CH11			Analog input channel 11, group 11

表 2-41 模拟输入 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
U2	AN28/P40.13	I	S / HighZ / VDDM	<b>Analog Input 28</b>
	SENT_SENT13A			<b>Receive input channel 13</b>
	EVADC_G3CH4			<b>Analog input channel 4, group 3</b>
	EVADC_G4CH4			<b>Analog input channel 4, group 4</b>
U1	AN29/P40.14	I	S / HighZ / VDDM	<b>Analog Input 29</b>
	SENT_SENT14A			<b>Receive input channel 14</b>
	EVADC_G3CH5			<b>Analog input channel 5, group 3</b>
	EVADC_G4CH5			<b>Analog input channel 5, group 4</b>
T4	AN30	I	D / HighZ / VDDM	<b>Analog Input 30</b>
	EVADC_G3CH6			<b>Analog input channel 6, group 3</b>
	EVADC_G4CH6			<b>Analog input channel 6, group 4</b>
R4	AN31	I	D / HighZ / VDDM	<b>Analog Input 31</b>
	EVADC_G3CH7			<b>Analog input channel 7, group 3</b>
	EVADC_G4CH7			<b>Analog input channel 7, group 4</b>
P4	AN32/P40.4	I	S / HighZ / VDDM	<b>Analog Input 32</b>
	SENT_SENT4A			<b>Receive input channel 4</b>
	EVADC_G8CH0			<b>Analog input channel 0, group 8</b>
	CCU60_CCPOS2D			<b>Hall capture input 2</b>
	EVADC_G11CH12			<b>Analog input channel 12, group 11</b>
R1	AN33/P40.5	I	S / HighZ / VDDM	<b>Analog Input 33</b>
	SENT_SENT5A			<b>Receive input channel 5</b>
	EVADC_G8CH1			<b>Analog input channel 1, group 8</b>
	CCU61_CCPOS0D			<b>Hall capture input 0</b>
	EVADC_G11CH13			<b>Analog input channel 13, group 11</b>
P5	AN34	I	D / HighZ / VDDM	<b>Analog Input 34</b>
	EVADC_G8CH2			<b>Analog input channel 2, group 8</b>
	EVADC_G11CH14			<b>Analog input channel 14, group 11</b>
R2	AN35	I	D / HighZ / VDDM	<b>Analog Input 35</b>
	EVADC_G8CH3			<b>Analog input channel 3, group 8</b>
	EVADC_G11CH15			<b>Analog input channel 15, group 11</b>
N4	AN36/P40.6	I	S / HighZ / VDDM	<b>Analog Input 36</b>
	SENT_SENT6A			<b>Receive input channel 6</b>
	EVADC_G8CH4			<b>Analog input channel 4, group 8</b>
	CCU61_CCPOS1B			<b>Hall capture input 1</b>
	EDSADC_EDS1PA			<b>Positive analog input channel 1, pin A</b>

表 2-41 模拟输入 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
P2	AN37/P40.7	I	S / HighZ / VDDM	Analog Input 37
	SENT_SENT7A			Receive input channel 7
	EVADC_G8CH5			Analog input channel 5, group 8
	CCU61_CCPOS1D			Hall capture input 1
	EDSADC_EDS1NA			Negative analog input channel 1, pin A
N5	AN38/P40.8	I	S / HighZ / VDDM	Analog Input 38
	SENT_SENT8A			Receive input channel 8
	EVADC_G8CH6			Analog input channel 6, group 8
	CCU61_CCPOS2B			Hall capture input 2
	EDSADC_EDS1PB			Positive analog input channel 1, pin B
P1	AN39/P40.9	I	S / HighZ / VDDM	Analog Input 39
	SENT_SENT9A			Receive input channel 9
	EVADC_G8CH7			Analog input channel 7, group 8
	CCU61_CCPOS2D			Hall capture input 2
	EDSADC_EDS1NB			Negative analog input channel 1, pin B
M5	AN40	I	D / HighZ / VDDM	Analog Input 40
	EVADC_G8CH8			Analog input channel 8, group 8
	EVADC_G4CH0			Analog input channel 0, group 4
M4	AN41	I	D / HighZ / VDDM	Analog Input 41
	EVADC_G8CH9			Analog input channel 9, group 8
	EVADC_G4CH1			Analog input channel 1, group 4
L5	AN42	I	D / HighZ / VDDM	Analog Input 42
	EVADC_G8CH10			Analog input channel 10, group 8
	EVADC_G4CH2			Analog input channel 2, group 4
L4	AN43	I	D / HighZ / VDDM	Analog Input 43
	EVADC_G8CH11			Analog input channel 11, group 8
	EVADC_G4CH3			Analog input channel 3, group 4
N1	AN44	I	D / HighZ / VDDM	Analog Input 44
	EVADC_G8CH12			Analog input channel 12, group 8
	EDSADC_EDS1PC			Positive analog input channel 1, pin C
N2	AN45	I	D / HighZ / VDDM	Analog Input 45
	EVADC_G8CH13			Analog input channel 13, group 8
	EDSADC_EDS1NC			Negative analog input channel 1, pin C
M1	AN46	I	D / HighZ / VDDM	Analog Input 46
	EVADC_G8CH14			Analog input channel 14, group 8
	EDSADC_EDS1PD			Positive analog input channel 1, pin D

表 2-41 模拟输入 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
M2	AN47	I	D / HighZ / VDDM	<b>Analog Input 47</b>
	EVADC_G8CH15			<b>Analog input channel 15, group 8</b>
	EDSADC_EDS1ND			<b>Negative analog input channel 1, pin D</b>

注释：端口引脚P32.0和P32.1是双向引脚，具有以下两个功能：

3. 如果将这些引脚用作标准GPIO，则可以使用P32.0和P32.1引脚配置表中定义的功能。
4. 如果引脚用作外部MOSFET的预驱动器（内部DCDC情况），P32.0和P32.1将充当名为VGATE1N和VGATE1P的模拟IO。

表 2-42 系统 I/O

Ball	Symbol	Ctrl.	Buffer Type	Function
L7	AGBTCLKN (VSS)	I	AGBT_C LK / VEXT	<b>Input PAD (negative pole) for the external 100 MHz differential clock.</b> AGBT Input; (TC3xx devices without AGBT: VSS)
K7	AGBTCLKP (VSS)	I	AGBT_C LK / VEXT	<b>Input PAD (positive pole) for the external 100 MHz differential clock.</b> AGBT Input; (TC3xx devices without AGBT: VSS)
P10	AGBTTXN (VSS)	O	AGBT_T X / VEXT	<b>Off-chip driver output PAD of the 2.5Gbps transmitter, negative pole</b> AGBT Output; (TC3xx devices without AGBT: VSS)
P11	AGBTTXP (VSS)	O	AGBT_T X / VEXT	<b>Off-chip driver output PAD of the 2.5Gbps transmitter, positive pole</b> AGBT Output; (TC3xx devices without AGBT: VSS)
L14	AGBTERR (VSS)	I	FAST / PD / VEXT	<b>Input PAD for CRC error from FPGA.</b> AGBT Input; (TC3xx devices without AGBT: VSS)
W17	VGATE1P	O	—	<b>DCDC P ch. MOSFET gate driver output</b> P32.1 / External Pass Device gate control for EVRC
Y17	VGATE1N	O	—	<b>DCDC N ch. MOSFET gate driver output</b> P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
M20	XTAL1	I	XTAL / VEXT	<b>XTAL pad1</b> XTAL1. Main Oscillator/PLL/Clock Generator Input.
M19	XTAL2	O	XTAL / VEXT	<b>XTAL pad2</b> XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT
K14	DAPE0	I	FAST / PD2 / VEXT	<b>DAPE: DAPE0 Clock Input</b> DAPE: DAPE0 clock input (PD Devices: NC)

表 2-42 系统 I/O (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
L19	TRST	I	FAST /	<b>JTAG Module Reset/Enable Input</b>
	DAPE0	I	PU2 / VEXT	<b>DAPE: DAPE0 Clock Input</b>
K16	TMS	I	FAST /	<b>JTAG Module State Machine Control Input</b>
	DAP1	I/O	PD2 / VEXT	<b>DAP: DAP1 Data I/O</b>
J16	TCK	I	FAST /	<b>JTAG Module Clock Input</b>
	DAP0	I	PD2 / VEXT	<b>DAP: DAP0 Clock Input</b>
G11	DAPE1	I/O	FAST / PD2 / VEXT	<b>DAPE: DAPE1 Data I/O</b> DAPE: DAPE1 Data I/O (PD Devices: VSS)
G10	DAPE2	I/O	FAST / PD2 / VEXT	<b>DAPE: DAPE2 Data I/O</b> DAPE: DAPE2 Data I/O (PD Devices: VSS)
G16	ESR1	I/O	FAST / PU1 / VEXT	<b>ESR1 Port Pin input - can be used to trigger a reset or an NMI</b> ESR1: External System Request Reset 1. Default NMI function. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter 'Reset Control Unit' and SCU_IOCRR register description. PMS_EVRWUP: EVR Wakeup Pin
	PMS_ESR1WKP	I		<b>ESR1 pin input</b>
F16	ESR0	I/O	FAST / OD / VEXT	<b>ESR0 Port Pin input - can be used to trigger a reset or an NMI</b> ESR0: External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter 'Reset Control Unit' and SCU_IOCRR register description. PMS_EVRWUP: EVR Wakeup Pin
	PMS_ESR0WKP	I		<b>ESR0 pin input</b>
G17	PORST	I/O	PORST / PD / VEXT	<b>PORST pin</b> Power On Reset Input. Additional strong PD in case of power fail.

表 2-43 供电

Ball	Symbol	Ctrl.	Buffer Type	Function
P8, P13, N7, N14, E15, H14, D16, G13	VDD	I	—	Digital Core Power Supply (1.25V)
A2, B3, V19, W20	VEXT	I	—	External Power Supply (5V / 3.3V)
D5	VFLEX	I	—	Digital Power Supply for Flex Port Pads (5V / 3.3V)
Y5	VDDM	I	—	ADC Analog Power Supply (5V / 3.3V)
B18, A19	VDDP3	I	—	Flash Power Supply (3.3V)
B2, D4, E5, T16, U17, W19, Y20, E16, D17, B19, A20	VSS	I	—	Digital Ground
Y4	VSSM	I	—	Analog Ground for VDDM
P9, P12, N9, N10, N11, N12, M7, M8, M10, M11, M13, M14, L8, L9, L10, L11, L12, L13, K8, K9, K10, K11, K12, K13, J7, J8, J10, J11, J13, J14, H9, H10, H11, H12, G9, G12	VSS	I	—	Digital Ground
L20	VSS	I	—	Oscillator Ground, VSS(OSC)
Y6	VAREF1	I	—	Positive Analog Reference Voltage 1
Y7	VAGND1	I	—	Negative Analog Reference Voltage 1
T1	VAREF2	I	—	Positive Analog Reference Voltage 2
T2	VAGND2	I	—	Negative Analog Reference Voltage 2
A1, Y1, U4	NC1	I	—	Not connected. These pins are not connected on package level and will not be used for future extensions
G8, H7	VDDSB (VDD)	I	—	Devices with integrated EMEM: EMEM SRAM Standby Power Supply, VDDSB (1.25V); Devices without integrated EMEM: VDD (1.25V)

表 2-43 供电 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
T11	VEVRSB	I	—	<b>Standby Power Supply (5V / 3.3V) for the Standby SRAM</b>
N19	VDD	I	—	<b>Digital Power Supply for Oscillator (1.25V), VDD(OSC)</b>
N20	VEXT	I	—	<b>Digital Power Supply for Oscillator (shall be supplied with same level as used for VEXT), VEXT(OSC)</b>

## 2.3 LFBGA-292 ADAS 封装变体引脚配置

表 2-44 端口 P00 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
L2	P00.0	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM5_IN4_10			<b>Mux input channel 4 of TIM module 5</b>
	GTM_TIM3_IN0_1			<b>Mux input channel 0 of TIM module 3</b>
	GTM_TIM2_IN0_1			<b>Mux input channel 0 of TIM module 2</b>
	CCU61_CTRAPA			<b>Trap input capture</b>
	CCU60_T12HRE			<b>External timer start 12</b>
	MSC0_INJ0			<b>Injection signal from port</b>
	GETH_MDIOA			<b>MDIO Input</b>
	P00.0			O0
	GTM_TOUT9	O1	<b>GTM muxed output</b>	
	IOM_REF0_9		<b>Reference input 0</b>	
	ASCLIN3_ASCLK	O2	<b>Shift clock output</b>	
	ASCLIN3_ATX	O3	<b>Transmit output</b>	
	IOM_MON2_15		<b>Monitor input 2</b>	
	IOM_REF2_15		<b>Reference input 2</b>	
	—	O4	<b>Reserved</b>	
	CAN10_TXD	O5	<b>CAN transmit output node 0</b>	
	—	O6	<b>Reserved</b>	
	CCU60_COUT63	O7	<b>T13 PWM channel 63</b>	
	IOM_MON1_6		<b>Monitor input 1</b>	
IOM_REF1_0	<b>Reference input 1</b>			
GETH_MDIO	O	<b>MDIO Output</b>		

表 2-44 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
M2	P00.1	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM5_IN5_11			<b>Mux input channel 5 of TIM module 5</b>
	GTM_TIM3_IN1_1			<b>Mux input channel 1 of TIM module 3</b>
	GTM_TIM2_IN1_1			<b>Mux input channel 1 of TIM module 2</b>
	CCU60_CC60INB			<b>T12 capture input 60</b>
	ASCLIN3_ARXE			<b>Receive input</b>
	EDSADC_DSCIN5A			<b>Modulator clock input, channel 5</b>
	CAN10_RXDA			<b>CAN receive input node 0</b>
	PSI5_RX0A			<b>RXD inputs (receive data) channel 0</b>
	CCU61_CC60INA			<b>T12 capture input 60</b>
	SENT_SENT0B			<b>Receive input channel 0</b>
	EDSADC_DSCIN7B			<b>Modulator clock input, channel 7</b>
	EVADC_G9CH11			AI
	EDSADC_EDS5NA	<b>Negative analog input channel 5, pin A</b>		
	P00.1	O0	<b>General-purpose output</b>	
	GTM_TOUT10	O1	<b>GTM muxed output</b>	
	IOM_REF0_10	O2	<b>Reference input 0</b>	
	ASCLIN3_ATX		<b>Transmit output</b>	
	IOM_MON2_15		<b>Monitor input 2</b>	
	IOM_REF2_15	O3	<b>Reference input 2</b>	
	—		<b>Reserved</b>	
	EDSADC_DSCOUT5	O4	<b>Modulator clock output</b>	
	EDSADC_DSCOUT7	O5	<b>Modulator clock output</b>	
	SENT_SPC0	O6	<b>Transmit output</b>	
CCU61_CC60	O7	<b>T12 PWM channel 60</b>		
IOM_MON1_8		<b>Monitor input 1</b>		
IOM_REF1_13		<b>Reference input 1</b>		

表 2-44 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
M1	P00.2	I	SLOW / PU1 / VEXT / ES1	<b>General-purpose input</b>
	GTM_TIM5_IN6_11			<b>Mux input channel 6 of TIM module 5</b>
	GTM_TIM3_IN1_2			<b>Mux input channel 1 of TIM module 3</b>
	GTM_TIM2_IN1_2			<b>Mux input channel 1 of TIM module 2</b>
	EDSADC_DSDIN7B			<b>Digital datastream input, channel 7</b>
	EDSADC_DSDIN5A			<b>Digital datastream input, channel 5</b>
	SENT_SENT1B			<b>Receive input channel 1</b>
	EVADC_G9CH10	AI	<b>Analog input channel 10, group 9</b>	
	EDSADC_EDS5PA		<b>Positive analog input channel 5, pin A</b>	
	P00.2	O0	<b>General-purpose output</b>	
	GTM_TOUT11	O1	<b>GTM muxed output</b>	
	IOM_REF0_11		<b>Reference input 0</b>	
	ASCLIN3_ASCLK	O2	<b>Shift clock output</b>	
	CAN21_TXD	O3	<b>CAN transmit output node 1</b>	
	PSI5_TX0	O4	<b>TXD outputs (send data)</b>	
	IOM_MON1_14		<b>Monitor input 1</b>	
	IOM_REF1_14		<b>Reference input 1</b>	
	CAN03_TXD	O5	<b>CAN transmit output node 3</b>	
	IOM_MON2_8		<b>Monitor input 2</b>	
	IOM_REF2_8		<b>Reference input 2</b>	
	QSPI3_SLSO4	O6	<b>Master slave select output</b>	
	CCU61_COUT60	O7	<b>T12 PWM channel 60</b>	
	IOM_MON1_11		<b>Monitor input 1</b>	
	IOM_REF1_10		<b>Reference input 1</b>	

表 2-44 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
M4	P00.3	I	SLOW / PU1 / VEXT / ES1	<b>General-purpose input</b>
	GTM_TIM5_IN7_10			<b>Mux input channel 7 of TIM module 5</b>
	GTM_TIM3_IN2_1			<b>Mux input channel 2 of TIM module 3</b>
	GTM_TIM2_IN2_1			<b>Mux input channel 2 of TIM module 2</b>
	CCU60_CC61INB			<b>T12 capture input 61</b>
	EDSADC_DSCIN3A			<b>Modulator clock input, channel 3</b>
	EDSADC_ITR5F			<b>Trigger/Gate input, channel 5</b>
	PSI5_RX1A			<b>RXD inputs (receive data) channel 1</b>
	CAN03_RXDA			<b>CAN receive input node 3</b>
	CAN21_RXDA			<b>CAN receive input node 1</b>
	PSI5S_RXA			<b>RX data input</b>
	SENT_SENT2B			<b>Receive input channel 2</b>
	CCU61_CC61INA			<b>T12 capture input 61</b>
	EVADC_G9CH9			AI
	EDSADC_EDS5NB		<b>Negative analog input channel 5, pin B</b>	
	P00.3	O0	<b>General-purpose output</b>	
	GTM_TOUT12	O1	<b>GTM muxed output</b>	
	IOM_REF0_12		<b>Reference input 0</b>	
	ASCLIN3_ASLSO	O2	<b>Slave select signal output</b>	
	—	O3	<b>Reserved</b>	
	EDSADC_DSCOUT3	O4	<b>Modulator clock output</b>	
	—	O5	<b>Reserved</b>	
	SENT_SPC2	O6	<b>Transmit output</b>	
	CCU61_CC61	O7	<b>T12 PWM channel 61</b>	
	IOM_MON1_9		<b>Monitor input 1</b>	
	IOM_REF1_12		<b>Reference input 1</b>	

表 2-44 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
M5	P00.4	I	SLOW / PU1 / VEXT / ES1	<b>General-purpose input</b>	
	GTM_TIM6_IN4_1			<b>Mux input channel 4 of TIM module 6</b>	
	GTM_TIM3_IN3_1			<b>Mux input channel 3 of TIM module 3</b>	
	GTM_TIM2_IN3_1			<b>Mux input channel 3 of TIM module 2</b>	
	SCU_E_REQ2_2			<b>ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>	
	SENT_SENT3B			<b>Receive input channel 3</b>	
	EDSADC_DSDIN3A			<b>Digital datastream input, channel 3</b>	
	EDSADC_SGNA			<b>Carrier sign signal input</b>	
	ASCLIN10_ARXA			<b>Receive input</b>	
	GTM_DTMA5_0			<b>CDTM5_DTM4</b>	
	GTM_DTMT3_0			<b>CDTM3_DTM0</b>	
	EVADC_G9CH8			AI	<b>Analog input channel 8, group 9</b>
	EDSADC_EDS5PB				<b>Positive analog input channel 5, pin B</b>
	P00.4	O0	<b>General-purpose output</b>		
	GTM_TOUT13	O1	<b>GTM muxed output</b>		
	IOM_REF0_13		<b>Reference input 0</b>		
	PSI5S_TX	O2	<b>TX data output</b>		
	CAN11_TXD	O3	<b>CAN transmit output node 1</b>		
	PSI5_TX1	O4	<b>TXD outputs (send data)</b>		
	IOM_MON1_15		<b>Monitor input 1</b>		
	EVADC_FC4BFLOUT	O5	<b>Boundary flag output, FC channel 4</b>		
	SENT_SPC3	O6	<b>Transmit output</b>		
	CCU61_COUT61	O7	<b>T12 PWM channel 61</b>		
IOM_MON1_12	<b>Monitor input 1</b>				
IOM_REF1_9	<b>Reference input 1</b>				

表 2-44 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
N5	P00.5	I	SLOW / PU1 / VEXT / ES1	<b>General-purpose input</b>
	GTM_TIM3_IN4_1			<b>Mux input channel 4 of TIM module 3</b>
	GTM_TIM3_IN0_11			<b>Mux input channel 0 of TIM module 3</b>
	GTM_TIM2_IN4_1			<b>Mux input channel 4 of TIM module 2</b>
	CCU60_CC62INB			<b>T12 capture input 62</b>
	EDSADC_DSCIN2A			<b>Modulator clock input, channel 2</b>
	PSI5_RX2A			<b>RXD inputs (receive data) channel 2</b>
	CCU61_CC62INA			<b>T12 capture input 62</b>
	SENT_SENT4B			<b>Receive input channel 4</b>
	CAN11_RXDB			<b>CAN receive input node 1</b>
	GTM_DTMT1_1			<b>CDTM1_DTM0</b>
	GTM_DTMT4_2			<b>CDTM4_DTM0</b>
	EVADC_G9CH7			AI
	P00.5	O0	<b>General-purpose output</b>	
	GTM_TOUT14	O1	<b>GTM muxed output</b>	
	IOM_REF0_14		<b>Reference input 0</b>	
	EDSADC_CGPWMN	O2	<b>Negative carrier generator output</b>	
	QSPI3_SLSO3	O3	<b>Master slave select output</b>	
	EDSADC_DSCOUT2	O4	<b>Modulator clock output</b>	
	EVADC_FC0BFLOUT	O5	<b>Boundary flag output, FC channel 0</b>	
SENT_SPC4	O6	<b>Transmit output</b>		
CCU61_CC62	O7	<b>T12 PWM channel 62</b>		
IOM_MON1_10		<b>Monitor input 1</b>		
IOM_REF1_11		<b>Reference input 1</b>		

表 2-44 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
N4	P00.6	I	SLOW / PU1 / VEXT / ES1	<b>General-purpose input</b>
	GTM_TIM3_IN5_1			<b>Mux input channel 5 of TIM module 3</b>
	GTM_TIM3_IN1_14			<b>Mux input channel 1 of TIM module 3</b>
	GTM_TIM2_IN5_1			<b>Mux input channel 5 of TIM module 2</b>
	EDSADC_ITR4F			<b>Trigger/Gate input, channel 4</b>
	EDSADC_DSDIN2A			<b>Digital datastream input, channel 2</b>
	SENT_SENT5B			<b>Receive input channel 5</b>
	ASCLIN5_ARXA			<b>Receive input</b>
	GTM_DTMA6_0			<b>CDTM6_DTM4</b>
	GTM_DTMT3_1			<b>CDTM3_DTM0</b>
	EVADC_G9CH6	AI	<b>Analog input channel 6, group 9</b>	
	P00.6	O0	<b>General-purpose output</b>	
	GTM_TOUT15	O1	<b>GTM muxed output</b>	
	IOM_REF0_15		<b>Reference input 0</b>	
	EDSADC_CGPWMP	O2	<b>Positive carrier generator output</b>	
	EVADC_FC5BFLOUT	O3	<b>Boundary flag output, FC channel 5</b>	
	PSI5_TX2	O4	<b>TXD outputs (send data)</b>	
	IOM_REF1_15		<b>Reference input 1</b>	
	EVADC_EMUX10	O5	<b>Control of external analog multiplexer interface 1</b>	
	SENT_SPC5	O6	<b>Transmit output</b>	
CCU61_COUT62	O7	<b>T12 PWM channel 62</b>		
IOM_MON1_13		<b>Monitor input 1</b>		
IOM_REF1_8		<b>Reference input 1</b>		

表 2-44 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
N2	P00.7	I	SLOW / PU1 / VEXT / ES1	<b>General-purpose input</b>
	GTM_TIM3_IN6_1			<b>Mux input channel 6 of TIM module 3</b>
	GTM_TIM3_IN2_11			<b>Mux input channel 2 of TIM module 3</b>
	GTM_TIM2_IN6_1			<b>Mux input channel 6 of TIM module 2</b>
	CCU61_CC60INC			<b>T12 capture input 60</b>
	SENT_SENT6B			<b>Receive input channel 6</b>
	EDSADC_DSCIN4A			<b>Modulator clock input, channel 4</b>
	GPT120_T2INA			<b>Trigger/gate input of timer T2</b>
	CCU61_CCPOS0A			<b>Hall capture input 0</b>
	CCU60_T12HRB			<b>External timer start 12</b>
	GTM_DTMT0_2			<b>CDTM0_DTM0</b>
	EVADC_G9CH5			AI
	EDSADC_EDS4NA	<b>Negative analog input channel 4, pin A</b>		
	P00.7	O0	<b>General-purpose output</b>	
	GTM_TOUT16	O1	<b>GTM muxed output</b>	
	ASCLIN5_ATX	O2	<b>Transmit output</b>	
	EVADC_FC2BFLOUT	O3	<b>Boundary flag output, FC channel 2</b>	
	EDSADC_DSCOUT4	O4	<b>Modulator clock output</b>	
	EVADC_EMUX11	O5	<b>Control of external analog multiplexer interface 1</b>	
	SENT_SPC6	O6	<b>Transmit output</b>	
	CCU61_CC60	O7	<b>T12 PWM channel 60</b>	
	IOM_MON1_8		<b>Monitor input 1</b>	
	IOM_REF1_13		<b>Reference input 1</b>	

表 2-44 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
N1	P00.8	I	SLOW / PU1 / VEXT / ES1	General-purpose input	
	GTM_TIM3_IN7_1			Mux input channel 7 of TIM module 3	
	GTM_TIM3_IN3_11			Mux input channel 3 of TIM module 3	
	GTM_TIM2_IN7_1			Mux input channel 7 of TIM module 2	
	CCU61_CC61INC			T12 capture input 61	
	SENT_SENT7B			Receive input channel 7	
	EDSADC_DSDIN4A			Digital datastream input, channel 4	
	GPT120_T2EUDA			Count direction control input of timer T2	
	CCU61_CCPOS1A			Hall capture input 1	
	CCU60_T13HRB			External timer start 13	
	ASCLIN10_ARXB			Receive input	
	EVADC_G9CH4			AI	Analog input channel 4, group 9
	EDSADC_EDS4PA				Positive analog input channel 4, pin A
	P00.8	O0	General-purpose output		
	GTM_TOUT17	O1	GTM muxed output		
	QSPI3_SLSO6	O2	Master slave select output		
	ASCLIN10_ATX	O3	Transmit output		
	—	O4	Reserved		
	EVADC_EMUX12	O5	Control of external analog multiplexer interface 1		
	SENT_SPC7	O6	Transmit output		
	CCU61_CC61	O7	T12 PWM channel 61		
	IOM_MON1_9		Monitor input 1		
	IOM_REF1_12		Reference input 1		

表 2-44 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
P2	P00.9	I	SLOW / PU1 / VEXT / ES1	<b>General-purpose input</b>
	GTM_TIM4_IN0_7			<b>Mux input channel 0 of TIM module 4</b>
	GTM_TIM1_IN0_1			<b>Mux input channel 0 of TIM module 1</b>
	GTM_TIM0_IN0_1			<b>Mux input channel 0 of TIM module 0</b>
	CCU61_CC62INC			<b>T12 capture input 62</b>
	SENT_SENT8B			<b>Receive input channel 8</b>
	CCU61_CCPOS2A			<b>Hall capture input 2</b>
	EDSADC_DSCIN1A			<b>Modulator clock input, channel 1</b>
	EDSADC_ITR3F			<b>Trigger/Gate input, channel 3</b>
	GPT120_T4EUDA			<b>Count direction control input of timer T4</b>
	CCU60_T13HRC			<b>External timer start 13</b>
	CCU60_T12HRC			<b>External timer start 12</b>
	EVADC_G9CH3			AI
	EDSADC_EDS4NB	<b>Negative analog input channel 4, pin B</b>		
	P00.9	O0	<b>General-purpose output</b>	
	GTM_TOUT18	O1	<b>GTM muxed output</b>	
	QSPI3_SLSO7	O2	<b>Master slave select output</b>	
	ASCLIN3_ARTS	O3	<b>Ready to send output</b>	
	EDSADC_DSCOUT1	O4	<b>Modulator clock output</b>	
	ASCLIN4_ATX	O5	<b>Transmit output</b>	
	SENT_SPC8	O6	<b>Transmit output</b>	
	CCU61_CC62	O7	<b>T12 PWM channel 62</b>	
	IOM_MON1_10		<b>Monitor input 1</b>	
IOM_REF1_11	<b>Reference input 1</b>			

表 2-44 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
P1	P00.10	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM4_IN1_11			Mux input channel 1 of TIM module 4
	GTM_TIM1_IN1_1			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_1			Mux input channel 1 of TIM module 0
	SENT_SENT9B			Receive input channel 9
	EDSADC_DSDIN1A			Digital datastream input, channel 1
	EVADC_G9CH2			Analog input channel 2, group 9
	EDSADC_EDS4PB	AI	Positive analog input channel 4, pin B	
	P00.10	O0	General-purpose output	
	GTM_TOUT19	O1	GTM muxed output	
	ASCLIN4_ASCLK	O2	Shift clock output	
	—	O3	Reserved	
	—	O4	Reserved	
	—	O5	Reserved	
	SENT_SPC9	O6	Transmit output	
	CCU61_COUT63	O7	T13 PWM channel 63	
	IOM_MON1_7		Monitor input 1	
IOM_REF1_7	Reference input 1			
R1	P00.11	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM4_IN2_11			Mux input channel 2 of TIM module 4
	GTM_TIM1_IN2_1			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_1			Mux input channel 2 of TIM module 0
	CCU60_CTRAPA			Trap input capture
	EDSADC_DSCIN0A			Modulator clock input, channel 0
	CCU61_T12HRE			External timer start 12
	SENT_SENT10B	Receive input channel 10		
	EVADC_G9CH1	AI	Analog input channel 1, group 9	
	EVADC_FC3CH0	Analog input FC channel 3		
	P00.11	O0	General-purpose output	
	GTM_TOUT20	O1	GTM muxed output	
	ASCLIN4_ASLSO	O2	Slave select signal output	
	—	O3	Reserved	
	EDSADC_DSCOUT0	O4	Modulator clock output	
	—	O5	Reserved	
	—	O6	Reserved	
—	O7	Reserved		

表 2-44 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
R2	P00.12	I	SLOW / PU1 / VEXT / ES1	<b>General-purpose input</b>
	GTM_TIM4_IN3_11			<b>Mux input channel 3 of TIM module 4</b>
	GTM_TIM1_IN3_1			<b>Mux input channel 3 of TIM module 1</b>
	GTM_TIM0_IN3_1			<b>Mux input channel 3 of TIM module 0</b>
	ASCLIN3_ACTSA			<b>Clear to send input</b>
	EDSADC_DSDIN0A			<b>Digital datastream input, channel 0</b>
	ASCLIN4_ARXA			<b>Receive input</b>
	SENT_SENT11B			<b>Receive input channel 11</b>
	EVADC_G9CH0			AI
	EVADC_FC2CH0		<b>Analog input FC channel 2</b>	
	P00.12	O0	<b>General-purpose output</b>	
	GTM_TOUT21	O1	<b>GTM muxed output</b>	
	—	O2	<b>Reserved</b>	
	—	O3	<b>Reserved</b>	
	—	O4	<b>Reserved</b>	
	—	O5	<b>Reserved</b>	
	—	O6	<b>Reserved</b>	
	CCU61_COUT63	O7	<b>T13 PWM channel 63</b>	
	IOM_MON1_7		<b>Monitor input 1</b>	
	IOM_REF1_7		<b>Reference input 1</b>	

表 2-45 端口 P02 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
J1	P02.0	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN0_2			<b>Mux input channel 0 of TIM module 1</b>
	GTM_TIM0_IN0_2			<b>Mux input channel 0 of TIM module 0</b>
	CCU61_CC60INB			<b>T12 capture input 60</b>
	ASCLIN2_ARXG			<b>Receive input</b>
	CCU60_CC60INA			<b>T12 capture input 60</b>
	SCU_E_REQ3_2			<b>ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	GTM_DTMA0_0			<b>CDTM0_DTM4</b>
	P02.0			O0
	GTM_TOUT0	O1	<b>GTM muxed output</b>	
	IOM_REF0_0		<b>Reference input 0</b>	
	ASCLIN2_ATX	O2	<b>Transmit output</b>	
	IOM_MON2_14		<b>Monitor input 2</b>	
	IOM_REF2_14		<b>Reference input 2</b>	
	QSPI3_SLSO1	O3	<b>Master slave select output</b>	
	EDSADC_CGPWMN	O4	<b>Negative carrier generator output</b>	
	CAN00_TXD	O5	<b>CAN transmit output node 0</b>	
	IOM_MON2_5		<b>Monitor input 2</b>	
	IOM_REF2_5		<b>Reference input 2</b>	
	ERAY0_TXDA	O6	<b>Transmit Channel A</b>	
CCU60_CC60	O7	<b>T12 PWM channel 60</b>		
IOM_MON1_2		<b>Monitor input 1</b>		
IOM_REF1_6		<b>Reference input 1</b>		

表 2-45 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
J2	P02.1	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN1_2			<b>Mux input channel 1 of TIM module 1</b>
	GTM_TIM0_IN1_2			<b>Mux input channel 1 of TIM module 0</b>
	ERAY0_RXDA2			<b>Receive Channel A2</b>
	ASCLIN2_ARXB			<b>Receive input</b>
	CAN00_RXDA			<b>CAN receive input node 0</b>
	SCU_E_REQ2_1			<b>ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	P02.1	O0	<b>General-purpose output</b>	
	GTM_TOUT1	O1	<b>GTM muxed output</b>	
	IOM_REF0_1		<b>Reference input 0</b>	
	QSPI4_SLSO7	O2	<b>Master slave select output</b>	
	QSPI3_SLSO2	O3	<b>Master slave select output</b>	
	EDSADC_CGPWMP	O4	<b>Positive carrier generator output</b>	
	—	O5	<b>Reserved</b>	
	—	O6	<b>Reserved</b>	
	CCU60_COUT60	O7	<b>T12 PWM channel 60</b>	
	IOM_MON1_3		<b>Monitor input 1</b>	
	IOM_REF1_3		<b>Reference input 1</b>	

表 2-45 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
K1	P02.2	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN2_2			<b>Mux input channel 2 of TIM module 1</b>
	GTM_TIM0_IN2_2			<b>Mux input channel 2 of TIM module 0</b>
	CCU61_CC61INB			<b>T12 capture input 61</b>
	CCU60_CC61INA			<b>T12 capture input 61</b>
	SENT_SENT14B			<b>Receive input channel 14</b>
	P02.2	O0		<b>General-purpose output</b>
	GTM_TOUT2	O1		<b>GTM muxed output</b>
	IOM_REF0_2	O2		<b>Reference input 0</b>
	ASCLIN1_ATX			<b>Transmit output</b>
	IOM_MON2_13			<b>Monitor input 2</b>
	IOM_REF2_13	O3		<b>Reference input 2</b>
	QSPI3_SLSO3			<b>Master slave select output</b>
	PSI5_TX0	O4		<b>TXD outputs (send data)</b>
	IOM_MON1_14	O5		<b>Monitor input 1</b>
	IOM_REF1_14			<b>Reference input 1</b>
	CAN02_TXD			<b>CAN transmit output node 2</b>
	IOM_MON2_7	O6		<b>Monitor input 2</b>
	IOM_REF2_7			<b>Reference input 2</b>
	ERAY0_TXDB	O7		<b>Transmit Channel B</b>
	CCU60_CC61	O7		<b>T12 PWM channel 61</b>
	IOM_MON1_1			<b>Monitor input 1</b>
	IOM_REF1_5			<b>Reference input 1</b>

表 2-45 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
K2	P02.3	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN3_2			<b>Mux input channel 3 of TIM module 1</b>
	GTM_TIM0_IN3_2			<b>Mux input channel 3 of TIM module 0</b>
	EDSADC_DSCIN5B			<b>Modulator clock input, channel 5</b>
	ERAY0_RXDB2			<b>Receive Channel B2</b>
	CAN02_RXDB			<b>CAN receive input node 2</b>
	ASCLIN1_ARXG			<b>Receive input</b>
	MSC1_SDI1			<b>Upstream asynchronous input signal</b>
	PSI5_RX0B			<b>RXD inputs (receive data) channel 0</b>
	SENT_SENT13B			<b>Receive input channel 13</b>
	P02.3	O0	<b>General-purpose output</b>	
	GTM_TOUT3	O1	<b>GTM muxed output</b>	
	IOM_REF0_3		<b>Reference input 0</b>	
	ASCLIN2_ASLSO	O2	<b>Slave select signal output</b>	
	QSPI3_SLSO4	O3	<b>Master slave select output</b>	
	EDSADC_DSCOUT5	O4	<b>Modulator clock output</b>	
	—	O5	<b>Reserved</b>	
	—	O6	<b>Reserved</b>	
	CCU60_COUT61	O7	<b>T12 PWM channel 61</b>	
	IOM_MON1_4		<b>Monitor input 1</b>	
IOM_REF1_2	<b>Reference input 1</b>			

表 2-45 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
K4	P02.4	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN4_1			<b>Mux input channel 4 of TIM module 1</b>
	GTM_TIM0_IN4_1			<b>Mux input channel 4 of TIM module 0</b>
	CCU61_CC62INB			<b>T12 capture input 62</b>
	EDSADC_DSDIN5B			<b>Digital datastream input, channel 5</b>
	QSPI3_SLSIA			<b>Slave select input</b>
	CCU60_CC62INA			<b>T12 capture input 62</b>
	I2C0_SDAA			<b>Serial Data Input 0</b>
	CAN11_RXDA			<b>CAN receive input node 1</b>
	CAN0_ECTT1			<b>External CAN time trigger input</b>
	SENT_SENT12B			<b>Receive input channel 12</b>
	P02.4	O0		<b>General-purpose output</b>
	GTM_TOUT4	O1		<b>GTM muxed output</b>
	IOM_REF0_4			<b>Reference input 0</b>
	ASCLIN2_ASCLK	O2		<b>Shift clock output</b>
	QSPI3_SLSO0	O3		<b>Master slave select output</b>
	PSI5S_CLK	O4		<b>PSI5S CLK is a clock that can be used on a pin to drive the external PHY.</b>
	I2C0_SDA	O5		<b>Serial Data Output</b>
	ERAY0_TXENA	O6		<b>Transmit Enable Channel A</b>
	CCU60_CC62	O7		<b>T12 PWM channel 62</b>
IOM_MON1_0	<b>Monitor input 1</b>			
IOM_REF1_4	<b>Reference input 1</b>			

表 2-45 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
K5	P02.5	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN5_1			<b>Mux input channel 5 of TIM module 1</b>
	GTM_TIM0_IN5_1			<b>Mux input channel 5 of TIM module 0</b>
	EDSADC_DSCIN4B			<b>Modulator clock input, channel 4</b>
	I2C0_SCLA			<b>Serial Clock Input 0</b>
	PSI5_RX1B			<b>RXD inputs (receive data) channel 1</b>
	PSI5S_RXB			<b>RX data input</b>
	QSPI3_MRSTA			<b>Master SPI data input</b>
	SENT_SENT3C			<b>Receive input channel 3</b>
	CAN0_ECTT2			<b>External CAN time trigger input</b>
	P02.5	O0	<b>General-purpose output</b>	
	GTM_TOUT5	O1	<b>GTM muxed output</b>	
	IOM_REF0_5	O2	<b>Reference input 0</b>	
	CAN11_TXD		<b>CAN transmit output node 1</b>	
	QSPI3_MRST	O3	<b>Slave SPI data output</b>	
	IOM_MON2_3	O3	<b>Monitor input 2</b>	
	IOM_REF2_3		<b>Reference input 2</b>	
	EDSADC_DSCOUT4	O4	<b>Modulator clock output</b>	
	I2C0_SCL	O5	<b>Serial Clock Output</b>	
	ERAY0_TXENB	O6	<b>Transmit Enable Channel B</b>	
	CCU60_COUT62	O7	<b>T12 PWM channel 62</b>	
IOM_MON1_5	O7	<b>Monitor input 1</b>		
IOM_REF1_1		<b>Reference input 1</b>		

表 2-45 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
L1	P02.6	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM3_IN0_10			<b>Mux input channel 0 of TIM module 3</b>
	GTM_TIM1_IN6_1			<b>Mux input channel 6 of TIM module 1</b>
	GTM_TIM0_IN6_1			<b>Mux input channel 6 of TIM module 0</b>
	CCU60_CC60INC			<b>T12 capture input 60</b>
	SENT_SENT2C			<b>Receive input channel 2</b>
	EDSADC_DSDIN4B			<b>Digital datastream input, channel 4</b>
	EDSADC_ITR5E			<b>Trigger/Gate input, channel 5</b>
	GPT120_T3INA			<b>Trigger/gate input of core timer T3</b>
	CCU60_CCPOS0A			<b>Hall capture input 0</b>
	CCU61_T12HRB			<b>External timer start 12</b>
	QSPI3_MTSRA			<b>Slave SPI data input</b>
	RIF0_RAMP1B			<b>External RAMP B input</b>
	P02.6			00
	GTM_TOUT6	01	<b>GTM muxed output</b>	
	IOM_REF0_6		<b>Reference input 0</b>	
	PSI5S_TX	02	<b>TX data output</b>	
	QSPI3_MTSR	03	<b>Master SPI data output</b>	
	PSI5_TX1	04	<b>TXD outputs (send data)</b>	
	IOM_MON1_15		<b>Monitor input 1</b>	
	EVADC_EMUX00	05	<b>Control of external analog multiplexer interface 0</b>	
	—	06	<b>Reserved</b>	
	CCU60_CC60	07	<b>T12 PWM channel 60</b>	
	IOM_MON1_2		<b>Monitor input 1</b>	
IOM_REF1_6	<b>Reference input 1</b>			

表 2-45 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
L4	P02.7	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM3_IN1_10			<b>Mux input channel 1 of TIM module 3</b>
	GTM_TIM1_IN7_1			<b>Mux input channel 7 of TIM module 1</b>
	GTM_TIM0_IN7_1			<b>Mux input channel 7 of TIM module 0</b>
	CCU60_CC61INC			<b>T12 capture input 61</b>
	SENT_SENT1C			<b>Receive input channel 1</b>
	EDSADC_DSCIN3B			<b>Modulator clock input, channel 3</b>
	EDSADC_ITR4E			<b>Trigger/Gate input, channel 4</b>
	GPT120_T3EUDA			<b>Count direction control input of core timer T3</b>
	PSI5_RX2B			<b>RXD inputs (receive data) channel 2</b>
	CCU60_CCPOS1A			<b>Hall capture input 1</b>
	QSPI3_SCLKA			<b>Slave SPI clock inputs</b>
	CCU61_T13HRB			<b>External timer start 13</b>
	P02.7			O0
	GTM_TOUT7	O1	<b>GTM muxed output</b>	
	IOM_REF0_7	O2	<b>Reference input 0</b>	
	—		<b>Reserved</b>	
	QSPI3_SCLK	O3	<b>Master SPI clock output</b>	
	EDSADC_DSCOUT3	O4	<b>Modulator clock output</b>	
	EVADC_EMUX01	O5	<b>Control of external analog multiplexer interface 0</b>	
SENT_SPC1	O6	<b>Transmit output</b>		
CCU60_CC61	O7	<b>T12 PWM channel 61</b>		
IOM_MON1_1		<b>Monitor input 1</b>		
IOM_REF1_5		<b>Reference input 1</b>		

表 2-45 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
L5	P02.8	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM3_IN2_10			<b>Mux input channel 2 of TIM module 3</b>
	GTM_TIM3_IN0_2			<b>Mux input channel 0 of TIM module 3</b>
	GTM_TIM2_IN0_2			<b>Mux input channel 0 of TIM module 2</b>
	CCU60_CC62INC			<b>T12 capture input 62</b>
	SENT_SENT0C			<b>Receive input channel 0</b>
	CCU60_CCPOS2A			<b>Hall capture input 2</b>
	EDSADC_DSDIN3B			<b>Digital datastream input, channel 3</b>
	EDSADC_ITR3E			<b>Trigger/Gate input, channel 3</b>
	GPT120_T4INA			<b>Trigger/gate input of timer T4</b>
	CCU61_T12HRC			<b>External timer start 12</b>
	CCU61_T13HRC			<b>External timer start 13</b>
	GTM_DTMA0_1			<b>CDTM0_DTM4</b>
	P02.8			O0
	GTM_TOUT8	O1	<b>GTM muxed output</b>	
	IOM_REF0_8		<b>Reference input 0</b>	
	QSPI3_SLSO5	O2	<b>Master slave select output</b>	
	ASCLIN8_ASCLK	O3	<b>Shift clock output</b>	
	PSI5_TX2	O4	<b>TXD outputs (send data)</b>	
	IOM_REF1_15		<b>Reference input 1</b>	
EVADC_EMUX02	O5	<b>Control of external analog multiplexer interface 0</b>		
GETH_MDC	O6	<b>MDIO clock</b>		
CCU60_CC62	O7	<b>T12 PWM channel 62</b>		
IOM_MON1_0		<b>Monitor input 1</b>		
IOM_REF1_4		<b>Reference input 1</b>		

表 2-46 端口 P10 功能

Ball	Symbol	Ctrl.	Buffer Type	Function	
E4	P10.0	I	SLOW / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM4_IN0_12			Mux input channel 0 of TIM module 4	
	GTM_TIM1_IN4_2			Mux input channel 4 of TIM module 1	
	GTM_TIM0_IN4_2			Mux input channel 4 of TIM module 0	
	GPT120_T6EUDB			Count direction control input of core timer T6	
	ASCLIN11_ARXA			Receive input	
	GETH_RXERC			Receive Error MII	
	GTM_DTMA5_2			CDTM5_DTM4	
	P10.0			O0	General-purpose output
	GTM_TOUT102			O1	GTM muxed output
	ASCLIN11_ATX			O2	Transmit output
	QSPI1_SLSO10			O3	Master slave select output
	—			O4	Reserved
	EVADC_FC6BFLOUT			O5	Boundary flag output, FC channel 6
—	O6	Reserved			
—	O7	Reserved			
F4	P10.1	I	FAST / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM4_IN4_12			Mux input channel 4 of TIM module 4	
	GTM_TIM1_IN1_3			Mux input channel 1 of TIM module 1	
	GTM_TIM0_IN1_3			Mux input channel 1 of TIM module 0	
	GPT120_T5EUDB			Count direction control input of timer T5	
	QSPI1_MRSTA			Master SPI data input	
	GTM_DTMT0_1			CDTM0_DTM0	
	P10.1			O0	General-purpose output
	GTM_TOUT103			O1	GTM muxed output
	QSPI1_MTSR			O2	Master SPI data output
	QSPI1_MRST			O3	Slave SPI data output
	IOM_MON2_1				Monitor input 2
	IOM_REF2_1				Reference input 2
	MSC0_EN1			O4	Chip Select
EVADC_FC1BFLOUT	O5	Boundary flag output, FC channel 1			
—	O6	Reserved			
—	O7	Reserved			

表 2-46 端口 P10 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
F5	P10.2	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM4_IN5_12			<b>Mux input channel 5 of TIM module 4</b>
	GTM_TIM1_IN2_3			<b>Mux input channel 2 of TIM module 1</b>
	GTM_TIM0_IN2_3			<b>Mux input channel 2 of TIM module 0</b>
	CAN02_RXDE			<b>CAN receive input node 2</b>
	MSC0_SDI1			<b>Upstream asynchronous input signal</b>
	QSPI1_SCLKA			<b>Slave SPI clock inputs</b>
	GPT120_T6INB			<b>Trigger/gate input of core timer T6</b>
	SCU_E_REQ2_0			<b>ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	GTM_DTMT2_2			<b>CDTM2_DTM0</b>
	P10.2	00	<b>General-purpose output</b>	
	GTM_TOUT104	01	<b>GTM muxed output</b>	
	IOM_MON2_9		<b>Monitor input 2</b>	
	—	02	<b>Reserved</b>	
	QSPI1_SCLK	03	<b>Master SPI clock output</b>	
	MSC0_EN0	04	<b>Chip Select</b>	
	EVADC_FC3BFLOUT	05	<b>Boundary flag output, FC channel 3</b>	
	—	06	<b>Reserved</b>	
	—	07	<b>Reserved</b>	

表 2-46 端口 P10 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
G4	P10.3	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN6_10			Mux input channel 6 of TIM module 4
	GTM_TIM1_IN3_3			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_3			Mux input channel 3 of TIM module 0
	QSPI1_MTSRA			Slave SPI data input
	SCU_E_REQ3_0			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	GPT120_T5INB			Trigger/gate input of timer T5
	P10.3	O0	General-purpose output	
	GTM_TOUT105	O1	GTM muxed output	
	IOM_MON2_10		Monitor input 2	
	—	O2	Reserved	
	QSPI1_MTSR	O3	Master SPI data output	
	MSC0_EN0	O4	Chip Select	
	—	O5	Reserved	
	CAN02_TXD	O6	CAN transmit output node 2	
	IOM_MON2_7		Monitor input 2	
	IOM_REF2_7		Reference input 2	
—	O7	Reserved		
G5	P10.4	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN7_3			Mux input channel 7 of TIM module 4
	GTM_TIM1_IN6_2			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_2			Mux input channel 6 of TIM module 0
	QSPI1_MTSRC			Slave SPI data input
	CCU60_CCPOS0C			Hall capture input 0
	GPT120_T3INB			Trigger/gate input of core timer T3
	ASCLIN11_ARXB	Receive input		
	P10.4	O0	General-purpose output	
	GTM_TOUT106	O1	GTM muxed output	
	IOM_MON2_11		Monitor input 2	
	—	O2	Reserved	
	QSPI1_SLSO8	O3	Master slave select output	
	QSPI1_MTSR	O4	Master SPI data output	
	MSC0_EN0	O5	Chip Select	
	—	O6	Reserved	
	—	O7	Reserved	

表 2-46 端口 P10 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
H4	P10.5	I	SLOW / PU2 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM4_IN3_13			<b>Mux input channel 3 of TIM module 4</b>
	GTM_TIM1_IN2_4			<b>Mux input channel 2 of TIM module 1</b>
	GTM_TIM0_IN2_4			<b>Mux input channel 2 of TIM module 0</b>
	PMS_HWCFG4IN			<b>HWCFG4 pin input</b>
	CAN20_RXDA			<b>CAN receive input node 0</b>
	MSC0_INJ1			<b>Injection signal from port</b>
	P10.5			O0
	GTM_TOUT107	O1		<b>GTM muxed output</b>
	IOM_REF2_9			<b>Reference input 2</b>
	ASCLIN2_ATX	O2		<b>Transmit output</b>
	IOM_MON2_14			<b>Monitor input 2</b>
	IOM_REF2_14			<b>Reference input 2</b>
	QSPI3_SLSO8	O3		<b>Master slave select output</b>
	QSPI1_SLSO9	O4		<b>Master slave select output</b>
	GPT120_T6OUT	O5		<b>External output for overflow/underflow detection of core timer T6</b>
	ASCLIN2_ASLSO	O6		<b>Slave select signal output</b>
	PSI5_TX3	O7		<b>TXD outputs (send data)</b>

表 2-46 端口 P10 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
H5	P10.6	I	SLOW / PU2 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM4_IN2_13			<b>Mux input channel 2 of TIM module 4</b>
	GTM_TIM1_IN3_4			<b>Mux input channel 3 of TIM module 1</b>
	GTM_TIM0_IN3_4			<b>Mux input channel 3 of TIM module 0</b>
	PSI5_RX3C			<b>RXD inputs (receive data) channel 3</b>
	ASCLIN2_ARXD			<b>Receive input</b>
	QSPI3_MTSRB			<b>Slave SPI data input</b>
	PMS_HWCFG5IN			<b>HWCFG5 pin input</b>
	P10.6			O0
	GTM_TOUT108	O1	<b>GTM muxed output</b>	
	IOM_REF2_10		<b>Reference input 2</b>	
	ASCLIN2_ASCLK	O2	<b>Shift clock output</b>	
	QSPI3_MTSR	O3	<b>Master SPI data output</b>	
	GPT120_T3OUT	O4	<b>External output for overflow/underflow detection of core timer T3</b>	
	CAN20_TXD	O5	<b>CAN transmit output node 0</b>	
	QSPI1_MRST	O6	<b>Slave SPI data output</b>	
	IOM_MON2_1		<b>Monitor input 2</b>	
	IOM_REF2_1		<b>Reference input 2</b>	
	EVADC_FC7BFLOUT	O7	<b>Boundary flag output, FC channel 7</b>	

表 2-46 端口 P10 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
J5	P10.7	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN0_3			<b>Mux input channel 0 of TIM module 1</b>
	GTM_TIM0_IN0_3			<b>Mux input channel 0 of TIM module 0</b>
	GPT120_T3EUIDB			<b>Count direction control input of core timer T3</b>
	ASCLIN2_ACTSA			<b>Clear to send input</b>
	QSPI3_MRSTB			<b>Master SPI data input</b>
	SCU_E_REQ0_2			<b>ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	CCU60_CCPOS1C			<b>Hall capture input 1</b>
	P10.7	O0	<b>General-purpose output</b>	
	GTM_TOUT109	O1	<b>GTM muxed output</b>	
	IOM_REF2_11	O2	<b>Reference input 2</b>	
	—		<b>Reserved</b>	
	QSPI3_MRST	O3	<b>Slave SPI data output</b>	
	IOM_MON2_3		<b>Monitor input 2</b>	
	IOM_REF2_3		<b>Reference input 2</b>	
	—	O4	<b>Reserved</b>	
	CAN20_TXD	O5	<b>CAN transmit output node 0</b>	
	CAN12_TXD	O6	<b>CAN transmit output node 2</b>	
	—	O7	<b>Reserved</b>	

表 2-46 端口 P10 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
J4	P10.8	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>	
	GTM_TIM4_IN0_13			<b>Mux input channel 0 of TIM module 4</b>	
	GTM_TIM1_IN5_2			<b>Mux input channel 5 of TIM module 1</b>	
	GTM_TIM0_IN5_2			<b>Mux input channel 5 of TIM module 0</b>	
	CAN12_RXDB			<b>CAN receive input node 2</b>	
	GPT120_T4INB			<b>Trigger/gate input of timer T4</b>	
	QSPI3_SCLKB			<b>Slave SPI clock inputs</b>	
	SCU_E_REQ1_2			<b>ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>	
	CCU60_CCPOS2C			<b>Hall capture input 2</b>	
	CAN20_RXDB			<b>CAN receive input node 0</b>	
	RIF1_RAMP1B			<b>External RAMP B input</b>	
	P10.8			O0	<b>General-purpose output</b>
	GTM_TOUT110			O1	<b>GTM muxed output</b>
	ASCLIN2_ARTS	O2	<b>Ready to send output</b>		
	QSPI3_SCLK	O3	<b>Master SPI clock output</b>		
	—	O4	<b>Reserved</b>		
	—	O5	<b>Reserved</b>		
	—	O6	<b>Reserved</b>		
	—	O7	<b>Reserved</b>		

表 2-47 端口 P11 功能

Ball	Symbol	Ctrl.	Buffer Type	Function	
E10	P11.0	I	RFAST / PU1 / VFLEX / ES	<b>General-purpose input</b>	
	GTM_TIM7_IN5_1			<b>Mux input channel 5 of TIM module 7</b>	
	GTM_TIM4_IN0_4			<b>Mux input channel 0 of TIM module 4</b>	
	GTM_TIM2_IN0_7			<b>Mux input channel 0 of TIM module 2</b>	
	ASCLIN3_ARXB			<b>Receive input</b>	
	GTM_DTMA2_1			<b>CDTM2_DTM4</b>	
	P11.0			O0	<b>General-purpose output</b>
	GTM_TOUT119			O1	<b>GTM muxed output</b>
	ASCLIN3_ATX			O2	<b>Transmit output</b>
	IOM_MON2_15				<b>Monitor input 2</b>
	IOM_REF2_15				<b>Reference input 2</b>
	—	O3	<b>Reserved</b>		
	—	O4	<b>Reserved</b>		
	CAN11_TXD	O5	<b>CAN transmit output node 1</b>		
	GETH_TXD3	O6	<b>Transmit Data</b>		
—	O7	<b>Reserved</b>			
E9	P11.1	I	RFAST / PU1 / VFLEX / ES	<b>General-purpose input</b>	
	GTM_TIM7_IN6_1			<b>Mux input channel 6 of TIM module 7</b>	
	GTM_TIM4_IN1_5			<b>Mux input channel 1 of TIM module 4</b>	
	GTM_TIM2_IN1_6			<b>Mux input channel 1 of TIM module 2</b>	
	P11.1			O0	<b>General-purpose output</b>
	GTM_TOUT120			O1	<b>GTM muxed output</b>
	ASCLIN3_ASCLK			O2	<b>Shift clock output</b>
	ASCLIN3_ATX			O3	<b>Transmit output</b>
	IOM_MON2_15				<b>Monitor input 2</b>
	IOM_REF2_15				<b>Reference input 2</b>
	—			O4	<b>Reserved</b>
	CAN12_TXD	O5	<b>CAN transmit output node 2</b>		
	GETH_TXD2	O6	<b>Transmit Data</b>		
	—	O7	<b>Reserved</b>		

表 2-47 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A12	P11.2	I	RFAST / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM3_IN1_3			Mux input channel 1 of TIM module 3
	GTM_TIM2_IN1_3			Mux input channel 1 of TIM module 2
	P11.2	O0		General-purpose output
	GTM_TOUT95	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO5	O3		Master slave select output
	QSPI1_SLSO5	O4		Master slave select output
	MSC0_EN1	O5		Chip Select
	GETH_TXD1	O6		Transmit Data
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1
B12	P11.3	I	RFAST / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM3_IN2_2			Mux input channel 2 of TIM module 3
	GTM_TIM2_IN2_2			Mux input channel 2 of TIM module 2
	MSC0_SDI3			Upstream asynchronous input signal
	QSPI1_MRSTB			Master SPI data input
	P11.3	O0		General-purpose output
	GTM_TOUT96	O1		GTM muxed output
	—	O2		Reserved
	QSPI1_MRST	O3		Slave SPI data output
	IOM_MON2_1			Monitor input 2
	IOM_REF2_1			Reference input 2
	ERAY0_TXDA			O4
	—	O5		Reserved
	GETH_TXD0	O6		Transmit Data
	CCU60_COUT62	O7		T12 PWM channel 62
	IOM_MON1_5			Monitor input 1
IOM_REF1_1	Reference input 1			

表 2-47 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
D10	P11.4	I	RFAST / PU1 / VFLEX / ES	<b>General-purpose input</b>
	GTM_TIM7_IN7_1			<b>Mux input channel 7 of TIM module 7</b>
	GTM_TIM4_IN2_5			<b>Mux input channel 2 of TIM module 4</b>
	GTM_TIM2_IN2_6			<b>Mux input channel 2 of TIM module 2</b>
	GETH_RXCLKB			<b>Receive Clock MII</b>
	P11.4	O0		<b>General-purpose output</b>
	GTM_TOUT121	O1		<b>GTM muxed output</b>
	ASCLIN3_ASCLK	O2		<b>Shift clock output</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	CAN13_TXD	O5		<b>CAN transmit output node 3</b>
	GETH_TXER	O6		<b>Transmit Error MII</b>
	GETH_TXCLK	O7		<b>Transmit Clock Output for RGMII</b>
D8	P11.5	I	SLOW / RGMII_In put / PU1 / VFLEX / ES	<b>General-purpose input</b>
	GTM_TIM4_IN3_5			<b>Mux input channel 3 of TIM module 4</b>
	GTM_TIM2_IN3_8			<b>Mux input channel 3 of TIM module 2</b>
	GETH_TXCLKA			<b>Transmit Clock Input for MII</b>
	GETH_GREFCLK			<b>Gigabit Reference Clock input for RGMII (125 MHz high precision)</b>
	P11.5	O0		<b>General-purpose output</b>
	GTM_TOUT122	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	CAN20_TXD	O5		<b>CAN transmit output node 0</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>

表 2-47 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
D9	P11.6	I	RFAST / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM3_IN3_2			Mux input channel 3 of TIM module 3
	GTM_TIM2_IN3_2			Mux input channel 3 of TIM module 2
	QSPI1_SCLKB			Slave SPI clock inputs
	P11.6	O0		General-purpose output
	GTM_TOUT97	O1		GTM muxed output
	ERAY0_TXENB	O2		Transmit Enable Channel B
	QSPI1_SCLK	O3		Master SPI clock output
	ERAY0_TXENA	O4		Transmit Enable Channel A
	MSC0_FCLP	O5		Shift-clock direct part of the differential signal
	GETH_TXEN	O6		Transmit Enable MII and RMII
	GETH_TCTL			Transmit Control for RGMII
	CCU60_COUT61	O7		T12 PWM channel 61
	IOM_MON1_4			Monitor input 1
IOM_REF1_2		Reference input 1		
E8	P11.7	I	SLOW / RGMII_In put / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM4_IN4_5			Mux input channel 4 of TIM module 4
	GTM_TIM2_IN4_7			Mux input channel 4 of TIM module 2
	GETH_RXD3A			Receive Data 3 MII and RGMII (RGMII can use RXD3A only)
	CAN11_RXDD			CAN receive input node 1
	P11.7	O0		General-purpose output
	GTM_TOUT123	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-47 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
E7	P11.8	I	SLOW / RGMII_In put / PU1 / VFLEX / ES	<b>General-purpose input</b>
	GTM_TIM4_IN5_5			<b>Mux input channel 5 of TIM module 4</b>
	GTM_TIM2_IN5_8			<b>Mux input channel 5 of TIM module 2</b>
	GETH_RXD2A			<b>Receive Data 2 MII and RGMII (RGMII can use RXD2A only)</b>
	CAN12_RXDD			<b>CAN receive input node 2</b>
	P11.8	O0		<b>General-purpose output</b>
	GTM_TOUT124	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
A11	P11.9	I	FAST / RGMII_In put / PU1 / VFLEX / ES	<b>General-purpose input</b>
	GTM_TIM3_IN4_2			<b>Mux input channel 4 of TIM module 3</b>
	GTM_TIM2_IN4_2			<b>Mux input channel 4 of TIM module 2</b>
	QSPI1_MTSRB			<b>Slave SPI data input</b>
	ERAY0_RXDA1			<b>Receive Channel A1</b>
	GETH_RXD1A			<b>Receive Data 1 MII, RMII and RGMII (RGMII can use RXD1A only)</b>
	P11.9	O0		<b>General-purpose output</b>
	GTM_TOUT98	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	QSPI1_MTSR	O3		<b>Master SPI data output</b>
	—	O4		<b>Reserved</b>
	MSC0_SOP	O5		<b>Data output - direct part of the differential signal</b>
	—	O6		<b>Reserved</b>
	CCU60_COUT60	O7		<b>T12 PWM channel 60</b>
	IOM_MON1_3			<b>Monitor input 1</b>
IOM_REF1_3		<b>Reference input 1</b>		

表 2-47 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
B11	P11.10	I	FAST / RGMII_Input / PU1 / VFLEX / ES	<b>General-purpose input</b>	
	GTM_TIM3_IN5_2			<b>Mux input channel 5 of TIM module 3</b>	
	GTM_TIM2_IN5_2			<b>Mux input channel 5 of TIM module 2</b>	
	GTM_TIM2_IN0_9			<b>Mux input channel 0 of TIM module 2</b>	
	CAN03_RXDD			<b>CAN receive input node 3</b>	
	ERAY0_RXDB1			<b>Receive Channel B1</b>	
	ASCLIN1_ARXE			<b>Receive input</b>	
	SCU_E_REQ6_3			<b>ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>	
	MSC0_SDI0			<b>Upstream asynchronous input signal</b>	
	GETH_RXD0A			<b>Receive Data 0 MII, RMII and RGMII (RGMII can use RXD0A only)</b>	
	QSPI1_SLSIA			<b>Slave select input</b>	
	P11.10			O0	<b>General-purpose output</b>
	GTM_TOUT99			O1	<b>GTM muxed output</b>
	—	O2	<b>Reserved</b>		
	QSPI0_SLSO3	O3	<b>Master slave select output</b>		
	QSPI1_SLSO3	O4	<b>Master slave select output</b>		
	—	O5	<b>Reserved</b>		
	—	O6	<b>Reserved</b>		
	CCU60_CC62	O7	<b>T12 PWM channel 62</b>		
IOM_MON1_0	<b>Monitor input 1</b>				
IOM_REF1_4	<b>Reference input 1</b>				

表 2-47 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A10	P11.11	I	FAST / RGMII_In put / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM3_IN6_2			Mux input channel 6 of TIM module 3
	GTM_TIM3_IN0_14			Mux input channel 0 of TIM module 3
	GTM_TIM2_IN6_2			Mux input channel 6 of TIM module 2
	GETH_CRSDVA			Carrier Sense / Data Valid combi-signal for RMII
	GETH_RXDVA			Receive Data Valid MII
	GETH_CRSB			Carrier Sense MII
	GETH_RCTLA			Receive Control for RGMII
	P11.11			O0
	GTM_TOUT100	O1	GTM muxed output	
	—	O2	Reserved	
	QSPI0_SLSO4	O3	Master slave select output	
	QSPI1_SLSO4	O4	Master slave select output	
	MSC0_EN0	O5	Chip Select	
	ERAY0_TXENB	O6	Transmit Enable Channel B	
	CCU60_CC61	O7	T12 PWM channel 61	
	IOM_MON1_1		Monitor input 1	
IOM_REF1_5	Reference input 1			
B10	P11.12	I	FAST / RGMII_In put / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM3_IN7_2			Mux input channel 7 of TIM module 3
	GTM_TIM2_IN7_2			Mux input channel 7 of TIM module 2
	GETH_REFCLKA			Reference Clock input for RMII (50 MHz)
	GETH_TXCLKB			Transmit Clock Input for MII
	GETH_RXCLKA			Receive Clock MII
	P11.12	O0	General-purpose output	
	GTM_TOUT101	O1	GTM muxed output	
	ASCLIN1_ATX	O2	Transmit output	
	IOM_MON2_13		Monitor input 2	
	IOM_REF2_13		Reference input 2	
	GTM_CLK2	O3	CGM generated clock	
	ERAY0_TXDB	O4	Transmit Channel B	
	CAN03_TXD	O5	CAN transmit output node 3	
	IOM_MON2_8		Monitor input 2	
	IOM_REF2_8	O6	Reference input 2	
	CCU_EXTCLK1		External Clock 1	
	CCU60_CC60		T12 PWM channel 60	
	IOM_MON1_2	O7	Monitor input 1	
IOM_REF1_6	Reference input 1			

表 2-47 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
E6	P11.13	I	SLOW / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM4_IN6_5			Mux input channel 6 of TIM module 4
	GTM_TIM2_IN6_7			Mux input channel 6 of TIM module 2
	GETH_RXERA			Receive Error MII
	I2C1_SDAA			Serial Data Input 0
	CAN13_RXDD			CAN receive input node 3
	P11.13			00
	GTM_TOUT125	01		GTM muxed output
	—	02		Reserved
	—	03		Reserved
	—	04		Reserved
	—	05		Reserved
	I2C1_SDA	06		Serial Data Output
	—	07		Reserved
D7	P11.14	I	SLOW / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM4_IN7_4			Mux input channel 7 of TIM module 4
	GTM_TIM2_IN7_8			Mux input channel 7 of TIM module 2
	GETH_CRSDVB			Carrier Sense / Data Valid combi-signal for RMII
	GETH_RXDVB			Receive Data Valid MII
	GETH_CRSA			Carrier Sense MII
	I2C1_SCLA			Serial Clock Input 0
	CAN20_RXDF	CAN receive input node 0		
	P11.14	00		General-purpose output
	GTM_TOUT126	01		GTM muxed output
	—	02		Reserved
	—	03		Reserved
	—	04		Reserved
	—	05		Reserved
I2C1_SCL	06	Serial Clock Output		
—	07	Reserved		

表 2-47 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
D6	P11.15	I	SLOW / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM4_IN7_5			Mux input channel 7 of TIM module 4
	GTM_TIM0_IN7_8			Mux input channel 7 of TIM module 0
	GETH_COLA			Collision MII
	P11.15	O0		General-purpose output
	GTM_TOUT127	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-48 端口 P12 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
E12	P12.0	I	SLOW / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM7_IN3_2			Mux input channel 3 of TIM module 7
	GTM_TIM4_IN0_5			Mux input channel 0 of TIM module 4
	GTM_TIM3_IN0_7			Mux input channel 0 of TIM module 3
	CAN00_RXDC			CAN receive input node 0
	GETH_RXCLKC			Receive Clock MII
	GTM_DTMA4_0			CDTM4_DTM4
	P12.0	O0		General-purpose output
	GTM_TOUT128	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
GETH_MDC	O6	MDIO clock		
—	O7	Reserved		

表 2-48 端口 P12 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
E11	P12.1	I	SLOW / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM7_IN4_1			Mux input channel 4 of TIM module 7
	GTM_TIM4_IN1_6			Mux input channel 1 of TIM module 4
	GTM_TIM3_IN1_6			Mux input channel 1 of TIM module 3
	GETH_MDIOC			MDIO Input
	P12.1	O0		General-purpose output
	GTM_TOUT129	O1		GTM muxed output
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	CAN00_TXD	O5		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	—	O6		Reserved
	—	O7		Reserved
	GETH_MDIO	O		MDIO Output

表 2-49 端口 P14 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
B16	P14.0	I	FAST / PU1 / VEXT / ES2	General-purpose input
	GTM_TIM1_IN3_5			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_5			Mux input channel 3 of TIM module 0
	SENT_SENT17D			Receive input channel 17
	P14.0	O0		General-purpose output
	GTM_TOUT80	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	ERAY0_TXDA	O3		Transmit Channel A
	ERAY0_TXDB	O4		Transmit Channel B
	CAN01_TXD	O5		CAN transmit output node 1
	IOM_MON2_6			Monitor input 2
	IOM_REF2_6	O6		Reference input 2
	ASCLIN0_ASCLK			Shift clock output
	CCU60_COUT62			T12 PWM channel 62
	IOM_MON1_5	O7		Monitor input 1
	IOM_REF1_1			Reference input 1

表 2-49 端口 P14 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A15	P14.1	I	FAST / PU1 / VEXT / ES2	<b>General-purpose input</b>
	GTM_TIM1_IN4_3			<b>Mux input channel 4 of TIM module 1</b>
	GTM_TIM0_IN4_3			<b>Mux input channel 4 of TIM module 0</b>
	ERAY0_RXDA3			<b>Receive Channel A3</b>
	ASCLIN0_ARXA			<b>Receive input</b>
	SENT_SENT18D			<b>Receive input channel 18</b>
	ERAY0_RXDB3			<b>Receive Channel B3</b>
	CAN01_RXDB			<b>CAN receive input node 1</b>
	SCU_E_REQ3_1			<b>ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	PMS_PINAWKP			<b>PINA ( P14.1) pin input</b>
	P14.1	00	<b>General-purpose output</b>	
	GTM_TOUT81	01	<b>GTM muxed output</b>	
	ASCLIN0_ATX	02	<b>Transmit output</b>	
	IOM_MON2_12		<b>Monitor input 2</b>	
	IOM_REF2_12	<b>Reference input 2</b>		
	—	03	<b>Reserved</b>	
	—	04	<b>Reserved</b>	
	—	05	<b>Reserved</b>	
	—	06	<b>Reserved</b>	
	CCU60_COUT63	07	<b>T13 PWM channel 63</b>	
IOM_MON1_6	<b>Monitor input 1</b>			
IOM_REF1_0	<b>Reference input 1</b>			
E13	P14.2	I	SLOW / PU2 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN5_3			<b>Mux input channel 5 of TIM module 1</b>
	GTM_TIM0_IN5_3			<b>Mux input channel 5 of TIM module 0</b>
	PMS_HWCFG2IN			<b>HWCFG2 pin input</b>
	P14.2	00	<b>General-purpose output</b>	
	GTM_TOUT82	01	<b>GTM muxed output</b>	
	ASCLIN2_ATX	02	<b>Transmit output</b>	
	IOM_MON2_14		<b>Monitor input 2</b>	
	IOM_REF2_14		<b>Reference input 2</b>	
	QSPI2_SLSO1	03	<b>Master slave select output</b>	
	—	04	<b>Reserved</b>	
	—	05	<b>Reserved</b>	
	ASCLIN2_ASCLK	06	<b>Shift clock output</b>	
	—	07	<b>Reserved</b>	

表 2-49 端口 P14 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
B14	P14.3	I	SLOW / PU2 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN6_3			<b>Mux input channel 6 of TIM module 1</b>
	GTM_TIM0_IN6_3			<b>Mux input channel 6 of TIM module 0</b>
	PMS_HWCFG3IN			<b>HWCFG3 pin input</b>
	ASCLIN2_ARXA			<b>Receive input</b>
	MSC0_SDI2			<b>Upstream asynchronous input signal</b>
	SCU_E_REQ1_0			<b>ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	P14.3	O0	<b>General-purpose output</b>	
	GTM_TOUT83	O1	<b>GTM muxed output</b>	
	ASCLIN2_ATX	O2	<b>Transmit output</b>	
	IOM_MON2_14		<b>Monitor input 2</b>	
	IOM_REF2_14		<b>Reference input 2</b>	
	QSPI2_SLSO3	O3	<b>Master slave select output</b>	
	ASCLIN1_ASLSO	O4	<b>Slave select signal output</b>	
	ASCLIN3_ASLSO	O5	<b>Slave select signal output</b>	
	—	O6	<b>Reserved</b>	
	—	O7	<b>Reserved</b>	
B15	P14.4	I	SLOW / PU2 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN7_2			<b>Mux input channel 7 of TIM module 1</b>
	GTM_TIM0_IN7_2			<b>Mux input channel 7 of TIM module 0</b>
	PMS_HWCFG6IN			<b>HWCFG6 pin input</b>
	GTM_DTMT0_0			<b>CDTMO_DTM0</b>
	P14.4	O0	<b>General-purpose output</b>	
	GTM_TOUT84	O1	<b>GTM muxed output</b>	
	—	O2	<b>Reserved</b>	
	—	O3	<b>Reserved</b>	
	—	O4	<b>Reserved</b>	
	—	O5	<b>Reserved</b>	
	GETH_PPS	O6	<b>Pulse Per Second</b>	
	—	O7	<b>Reserved</b>	

表 2-49 端口 P14 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A14	P14.5	I	FAST / PU2 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN0_4			<b>Mux input channel 0 of TIM module 1</b>
	GTM_TIM0_IN0_4			<b>Mux input channel 0 of TIM module 0</b>
	PMS_HWCFG1IN			<b>HWCFG1 pin input</b>
	QSPI5_MRSTB			<b>Master SPI data input</b>
	GTM_DTMA2_0			<b>CDTM2_DTM4</b>
	P14.5			O0
	GTM_TOUT85	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	QSPI5_MRST	O3		<b>Slave SPI data output</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	ERAY0_TXDB	O6		<b>Transmit Channel B</b>
	ERAY1_TXDB	O7		<b>Transmit Channel B</b>
B13	P14.6	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN1_4			<b>Mux input channel 1 of TIM module 1</b>
	GTM_TIM0_IN1_4			<b>Mux input channel 1 of TIM module 0</b>
	QSPI5_MTSRB			<b>Slave SPI data input</b>
	P14.6	O0		<b>General-purpose output</b>
	GTM_TOUT86	O1		<b>GTM muxed output</b>
	QSPI5_MTSR	O2		<b>Master SPI data output</b>
	QSPI2_SLSO2	O3		<b>Master slave select output</b>
	CAN13_TXD	O4		<b>CAN transmit output node 3</b>
	—	O5		<b>Reserved</b>
	ERAY0_TXENB	O6		<b>Transmit Enable Channel B</b>
	ERAY1_TXENB	O7		<b>Transmit Enable Channel B</b>

表 2-49 端口 P14 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
D13	P14.7	I	SLOW / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM4_IN7_10			Mux input channel 7 of TIM module 4	
	GTM_TIM1_IN0_5			Mux input channel 0 of TIM module 1	
	GTM_TIM0_IN0_5			Mux input channel 0 of TIM module 0	
	ERAY0_RXDB0			Receive Channel B0	
	ERAY1_RXDB0			Receive Channel B0	
	CAN10_RXDB			CAN receive input node 0	
	CAN13_RXDA			CAN receive input node 3	
	ASCLIN9_ARXC			Receive input	
	P14.7			O0	General-purpose output
	GTM_TOUT87	O1	GTM muxed output		
	ASCLIN0_ARTS	O2	Ready to send output		
	QSPI2_SLSO4	O3	Master slave select output		
	ASCLIN9_ATX	O4	Transmit output		
	—	O5	Reserved		
	—	O6	Reserved		
	—	O7	Reserved		
A13	P14.8	I	SLOW / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM3_IN2_3			Mux input channel 2 of TIM module 3	
	GTM_TIM2_IN2_3			Mux input channel 2 of TIM module 2	
	ERAY0_RXDA0			Receive Channel A0	
	CAN02_RXDD			CAN receive input node 2	
	ASCLIN1_ARXD			Receive input	
	ERAY1_RXDA0			Receive Channel A0	
	P14.8			O0	General-purpose output
	GTM_TOUT88			O1	GTM muxed output
	ASCLIN5_ASLSO			O2	Slave select signal output
	ASCLIN7_ASLSO	O3	Slave select signal output		
	—	O4	Reserved		
	—	O5	Reserved		
	—	O6	Reserved		
	—	O7	Reserved		

表 2-49 端口 P14 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
D12	P14.9	I	LVDS_RX / FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM3_IN3_3			<b>Mux input channel 3 of TIM module 3</b>
	GTM_TIM2_IN3_3			<b>Mux input channel 3 of TIM module 2</b>
	ASCLIN0_ACTSA			<b>Clear to send input</b>
	QSPI2_MRSTFN			<b>Master SPI data input (LVDS N line)</b>
	ASCLIN9_ARXD			<b>Receive input</b>
	P14.9			O0
	GTM_TOUT89	O1	<b>GTM muxed output</b>	
	CAN23_TXD	O2	<b>CAN transmit output node 3</b>	
	MSC0_EN1	O3	<b>Chip Select</b>	
	CAN10_TXD	O4	<b>CAN transmit output node 0</b>	
	ERAY0_TXENB	O5	<b>Transmit Enable Channel B</b>	
	ERAY0_TXENA	O6	<b>Transmit Enable Channel A</b>	
	ERAY1_TXENA	O7	<b>Transmit Enable Channel A</b>	
D11	P14.10	I	LVDS_RX / FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM3_IN4_3			<b>Mux input channel 4 of TIM module 3</b>
	GTM_TIM2_IN4_3			<b>Mux input channel 4 of TIM module 2</b>
	CAN23_RXDA			<b>CAN receive input node 3</b>
	QSPI2_MRSTFP			<b>Master SPI data input (LVDS P line)</b>
	P14.10	O0	<b>General-purpose output</b>	
	GTM_TOUT90	O1	<b>GTM muxed output</b>	
	QSPI5_SCLK	O2	<b>Master SPI clock output</b>	
	MSC0_EN0	O3	<b>Chip Select</b>	
	ASCLIN1_ATX	O4	<b>Transmit output</b>	
	IOM_MON2_13		<b>Monitor input 2</b>	
	IOM_REF2_13		<b>Reference input 2</b>	
	CAN02_TXD	O5	<b>CAN transmit output node 2</b>	
	IOM_MON2_7		<b>Monitor input 2</b>	
	IOM_REF2_7		<b>Reference input 2</b>	
	ERAY0_TXDA	O6	<b>Transmit Channel A</b>	
ERAY1_TXDA	O7	<b>Transmit Channel A</b>		

表 2-50 端口 P15 功能

Ball	Symbol	Ctrl.	Buffer Type	Function	
B20	P15.0	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>	
	GTM_TIM3_IN3_4			<b>Mux input channel 3 of TIM module 3</b>	
	GTM_TIM2_IN3_4			<b>Mux input channel 3 of TIM module 2</b>	
	SDMMC0_DAT7_IN			<b>read data in</b>	
	P15.0			O0	<b>General-purpose output</b>
	GTM_TOUT71			O1	<b>GTM muxed output</b>
	ASCLIN1_ATX			O2	<b>Transmit output</b>
	IOM_MON2_13				<b>Monitor input 2</b>
	IOM_REF2_13				<b>Reference input 2</b>
	QSPI0_SLSO13			O3	<b>Master slave select output</b>
	—	O4	<b>Reserved</b>		
	CAN02_TXD	O5	<b>CAN transmit output node 2</b>		
	IOM_MON2_7		<b>Monitor input 2</b>		
	IOM_REF2_7		<b>Reference input 2</b>		
	ASCLIN1_ASCLK	O6	<b>Shift clock output</b>		
	—	O7	<b>Reserved</b>		
	SDMMC0_DAT7	O	<b>write data out</b>		
A18	P15.1	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>	
	GTM_TIM3_IN4_4			<b>Mux input channel 4 of TIM module 3</b>	
	GTM_TIM2_IN4_4			<b>Mux input channel 4 of TIM module 2</b>	
	CAN02_RXDA			<b>CAN receive input node 2</b>	
	ASCLIN1_ARXA			<b>Receive input</b>	
	QSPI2_SLSIB			<b>Slave select input</b>	
	SCU_E_REQ7_2			<b>ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>	
	P15.1			O0	<b>General-purpose output</b>
	GTM_TOUT72			O1	<b>GTM muxed output</b>
	ASCLIN1_ATX			O2	<b>Transmit output</b>
	IOM_MON2_13	<b>Monitor input 2</b>			
	IOM_REF2_13	<b>Reference input 2</b>			
	QSPI2_SLSO5	O3	<b>Master slave select output</b>		
	—	O4	<b>Reserved</b>		
	—	O5	<b>Reserved</b>		
	—	O6	<b>Reserved</b>		
	SDMMC0_CLK	O7	<b>card clock</b>		

表 2-50 端口 P15 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
C19	P15.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN5_4			Mux input channel 5 of TIM module 3
	GTM_TIM2_IN5_4			Mux input channel 5 of TIM module 2
	QSPI2_SLSIA			Slave select input
	SENT_SENT10D			Receive input channel 10
	QSPI2_MRSTE			Master SPI data input
	QSPI2_HSICINA			Highspeed capture channel
	P15.2			O0
	GTM_TOUT73	O1	GTM muxed output	
	ASCLIN0_ATX	O2	Transmit output	
	IOM_MON2_12		Monitor input 2	
	IOM_REF2_12		Reference input 2	
	QSPI2_SLSO0	O3	Master slave select output	
	—	O4	Reserved	
	CAN01_TXD	O5	CAN transmit output node 1	
	IOM_MON2_6		Monitor input 2	
	IOM_REF2_6		Reference input 2	
	ASCLIN0_ASCLK	O6	Shift clock output	
	—	O7	Reserved	
	B17	P15.3	I	FAST / PU1 / VEXT / ES
GTM_TIM3_IN6_4		Mux input channel 6 of TIM module 3		
GTM_TIM2_IN6_4		Mux input channel 6 of TIM module 2		
CAN01_RXDA		CAN receive input node 1		
ASCLIN0_ARXB		Receive input		
QSPI2_SCLKA		Slave SPI clock inputs		
QSPI2_HSICINB		Highspeed capture channel		
SDMMC0_CMD_IN		command in		
P15.3		O0	General-purpose output	
GTM_TOUT74		O1	GTM muxed output	
ASCLIN0_ATX		O2	Transmit output	
IOM_MON2_12			Monitor input 2	
IOM_REF2_12			Reference input 2	
QSPI2_SCLK		O3	Master SPI clock output	
—		O4	Reserved	
MSC0_EN1		O5	Chip Select	
—		O6	Reserved	
—		O7	Reserved	
SDMMC0_CMD		O	command out	

表 2-50 端口 P15 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A17	P15.4	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM3_IN7_4			<b>Mux input channel 7 of TIM module 3</b>
	GTM_TIM2_IN7_4			<b>Mux input channel 7 of TIM module 2</b>
	I2C0_SCLC			<b>Serial Clock Input 2</b>
	QSPI2_MRSTA			<b>Master SPI data input</b>
	SCU_E_REQ0_0			<b>ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	SENT_SENT11D			<b>Receive input channel 11</b>
	P15.4			O0
	GTM_TOUT75	O1	<b>GTM muxed output</b>	
	ASCLIN1_ATX	O2	<b>Transmit output</b>	
	IOM_MON2_13		<b>Monitor input 2</b>	
	IOM_REF2_13		<b>Reference input 2</b>	
	QSPI2_MRST	O3	<b>Slave SPI data output</b>	
	IOM_MON2_2		<b>Monitor input 2</b>	
	IOM_REF2_2		<b>Reference input 2</b>	
	—	O4	<b>Reserved</b>	
	—	O5	<b>Reserved</b>	
	I2C0_SCL	O6	<b>Serial Clock Output</b>	
	CCU60_CC62	O7	<b>T12 PWM channel 62</b>	
	IOM_MON1_0		<b>Monitor input 1</b>	
IOM_REF1_4	<b>Reference input 1</b>			

表 2-50 端口 P15 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
E14	P15.5	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM3_IN0_4			<b>Mux input channel 0 of TIM module 3</b>
	GTM_TIM2_IN0_4			<b>Mux input channel 0 of TIM module 2</b>
	ASCLIN1_ARXB			<b>Receive input</b>
	I2C0_SDAC			<b>Serial Data Input 2</b>
	QSPI2_MTSRA			<b>Slave SPI data input</b>
	SCU_E_REQ4_3			<b>ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	P15.5	O0	<b>General-purpose output</b>	
	GTM_TOUT76	O1	<b>GTM muxed output</b>	
	ASCLIN1_ATX	O2	<b>Transmit output</b>	
	IOM_MON2_13		<b>Monitor input 2</b>	
	IOM_REF2_13		<b>Reference input 2</b>	
	QSPI2_MTSR	O3	<b>Master SPI data output</b>	
	—	O4	<b>Reserved</b>	
	MSC0_EN0	O5	<b>Chip Select</b>	
	I2C0_SDA	O6	<b>Serial Data Output</b>	
	CCU60_CC61	O7	<b>T12 PWM channel 61</b>	
	IOM_MON1_1		<b>Monitor input 1</b>	
	IOM_REF1_5		<b>Reference input 1</b>	
A16	P15.6	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM2_IN2_14			<b>Mux input channel 2 of TIM module 2</b>
	GTM_TIM1_IN0_6			<b>Mux input channel 0 of TIM module 1</b>
	GTM_TIM0_IN0_6			<b>Mux input channel 0 of TIM module 0</b>
	QSPI2_MTSRB			<b>Slave SPI data input</b>
	P15.6	O0	<b>General-purpose output</b>	
	GTM_TOUT77	O1	<b>GTM muxed output</b>	
	ASCLIN3_ATX	O2	<b>Transmit output</b>	
	IOM_MON2_15		<b>Monitor input 2</b>	
	IOM_REF2_15		<b>Reference input 2</b>	
	QSPI2_MTSR	O3	<b>Master SPI data output</b>	
	QSPI5_SLSO3	O4	<b>Master slave select output</b>	
	QSPI2_SCLK	O5	<b>Master SPI clock output</b>	
	ASCLIN3_ASCLK	O6	<b>Shift clock output</b>	
	CCU60_CC60	O7	<b>T12 PWM channel 60</b>	
	IOM_MON1_2		<b>Monitor input 1</b>	
	IOM_REF1_6		<b>Reference input 1</b>	

表 2-50 端口 P15 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
D15	P15.7	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN1_5			<b>Mux input channel 1 of TIM module 1</b>
	GTM_TIM0_IN1_5			<b>Mux input channel 1 of TIM module 0</b>
	ASCLIN3_ARXA			<b>Receive input</b>
	QSPI2_MRSTB			<b>Master SPI data input</b>
	P15.7	O0		<b>General-purpose output</b>
	GTM_TOUT78	O1		<b>GTM muxed output</b>
	ASCLIN3_ATX	O2		<b>Transmit output</b>
	IOM_MON2_15			<b>Monitor input 2</b>
	IOM_REF2_15			<b>Reference input 2</b>
	QSPI2_MRST	O3		<b>Slave SPI data output</b>
	IOM_MON2_2			<b>Monitor input 2</b>
	IOM_REF2_2			<b>Reference input 2</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	CCU60_COUT60	O7		<b>T12 PWM channel 60</b>
IOM_MON1_3	<b>Monitor input 1</b>			
IOM_REF1_3	<b>Reference input 1</b>			
D14	P15.8	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN2_5			<b>Mux input channel 2 of TIM module 1</b>
	GTM_TIM0_IN2_5			<b>Mux input channel 2 of TIM module 0</b>
	QSPI2_SCLKB			<b>Slave SPI clock inputs</b>
	SCU_E_REQ5_0			<b>ERU Channel 5 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	P15.8	O0		<b>General-purpose output</b>
	GTM_TOUT79	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	QSPI2_SCLK	O3		<b>Master SPI clock output</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	ASCLIN3_ASCLK	O6		<b>Shift clock output</b>
	CCU60_COUT61	O7		<b>T12 PWM channel 61</b>
	IOM_MON1_4			<b>Monitor input 1</b>
	IOM_REF1_2			<b>Reference input 1</b>

表 2-51 端口 P20 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
H20	P20.0	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN6_7			<b>Mux input channel 6 of TIM module 1</b>
	GTM_TIM1_IN4_9			<b>Mux input channel 4 of TIM module 1</b>
	GTM_TIM0_IN6_7			<b>Mux input channel 6 of TIM module 0</b>
	CAN03_RXDC			<b>CAN receive input node 3</b>
	CCU_PAD_SYSCLK			<b>Sysclk input</b>
	CAN21_RXDC			<b>CAN receive input node 1</b>
	CBS_TGI0			<b>Trigger input</b>
	SCU_E_REQ6_0			<b>ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	GPT120_T6EUDA			<b>Count direction control input of core timer T6</b>
	P20.0	O0	<b>General-purpose output</b>	
	GTM_TOUT59	O1	<b>GTM muxed output</b>	
	ASCLIN3_ATX	O2	<b>Transmit output</b>	
	IOM_MON2_15		<b>Monitor input 2</b>	
	IOM_REF2_15	O3	<b>Reference input 2</b>	
	ASCLIN3_ASCLK		<b>Shift clock output</b>	
	—	O4	<b>Reserved</b>	
	HSCT0_SYSCLK_OUT	O5	<b>sys clock output</b>	
	—	O6	<b>Reserved</b>	
	—	O7	<b>Reserved</b>	
CBS_TGO0	O	<b>Trigger output</b>		
G19	P20.1	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM4_IN4_11			<b>Mux input channel 4 of TIM module 4</b>
	GTM_TIM3_IN3_5			<b>Mux input channel 3 of TIM module 3</b>
	GTM_TIM2_IN3_5			<b>Mux input channel 3 of TIM module 2</b>
	CBS_TGI1			<b>Trigger input</b>
	GTM_DTMA1_1			<b>CDTM1_DTM4</b>
	P20.1	O0	<b>General-purpose output</b>	
	GTM_TOUT60	O1	<b>GTM muxed output</b>	
	—	O2	<b>Reserved</b>	
	—	O3	<b>Reserved</b>	
	—	O4	<b>Reserved</b>	
	—	O5	<b>Reserved</b>	
	—	O6	<b>Reserved</b>	
	—	O7	<b>Reserved</b>	
	CBS_TGO1	O	<b>Trigger output</b>	

表 2-51 端口 P20 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
H19	P20.2	I	S / PU / VEXT	<b>General-purpose input</b> This pin is latched at power on reset release to enter test mode.
	TESTMODE			<b>Testmode Enable Input</b>
G20	P20.3	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM4_IN5_11			<b>Mux input channel 5 of TIM module 4</b>
	GTM_TIM3_IN4_5			<b>Mux input channel 4 of TIM module 3</b>
	GTM_TIM2_IN4_5			<b>Mux input channel 4 of TIM module 2</b>
	ASCLIN3_ARXC			<b>Receive input</b>
	GPT120_T6INA			<b>Trigger/gate input of core timer T6</b>
	P20.3	O0		<b>General-purpose output</b>
	GTM_TOUT61	O1		<b>GTM muxed output</b>
	ASCLIN3_ATX	O2		<b>Transmit output</b>
	IOM_MON2_15			<b>Monitor input 2</b>
	IOM_REF2_15			<b>Reference input 2</b>
	QSPI0_SLSO9	O3		<b>Master slave select output</b>
	QSPI2_SLSO9	O4		<b>Master slave select output</b>
	CAN03_TXD	O5		<b>CAN transmit output node 3</b>
	IOM_MON2_8			<b>Monitor input 2</b>
	IOM_REF2_8			<b>Reference input 2</b>
	CAN21_TXD	O6		<b>CAN transmit output node 1</b>
	—	O7		<b>Reserved</b>
	F17	P20.6	I	SLOW / PU1 / VEXT / ES
GTM_TIM6_IN0_1			<b>Mux input channel 0 of TIM module 6</b>	
GTM_TIM3_IN6_5			<b>Mux input channel 6 of TIM module 3</b>	
GTM_TIM2_IN6_5			<b>Mux input channel 6 of TIM module 2</b>	
CAN12_RXDA			<b>CAN receive input node 2</b>	
ASCLIN9_ARXE			<b>Receive input</b>	
P20.6		O0		<b>General-purpose output</b>
GTM_TOUT62		O1		<b>GTM muxed output</b>
ASCLIN1_ARTS		O2		<b>Ready to send output</b>
QSPI0_SLSO8		O3		<b>Master slave select output</b>
QSPI2_SLSO8		O4		<b>Master slave select output</b>
—		O5		<b>Reserved</b>
—		O6		<b>Reserved</b>
—		O7		<b>Reserved</b>

表 2-51 端口 P20 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
F19	P20.7	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>	
	GTM_TIM3_IN7_5			<b>Mux input channel 7 of TIM module 3</b>	
	GTM_TIM2_IN7_5			<b>Mux input channel 7 of TIM module 2</b>	
	GTM_TIM1_IN5_8			<b>Mux input channel 5 of TIM module 1</b>	
	GTM_TIM6_IN1_1			<b>Mux input channel 1 of TIM module 6</b>	
	CAN00_RXDB			<b>CAN receive input node 0</b>	
	ASCLIN1_ACTSA			<b>Clear to send input</b>	
	ASCLIN9_ARXF			<b>Receive input</b>	
	SDMMC0_DAT0_IN			<b>read data in</b>	
	P20.7			O0	<b>General-purpose output</b>
	GTM_TOUT63	O1	<b>GTM muxed output</b>		
	ASCLIN9_ATX	O2	<b>Transmit output</b>		
	—	O3	<b>Reserved</b>		
	—	O4	<b>Reserved</b>		
	CAN12_TXD	O5	<b>CAN transmit output node 2</b>		
	—	O6	<b>Reserved</b>		
	CCU61_COUT63	O7	<b>T13 PWM channel 63</b>		
	IOM_MON1_7		<b>Monitor input 1</b>		
	IOM_REF1_7		<b>Reference input 1</b>		
	SDMMC0_DAT0	O	<b>write data out</b>		
F20	P20.8	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>	
	GTM_TIM6_IN2_1			<b>Mux input channel 2 of TIM module 6</b>	
	GTM_TIM1_IN7_3			<b>Mux input channel 7 of TIM module 1</b>	
	GTM_TIM0_IN7_3			<b>Mux input channel 7 of TIM module 0</b>	
	SDMMC0_DAT1_IN			<b>read data in</b>	
	P20.8			O0	<b>General-purpose output</b>
	GTM_TOUT64			O1	<b>GTM muxed output</b>
	ASCLIN1_ASLSO			O2	<b>Slave select signal output</b>
	QSPI0_SLSO0			O3	<b>Master slave select output</b>
	QSPI1_SLSO0			O4	<b>Master slave select output</b>
	CAN00_TXD	O5	<b>CAN transmit output node 0</b>		
	IOM_MON2_5		<b>Monitor input 2</b>		
	IOM_REF2_5		<b>Reference input 2</b>		
	—	O6	<b>Reserved</b>		
	CCU61_CC60	O7	<b>T12 PWM channel 60</b>		
	IOM_MON1_8		<b>Monitor input 1</b>		
	IOM_REF1_13		<b>Reference input 1</b>		
	SDMMC0_DAT1	O	<b>write data out</b>		

表 2-51 端口 P20 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
E17	P20.9	I	FAST / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM6_IN3_1			Mux input channel 3 of TIM module 6	
	GTM_TIM3_IN5_5			Mux input channel 5 of TIM module 3	
	GTM_TIM2_IN5_5			Mux input channel 5 of TIM module 2	
	CAN03_RXDE			CAN receive input node 3	
	ASCLIN1_ARXC			Receive input	
	QSPI0_SLSIB			Slave select input	
	SCU_E_REQ7_0			ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)	
	P20.9			O0	General-purpose output
	GTM_TOUT65	O1	GTM muxed output		
	—	O2	Reserved		
	QSPI0_SLSO1	O3	Master slave select output		
	QSPI1_SLSO1	O4	Master slave select output		
	—	O5	Reserved		
	—	O6	Reserved		
	CCU61_CC61	O7	T12 PWM channel 61		
	IOM_MON1_9		Monitor input 1		
	IOM_REF1_12		Reference input 1		
	E19	P20.10	I	FAST / PU1 / VEXT / ES	General-purpose input
GTM_TIM3_IN6_6		Mux input channel 6 of TIM module 3			
GTM_TIM2_IN6_6		Mux input channel 6 of TIM module 2			
SDMMC0_DAT2_IN		read data in			
P20.10		O0			General-purpose output
GTM_TOUT66		O1			GTM muxed output
ASCLIN1_ATX		O2			Transmit output
IOM_MON2_13					Monitor input 2
IOM_REF2_13					Reference input 2
QSPI0_SLSO6			Master slave select output		
QSPI2_SLSO7		O4	Master slave select output		
CAN03_TXD		O5	CAN transmit output node 3		
IOM_MON2_8			Monitor input 2		
IOM_REF2_8			Reference input 2		
ASCLIN1_ASCLK			O6	Shift clock output	
CCU61_CC62		O7	T12 PWM channel 62		
IOM_MON1_10			Monitor input 1		
IOM_REF1_11			Reference input 1		
SDMMC0_DAT2			O	write data out	

表 2-51 端口 P20 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
E20	P20.11	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN7_6			Mux input channel 7 of TIM module 3
	GTM_TIM2_IN7_6			Mux input channel 7 of TIM module 2
	QSPI0_SCLKA			Slave SPI clock inputs
	SDMMC0_DAT3_IN			read data in
	P20.11	00		General-purpose output
	GTM_TOUT67	01		GTM muxed output
	—	02		Reserved
	QSPI0_SCLK	03		Master SPI clock output
	—	04		Reserved
	—	05		Reserved
	—	06		Reserved
	CCU61_COUT60	07		T12 PWM channel 60
	IOM_MON1_11			Monitor input 1
	IOM_REF1_10			Reference input 1
SDMMC0_DAT3	0	write data out		
D19	P20.12	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN0_5			Mux input channel 0 of TIM module 3
	GTM_TIM2_IN0_5			Mux input channel 0 of TIM module 2
	QSPI0_MRSTA			Master SPI data input
	SDMMC0_DAT4_IN			read data in
	IOM_PIN_13	GPIO pad input to FPC		
	P20.12	00		General-purpose output
	GTM_TOUT68	01		GTM muxed output
	IOM_MON0_13	02		Monitor input 0
	—			Reserved
	QSPI0_MRST			Slave SPI data output
	IOM_MON2_0	03		Monitor input 2
	IOM_REF2_0			Reference input 2
	QSPI0_MTSR			Master SPI data output
	—	05		Reserved
	—	06		Reserved
	CCU61_COUT61	07		T12 PWM channel 61
	IOM_MON1_12			Monitor input 1
	IOM_REF1_9			Reference input 1
SDMMC0_DAT4	0	write data out		

表 2-51 端口 P20 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
D20	P20.13	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM3_IN1_4			<b>Mux input channel 1 of TIM module 3</b>
	GTM_TIM2_IN1_4			<b>Mux input channel 1 of TIM module 2</b>
	QSPI0_SLSIA			<b>Slave select input</b>
	SDMMC0_DAT5_IN			<b>read data in</b>
	IOM_PIN_14			<b>GPIO pad input to FPC</b>
	P20.13			O0
	GTM_TOUT69	O1		<b>GTM muxed output</b>
	IOM_MON0_14			<b>Monitor input 0</b>
	—	O2		<b>Reserved</b>
	QSPI0_SLSO2	O3		<b>Master slave select output</b>
	QSPI1_SLSO2	O4		<b>Master slave select output</b>
	QSPI0_SCLK	O5		<b>Master SPI clock output</b>
	—	O6		<b>Reserved</b>
	CCU61_COUT62	O7		<b>T12 PWM channel 62</b>
	IOM_MON1_13			<b>Monitor input 1</b>
	IOM_REF1_8			<b>Reference input 1</b>
SDMMC0_DAT5	O	<b>write data out</b>		
C20	P20.14	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM3_IN2_4			<b>Mux input channel 2 of TIM module 3</b>
	GTM_TIM2_IN2_4			<b>Mux input channel 2 of TIM module 2</b>
	QSPI0_MTSRA			<b>Slave SPI data input</b>
	SDMMC0_DAT6_IN			<b>read data in</b>
	IOM_PIN_15			<b>GPIO pad input to FPC</b>
	P20.14			O0
	GTM_TOUT70	O1		<b>GTM muxed output</b>
	IOM_MON0_15			<b>Monitor input 0</b>
	—	O2		<b>Reserved</b>
	QSPI0_MTSR	O3		<b>Master SPI data output</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	SDMMC0_DAT6	O		<b>write data out</b>

表 2-52 端口 P21 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
K17	P21.0	I	LVDS_RX / FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM4_IN0_11			<b>Mux input channel 0 of TIM module 4</b>
	GTM_TIM3_IN4_6			<b>Mux input channel 4 of TIM module 3</b>
	GTM_TIM2_IN4_6			<b>Mux input channel 4 of TIM module 2</b>
	QSPI4_MRSTDN			<b>Master SPI data input (LVDS N line)</b>
	DMU_FDEST			<b>Enter destructive debug mode</b>
	ASCLIN11_ARXC			<b>Receive input</b>
	HSCT1_RXDN			<b>Rx data</b>
	P21.0	O0	<b>General-purpose output</b>	
	GTM_TOUT51	O1	<b>GTM muxed output</b>	
	ASCLIN11_ATX	O2	<b>Transmit output</b>	
	—	O3	<b>Reserved</b>	
	—	O4	<b>Reserved</b>	
	—	O5	<b>Reserved</b>	
	—	O6	<b>Reserved</b>	
	—	O7	<b>Reserved</b>	
HSM_HSM1	O	<b>Pin Output Value</b>		
J17	P21.1	I	LVDS_RX / FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM4_IN1_13			<b>Mux input channel 1 of TIM module 4</b>
	GTM_TIM3_IN5_6			<b>Mux input channel 5 of TIM module 3</b>
	GTM_TIM2_IN5_6			<b>Mux input channel 5 of TIM module 2</b>
	QSPI4_MRSTDP			<b>Master SPI data input (LVDS P line)</b>
	ASCLIN11_ARXD			<b>Receive input</b>
	HSCT1_RXDP			<b>Rx data</b>
	GTM_DTMA4_1			<b>CDTM4_DTM4</b>
	P21.1	O0	<b>General-purpose output</b>	
	GTM_TOUT52	O1	<b>GTM muxed output</b>	
	—	O2	<b>Reserved</b>	
	—	O3	<b>Reserved</b>	
	—	O4	<b>Reserved</b>	
	—	O5	<b>Reserved</b>	
	—	O6	<b>Reserved</b>	
	—	O7	<b>Reserved</b>	
HSM_HSM2	O	<b>Pin Output Value</b>		

表 2-52 端口 P21 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
K19	P21.2	I	LVDS_RX / FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM5_IN4_11			<b>Mux input channel 4 of TIM module 5</b>
	GTM_TIM1_IN0_7			<b>Mux input channel 0 of TIM module 1</b>
	GTM_TIM0_IN0_7			<b>Mux input channel 0 of TIM module 0</b>
	QSPI2_MRSTCN			<b>Master SPI data input (LVDS N line)</b>
	SCU_EMGSTOP_POR T_B			<b>Emergency stop Port Pin B input request</b>
	ASCLIN3_ARXGN			<b>Differential Receive input (low active)</b>
	HSCT0_RXDN			<b>Rx data</b>
	QSPI4_MRSTCN			<b>Master SPI data input (LVDS N line)</b>
	ASCLIN11_ARXE			<b>Receive input</b>
	GTM_DTMA1_0			<b>CDTM1_DTM4</b>
	P21.2	O0		<b>General-purpose output</b>
	GTM_TOUT53	O1		<b>GTM muxed output</b>
	ASCLIN3_ASLSO	O2		<b>Slave select signal output</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	GETH_MDC	O5		<b>MDIO clock</b>
—	O6	<b>Reserved</b>		
—	O7	<b>Reserved</b>		
J19	P21.3	I	LVDS_RX / FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM5_IN5_12			<b>Mux input channel 5 of TIM module 5</b>
	GTM_TIM1_IN1_6			<b>Mux input channel 1 of TIM module 1</b>
	GTM_TIM0_IN1_6			<b>Mux input channel 1 of TIM module 0</b>
	QSPI2_MRSTCP			<b>Master SPI data input (LVDS P line)</b>
	ASCLIN3_ARXGP			<b>Differential Receive input (high active)</b>
	GETH_MDIOD			<b>MDIO Input</b>
	HSCT0_RXDP			<b>Rx data</b>
	QSPI4_MRSTCP			<b>Master SPI data input (LVDS P line)</b>
	P21.3	O0		<b>General-purpose output</b>
	GTM_TOUT54	O1		<b>GTM muxed output</b>
	ASCLIN11_ASCLK	O2		<b>Shift clock output</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
GETH_MDIO	O	<b>MDIO Output</b>		

表 2-52 端口 P21 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
K20	P21.4	I	LVDS_TX / FAST / PU1 / VEXT / ES6	<b>General-purpose input</b>
	GTM_TIM5_IN6_12			<b>Mux input channel 6 of TIM module 5</b>
	GTM_TIM1_IN2_6			<b>Mux input channel 2 of TIM module 1</b>
	GTM_TIM0_IN2_6			<b>Mux input channel 2 of TIM module 0</b>
	P21.4	O0		<b>General-purpose output</b>
	GTM_TOUT55	O1		<b>GTM muxed output</b>
	ASCLIN11_ASLSO	O2		<b>Slave select signal output</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	HSCT0_TXDN	O		<b>Tx data</b>
J20	P21.5	I	LVDS_TX / FAST / PU1 / VEXT / ES6	<b>General-purpose input</b>
	GTM_TIM5_IN7_11			<b>Mux input channel 7 of TIM module 5</b>
	GTM_TIM1_IN3_6			<b>Mux input channel 3 of TIM module 1</b>
	GTM_TIM0_IN3_6			<b>Mux input channel 3 of TIM module 0</b>
	ASCLIN11_ARXF			<b>Receive input</b>
	P21.5	O0		<b>General-purpose output</b>
	GTM_TOUT56	O1		<b>GTM muxed output</b>
	ASCLIN3_ASCLK	O2		<b>Shift clock output</b>
	ASCLIN11_ATX	O3		<b>Transmit output</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
HSCT0_TXDP	O	<b>Tx data</b>		

表 2-52 端口 P21 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
H17	P21.6/TDI	I	FAST / PD / PU2 / VEXT / ES3	<b>General-purpose input</b> PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ.
	GTM_TIM4_IN2_12			<b>Mux input channel 2 of TIM module 4</b>
	GTM_TIM1_IN4_8			<b>Mux input channel 4 of TIM module 1</b>
	GTM_TIM0_IN4_8			<b>Mux input channel 4 of TIM module 0</b>
	GPT120_T5EUDA			<b>Count direction control input of timer T5</b>
	ASCLIN3_ARXF			<b>Receive input</b>
	CBS_TGI2			<b>Trigger input</b>
	TDI			<b>JTAG Module Data Input</b>
	P21.6	O0	<b>General-purpose output</b>	
	GTM_TOUT57	O1	<b>GTM muxed output</b>	
	ASCLIN3_ASLSO	O2	<b>Slave select signal output</b>	
	—	O3	<b>Reserved</b>	
	—	O4	<b>Reserved</b>	
	—	O5	<b>Reserved</b>	
	—	O6	<b>Reserved</b>	
	GPT120_T3OUT	O7	<b>External output for overflow/underflow detection of core timer T3</b>	
	CBS_TGO2	O	<b>Trigger output</b>	
	DAP3	I/O	<b>DAP: DAP3 Data I/O</b>	
	DAPE1	I/O	<b>DAPE: DAPE1 Data I/O</b>	

表 2-52 端口 P21 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
H16	P21.7/TDO	I	FAST / PU2 / VEXT / ES4	<b>General-purpose input</b>
	GTM_TIM4_IN3_12			<b>Mux input channel 3 of TIM module 4</b>
	GTM_TIM1_IN5_7			<b>Mux input channel 5 of TIM module 1</b>
	GTM_TIM0_IN5_7			<b>Mux input channel 5 of TIM module 0</b>
	GPT120_T5INA			<b>Trigger/gate input of timer T5</b>
	CBS_TGI3			<b>Trigger input</b>
	GETH_RXERB			<b>Receive Error MII</b>
	P21.7	O0		<b>General-purpose output</b>
	GTM_TOUT58	O1		<b>GTM muxed output</b>
	ASCLIN3_ATX	O2		<b>Transmit output</b>
	IOM_MON2_15			<b>Monitor input 2</b>
	IOM_REF2_15			<b>Reference input 2</b>
	ASCLIN3_ASCLK	O3		<b>Shift clock output</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	GPT120_T6OUT	O7		<b>External output for overflow/underflow detection of core timer T6</b>
	CBS_TGO3	O		<b>Trigger output</b>
	DAP2	I/O		<b>DAP: DAP2 Data I/O</b>
	DAPE2	I/O		<b>DAPE: DAPE2 Data I/O</b>
TDO	O	<b>JTAG Module Data Output</b>		

表 2-53 端口 P22 功能

Ball	Symbol	Ctrl.	Buffer Type	Function	
P20	P22.0	I	LVDS_TX / FAST / PU1 / VEXT / ES6	<b>General-purpose input</b>	
	GTM_TIM7_IN3_1			<b>Mux input channel 3 of TIM module 7</b>	
	GTM_TIM1_IN1_7			<b>Mux input channel 1 of TIM module 1</b>	
	GTM_TIM0_IN1_7			<b>Mux input channel 1 of TIM module 0</b>	
	QSPI4_MTSRB			<b>Slave SPI data input</b>	
	ASCLIN6_ARXE			<b>Receive input</b>	
	P22.0			O0	<b>General-purpose output</b>
	GTM_TOUT47			O1	<b>GTM muxed output</b>
	ASCLIN3_ATXN			O2	<b>Differential Transmit output (low active)</b>
	QSPI4_MTSR			O3	<b>Master SPI data output</b>
	QSPI4_SCLKN			O4	<b>Master SPI clock output (LVDS N line)</b>
	MSC1_FCLN			O5	<b>Shift-clock inverted part of the differential signal</b>
	—			O6	<b>Reserved</b>
	ASCLIN6_ATX	O7	<b>Transmit output</b>		
P19	P22.1	I	LVDS_TX / FAST / PU1 / VEXT / ES6	<b>General-purpose input</b>	
	GTM_TIM7_IN2_1			<b>Mux input channel 2 of TIM module 7</b>	
	GTM_TIM1_IN0_8			<b>Mux input channel 0 of TIM module 1</b>	
	GTM_TIM0_IN0_8			<b>Mux input channel 0 of TIM module 0</b>	
	QSPI4_MRSTB			<b>Master SPI data input</b>	
	ASCLIN7_ARXE			<b>Receive input</b>	
	P22.1			O0	<b>General-purpose output</b>
	GTM_TOUT48			O1	<b>GTM muxed output</b>
	ASCLIN3_ATXP			O2	<b>Differential Transmit output (high active)</b>
	QSPI4_MRST			O3	<b>Slave SPI data output</b>
	IOM_MON2_4				<b>Monitor input 2</b>
	IOM_REF2_4				<b>Reference input 2</b>
	QSPI4_SCLKP			O4	<b>Master SPI clock output (LVDS P line)</b>
	MSC1_FCLP	O5	<b>Shift-clock direct part of the differential signal</b>		
—	O6	<b>Reserved</b>			
ASCLIN7_ATX	O7	<b>Transmit output</b>			

表 2-53 端口 P22 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
R20	P22.2	I	LVDS_TX / FAST / PU1 / VEXT / ES6	<b>General-purpose input</b>
	GTM_TIM7_IN1_1			<b>Mux input channel 1 of TIM module 7</b>
	GTM_TIM1_IN3_7			<b>Mux input channel 3 of TIM module 1</b>
	GTM_TIM0_IN3_7			<b>Mux input channel 3 of TIM module 0</b>
	QSPI4_SLSIB			<b>Slave select input</b>
	P22.2	O0		<b>General-purpose output</b>
	GTM_TOUT49	O1		<b>GTM muxed output</b>
	ASCLIN5_ATX	O2		<b>Transmit output</b>
	QSPI4_SLSO3	O3		<b>Master slave select output</b>
	QSPI4_MTSRN	O4		<b>Master SPI data output (LVDS N line)</b>
	MSC1_SON	O5		<b>Data output - inverted part of the differential signal</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	HSCT1_TXDN	O		<b>Tx data</b>
R19	P22.3	I	LVDS_TX / FAST / PU1 / VEXT / ES6	<b>General-purpose input</b>
	GTM_TIM7_IN0_1			<b>Mux input channel 0 of TIM module 7</b>
	GTM_TIM1_IN4_4			<b>Mux input channel 4 of TIM module 1</b>
	GTM_TIM0_IN4_4			<b>Mux input channel 4 of TIM module 0</b>
	QSPI4_SCLKB			<b>Slave SPI clock inputs</b>
	ASCLIN5_ARXC			<b>Receive input</b>
	P22.3	O0		<b>General-purpose output</b>
	GTM_TOUT50	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	QSPI4_SCLK	O3		<b>Master SPI clock output</b>
	QSPI4_MTSRP	O4		<b>Master SPI data output (LVDS P line)</b>
	MSC1_SOP	O5		<b>Data output - direct part of the differential signal</b>
	—	O6		<b>Reserved</b>
	HSPDM_MUTE	O7		<b>Mute output from the micro controller which could be used to control an external Transmitter</b>
HSCT1_TXDP	O		<b>Tx data</b>	

表 2-53 端口 P22 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
P16	P22.4	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM3_IN0_8			<b>Mux input channel 0 of TIM module 3</b>
	ASCLIN7_ARXF			<b>Receive input</b>
	GTM_DTMA3_0			<b>CDTM3_DTM4</b>
	P22.4	O0		<b>General-purpose output</b>
	GTM_TOUT130	O1		<b>GTM muxed output</b>
	ASCLIN4_ASLSO	O2		<b>Slave select signal output</b>
	—	O3		<b>Reserved</b>
	QSPI0_SLSO12	O4		<b>Master slave select output</b>
	—	O5		<b>Reserved</b>
	CAN13_TXD	O6		<b>CAN transmit output node 3</b>
	HSPDM_BS0_OUT	O7		<b>Bit stream 0 output to the pad</b>
P17	P22.5	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM3_IN1_7			<b>Mux input channel 1 of TIM module 3</b>
	QSPI0_MTSRC			<b>Slave SPI data input</b>
	CAN13_RXDC			<b>CAN receive input node 3</b>
	P22.5	O0		<b>General-purpose output</b>
	GTM_TOUT131	O1		<b>GTM muxed output</b>
	ASCLIN4_ATX	O2		<b>Transmit output</b>
	—	O3		<b>Reserved</b>
	QSPI0_MTSR	O4		<b>Master SPI data output</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	HSPDM_BS1_OUT	O7		<b>Bit stream 1 output to the pad</b>

表 2-53 端口 P22 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
N16	P22.6	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN2_6			Mux input channel 2 of TIM module 3
	GTM_TIM2_IN6_14			Mux input channel 6 of TIM module 2
	QSPI0_MRSTC			Master SPI data input
	ASCLIN4_ARXC			Receive input
	P22.6	O0		General-purpose output
	GTM_TOUT132	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	QSPI0_MRST	O4		Slave SPI data output
	IOM_MON2_0			Monitor input 2
	IOM_REF2_0			Reference input 2
	CAN21_TXD	O5		CAN transmit output node 1
	—	O6		Reserved
—	O7	Reserved		
N17	P22.7	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN3_7			Mux input channel 3 of TIM module 3
	QSPI0_SCLKC			Slave SPI clock inputs
	CAN21_RXDF			CAN receive input node 1
	P22.7	O0		General-purpose output
	GTM_TOUT133	O1		GTM muxed output
	ASCLIN4_ASCLK	O2		Shift clock output
	—	O3		Reserved
	QSPI0_SCLK	O4		Master SPI clock output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-53 端口 P22 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
M16	P22.8	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN0_4			Mux input channel 0 of TIM module 5
	GTM_TIM3_IN4_7			Mux input channel 4 of TIM module 3
	QSPI0_SCLKB			Slave SPI clock inputs
	P22.8	O0		General-purpose output
	GTM_TOUT134	O1		GTM muxed output
	ASCLIN5_ASCLK	O2		Shift clock output
	—	O3		Reserved
	QSPI0_SCLK	O4		Master SPI clock output
	CAN22_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	—	O7		Reserved
M17	P22.9	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN1_10			Mux input channel 1 of TIM module 5
	GTM_TIM3_IN5_7			Mux input channel 5 of TIM module 3
	QSPI0_MRSTB			Master SPI data input
	ASCLIN4_ARXD			Receive input
	CAN22_RXDE			CAN receive input node 2
	GTM_DTMA3_1			CDTM3_DTM4
	P22.9	O0		General-purpose output
	GTM_TOUT135	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	QSPI0_MRST	O4		Slave SPI data output
	IOM_MON2_0			Monitor input 2
	IOM_REF2_0			Reference input 2
	—	O5		Reserved
	—	O6		Reserved
—	O7	Reserved		

表 2-53 端口 P22 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
L16	P22.10	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN2_8			Mux input channel 2 of TIM module 5
	GTM_TIM3_IN6_7			Mux input channel 6 of TIM module 3
	QSPI0_MTSRB			Slave SPI data input
	P22.10	O0		General-purpose output
	GTM_TOUT136	O1		GTM muxed output
	ASCLIN4_ATX	O2		Transmit output
	—	O3		Reserved
	QSPI0_MTSR	O4		Master SPI data output
	CAN23_TXD	O5		CAN transmit output node 3
	—	O6		Reserved
	—	O7		Reserved
L17	P22.11	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN3_10			Mux input channel 3 of TIM module 5
	GTM_TIM3_IN7_7			Mux input channel 7 of TIM module 3
	CAN23_RXDE			CAN receive input node 3
	P22.11	O0		General-purpose output
	GTM_TOUT137	O1		GTM muxed output
	ASCLIN4_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	QSPI0_SLSO10	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-54 端口 P23 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
V20	P23.0	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM6_IN7_1			<b>Mux input channel 7 of TIM module 6</b>
	GTM_TIM1_IN5_4			<b>Mux input channel 5 of TIM module 1</b>
	GTM_TIM0_IN5_4			<b>Mux input channel 5 of TIM module 0</b>
	CAN10_RXDC			<b>CAN receive input node 0</b>
	P23.0	O0		<b>General-purpose output</b>
	GTM_TOUT41	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
U19	P23.1	I	FAST / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM6_IN6_1			<b>Mux input channel 6 of TIM module 6</b>
	GTM_TIM1_IN6_4			<b>Mux input channel 6 of TIM module 1</b>
	GTM_TIM0_IN6_4			<b>Mux input channel 6 of TIM module 0</b>
	MSC1_SDIO			<b>Upstream asynchronous input signal</b>
	ASCLIN6_ARXF			<b>Receive input</b>
	P23.1	O0		<b>General-purpose output</b>
	GTM_TOUT42	O1		<b>GTM muxed output</b>
	ASCLIN1_ARTS	O2		<b>Ready to send output</b>
	QSPI4_SLSO6	O3		<b>Master slave select output</b>
	GTM_CLK0	O4		<b>CGM generated clock</b>
	CAN10_TXD	O5		<b>CAN transmit output node 0</b>
	CCU_EXTCLK0	O6		<b>External Clock 0</b>
	ASCLIN6_ASCLK	O7		<b>Shift clock output</b>

表 2-54 端口 P23 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
U20	P23.2	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM6_IN5_1			Mux input channel 5 of TIM module 6
	GTM_TIM1_IN6_5			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_5			Mux input channel 6 of TIM module 0
	ASCLIN7_ARXC			Receive input
	P23.2	O0		General-purpose output
	GTM_TOUT43	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	CAN23_TXD	O4		CAN transmit output node 3
	CAN12_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	—	O7		Reserved
T19	P23.3	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM6_IN4_2			Mux input channel 4 of TIM module 6
	GTM_TIM1_IN7_4			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_4			Mux input channel 7 of TIM module 0
	MSC1_INJ0			Injection signal from port
	ASCLIN6_ARXA			Receive input
	CAN12_RXDC			CAN receive input node 2
	CAN23_RXDB			CAN receive input node 3
	P23.3	O0		General-purpose output
	GTM_TOUT44	O1		GTM muxed output
	ASCLIN7_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
—	O7	Reserved		

表 2-54 端口 P23 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
T20	P23.4	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM6_IN3_2			Mux input channel 3 of TIM module 6
	GTM_TIM1_IN7_5			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_5			Mux input channel 7 of TIM module 0
	P23.4	O0		General-purpose output
	GTM_TOUT45	O1		GTM muxed output
	ASCLIN6_ASLSO	O2		Slave select signal output
	QSPI4_SLSO5	O3		Master slave select output
	—	O4		Reserved
	MSC1_EN0	O5		Chip Select
	—	O6		Reserved
	—	O7		Reserved
T17	P23.5	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM6_IN2_2			Mux input channel 2 of TIM module 6
	GTM_TIM1_IN2_7			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_7			Mux input channel 2 of TIM module 0
	P23.5	O0		General-purpose output
	GTM_TOUT46	O1		GTM muxed output
	ASCLIN6_ATX	O2		Transmit output
	QSPI4_SLSO4	O3		Master slave select output
	—	O4		Reserved
	MSC1_EN1	O5		Chip Select
	CAN22_TXD	O6		CAN transmit output node 2
	—	O7		Reserved
R17	P23.6	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM6_IN1_2			Mux input channel 1 of TIM module 6
	GTM_TIM4_IN2_7			Mux input channel 2 of TIM module 4
	GTM_TIM1_IN2_10			Mux input channel 2 of TIM module 1
	CAN22_RXDC			CAN receive input node 2
	P23.6	O0		General-purpose output
	GTM_TOUT138	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	QSPI0_SLSO11	O4		Master slave select output
	CAN11_TXD	O5		CAN transmit output node 1
	—	O6		Reserved
—	O7	Reserved		

表 2-54 端口 P23 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
R16	P23.7	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM6_IN0_2			<b>Mux input channel 0 of TIM module 6</b>
	GTM_TIM4_IN3_7			<b>Mux input channel 3 of TIM module 4</b>
	GTM_TIM1_IN3_10			<b>Mux input channel 3 of TIM module 1</b>
	CAN11_RXDC			<b>CAN receive input node 1</b>
	P23.7	O0		<b>General-purpose output</b>
	GTM_TOUT139	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>

表 2-55 端口 P32 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
Y17	P32.0	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b> P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
	GTM_TIM3_IN2_5			<b>Mux input channel 2 of TIM module 3</b>
	GTM_TIM2_IN2_5			<b>Mux input channel 2 of TIM module 2</b>
	P32.0	O0		<b>General-purpose output</b>
	GTM_TOUT36	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>

表 2-55 端口 P32 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
W17	P32.1	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b> P32.1 / External Pass Device gate control for EVRC
	GTM_TIM3_IN3_15			<b>Mux input channel 3 of TIM module 3</b>
	P32.1	O0		<b>General-purpose output</b>
	GTM_TOUT37	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
—	O7	<b>Reserved</b>		
Y18	P32.2	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM1_IN3_8			<b>Mux input channel 3 of TIM module 1</b>
	GTM_TIM0_IN3_8			<b>Mux input channel 3 of TIM module 0</b>
	CAN03_RXDB			<b>CAN receive input node 3</b>
	ASCLIN3_ARXD			<b>Receive input</b>
	CAN21_RXDD			<b>CAN receive input node 1</b>
	P32.2	O0		<b>General-purpose output</b>
	GTM_TOUT38	O1		<b>GTM muxed output</b>
	ASCLIN3_ATX	O2		<b>Transmit output</b>
	IOM_MON2_15			<b>Monitor input 2</b>
	IOM_REF2_15			<b>Reference input 2</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	PMS_DCDCSYNCO	O6		<b>DC-DC synchronization output</b>
—	O7	<b>Reserved</b>		

表 2-55 端口 P32 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y19	P32.3	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN4_5			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_5			Mux input channel 4 of TIM module 0
	P32.3	O0		General-purpose output
	GTM_TOUT39	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	—	O3		Reserved
	ASCLIN3_ASCLK	O4		Shift clock output
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	CAN21_TXD	O6		CAN transmit output node 1
	—	O7		Reserved
W18	P32.4	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN5_5			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_5			Mux input channel 5 of TIM module 0
	ASCLIN1_ACTSB			Clear to send input
	MSC1_SDI2			Upstream asynchronous input signal
	P32.4	O0		General-purpose output
	GTM_TOUT40	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	GTM_CLK1	O4		CGM generated clock
	MSC1_EN0	O5		Chip Select
	CCU_EXTCLK1	O6		External Clock 1
	CCU60_COUT63			T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0	O7		Reference input 1
PMS_DCDCSYNCO	DC-DC synchronization output			

表 2-55 端口 P32 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function	
T15	P32.5	I	SLOW / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM5_IN5_9			Mux input channel 5 of TIM module 5	
	GTM_TIM4_IN1_14			Mux input channel 1 of TIM module 4	
	GTM_TIM3_IN5_8			Mux input channel 5 of TIM module 3	
	SENT_SENT10C			Receive input channel 10	
	P32.5	O0		General-purpose output	
	GTM_TOUT140	O1		GTM muxed output	
	ASCLIN2_ATX	O2		Transmit output	
	IOM_MON2_14			Monitor input 2	
	IOM_REF2_14			Reference input 2	
	—	O3		Reserved	
	—	O4		Reserved	
	—	O5		Reserved	
	CAN02_TXD	O6		CAN transmit output node 2	
	IOM_MON2_7			Monitor input 2	
	IOM_REF2_7			Reference input 2	
	—	O7		Reserved	
U15	P32.6	I	SLOW / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM5_IN6_9			Mux input channel 6 of TIM module 5	
	GTM_TIM4_IN4_15			Mux input channel 4 of TIM module 4	
	GTM_TIM3_IN6_8			Mux input channel 6 of TIM module 3	
	CAN02_RXDC			CAN receive input node 2	
	CBS_TGI4			Trigger input	
	ASCLIN2_ARXF			Receive input	
	ASCLIN6_ARXC			Receive input	
	SENT_SENT11C			Receive input channel 11	
	P32.6			O0	General-purpose output
	GTM_TOUT141			O1	GTM muxed output
	—			O2	Reserved
	—			O3	Reserved
	QSPI2_SLSO12			O4	Master slave select output
	CAN22_TXD			O5	CAN transmit output node 2
	—			O6	Reserved
	—			O7	Reserved
CBS_TGO4	O	Trigger output			

表 2-55 端口 P32 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
U16	P32.7	I	SLOW / PU1 / VEXT / ES	<b>General-purpose input</b>
	GTM_TIM5_IN7_8			<b>Mux input channel 7 of TIM module 5</b>
	GTM_TIM4_IN0_15			<b>Mux input channel 0 of TIM module 4</b>
	GTM_TIM3_IN7_8			<b>Mux input channel 7 of TIM module 3</b>
	CBS_TGI5			<b>Trigger input</b>
	CAN22_RXDB			<b>CAN receive input node 2</b>
	SENT_SENT12C			<b>Receive input channel 12</b>
	P32.7	O0		<b>General-purpose output</b>
	GTM_TOUT142	O1		<b>GTM muxed output</b>
	ASCLIN6_ATX	O2		<b>Transmit output</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	—	O7		<b>Reserved</b>
	CBS_TGO5	O		<b>Trigger output</b>

表 2-56 端口 P33 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
W10	P33.0	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM3_IN0_13			<b>Mux input channel 0 of TIM module 3</b>
	GTM_TIM1_IN4_6			<b>Mux input channel 4 of TIM module 1</b>
	GTM_TIM0_IN4_6			<b>Mux input channel 4 of TIM module 0</b>
	EDSADC_ITR0E			<b>Trigger/Gate input, channel 0</b>
	SENT_SENT13C			<b>Receive input channel 13</b>
	IOM_PIN_0			<b>GPIO pad input to FPC</b>
	GTM_DTMT1_2			<b>CDTM1_DTM0</b>
	EVADC_G10CH7	AI		<b>Analog input channel 7, group 10</b>
	EVADC_FC7CH0			<b>Analog input FC channel 7</b>
	P33.0	O0	<b>General-purpose output</b>	
	GTM_TOUT22	O1	<b>GTM muxed output</b>	
	IOM_MON0_0		<b>Monitor input 0</b>	
	IOM_GTM_0		<b>GTM-provided inputs to EXOR combiner</b>	
	ASCLIN5_ATX	O2	<b>Transmit output</b>	
	—	O3	<b>Reserved</b>	
	—	O4	<b>Reserved</b>	
	—	O5	<b>Reserved</b>	
	EVADC_FC2BFLOUT	O6	<b>Boundary flag output, FC channel 2</b>	
	—	O7	<b>Reserved</b>	

表 2-56 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y10	P33.1	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM3_IN1_15			<b>Mux input channel 1 of TIM module 3</b>
	GTM_TIM1_IN5_6			<b>Mux input channel 5 of TIM module 1</b>
	GTM_TIM0_IN5_6			<b>Mux input channel 5 of TIM module 0</b>
	EDSADC_ITR1E			<b>Trigger/Gate input, channel 1</b>
	PSI5_RX0C			<b>RXD inputs (receive data) channel 0</b>
	EDSADC_DSCIN2B			<b>Modulator clock input, channel 2</b>
	SENT_SENT9C			<b>Receive input channel 9</b>
	ASCLIN8_ARXC			<b>Receive input</b>
	IOM_PIN_1			<b>GPIO pad input to FPC</b>
	EVADC_G10CH6	AI		<b>Analog input channel 6, group 10</b>
	EVADC_FC6CH0		<b>Analog input FC channel 6</b>	
	P33.1	O0	<b>General-purpose output</b>	
	GTM_TOUT23	O1	<b>GTM muxed output</b>	
	IOM_MON0_1		<b>Monitor input 0</b>	
	IOM_GTM_1		<b>GTM-provided inputs to EXOR combiner</b>	
	ASCLIN3_ASLSO	O2	<b>Slave select signal output</b>	
	QSPI2_SCLK	O3	<b>Master SPI clock output</b>	
	EDSADC_DSCOUT2	O4	<b>Modulator clock output</b>	
	EVADC_EMUX02	O5	<b>Control of external analog multiplexer interface 0</b>	
	EVADC_FC4BFLOUT	O6	<b>Boundary flag output, FC channel 4</b>	
	—	O7	<b>Reserved</b>	

表 2-56 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
W11	P33.2	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM3_IN2_14			<b>Mux input channel 2 of TIM module 3</b>
	GTM_TIM1_IN6_6			<b>Mux input channel 6 of TIM module 1</b>
	GTM_TIM0_IN6_6			<b>Mux input channel 6 of TIM module 0</b>
	EDSADC_ITR2E			<b>Trigger/Gate input, channel 2</b>
	SENT_SENT8C			<b>Receive input channel 8</b>
	EDSADC_DSDIN2B			<b>Digital datastream input, channel 2</b>
	IOM_PIN_2			<b>GPIO pad input to FPC</b>
	EVADC_G10CH5			AI
	EVADC_FC5CH0	<b>Analog input FC channel 5</b>		
	P33.2	O0	<b>General-purpose output</b>	
	GTM_TOUT24	O1	<b>GTM muxed output</b>	
	IOM_MON0_2		<b>Monitor input 0</b>	
	IOM_GTM_2		<b>GTM-provided inputs to EXOR combiner</b>	
	ASCLIN3_ASCLK	O2	<b>Shift clock output</b>	
	QSPI2_SLSO10	O3	<b>Master slave select output</b>	
	PSI5_TX0	O4	<b>TXD outputs (send data)</b>	
	IOM_MON1_14		<b>Monitor input 1</b>	
	IOM_REF1_14		<b>Reference input 1</b>	
	EVADC_EMUX01	O5	<b>Control of external analog multiplexer interface 0</b>	
	EVADC_FC3BFLOUT	O6	<b>Boundary flag output, FC channel 3</b>	
	—	O7	<b>Reserved</b>	

表 2-56 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y11	P33.3	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM3_IN3_12			<b>Mux input channel 3 of TIM module 3</b>
	GTM_TIM1_IN7_6			<b>Mux input channel 7 of TIM module 1</b>
	GTM_TIM0_IN7_6			<b>Mux input channel 7 of TIM module 0</b>
	PSI5_RX1C			<b>RXD inputs (receive data) channel 1</b>
	SENT_SENT7C			<b>Receive input channel 7</b>
	EDSADC_DSCIN1B			<b>Modulator clock input, channel 1</b>
	IOM_PIN_3			<b>GPIO pad input to FPC</b>
	EVADC_G10CH4	AI	<b>Analog input channel 4, group 10</b>	
	EVADC_FC4CH0		<b>Analog input FC channel 4</b>	
	P33.3	O0	<b>General-purpose output</b>	
	GTM_TOUT25	O1	<b>GTM muxed output</b>	
	IOM_MON0_3		<b>Monitor input 0</b>	
	IOM_GTM_3		<b>GTM-provided inputs to EXOR combiner</b>	
	ASCLIN5_ASCLK	O2	<b>Shift clock output</b>	
	QSPI4_SLSO2	O3	<b>Master slave select output</b>	
	EDSADC_DSCOUT1	O4	<b>Modulator clock output</b>	
	EVADC_EMUX00	O5	<b>Control of external analog multiplexer interface 0</b>	
	EVADC_FC5BFLOUT	O6	<b>Boundary flag output, FC channel 5</b>	
	—	O7	<b>Reserved</b>	

表 2-56 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
W12	P33.4	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM4_IN4_10			<b>Mux input channel 4 of TIM module 4</b>
	GTM_TIM1_IN0_10			<b>Mux input channel 0 of TIM module 1</b>
	GTM_TIM0_IN0_10			<b>Mux input channel 0 of TIM module 0</b>
	EDSADC_ITR0F			<b>Trigger/Gate input, channel 0</b>
	SENT_SENT6C			<b>Receive input channel 6</b>
	EDSADC_DSDIN1B			<b>Digital datastream input, channel 1</b>
	CCU61_CTRAPC			<b>Trap input capture</b>
	ASCLIN5_ARXB			<b>Receive input</b>
	IOM_PIN_4			<b>GPIO pad input to FPC</b>
	GTM_DTMT2_0			<b>CDTM2_DTM0</b>
	EVADC_G10CH3			AI
	P33.4	O0	<b>General-purpose output</b>	
	GTM_TOUT26	O1	<b>GTM muxed output</b>	
	IOM_MON0_4		<b>Monitor input 0</b>	
	IOM_GTM_4		<b>GTM-provided inputs to EXOR combiner</b>	
	ASCLIN2_ARTS	O2	<b>Ready to send output</b>	
	QSPI2_SLSO12	O3	<b>Master slave select output</b>	
	PSI5_TX1	O4	<b>TXD outputs (send data)</b>	
	IOM_MON1_15		<b>Monitor input 1</b>	
	EVADC_EMUX12		<b>Control of external analog multiplexer interface 1</b>	
	EVADC_FC0BFLOUT	O6	<b>Boundary flag output, FC channel 0</b>	
	CAN13_TXD	O7	<b>CAN transmit output node 3</b>	

表 2-56 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y12	P33.5	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM4_IN5_10			<b>Mux input channel 5 of TIM module 4</b>
	GTM_TIM1_IN1_8			<b>Mux input channel 1 of TIM module 1</b>
	GTM_TIM0_IN1_8			<b>Mux input channel 1 of TIM module 0</b>
	EDSADC_DSCIN0B			<b>Modulator clock input, channel 0</b>
	EDSADC_ITR1F			<b>Trigger/Gate input, channel 1</b>
	GPT120_T4EUDB			<b>Count direction control input of timer T4</b>
	PSI5S_RXC			<b>RX data input</b>
	ASCLIN2_ACTSB			<b>Clear to send input</b>
	CCU61_CCPOS2C			<b>Hall capture input 2</b>
	PSI5_RX2C			<b>RXD inputs (receive data) channel 2</b>
	SENT_SENT5C			<b>Receive input channel 5</b>
	CAN13_RXDB			<b>CAN receive input node 3</b>
	IOM_PIN_5			<b>GPIO pad input to FPC</b>
	EVADC_G10CH2	AI	<b>Analog input channel 2, group 10</b>	
	P33.5	O0	<b>General-purpose output</b>	
	GTM_TOUT27	O1	<b>GTM muxed output</b>	
	IOM_MON0_5	O1	<b>Monitor input 0</b>	
	IOM_GTM_5		<b>GTM-provided inputs to EXOR combiner</b>	
	QSPI0_SLSO7	O2	<b>Master slave select output</b>	
	QSPI1_SLSO7	O3	<b>Master slave select output</b>	
	EDSADC_DSCOUT0	O4	<b>Modulator clock output</b>	
	EVADC_EMUX11	O5	<b>Control of external analog multiplexer interface 1</b>	
	EVADC_FC2BFLOUT	O6	<b>Boundary flag output, FC channel 2</b>	
	ASCLIN5_ASLSO	O7	<b>Slave select signal output</b>	

表 2-56 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
W13	P33.6	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM1_IN2_9			<b>Mux input channel 2 of TIM module 1</b>
	GTM_TIM0_IN2_9			<b>Mux input channel 2 of TIM module 0</b>
	EDSADC_ITR2F			<b>Trigger/Gate input, channel 2</b>
	GPT120_T2EUDB			<b>Count direction control input of timer T2</b>
	SENT_SENT4C			<b>Receive input channel 4</b>
	CCU61_CCPOS1C			<b>Hall capture input 1</b>
	EDSADC_DSDIN0B			<b>Digital datastream input, channel 0</b>
	ASCLIN8_ARXD			<b>Receive input</b>
	IOM_PIN_6			<b>GPIO pad input to FPC</b>
	GTM_DTMT2_1			<b>CDTM2_DTM0</b>
	EVADC_G10CH1			AI
	P33.6	O0	<b>General-purpose output</b>	
	GTM_TOUT28	O1	<b>GTM muxed output</b>	
	IOM_MON0_6		<b>Monitor input 0</b>	
	IOM_GTM_6		<b>GTM-provided inputs to EXOR combiner</b>	
	ASCLIN2_ASLSO	O2	<b>Slave select signal output</b>	
	QSPI2_SLSO11	O3	<b>Master slave select output</b>	
	PSI5_TX2	O4	<b>TXD outputs (send data)</b>	
	IOM_REF1_15		<b>Reference input 1</b>	
	EVADC_EMUX10	O5	<b>Control of external analog multiplexer interface 1</b>	
	EVADC_FC1BFLOUT	O6	<b>Boundary flag output, FC channel 1</b>	
	PSI5_TX	O7	<b>TX data output</b>	

表 2-56 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y13	P33.7	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM1_IN3_9			<b>Mux input channel 3 of TIM module 1</b>
	GTM_TIM0_IN3_9			<b>Mux input channel 3 of TIM module 0</b>
	CAN00_RXDE			<b>CAN receive input node 0</b>
	GPT120_T2INB			<b>Trigger/gate input of timer T2</b>
	CCU61_CCPOS0C			<b>Hall capture input 0</b>
	SCU_E_REQ4_0			<b>ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)</b>
	SENT_SENT14C			<b>Receive input channel 14</b>
	IOM_PIN_7			<b>GPIO pad input to FPC</b>
	EVADC_G10CH0			AI
	P33.7	O0	<b>General-purpose output</b>	
	GTM_TOUT29	O1	<b>GTM muxed output</b>	
	IOM_MON0_7		<b>Monitor input 0</b>	
	IOM_GTM_7		<b>GTM-provided inputs to EXOR combiner</b>	
	ASCLIN2_ASCLK	O2	<b>Shift clock output</b>	
	QSPI4_SLSO7	O3	<b>Master slave select output</b>	
	ASCLIN8_ATX	O4	<b>Transmit output</b>	
	—	O5	<b>Reserved</b>	
	EVADC_FC3BFLOUT	O6	<b>Boundary flag output, FC channel 3</b>	
	—	O7	<b>Reserved</b>	

表 2-56 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
W14	P33.8	I	FAST / HighZ / VEVR SB	<b>General-purpose input</b>
	GTM_TIM1_IN4_7			<b>Mux input channel 4 of TIM module 1</b>
	GTM_TIM0_IN4_7			<b>Mux input channel 4 of TIM module 0</b>
	ASCLIN2_ARXE			<b>Receive input</b>
	SCU_EMGSTOP_POR T_A			<b>Emergency stop Port Pin A input request</b>
	IOM_PIN_8			<b>GPIO pad input to FPC</b>
	P33.8	O0		<b>General-purpose output</b>
	GTM_TOUT30	O1		<b>GTM muxed output</b>
	IOM_MON0_8			<b>Monitor input 0</b>
	ASCLIN2_ATX	O2		<b>Transmit output</b>
	IOM_MON2_14			<b>Monitor input 2</b>
	IOM_REF2_14			<b>Reference input 2</b>
	QSPI4_SLSO2	O3		<b>Master slave select output</b>
	—	O4		<b>Reserved</b>
	CAN00_TXD	O5		<b>CAN transmit output node 0</b>
	IOM_MON2_5			<b>Monitor input 2</b>
	IOM_REF2_5			<b>Reference input 2</b>
	—	O6		<b>Reserved</b>
	CCU61_COUT62	O7		<b>T12 PWM channel 62</b>
	IOM_MON1_13			<b>Monitor input 1</b>
IOM_REF1_8	<b>Reference input 1</b>			
SMU_FSP0	O	<b>FSP[1..0] Output Signals - Generated by SMU_core</b>		

表 2-56 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y14	P33.9	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM1_IN1_9			<b>Mux input channel 1 of TIM module 1</b>
	GTM_TIM0_IN1_9			<b>Mux input channel 1 of TIM module 0</b>
	QSPI3_HSICINA			<b>Highspeed capture channel</b>
	IOM_PIN_9			<b>GPIO pad input to FPC</b>
	P33.9	O0		<b>General-purpose output</b>
	GTM_TOUT31	O1		<b>GTM muxed output</b>
	IOM_MON0_9			<b>Monitor input 0</b>
	ASCLIN2_ATX	O2		<b>Transmit output</b>
	IOM_MON2_14			<b>Monitor input 2</b>
	IOM_REF2_14			<b>Reference input 2</b>
	QSPI4_SLSO1	O3		<b>Master slave select output</b>
	ASCLIN2_ASCLK	O4		<b>Shift clock output</b>
	CAN01_TXD	O5		<b>CAN transmit output node 1</b>
	IOM_MON2_6			<b>Monitor input 2</b>
	IOM_REF2_6			<b>Reference input 2</b>
	ASCLIN0_ATX	O6		<b>Transmit output</b>
	IOM_MON2_12			<b>Monitor input 2</b>
	IOM_REF2_12			<b>Reference input 2</b>
	CCU61_CC62	O7		<b>T12 PWM channel 62</b>
	IOM_MON1_10			<b>Monitor input 1</b>
	IOM_REF1_11			<b>Reference input 1</b>

表 2-56 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
W15	P33.10	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM4_IN4_14			Mux input channel 4 of TIM module 4
	GTM_TIM1_IN0_9			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_9			Mux input channel 0 of TIM module 0
	QSPI4_SLSIA			Slave select input
	QSPI3_HSICINB			Highspeed capture channel
	CAN01_RXDD			CAN receive input node 1
	ASCLIN0_ARXD			Receive input
	IOM_PIN_10			GPIO pad input to FPC
	P33.10			00
	GTM_TOUT32	01	GTM muxed output	
	IOM_MON0_10		Monitor input 0	
	QSPI1_SLSO6	02	Master slave select output	
	QSPI4_SLSO0	03	Master slave select output	
	ASCLIN1_ASLSO	04	Slave select signal output	
	PSI5S_CLK	05	PSI5S CLK is a clock that can be used on a pin to drive the external PHY.	
	—	06	Reserved	
	CCU61_COUT61	07	T12 PWM channel 61	
	IOM_MON1_12		Monitor input 1	
	IOM_REF1_9		Reference input 1	
SMU_FSP1	0	FSP[1..0] Output Signals - Generated by SMU_core		
Y15	P33.11	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN2_8			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_8			Mux input channel 2 of TIM module 0
	QSPI4_SCLKA			Slave SPI clock inputs
	IOM_PIN_11			GPIO pad input to FPC
	P33.11	00	General-purpose output	
	GTM_TOUT33	01	GTM muxed output	
	IOM_MON0_11		Monitor input 0	
	ASCLIN1_ASCLK	02	Shift clock output	
	QSPI4_SCLK	03	Master SPI clock output	
	—	04	Reserved	
	—	05	Reserved	
	EDSADC_CGPWMN	06	Negative carrier generator output	
	CCU61_CC61	07	T12 PWM channel 61	
	IOM_MON1_9		Monitor input 1	
	IOM_REF1_12		Reference input 1	

表 2-56 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
W16	P33.12	I	FAST / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM3_IN0_6			<b>Mux input channel 0 of TIM module 3</b>
	GTM_TIM2_IN0_6			<b>Mux input channel 0 of TIM module 2</b>
	QSPI4_MTSRA			<b>Slave SPI data input</b>
	CAN00_RXDD			<b>CAN receive input node 0</b>
	PMS_PINBWKP			<b>PINB (P33.12) pin input</b>
	IOM_PIN_12			<b>GPIO pad input to FPC</b>
	P33.12			O0
	GTM_TOUT34	O1		<b>GTM muxed output</b>
	IOM_MON0_12			<b>Monitor input 0</b>
	ASCLIN1_ATX	O2		<b>Transmit output</b>
	IOM_MON2_13			<b>Monitor input 2</b>
	IOM_REF2_13			<b>Reference input 2</b>
	QSPI4_MTSR	O3		<b>Master SPI data output</b>
	ASCLIN1_ASCLK	O4		<b>Shift clock output</b>
	CAN22_TXD	O5		<b>CAN transmit output node 2</b>
	EDSADC_CGPWMP	O6		<b>Positive carrier generator output</b>
	CCU61_COUT60	O7		<b>T12 PWM channel 60</b>
	IOM_MON1_11			<b>Monitor input 1</b>
	IOM_REF1_10			<b>Reference input 1</b>

表 2-56 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y16	P33.13	I	FAST / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM3_IN1_5			<b>Mux input channel 1 of TIM module 3</b>
	GTM_TIM2_IN1_5			<b>Mux input channel 1 of TIM module 2</b>
	ASCLIN1_ARXF			<b>Receive input</b>
	EDSADC_SGNB			<b>Carrier sign signal input</b>
	QSPI4_MRSTA			<b>Master SPI data input</b>
	MSC1_INJ1			<b>Injection signal from port</b>
	CAN22_RXDA			<b>CAN receive input node 2</b>
	P33.13			O0
	GTM_TOUT35	O1	<b>GTM muxed output</b>	
	ASCLIN1_ATX	O2	<b>Transmit output</b>	
	IOM_MON2_13		<b>Monitor input 2</b>	
	IOM_REF2_13		<b>Reference input 2</b>	
	QSPI4_MRST	O3	<b>Slave SPI data output</b>	
	IOM_MON2_4		<b>Monitor input 2</b>	
	IOM_REF2_4		<b>Reference input 2</b>	
	QSPI2_SLSO6	O4	<b>Master slave select output</b>	
	CAN00_TXD	O5	<b>CAN transmit output node 0</b>	
	IOM_MON2_5		<b>Monitor input 2</b>	
	IOM_REF2_5		<b>Reference input 2</b>	
	—	O6	<b>Reserved</b>	
	CCU61_CC60	O7	<b>T12 PWM channel 60</b>	
	IOM_MON1_8		<b>Monitor input 1</b>	
	IOM_REF1_13		<b>Reference input 1</b>	

表 2-56 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
T14	P33.14	I	FAST / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM5_IN0_8			<b>Mux input channel 0 of TIM module 5</b>
	GTM_TIM4_IN5_14			<b>Mux input channel 5 of TIM module 4</b>
	GTM_TIM2_IN0_8			<b>Mux input channel 0 of TIM module 2</b>
	QSPI2_SCLKD			<b>Slave SPI clock inputs</b>
	CBS_TGI6			<b>Trigger input</b>
	P33.14	O0		<b>General-purpose output</b>
	GTM_TOUT143	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	QSPI2_SCLK	O3		<b>Master SPI clock output</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	CCU60_CC62	O7		<b>T12 PWM channel 62</b>
	IOM_MON1_0			<b>Monitor input 1</b>
	IOM_REF1_4			<b>Reference input 1</b>
CBS_TGO6	O	<b>Trigger output</b>		
U14	P33.15	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM5_IN1_9			<b>Mux input channel 1 of TIM module 5</b>
	GTM_TIM4_IN6_12			<b>Mux input channel 6 of TIM module 4</b>
	GTM_TIM2_IN1_7			<b>Mux input channel 1 of TIM module 2</b>
	CBS_TGI7			<b>Trigger input</b>
	P33.15	O0		<b>General-purpose output</b>
	GTM_TOUT144	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	QSPI2_SLSO11	O3		<b>Master slave select output</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	CCU60_COUT62	O7		<b>T12 PWM channel 62</b>
	IOM_MON1_5			<b>Monitor input 1</b>
	IOM_REF1_1			<b>Reference input 1</b>
	CBS_TGO7	O		<b>Trigger output</b>

表 2-57 端口 P34 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
U11	P34.1	I	SLOW / PU1 / VEVRSB / ES5	<b>General-purpose input</b>
	GTM_TIM5_IN3_9			<b>Mux input channel 3 of TIM module 5</b>
	GTM_TIM3_IN4_12			<b>Mux input channel 4 of TIM module 3</b>
	GTM_TIM2_IN3_9			<b>Mux input channel 3 of TIM module 2</b>
	EVADC_G10CH11	AI		<b>Analog input channel 11, group 10</b>
	P34.1	O0		<b>General-purpose output</b>
	GTM_TOUT146	O1		<b>GTM muxed output</b>
	ASCLIN4_ATX	O2		<b>Transmit output</b>
	—	O3		<b>Reserved</b>
	CAN00_TXD	O4		<b>CAN transmit output node 0</b>
	IOM_MON2_5			<b>Monitor input 2</b>
	IOM_REF2_5			<b>Reference input 2</b>
	CAN20_TXD	O5		<b>CAN transmit output node 0</b>
	—	O6		<b>Reserved</b>
	CCU60_COUT63	O7		<b>T13 PWM channel 63</b>
	IOM_MON1_6			<b>Monitor input 1</b>
IOM_REF1_0		<b>Reference input 1</b>		
T12	P34.2	I	SLOW / PU1 / VEVRSB / ES	<b>General-purpose input</b>
	GTM_TIM5_IN4_9			<b>Mux input channel 4 of TIM module 5</b>
	GTM_TIM3_IN5_13			<b>Mux input channel 5 of TIM module 3</b>
	GTM_TIM2_IN4_8			<b>Mux input channel 4 of TIM module 2</b>
	ASCLIN4_ARXB			<b>Receive input</b>
	CAN00_RXDG			<b>CAN receive input node 0</b>
	CAN20_RXDC			<b>CAN receive input node 0</b>
	EVADC_G10CH10	AI		<b>Analog input channel 10, group 10</b>
	P34.2	O0		<b>General-purpose output</b>
	GTM_TOUT147	O1		<b>GTM muxed output</b>
	—	O2		<b>Reserved</b>
	—	O3		<b>Reserved</b>
	—	O4		<b>Reserved</b>
	—	O5		<b>Reserved</b>
	—	O6		<b>Reserved</b>
	CCU60_CC60	O7		<b>T12 PWM channel 60</b>
IOM_MON1_2		<b>Monitor input 1</b>		
IOM_REF1_6		<b>Reference input 1</b>		

表 2-57 端口 P34 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
U12	P34.3	I	SLOW / PU1 / VEVRSB / ES	General-purpose input
	GTM_TIM5_IN5_10			Mux input channel 5 of TIM module 5
	GTM_TIM3_IN6_13			Mux input channel 6 of TIM module 3
	GTM_TIM2_IN5_9			Mux input channel 5 of TIM module 2
	EVADC_G10CH9	AI		Analog input channel 9, group 10
	P34.3	O0		General-purpose output
	GTM_TOUT148	O1		GTM muxed output
	ASCLIN4_ASCLK	O2		Shift clock output
	—	O3		Reserved
	QSPI2_SLSO10	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT60	O7		T12 PWM channel 60
	IOM_MON1_3			Monitor input 1
IOM_REF1_3	Reference input 1			
T13	P34.4	I	SLOW / PU1 / VEVRSB / ES	General-purpose input
	GTM_TIM5_IN6_10			Mux input channel 6 of TIM module 5
	GTM_TIM3_IN7_12			Mux input channel 7 of TIM module 3
	GTM_TIM2_IN6_8			Mux input channel 6 of TIM module 2
	QSPI2_MRSTD			Master SPI data input
	EVADC_G10CH8	AI		Analog input channel 8, group 10
	P34.4	O0		General-purpose output
	GTM_TOUT149	O1		GTM muxed output
	ASCLIN4_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	QSPI2_MRST	O4		Slave SPI data output
	IOM_MON2_2	O5		Monitor input 2
	IOM_REF2_2			Reference input 2
	—			Reserved
	EVADC_FC6BFLOUT	O6		Boundary flag output, FC channel 6
	CCU60_CC61	O7		T12 PWM channel 61
IOM_MON1_1	Monitor input 1			
IOM_REF1_5	Reference input 1			

表 2-57 端口 P34 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
U13	P34.5	I	FAST / PU1 / VEVRSB / ES	General-purpose input
	GTM_TIM5_IN7_9			Mux input channel 7 of TIM module 5
	GTM_TIM4_IN7_12			Mux input channel 7 of TIM module 4
	GTM_TIM2_IN7_9			Mux input channel 7 of TIM module 2
	QSPI2_MTSRD			Slave SPI data input
	ASCLIN8_ARXE			Receive input
	P34.5	O0		General-purpose output
	GTM_TOUT150	O1		GTM muxed output
	ASCLIN8_ATX	O2		Transmit output
	—	O3		Reserved
	QSPI2_MTSR	O4		Master SPI data output
	—	O5		Reserved
	EVADC_FC7BFLOUT	O6		Boundary flag output, FC channel 7
	CCU60_COUT61	O7		T12 PWM channel 61
IOM_MON1_4		Monitor input 1		
IOM_REF1_2		Reference input 1		

表 2-58 端口 P50 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
C2	P50.0	I	LVDS_R X / HighZ / VEXT / ES	—
	RIF0_D1N			LVDS RX Input (inverted Data Bits of Channel #0)
C1	P50.1	I	LVDS_R X / HighZ / VEXT / ES	—
	RIF0_D1P			LVDS RX Input (Data Bits of Channel #0)
D2	P50.2	I	LVDS_R X / HighZ / VEXT / ES	—
	RIF0_D2N			LVDS RX Input (inverted Data Bits of Channel #1)
D1	P50.3	I	LVDS_R X / HighZ / VEXT / ES	—
	RIF0_D2P			LVDS RX Input (Data Bits of Channel #1)
E2	P50.4	I	LVDS_R X / HighZ / VEXT / ES	—
	RIF0_CLKN			LVDS RX Input (inverted Serial Clock)

表 2-58 端口 P50 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
E1	P50.5	I	LVDS_R X / HighZ / VEXT / ES	—
	RIF0_CLKP			<b>LVDS RX Input (Serial Clock)</b>
F2	P50.6	I	LVDS_R X / HighZ / VEXT / ES	—
	RIF0_FRP			<b>LVDS RX Input (FrameClock)</b>
F1	P50.7	I	LVDS_R X / HighZ / VEXT / ES	—
	RIF0_FRN			<b>LVDS RX Input (inverted FrameClock)</b>
G2	P50.8	I	LVDS_R X / HighZ / VEXT / ES	—
	RIF0_D3P			<b>LVDS RX Input (Data Bits of Channel #2)</b>
G1	P50.9	I	LVDS_R X / HighZ / VEXT / ES	—
	RIF0_D3N			<b>LVDS RX Input (inverted Data Bits of Channel #2)</b>
H2	P50.10	I	LVDS_R X / HighZ / VEXT / ES	—
	RIF0_D4P			<b>LVDS RX Input (Data Bits of Channel #3)</b>
H1	P50.11	I	LVDS_R X / HighZ / VEXT / ES	—
	RIF0_D4N			<b>LVDS RX Input (inverted Data Bits of Channel #3)</b>

表 2-59 端口 P51 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
B9	P51.0	I	LVDS_R X / HighZ / VEXT / ES	—
	RIF1_D1N			<b>LVDS RX Input (inverted Data Bits of Channel #0)</b>
A9	P51.1	I	LVDS_R X / HighZ / VEXT / ES	—
	RIF1_D1P			<b>LVDS RX Input (Data Bits of Channel #0)</b>
B8	P51.2	I	LVDS_R X / HighZ / VEXT / ES	—
	RIF1_D2N			<b>LVDS RX Input (inverted Data Bits of Channel #1)</b>

表 2-59 端口 P51 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A8	P51.3	I	LVDS_R X / HighZ / VEXT / ES	—
	RIF1_D2P			<b>LVDS RX Input (Data Bits of Channel #1)</b>
B7	P51.4	I	LVDS_R X / HighZ / VEXT / ES	—
	RIF1_CLKN			<b>LVDS RX Input (inverted Serial Clock)</b>
A7	P51.5	I	LVDS_R X / HighZ / VEXT / ES	—
	RIF1_CLKP			<b>LVDS RX Input (Serial Clock)</b>
B6	P51.6	I	LVDS_R X / HighZ / VEXT / ES	—
	RIF1_FRP			<b>LVDS RX Input (FrameClock)</b>
A6	P51.7	I	LVDS_R X / HighZ / VEXT / ES	—
	RIF1_FRN			<b>LVDS RX Input (inverted FrameClock)</b>
B5	P51.8	I	LVDS_R X / HighZ / VEXT / ES	—
	RIF1_D3P			<b>LVDS RX Input (Data Bits of Channel #2)</b>
A5	P51.9	I	LVDS_R X / HighZ / VEXT / ES	—
	RIF1_D3N			<b>LVDS RX Input (inverted Data Bits of Channel #2)</b>
B4	P51.10	I	LVDS_R X / HighZ / VEXT / ES	—
	RIF1_D4P			<b>LVDS RX Input (Data Bits of Channel #3)</b>
A4	P51.11	I	LVDS_R X / HighZ / VEXT / ES	—
	RIF1_D4N			<b>LVDS RX Input (inverted Data Bits of Channel #3)</b>

表 2-60 模拟输入

Ball	Symbol	Ctrl.	Buffer Type	Function
T10	AN0	I	D / HighZ / VDDM	<b>Analog Input 0</b>
	EVADC_G0CH0			<b>Analog input channel 0, group 0</b>
	EDSADC_EDS3PA			<b>Positive analog input channel 3, pin A</b>

表 2-60 模拟输入 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
U10	AN1	I	D / HighZ / VDDM	<b>Analog Input 1</b>
	EVADC_G0CH1			<b>Analog input channel 1, group 0</b>
	EDSADC_EDS3NA			<b>Negative analog input channel 3, pin A</b>
W9	AN2	I	D / HighZ / VDDM	<b>Analog Input 2</b>
	EVADC_G0CH2			<b>Analog input channel 2, group 0</b>
	EDSADC_EDS0PA			<b>Positive analog input channel 0, pin A</b>
U9	AN3	I	D / HighZ / VDDM	<b>Analog Input 3</b>
	EVADC_G0CH3			<b>Analog input channel 3, group 0</b>
	EDSADC_EDS0NA			<b>Negative analog input channel 0, pin A</b>
T9	AN4	I	D / HighZ / VDDM	<b>Analog Input 4</b>
	EVADC_G11CH0			<b>Analog input channel 0, group 11</b>
	EVADC_G0CH4			<b>Analog input channel 4, group 0</b>
Y9	AN5	I	D / HighZ / VDDM	<b>Analog Input 5</b>
	EVADC_G11CH1			<b>Analog input channel 1, group 11</b>
	EVADC_G0CH5			<b>Analog input channel 5, group 0</b>
T8	AN6	I	D / HighZ / VDDM	<b>Analog Input 6</b>
	EVADC_G11CH2			<b>Analog input channel 2, group 11</b>
	EVADC_G0CH6			<b>Analog input channel 6, group 0</b>
U8	AN7	I	D / HighZ / VDDM	<b>Analog Input 7</b>
	EVADC_G11CH3			<b>Analog input channel 3, group 11</b>
	EVADC_G0CH7			<b>Analog input channel 7, group 0</b>
W8	AN8	I	D / HighZ / VDDM	<b>Analog Input 8</b>
	EVADC_G11CH4			<b>Analog input channel 4, group 11</b>
	EVADC_G1CH0			<b>Analog input channel 0, group 1</b>
U7	AN9	I	D / HighZ / VDDM	<b>Analog Input 9</b>
	EVADC_G11CH5			<b>Analog input channel 5, group 11</b>
	EVADC_G1CH1			<b>Analog input channel 1, group 1</b>
Y8	AN10	I	D / HighZ / VDDM	<b>Analog Input 10</b>
	EVADC_G11CH6			<b>Analog input channel 6, group 11</b>
	EVADC_G1CH2			<b>Analog input channel 2, group 1</b>
W7	AN11	I	D / HighZ / VDDM	<b>Analog Input 11</b>
	EVADC_G11CH7			<b>Analog input channel 7, group 11</b>
	EVADC_G1CH3			<b>Analog input channel 3, group 1</b>
T7	AN12	I	D / HighZ / VDDM	<b>Analog Input 12</b>
	EVADC_G1CH4			<b>Analog input channel 4, group 1</b>
	EDSADC_EDS0PB			<b>Positive analog input channel 0, pin B</b>

表 2-60 模拟输入 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
W6	AN13	I	D / HighZ / VDDM	<b>Analog Input 13</b>
	EVADC_G1CH5			<b>Analog input channel 5, group 1</b>
	EDSADC_EDS0NB			<b>Negative analog input channel 0, pin B</b>
U6	AN14	I	D / HighZ / VDDM	<b>Analog Input 14</b>
	EVADC_G1CH6			<b>Analog input channel 6, group 1</b>
	EDSADC_EDS3PB			<b>Positive analog input channel 3, pin B</b>
T6	AN15	I	D / HighZ / VDDM	<b>Analog Input 15</b>
	EVADC_G1CH7			<b>Analog input channel 7, group 1</b>
	EDSADC_EDS3NB			<b>Negative analog input channel 3, pin N</b>
W5	AN16	I	D / HighZ / VDDM	<b>Analog Input 16</b>
	EVADC_G2CH0			<b>Analog input channel 0, group 2</b>
	EVADC_FC0CH0			<b>Analog input FC channel 0</b>
U5	AN17/P40.10	I	S / HighZ / VDDM	<b>Analog Input 17</b>
	SENT_SENT10A			<b>Receive input channel 10</b>
	EVADC_G2CH1			<b>Analog input channel 1, group 2</b>
	EVADC_FC1CH0			<b>Analog input FC channel 1</b>
W4	AN18/P40.11	I	S / HighZ / VDDM	<b>Analog Input 18</b>
	SENT_SENT11A			<b>Receive input channel 11</b>
	EVADC_G11CH8			<b>Analog input channel 8, group 11</b>
	EVADC_G2CH2			<b>Analog input channel 2, group 2</b>
W3	AN19/P40.12	I	S / HighZ / VDDM	<b>Analog Input 19</b>
	SENT_SENT12A			<b>Receive input channel 12</b>
	EVADC_G11CH9			<b>Analog input channel 9, group 11</b>
	EVADC_G2CH3			<b>Analog input channel 3, group 2</b>
Y3	AN20	I	D / HighZ / VDDM	<b>Analog Input 20</b>
	EVADC_G2CH4			<b>Analog input channel 4, group 2</b>
	EDSADC_EDS2PA			<b>Positive analog input channel 2, pin A</b>
Y2	AN21	I	D / HighZ / VDDM	<b>Analog Input 21</b>
	EVADC_G2CH5			<b>Analog input channel 5, group 2</b>
	EDSADC_EDS2NA			<b>Negative analog input channel 2, pin A</b>
T5	AN22	I	D / HighZ / VDDM	<b>Analog Input 22</b>
	EVADC_G2CH6			<b>Analog input channel 6, group 2</b>
R5	AN23	I	D / HighZ / VDDM	<b>Analog Input 23</b>
	EVADC_G2CH7			<b>Analog input channel 7, group 2</b>

表 2-60 模拟输入 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
T4	AN24/P40.0	I	S / HighZ / VDDM	<b>Analog Input 24</b>
	SENT_SENT0A			<b>Receive input channel 0</b>
	EVADC_G3CH0			<b>Analog input channel 0, group 3</b>
	CCU60_CCPOS0D			<b>Hall capture input 0</b>
	EDSADC_EDS2PB			<b>Positive analog input channel 2, pin B</b>
R4	AN25/P40.1	I	S / HighZ / VDDM	<b>Analog Input 25</b>
	SENT_SENT1A			<b>Receive input channel 1</b>
	EVADC_G3CH1			<b>Analog input channel 1, group 3</b>
	CCU60_CCPOS1B			<b>Hall capture input 1</b>
	EDSADC_EDS2NB			<b>Negative analog input channel 2, pin B</b>
W1	AN36/P40.6	I	S / HighZ / VDDM	<b>Analog Input 36</b>
	SENT_SENT6A			<b>Receive input channel 6</b>
	EVADC_G8CH4			<b>Analog input channel 4, group 8</b>
	CCU61_CCPOS1B			<b>Hall capture input 1</b>
	EDSADC_EDS1PA			<b>Positive analog input channel 1, pin A</b>
V2	AN37/P40.7	I	S / HighZ / VDDM	<b>Analog Input 37</b>
	SENT_SENT7A			<b>Receive input channel 7</b>
	EVADC_G8CH5			<b>Analog input channel 5, group 8</b>
	CCU61_CCPOS1D			<b>Hall capture input 1</b>
	EDSADC_EDS1NA			<b>Negative analog input channel 1, pin A</b>
W2	AN38/P40.8	I	S / HighZ / VDDM	<b>Analog Input 38</b>
	SENT_SENT8A			<b>Receive input channel 8</b>
	EVADC_G8CH6			<b>Analog input channel 6, group 8</b>
	CCU61_CCPOS2B			<b>Hall capture input 2</b>
	EDSADC_EDS1PB			<b>Positive analog input channel 1, pin B</b>
V1	AN39/P40.9	I	S / HighZ / VDDM	<b>Analog Input 39</b>
	SENT_SENT9A			<b>Receive input channel 9</b>
	EVADC_G8CH7			<b>Analog input channel 7, group 8</b>
	CCU61_CCPOS2D			<b>Hall capture input 2</b>
	EDSADC_EDS1NB			<b>Negative analog input channel 1, pin B</b>
U1	AN44	I	D / HighZ / VDDM	<b>Analog Input 44</b>
	EVADC_G8CH12			<b>Analog input channel 12, group 8</b>
	EDSADC_EDS1PC			<b>Positive analog input channel 1, pin C</b>
P5	AN45	I	D / HighZ / VDDM	<b>Analog Input 45</b>
	EVADC_G8CH13			<b>Analog input channel 13, group 8</b>
	EDSADC_EDS1NC			<b>Negative analog input channel 1, pin C</b>

表 2-60 模拟输入 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
U2	AN46	I	D / HighZ / VDDM	<b>Analog Input 46</b>
	EVADC_G8CH14			<b>Analog input channel 14, group 8</b>
	EDSADC_EDS1PD			<b>Positive analog input channel 1, pin D</b>
P4	AN47	I	D / HighZ / VDDM	<b>Analog Input 47</b>
	EVADC_G8CH15			<b>Analog input channel 15, group 8</b>
	EDSADC_EDS1ND			<b>Negative analog input channel 1, pin D</b>

注释：端口引脚P32.0和P32.1是双向引脚，具有以下两个功能：

- 如果将这些引脚用作标准GPIO，则可以使用P32.0和P32.1引脚配置表中定义的功能。
- 如果引脚用作外部MOSFET的预驱动器（内部DCDC情况），P32.0和P32.1将充当名为VGATE1N和VGATE1P的模拟IO。

表 2-61 系统 I/O

Ball	Symbol	Ctrl.	Buffer Type	Function
L7	AGBTCLKN (VSS)	I	AGBT_C LK / VEXT	<b>Input PAD (negative pole) for the external 100 MHz differential clock.</b> AGBT Input; (TC3xx devices without AGBT: VSS)
K7	AGBTCLKP (VSS)	I	AGBT_C LK / VEXT	<b>Input PAD (positive pole) for the external 100 MHz differential clock.</b> AGBT Input; (TC3xx devices without AGBT: VSS)
P10	AGBTTXN (VSS)	O	AGBT_T X / VEXT	<b>Off-chip driver output PAD of the 2.5Gbps transmitter, negative pole</b> AGBT Output; (TC3xx devices without AGBT: VSS)
P11	AGBTTXP (VSS)	O	AGBT_T X / VEXT	<b>Off-chip driver output PAD of the 2.5Gbps transmitter, positive pole</b> AGBT Output; (TC3xx devices without AGBT: VSS)
L14	AGBTERR (VSS)	I	FAST / PD / VEXT	<b>Input PAD for CRC error from FPGA.</b> AGBT Input; (TC3xx devices without AGBT: VSS)
W17	VGATE1P	O	—	<b>DCDC P ch. MOSFET gate driver output</b> P32.1 / External Pass Device gate control for EVRC
Y17	VGATE1N	O	—	<b>DCDC N ch. MOSFET gate driver output</b> P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
M20	XTAL1	I	XTAL / VEXT	<b>XTAL pad1</b> XTAL1. Main Oscillator/PLL/Clock Generator Input.
M19	XTAL2	O	XTAL / VEXT	<b>XTAL pad2</b> XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT

表 2-61 系统 I/O (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
K14	DAPE0	I	FAST / PD2 / VEXT	<b>DAPE: DAPE0 Clock Input</b> DAPE: DAPE0 clock input (PD Devices: NC)
L19	TRST	I	FAST /	<b>JTAG Module Reset/Enable Input</b>
	DAPE0	I	PU2 / VEXT	<b>DAPE: DAPE0 Clock Input</b>
K16	TMS	I	FAST /	<b>JTAG Module State Machine Control Input</b>
	DAP1	I/O	PD2 / VEXT	<b>DAP: DAP1 Data I/O</b>
J16	TCK	I	FAST /	<b>JTAG Module Clock Input</b>
	DAP0	I	PD2 / VEXT	<b>DAP: DAP0 Clock Input</b>
G11	DAPE1	I/O	FAST / PD2 / VEXT	<b>DAPE: DAPE1 Data I/O</b> DAPE: DAPE1 Data I/O (PD Devices: VSS)
G10	DAPE2	I/O	FAST / PD2 / VEXT	<b>DAPE: DAPE2 Data I/O</b> DAPE: DAPE2 Data I/O (PD Devices: VSS)
G16	ESR1	I/O	FAST / PU1 / VEXT	<b>ESR1 Port Pin input - can be used to trigger a reset or an NMI</b> ESR1: External System Request Reset 1. Default NMI function. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter 'Reset Control Unit' and SCU_IOCRR register description. PMS_EVRWUP: EVR Wakeup Pin
	PMS_ESR1WKP	I		<b>ESR1 pin input</b>
F16	ESR0	I/O	FAST / OD / VEXT	<b>ESR0 Port Pin input - can be used to trigger a reset or an NMI</b> ESR0: External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter 'Reset Control Unit' and SCU_IOCRR register description. PMS_EVRWUP: EVR Wakeup Pin
	PMS_ESR0WKP	I		<b>ESR0 pin input</b>
G17	PORST	I/O	PORST / PD / VEXT	<b>PORST pin</b> Power On Reset Input. Additional strong PD in case of power fail.

表 2-62 供电

Ball	Symbol	Ctrl.	Buffer Type	Function
P8, P13, N7, N14, E15, H14, D16, G13, G8, H7	VDD		—	<b>Digital Core Power Supply (1.25V)</b>
A2, B3, V19, W20	VEXT		—	<b>External Power Supply (5V / 3.3V)</b>
D5	VFLEX		—	<b>Digital Power Supply for Flex Port Pads (5V / 3.3V)</b>
Y5	VDDM		—	<b>ADC Analog Power Supply (5V / 3.3V)</b>
B18, A19	VDDP3		—	<b>Flash Power Supply (3.3V)</b>
B2, D4, E5, T16, U17, W19, Y20, E16, D17, B19, A20	VSS		—	<b>Digital Ground</b>
Y4	VSSM		—	<b>Analog Ground for VDDM</b>
P9, P12, N9, N10, N11, N12, M7, M8, M10, M11, M13, M14, L8, L9, L10, L11, L12, L13, K8, K9, K10, K11, K12, K13, J7, J8, J10, J11, J13, J14, H9, H10, H11, H12, G9, G12	VSS		—	<b>Digital Ground</b>
L20	VSS		—	<b>Oscillator Ground, VSS(OSC)</b>
Y6	VAREF1		—	<b>Positive Analog Reference Voltage 1</b>
Y7	VAGND1		—	<b>Negative Analog Reference Voltage 1</b>
T1	VAREF2		—	<b>Positive Analog Reference Voltage 2</b>
T2	VAGND2		—	<b>Negative Analog Reference Voltage 2</b>
A3, B1	NC		—	<b>Not connected. These pins are reserved for future extensions and shall not be connected externally</b>
A1, Y1, U4	NC1		—	<b>Not connected. These pins are not connected on package level and will not be used for future extensions</b>
T11	VEVRSB		—	<b>Standby Power Supply (5V / 3.3V) for the Standby SRAM</b>

表 2-62 供电 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
N19	VDD	I	—	<b>Digital Power Supply for Oscillator (1.25V), VDD(OSC)</b>
N20	VEXT	I	—	<b>Digital Power Supply for Oscillator (shall be supplied with same level as used for VEXT), VEXT(OSC)</b>

## 2.4 焊盘框中焊盘的顺序

表2-63 焊盘清单

Number	Pad Name	Pad Type	X	Y	Comment
1	VEXT	Vx	255699	175644	Supply Voltage
2	VSS	Vx	356499	175644	Supply Voltage
3	P14.0	FAST / PU1 / VEXT / ES2	457299	175644	General-purpose I/O
4	P15.7	FAST / PU1 / VEXT / ES	558099	175644	General-purpose I/O
5	VDDP3	Vx	635499	322614	Supply Voltage
6	VDD	Vx	714699	175644	Supply Voltage
7	P15.10	LVDS_TX / FAST / PU1 / VEXT / ES6	826200	322614	General-purpose I/O
8	P15.11	LVDS_TX / FAST / PU1 / VEXT / ES6	920196	322614	General-purpose I/O
9	VSS	Vx	1031697	175644	Supply Voltage
10	P15.12	LVDS_TX / FAST / PU1 / VEXT / ES6	1143198	322614	General-purpose I/O
11	P15.13	LVDS_TX / FAST / PU1 / VEXT / ES6	1237194	322614	General-purpose I/O
12	P14.4	SLOW / PU2 / VEXT / ES	1348695	175644	General-purpose I/O
13	P15.15	FAST / PU1 / VEXT / ES	1395693	322614	General-purpose I/O
14	VDD	Vx	1463499	175644	Supply Voltage
15	P15.14	FAST / PU1 / VEXT / ES	1517499	322614	General-purpose I/O
16	P14.3	SLOW / PU2 / VEXT / ES	1564497	175644	General-purpose I/O
17	P14.11	SLOW / PU1 / VEXT / ES	1611495	322614	General-purpose I/O
18	VSS	Vx	1665999	175644	Supply Voltage
19	P14.1	FAST / PU1 / VEXT / ES2	1724499	322614	General-purpose I/O
20	P15.8	FAST / PU1 / VEXT / ES	1771497	175644	General-purpose I/O
21	P14.13	FAST / PU1 / VEXT / ES	1818495	322614	General-purpose I/O
22	VSS	Vx	1865493	175644	Supply Voltage

**表2-63 焊盘清单 (续)**

Number	Pad Name	Pad Type	X	Y	Comment
23	P14.12	SLOW / PU1 / VEXT / ES	1912491	322614	General-purpose I/O
24	VEXT	Vx	1959489	175644	Supply Voltage
25	P14.5	FAST / PU2 / VEXT / ES	2006487	322614	General-purpose I/O
26	VDD	Vx	2069505	175644	Supply Voltage
27	P14.15	SLOW / PU1 / VEXT / ES	2125503	322614	General-purpose I/O
28	P14.6	FAST / PU1 / VEXT / ES	2172501	175644	General-purpose I/O
29	P14.14	FAST / PU1 / VEXT / ES	2219499	322614	General-purpose I/O
30	P14.7	SLOW / PU1 / VEXT / ES	2266497	175644	General-purpose I/O
31	P14.8	SLOW / PU1 / VEXT / ES	2313495	322614	General-purpose I/O
32	VSS	Vx	2375001	175644	Supply Voltage
33	P13.0	LVDS_TX / FAST / PU1 / VEXT / ES6	2486502	322614	General-purpose I/O
34	P13.1	LVDS_TX / FAST / PU1 / VEXT / ES6	2580498	322614	General-purpose I/O
35	VDD	Vx	2691999	175644	Supply Voltage
36	VDD	Vx	2781999	175644	Supply Voltage
37	P13.2	LVDS_TX / FAST / PU1 / VEXT / ES6	2893500	322614	General-purpose I/O
38	P13.3	LVDS_TX / FAST / PU1 / VEXT / ES6	2987496	322614	General-purpose I/O
39	VSS	Vx	3098997	175644	Supply Voltage
40	VSS	Vx	3188997	175644	Supply Voltage
41	P13.4	LVDS_TX / FAST / PU1 / VEXT / ES6	3300498	322614	General-purpose I/O
42	P13.5	LVDS_TX / FAST / PU1 / VEXT / ES6	3394494	322614	General-purpose I/O
43	P14.2	SLOW / PU2 / VEXT / ES	3505995	175644	General-purpose I/O

**表2-63 焊盘清单 (续)**

Number	Pad Name	Pad Type	X	Y	Comment
44	P13.6	LVDS_TX / FAST / PU1 / VEXT / ES6	3617496	322614	General-purpose I/O
45	P13.7	LVDS_TX / FAST / PU1 / VEXT / ES6	3711492	322614	General-purpose I/O
46	VDD	Vx	3822993	322614	Supply Voltage
47	VSS	Vx	3869991	175644	Supply Voltage
48	VSS	Vx	3974499	175644	Supply Voltage
49	VDD	Vx	4064499	322614	Supply Voltage
50	VEXT	Vx	4152501	175644	Supply Voltage
51	VDDP3	Vx	4334499	175644	Supply Voltage
52	VDDP3	Vx	4388499	322614	Supply Voltage
53	VDDP3	Vx	4469499	175644	Supply Voltage
54	VSS	Vx	4556979	175644	Supply Voltage
55	P13.10	SLOW / PU1 / VEXT / ES	4603977	322614	General-purpose I/O
56	P13.9	FAST / PU1 / VEXT / ES	4650975	175644	General-purpose I/O
57	P13.11	SLOW / PU1 / VEXT / ES	4697973	322614	General-purpose I/O
58	P14.9	LVDS_RX / FAST / PU1 / VEXT / ES	4773024	175644	General-purpose I/O
59	P14.10	LVDS_RX / FAST / PU1 / VEXT / ES	4867020	175644	General-purpose I/O
60	P13.12	SLOW / PU1 / VEXT / ES	4942071	322614	General-purpose I/O
61	VDD	Vx	5031567	175644	Supply Voltage
62	P13.13	SLOW / PU1 / VEXT / ES	5125563	322614	General-purpose I/O
63	VSS	Vx	5219559	175644	Supply Voltage
64	P13.14	SLOW / PU1 / VEXT / ES	5309055	322614	General-purpose I/O
65	VSS	Vx	5356053	175644	Supply Voltage
66	P13.15	SLOW / PU1 / VEXT / ES	5403051	322614	General-purpose I/O
67	VEXT	Vx	5450049	175644	Supply Voltage
68	P12.0	SLOW / PU1 / VFLEX / ES	5547231	322614	General-purpose I/O

**表2-63 焊盘清单 (续)**

Number	Pad Name	Pad Type	X	Y	Comment
69	P12.1	SLOW / PU1 / VFLEX / ES	5594229	175644	General-purpose I/O
70	P11.0	RFAST / PU1 / VFLEX / ES	5703633	322614	General-purpose I/O
71	VFLEX	Vx	5750631	175644	Supply Voltage
72	P11.1	RFAST / PU1 / VFLEX / ES	5825835	322614	General-purpose I/O
73	VSS	Vx	5872833	175644	Supply Voltage
74	P11.2	RFAST / PU1 / VFLEX / ES	5948037	322614	General-purpose I/O
75	VDD	Vx	5995035	175644	Supply Voltage
76	P11.4	RFAST / PU1 / VFLEX / ES	6110739	322614	General-purpose I/O
77	VSS	Vx	6198237	175644	Supply Voltage
78	P11.3	RFAST / PU1 / VFLEX / ES	6273441	322614	General-purpose I/O
79	VFLEX	Vx	6320439	175644	Supply Voltage
80	P11.6	RFAST / PU1 / VFLEX / ES	6395643	322614	General-purpose I/O
81	VSS	Vx	6442641	175644	Supply Voltage
82	P11.5	SLOW / RGMII_Input / PU1 / VFLEX / ES	6489639	322614	General-purpose I/O
83	VDD	Vx	6602499	175644	Supply Voltage
84	VSS	Vx	6687999	175644	Supply Voltage
85	P11.7	SLOW / RGMII_Input / PU1 / VFLEX / ES	6791499	175644	General-purpose I/O
86	P11.9	FAST / RGMII_Input / PU1 / VFLEX / ES	6842097	322614	General-purpose I/O
87	VFLEX	Vx	6892695	175644	Supply Voltage
88	P11.8	SLOW / RGMII_Input / PU1 / VFLEX / ES	6939693	322614	General-purpose I/O
89	P11.10	FAST / RGMII_Input / PU1 / VFLEX / ES	6990291	175644	General-purpose I/O

**表2-63 焊盘清单 (续)**

Number	Pad Name	Pad Type	X	Y	Comment
90	P11.11	FAST / RGMII_Input / PU1 / VFLEX / ES	7040889	322614	General-purpose I/O
91	VSS	Vx	7091487	175644	Supply Voltage
92	P11.12	FAST / RGMII_Input / PU1 / VFLEX / ES	7138485	322614	General-purpose I/O
93	VDD	Vx	7209999	175644	Supply Voltage
94	VSS	Vx	7302285	175644	Supply Voltage
95	P11.14	SLOW / PU1 / VFLEX / ES	7399503	322614	General-purpose I/O
96	P11.13	SLOW / PU1 / VFLEX / ES	7446501	175644	General-purpose I/O
97	P11.15	SLOW / PU1 / VFLEX / ES	7493499	322614	General-purpose I/O
98	VSS	Vx	7567713	175644	Supply Voltage
99	VDD	Vx	7632711	322614	Supply Voltage
100	P10.0	SLOW / PU1 / VEXT / ES	7715709	322614	General-purpose I/O
101	P10.1	FAST / PU1 / VEXT / ES	7762707	175644	General-purpose I/O
102	P10.3	FAST / PU1 / VEXT / ES	7809705	322614	General-purpose I/O
103	P10.4	FAST / PU1 / VEXT / ES	7856703	175644	General-purpose I/O
104	P10.2	FAST / PU1 / VEXT / ES	7903701	322614	General-purpose I/O
105	VSS	Vx	7950699	175644	Supply Voltage
106	P10.6	SLOW / PU2 / VEXT / ES	7997697	322614	General-purpose I/O
107	P10.5	SLOW / PU2 / VEXT / ES	8044695	175644	General-purpose I/O
108	P10.7	SLOW / PU1 / VEXT / ES	8091693	322614	General-purpose I/O
109	VEXT	Vx	8138691	175644	Supply Voltage
110	P10.9	SLOW / PU1 / VEXT / ES	8185689	322614	General-purpose I/O
111	P10.8	SLOW / PU1 / VEXT / ES	8232687	175644	General-purpose I/O
112	VDDSB	Vx	8279685	322614	Supply Voltage

**表2-63 焊盘清单 (续)**

Number	Pad Name	Pad Type	X	Y	Comment
113	VSS	Vx	8326683	175644	Supply Voltage
114	P10.10	SLOW / PU1 / VEXT / ES	8389701	322614	General-purpose I/O
115	VSS	Vx	8436699	175644	Supply Voltage
116	P10.11	SLOW / PU1 / VEXT / ES	8483697	322614	General-purpose I/O
117	VDD	Vx	8548695	175644	Supply Voltage
118	P10.13	SLOW / PU1 / VEXT / ES	8613693	322614	General-purpose I/O
119	VSS	Vx	8685513	175644	Supply Voltage
120	VDDSB	Vx	8732511	322614	Supply Voltage
121	VDDSB	Vx	8815509	322614	Supply Voltage
122	VSS	Vx	8862507	175644	Supply Voltage
123	P10.14	SLOW / PU1 / VEXT / ES	8909505	322614	General-purpose I/O
124	VEXT	Vx	8956503	175644	Supply Voltage
125	P10.15	SLOW / PU1 / VEXT / ES	9003501	322614	General-purpose I/O
126	P51.0	LVDS_RX / HighZ / VEXT / ES	9067500	175644	General-purpose I/O
127	P51.1	LVDS_RX / HighZ / VEXT / ES	9148500	175644	General-purpose I/O
128	P51.2	LVDS_RX / HighZ / VEXT / ES	9229500	175644	General-purpose I/O
129	P51.3	LVDS_RX / HighZ / VEXT / ES	9310500	175644	General-purpose I/O
130	P51.4	LVDS_RX / HighZ / VEXT / ES	9391500	175644	General-purpose I/O
131	P51.5	LVDS_RX / HighZ / VEXT / ES	9472500	175644	General-purpose I/O
132	P51.6	LVDS_RX / HighZ / VEXT / ES	9589500	175644	General-purpose I/O
133	P51.7	LVDS_RX / HighZ / VEXT / ES	9670500	175644	General-purpose I/O

**表2-63 焊盘清单 (续)**

Number	Pad Name	Pad Type	X	Y	Comment
134	P51.8	LVDS_RX / HighZ / VEXT / ES	9751500	175644	General-purpose I/O
135	P51.9	LVDS_RX / HighZ / VEXT / ES	9832500	175644	General-purpose I/O
136	P51.10	LVDS_RX / HighZ / VEXT / ES	9913500	175644	General-purpose I/O
137	P51.11	LVDS_RX / HighZ / VEXT / ES	9994500	175644	General-purpose I/O
138	VDDSB	Vx	10085499	175644	Supply Voltage
139	VSS	Vx	10185741	175644	Supply Voltage
140	VEXT	Vx	10265796	255699	Supply Voltage
141	VSS	Vx	10265796	356499	Supply Voltage
142	P50.0	LVDS_RX / HighZ / VEXT / ES	10265796	474300	General-purpose I/O
143	P50.1	LVDS_RX / HighZ / VEXT / ES	10265796	555300	General-purpose I/O
144	P50.2	LVDS_RX / HighZ / VEXT / ES	10265796	636300	General-purpose I/O
145	P50.3	LVDS_RX / HighZ / VEXT / ES	10265796	717300	General-purpose I/O
146	P50.4	LVDS_RX / HighZ / VEXT / ES	10265796	798300	General-purpose I/O
147	P50.5	LVDS_RX / HighZ / VEXT / ES	10265796	879300	General-purpose I/O
148	P50.6	LVDS_RX / HighZ / VEXT / ES	10265796	996300	General-purpose I/O
149	P50.7	LVDS_RX / HighZ / VEXT / ES	10265796	1077300	General-purpose I/O
150	P50.8	LVDS_RX / HighZ / VEXT / ES	10265796	1158300	General-purpose I/O

**表2-63 焊盘清单 (续)**

Number	Pad Name	Pad Type	X	Y	Comment
151	P50.9	LVDS_RX / HighZ / VEXT / ES	10265796	1239300	General-purpose I/O
152	P50.10	LVDS_RX / HighZ / VEXT / ES	10265796	1320300	General-purpose I/O
153	P50.11	LVDS_RX / HighZ / VEXT / ES	10265796	1401300	General-purpose I/O
154	VDDSB	Vx	10118826	1465299	Supply Voltage
155	VSS	Vx	10265796	1512297	Supply Voltage
156	P02.13	SLOW / PU1 / VEXT / ES	10118826	1586295	General-purpose I/O
157	VDD	Vx	10265796	1679499	Supply Voltage
158	P02.12	SLOW / PU1 / VEXT / ES	10118826	1751499	General-purpose I/O
159	VEXT	Vx	10265796	1798497	Supply Voltage
160	P02.15	FAST / PU1 / VEXT / ES	10118826	1845495	General-purpose I/O
161	VSS	Vx	10265796	1892493	Supply Voltage
162	P02.14	SLOW / PU1 / VEXT / ES	10118826	1939491	General-purpose I/O
163	P02.9	SLOW / PU1 / VEXT / ES	10265796	1986489	General-purpose I/O
164	P02.4	FAST / PU1 / VEXT / ES	10118826	2033487	General-purpose I/O
165	P02.0	FAST / PU1 / VEXT / ES	10265796	2080485	General-purpose I/O
166	P02.5	FAST / PU1 / VEXT / ES	10118826	2127483	General-purpose I/O
167	P02.1	SLOW / PU1 / VEXT / ES	10265796	2174481	General-purpose I/O
168	P01.0	SLOW / PU1 / VEXT / ES	10118826	2221479	General-purpose I/O
169	VSS	Vx	10265796	2292975	Supply Voltage
170	VSS	Vx	10265796	2411199	Supply Voltage
171	VDDSB	Vx	10118826	2458197	Supply Voltage
172	P02.11	SLOW / PU1 / VEXT / ES	10265796	2505195	General-purpose I/O
173	P02.6	FAST / PU1 / VEXT / ES	10118826	2552193	General-purpose I/O

**表2-63 焊盘清单 (续)**

Number	Pad Name	Pad Type	X	Y	Comment
174	P02.2	FAST / PU1 / VEXT / ES	10265796	2599191	General-purpose I/O
175	P01.1	SLOW / PU1 / VEXT / ES	10118826	2646189	General-purpose I/O
176	P02.3	SLOW / PU1 / VEXT / ES	10265796	2693187	General-purpose I/O
177	P01.2	SLOW / PU1 / VEXT / ES	10118826	2740185	General-purpose I/O
178	VDD	Vx	10265796	2831499	Supply Voltage
179	VDD	Vx	10265796	2921499	Supply Voltage
180	P02.7	FAST / PU1 / VEXT / ES	10265796	3037437	General-purpose I/O
181	VSS	Vx	10265796	3146499	Supply Voltage
182	P01.8	SLOW / PU1 / VEXT / ES	10118826	3285567	General-purpose I/O
183	P02.10	SLOW / PU1 / VEXT / ES	10265796	3332565	General-purpose I/O
184	P01.9	SLOW / PU1 / VEXT / ES	10118826	3379563	General-purpose I/O
185	P01.4	SLOW / PU1 / VEXT / ES	10265796	3426561	General-purpose I/O
186	P02.8	SLOW / PU1 / VEXT / ES	10118826	3473559	General-purpose I/O
187	VSS	Vx	10265796	3596553	Supply Voltage
188	VDDSB	Vx	10118826	3643551	Supply Voltage
189	VEXT	Vx	10265796	3708549	Supply Voltage
190	P01.11	SLOW / PU1 / VEXT / ES	10118826	3755547	General-purpose I/O
191	VSS	Vx	10265796	3802545	Supply Voltage
192	P01.10	SLOW / PU1 / VEXT / ES	10118826	3849543	General-purpose I/O
193	P01.3	SLOW / PU1 / VEXT / ES	10265796	3896541	General-purpose I/O
194	P00.0	FAST / PU1 / VEXT / ES	10118826	3943539	General-purpose I/O
195	P01.6	FAST / PU1 / VEXT / ES	10265796	3990537	General-purpose I/O
196	P01.13	FAST / PU1 / VEXT / ES	10118826	4037535	General-purpose I/O
197	P01.5	SLOW / PU1 / VEXT / ES	10265796	4084533	General-purpose I/O

**表2-63 焊盘清单 (续)**

Number	Pad Name	Pad Type	X	Y	Comment
198	P01.12	FAST / PU1 / VEXT / ES	10118826	4131531	General-purpose I/O
199	VDD	Vx	10265796	4225527	Supply Voltage
200	P01.15	SLOW / PU1 / VEXT / ES	10118826	4319523	General-purpose I/O
201	VSS	Vx	10265796	4413519	Supply Voltage
202	VDDSB	Vx	10118826	4460517	Supply Voltage
203	VDDSB	Vx	10118826	4554513	Supply Voltage
204	VSS	Vx	10265796	4601511	Supply Voltage
205	P01.14	FAST / PU1 / VEXT / ES	10118826	4687515	General-purpose I/O
206	RESERVED	Vx	10265796	4734513	OTPMust be bonded to VSS
207	P00.13	FAST / PU1 / VEXT / ES	10118826	4781511	General-purpose I/O
208	VDD	Vx	10265796	4875507	Supply Voltage
209	P00.15	FAST / PU1 / VEXT / ES	10118826	4969503	General-purpose I/O
210	P01.7	FAST / PU1 / VEXT / ES	10265796	5016501	General-purpose I/O
211	P00.14	SLOW / PU1 / VEXT / ES	10118826	5063499	General-purpose I/O
212	VSS	Vx	10265796	5153499	Supply Voltage
213	VDD	Vx	10265796	5243499	Supply Voltage
214	VDD	Vx	10265796	5333499	Supply Voltage
215	P00.1	SLOW / PU1 / VEXT / ES	10265796	5471442	General-purpose I/O
216	P00.2	SLOW / PU1 / VEXT / ES1	10118826	5518440	General-purpose I/O
217	P00.3	SLOW / PU1 / VEXT / ES1	10265796	5565438	General-purpose I/O
218	P00.4	SLOW / PU1 / VEXT / ES1	10118826	5612436	General-purpose I/O
219	VSS	Vx	10265796	5659434	Supply Voltage
220	P00.5	SLOW / PU1 / VEXT / ES1	10118826	5706432	General-purpose I/O
221	VEXT	Vx	10265796	5753430	Supply Voltage
222	P00.6	SLOW / PU1 / VEXT / ES1	10118826	5800428	General-purpose I/O
223	P00.7	SLOW / PU1 / VEXT / ES1	10265796	5847426	General-purpose I/O

**表2-63 焊盘清单 (续)**

Number	Pad Name	Pad Type	X	Y	Comment
224	P00.8	SLOW / PU1 / VEXT / ES1	10118826	5894424	General-purpose I/O
225	P00.9	SLOW / PU1 / VEXT / ES1	10265796	5941422	General-purpose I/O
226	P00.10	SLOW / PU1 / VEXT / ES1	10118826	5988420	General-purpose I/O
227	P00.11	SLOW / PU1 / VEXT / ES1	10265796	6035418	General-purpose I/O
228	P00.12	SLOW / PU1 / VEXT / ES1	10118826	6082416	General-purpose I/O
229	AN47	D / HighZ / VDDM	10265796	6156630	Analog Input 47
230	VDDM	Vx	10118826	6203628	Supply Voltage
231	VSSM	Vx	10265796	6250626	Supply Voltage
232	AN46	D / HighZ / VDDM	10118826	6297624	Analog Input 46
233	AN45	D / HighZ / VDDM	10265796	6344622	Analog Input 45
234	VDDM	Vx	10118826	6391620	Supply Voltage
235	VSSM	Vx	10265796	6438618	Supply Voltage
236	AN44	D / HighZ / VDDM	10118826	6485616	Analog Input 44
237	VAREF5	Vx	10265796	6532614	Supply Voltage
238	VAREF4	Vx	10118826	6594615	Supply Voltage
239	VAGND5	Vx	10265796	6656616	Supply Voltage
240	VAGND4	Vx	10118826	6718617	Supply Voltage
241	AN43	D / HighZ / VDDM	10265796	6765615	Analog Input 43
242	AN42	D / HighZ / VDDM	10118826	6812613	Analog Input 42
243	VSSM	Vx	10265796	6859611	Supply Voltage
244	VDDM	Vx	10118826	6906609	Supply Voltage
245	AN41	D / HighZ / VDDM	10265796	6953607	Analog Input 41
246	AN40	D / HighZ / VDDM	10118826	7000605	Analog Input 40
247	VSSM	Vx	10265796	7047603	Supply Voltage
248	AN39/P40.9	S / HighZ / VDDM	10118826	7094601	Analog Input 39
249	VDDM_EXT_CONVPAD	Vx	10265796	7141599	Supply Voltage

**表2-63 焊盘清单 (续)**

Number	Pad Name	Pad Type	X	Y	Comment
250	AN38/P40.8	S / HighZ / VDDM	10118826	7188597	Analog Input 38
251	AN37/P40.7	S / HighZ / VDDM	10265796	7235595	Analog Input 37
252	AN36/P40.6	S / HighZ / VDDM	10118826	7282593	Analog Input 36
253	AN35	D / HighZ / VDDM	10265796	7329591	Analog Input 35
254	AN34	D / HighZ / VDDM	10118826	7376589	Analog Input 34
255	AN33/P40.5	S / HighZ / VDDM	10265796	7423587	Analog Input 33
256	AN32/P40.4	S / HighZ / VDDM	10118826	7470585	Analog Input 32
257	VAREF3	Vx	10265796	7517583	Supply Voltage
258	VAREF2	Vx	10118826	7579584	Supply Voltage
259	VAGND3	Vx	10265796	7641585	Supply Voltage
260	VAGND2	Vx	10118826	7703586	Supply Voltage
261	AN73	D / HighZ / VDDM	10265796	7750584	Analog Input 73
262	AN72	D / HighZ / VDDM	10118826	7797582	Analog Input 72
263	AN71/P41.3	S / HighZ / VDDM	10265796	7844580	Analog Input 71
264	AN70/P41.2	S / HighZ / VDDM	10118826	7891578	Analog Input 70
265	AN69/P41.1	S / HighZ / VDDM	10265796	7938576	Analog Input 69
266	AN68/P41.0	S / HighZ / VDDM	10118826	7985574	Analog Input 68
267	AN67/P40.15	S / HighZ / VDDM	10265796	8032572	Analog Input 67
268	AN66	D / HighZ / VDDM	10118826	8079570	Analog Input 66
269	AN65	D / HighZ / VDDM	10265796	8126568	Analog Input 65
270	VDDM_EXT_ CONVIF	Vx	10118826	8173566	Supply Voltage
271	VSSM_CONVI F	Vx	10265796	8220564	Supply Voltage
272	AN64/P41.8	S / HighZ / VDDM	10118826	8267562	Analog Input 64

**表2-63 焊盘清单 (续)**

Number	Pad Name	Pad Type	X	Y	Comment
273	AN63/P41.7	S / HighZ / VDDM	10265796	8314560	Analog Input 63
274	AN62/P41.6	S / HighZ / VDDM	10118826	8361558	Analog Input 62
275	AN61	D / HighZ / VDDM	10265796	8408556	Analog Input 61
276	AN60	D / HighZ / VDDM	10118826	8455554	Analog Input 60
277	AN59	D / HighZ / VDDM	10265796	8502552	Analog Input 59
278	AN58	D / HighZ / VDDM	10118826	8549550	Analog Input 58
279	AN57	D / HighZ / VDDM	10265796	8596548	Analog Input 57
280	AN56	D / HighZ / VDDM	10118826	8643546	Analog Input 56
281	AN55/P41.5	S / HighZ / VDDM	10265796	8690544	Analog Input 55
282	AN54/P41.4	S / HighZ / VDDM	10118826	8737542	Analog Input 54
283	AN53	D / HighZ / VDDM	10265796	8784540	Analog Input 53
284	AN52	D / HighZ / VDDM	10118826	8831538	Analog Input 52
285	AN51	D / HighZ / VDDM	10265796	8878536	Analog Input 51
286	AN50	D / HighZ / VDDM	10265796	8958537	Analog Input 50
287	AN49	D / HighZ / VDDM	10265796	9038538	Analog Input 49
288	AN48	D / HighZ / VDDM	10265796	9118539	Analog Input 48
289	AN31	D / HighZ / VDDM	10194939	9189396	Analog Input 31
290	AN30	D / HighZ / VDDM	10114938	9189396	Analog Input 30
291	AN29/P40.14	S / HighZ / VDDM	10034937	9189396	Analog Input 29
292	AN28/P40.13	S / HighZ / VDDM	9954936	9189396	Analog Input 28
293	AN27/P40.3	S / HighZ / VDDM	9907938	9042426	Analog Input 27

**表2-63 焊盘清单 (续)**

Number	Pad Name	Pad Type	X	Y	Comment
294	AN26/P40.2	S / HighZ / VDDM	9860940	9189396	Analog Input 26
295	AN25/P40.1	S / HighZ / VDDM	9813942	9042426	Analog Input 25
296	AN24/P40.0	S / HighZ / VDDM	9766944	9189396	Analog Input 24
297	AN23	D / HighZ / VDDM	9719946	9042426	Analog Input 23
298	AN22	D / HighZ / VDDM	9672948	9189396	Analog Input 22
299	AN21	D / HighZ / VDDM	9625950	9042426	Analog Input 21
300	AN20	D / HighZ / VDDM	9578952	9189396	Analog Input 20
301	AN19/P40.12	S / HighZ / VDDM	9531954	9042426	Analog Input 19
302	AN18/P40.11	S / HighZ / VDDM	9484956	9189396	Analog Input 18
303	AN17/P40.10	S / HighZ / VDDM	9437958	9042426	Analog Input 17
304	AN16	D / HighZ / VDDM	9390960	9189396	Analog Input 16
305	AN15	D / HighZ / VDDM	9343962	9042426	Analog Input 15
306	VAGND1	Vx	9296964	9189396	Supply Voltage
307	VAGND0	Vx	9249966	9042426	Supply Voltage
308	VAREF1	Vx	9202968	9189396	Supply Voltage
309	VAREF0	Vx	9155970	9042426	Supply Voltage
310	AN14	D / HighZ / VDDM	9108972	9189396	Analog Input 14
311	VDDM	Vx	9061974	9042426	Supply Voltage
312	VSSM	Vx	9014976	9189396	Supply Voltage
313	AN13	D / HighZ / VDDM	8967978	9042426	Analog Input 13
314	VSSM	Vx	8920980	9189396	Supply Voltage
315	VDDM	Vx	8873982	9042426	Supply Voltage
316	AN12	D / HighZ / VDDM	8826984	9189396	Analog Input 12
317	AN11	D / HighZ / VDDM	8779986	9042426	Analog Input 11
318	AN10	D / HighZ / VDDM	8732988	9189396	Analog Input 10

**表2-63 焊盘清单 (续)**

Number	Pad Name	Pad Type	X	Y	Comment
319	AN9	D / HighZ / VDDM	8685990	9042426	Analog Input 9
320	AN8	D / HighZ / VDDM	8638992	9189396	Analog Input 8
321	AN7	D / HighZ / VDDM	8591994	9042426	Analog Input 7
322	AN6	D / HighZ / VDDM	8544996	9189396	Analog Input 6
323	AN5	D / HighZ / VDDM	8497998	9042426	Analog Input 5
324	AN4	D / HighZ / VDDM	8451000	9189396	Analog Input 4
325	AN3	D / HighZ / VDDM	8404002	9042426	Analog Input 3
326	AN2	D / HighZ / VDDM	8357004	9189396	Analog Input 2
327	AN1	D / HighZ / VDDM	8310006	9042426	Analog Input 1
328	AN0	D / HighZ / VDDM	8263008	9189396	Analog Input 0
329	VEVRSB	Vx	8176041	9042426	Supply Voltage
330	VSS	Vx	8104041	9189396	Supply Voltage
331	VDD	Vx	8057043	9042426	Supply Voltage
332	VSS	Vx	8010045	9189396	Supply Voltage
333	AGBTCLKN (VSS)	AGBT_CLK / VEXT	7888959	9189441	Input PAD (negative pole) for the external 100 MHz differential clock. AGBT Input; (TC3xx devices without AGBT: VSS)
334	AGBTCLKP (VSS)	AGBT_CLK / VEXT	7807869	9189441	Input PAD (positive pole) for the external 100 MHz differential clock. AGBT Input; (TC3xx devices without AGBT: VSS)
335	VEXT	Vx	7726959	9189441	Supply Voltage
336	VSS	Vx	7645959	9189441	Supply Voltage
337	AGBTTXN (VSS)	AGBT_TX / VEXT	7538027	9189441	Off-chip driver output PAD of the 2.5Gbps transmitter, negative pole AGBT Output; (TC3xx devices without AGBT: VSS)

**表2-63 焊盘清单 (续)**

Number	Pad Name	Pad Type	X	Y	Comment
338	AGBTTXP (VSS)	AGBT_TX / VEXT	7456937	9189441	Off-chip driver output PAD of the 2.5Gbps transmitter, positive pole AGBT Output; (TC3xx devices without AGBT: VSS)
339	AGBTERR (VSS)	FAST / PD / VEXT	7266739	9189302	Input PAD for CRC error from FPGA. AGBT Input; (TC3xx devices without AGBT: VSS)
340	VDD	Vx	7168018	9042426	Supply Voltage
341	VSS	Vx	7121020	9189396	Supply Voltage
342	P33.1	SLOW / PU1 / VEVRSB / ES5	7071741	9042426	General-purpose I/O
343	P33.0	SLOW / PU1 / VEVRSB / ES5	7024743	9189396	General-purpose I/O
344	P33.3	SLOW / PU1 / VEVRSB / ES5	6977745	9042426	General-purpose I/O
345	P33.2	SLOW / PU1 / VEVRSB / ES5	6930747	9189396	General-purpose I/O
346	P33.5	SLOW / PU1 / VEVRSB / ES5	6883749	9042426	General-purpose I/O
347	P34.1	SLOW / PU1 / VEVRSB / ES5	6836751	9189396	General-purpose I/O
348	P33.4	SLOW / PU1 / VEVRSB / ES5	6789753	9042426	General-purpose I/O
349	P34.3	SLOW / PU1 / VEVRSB / ES	6742755	9189396	General-purpose I/O
350	P33.7	SLOW / PU1 / VEVRSB / ES5	6695757	9042426	General-purpose I/O
351	VSS	Vx	6605559	9189396	Supply Voltage
352	VDD	Vx	6558561	9042426	Supply Voltage
353	P34.2	SLOW / PU1 / VEVRSB / ES	6511563	9189396	General-purpose I/O
354	P33.6	SLOW / PU1 / VEVRSB / ES5	6464565	9042426	General-purpose I/O

**表2-63 焊盘清单 (续)**

Number	Pad Name	Pad Type	X	Y	Comment
355	VSS	Vx	6417567	9189396	Supply Voltage
356	P33.9	SLOW / PU1 / VEVRSB / ES5	6370569	9042426	General-purpose I/O
357	VEVRSB	Vx	6323571	9189396	Supply Voltage
358	P33.8	FAST / HighZ / VEVRSB	6276573	9042426	General-purpose I/O
359	P34.5	FAST / PU1 / VEVRSB / ES	6229575	9189396	General-purpose I/O
360	P33.11	FAST / PU1 / VEVRSB / ES5	6182577	9042426	General-purpose I/O
361	P34.4	SLOW / PU1 / VEVRSB / ES	6135579	9189396	General-purpose I/O
362	P33.10	FAST / PU1 / VEVRSB / ES5	6088581	9042426	General-purpose I/O
363	P33.15	SLOW / PU1 / VEVRSB / ES5	6041583	9189396	General-purpose I/O
364	P33.13	FAST / PU1 / VEVRSB / ES5	5994585	9042426	General-purpose I/O
365	P33.14	FAST / PU1 / VEVRSB / ES5	5947587	9189396	General-purpose I/O
366	VEVRSB	Vx	5853591	9042426	Supply Voltage
367	VEVRSB	Vx	5806593	9189396	Supply Voltage
368	P33.12	FAST / PU1 / VEVRSB / ES5	5759595	9042426	General-purpose I/O
369	VSS	Vx	5712597	9189396	Supply Voltage
370	VEXT	Vx	5629383	9042426	Supply Voltage
371	P32.1	SLOW / PU1 / VEXT / ES	5582385	9189396	General-purpose I/O
372	VGATE1P	Vx	5535387	9042426	DCDC P ch. MOSFET gate driver output
373	VSS	Vx	5488389	9189396	Supply Voltage
374	VGATE1N	Vx	5441391	9042426	DCDC N ch. MOSFET gate driver output
375	P32.0	SLOW / PU1 / VEXT / ES	5394393	9189396	General-purpose I/O
376	VDD	Vx	5287941	9189396	Supply Voltage

**表2-63 焊盘清单 (续)**

Number	Pad Name	Pad Type	X	Y	Comment
377	VSS	Vx	5197941	9189396	Supply Voltage
381	RESERVED	Vx	4747941	9189396	PBIST_OFF Must be bonded to VSS
383	VDD	Vx	4621941	9189396	Supply Voltage
384	VDD	Vx	4504941	9189396	Supply Voltage
386	VSS	Vx	4414941	9189396	Supply Voltage
387	VSS	Vx	4306941	9189396	Supply Voltage
388	VSS	Vx	4171941	9189396	Supply Voltage
389	VDD	Vx	4036941	9189396	Supply Voltage
390	P32.2	SLOW / PU1 / VEXT / ES	3915927	9042426	General-purpose I/O
391	P32.5	SLOW / PU1 / VEXT / ES	3868929	9189396	General-purpose I/O
392	P32.4	FAST / PU1 / VEXT / ES	3821931	9042426	General-purpose I/O
393	VSS	Vx	3774933	9189396	Supply Voltage
394	P32.3	SLOW / PU1 / VEXT / ES	3727935	9042426	General-purpose I/O
395	VEXT	Vx	3680937	9189396	Supply Voltage
396	P32.7	SLOW / PU1 / VEXT / ES	3633939	9042426	General-purpose I/O
397	P32.6	SLOW / PU1 / VEXT / ES	3586941	9189396	General-purpose I/O
398	VDD	Vx	3496941	9189396	Supply Voltage
399	VDD	Vx	3406941	9189396	Supply Voltage
400	VDD	Vx	3316941	9189396	Supply Voltage
401	VSS	Vx	3226941	9189396	Supply Voltage
402	VSS	Vx	3136941	9189396	Supply Voltage
403	VSS	Vx	3046941	9189396	Supply Voltage
404	VDD	Vx	2999943	9042426	Supply Voltage
405	VDD	Vx	2844441	9189396	Supply Voltage
406	VSS	Vx	2754441	9189396	Supply Voltage
407	P31.0	FAST / PU1 / VEBU / ES	2653911	9189396	General-purpose I/O
408	P31.1	FAST / PU1 / VEBU / ES	2606913	9042426	General-purpose I/O
409	P31.2	FAST / PU1 / VEBU / ES	2559915	9189396	General-purpose I/O
410	P31.3	FAST / PU1 / VEBU / ES	2512917	9042426	General-purpose I/O
411	VSS	Vx	2465919	9189396	Supply Voltage

引脚定义及功能：焊盘框中焊盘的顺序

**表2-63 焊盘清单 (续)**

Number	Pad Name	Pad Type	X	Y	Comment
412	P31.4	FAST / PU1 / VEBU / ES	2418921	9042426	General-purpose I/O
413	P31.5	FAST / PU1 / VEBU / ES	2371923	9189396	General-purpose I/O
414	P31.6	FAST / PU1 / VEBU / ES	2324925	9042426	General-purpose I/O
415	P31.7	FAST / PU1 / VEBU / ES	2277927	9189396	General-purpose I/O
416	P31.8	FAST / PU1 / VEBU / ES	2230929	9042426	General-purpose I/O
417	VEBU	Vx	2183931	9189396	Supply Voltage
418	P31.9	FAST / PU1 / VEBU / ES	2136933	9042426	General-purpose I/O
419	P31.10	FAST / PU1 / VEBU / ES	2089935	9189396	General-purpose I/O
420	P31.11	FAST / PU1 / VEBU / ES	2042937	9042426	General-purpose I/O
421	P31.14	FAST / PU1 / VEBU / ES	1995939	9189396	General-purpose I/O
422	P31.12	FAST / PU1 / VEBU / ES	1948941	9042426	General-purpose I/O
423	VDD	Vx	1858941	9189396	Supply Voltage
424	VSS	Vx	1768941	9189396	Supply Voltage
425	P31.13	FAST / PU1 / VEBU / ES	1679913	9042426	General-purpose I/O
426	P31.15	FAST / PU1 / VEBU / ES	1632915	9189396	General-purpose I/O
427	P30.0	FAST / PU1 / VEBU / ES	1585917	9042426	General-purpose I/O
428	P30.1	FAST / PU1 / VEBU / ES	1538919	9189396	General-purpose I/O
429	P30.2	FAST / PU1 / VEBU / ES	1491921	9042426	General-purpose I/O
430	P30.3	FAST / PU1 / VEBU / ES	1444923	9189396	General-purpose I/O
431	P30.4	FAST / PU1 / VEBU / ES	1397925	9042426	General-purpose I/O
432	VEBU	Vx	1350927	9189396	Supply Voltage
433	P30.5	FAST / PU1 / VEBU / ES	1303929	9042426	General-purpose I/O
434	P30.6	FAST / PU1 / VEBU / ES	1256931	9189396	General-purpose I/O

**表2-63 焊盘清单 (续)**

Number	Pad Name	Pad Type	X	Y	Comment
435	P30.7	FAST / PU1 / VEBU / ES	1209933	9042426	General-purpose I/O
436	P30.8	FAST / PU1 / VEBU / ES	1162935	9189396	General-purpose I/O
437	P30.9	FAST / PU1 / VEBU / ES	1115937	9042426	General-purpose I/O
438	VSS	Vx	1068939	9189396	Supply Voltage
439	P30.10	FAST / PU1 / VEBU / ES	1021941	9042426	General-purpose I/O
440	VSS	Vx	931941	9189396	Supply Voltage
441	VDD	Vx	841941	9189396	Supply Voltage
442	P30.11	FAST / PU1 / VEBU / ES	754137	9042426	General-purpose I/O
443	P30.12	FAST / PU1 / VEBU / ES	707139	9189396	General-purpose I/O
444	P30.15	FAST / PU1 / VEBU / ES	660141	9042426	General-purpose I/O
445	P30.13	FAST / PU1 / VEBU / ES	559341	9189396	General-purpose I/O
446	P30.14	FAST / PU1 / VEBU / ES	458541	9189396	General-purpose I/O
447	P26.0	SLOW / PU1 / VEBU / ES	357741	9189396	General-purpose I/O
448	P25.0	FAST / PU1 / VEBU / ES	256941	9189396	General-purpose I/O
449	P25.1	FAST / PU1 / VEBU / ES	175644	9109341	General-purpose I/O
450	P25.2	FAST / PU1 / VEBU / ES	175644	9008541	General-purpose I/O
451	P25.3	FAST / PU1 / VEBU / ES	175644	8907741	General-purpose I/O
452	P25.4	FAST / PU1 / VEBU / ES	175644	8806941	General-purpose I/O
453	P25.5	FAST / PU1 / VEBU / ES	175644	8706141	General-purpose I/O
454	P25.7	FAST / PU1 / VEBU / ES	322614	8659143	General-purpose I/O
455	VEBU	Vx	175644	8612145	Supply Voltage
456	P25.9	FAST / PU1 / VEBU / ES	322614	8565147	General-purpose I/O
457	VSS	Vx	175644	8518149	Supply Voltage

**表2-63 焊盘清单 (续)**

Number	Pad Name	Pad Type	X	Y	Comment
458	P25.8	FAST / PU1 / VEBU / ES	322614	8471151	General-purpose I/O
459	VDD	Vx	175644	8410653	Supply Voltage
460	P25.11	FAST / PU1 / VEBU / ES	322614	8350155	General-purpose I/O
461	VSS	Vx	175644	8289657	Supply Voltage
462	P25.10	FAST / PU1 / VEBU / ES	322614	8229159	General-purpose I/O
463	P25.12	FAST / PU1 / VEBU / ES	175644	8182161	General-purpose I/O
464	P25.13	FAST / PU1 / VEBU / ES	322614	8135163	General-purpose I/O
465	P25.14	FAST / PU1 / VEBU / ES	175644	8088165	General-purpose I/O
466	P25.15	FAST / PU1 / VEBU / ES	322614	8041167	General-purpose I/O
467	P25.6	FAST / PU1 / VEBU / ES	175644	7994169	General-purpose I/O
468	P24.1	FAST / PU1 / VEBU / ES	322614	7947171	General-purpose I/O
469	P24.0	FAST / PU1 / VEBU / ES	175644	7900173	General-purpose I/O
470	P24.3	FAST / PU1 / VEBU / ES	322614	7853175	General-purpose I/O
471	VDD	Vx	175644	7780041	Supply Voltage
472	P24.2	FAST / PU1 / VEBU / ES	322614	7708041	General-purpose I/O
473	VSS	Vx	175644	7645041	Supply Voltage
474	P24.5	FAST / PU1 / VEBU / ES	322614	7577667	General-purpose I/O
475	P24.4	FAST / PU1 / VEBU / ES	175644	7530669	General-purpose I/O
476	P24.7	FAST / PU1 / VEBU / ES	322614	7483671	General-purpose I/O
477	P24.6	FAST / PU1 / VEBU / ES	175644	7436673	General-purpose I/O
478	P24.9	FAST / PU1 / VEBU / ES	322614	7389675	General-purpose I/O
479	VEBU	Vx	175644	7342677	Supply Voltage
480	P24.11	FAST / PU1 / VEBU / ES	322614	7295679	General-purpose I/O
481	VSS	Vx	175644	7248681	Supply Voltage

**表2-63 焊盘清单 (续)**

Number	Pad Name	Pad Type	X	Y	Comment
482	P24.13	FAST / PU1 / VEBU / ES	322614	7201683	General-purpose I/O
483	P24.8	FAST / PU1 / VEBU / ES	175644	7154685	General-purpose I/O
484	P24.14	FAST / PU1 / VEBU / ES	322614	7107687	General-purpose I/O
485	P24.10	FAST / PU1 / VEBU / ES	175644	7060689	General-purpose I/O
486	P24.15	FAST / PU1 / VEBU / ES	322614	7013691	General-purpose I/O
487	P24.12	FAST / PU1 / VEBU / ES	175644	6966693	General-purpose I/O
488	P23.0	SLOW / PU1 / VEXT / ES	322614	6892479	General-purpose I/O
489	VDD	Vx	175644	6785541	Supply Voltage
490	VDD	Vx	175644	6695541	Supply Voltage
491	P23.2	SLOW / PU1 / VEXT / ES	322614	6592041	General-purpose I/O
492	VSS	Vx	175644	6488541	Supply Voltage
493	VSS	Vx	175644	6398541	Supply Voltage
494	P23.1	FAST / PU1 / VEXT / ES	322614	6295041	General-purpose I/O
495	P23.5	FAST / PU1 / VEXT / ES	175644	6248043	General-purpose I/O
496	P23.4	FAST / PU1 / VEXT / ES	322614	6201045	General-purpose I/O
497	VSS	Vx	175644	6154047	Supply Voltage
498	P23.3	SLOW / PU1 / VEXT / ES	322614	6107049	General-purpose I/O
499	P23.6	SLOW / PU1 / VEXT / ES	175644	6060051	General-purpose I/O
500	VEXT	Vx	322614	6013053	Supply Voltage
501	P23.7	SLOW / PU1 / VEXT / ES	175644	5966055	General-purpose I/O
502	VDD	Vx	175644	5849541	Supply Voltage
503	VSS	Vx	175644	5759541	Supply Voltage
505	VDD	Vx	348147	5664825	Supply Voltage
506	VSS	Vx	179145	5617827	Supply Voltage
507	XTAL1	XTAL / VEXT	179145	5458176	XTAL pad1 XTAL1. Main Oscillator/PLL/Clock Generator Input.

**表2-63 焊盘清单 (续)**

Number	Pad Name	Pad Type	X	Y	Comment
508	XTAL2	XTAL / VEXT	179145	5364180	XTAL pad2 XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT
509	VSS	Vx	179145	5204529	Supply Voltage
510	VEXT	Vx	348147	5157531	Supply Voltage
512	P22.2	LVDS_TX / FAST / PU1 / VEXT / ES6	322614	4988520	General-purpose I/O
513	P22.3	LVDS_TX / FAST / PU1 / VEXT / ES6	322614	4894524	General-purpose I/O
514	VDD	Vx	322614	4783023	Supply Voltage
515	VSS	Vx	175644	4713525	Supply Voltage
516	P22.0	LVDS_TX / FAST / PU1 / VEXT / ES6	322614	4602024	General-purpose I/O
517	P22.1	LVDS_TX / FAST / PU1 / VEXT / ES6	322614	4508028	General-purpose I/O
518	P22.4	FAST / PU1 / VEXT / ES	175644	4396527	General-purpose I/O
519	P22.5	FAST / PU1 / VEXT / ES	322614	4349529	General-purpose I/O
520	P22.6	SLOW / PU1 / VEXT / ES	175644	4302531	General-purpose I/O
521	P22.7	SLOW / PU1 / VEXT / ES	322614	4255533	General-purpose I/O
522	VSS	Vx	175644	4208535	Supply Voltage
523	VEXT	Vx	322614	4161537	Supply Voltage
524	P22.8	SLOW / PU1 / VEXT / ES	175644	4114539	General-purpose I/O
525	P22.9	SLOW / PU1 / VEXT / ES	322614	4067541	General-purpose I/O
526	VDD	Vx	175644	3977541	Supply Voltage
527	VSS	Vx	175644	3887541	Supply Voltage
528	P22.10	SLOW / PU1 / VEXT / ES	175644	3797037	General-purpose I/O
529	P22.11	SLOW / PU1 / VEXT / ES	322614	3750039	General-purpose I/O
530	DAPE0	FAST / PD2 / VEXT	175644	3703041	DAPE: DAPE0 Clock Input DAPE: DAPE0 clock input (PD Devices: NC)

**表2-63 焊盘清单 (续)**

Number	Pad Name	Pad Type	X	Y	Comment
531	TRST	FAST / PU2 / VEXT	322614	3656043	JTAG Module Reset/Enable Input
532	VSS	Vx	175644	3609045	Supply Voltage
533	P21.0	LVDS_RX / FAST / PU1 / VEXT / ES	322614	3533994	General-purpose I/O
534	P21.1	LVDS_RX / FAST / PU1 / VEXT / ES	322614	3439998	General-purpose I/O
535	VDD	Vx	175644	3304647	Supply Voltage
536	P21.2	LVDS_RX / FAST / PU1 / VEXT / ES	322614	3211596	General-purpose I/O
537	P21.3	LVDS_RX / FAST / PU1 / VEXT / ES	322614	3117600	General-purpose I/O
538	VSS	Vx	175644	3024549	Supply Voltage
539	P21.4	LVDS_TX / FAST / PU1 / VEXT / ES6	322614	2913048	General-purpose I/O
540	P21.5	LVDS_TX / FAST / PU1 / VEXT / ES6	322614	2819052	General-purpose I/O
541	TMS	FAST / PD2 / VEXT	175644	2707551	JTAG Module State Machine Control Input
542	P20.0	FAST / PU1 / VEXT / ES	322614	2660553	General-purpose I/O
543	TCK	FAST / PD2 / VEXT	175644	2613555	JTAG Module Clock Input
544	P20.2	S / PU / VEXT	322614	2566557	General-purpose I/O This pin is latched at power on reset release to enter test mode.
545	VEXT	Vx	175644	2519559	Supply Voltage
546	VDD	Vx	175644	2436561	Supply Voltage
547	VDD	Vx	175644	2346561	Supply Voltage
548	VSS	Vx	175644	2229561	Supply Voltage
549	P20.3	SLOW / PU1 / VEXT / ES	322614	2081727	General-purpose I/O
550	DAPE1	FAST / PD2 / VEXT	175644	2034729	DAPE: DAPE1 Data I/O DAPE: DAPE1 Data I/O (PD Devices: VSS)

**表2-63 焊盘清单 (续)**

Number	Pad Name	Pad Type	X	Y	Comment
551	P21.6/TDI	FAST / PD / PU2 / VEXT / ES3	322614	1987731	General-purpose I/O PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ.
552	DAPE2	FAST / PD2 / VEXT	175644	1940733	DAPE: DAPE2 Data I/O DAPE: DAPE2 Data I/O (PD Devices: VSS)
553	VEXT	Vx	322614	1893735	Supply Voltage
554	VSS	Vx	175644	1846737	Supply Voltage
555	P21.7/TDO	FAST / PU2 / VEXT / ES4	322614	1799739	General-purpose I/O
556	ESR1	FAST / PU1 / VEXT	175644	1752741	ESR1 Port Pin input - can be used to trigger a reset or an NMI ESR1: External System Request Reset 1. Default NMI function. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter 'Reset Control Unit' and SCU_IOCR register description. PMS_EVRWUP: EVR Wakeup Pin
557	P20.8	FAST / PU1 / VEXT / ES	322614	1705743	General-purpose I/O
558	VDD	Vx	175644	1642725	Supply Voltage
559	VSS	Vx	175644	1557225	Supply Voltage
560	P20.1	SLOW / PU1 / VEXT / ES	322614	1494207	General-purpose I/O

**表2-63 焊盘清单 (续)**

Number	Pad Name	Pad Type	X	Y	Comment
561	ESR0	FAST / OD / VEXT	175644	1447209	ESR0 Port Pin input - can be used to trigger a reset or an NMI ESR0: External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter 'Reset Control Unit' and SCU_IOC register description. PMS_EVRWUP: EVR Wakeup Pin
562	PORST	PORST / PD / VEXT	322614	1400211	PORST pin Power On Reset Input. Additional strong PD in case of power fail.
563	P20.6	SLOW / PU1 / VEXT / ES	175644	1353213	General-purpose I/O
564	P20.11	FAST / PU1 / VEXT / ES	322614	1306215	General-purpose I/O
565	P15.5	FAST / PU1 / VEXT / ES	175644	1259217	General-purpose I/O
566	P20.7	FAST / PU1 / VEXT / ES	322614	1212219	General-purpose I/O
567	VSS	Vx	175644	1165221	Supply Voltage
568	P20.10	FAST / PU1 / VEXT / ES	322614	1118223	General-purpose I/O
569	VEXT	Vx	175644	1071225	Supply Voltage
570	P20.13	FAST / PU1 / VEXT / ES	322614	1024227	General-purpose I/O
571	VDD	Vx	175644	968229	Supply Voltage
572	P20.12	FAST / PU1 / VEXT / ES	322614	912231	General-purpose I/O
573	VSS	Vx	175644	856233	Supply Voltage
574	P20.14	FAST / PU1 / VEXT / ES	322614	800235	General-purpose I/O

表2-63 焊盘清单 (续)

Number	Pad Name	Pad Type	X	Y	Comment
575	P15.2	FAST / PU1 / VEXT / ES	175644	753237	General-purpose I/O
576	P15.0	FAST / PU1 / VEXT / ES	322614	706239	General-purpose I/O
577	P15.1	FAST / PU1 / VEXT / ES	175644	659241	General-purpose I/O
578	P15.3	FAST / PU1 / VEXT / ES	175644	558441	General-purpose I/O
579	P15.4	FAST / PU1 / VEXT / ES	175644	457641	General-purpose I/O
580	P15.6	FAST / PU1 / VEXT / ES	175644	356841	General-purpose I/O
581	P20.9	FAST / PU1 / VEXT / ES	175644	256041	General-purpose I/O

在第3节“电气规格”的表格中，每当使用术语“相邻焊盘”时，详细定义如图2-63所示。此表述也适用于次邻/最近邻焊盘。

为了找出谁在影响目标焊盘上的操作（干扰），必须定义大量活动的近邻焊盘（ACNP）。

寻找近邻焊盘。

焊盘环有四个边：底部、左侧、顶部、右侧。每条边都是有限的，即有两个端点。

每个焊盘都有两个直接（第一个）邻居，除非它位于边缘的末端。在这种情况下，它只有一个相邻焊盘。类似地，每个焊盘都有两个间接（第二）邻居，除非它或它的第一个邻居位于边缘的末端。我们将这些第一和第二个邻居统称为近邻焊盘。因此每个焊盘都有2到4个近邻焊盘。

可以按照以下顺序寻找近邻：

- 1.) 选择目标焊盘并在图2-63中查找其“X”和“Y”坐标。
- 2.) 通过计算与选定焊盘的“X”和“Y”距离来找到第一和第二个邻居。图2-63按“Y”坐标排序，这可能有助于定位4个近邻候选者（如果焊盘靠近边缘，则最终可能有少于4个近邻）。

定义活跃焊盘：

如果焊盘当前正在使用并且名称中没有“V<sub>xx</sub>”，则表示焊盘活跃。确定活跃的

邻近焊盘的数量遵循以下规则：

- 如果第一个邻居是活跃的，那么我们对其进行计数，并检查第二个邻居（在选定焊盘的另一侧）是否活跃。
- 如果第一个邻居不活跃，那么我们就不会检查另一侧的第二个邻居。

## 2.5 标志

本第 2 章中的数据与文件 TC39xed\_IO\_Spirit\_v2.0.0.1.24.xml 相匹配。

### Ctrl 列:

- I = 输入 (对于具有 IOCR 位字段选择  $PCx = 0XXX_B$  的 GPIO 端口)
- O = 输出 (对于 GPIO 端口, “O”在大多数情况下代表端口 HWOUT 功能)
- O0 = 带有 IOCR 位字段选择的输出  $PCx = 1X000_B$
- O1 = 带有 IOCR 位字段选择的输出  $PCx = 1X001_B$  (ALT1)
- O2 = 带 IOCR 位字段选择的输出  $PCx = 1X010_B$  (ALT2)
- O3 = 带 IOCR 位字段选择的输出  $PCx = 1X011_B$  (ALT3)
- O4 = 带 IOCR 位字段选择的输出  $PCx = 1X100_B$  (ALT4)
- O5 = 带 IOCR 位字段选择的输出  $PCx = 1X101_B$  (ALT5)
- O6 = 带 IOCR 位字段选择的输出  $PCx = 1X110_B$  (ALT6)
- O7 = 带 IOCR 位字段选择的输出  $PCx = 1X111_B$  (ALT7)

### “缓冲区类型”列:

- RFAST = 焊盘类 RFAST (5V/3.3V)
- FAST = 焊盘类 FAST (5V/3.3V)
- SLOW = 焊盘类 SLOW (5V/3.3V)
- LVDS\_TX = 焊盘类 LVDS 发送
- LVDS\_RX = 焊盘类 LVDS 接收
- S = 焊盘类 S (模拟输入覆盖通用输入)
- D = 焊盘类 D (模拟输入)
- Porst = Porst 输入焊盘
- XTAL1 = XTAL1 输入焊盘
- XTAL2 = XTAL2 输入焊盘

- PU = 复位期间连接上拉电阻 ( $\overline{PORST} = 0$ )
- PU1 = 复位期间连接上拉电阻 ( $\overline{PORST} = 0$ )<sup>1)</sup>
- PU2 = 启动和复位期间连接上拉电阻, 待机模式下为 HighZ
- PD = 复位期间连接下拉电阻 ( $\overline{PORST} = 0$ )
- PD1 = 在复位期间连接下拉电阻 ( $\overline{PORST} = 0$ )<sup>1)</sup>
- PD2 = 在启动和复位期间连接下拉电阻, 待机模式下为高阻态
- OD = 复位期间开漏 ( $\overline{PORST} = 0$ )
- ES = 支持紧急停止
- ES1=ES。ES 可被重用于VADC, 通过 P00\_PCSR 控制
- ES2=ES。ES 可以被用于DXCPL - DAP 通过 CAN 物理层, 不能被用于DXCM - 通过 CAN 消息调试
- ES3=ES。如果此引脚用作 TDI 则 ES 可以被用于JTAG 模式
- ES4 = ES, ES 可由 JTAG 或三引脚DAP 模式控制

1) PORST 下拉期间和之后, GPIO (Px.y) 的默认状态通过 HWCFG6 (P14.4) 控制。请另参阅 PMS、HWCFG[6] 章节。

ES5=ES。如果实施的话，备用控制器 (SCR) 可以重用 ES。可以通过控制寄存器 P33\_PCSR 和 P34\_PCSR 禁用重用

ES6=ES。在 LVDS TX 焊盘上，ES 仅在 CMOS 模式下影响焊盘，而不在 LVDS 模式下影响焊盘。因此，仅当 LPCRx.TX\_EN 选择 CMOS 模式时，ES 事件中输出才会关闭

## 3 电气规格参数

### 3.1 参数解释

本节列出的参数部分代表TC39x的特性，部分代表其对系统的要求。为了帮助在评估设计时轻松解释参数，它们在“符号”列中用两个字母的缩写标记：

- **CC**

这些参数表明了控制器特性（**C**ontroller **C**haracteristics），这是TC39x的一个显著特点，在系统设计中必须加以考虑。

- **SR**

这些参数表明了系统要求（**S**ystem **R**equirements），必须由采用TC39x设计的微处理器系统提供。

### 3.2 绝对最大额定值

超过“绝对最大额定值”所列值的载荷可能会对器件造成永久性损坏。这仅仅是一个载荷额定值，并不意味着设备在这些条件下或任何其他高于本规格操作部分所示条件的情况下能够正常运行。长时间暴露于绝对最大额定条件可能会影响器件的可靠性。

表 3-1 最大绝对额定值

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Storage Temperature	$T_{ST}$ SR	-65	-	150	°C	upto 65h @ $T_J = 150^\circ\text{C}$
Voltage at $V_{DD}$ power supply pins with respect to $V_{SS1}$ 2)	$V_{DD}$ SR	-	-	1.65	V	upto 2.8h
		-	-	1.45	V	upto 72h
Voltage at $V_{DDP3}$ power supply pins with respect to $V_{SS}$	$V_{DDP3}$ SR	-	-	4.43	V	
Voltage at $V_{DDM}$ , $V_{EXT}$ , $V_{FLEX}$ and $V_{EVR SB}$ power supply pins with respect to $V_{SS}$	$V_{DDM}$ SR	-	-	6.75	V	upto 2.8h
		-	-	5.6	V	upto 72h
Voltage on all analog and class S input pins with respect to $V_{SS}$ 3)	$V_{IN}$ SR	-0.7	-	6.75	V	
Voltage on all other input pins with respect to $V_{SS3}$	$V_{IN}$ SR	-0.7	-	6.75	V	
Input current on any pin during overload condition 4) 5)	$I_{IN}$ SR	-10	-	10	mA	
Absolute maximum sum of all input circuit currents during overload condition. 4)	$\Sigma I_{IN}$ SR	-100	-	100	mA	

- 1) 有效期累计长达2.8小时，脉冲形式跟随电源接通阶段，其中上升和下降时间与系统电容和电感有关。
- 2) 由于EVRC输出电压在开关关闭阶段振荡， $V_{DD}$ 可能降至-0.72V，对于 $V_{DD}$ ，输入电平降至关闭阶段的-0.72V不会造成任何损坏或可靠性问题。
- 3) 只要不违反受影响焊盘的过载引脚可靠性部分中定义的时间和电流，低于 $V_{INmin}$ 的电压就不会对器件可靠性产生影响。
- 4) 此参数是绝对最大额定值，长时间暴露于绝对最大额定值可能会损坏器件。
- 5) 指定的最小和最大值表示在运行期间未使用的任何快速、RFast、慢速和S级焊盘的输出端出现短路条件时必须维持的电流限值。  
这也涵盖了 $C_L=200\text{pF}$ 时由于操作切换而产生的输出电流。

### 3.3 过载下的引脚可靠性

当接收来自高压设备的信号时，低压设备会出现超出其自身 IO 电源规格的过载电流和电压。

下表定义了满足以下所有条件的情况下不会对可靠性造成任何负面影响的过载条件：

- 不超过过载条件允许的时间间隔（在注释栏中定义）。如果没有定义时间限制，则允许的时间包括“运行寿命小时数”和“非活动寿命小时数”。表 3-77 和 表 3-78 中的小时数仅作为示例，适用的数字由英飞凌接受的客户资料定义。
- 工作条件满足
  - 焊盘供电电平
  - 温度

如果引脚电流超出工作条件但在过载参数范围内，则无法再保证此引脚的参数功能符合工作条件中的规定。但在大多数情况下，操作仍可进行，因为参数宽松。

表 3-2 过载参数

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current on any digital pin during overload condition	$I_{IN}$	-5	-	5	mA	except LVDS pins
		-15 <sup>1)</sup>	-	15 <sup>1)</sup>	mA	except LVDS pins; limited to max. 20 pulses with 1ms pulse length
Input current on LVDS pin during overload condition	$I_{INLVDS}$	-3	-	3	mA	
Input current on analog input pin during overload condition	$I_{INANA}$	-3	-	3	mA	
		-5	-	5	mA	limited to 60h over lifetime
Absolute sum of all analog input currents for analog inputs during overload condition	$I_{INSA}$	-20	-	20	mA	
Absolute maximum sum of all input circuit currents during overload condition (digital and analog combined)	$\Sigma I_{INS}$	-100	-	100	mA	
Signal voltage over/undershoot at GPIOs	$V_{OUS}$	$V_{SS} - 2$	-	$V_{EXT/FLEX} + 2$	V	limited to 60h over lifetime; Valid for non LVDS and analog pads
Sum of all inactive device pin currents	$I_{IDS}$	-100	-	100	mA	
Static pin output current	$I_{OUT CC}$	-	-	2.5	mA	100% duty cycle; output driver = medium
		-	-	5	mA	100% duty cycle; output driver = strong

表 3-2 过载参数 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overload coupling factor for digital inputs, negative	$K_{\text{OVDN CC}}$	-	-	$3 \cdot 10^{-4}$		Overload injected on GPIO non LVDS pad and affecting neighbor fast pads; $-5\text{mA} < I_{\text{IN}} < 0\text{mA}$
		-	-	$2 \cdot 10^{-3}$		Overload injected on GPIO non LVDS pad and affecting neighbor slow pads VGASTE1N and VGATE1P; $-5\text{mA} < I_{\text{IN}} < 0\text{mA}$
		-	-	$1 \cdot 10^{-4}$		Overload injected on GPIO non LVDS pad and affecting neighbor slow pads; $-5\text{mA} < I_{\text{IN}} < 0\text{mA}$
		-	-	0.8		Overload injected on LVDS RX pad and affecting neighbor LVDS pads
		-	-	0.5		Overload injected on LVDS TX pad and affecting neighbor LVDS pads
		-	-			
Overload coupling factor for digital inputs, positive	$K_{\text{OVDP CC}}$	-	-	$1.5 \cdot 10^{-3}$		Overload injected on GPIO non LVDS pad and affecting neighbor GPIO non LVDS pads
		-	-	1		Overload injected on LVDS RX pad and affecting neighbor LVDS pads
		-	-	$5 \cdot 10^{-3}$		Overload injected on LVDS TX pad and affecting neighbor LVDS pads
Overload coupling factor for analog inputs, negative <sup>2)</sup>	$K_{\text{OVAN CC}}$	-	-	$1 \cdot 10^{-4}$		Analog inputs overlaid with slow pads or pull down diagnostics; $-5\text{mA} < I_{\text{IN}} < 0\text{mA}$
		-	-	$1 \cdot 10^{-5}$		else; $-5\text{mA} < I_{\text{IN}} < 0\text{mA}$

表 3-2 过载参数 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overload coupling factor for analog inputs, positive <sup>2)</sup>	$K_{OVAP\ CC}$	-	-	$2 \cdot 10^{-4}$		Analoge inputs overlaid with slow pads or pull down diagnostics; $0\text{mA} < I_{IN} < 5\text{mA}$
		-	-	$2 \cdot 10^{-5}$		else; $0\text{mA} < I_{IN} < 5\text{mA}$

- 1) 降低的 VADC / DSADC 结果精度和 / 或 GPIO 输入电平 ( $V_{IL}$  和  $V_{IH}$ ) 可能与指定参数不同。
- 2) 模拟输入上的过载耦合是由焊盘、输入多路复用器和周围结构之间的寄生效应引起的。已针对所有通道排列验证了给定的参数。还观察一个引脚与多个通道的多个连接。

### 3.4 工作条件

为了确保 TC39x 的正确操作和可靠性，不得超过以下工作条件。除非另有说明，以下部分中指定的所有参数均指这些工作条件。

施加到 TC39x 的数字电源电压必须是静态调节电压。

下表中指定的所有参数均指这些工作条件（见下表），除非在注释/测试条件栏中另有说明。

表 3-3 工作条件

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SRI frequency	$f_{SRI}$ SR	-	-	300	MHz	
CPU Frequency (All CPUs)	$f_{CPUx}$ SR	-	-	300	MHz	
PLL0 output frequency	$f_{PLL0}$ SR	20	-	300	MHz	
SPB frequency	$f_{SPB}$ SR	-	-	100	MHz	
FSI2 frequency	$f_{FSI2}$ SR	-	-	300	MHz	
FSI frequency	$f_{FSI}$ SR	20	-	100	MHz	
GTM frequency	$f_{GTM}$ SR	-	-	200	MHz	
STM frequency	$f_{STM}$ SR	-	-	100	MHz	
ERAY frequency	$f_{ERAY}$ SR	-	80	-	MHz	
BBB frequency	$f_{BBB}$ SR	-	-	150	MHz	
VADC frequency	$f_{ADC}$ SR	-	-	160	MHz	
ASCLIN Operating Frequency	$f_{ASCLINx}$ SR	-	-	200	MHz	
CAN frequency	$f_{CAN}$ SR	-	-	80	MHz	
EBU operating frequency	$f_{EBU}$ SR	-	-	160	MHz	
I2C frequency	$f_{I2C}$ SR	-	-	100	MHz	
Operating MSC Frequency	$f_{MSC}$ SR	-	-	200	MHz	
PLL1 output frequency from PER PLL	$f_{PLL1}$ SR	20	-	320	MHz	
PLL2 output frequency from PER PLL	$f_{PLL2}$ SR	20	-	200	MHz	
QSPI Frequency	$f_{QSPI}$ SR	-	-	200	MHz	
ADAS clock frequency	$f_{ADAS}$ CC	200	-	300	MHz	
MCANH frequency	$f_{MCANH}$ CC	-	-	100	MHz	
GETH frequency	$f_{GETH}$ CC	100	-	150	MHz	
Ambient Temperature	$T_A$ SR	-40	-	125	°C	valid for all SAK products
		-40	-	150	°C	valid for all SAL products with package

**表 3-3 工作条件 (续)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Junction Temperature	$T_{J\ SR}$	-40	-	150	°C	valid for all SAK products
		-40	-	170	°C	valid for all SAL products
Core Supply Voltage	$V_{DD\ SR}$	1.125 <sup>1)</sup>	1.25	1.375 <sup>2)</sup>	V	
ADC analog supply voltage	$V_{DDM\ SR}$	2.97	5.0	5.5 <sup>3)</sup>	V	
Digital external supply voltage for pads and EVR	$V_{EXT\ SR}$	4.5	5.0	5.5 <sup>3)</sup>	V	Nominal 5V Pad / Port Pin supply range. 5V pad parameters are valid.
		2.97	3.3	3.63	V	Nominal 3.3V Pad / Port Pin supply range with VDDP3 supplied externally and EVR33 inactive. 3.3V pad parameters are valid.
		3.6	-	4.5	V	Flash configured in cranking mode; Flash read operation with reduced performance. EVR33 active in low voltage mode. 3.3V pad parameters are valid.
		2.97	-	3.6	V	Incase EVR33 is active, Flash configured in sleep mode and execution switched to RAM. 3.3V pad parameters are valid.
Digital supply voltage for EBU	$V_{EBU\ CC}$	2.97	3.3	3.63	V	3.3V pad parameters are valid
		4.5	5	5.5	V	5V pad parameters are valid
Digital supply voltage for Flex port	$V_{FLEX\ SR}$	2.97	-	4.0	V	3.3V pad parameters are valid
		4.5	5.0	5.5 <sup>3)</sup>	V	5V pad parameters are valid
Digital supply voltage for Flash	$V_{DDP3\ SR}$	2.97	3.3	3.63 <sup>4)</sup>	V	
		2.6	-	3.63	V	Flash configured in cranking mode; Flash read operation with reduced performance.
Digital ground voltage	$V_{SS\ SR}$	0	-	-	V	

表 3-3 工作条件 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Analog ground voltage for $V_{DDM}$	$V_{SSM\ CC}$	-0.1	0	0.1	V	
Digital external supply voltage for EVR and during Standby mode	$V_{EVR\ SB\ SR}$	2.97 <sup>5)</sup>	-	5.5	V	
Voltage to ensure defined pad states	$V_{DDPPA\ CC}$	1.3 <sup>6)</sup>	-	-	V	

- 1) 对于  $V_{DD}$ , 当  $1.08V \leq V_{DD} < 1.125V$  时, 仍可进行操作, 参数宽松。
- 2) 允许过冲电压至 1.69V, 但累计持续时间不得超过 2 小时, ADC 精度降低且漏电增加。
- 3) 允许过冲电压至 6.5V, 但累计持续时间不得超过 2 小时, ADC 精度降低且漏电增加。
- 4) 允许过冲电压至 4.29V, 但累计持续时间不得超过 2 小时, ADC 精度降低且漏电增加。
- 5)  $V_{EVR\ SB}$  供电电压在待机模式下可降至 2.6V。  $V_{EVR\ SB}$  上需接一个 100nF 电容供应引脚。
- 6) 当 VEXT 达到此电平时, HWCFG[6] 引脚被锁存, 并且在端口引脚处激活上拉或三态。

### 供电电压随时间的限制

$V_{EXT/FLEX/DDM}$  电源轨的最大工作电压在整个使用寿命期间受到限制。

下面的电压曲线就是一个例子。为了满足质量和可靠性目标, 特定应用的电压分布需要经过英飞凌科技的验证。

表 3-4 电压曲线示例

$V_{EXT/FLEX/DDM} =$	Duration [h]
$5.4\ V < V_{EXT/FLEX/DDM} \leq 5.5\ V$	$\leq 5\%$ of lifetime
$5.15\ V < V_{EXT/FLEX/DDM} \leq 5.4\ V$	$\leq 15\%$ of lifetime
$4.85\ V < V_{EXT/FLEX/DDM} \leq 5.15\ V$	$\leq 60\%$ of lifetime
$4.6\ V < V_{EXT/FLEX/DDM} \leq 4.85\ V$	$\leq 15\%$ of lifetime
$4.5\ V < V_{EXT/FLEX/DDM} \leq 4.6\ V$	$\leq 5\%$ of lifetime

在整个使用寿命期间,  $V_{DD}$  电源轨的最大工作电压是有限的。

下面的电压曲线就是一个例子。为了满足质量和可靠性目标, 特定应用的电压分布需要经过英飞凌科技的验证。

表 3-5 电压曲线示例

$V_{DD} =$	Duration [h]
$1.325\ V < V_{DD} \leq 1.375\ V$	$\leq 5\%$ of lifetime
$1.275\ V < V_{DD} \leq 1.325\ V$	$\leq 15\%$ of lifetime
$1.225\ V < V_{DD} \leq 1.275\ V$	$\leq 60\%$ of lifetime
$1.175\ V < V_{DD} \leq 1.225\ V$	$\leq 15\%$ of lifetime
$1.125\ V < V_{DD} \leq 1.175\ V$	$\leq 5\%$ of lifetime

### 3.5 5 V / 3.3 V 可切换焊盘

焊盘类别为慢速 GPIO 和快速 GPIO，支持汽车级 (AL) 或 TTL 级 (TTL) 操作。参数是为 AL 操作定义的，并在 TTL 操作中降低。

表 3-6  $\overline{\text{PORST}}$  焊盘

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
PORST pad Output current	$I_{\text{PORST CC}}$	13	-	-	mA	$V_{\text{EXT}} = 2.97\text{V}; V_{\text{PORST}} = 0.9\text{V}$
Spike filter always blocked pulse duration	$t_{\text{SF1 CC}}$	-	-	80	ns	
Spike filter pass-through blocked pulse duration	$t_{\text{SF2 CC}}$	260	-	-	ns	without additional PORST Digital Filter active (PORSTDF = 0).
Input hysteresis <sup>1)</sup>	$HYS \text{ CC}$	$0.055 * V_{\text{EXT}}$	-	-	V	non of the neighbor pads are used as output;TTL (degraded, used for CIF)
Pull-down current <sup>2)</sup>	$I_{\text{PDL CC}}$	-	-	130	$\mu\text{A}$	$V_{\text{IH}}$ ; TTL (degraded, used for CIF)
		15	-	-	$\mu\text{A}$	$V_{\text{IL}}$ ; TTL (degraded, used for CIF)
Input leakage current	$I_{\text{OZ CC}}$	-450	-	450	nA	$T_{\text{J}} \leq 150^{\circ}\text{C}; (0.1 * V_{\text{EXT}}) < V_{\text{IN}} < (0.9 * V_{\text{EXT}})$
		-500	-	500	nA	$T_{\text{J}} \leq 150^{\circ}\text{C}; \text{else}$
		-900	-	900	nA	$T_{\text{J}} \leq 170^{\circ}\text{C}; (0.1 * V_{\text{EXT}}) < V_{\text{IN}} < (0.9 * V_{\text{EXT}})$
		-950	-	950	nA	$T_{\text{J}} \leq 170^{\circ}\text{C}; \text{else}$
Input high voltage level	$V_{\text{IH SR}}$	1.4	-	-	V	TTL (degraded, used for CIF); $V_{\text{EXT}} = 2.97\text{V}$
		2.0	-	-	V	TTL; $V_{\text{EXT}} = 4.5\text{V}$
Input low voltage level	$V_{\text{IL SR}}$	-	-	0.5	V	TTL (degraded, used for CIF); $V_{\text{EXT}} = 2.97\text{V}$
		-	-	0.8	V	TTL; $V_{\text{EXT}} = 4.5\text{V}$
Pin capacitance	$C_{\text{I0 CC}}$	-	2	3	pF	in addition 2.5pF from package to be added

1) 实施滞后是为了避免亚稳态和由于内部地弹而引起的切换。不能保证它能抑制由于外部系统噪声而引起的切换。

2) 下拉电阻的值通过表 VADC 5V 中的参数  $R_{\text{MDD}}$  定义。

**表 3-7 快速 5V GPIO**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	$R_{\text{DS(on) CC}}$	125	225	320	Ohm	medium driver; $I_{\text{OH/OL}} = 2\text{mA}$
		31	55	80	Ohm	strong driver; $I_{\text{OH/OL}} = 8\text{mA}$
Rise / Fall time <sup>1)2)</sup>	$t_{\text{RF CC}}$	1.6	-	3.2	ns	$C_L = 25\text{pF}$ ; driver = strong sharp edge; from $0.2 * V_{\text{EXT/FLEX/EVRSB}}$ to $0.8 * V_{\text{EXT/FLEX/EVRSB}}$
		$4+0.55 * C_L$	$4+0.75 * C_L$	$12+1.0 * C_L$	ns	driver = medium; $C_L \leq 200\text{pF}$
		$1.0+0.18 * C_L$	$2.5+0.27 * C_L$	$5.0+0.35 * C_L$	ns	driver = strong edge = medium; $C_L \leq 200\text{pF}$
		$0.5+0.08 * C_L$	$0.5+0.11 * C_L$	$1.0+0.17 * C_L$	ns	driver = strong edge = sharp; $C_L \leq 200\text{pF}$
Asymmetry of sending	$t_{\text{TX\_ASYM CC}}$	-1	-	1	ns	valid for all data rates excluding clock tolerance
Input frequency	$f_{\text{IN CC}}$	-	-	160	MHz	
Input hysteresis <sup>3)</sup>	$HYS \text{ CC}$	$0.09 * V_{\text{EXT/FLEX/EVRSB}}$	-	-	V	non of the neighbor pads are used as output; AL
		$0.075 * V_{\text{EXT/FLEX/EVRSB}}$	-	-	V	non of the neighbor pads are used as output; TTL
		75	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current <sup>4)</sup>	$I_{\text{PUH CC}}$	30	-	-	$\mu\text{A}$	$V_{\text{IH}}$ ; AL or TTL
		-	-	130	$\mu\text{A}$	$V_{\text{IL}}$ ; AL or TTL
Pull-down current <sup>5)</sup>	$I_{\text{PDL CC}}$	-	-	130	$\mu\text{A}$	$V_{\text{IH}}$ ; AL or TTL
		30	-	-	$\mu\text{A}$	$V_{\text{IL}}$ ; AL
		28	-	-	$\mu\text{A}$	$V_{\text{IL}}$ ; TTL

表 3-7 快速 5V GPIO (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current	$I_{OZ\ CC}$	-1100	-	1100	nA	$T_J \leq 150^\circ\text{C}$ ; $(0.1 \cdot V_{EXT/FLEX/EVRSB}) < V_{IN} < (0.9 \cdot V_{EXT/FLEX/EVRSB})$
		-2500	-	2500	nA	$T_J \leq 150^\circ\text{C}$ ; $(0.1 \cdot V_{EXT/FLEX}) < V_{IN} < (0.9 \cdot V_{EXT/FLEX})$ ; LVDS_TX / Fast pad type
		-6000	-	6000	nA	$T_J \leq 150^\circ\text{C}$ ; LVDS_RX / Fast pad type; else
		-3200	-	3200	nA	$T_J \leq 150^\circ\text{C}$ ; LVDS_TX / Fast pad type; else
		-1500	-	1500	nA	$T_J \leq 150^\circ\text{C}$ ; else
		-2000	-	2000	nA	$T_J \leq 170^\circ\text{C}$ ; $(0.1 \cdot V_{EXT/FLEX/EVRSB}) < V_{IN} < (0.9 \cdot V_{EXT/FLEX/EVRSB})$
		-4000	-	4000	nA	$T_J \leq 170^\circ\text{C}$ ; $(0.1 \cdot V_{EXT/FLEX}) < V_{IN} < (0.9 \cdot V_{EXT/FLEX})$ ; LVDS_TX / Fast pad type
		-13500	-	13500	nA	$T_J \leq 170^\circ\text{C}$ ; LVDS_RX / Fast pad type; else
		-5100	-	5100	nA	$T_J \leq 170^\circ\text{C}$ ; LVDS_TX / Fast pad type; else
Input high voltage level	$V_{IH\ SR}$	$0.7 \cdot V_{EXT/FLEX/EVRSB}$	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	$V_{IL\ SR}$	-	-	$0.44 \cdot V_{EXT/FLEX/EVRSB}$	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	$V_{ILD\ SR}$	-50	-	50	mV	max. variation of 1ms; $V_{EXT/FLEX/EVRSB} = \text{constant}$ ; AL
Pin capacitance	$C_{IO\ CC}$	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	$t_{SET\ CC}$	-	-	100	ns	

1) 在公式中，需要以 pF 为单位输入  $C_L$  的值才能获得 ns 为单位的結果。

2) 上升/下降时间定义为焊盘供电电压的 10% - 90%。

- 3) 实施滞后是为了避免亚稳态和由于内部地弹而引起的切换。不能保证它能抑制由于外部系统噪声而引起的切换。
- 4) 上拉电阻的值通过表 VADC 5V 中的参数  $R_{MDU}$  定义。
- 5) 下拉电阻的值通过表 VADC 5V 中的参数  $R_{MDD}$  定义。

**表 3-8 快速 3.3V GPIO**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	$R_{DSON\ CC}$	125	225	320	Ohm	medium driver; $I_{OH/OL} = 2mA$
		31	55	80	Ohm	strong driver; $I_{OH/OL} = 8mA$
Rise / Fall time <sup>1)2)</sup>	$t_{RF\ CC}$	1.6	-	4.5	ns	$C_L = 25pF$ ; driver = strong sharp edge; from $0.2 * V_{EXT/FLEX/EVRSB}$ to $0.8 * V_{EXT/FLEX/EVRSB}$
		-	-	5	ns	$C_L = 25pF$ ; driver = strong sharp edge; from 0.8V to 2.0V (RMII)
		$2+0.57 * C_L$	$5.5+0.75 * C_L$	$10+1.25 * C_L$	ns	driver = medium; $C_L \leq 200pF$
		$1.5+0.18 * C_L$	$1.5+0.28 * C_L$	$8+0.4 * C_L$	ns	driver = strong edge = medium; $C_L \leq 200pF$
		$0.75+0.08 * C_L$	$0.75+0.11 * C_L$	$2.5+0.21 * C_L$	ns	driver = strong edge = sharp; $C_L \leq 200pF$
Asymmetry of sending	$t_{TX\_ASYM\ CC}$	-1	-	1	ns	valid for all data rates excluding clock tolerance
Input frequency	$f_{IN\ CC}$	-	-	160	MHz	
Input hysteresis <sup>3)</sup>	$HYS\ CC$	$0.055 * V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; AL
		$0.09 * V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; TTL
		$0.055 * V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output;TTL (degraded, used for CIF)
		125	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL

表 3-8 快速 3.3V GPIO (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pull-up current <sup>4)</sup>	$I_{PUH\ CC}$	17	-	-	$\mu\text{A}$	$V_{IH}$ ; AL and TTL (degraded, used for CIF)
		11	-	-	$\mu\text{A}$	$V_{IH}$ ; TTL
		-	-	80	$\mu\text{A}$	$V_{IL}$ ; AL and TTL and TTL (degraded, used for CIF)
Pull-down current <sup>5)</sup>	$I_{PDL\ CC}$	-	-	105	$\mu\text{A}$	$V_{IH}$ ; AL and TTL (degraded, used for CIF)
		-	-	115	$\mu\text{A}$	$V_{IH}$ ; TTL
		19	-	-	$\mu\text{A}$	$V_{IL}$ ; AL and TTL
		15	-	-	$\mu\text{A}$	$V_{IL}$ ; TTL (degraded, used for CIF)
Input leakage current	$I_{OZ\ CC}$	-1100	-	1100	nA	$T_J \leq 150^\circ\text{C}$ ; $(0.1 * V_{EXT/FLEX/EVRSB}) < V_{IN} < (0.9 * V_{EXT/FLEX/EVRSB})$
		-2500	-	2500	nA	$T_J \leq 150^\circ\text{C}$ ; $(0.1 * V_{EXT/FLEX}) < V_{IN} < (0.9 * V_{EXT/FLEX})$ ; LVDS_TX / Fast pad type
		-6000	-	6000	nA	$T_J \leq 150^\circ\text{C}$ ; LVDS_RX / Fast pad type; else
		-3200	-	3200	nA	$T_J \leq 150^\circ\text{C}$ ; LVDS_TX / Fast pad type; else
		-1500	-	1500	nA	$T_J \leq 150^\circ\text{C}$ ; else
		-2000	-	2000	nA	$T_J \leq 170^\circ\text{C}$ ; $(0.1 * V_{EXT/FLEX/EVRSB}) < V_{IN} < (0.9 * V_{EXT/FLEX/EVRSB})$
		-4000	-	4000	nA	$T_J \leq 170^\circ\text{C}$ ; $(0.1 * V_{EXT/FLEX}) < V_{IN} < (0.9 * V_{EXT/FLEX})$ ; LVDS_TX / Fast pad type
		-13500	-	13500	nA	$T_J \leq 170^\circ\text{C}$ ; LVDS_RX / Fast pad type; else
		-5100	-	5100	nA	$T_J \leq 170^\circ\text{C}$ ; LVDS_TX / Fast pad type; else
-2500	-	2500	nA	$T_J \leq 170^\circ\text{C}$ ; else		

表 3-8 快速 3.3V GPIO (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input high voltage level	$V_{IH\ SR}$	0.7 *	-	-	V	AL
		$V_{EXT/FLEX/E}$ VRSB	-	-	V	TTL
		2.0	-	-	V	TTL (degraded, used for CIF)
Input low voltage level	$V_{IL\ SR}$	1.4	-	-	V	TTL (degraded, used for CIF)
		-	-	0.42 *	V	AL
		-	-	$V_{EXT/FLEX/E}$ VRSB	V	TTL
Input low/high voltage level	$V_{ILH\ SR}$	-	-	0.8	V	TTL (degraded, used for CIF)
		-	-	0.5	V	TTL (degraded, used for CIF)
Input low/high voltage level	$V_{ILH\ SR}$	1.0	-	1.9	V	RGMII; no hysteresis available
Input low threshold variation	$V_{ILD\ SR}$	-33	-	33	mV	max. variation of 1ms; $V_{EXT/FLEX/EVRSB} =$ constant; AL
Pin capacitance	$C_{IO\ CC}$	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	$t_{SET\ CC}$	-	-	100	ns	

- 1) 在公式中，需要以 pF 为单位输入  $C_L$  的值才能获得 ns 为单位的結果。
- 2) 上升/下降时间定义为焊盘供电电压的 10% - 90%。
- 3) 实施滞后是为了避免亚稳态和由于内部地弹而引起的切换。不能保证它能抑制由于外部系统噪声而引起的切换。
- 4) 上拉电阻的值通过表 VADC 5V 中的参数  $R_{MDU}$  定义。
- 5) 下拉电阻的值通过表 VADC 5V 中的参数  $R_{MDD}$  定义。

表 3-9 慢速 5V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	$R_{DSON\ CC}$	125	225	320	Ohm	medium driver; $I_{OH/OL} = 2mA$
Rise / Fall time <sup>1) 2)</sup>	$t_{RF\ CC}$	$4+0.55*C_L$	$4+0.75*C_L$	$12+1*C_L$	ns	driver = medium edge = medium ; $C_L \leq 200pF$
		$1.5+0.25*C_L$	$2.5+0.40*C_L$	$7+0.55*C_L$	ns	driver = medium edge = sharp ; $C_L \leq 200pF$
Asymmetry of sending	$t_{TX\_ASYM\ CC}$	-1	-	1	ns	valid for all data rates excluding clock tolerance
Input frequency	$f_{IN\ CC}$	-	-	160	MHz	

表 3-9 慢速 5V GPIO (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input hysteresis <sup>3)</sup>	$HYS_{CC}$	0.09 *	-	-	V	non of the neighbor pads are used as output; AL
		$V_{EXT/FLEX/E}$ VRSB				
		0.075 *	-	-	V	non of the neighbor pads are used as output; TTL
		$V_{EXT/FLEX/E}$ VRSB				
		75	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current <sup>4)</sup>	$I_{PUH_{CC}}$	30	-	-	$\mu A$	$V_{IH}$ ; AL or TTL; except VGATE1P; except VGATE1N and $T_J > 150^\circ C$
		-	-	130	$\mu A$	$V_{IL}$ ; AL or TTL; except VGATE1P; except VGATE1N and $T_J > 150^\circ C$
Pull-down current <sup>5)</sup>	$I_{PDL_{CC}}$	-	-	130	$\mu A$	$V_{IH}$ ; AL or TTL
		30	-	-	$\mu A$	$V_{IL}$ ; AL
		28	-	-	$\mu A$	$V_{IL}$ ; TTL
Input leakage current	$I_{OZ_{CC}}$	-300	-	300	nA	$T_J \leq 150^\circ C$ ; $(0.1 * V_{EXT/FLEX/EVRSB}) < V_{IN} < (0.9 * V_{EXT/FLEX/EVRSB})$
		-400	-	400	nA	$T_J \leq 150^\circ C$ ; else
		-600	-	600	nA	$T_J \leq 170^\circ C$ ; $(0.1 * V_{EXT/FLEX/EVRSB}) < V_{IN} < (0.9 * V_{EXT/FLEX/EVRSB})$
		-750	-	750	nA	$T_J \leq 170^\circ C$ ; else
		-18000	-	18000	nA	P32.0 and P32.1; $T_J \leq 150^\circ C$
		-38000	-	38000	nA	P32.0 and P32.1; $T_J \leq 170^\circ C$
Input high voltage level	$V_{IH_{SR}}$	0.7 *	-	-	V	AL
		$V_{EXT/FLEX/E}$ VRSB				
		2.0	-	-	V	TTL
Input low voltage level	$V_{IL_{SR}}$	-	-	0.44 *	V	AL
				$V_{EXT/FLEX/E}$ VRSB		
		-	-	0.8	V	TTL

表 3-9 慢速 5V GPIO (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low threshold variation	$V_{ILD\ SR}$	-50	-	50	mV	max. variation of 1ms; $V_{EXT/FLEX/EVRSB} =$ constant; AL
Pin capacitance	$C_{IO\ CC}$	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	$t_{SET\ CC}$	-	-	100	ns	

- 1) 在公式中，需要以 pF 为单位输入  $C_L$  的值才能获得 ns 为单位的结果。
- 2) 上升/下降时间定义为焊盘供电电压的 10% - 90%。
- 3) 实施滞后是为了避免亚稳态和由于内部地弹而引起的切换。不能保证它能抑制由于外部系统噪声而引起的切换。
- 4) 上拉电阻的值通过表 VADC 5V 中的参数  $R_{MDU}$  定义。
- 5) 下拉电阻的值通过表 VADC 5V 中的参数  $R_{MDD}$  定义。

表 3-10 慢速 3.3V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	$R_{DSON\ CC}$	125	225	320	Ohm	medium driver; $I_{OH/OL} =$ 2mA
Rise / Fall time <sup>1)2)</sup>	$t_{RF\ CC}$	$2+0.57 \cdot C_L$	$5.5+0.75 \cdot C_L$	$10+1.25 \cdot C_L$	ns	driver = medium edge = medium; $C_L \leq 200\text{pF}$
		$2+0.30 \cdot C_L$	$3.5+0.50 \cdot C_L$	$5+0.70 \cdot C_L$	ns	driver = medium edge = sharp; $C_L \leq 200\text{pF}$
Asymmetry of sending	$t_{TX\_ASYM\ CC}$	-1	-	1	ns	valid for all data rates excluding clock tolerance
Input frequency	$f_{IN\ CC}$	-	-	160	MHz	
Input hysteresis <sup>3)</sup>	$HYS\ CC$	$0.055 \cdot V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; AL
		$0.09 \cdot V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; TTL
		$0.055 \cdot V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output;TTL (degraded, used for CIF)
		125	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL

表 3-10 慢速 3.3V GPIO (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pull-up current <sup>4)</sup>	$I_{PUH\ CC}$	17	-	-	$\mu A$	$V_{IH}$ ; AL and TTL (degraded, used for CIF); except VGATE1P; except VGATE1N and $T_J > 150^\circ C$
		11	-	-	$\mu A$	$V_{IH}$ ; TTL; except VGATE1P; except VGATE1N and $T_J > 150^\circ C$
		-	-	80	$\mu A$	$V_{IL}$ ; AL and TTL and TTL (degraded, used for CIF); except VGATE1P; except VGATE1N and $T_J > 150^\circ C$
Pull-down current <sup>5)</sup>	$I_{PDL\ CC}$	-	-	105	$\mu A$	$V_{IH}$ ; AL and TTL (degraded, used for CIF)
		-	-	115	$\mu A$	$V_{IH}$ ; TTL
		19	-	-	$\mu A$	$V_{IL}$ ; AL and TTL
		15	-	-	$\mu A$	$V_{IL}$ ; TTL (degraded, used for CIF)
Input leakage current	$I_{OZ\ CC}$	-300	-	300	nA	$T_J \leq 150^\circ C$ ; $(0.1 * V_{EXT/FLEX/EVRSB}) < V_{IN} < (0.9 * V_{EXT/FLEX/EVRSB})$
		-400	-	400	nA	$T_J \leq 150^\circ C$ ; else
		-600	-	600	nA	$T_J \leq 170^\circ C$ ; $(0.1 * V_{EXT/FLEX/EVRSB}) < V_{IN} < (0.9 * V_{EXT/FLEX/EVRSB})$
		-750	-	750	nA	$T_J \leq 170^\circ C$ ; else
		-18000	-	18000	nA	P32.0 and P32.1; $T_J \leq 150^\circ C$
		-38000	-	38000	nA	P32.0 and P32.1; $T_J \leq 170^\circ C$
Input high voltage level	$V_{IH\ SR}$	0.7 * $V_{EXT/FLEX/EVRSB}$	-	-	V	AL
		2.0	-	-	V	TTL
		1.4	-	-	V	TTL (degraded, used for CIF)

表 3-10 慢速 3.3V GPIO (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage level	$V_{IL\ SR}$	-	-	0.42 * $V_{EXT/FLEX/EVRSB}$	V	AL
		-	-	0.8	V	TTL
		-	-	0.5	V	TTL (degraded, used for CIF)
Input low/high voltage level	$V_{ILH\ SR}$	1.0	-	1.9	V	RGMII; no hysteresis available
Input low threshold variation	$V_{ILD\ SR}$	-33	-	33	mV	max. variation of 1ms; $V_{EXT/FLEX/EVRSB} =$ constant; AL
Pin capacitance	$C_{IO\ CC}$	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	$t_{SET\ CC}$	-	-	100	ns	

- 1) 在公式中，需要以 pF 为单位输入  $C_L$  的值才能获得 ns 为单位的结果。
- 2) 上升/下降时间定义为焊盘供电电压的 10% - 90%。
- 3) 实施滞后是为了避免亚稳态和由于内部地弹而引起的切换。不能保证它能抑制由于外部系统噪声而引起的切换。
- 4) 上拉电阻的值通过表 VADC 5V 中的参数  $R_{MDU}$  定义。
- 5) 下拉电阻的值通过表 VADC 5V 中的参数  $R_{MDD}$  定义。

表 3-11 RFast 5V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	$R_{DSON\ CC}$	125	225	320	Ohm	medium driver; $I_{OH/OL} = 2\text{mA}$
		31	55	80	Ohm	strong driver; $I_{OH/OL} = 8\text{mA}$
Rise / Fall time <sup>1)2)</sup>	$t_{RF\ CC}$	1.6	-	3.2	ns	$C_L = 25\text{pF}$ ; driver = strong sharp edge; from $0.2 * V_{FLEX}$ to $0.8 * V_{FLEX}$
		$4+0.55 * C_L$	$4+0.75 * C_L$	$12+1.0 * C_L$	ns	driver = medium; $C_L \leq 200\text{pF}$
		$1.0+0.18 * C_L$	$2.5+0.27 * C_L$	$5.0+0.35 * C_L$	ns	driver = strong edge = medium; $C_L \leq 200\text{pF}$
		$0.5+0.08 * C_L$	$0.5+0.11 * C_L$	$1.0+0.17 * C_L$	ns	driver = strong edge = sharp; $C_L \leq 200\text{pF}$
Asymmetry of sending	$t_{TX\_ASYM\ CC}$	-0.5	-	0.5	ns	valid for all data rates excluding clock tolerance

表 3-11 RFast 5V GPIO (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	$f_{IN}$ CC	-	-	160	MHz	
Input hysteresis <sup>3)</sup>	$HYS$ CC	0.09 * $V_{FLEX}$	-	-	V	non of the neighbor pads are used as output; AL
		0.075 * $V_{FLEX}$	-	-	V	non of the neighbor pads are used as output; TTL
		75	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current <sup>4)</sup>	$I_{PUH}$ CC	30	-	-	$\mu$ A	$V_{IH}$ ; AL or TTL
		-	-	130	$\mu$ A	$V_{IL}$ ; AL or TTL
Pull-down current <sup>5)</sup>	$I_{PDL}$ CC	-	-	130	$\mu$ A	$V_{IH}$ ; AL or TTL
		30	-	-	$\mu$ A	$V_{IL}$ ; AL
		28	-	-	$\mu$ A	$V_{IL}$ ; TTL
Input leakage current	$I_{OZ}$ CC	-1700	-	1700	nA	$T_J \leq 150^\circ\text{C}$ ; $(0.1 * V_{FLEX}) < V_{IN} < (0.9 * V_{FLEX})$
		-2100	-	2100	nA	$T_J \leq 150^\circ\text{C}$ ; else
		-3000	-	3000	nA	$T_J \leq 170^\circ\text{C}$ ; $(0.1 * V_{FLEX}) < V_{IN} < (0.9 * V_{FLEX})$
		-4000	-	4000	nA	$T_J \leq 170^\circ\text{C}$ ; else
Input high voltage level	$V_{IH}$ SR	$0.7 * V_{FLEX}$	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	$V_{IL}$ SR	-	-	$0.44 * V_{FLEX}$	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	$V_{ILD}$ SR	-50	-	50	mV	max. variation of 1ms; $V_{FLEX} = \text{constant}$ ; AL
Pin capacitance	$C_{IO}$ CC	-	2	3.5	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	$t_{SET}$ CC	-	-	100	ns	

1) 在公式中，需要以 pF 为单位输入  $C_L$  的值才能获得 ns 为单位的的结果。

2) 上升/下降时间定义为焊盘供电电压的 10% - 90%。

3) 实施滞后是为了避免亚稳态和由于内部地弹而引起的切换。不能保证它能抑制由于外部系统噪声而引起的切换。

4) 上拉电阻的值通过表 VADC 5V 中的参数  $R_{MDU}$  定义。

5) 下拉电阻的值通过表 VADC 5V 中的参数  $R_{MDD}$  定义。

**表 3-12 RFast 3.3V 焊盘**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	$R_{DS(ON)CC}$	8	20	30	Ohm	Driver = RGMII; $I_{OH/OL} = 8mA$
		125	225	320	Ohm	medium driver; $I_{OH/OL} = 2mA$
		31	55	80	Ohm	strong driver; $I_{OH/OL} = 8mA$
Input Duty Cycle	$f_D SR$	47.5	50	52.5		
Rise / Fall time <sup>1)2)</sup>	$t_{RFCC}$	1.6	-	4.5	ns	$C_L = 25pF$ ; driver = strong sharp edge; from $0.2 * V_{FLEX}$ to $0.8 * V_{FLEX}$
		-	-	5	ns	$C_L = 25pF$ ; driver = strong sharp edge; from 0.8V to 2.0V (RMII)
		-	-	1	ns	Driver = RGMII; from 20%V to 80%V; $C_L = 15pF$
		$2+0.57 * C_L$	$5.5+0.75 * C_L$	$10+1.25 * C_L$	ns	driver = medium; $C_L \leq 200pF$
		$1.5+0.18 * C_L$	$1.5+0.28 * C_L$	$8+0.4 * C_L$	ns	driver = strong edge = medium; $C_L \leq 200pF$
		$0.75+0.08 * C_L$	$0.75+0.11 * C_L$	$2.5+0.21 * C_L$	ns	driver = strong edge = sharp; $C_L \leq 200pF$
Asymmetry of sending	$t_{TX\_ASYMCC}$	-0.4	-	0.4	ns	valid for all data rates excluding clock tolerance
Input frequency	$f_{INCC}$	-	-	160	MHz	

**表 3-12 RFast 3.3V 焊盘 (续)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input hysteresis <sup>3)</sup>	$HYS_{CC}$	0.055 * $V_{FLEX}$	-	-	V	non of the neighbor pads are used as output; AL
		0.09 * $V_{FLEX}$	-	-	V	non of the neighbor pads are used as output; TTL
		0.055 * $V_{FLEX}$	-	-	V	non of the neighbor pads are used as output;TTL (degraded, used for CIF)
		125	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current <sup>4)</sup>	$I_{PUH_{CC}}$	17	-	-	$\mu A$	$V_{IH}$ ; AL and TTL (degraded, used for CIF)
		11	-	-	$\mu A$	$V_{IH}$ ; TTL
		-	-	80	$\mu A$	$V_{IL}$ ; AL and TTL and TTL (degraded, used for CIF)
Pull-down current <sup>5)</sup>	$I_{PDL_{CC}}$	-	-	105	$\mu A$	$V_{IH}$ ; AL and TTL (degraded, used for CIF)
		-	-	115	$\mu A$	$V_{IH}$ ; TTL
		19	-	-	$\mu A$	$V_{IL}$ ; AL and TTL
		15	-	-	$\mu A$	$V_{IL}$ ; TTL (degraded, used for CIF)
Input leakage current	$I_{OZ_{CC}}$	-1700	-	1700	nA	$T_J \leq 150^\circ C$ ; (0.1 * $V_{FLEX}$ ) < $V_{IN}$ < (0.9 * $V_{FLEX}$ )
		-2100	-	2100	nA	$T_J \leq 150^\circ C$ ; else
		-3000	-	3000	nA	$T_J \leq 170^\circ C$ ; (0.1 * $V_{FLEX}$ ) < $V_{IN}$ < (0.9 * $V_{FLEX}$ )
		-4000	-	4000	nA	$T_J \leq 170^\circ C$ ; else
Input high voltage level	$V_{IH_{SR}}$	0.7 * $V_{FLEX}$	-	-	V	AL
		2.0	-	-	V	TTL
		1.4	-	-	V	TTL (degraded, used for CIF)

表 3-12 RFast 3.3V 焊盘 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage level	$V_{IL\ SR}$	-	-	0.42 * $V_{FLEX}$	V	AL
		-	-	0.8	V	TTL
		-	-	0.5	V	TTL (degraded, used for CIF)
Input low threshold variation	$V_{ILD\ SR}$	-33	-	33	mV	max. variation of 1ms; $V_{FLEX} = \text{constant}$ ; AL
Pin capacitance	$C_{IO\ CC}$	-	2	3.5	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	$t_{SET\ CC}$	-	-	100	ns	

- 1) 在公式中，需要以 pF 为单位输入  $C_L$  的值才能获得 ns 为单位的結果。
- 2) 上升/下降时间定义为焊盘供电电压的 10% - 90%。
- 3) 实施滞后是为了避免亚稳态和由于内部地弹而引起的切换。不能保证它能抑制由于外部系统噪声而引起的切换。
- 4) 上拉电阻的值通过表 VADC 5V 中的参数  $R_{MDU}$  定义。
- 5) 下拉电阻的值通过表 VADC 5V 中的参数  $R_{MDD}$  定义。

表 3-13 S 类 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	$f_{IN\ CC}$	-	-	160	MHz	
Input hysteresis <sup>1)</sup>	$HYS\ CC$	0.09 * $V_{DDM}$	-	-	V	non of the neighbor pads are used as output; AL
		0.075 * $V_{DDM}$	-	-	V	non of the neighbor pads are used as output; TTL
		75	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current <sup>2)</sup>	$I_{PUH\ CC}$	30	-	-	$\mu A$	$V_{IH}$ ; AL or TTL
		-	-	130	$\mu A$	$V_{IL}$ ; AL or TTL
Pull-down current <sup>3)</sup>	$I_{PDL\ CC}$	-	-	130	$\mu A$	$V_{IH}$ ; AL or TTL
		30	-	-	$\mu A$	$V_{IL}$ ; AL
		28	-	-	$\mu A$	$V_{IL}$ ; TTL

表 3-13 S 类 5V (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current	$I_{OZ\ CC}$	-150	-	150	nA	$T_J \leq 150^\circ\text{C}$ ; else
		-300	-	300	nA	$T_J \leq 150^\circ\text{C}$ ; PDD option available, or AltRef option available and EDSADC channel connected, or two EDSADC channels connected
		-300	-	300	nA	$T_J \leq 170^\circ\text{C}$ ; else
		-600	-	600	nA	$T_J \leq 170^\circ\text{C}$ ; PDD option available, or AltRef option available and EDSADC channel connected, or two EDSADC channels connected
Input high voltage level	$V_{IH\ SR}$	$0.7 * V_{DDM}$	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	$V_{IL\ SR}$	-	-	$0.44 * V_{DDM}$	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	$V_{ILD\ SR}$	-50	-	50	mV	max. variation of 1ms; $V_{DDM} = \text{constant}$ ; AL
Pin capacitance	$C_{IO\ CC}$	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	$t_{SET\ CC}$	-	-	100	ns	

- 1) 实施滞后是为了避免亚稳态和由于内部地弹而引起的切换。不能保证它能抑制由于外部系统噪声而引起的切换。
- 2) 上拉电阻的值通过表 VADC 5V 中的参数  $R_{MDU}$  定义。
- 3) 下拉电阻的值通过表 VADC 5V 中的参数  $R_{MDD}$  定义。

表 3-14 S 类 3.3V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	$f_{IN\ CC}$	-	-	160	MHz	

表 3-14 S 类 3.3V (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input hysteresis <sup>1)</sup>	$HYS_{CC}$	0.055 * $V_{DDM}$	-	-	V	non of the neighbor pads are used as output; AL
		0.09 * $V_{DDM}$	-	-	V	non of the neighbor pads are used as output; TTL
		0.065 * $V_{DDM}$	-	-	V	non of the neighbor pads are used as output; TTL (degraded used for CIF)
		125	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current <sup>2)</sup>	$I_{PUH_{CC}}$	17	-	-	$\mu A$	$V_{IH}$ ; AL and TTL (degraded, used for CIF)
		11	-	-	$\mu A$	$V_{IH}$ ; TTL
		-	-	80	$\mu A$	$V_{IL}$
Pull-down current <sup>3)</sup>	$I_{PDL_{CC}}$	-	-	105	$\mu A$	$V_{IH}$ ; AL and TTL (degraded, used for CIF)
		-	-	115	$\mu A$	$V_{IH}$ ; TTL
		19	-	-	$\mu A$	$V_{IL}$ ; AL and TTL
		15	-	-	$\mu A$	$V_{IL}$ ; TTL (degraded, used for CIF)
Input leakage current	$I_{OZ_{CC}}$	-150	-	150	nA	$T_J \leq 150^\circ C$ ; else
		-300	-	300	nA	$T_J \leq 150^\circ C$ ; PDD option available, or AltRef option available and EDSADC channel connected
		-300	-	300	nA	$T_J \leq 170^\circ C$ ; else
		-600	-	600	nA	$T_J \leq 170^\circ C$ ; PDD option available
Input high voltage level	$V_{IH_{SR}}$	0.7 * $V_{DDM}$	-	-	V	AL
		2.0	-	-	V	TTL
		1.4	-	-	V	TTL (degraded, used for CIF)

表 3-14 S 类 3.3V (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage level	$V_{IL\ SR}$	-	-	0.42 * $V_{DDM}$	V	AL
		-	-	0.8	V	TTL
		-	-	0.5	V	TTL (degraded, used for CIF)
Input low threshold variation	$V_{ILD\ SR}$	-33	-	33	mV	max. variation of 1ms; $V_{DDM} = \text{constant}$ ; AL
Pin capacitance	$C_{IO\ CC}$	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	$t_{SET\ CC}$	-	-	100	ns	

- 1) 实施滞后是为了避免亚稳态和由于内部地弹而引起的切换。不能保证它能抑制由于外部系统噪声而引起的切换。
- 2) 上拉电阻的值通过表 VADC 5V 中的参数  $R_{MDU}$  定义。
- 3) 下拉电阻的值通过表 VADC 5V 中的参数  $R_{MDD}$  定义。

表 3-15 D 类

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current	$I_{OZ\ CC}$	-150	-	150	nA	$T_J \leq 150^\circ\text{C}$ ; else
		-300 <sup>1)</sup>	-	300 <sup>1)</sup>	nA	$T_J \leq 150^\circ\text{C}$ ; PDD option available, or AltRef option available and EDSADC channel connected, or two EDSADC channels connected
		-300	-	300	nA	$T_J \leq 170^\circ\text{C}$ ; else
		-600 <sup>2)</sup>	-	600 <sup>2)</sup>	nA	$T_J \leq 170^\circ\text{C}$ ; PDD option available, or AltRef option available and EDSADC channel connected, or two EDSADC channels connected
Pin capacitance	$C_{IO\ CC}$	-	2	3	pF	in addition 2.5pF from package to be added

- 1) 对于 AN11, 需要添加 100 nA。
- 2) 对于 AN11, 需要添加 200 nA。

表 3-16 ADC基准焊盘

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current for $V_{AREF}$	$I_{OZZ\ CC}$	-2 <sup>1)</sup>	-	2 <sup>1)</sup>	$\mu\text{A}$	$T_J \leq 150^\circ\text{C}$ ; $V_{AREF} < V_{DDM}$ ; for EVADC; valid for BGA292 and BGA292 ADAS feature set
		-7 <sup>1)</sup>	-	7 <sup>1)</sup>	$\mu\text{A}$	$T_J \leq 150^\circ\text{C}$ ; $V_{AREF} \leq V_{DDM} + 50\text{mV}$ ; for EVADC; valid for BGA292 and BGA292 ADAS feature set
		-4 <sup>1)</sup>	-	4 <sup>1)</sup>	$\mu\text{A}$	$T_J \leq 170^\circ\text{C}$ ; $V_{AREF} < V_{DDM}$ ; for EVADC; valid for BGA292 and BGA292 ADAS feature set
		-14 <sup>1)</sup>	-	14 <sup>1)</sup>	$\mu\text{A}$	$T_J \leq 170^\circ\text{C}$ ; $V_{AREF} \leq V_{DDM} + 50\text{mV}$ ; for EVADC; valid for BGA292 and BGA292 ADAS feature set
		-1 <sup>2)</sup>	-	1 <sup>2)</sup>	$\mu\text{A}$	$T_J \leq 150^\circ\text{C}$ ; $V_{AREF} < V_{DDM}$ ; for EVADC; valid for BGA516
		-2 <sup>2)</sup>	-	2 <sup>2)</sup>	$\mu\text{A}$	$T_J \leq 170^\circ\text{C}$ ; $V_{AREF} < V_{DDM}$ ; for EVADC; valid for BGA516
		-3.5 <sup>2)</sup>	-	3.5 <sup>2)</sup>	$\mu\text{A}$	$T_J \leq 150^\circ\text{C}$ ; $V_{AREF} \leq V_{DDM} + 50\text{mV}$ ; for EVADC; valid for BGA516
		-7 <sup>2)</sup>	-	7 <sup>2)</sup>	$\mu\text{A}$	$T_J \leq 170^\circ\text{C}$ ; $V_{AREF} \leq V_{DDM} + 50\text{mV}$ ; for EVADC; valid for BGA516
		-2 <sup>3)</sup>	-	2 <sup>3)</sup>	$\mu\text{A}$	$T_J \leq 150^\circ\text{C}$ ; $V_{AREF} < V_{DDM}$ ; for EDSADC
		-4 <sup>3)</sup>	-	4 <sup>3)</sup>	$\mu\text{A}$	$T_J \leq 170^\circ\text{C}$ ; $V_{AREF} < V_{DDM}$ ; for EDSADC
		-6 <sup>3)</sup>	-	6 <sup>3)</sup>	$\mu\text{A}$	$T_J \leq 150^\circ\text{C}$ ; $V_{AREF} \leq V_{DDM} + 50\text{mV}$ ; for EDSADC
		-12 <sup>3)</sup>	-	12 <sup>3)</sup>	$\mu\text{A}$	$T_J \leq 170^\circ\text{C}$ ; $V_{AREF} \leq V_{DDM} + 50\text{mV}$ ; for EDSADC

- 1) 限制对 VAREF2 引脚有效。
- 2) 限制对 VAREF2 和 VAREF3 引脚均有效。
- 3) 限制对 VAREF1 引脚有效。

表 3-17 慢速 Pad 的驱动器模式选择

PDx.2	PDx.1	PDx.0	Port Functionality	Driver Setting
X	X	0	Speed grade 1	medium sharp edge (sm)
X	X	1	Speed grade 2	medium medium edge (m)

表 3-18 Fast Pad 驱动器模式选择

PDx.2	PDx.1	PDx.0	Port Functionality	Driver Setting
X	0	0	Speed grade 1	Strong sharp edge (ss)
X	0	1	Speed grade 2	Strong medium edge (sm)
X	1	0	Speed grade 3	medium (m)
X	1	1	Speed grade 4	Reserved, do not use this combination

表 3-19 RFast Pad 驱动器模式选择

PDx.2	PDx.1	PDx.0	Port Functionality	Driver Setting
X	0	0	Speed grade 1	Strong sharp edge (ss)
X	0	1	Speed grade 2	Strong medium edge (sm)
X	1	0	Speed grade 3	medium (m)
X	1	1	Speed grade 4	RGMII function is active

### 3.6 高性能 LVDS 焊盘

该 LVDS 焊盘类型用于新型 TC39x 的高速芯片到芯片通信接口。它由一个 LVDS 焊盘和一个快速焊盘组成。

对于所有 LVDS 参数， $C_L = 2.5 \text{ pF}$ 。

**表 3-20 LVDS - IEEE 标准 LVDS 通用链路 (GPL)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output impedance	$R_{0 \text{ CC}}$	40	-	140	Ohm	$V_{\text{cm}} = 1.0 \text{ V}$ and $1.4 \text{ V}$
Rise time (20% - 80%)	$t_{\text{rise}20 \text{ CC}}$	-	-	$0.75^1$	ns	$Z_L = 100 \text{ Ohm} \pm 20\%$ @2pF external load
Fall time (20% - 80%)	$t_{\text{fall}20 \text{ CC}}$	-	-	$0.75^2$	ns	$Z_L = 100 \text{ Ohm} \pm 20\%$ @2pF external load
Output differential voltage <sup>3)</sup>	$V_{\text{OD} \text{ CC}}$	240	-	330	mV	$R_T = 100 \text{ Ohm} \pm 1\%$ ; LPCRx.VDIFFADJ=00
		280	-	370	mV	$R_T = 100 \text{ Ohm} \pm 1\%$ ; LPCRx.VDIFFADJ=01
		320	-	410	mV	$R_T = 100 \text{ Ohm} \pm 1\%$ ; LPCRx.VDIFFADJ=10
		380	-	500	mV	$R_T = 100 \text{ Ohm} \pm 1\%$ ; LPCRx.VDIFFADJ=11; Multi slave operation
Output voltage high	$V_{\text{OH} \text{ CC}}$	-	-	1475	mV	$R_T = 100 \text{ Ohm} \pm 1\%$ VDIFFADJ=00 and 01
		-	-	1500	mV	$R_T = 100 \text{ Ohm} \pm 1\%$ VDIFFADJ=10 and 11
Output voltage low	$V_{\text{OL} \text{ CC}}$	925	-	-	mV	$R_T = 100 \text{ Ohm} \pm 1\%$ VDIFFADJ=00 and 01
		900	-	-	mV	$R_T = 100 \text{ Ohm} \pm 1\%$ VDIFFADJ=10 and 11
Output offset (Common mode) voltage	$V_{\text{OS} \text{ CC}}$	1125	-	1275	mV	$R_T = 100 \text{ Ohm} \pm 1\%$
Input voltage range	$V_{\text{I} \text{ SR}}$	0	-	1600	mV	Driver ground potential difference < 925 mV; $R_T = 100 \text{ Ohm} \pm 10\%$
		0	-	2400	mV	Driver ground potential difference < 925 mV; $R_T = 100 \text{ Ohm} \pm 20\%$
Input differential threshold	$V_{\text{idth} \text{ SR}}$	-100	-	100	mV	Driver ground potential difference < 900 mV; VDIFFADJ=10 and 11
		-100	-	100	mV	Driver ground potential difference < 925 mV; VDIFFADJ=00 and 01

表 3-20 LVDS - IEEE 标准 LVDS 通用链路 (GPL) (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Receiver differential input impedance	$R_{in} CC$	80	-	120	Ohm	$V_i \leq 2400 \text{ mV}$
Output differential voltage Sleep Mode <sup>4)</sup>	$V_{ODSM} CC$	-5	-	20	mV	$R_T = 100 \text{ Ohm} \pm 20\%$ ; LPCRx.VDIFFADJ=xx
Delta output impedance	$dR0 SR$	-	-	10	%	$V_{cm} = 1.0 \text{ V and } 1.4 \text{ V}$
Change in VOS between 0 and 1	$dVOS CC$	-	-	25	mV	$R_T = 100 \text{ Ohm} \pm 1\%$
Change in Vod between 0 and 1	$dVod CC$	-	-	25	mV	$R_T = 100 \text{ Ohm} \pm 1\%$
Pad set-up time	$t_{SET\_LVDS} CC$	-	10	13	$\mu\text{s}$	
Duty cycle	$t_{duty} CC$	45	-	55	%	

1)  $t_{rise20} = 0.75\text{ns} + (C_L - 2)[\text{pF}] * 20\text{ps}$ ,  $C_L$  定义外部负载。

2)  $t_{fall20} = 0.75\text{ns} + (C_L - 2)[\text{pF}] * 20\text{ps}$ ,  $C_L$  定义外部负载。

3) 潜在的对IEEE 标准 1596.3 的违反是为了新的多从站支持的特点, 符合 IEEE 标准 1596.3LPCRx.VDIFFADJ 必须配置为 01。

4) Tx的共模电压得以维持。

注释: 驱动器接地电位的差异定义为驱动器-接收器电位差, 在比较驱动器输出电压电平和接收器输入传输信号的电压电平时, 可能会导致电压偏移。

注释: "LVDS - IEEE 标准 LVDS 通用链路 (GPL)" 表中的  $R_T$  IEEE 标准 1596.3-1996 图3-5 中接收器的终端电阻在图3-1 中以  $R_{in}$  或以  $R_T=100\text{Ohm}$  表示, 但不能同时表示. 如果"注释/测试条件"栏中提到了  $R_T$ , 则总是选择图3-1 中的内部电阻  $R_{in}$ 。

启动后默认=CMOS功能

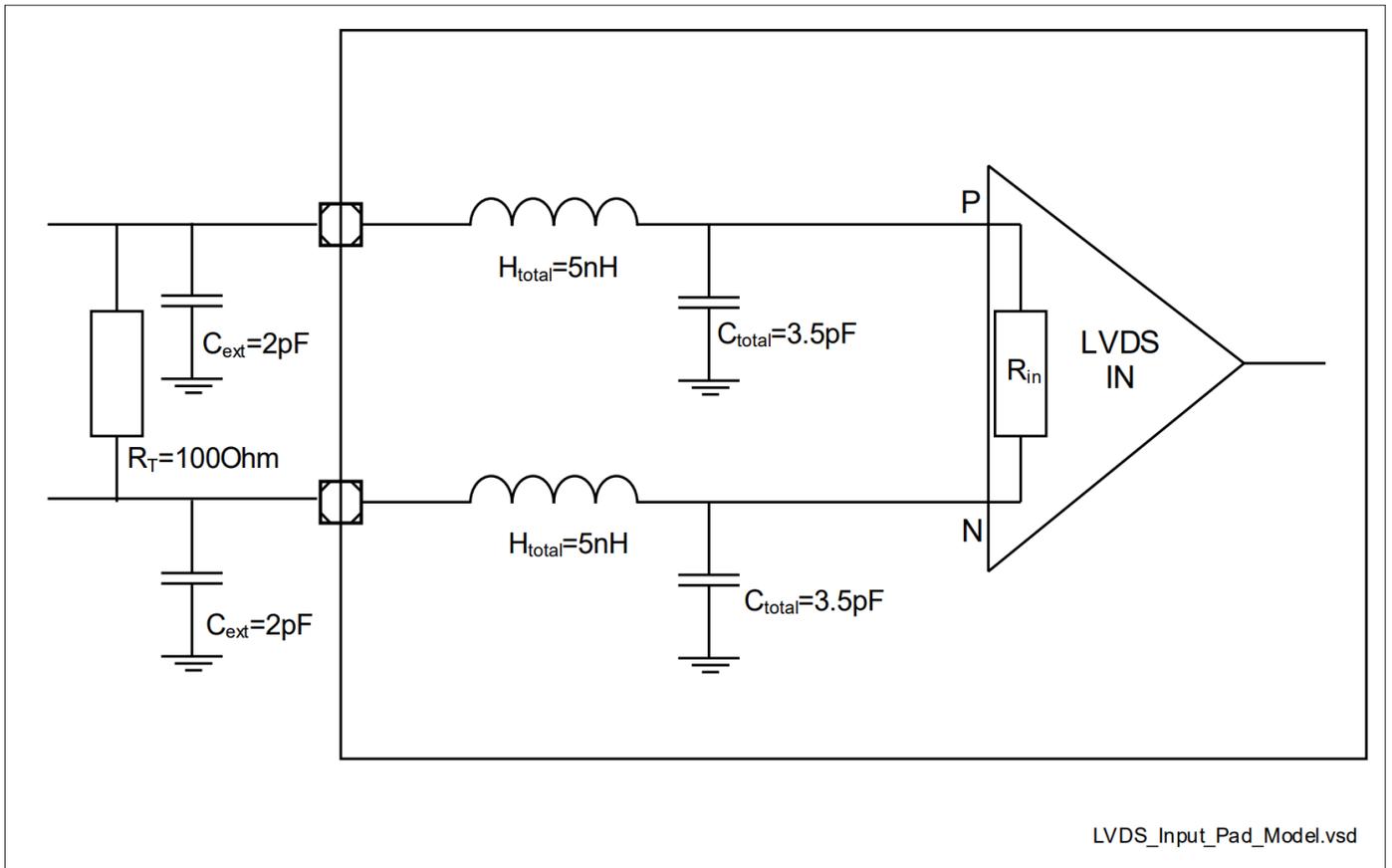


图 3-1 LVDS 焊盘输入模型

### 3.7 VADC 参数

转换器结果的准确性取决于基准电压范围。下表中的参数适用于 ( $V_{\text{AREF}} - V_{\text{AGND}}$ )  $\geq 4.5$  V 的基准电压范围。如果基准电压范围低于 4.5 V k 倍 (例如 3.3 V)，则精度参数将增加 1.1/k 倍 (例如  $1.1 \times 4.5 / 3.3 = 1.5$ )。

供电电压  $V_{\text{DDM}}$  上的噪声会影响转换。精度 (误差) 参数定义为供电电压纹波在 10 MHz 以内低于 20 mVpp (在 10 MHz 以上低于 5 mVpp)。

数字功能与模拟输入重叠会影响准确性。

总不可调整误差 (TUE) 的定义是无噪音的。总体偏差取决于 TUE 和  $EN_{\text{RMS}}$  (取决于噪声分布)。示例: 对于 4 sigma 的噪声分布且  $EN_{\text{RMS}} = 1.0$ , 附加峰峰值噪声误差为  $\pm(4 \times 1.0) = 8 \text{ LSB}_{12\text{o}}$

快速比较操作以 10 位值执行。

降噪功能通过增加额外的转换步骤来改善结果。因此, 转换时间也相应增加 (对于 1、3 或 7 个步骤, 每个步骤的转换时间分别为  $4 \times t_{\text{ADCI}} + 3 \times t_{\text{ADC}}$ )。

表 3-21 VADC 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
EVADC IVR output voltage	$V_{\text{DDK CC}}$	1.15	-	1.35	V	Measured at low temperature.
Deviation of IVR output voltage $V_{\text{DDK}}$	$dV_{\text{DDK CC}}$	-2	-	2	%	Based on device-specific value
Analog reference voltage <sup>1)</sup>	$V_{\text{AREF SR}}$	4.5	5.0	$V_{\text{DDM}} + 0.05$	V	$4.5 \text{ V} \leq V_{\text{DDM}} \leq 5.5 \text{ V}$
		2.97	3.3	$V_{\text{DDM}} + 0.05$	V	$2.97 \text{ V} \leq V_{\text{DDM}} < 4.5 \text{ V}$
Analog reference ground	$V_{\text{AGND SR}}$	$V_{\text{SSM}}$	$V_{\text{SSM}}$	$V_{\text{SSM}}$	V	$V_{\text{SSM}}$ and $V_{\text{AGND}}$ are connected together
Analog input voltage range	$V_{\text{AIN SR}}$	$V_{\text{AGND}}$	-	$V_{\text{AREF}}$	V	$V_{\text{AIN}}$ is limited by the respective pad supply voltage; see pin configuration (buffer type)
Converter reference clock	$f_{\text{ADCI SR}}$	16	40	53.33	MHz	$4.5 \text{ V} \leq V_{\text{DDM}} \leq 5.5 \text{ V}$
		16	20	26.67	MHz	$2.97 \text{ V} \leq V_{\text{DDM}} < 4.5 \text{ V}$
Total Unadjusted Error <sup>2) 3)</sup>	$TUE \text{ CC}$	-4	-	4	LSB	12-bit resolution for primary/secondary groups, 10-bit resolution for fast compare channels
INL Error <sup>2)</sup>	$EA_{\text{INL CC}}$	-3	-	3	LSB	
DNL error <sup>2) 4)</sup>	$EA_{\text{DNL CC}}$	-1	-	3	LSB	
Gain Error <sup>2)</sup>	$EA_{\text{GAIN CC}}$	-3.5	-	3.5	LSB	
Offset Error <sup>2) 3)</sup>	$EA_{\text{OFF CC}}$	-4	-	4	LSB	
RMS Noise <sup>2) 5) 6)</sup>	$EN_{\text{RMS CC}}$	-	0.5	0.8	LSB	Noise reduction level 3
		-	0.5	1.0	LSB	Standard conversion

表 3-21 VADC 5V (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reference input charge consumption per conversion (from $V_{AREF}$ ) <sup>7) 8) 9)</sup>	$Q_{CONV}$ CC	-	-	20	pC	$V_{AIN} = 0$ V (worst case), precharging disabled
		-	-	10	pC	$V_{AIN} = 0$ V (worst case), precharging enabled, $V_{DDM} - 5\% < V_{AREF} < V_{DDM} + 50$ mV
Switched capacitance of an analog input	$C_{AINS}$ CC	-	2.5	3.4	pF	Input buffer disabled
Analog input charge consumption <sup>10)</sup>	$Q_{AINS}$ CC	-	-	3.5	pC	Primary groups and fast compare channels; $V_{AIN} = V_{AREF}$ ; $V_{DDM} = 5.0$ V; input buffer enabled; $T_J \leq 150^\circ\text{C}$
		-	-	3.8	pC	Primary groups and fast compare channels; $V_{AIN} = V_{AREF}$ ; $V_{DDM} = 5.0$ V; input buffer enabled; $T_J > 150^\circ\text{C}$
		-	-	4.4	pC	Secondary groups; $V_{AIN} = V_{AREF}$ ; $V_{DDM} = 5.0$ V; input buffer enabled; $T_J \leq 150^\circ\text{C}$
		-	-	4.8	pC	Secondary groups; $V_{AIN} = V_{AREF}$ ; $V_{DDM} = 5.0$ V; input buffer enabled; $T_J > 150^\circ\text{C}$

表 3-21 VADC 5V (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Sampling time	$t_{s\text{ SR}}$	100	-	-	ns	Primary group or fast compare channel, 4.5 V $\leq V_{\text{DDM}} \leq 5.5$ V; input buffer disabled
		300	-	-	ns	Primary group or fast compare channel, 4.5 V $\leq V_{\text{DDM}} \leq 5.5$ V; input buffer enabled
		500	-	-	ns	Secondary group, 4.5 V $\leq V_{\text{DDM}} \leq 5.5$ V; input buffer disabled
		700	-	-	ns	Secondary group, 4.5 V $\leq V_{\text{DDM}} \leq 5.5$ V; input buffer enabled
		200	-	-	ns	Primary Group or fast compare channel, 2.97 V $\leq V_{\text{DDM}} < 4.5$ V; input buffer disabled
		400	-	-	ns	Primary group or fast compare channel, 2.97 V $\leq V_{\text{DDM}} < 4.5$ V; input buffer enabled
		1000	-	-	ns	Secondary group, 2.97 V $\leq V_{\text{DDM}} < 4.5$ V; input buffer disabled
		1200	-	-	ns	Secondary group, 2.97 V $\leq V_{\text{DDM}} < 4.5$ V; input buffer enabled
Sampling time for calibration	$t_{\text{SCAL SR}}$	50	-	-	ns	4.5 V $\leq V_{\text{DDM}} \leq 5.5$ V
		100	-	-	ns	2.97 V $\leq V_{\text{DDM}} < 4.5$ V
Input buffer switch-on time	$t_{\text{BUF CC}}$	-	0.4	1	$\mu\text{s}$	
Wakeup time	$t_{\text{WU CC}}$	-	0.1	0.2	$\mu\text{s}$	Fast standby mode
		-	1.6	3	$\mu\text{s}$	Slow standby mode
Broken wire detection delay against $V_{\text{AREF}}$	$t_{\text{BWR CC}}$	-	100	-	cycles	Result above 80% of full scale range, analog input buffer disabled
Broken wire detection delay against $V_{\text{AGND}}$	$t_{\text{BWG CC}}$	-	100	-	cycles	Result below 10% of full scale range, analog input buffer disabled
Converter diagnostics unit resistance <sup>11)</sup>	$R_{\text{CSD CC}}$	45	-	75	kOhm	
Converter diagnostics voltage accuracy	$dV_{\text{CSD CC}}$	-10	-	10	%	Percentage refers to $V_{\text{DDM}}$

表 3-21 VADC 5V (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Resistance of the multiplexer diagnostics pull-up device	$R_{MDU\ CC}$	30	-	42	kOhm	$0V \leq V_{IN} \leq 0.9 * V_{DDM}$ , Automotive Levels
		56	-	78	kOhm	$0V \leq V_{IN} \leq 0.9 * V_{DDM}$ , TTL Levels
Resistance of the multiplexer diagnostics pull-down device	$R_{MDD\ CC}$	43	-	58	kOhm	$0.1 * V_{DDM} \leq V_{IN} \leq V_{DDM}$ , Automotive level
		18	-	25	kOhm	$0.1 * V_{DDM} \leq V_{IN} \leq V_{DDM}$ , TTL level
Resistance of the pull-down test device	$R_{PDD\ CC}$	-	-	0.3	kOhm	Measured at pad input voltage $V_{IN} = V_{DDM} / 2$ .

- 1) 这些限制适用于标准基准输入以及备用基准输入。
- 2) 该参数取决于基准电压范围和电源纹波，请参阅简介。  
最坏情况下的组合误差是 TUE 和  $EN_{RMS}$  的算术组合。  
测试是在完成启动校准后禁用后校准的情况下进行的。
- 3) 映射到 SLOW 类型焊盘的模拟输入会影响精度。此参数的值以 3 LSB<sub>12</sub> 为单位递增。
- 4) 单调性特性，校准时不会漏码。
- 5) 参数  $EN_{RMS}$  指的是 1 sigma 分布。
- 6) 映射到 SLOW 类型焊盘的模拟输入 RMS 噪声 ( $EN_{RMS}$ ) 最高可达 2 LSB<sub>12</sub> (启用 DC/DC 软开关)。
- 7) 对于降低的参考电压  $V_{AREF} < 3.375V$ ，消耗的电荷 QCONV 会减少  $k2 = V_{AREF} [V] / 3.375$ 。对于降低的参考电压  $4.5V < V_{AREF} \leq 3.375V$ ，QCONV 不会降低。
- 8) 当 BWD (断线检测) 处于活动状态时，最大电荷增加 15 pC。
- 9) 快速比较通道仅消耗主/次组电荷的 1/3。
- 10) 对于具有叠加数字 GPIO 或 PDD 功能的模拟输入，该值增加 1 pC。
- 11) 使用至少 1.1  $\mu s$  的采样时间以确保测试电压正确稳定。

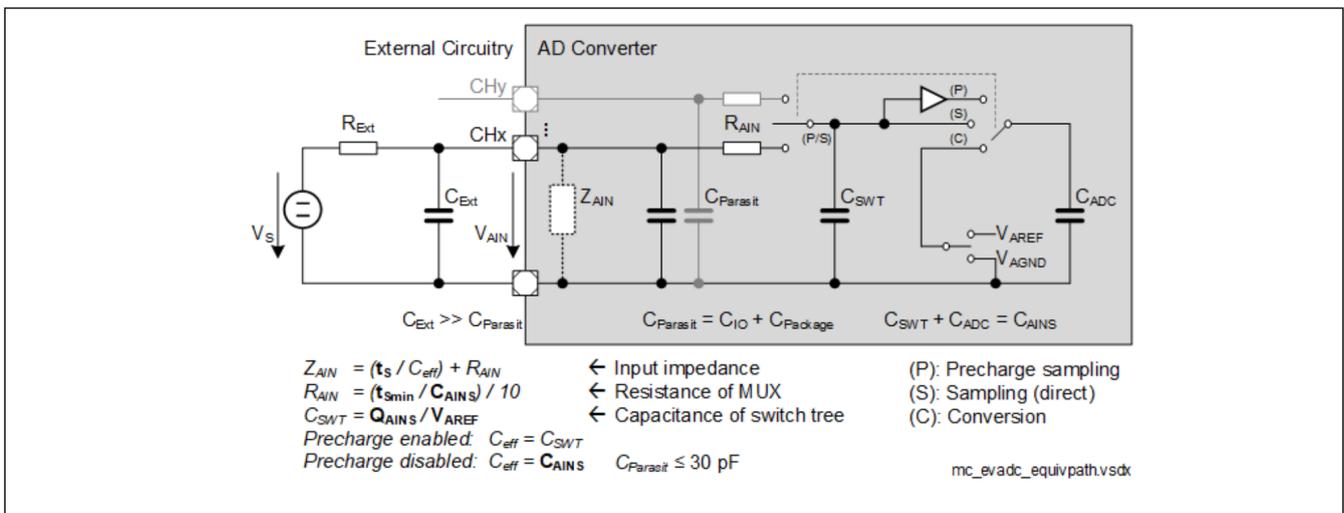


图 3-2 模拟输入等效电路

### 3.8 DSADC 参数

DSADC 参数仅对电压范围  $4.5\text{ V} \leq V_{\text{DDM}} \leq 5.5\text{ V}$  有效。

这些参数描述产品特性，不包括外部电路。如无明确定义，这些值适用于结温  $T_J \leq 150^\circ\text{C}$  的情况。

校准针对增益因子 1 和 2 指定，校准值参考这些设置。

信噪比 (SNR) 针对差分输入指定。对于单端操作，产生的信噪比会降低 6 dB。对于准差分模式（即使用  $V_{\text{CM}}$ ），增益 = 1 时信噪比会降低 6 dB，增益 = 2 时信噪比会降低 3 dB。

表 3-22 DSADC 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Common mode voltage bias resistance	$R_{\text{BIAS CC}}$	105	130	155	kOhm	On-chip variation $\leq \pm 2.5\%$ .
Positive reference voltage	$V_{\text{AREF SR}}$	4.5	-	$V_{\text{DDM}} + 0.05$	V	
Reference ground voltage	$V_{\text{AGND SR}}$	$V_{\text{SSM}}$	-	$V_{\text{SSM}}$	V	$V_{\text{SSM}}$ and $V_{\text{AGND}}$ are connected together
Reference load current	$I_{\text{REF CC}}$	-	10	12	$\mu\text{A}$	Per modulator
		-	-	14	$\mu\text{A}$	Per modulator, $T_J > 150^\circ\text{C}$
Common mode voltage accuracy <sup>1)</sup>	$dV_{\text{CM CC}}$	-100	-	100	mV	Deviation from selected voltage
Analog input voltage range	$V_{\text{DSIN SR}}$	$V_{\text{SSM}}$	-	$2 * V_{\text{DDM}}$	V	Differential; $V_{\text{DSXP}} - V_{\text{DSXN}}$
		$V_{\text{SSM}}$	-	$V_{\text{DDM}}$	V	Single ended
Input current <sup>2)</sup>	$I_{\text{RMS CC}}$	7	10	13	$\mu\text{A}$	Exact value ( $\pm 1\%$ ) available in UCB; valid for gain = 1 and $f_{\text{MOD}} = 26.7\text{ MHz}$
On-chip modulator clock frequency	$f_{\text{MOD SR}}$	16	-	40	MHz	
Gain error <sup>3)4)</sup>	$ED_{\text{GAIN CC}}$	-0.2 <sup>5)</sup>	$\pm 0.1$ <sup>5)</sup>	0.2 <sup>5)</sup>	%	$T_J \leq 150^\circ\text{C}$ ; Target, calibrated, $V_{\text{AREF}}$ constant after calibration; $f_{\text{MOD}} = 26.67\text{ MHz}$
		-	$\pm 0.25$	-	%	$T_J > 150^\circ\text{C}$ ; $V_{\text{AREF}}$ constant after calibration; $f_{\text{MOD}} = 26.67\text{ MHz}$
		-1	-	1	%	Calibrated once; $f_{\text{MOD}} = 26.67\text{ MHz}$
		-2.5	-	2.5	%	Uncalibrated; $f_{\text{MOD}} = 26.67\text{ MHz}$

表 3-22 DSADC 5V (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DC offset error <sup>3)</sup>	$ED_{OFF} CC$	-5 <sup>5)</sup>	-	5 <sup>5)</sup>	mV	Calibrated; $f_{MOD} = 26.67$ MHz
		-10	-	10	mV	Calibrated once; $f_{MOD} = 26.67$ MHz
		-30	-	30	mV	Uncalibrated; $f_{MOD} = 26.67$ MHz
Signal-Noise Ratio for differential input signals <sup>2)6)7)</sup>	$SNR CC$	80	-	-	dB	$T_J \leq 150^\circ C$ ; $f_{PB} = 30$ kHz; $f_{MOD} = 26.67$ MHz
		78	-	-	dB	$T_J \leq 150^\circ C$ ; $f_{PB} = 50$ kHz; $f_{MOD} = 26.67$ MHz
		74	-	-	dB	$T_J \leq 150^\circ C$ ; $f_{PB} = 100$ kHz; $f_{MOD} = 26.67$ MHz
Signal-Noise Ratio degradation	$DSNR CC$	-	-	3	dB	$T_J > 150^\circ C$ ; Resulting Signal-Noise Ratio value is SNR - DSNR
Spurious-free dynamic range <sup>3)</sup>	$SFDR CC$	60	-	-	dB	$f_{MOD} = 26.67$ MHz
Output sampling rate	$f_D CC$	3.906	-	300	kHz	16 MHz / 4096, without integrator
Pass band	$f_{PB} CC$	1.302	-	100	kHz	Output data rate: $f_D = f_{PB} * 3$ ; without integrator
		1.302	-	10	kHz	Output data rate: $f_D = f_{PB} * 6$ ; without integrator
Pass band ripple	$df_{PB} CC$	-0.08	-	0.08	dB	FIR filters enabled
Stop band attenuation	$SBA CC$	40	-	-	dB	$0.5f_D \dots 1.0f_D$
		45	-	-	dB	$1.0f_D \dots 1.5f_D$
		50	-	-	dB	$1.5f_D \dots 2.0f_D$
		55	-	-	dB	$2.0f_D \dots 2.5f_D$
		60	-	-	dB	$2.5f_D \dots OSR/2f_D$
DC compensation factor	$DCF CC$	-3	-	-	dB	$10^{-5}f_D$ , offset compensation filter enabled (FCFGMx.OCEN = 001 <sub>B</sub> )
Modulator settling time	$t_{MSET} CC$	-	-	20	$\mu s$	After switching on, voltage regulator already running

1) 在具有叠加 GPIO 功能的引脚上, 由于  $T_J > 150^\circ C$  时的漏电流, 最大限值最多增加 25 mV。

2) 有关详细信息, 请参阅用户手册章节。

3) 此参数在  $f_{MOD}$  定义的范围有效。

4) 如果采用相同的校准策略, 不同 DSADC 通道之间的增益不匹配误差在  $\pm 0.5\%$  以内

- 5) 如果温度变化  $>20^{\circ}\text{C}$ ，则需要重新校准
- 6) 这些值对于模拟增益因子 1 有效，每增加一个增益因子，减去 3 dB。
- 7) 对于单端输入信号和增益 1，SNR 降低 6 dB。

### 3.9 MHz 振荡器

OSC\_XTAL 用作精确的时钟源。OSC\_XTAL 支持 16 MHz 至 40 MHz 外部晶振。还支持陶瓷谐振器。

表 3-23 OSC\_XTAL

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current at XTAL1	$I_{IX1}$ CC	-70	-	70	μA	$V_{IN} > 0V$ ; $V_{IN} < V_{EXT}$
Oscillator frequency	$f_{OSC}$ SR	4	-	40	MHz	Direct Input Mode selected, if shaper is not bypassed
		16	-	40	MHz	External Crystal Mode selected
Oscillator start-up time	$t_{OSCS}$ CC	-	-	3 <sup>1)</sup>	ms	$20MHz \leq f_{OSC}$ and 8pF load capacitance
Input voltage at XTAL1 <sup>2)</sup>	$V_{IX}$ SR	-0.7	-	$V_{EXT} + 0.5$	V	If shaper is not bypassed
Input amplitude (peak to peak) at XTAL1	$V_{PPX}$ SR	$0.3 * V_{EXT}$	-	$V_{EXT} + 1.0$	V	If shaper is not bypassed; $f_{OSC} > 25MHz$
		$0.35 * V_{EXT}$	-	$V_{EXT} + 1.0$	V	If shaper is not bypassed; $f_{OSC} \leq 25MHz$
Internal load capacitor	$C_{L0}$ CC	1.30	1.40	1.55	pF	enabled via bit OSCCON.CAPOEN
Internal load capacitor	$C_{L1}$ CC	3.05	3.35	3.70	pF	enabled via bit OSCCON.CAP1EN
Internal load capacitor	$C_{L2}$ CC	7.85	8.70	9.55	pF	enabled via bit OSCCON.CAP2EN
Internal load capacitor	$C_{L3}$ CC	12.05	13.35	14.65	pF	enabled via bit OSCCON.CAP3EN
Internal load stray capacitor between XTAL1 and XTAL2	$C_{XINTS}$ CC	1.15	1.20	1.25	pF	
Internal load stray capacitor between XTAL1 and ground	$C_{XTAL1}$ CC	-	2.5	4	pF	
Duty cycle at XTAL1 <sup>3)</sup>	$DC_{X1}$ SR	35	-	65	%	$V_{XTAL1} = 0.5 * V_{PPX}$
Absolute RMS jitter at XTAL1 <sup>3)</sup>	$J_{ABSX1}$ SR	-	-	28	ps	10 KHz to $f_{OSC}/2$
Slew rate at XTAL1 <sup>3)</sup>	$SR_{XTAL1}$ SR	0.3	-	-	V/ns	Maximum 30% difference between rising and falling slew rate

1)  $t_{OSCS}$  定义为从振荡器模式设置为外部晶振模式的时刻开始，直到振荡在 XTAL1 处达到  $0.3 * V_{EXT}$  的幅度。

该值取决于所用外部晶振的频率。对于更快的晶振频率，该值会减小。

2) 对于电源 ( $V_{EXT} < 5.3V$   $V_{IX}$ ) 最小可低至 -0.9V。对于 XTAL1，低至 -0.9V 的输入电平不会导致使用外部晶振时损坏或出现可靠性问题。

3) XTAL1 的方波输入信号。

*注释：强烈建议测量最终目标系统（布局）中的振荡裕度（负阻），以确定振荡器运行的最佳参数。请参考晶振或陶瓷谐振器供应商指定的限制。*

### 3.10 备用时钟

备用时钟提供了替代时钟源。

表 3-24 备用时钟

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Back-up clock accuracy before trimming	$f_{\text{BACKUT CC}}$	70	100	130	MHz	$V_{\text{EXT}} \geq 2.97\text{V}$
Back-up clock accuracy after trimming <sup>1)</sup>	$f_{\text{BACKT CC}}$	98	100	102	MHz	$V_{\text{EXT}} \geq 2.97\text{V}$
Standby clock	$f_{\text{SB CC}}$	25	70	110	kHz	$V_{\text{EXT}} \geq 2.97\text{V}$

1) 通过每 2 毫秒定期调整温度和电压漂移，可以实现短期调整，从而满足 LIN 通信所需的精度，最高温度可达 125 摄氏度

### 3.11 温度感应器

**表3-25 DTS PMS**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time for each conversion <sup>1)</sup>	$t_M$ CC	-	-	2.7	ms	Measured from cold power-on reset release
Calibration reference accuracy	$T_{CALACC}$ CC	-1	-	1	°C	calibration points @ $T_J=-40^{\circ}\text{C}$ and $T_J=127^{\circ}\text{C}$
Accuracy over temperature range	$T_{NL}$ CC	-2	-	2	°C	$T_{CALACC}$ has to be added in addition
DTS temperature range	$T_{SR}$ SR	-40	-	170	°C	

1) 热复位后,  $t_M$  不会重新启动, 而是从上次转换开始测量。

**表 3-26 DTS 核心**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time for each conversion <sup>1)</sup>	$t_M$ CC	-	-	2.7	ms	Measured from cold power-on reset release
Temperature difference between on chip temperature sensors	$\Delta T$ CC	-3	-	3	°C	
Calibration reference accuracy	$T_{CALACC}$ CC	-2	-	2	°C	calibration points @ $T_J=-40^{\circ}\text{C}$ and $T_J=127^{\circ}\text{C}$
Accuracy over temperature range	$T_{NL}$ CC	-2	-	2	°C	$T_{CALACC}$ has to be added in addition
DTS temperature range	$T_{SR}$ SR	-40	-	170	°C	

1) 热复位后,  $t_M$  不会重新启动, 而是从上次转换开始测量。

### 3.12 电源电流

下面定义的总电源电流由漏电流和开关分量组成。

应用相关值通常低于下表给出的值，并且取决于客户的系统运行条件（例如热连接或使用的应用配置）。

下表中参数的工作条件为：

真正的（现实的）功率类型唤醒码定义以下条件：

- $T_J = 150\text{ }^\circ\text{C}$
- $f_{\text{SRI}} = f_{\text{CPUX}} = 300\text{ MHz}$
- $f_{\text{GTM}} = 200\text{ MHz}$
- $f_{\text{SPB}} = f_{\text{STM}} = f_{\text{BAUD1}} = f_{\text{BAUD2}} = f_{\text{ASCLINx}} = 100\text{ MHz}$
- $V_{\text{DD}} = 1.275\text{ V}$
- $V_{\text{DDP3}} / \text{FLEX} = 3.366\text{ V}$
- $V_{\text{EXT}} / \text{EVRSB} = V_{\text{DDM}} = 5.1\text{ V}$
- 所有核心都激活，包括四个锁步核（IPC=0.6）
- 以下模块处于非活动状态：HSM、HSCT、GETH、Ethernet、PSI5、I2C、FCE、EBU、SPU、RIF和MTU

最大功率模式码定义为以下条件：

- $T_J = 150\text{ }^\circ\text{C}$
- $f_{\text{SRI}} = f_{\text{CPUX}} = 300\text{ MHz}$
- $f_{\text{GTM}} = 200\text{ MHz}$
- $f_{\text{SPB}} = f_{\text{STM}} = f_{\text{BAUD1}} = f_{\text{BAUD2}} = f_{\text{ASCLINx}} = 100\text{ MHz}$
- $V_{\text{DD}} = 1.375\text{ V}$
- $V_{\text{DDP3}} / \text{FLEX} = 3.63\text{ V}$
- $V_{\text{EXT}} / \text{EVRSB} = V_{\text{DDM}} = 5.5\text{ V}$
- 所有核心都激活，包括四个锁步核心（IPC=1.2）
- 以下模块处于非活动状态：GETH、FCE、SPU、RIF和MTU

ADAS 电源模式定义了以下条件：

- $T_J = 125\text{ }^\circ\text{C}$
- $f_{\text{SRI}} = f_{\text{CPUX}} = 300\text{ MHz}$
- $f_{\text{GTM}} = 100\text{ MHz}$
- $f_{\text{SPU}} = 300\text{ MHz}$ ；（FFT 长度=2048，复杂窗口）
- $f_{\text{SPB}} = f_{\text{STM}} = f_{\text{BAUD1}} = f_{\text{BAUD2}} = f_{\text{ASCLINx}} = 100\text{ MHz}$
- $V_{\text{DD}} = 1.275\text{ V}$
- $V_{\text{DDP3}} / \text{EXT} / \text{FLEX} / \text{EVRSB} = V_{\text{DDM}} = 3.366\text{ V}$
- CPU0和CPU1（IPC=1.2）和CPU2（IPC=0.6）核心处于激活状态，包括三个锁步核心；CPU3（IPC=0.6）没有锁步核心处于激活状态
- 只有EVADC0和EVADC1激活
- 以下模块处于非活动状态：CPU4、CPU5、HSM、HSCT、GETH、PSI5、I2C、FCE、EBU、MSC、DSADC和MTU

表 3-27 电流消耗

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
$\Sigma$ Sum of $I_{DD}$ core and peripheral supply currents (incl. $I_{DDPORST} + \Sigma I_{DCCx0} + \Sigma I_{DCCxx} + I_{DDGTM} + I_{DDSB}$ )	$I_{DDRAIL}$ CC	-	-	1500	mA	ADAS power pattern
		-	-	1640	mA	max power pattern; $T_j=150^\circ\text{C}$
		-	-	1372	mA	real power pattern; $T_j=150^\circ\text{C}$
		-	-	1556	mA	real power pattern; $T_j=160^\circ\text{C}$
$I_{DD}$ core current during active power-on reset (PORST pin held low). Leakage current of core domain. <sup>1)</sup>	$I_{DDPORST}$ CC	-	-	300	mA	$V_{DD} = 1.275\text{V}$ ; $T_j=125^\circ\text{C}$
		-	-	575	mA	$V_{DD} = 1.275\text{V}$ ; $T_j=150^\circ\text{C}$
		-	-	759	mA	$V_{DD} = 1.275\text{V}$ ; $T_j=160^\circ\text{C}$
		-	-	835	mA	$V_{DD} = 1.275\text{V}$ ; $T_j=165^\circ\text{C}$
$\Sigma$ Sum of $I_{DDP3}$ 3.3 V supply currents	$I_{DDP3RAIL}$ CC	-	-	50 <sup>2)</sup>	mA	ADAS power pattern incl. Flash read current and Dflash programming current.
		-	-	60 <sup>2)</sup>	mA	max power pattern incl. Flash read current and Dflash programming current.
		-	-	50 <sup>2)</sup>	mA	real power pattern incl. Flash read current and Dflash programming current.
$\Sigma$ Sum of external $I_{EXT}$ supply currents (incl. $I_{EXTFLEX} + I_{EVRSB} + I_{EXTLVDS}$ )	$I_{EXTRAIL}$ CC	-	-	60	mA	max power pattern
		-	-	54 <sup>3)</sup>	mA	real power pattern
$I_{EXT}$ and $I_{FLEX}$ supply current	$I_{EXTFLEX}$ CC	-	-	22 <sup>1)1)4) 5)</sup>	mA	real power pattern with port activity absent; PORST output inactive.
$I_{EVRSB}$ supply current <sup>1)</sup>	$I_{EVRSB}$ CC	-	-	8	mA	real power pattern; PMS/EVR module current considered without SCR and Standby RAM during RUN mode.
$\Sigma$ Sum of external $I_{DDM}$ supply currents (incl. $I_{DDMEVADC} + I_{DDMEDSADC}$ )	$I_{DDM}$ CC	-	-	60	mA	real power pattern; sum of currents of EDSADC and EVADC modules

表 3-27 电流消耗 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
$\Sigma$ Sum of all currents (incl. $I_{EXTRAIL} + I_{DDMRIL} + I_{DDX3RAIL} + I_{DD}$ )	$I_{DDTOT} CC$	-	-	1536	mA	real power pattern; $T_J=150^\circ C$
		-	-	1720	mA	real power pattern; $T_J=160^\circ C$
$\Sigma$ Sum of all currents with DC-DC EVRC regulator active <sup>6)</sup>	$I_{DDTOTDC3} CC$	-	-	980	mA	real power pattern; EVRC reset settings with 72% efficiency; $V_{EXT} = 3.3V; T_J=160^\circ C$
$\Sigma$ Sum of all currents with DC-DC EVRC regulator active <sup>6)</sup>	$I_{DDTOTDC5} CC$	-	-	670	mA	real power pattern; EVRC reset settings with 72% efficiency; $V_{EXT} = 5V; T_J=160^\circ C$
$\Sigma$ Sum of all currents (SLEEP mode) <sup>1)</sup>	$I_{SLEEP} CC$	-	-	38	mA	All CPUs in idle, All peripherals in sleep, $f_{SRI/SPB} = 1 MHz$ via LPDIV divider; $T_J = 25^\circ C$
$\Sigma$ Sum of all currents (STANDBY mode) drawn at $V_{EVRSB}$ supply pin <sup>7)</sup>	$I_{STANDBY} CC$	-	-	130 <sup>8)</sup>	$\mu A$	32 kB Standby RAM block active. SCR inactive. Power to remaining domains switched off. $T_J = 25^\circ C$ ; $V_{EVRSB} = 5V$
Maximum power dissipation <sup>9)</sup>	$PD SR$	-	-	2240	mW	ADAS power pattern; $T_J=125^\circ C$
		-	-	3220	mW	max power pattern; $T_J=150^\circ C$
		-	-	2500	mW	real power pattern; $T_J=150^\circ C$

- 1) 限值是根据实际功率模式 ( $V_{DD} = 1.275V$ ) 定义的。对于最大功率模式, 限值必须乘以系数 1.22。
- 2) 实际的 Pflash 读取模式, Pflash 带宽利用率为 50%, 代码混合为 50% 的 0 和 50% 的 1。使用至少 100nF 的公共去耦电容 ( $V_{DDP3}$ )。在 3.3V 电源下以突发模式连续进行 Dflash 编程, 并并行进行实际的 Pflash 读取访问。相应闪存模块的擦除电流小于  $V_{DDP3}$  引脚上的相应编程电流。编程和擦除闪存可能会产生高达 45 mA / 20 ns 的瞬态电流尖峰。由去耦电容器和缓冲电容器处理。此参数与外部电源尺寸有关, 与热无关。
- 3) 针对实际功率模式定义了限制。对于 ADAS 电源模式限制总和为 40mA。
- 4) 电流消耗仅包括最小的端口活动。
- 5) 针对实际功率模式定义了限制。对于 ADAS 功率模式限制必须乘以系数 0.7。
- 6) 从外部调节器汲取的总电流是根据 72% EVRC SMPS 调节器效率估算的。IDDTOTDCx 是使用缩放的核心电流 [(IDD x VDD)/(Vin x Efficiency)] 根据 IDDTOT 计算得出的, 并构成所有其他轨电流和 IDDM。
- 7) 同样的电流限制也适用于其他功率模式。

- 8)  $\Sigma$  运行模式下 VEVR SB 电源引脚上所有电流的总和小于 ( $I_{EVRSB} + 4 \text{ mA}$  待机 RAM 电流 +  $I_{SCRSB}$  (如果 SCR 处于活动状态))。  $\Sigma$  建议在此引脚上至少使用 100 nF 去耦电容。 32kB 待机 SRAM 对  $I_{STANDBY}$  电流的使用不到 10 $\mu$ A。
- 9) 仅当所有电源均由外部供电且不包含 EVR33 和 EVRC 的功率损耗时, 这些值才有效。

表3-28 模块电流消耗

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
$I_{DDP3}$ supply current for programming of a Pflash or Dflash bank <sup>1)</sup>	$I_{DDP3PROG} CC$	-	-	25	mA	Pflash 3.3V programming current adder when using external 3.3V supply.
		-	-	9 <sup>2)</sup>	mA	Pflash 3.3V programming current adder when using external 5V supply.
$I_{EXT}$ supply current added by LVDS pads in LVDS mode <sup>1)</sup>	$I_{EXTLVDS} CC$	-	-	9 <sup>3)</sup>	mA	real power pattern; 6 pairs of LVDS pins active with receive function
		-	-	24	mA	real power pattern; 6 pairs of LVDS pins active with transmit function

**表 3-28 模块电流消耗 (续)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
$\Sigma$ Sum of external $I_{DDM}$ supply currents (incl. $I_{DDMEVADC} + I_{DDMEDSADC}$ )	$I_{DDM\ CC}$	-	-	44	mA	real power pattern; current for EDSADC modules only and EVADC modules are inactive; 11 EDSADC channels active continuously.
		-	-	63 <sup>4)</sup>	mA	max power pattern; current for EDSADC modules only and EVADC modules are inactive; all EDSADC channels active continuously.
		-	-	16 <sup>5)</sup>	mA	real power pattern; current for EVADC modules only and EDSADC modules are inactive; 12 EVADC modules active.
		-	-	20 <sup>6)</sup>	mA	max power pattern; current for EVADC modules only and EDSADC modules are inactive; all EVADC modules active.
$I_{DDP3}$ supply current for erasing of a Pflash or Dflash bank	$I_{DDP3ERASE\ CC}$	-	-	25	mA	Pflash 3.3V erasing current adder when using external 3.3V supply.
SCR 8-bit Standby Controller current incl. PMS in STANDBY Mode drawn at $V_{EVRSB}$ supply pin	$I_{SCR\ SB\ CC}$	-	-	7.5 <sup>7)</sup>	mA	SCR power pattern incl. PMS current consumption with fback clock active; $f_{SYS\_SCR} = 20\text{MHz}; T_j = 150^\circ\text{C}$
		-	0.150	-	mA	SCR power pattern incl. PMS current consumption with fback inactive; $f_{SYS\_SCR} = 70\text{kHz}; T_j = 25^\circ\text{C}$
SCR 8-bit Standby Controller CPU in IDLE mode <sup>8)</sup>	$I_{SCRIDLE\ CC}$	-	-	3.5	mA	real power pattern. CPU set into idle mode.

1) 同样的电流限制也适用于其他功率模式。

2) 在 5V 电压下对 Pflash 进行编程期间, VEXT 电源轨上会额外消耗 3 mA 电流。

3) 单个 LVDS 对的接收功能限制为 1.5mA ( $t_{EXTLVDS}$ )。

- 4) 单个 DS 通道实例消耗 4 mA。
- 5) 在具有 2 个 EVADC 的“ADAS 功率模式”下，EVADC 电流被限制为 3 mA ( $I_{DDM}$ )。
- 6) 单个 VADC 单元消耗 1.3 mA 的电流。
- 7) 如果激活了 SCRADCOMP，则需要考虑额外的 0.6 mA 加法器。
- 8) 限值是根据实际功率模式 ( $V_{DD} = 1.275V$ ) 定义的。对于最大功率模式，限值必须乘以系数 1.22。

表 3-29 模块核心电流消耗

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
$I_{DD}$ core current of CPUx main core with CPUx lockstep core inactive	$I_{DDCx0}$ CC	-	-	70	mA	max power pattern; IPC=1.2
		-	-	45	mA	real power pattern; IPC=0.6
$I_{DD}$ core current of CPUx main core with CPUx lockstep core active	$I_{DDCxX}$ CC	-	-	$I_{DDCx0} + 50$	mA	max power pattern; IPC=1.2
		-	-	$I_{DDCx0} + 40$	mA	real power pattern; IPC=0.6
$I_{DD}$ core current added by GTM	$I_{DDGTM}$ CC	-	-	160	mA	max power pattern
		-	-	130	mA	real power pattern; TIMx, TOMx, ATOMx, MCSx active. 3 clusters at 200 MHz.
		-	-	60	mA	TIMx, TOMx active at 100MHz. ATOMx, MCSx, DPLL inactive. 2 clusters at 100 MHz.
$I_{DD}$ core current added by HSM	$I_{DDHSM}$ CC	-	-	20 <sup>1)</sup>	mA	max power pattern; HSM running at 100MHz.
$I_{DD}$ core current added by SPU	$I_{DDSPU1}$ CC	-	-	360 <sup>2)</sup>	mA	CTRL.DIV = 00; SPU @ 300 MHz; FFT length 2048; DATSRC=EMEM; complex windowing
$I_{DD}$ core current added by SPU	$I_{DDSPU2}$ CC	-	-	310 <sup>2)</sup>	mA	CTRL.DIV = 00; SPU @ 300 MHz; FFT length 512; DATSRC=EMEM; complex windowing
$I_{DD}$ core dynamic current load jump during IDDSPU1 pattern.	$I_{DDSPULJ1}$ CC	-	-	390 <sup>3)</sup>	mA	CTRL.DIV = 00; SPU @ 300 MHz; FFT length 2048; DATSRC=EMEM; complex windowing

表 3-29 模块核心电流消耗 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
$I_{DD}$ core dynamic current load jump during IDDSPU2 pattern.	$I_{DDSPULJ2}$ CC	-	-	310 <sup>3)</sup>	mA	CTRL.DIV = 00; SPU @ 300 MHz; FFT length 512; DATSRC=EMEM; complex windowing
$I_{DD}$ core dynamic current added by LBIST	$I_{DDLBI}$ CC	-	-	150 <sup>4)</sup>	mA	LBIST Configuration A; $1.2V \leq V_{DD}$
$I_{DD}$ core dynamic current added by MBIST	$I_{DDMBI}$ CC	-	-	225	mA	fMBIST = 300MHz; tMBIST < 6ms. MTU Ganging procedure for SRAM test and initialization; VDD = 1.375V.

- 1) 电流消耗包括基本 HSM 活动，如 AES 模块。
- 2) 该电流估计为时钟激活时的 SPU 基本负载电流与条件中定义的 SPU 动态活动引起的平均电流之和。次级电压监测器过压阈值应设置为  $V_{DD} + 10\%$ ，欠压阈值应设置为  $V_{DD} - 9\%$ 。  
在  $I_{DDSPU1/2}$  使用情况下的 SPU 运行期间，外部供电的  $V_{DD}$  电压对于静态精度部分必须等于或大于 1.225V ( $V_{DD}$  标称 - 2%)，并且  $V_{DD}$  电源引脚的整体静态和动态范围应限制为 ( $V_{DD}$  标称 - 8%)。
- 3) SPU 活动期间的动态电流负载跳变由在超过 20 us 的建立时间持续时间后在  $V_{DD}$  引脚上观察到的条件定义。
- 4) LBIST 可在启动阶段执行，也可由应用软件触发。在 LBIST 执行时间  $t_{(LBIST)}$  内，二次电压监控器处于非活动状态。在启动阶段，外部提供的  $V_{DD}$  电压必须等于或大于 1.2V ( $V_{DD}$  标称 - 4%)，以确保静态准确性。如果  $V_{DD}$  由 EVRC 内部供电，则 EVRC 确保不违反  $V_{DD}$  的 1.2V 静态欠压限制。

### 3.12.1 计算 1.25 V 电流消耗

1.25 V 电源轨的电流消耗由两部分组成：

- 静态电流消耗
- 动态电流消耗

静态电流消耗与器件温度  $T_J$  相关，动态电流消耗取决于配置的时钟频率和执行的软件应用程序，需要将这两部分相加才能得到轨电流消耗。

(3.1)

$$I_0 = 5,8871 \left[ \frac{\text{mA}}{\text{C}} \right] \times e^{0,0246 \times T_J[\text{C}]}$$

(3.2)

$$I_0 = 16,4863 \left[ \frac{\text{mA}}{\text{C}} \right] \times e^{0,0232 \times T_J[\text{C}]}$$

方程式 (3.1) 定义典型的静态电流消耗和方程式 (3.2) 定义最大静态电流消耗，这两个公式在  $V_{DD} = 1.275$  V 时均有效。

### 3.13 电源基础结构和电源启动

### 3.13.1 供电上升和下降行为

电源轨的启动斜率应符合 SR (见表 3-33 供电坡道)。

#### 3.13.1.1 单电源模式 (a)

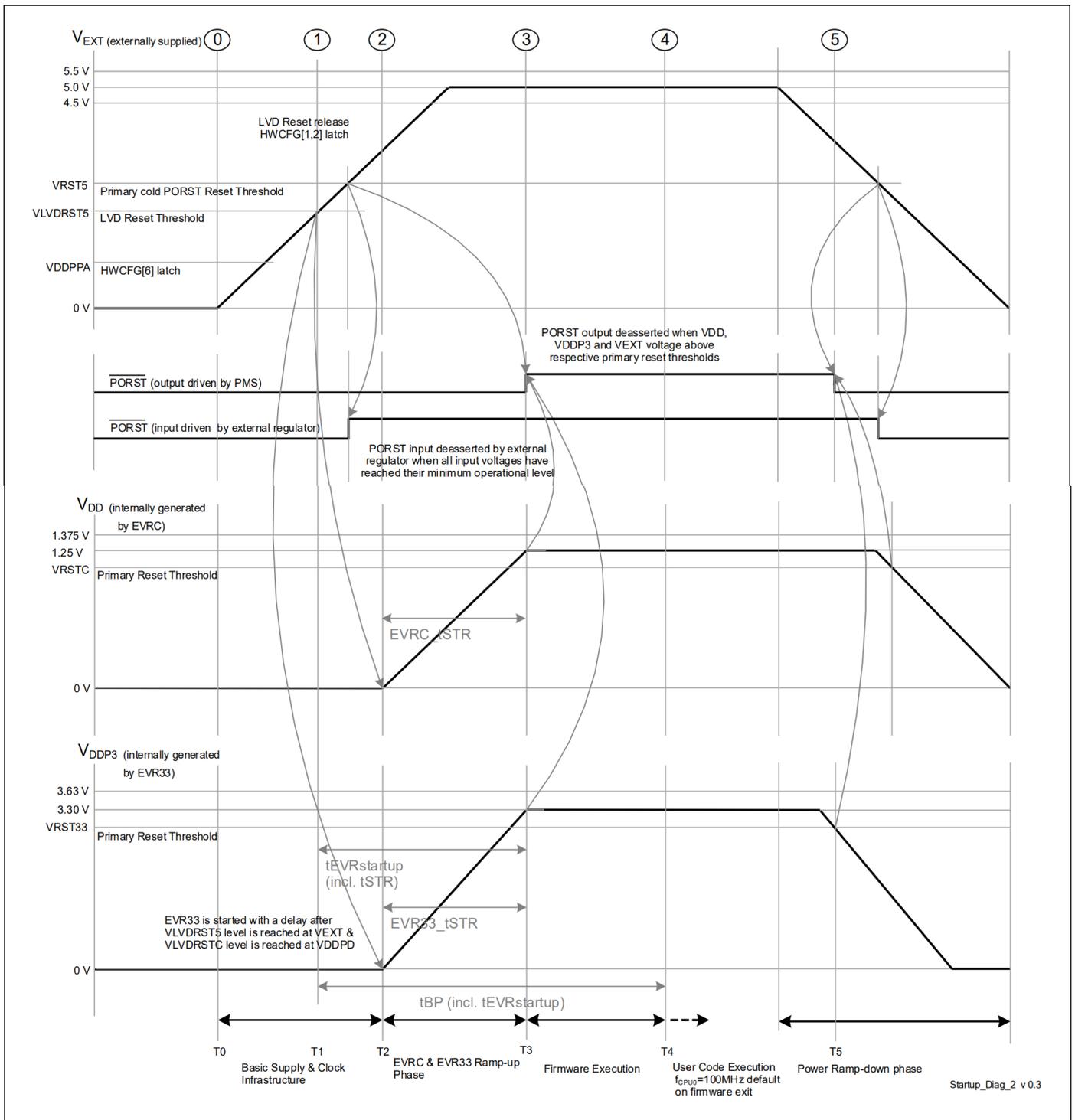


图 3-3 单电源模式 (a) - VEXT (5V) 单电源

VEXT = 5 V 单电源模式。VDD 和 VDDP3 由内置的 EVRC 和 EVR33 调节器从内部产生。

- 在基本基础结构和 EVRx 稳压器启动阶段 (T0 至 T2)，从外部稳压器 (dIEXT /dt) 吸取电流的速率受到限制，最大为 100 mA，稳定时间为 100 us。电源轨的启动斜率应符合数据手册参数 SR，斜率定义为 0% 至 100% 电压电平之间的最大切向斜率。实际波形可能不同于规格书。
- 此外，还确保在固件启动阶段 (T3 至 T4) 从调节器吸取的电流 (dIDD/dt) 限制为最大 100 mA，稳定时间为 100 us。
- 当 PORST (输入) 或 PORST (输出) 激活/置位时，PORST 激活/置位。
- PORST (输入) 有效意味着外部设备可通过将 PORST 引脚拉低，使复位保持有效。建议保持 PORST (输入) 有效，直到外部电源电压高于相应的主复位阈值。
- PORST (输出) 有效意味着  $\mu\text{C}$  在内部发出复位信号并将 PORST 引脚驱动至低电平，从而将复位信号传播至外部设备。当三个电源域 (VDD、VDDP3 或 VEXT) 中至少有一个违反其主要欠压复位阈值时， $\mu\text{C}$  会发出 PORST 置位 (输出) 信号。当所有电源均高于其主要复位阈值，且基本电源和时钟基础设施可用时， $\mu\text{C}$  会发出 PORST 不置位 (输出) 信号。在 T3 复位释放期间，预计负载跳变高达 150 mA (dIDD)。
- 电源时序如图 3-3 列举如下
  - T1 至 T2 是指外部电源上升时基本电源和时钟基础设施组件可用的时间段。带隙和内部时钟源启动，根据 HWCFG[2:1,4,5,6] 和 TESTMODE 引脚决定供电模式。T1 至 T2 是指外部电源上升时基本电源和时钟基础设施组件可用的时间段。启动带隙和内部时钟源。根据 HWCFG[2:1,6] 引脚决定供电模式。这些事件在 T1 时 LVD 复位释放后启动。当两个输入电压 VEXT 和 VEVRSB 分别高于 VLVD RST5 和 VLVD RSTSB 电平时，LVD 复位被释放。内部预调节器 VDDPD 输出电压高于 VLVD RSTC 水平。
  - T2 指的是 EVRC 和 EVR33 稳压器软启动的时间点。PORST (输入) 对 EVR33 或 EVRC 输出没有任何影响，尽管 PORST 已置位且器件处于复位状态，稳压器仍会继续产生相应的电压。产生的电压在 tSTR (数据手册参数) 时间内呈软上升趋势，以避免过冲。
  - T3 指的是所有电源都高于其主要复位阈值 (由 VRST5、VRST33 和 VRSTC 供电电压水平表示) 的时间点。EVRC 和 EVR33 调节器已经启动。PORST (输出) 不置位，并且 HWCFG[3:5] 引脚被 SCU 锁存在 PORST 上升沿。固件执行已启动。T1 和 T3 之间的时间记录为 tEVRstartup (数据手册参数)。
  - T4 指的是固件执行完成并且用户代码以 CPU0 的默认频率 100 MHz 开始执行的时间点。T0 和 T4 之间的时间记录为 tBP (数据手册参数)。
  - T5 指的是斜坡下降阶段期间至少一个外部提供或生成的电源 (VDD、VDDP3 或 VEXT) 降至其各自的初级欠压复位阈值以下的时间点。

## 3.13.1.2 单电源模式 (e)

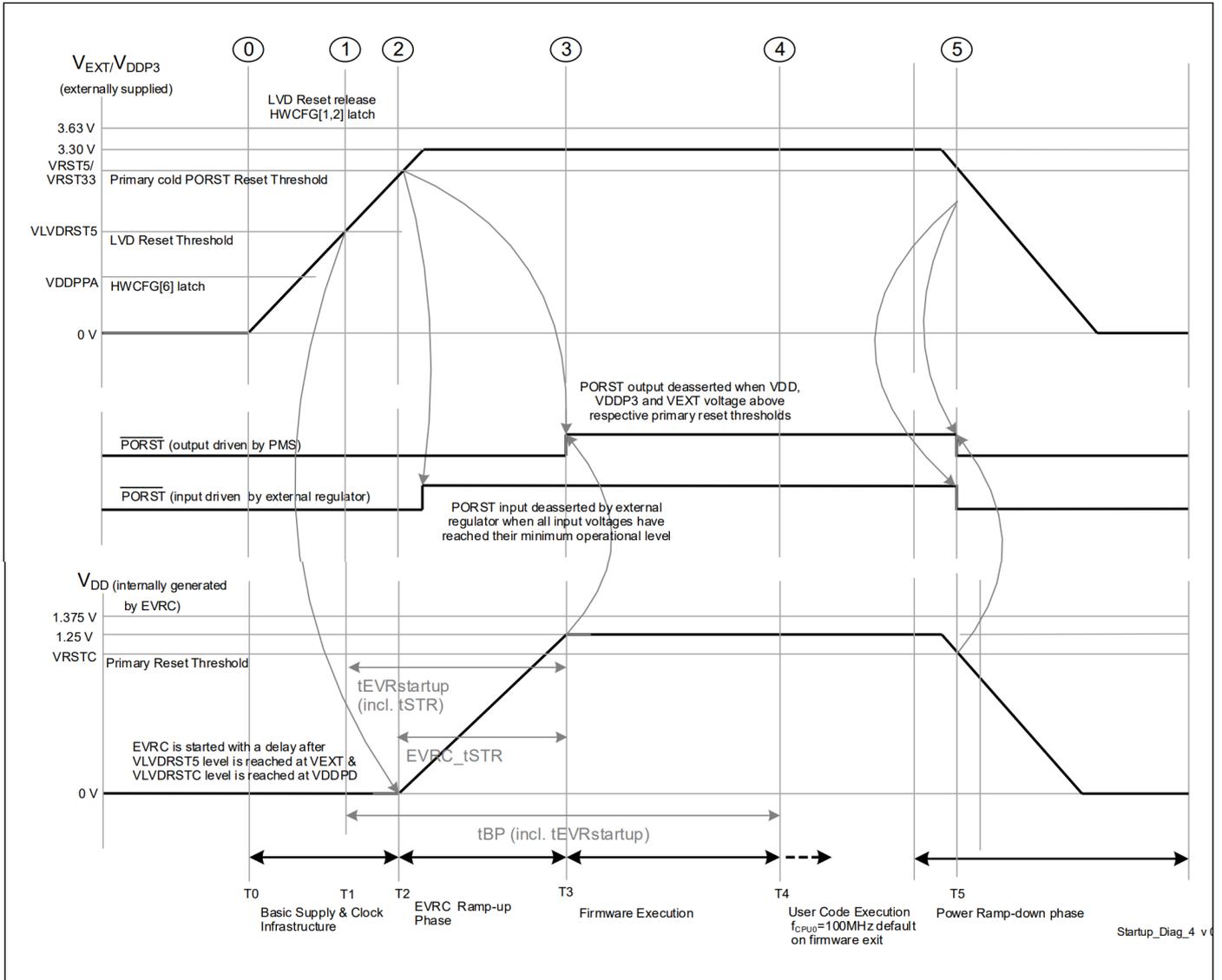


图 3-4 单电源模式 (e) - (VEXT 和 VDDP3) 3.3 V 单电源

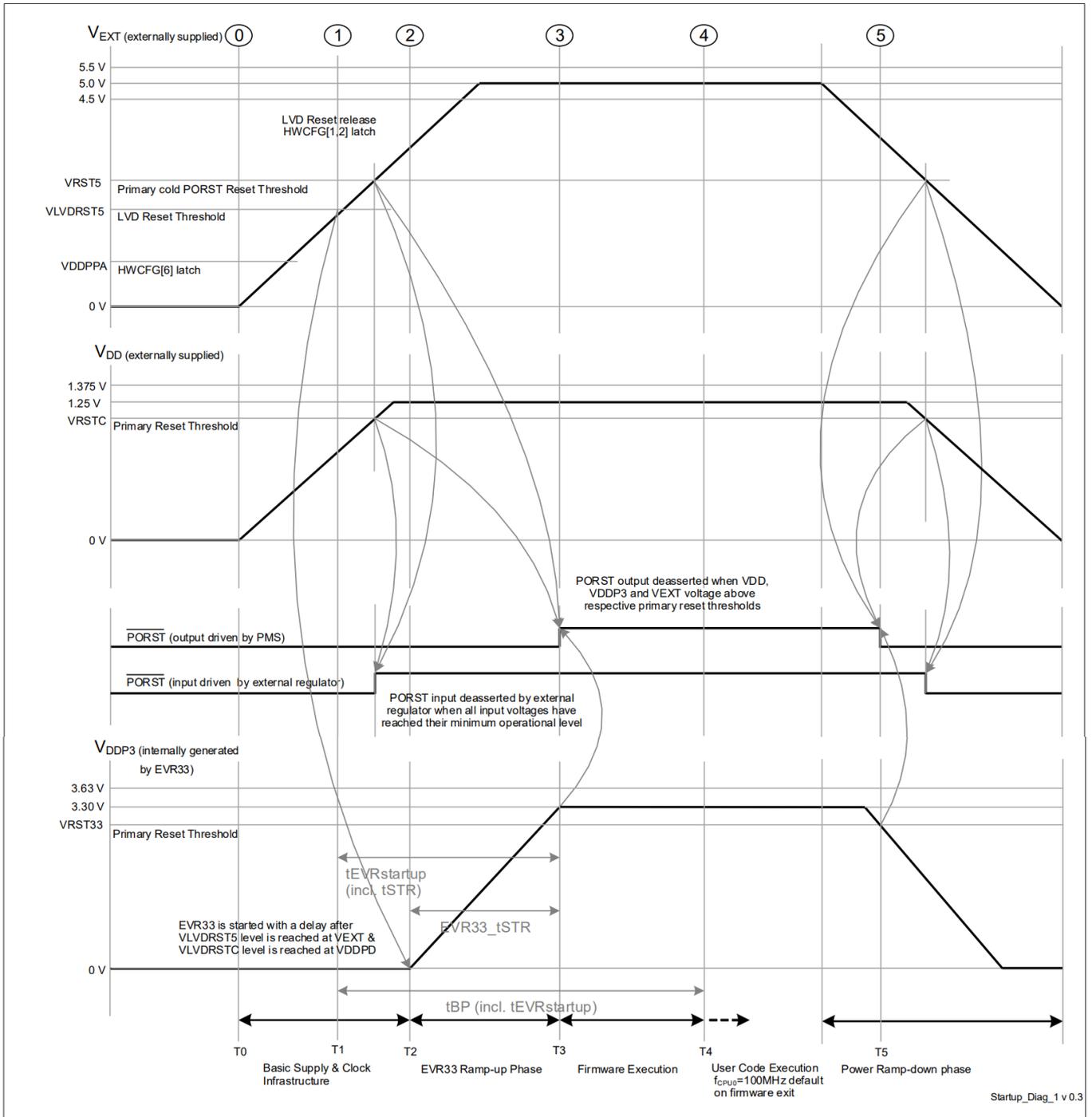
VEXT = VDDP3 = 3.3 V 单电源模式。VDD 由 EVRC 调节器内部产生。

- 从外部调节器汲取电流的速率 ( $di_{EXT}/dt$ ) 在启动阶段被限制为最大 100 mA，建立时间为 100 us。电源轨的启动斜率应符合数据手册参数 SR，斜率定义为 0% 至 100% 电压电平之间的最大切向斜率。实际波形可能不同于规格书。
- 当 PORST (输入) 或 PORST (输出) 激活/置位时，PORST 激活/置位。
- PORST (输入) 有效意味着外部设备可通过将 PORST 引脚拉低，使复位保持有效。建议保持 PORST (输入) 有效，直到外部电源电压高于相应的主复位阈值。
- PORST (输出) 有效意味着  $\mu C$  在内部发出复位信号并将 PORST 引脚驱动至低电平，从而将复位信号传播至外部设备。当三个电源域 (VDD、VDDP3 或 VEXT) 中至少有一个违反其主要欠压复位阈值时， $\mu C$  会发出 PORST 置位 (输出) 信号。当所有电源均高于其主要复位阈值，且基本电源和时钟基础设施可用时， $\mu C$  会发出 PORST 不置位 (输出) 信号。

基本供电和时钟基础设施可用。在 T3 复位释放期间，预计负载跳变高达 150 mA (dIDD)。

- 功率序列如图 3-4 列举如下
  - T1 至 T2 是指外部电源上升时基本电源和时钟基础设施组件可用的时间段。带隙和内部时钟源启动，根据 HWCFG[2:1,4,5,6] 和 TESTMODE 引脚决定供电模式。T1 至 T2 是指外部电源上升时基本电源和时钟基础设施组件可用的时间段。带隙和内部时钟源启动，根据 HWCFG[2:1,6] 引脚决定供电模式。这些事件在 T1 时 LVD 复位释放后启动。当两个输入电压 VEXT 和 VEVRSB 分别高于 VLVD RST5 和 VLVD RSTSB 电平时，LVD 复位被释放。内部预调节器 VDDPD 输出电压高于 VLVD RSTC 水平。
  - T2 指的是 EVRC 调节器软启动开始的时间点。PORST（输入）对 EVRC 输出没有任何影响，尽管 PORST 已置位且设备处于复位状态，调节器仍会继续产生相应的电压。产生的电压在 tSTR（数据手册参数）时间内呈软上升趋势，以避免过冲。
  - T3 指的是所有电源都高于其主要复位阈值（由 VRST5、VRST33 和 VRSTC 供电电压水平表示）的时间点。EVRC 调节器已启动。PORST（输出）不置位，并且 HWCFG[3:5] 引脚被 SCU 锁存在 PORST 上升沿。固件执行已启动。T1 和 T3 之间的时间记录为 tEVRstartup（数据手册参数）。
  - T4 指的是固件执行完成并且用户代码以 CPU0 的默认频率 100 MHz 开始执行的时间点。T0 和 T4 之间的时间记录为 tBP（数据手册参数）。
  - T5 指的是斜坡下降阶段期间至少一个外部提供或生成的电源（VDD、VDDP3 或 VEXT）降至其各自的初级欠压复位阈值以下的时间点。

## 3.13.1.3 外部供电模式 (d)


 图 3-5 外部供电模式 (d) -  $V_{EXT}$  和  $V_{DD}$  外部供电

$V_{EXT} = 5V$  且  $V_{DD}$  电源由外部供电。3.3V 由 EVR33 调节器内部产生。

- 外部电源  $V_{EXT}$  和  $V_{DD}$  可以在启动、上升和下降时间方面相互独立地上升或下降。电源轨的启动斜率应符合数据手册参数 SR。斜率定义为 0% 至 100% 电压电平之间的最大切向斜率。实际波形可能不同于规格书。预计在启动期间， $V_{EXT}$  会在  $V_{DD}$  轨之前上升。

如果 VDD 电源轨在 VEXT 之前上升；启动期间的 VDD 电源过冲应限制在工作电压范围内。

- 从外部调节器汲取电流的速率 ( $dI_{EXT}/dt$  或  $dI_{DD}/dt$ ) 在启动阶段被限制为最大 100 mA，建立时间为 100  $\mu$ s。
- 当 PORST (输入) 或 PORST (输出) 激活/置位时，PORST 激活/置位。
- PORST (输入) 有效意味着外部设备可通过将 PORST 引脚拉低，使复位保持有效。建议保持 PORST (输入) 有效，直到外部电源电压高于相应的主复位阈值。
- PORST (输出) 有效意味着  $\mu$ C 在内部发出复位信号并将 PORST 引脚驱动至低电平，从而将复位信号传播至外部设备。当三个电源域 (VDD、VDDP3 或 VEXT) 中至少有一个违反其主要欠压复位阈值时， $\mu$ C 会发出 PORST 置位 (输出) 信号。当所有电源均高于其主要复位阈值，且基本电源和时钟基础设施可用时， $\mu$ C 会发出 PORST 不置位 (输出) 信号。在 T3 复位释放期间，预计负载跳变高达 150 mA ( $dI_{DD}$ )。
- 功率序列如图 3-5 列举如下
  - T1 至 T2 是指外部电源上升时基本电源和时钟基础设施组件可用的时间段。带隙和内部时钟源启动。根据 HWCFG[2:1,4,5,6] 和 TESTMODE 引脚来决定供电模式。T1 至 T2 是指外部电源上升时基本电源和时钟基础设施组件可用的时间段。启动带隙和内部时钟源。根据 HWCFG[2:1,6] 引脚决定供电模式。这些事件在 T1 时 LVD 复位释放后启动。当两个输入电压 VEXT 和 VEVR3B 分别高于 VLVD RST5 和 VLVD RST5B 电平时，LVD 复位被释放。内部预调节器 VDDPD 输出电压高于 VLVD RSTC 水平。
  - T2 指的是 EVR33 调节器软启动开始的时间点。PORST (输入) 对 EVR33 输出没有任何影响，尽管 PORST 已置位且设备处于复位状态，调节器仍会继续产生相应的电压。产生的电压在  $t_{STR}$  (数据手册参数) 时间内呈软上升趋势，以避免过冲。
  - T3 指的是所有电源都高于其主要复位阈值 (由 VRST5、VRST33 和 VRSTC 供电电压水平表示) 的时间点。EVR33 稳压器已启动。PORST (输出) 不置位，并且 HWCFG[3:5] 引脚被 SCU 锁存在 PORST 上升沿。固件执行已启动。T1 和 T3 之间的时间记录为  $t_{EVRstartup}$  (数据手册参数)。
  - T4 指的是固件执行完成并且用户代码以 CPU0 的默认频率 100 MHz 开始执行的时间点。T0 和 T4 之间的时间记录为  $t_{BP}$  (数据手册参数)。
  - T5 指的是斜坡下降阶段期间至少一个外部提供或生成的电源 (VDD、VDDP3 或 VEXT) 降至其各自的初级欠压复位阈值以下的时间点。

### 3.13.1.4 外部供电模式 (h)

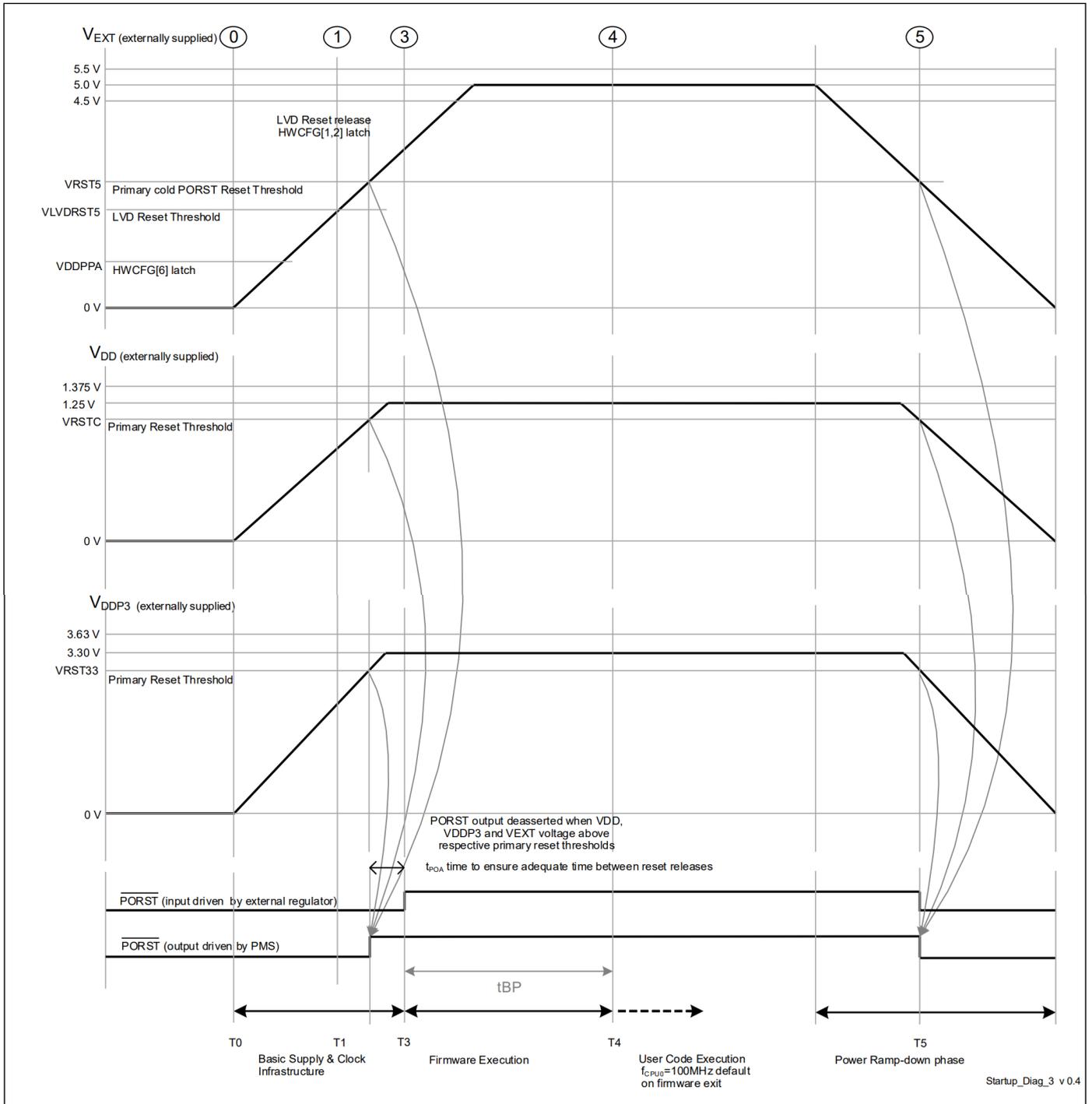


图 3-6 外部供电模式 (h) -  $V_{EXT}$ 、 $V_{DDP3}$  和  $V_{DD}$  外部供电

所有电源，即  $V_{EXT}$ 、 $V_{DDP3}$  和  $V_{DD}$  均由外部供电。

- 外部电源  $V_{EXT}$ 、 $V_{DDP3}$  和  $V_{DD}$  可能会根据启动、上升和下降时间而彼此独立地上升或下降。电源轨的启动斜率应符合数据手册参数 SR。斜率定义为 0% 至 100% 电压电平之间的最大切向斜率。实际波形可能不同于规格书。预计在启动期间， $V_{EXT}$  会在  $V_{DDP3}$  和  $V_{DD}$  轨之前上升。如果较小的电压轨在  $V_{EXT}$  之前上升，则启动期间的  $V_{DD}$  和  $V_{DDP3}$  电源过冲应限制在各自电压轨的工作电压范围内。

- 从外部调节器汲取电流的速率 ( $dI_{EXT}/dt$ ,  $dI_{DD}/dt$ 或 $dI_{DDP3}/dt$ ) 在启动阶段被限制为最大 100 mA, 建立时间为 100  $\mu$ s。
- 当 PORST (输入) 或 PORST (输出) 激活/置位时, PORST 激活/置位。
- PORST (输入) 有效意味着外部设备可通过将 PORST 引脚拉低, 使复位保持有效。建议保持 PORST (输入) 有效, 直到外部电源电压高于相应的主复位阈值。
- PORST (输出) 有效意味着  $\mu$ C 在内部发出复位信号并将 PORST 引脚驱动至低电平, 从而将复位信号传播至外部设备。当三个电源域 (VDD、VDDP3 或 VEXT) 中至少有一个违反其主要欠压复位阈值时,  $\mu$ C 会发出 PORST 置位 (输出) 信号。当所有电源均高于其主要复位阈值, 且基本电源和时钟基础设施可用时,  $\mu$ C 会发出 PORST 不置位 (输出) 信号。在 T3 复位释放期间, 预计负载跳变高达 150 mA ( $dI_{DD}$ )。
- 功率序列如图 3-6 列举如下
  - T1 至 T3 是指外部电源上升时基本电源和时钟基础设施组件可用的时间段。带隙和内部时钟源启动。根据 HWCFG[2:1,4,5,6] 和 TESTMODE 引脚来决定供电模式。T1 至 T2 是指外部电源上升时基本电源和时钟基础设施组件可用的时间段。带隙和内部时钟源启动, 根据 HWCFG[2:1,6] 引脚决定供电模式。这些事件在 T1 时 LVD 复位释放后启动。当两个输入电压 VEXT 和 VEVRSB 分别高于 VLVD RST5 和 VLVD RSTSB 电平时, LVD 复位被释放。内部预调节器 VDDPD 输出电压高于 VLVD RSTC 水平。
  - T3 指的是所有电源都高于其主要复位阈值 (由 VRST5、VRST33 和 VRSTC 供电电压水平表示) 的时间点。PORST (输出) 不置位, 并且 HWCFG[3:5] 引脚被 SCU 锁存在 PORST 上升沿。固件执行已启动。
  - T4 指的是固件执行完成并且用户代码以 CPU0 的默认频率 100 MHz 开始执行的时间点。T0 和 T4 之间的时间记录为 tBP (数据手册参数)。
  - T5 指的是斜坡下降阶段期间至少一个外部提供或生成的电源 (VDD、VDDP3 或 VEXT) 降至其各自的初级欠压复位阈值以下的时间点。

### 3.14 复位时间

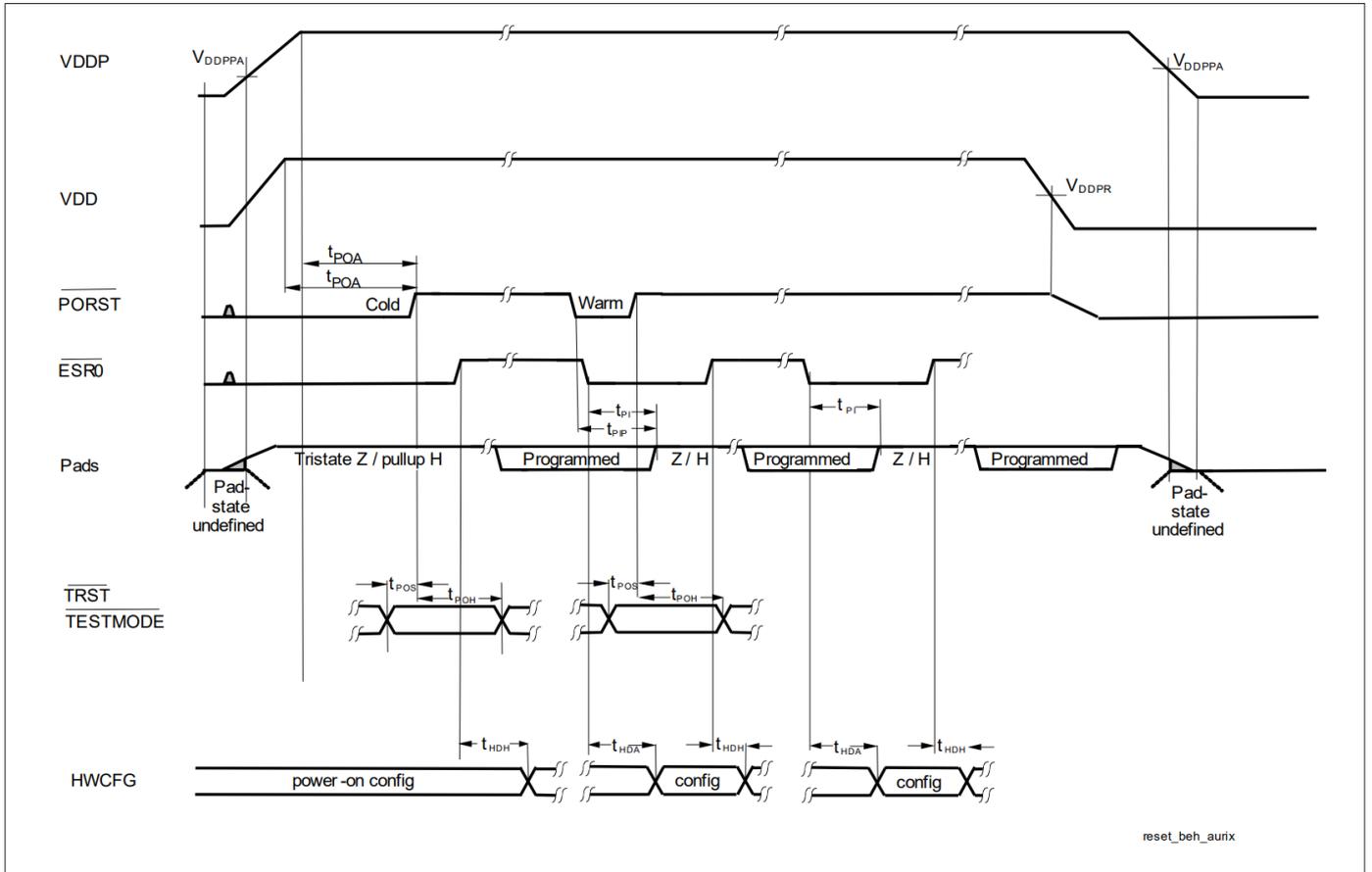
表 3-30 复位

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Application Reset Boot Time	$t_{B\ CC}$	-	-	400	$\mu\text{s}$	operating with max. frequencies, with valid BMI header
System Reset Boot Time	$t_{BS\ CC}$	-	-	1.1	ms	RAM initialization and HSM boot time are not included, with valid BMI header
Cold Power on Reset Boot Time <sup>1)</sup>	$t_{BP\ CC}$	-	-	3.1	ms	$dV_{EXT}/dT=1V/ms$ . $V_{EXT}>VLVDRST5$ . Boot time after Cold PORST including EVR ramp-up and Firmware execution time; RAM initialization and HSM boot time are not included.
		-	-	1.6	ms	Firmware execution time after PORST release without EVR ramp-up; RAM initialization and HSM boot time is not included
Minimum cold PORST reset hold time in case of power fail event issued by EVR primary monitors	$t_{EVRPOR\ CC}$	$10^{2)}$	-	-	$\mu\text{s}$	
PMS Infrastructure, EVRC and EVR33 overall start-up time till cold PORST reset release	$t_{EVRstartup\ CC}$	-	-	1	ms	$dV/dT=1V/ms$ . EVRC and EVR33 active
Minimum PORST active hold time externally after power supplies are stable at operating levels after start-up	$t_{POA\ SR}$	$1^{3)}$	-	-	ms	
Configurable PORST digital filter delay in addition to analog pad filter delay	$t_{PORSTDF\ CC}$	600	-	1200	ns	
Warm Reset Sequencing Delay	$t_{WARMRSTSEQ\ CC}$	-	-	180	$\mu\text{s}$	
HWCFG pins hold time from ESRO rising edge	$t_{HDH\ CC}$	$16 / f_{SPB}$	-	-	ns	

表 3-30 复位 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
HWCFG pins setup time to ESR0 rising edge	$t_{HDS}$ CC	0	-	-	ns	
Ports inactive after ESR0 reset active	$t_{PI}$ CC	$8000/f_{BAC}$ KT	-	$18000/f_{BA}$ CKT	s	
Ports inactive after PORST reset active	$t_{PIP}$ CC	-	-	150	ns	
Hold time from PORST rising edge	$t_{POH}$ SR	150	-	-	ns	
Setup time to PORST rising edge	$t_{POS}$ SR	0	-	-	ns	
Warm PORST reset boot time	$t_{BWP}$ CC	-	-	1.5	ms	without RAM initialization
LBIST execution time extending the boot time	$t_{LBIST}$ CC	-	-	6	ms	LBIST Configuration A; $1.2V \leq V_{DD}$
SCR reset boot time	$t_{SCR}$ CC	-	-	5	$\mu$ s	User Mode 0
		-	-	16	$\mu$ s	User Mode 1
		-	13.3	-	$\mu$ s	WDT double bit ECC, soft reset
Minimum external supplies hold time after warm reset assertion	$t_{SUPHOLD}$ CC	-	-	250	$\mu$ s	external supplies are $V_{EVRSB}$ , $V_{EXT}$ , $V_{FLEX}$ , $V_{EBU}$ , $V_{DDM}$ , $V_{DDP3}$ and $V_{DD}$

- 1) RAM 初始化另外增加 500 $\mu$ s。
- 2) 冷 PORST 复位由 uC 驱动，并维持在 VDDPPA 限制和绝对最大额定电压限制之间的扩展电压范围内。
- 3) 电源上升或电源恢复时的复位释放被延迟了 1.5% (默认值) 的电压滞后，该电压滞后高于 VEXT、VDDP3 和 VDD 轨上实施的欠压复位限值。这种机制有助于避免在电源缓慢上升期间，由于复位释放时压降/电流跳跃而导致的多个连续的冷 PORST 事件。



reset\_beh\_aunix

图 3-7 电源、焊盘和复位时间

## 3.15 EVR

表 3-31 EVR33 LDO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input voltage range	$V_{IN\ SR}$	3.60 <sup>1)</sup>	-	5.50	V	Normal RUN mode
		2.97 <sup>2)</sup>	-	5.50	V	Low voltage cranking mode
Output voltage operational range including load/line regulation and aging <sup>3)</sup>	$V_{OUT\ CC}$	2.97	3.3	3.63	V	Normal RUN mode
		2.60	3.3	3.63	V	Low voltage cranking mode; $I_{DDP3}=50mA$
Output $V_{DDX3}$ static voltage accuracy after trimming and aging without dynamic load/line regulation.	$V_{OUTT\ CC}$	3.225	3.3	3.375	V	Normal RUN mode
		2.78	3.3	3.375	V	Low voltage cranking mode; $I_{DDP3}=50mA$
Output buffer capacitance on $V_{OUT}$	$C_{OUT\ SR}$	1.45	2.2	3	$\mu F$	
Output buffer capacitor ESR	$C_{OUTESR\ SR}$	-	-	100 <sup>4)</sup>	mOhm	$f > 0.5MHz$ ; $f < 10MHz$
Maximum output current of the regulator	$I_{MAX\ CC}$	60 <sup>5)</sup>	-	-	mA	Normal RUN mode
Startup time	$t_{STR\ CC}$	-	500	1000	$\mu s$	Normal RUN mode
External $V_{IN}$ supply ramp <sup>6)</sup>	$dVin/dt\ SR$	-	1	-	V/ms	
Ripple on Output Voltage	$\Delta V_{OUTTC\ CC}$	-	-	33	mV	$V_{EXT} \geq 2.97V$ ; $V_{EXT} \leq 5.5V$ ; $I_{OUTTC} \geq 10mA$ ; $I_{OUTTC} \leq 60mA$ ; $\Delta V_{OUTTC} = (\text{peak to peak ripple} / 2)$
Load step response <sup>7)</sup>	$dVout/dIout\ CC$	-165	-	-	mV	Normal RUN mode; $dI=10$ to $60mA$ ; $dt=20ns$ ; $Tsettle=20us$
		-	-	165	mV	Normal RUN mode; $dI=60$ to $10mA$ ; $dt=20ns$ ; $Tsettle=20us$
		-180	-	-	mV	Low voltage cranking mode; $dI=10$ to $50mA$ ; $dt=20ns$ ; $Tsettle=20us$
		-	-	180	mV	Low voltage cranking mode; $dI=50$ to $10mA$ ; $dt=20ns$ ; $Tsettle=20us$

表 3-31 EVR33 LDO (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line step response	$dV_{out}/dV_{in}$ CC	-	-	40	mV	$dV_{in}/dT=1V/ms$ ; $dV=3.6$ to $5V$ ; $I_{MAX}=60mA$ ; $\Delta V_{OUTTC}$ is included
		-40	-	-	mV	$dV_{in}/dT=1V/ms$ ; $dV=5$ to $3.6V$ ; $I_{MAX}=60mA$ ; $\Delta V_{OUTTC}$ is included
		-	-	280	mV	$dV_{in}/dT=50V/ms$ ; $dV=3.6$ to $5V$ ; $I_{MAX}=60mA$
		-165	-	-	mV	$dV_{in}/dT=50V/ms$ ; $dV=5$ to $3.6V$ ; $I_{MAX}=60mA$

- 1) 最小输入电压中包含 300mV 的最大传输器件压差，以确保正常运行期间传输器件的最佳性能。
- 2) VEXT 输入电压降到 2.97V，将导致 VDDP3 输出电压降到 2.6V，如果在此之前已经将 Flash 切换到低性能模式，那么是可以正常工作的。
- 3) 如果使用 EVR33，则不允许使用外部感应负载。
- 4) 还建议从引脚到 EVR 输出电容器的电源走线电阻小于 100 mOhm。应在 Cout 之前靠近引脚的位置放置一个 100nF 的附加去耦电容。
- 5) 在低压模式（启动情况）下，使用片上传输装置时，IMAX 限制为 40 mA。在不使用 EVR33 的情况下，如果在电源上电时序中，3.3V 电压先于 5V 电压由外部稳压器供电，同时 5V VEXT 电压轨上电压不够时，则注入 3.3V VDDP3 电源轨的电流应限制在 500 mA 以内。
- 6) EVR 能够有效抵御 0 - 2.97 V 之间残余电压的上升。稳健性验证涵盖 0.5V/min 至 120V/ms 之间的 VEXT 电压斜坡范围。产生的电压本身在 tSTR 时间内遵循软上升趋势，以避免过冲。
- 7) 建立时间被定义为直到输出电压在单个器件平均值(VOUTT) 的+1% 范围内。

表 3-32 电源监视器

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Primary Undervoltage Reset threshold for $V_{DDP3}$ before trimming <sup>1)</sup>	$V_{RST33}$ CC	-	-	3.00	V	by reset release before EVR trimming on supply ramp-up
Primary undervoltage reset threshold for $V_{DD}$ before trimming	$V_{RSTC}$ CC	-	-	1.138	V	by reset release before trimming on supply ramp-up including 2 LSB voltage Hysteresis
$V_{EXT}$ primary undervoltage monitor accuracy after trimming <sup>2)</sup>	$V_{EXTPRIUV}$ CC	2.86	2.92	2.97	V	$V_{EXT}$ = Undervoltage cold PORST Primary Monitor Threshold
$V_{DDP3}$ primary undervoltage monitor accuracy after trimming <sup>2)</sup>	$V_{DDP3PRIUV}$ CC	2.86 <sup>3)</sup>	2.90	2.97	V	VDDP3 = Undervoltage cold PORST Primary Monitor Threshold
$V_{DD}$ primary undervoltage monitor accuracy after trimming <sup>2)</sup>	$V_{DDPRIUV}$ CC	1.08 <sup>3)</sup>	1.105	1.125	V	VDD = Undervoltage cold PORST Primary Monitor Threshold

表 3-32 电源监视器 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
EVR primary monitor measurement latency for a new supply value	$t_{PRIUV}$ CC	-	-	300	ns	The supply ramp / line jump slope is limited to 50V/ms for $V_{EXT}$ , $V_{DDP3}$ and $V_{DD}$ rails.
$V_{EXT}$ , $V_{DDM}$ & $V_{EVRSB}$ secondary supply monitor accuracy after trimming <sup>4) 5)</sup>	$V_{EXTMON}$ CC	3.2	3.3	3.4	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=3.3V=90h(O V,UV). EVRMONFILT.SWDFI L=1.
		4.5	4.6	4.7	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=4.6V=C8h(U V)/C9h(OV). EVRMONFILT.SWDFI L=1
		5.3	5.4	5.5	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=5.4V=EAh(U V)/ECh(OV). EVRMONFILT.SWDFI L=1
		4.9	5.0	5.1	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=5V=D9h(UV) /DAh(OV). EVRMONFILT.SWDFI L=1

表 3-32 电源监视器 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
$V_{DDP3}$ secondary supply monitor accuracy after trimming <sup>5)</sup>	$V_{DDP3MON}$ CC	2.97	3.035	3.1	V	EVR33xxVAL monitoring threshold=3.035V=CBh (UV)/CCh(OV). EVRMONFILT.EVR33 FIL = 3.
		3.235	3.30	3.365	V	EVR33xxVAL monitoring threshold=3.3V=DDh( OV, UV). EVRMONFILT.EVR33 FIL = 3.
		3.5	3.565	3.63	V	EVR33xxVAL monitoring threshold=3.565V=EEh (UV)/EFh(OV). EVRMONFILT.EVR33 FIL = 3.
$V_{DD}$ & $V_{DDPD}$ secondary supply monitor accuracy after trimming <sup>5)</sup>	$V_{DDMON}$ CC	1.125	1.15	1.175	V	EVRCxxVAL & PRExxVAL monitoring threshold=1.15V=C7h( UV )/C8h(OV). EVRMONFILT.EVRCFIL = 1.
		1.225	1.25	1.275	V	EVRCxxVAL & PRExxVAL monitoring threshold=1.25V=D9h( OV ,UV). EVRMONFILT.EVRCFIL = 1.
		1.325	1.35	1.375	V	EVRCxxVAL & PRExxVAL monitoring threshold=1.35V=EAh( UV )/EBh(OV). EVRMONFILT.EVRCFIL = 1.
$V_{EXT}$ LVD Primary undervoltage reset Monitor threshold	$V_{LVDRST5}$ CC	2.3	-	2.72	V	Power-down
		2.4	-	2.75	V	Power-up
$V_{EVRSB}$ LVD Primary undervoltage reset Monitor threshold	$V_{LVDRSTSB}$ CC	2.18	-	2.47	V	Power-down
		2.21	-	2.5	V	Power-up
$V_{EXT}$ and $V_{EVRSB}$ PBIST primary overvoltage Monitor threshold	$V_{PBIST5}$ CC	5.63	-	-	V	

表 3-32 电源监视器 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Primary undervoltage reset threshold for $V_{EXT}$ before trimming	$V_{RST5\ CC}$	-	-	3.0	V	by last cold PORST release on supply ramp-up including voltage hysteresis.
EVR secondary monitor measurement latency for all 6 supply rails	$t_{MON\ CC}$	-	-	3.2	$\mu s$	HPOSC and SHPBG bandgap trimmed. Filter inactive.

- 1) 电源上升时的复位释放在达到欠压复位阈值后会延迟 20-40 微秒的时间，并且电压滞后会高于欠压复位限值 1.5%。这种机制有助于避免在电源缓慢上升期间，由于复位释放时压降/电流跳跃而导致的多个连续的冷 PORST 事件。引脚的复位限制为 2.97V，适用于 EVR33 内部产生 3.3V 的情况。如果外部提供 3.3V 电源，则键合线压降将导致 VDDP3 引脚上电压达到 3.0V 就复位。
- 2) 监测器公差构成了带隙和 ADC 在工艺、电压和温度操作范围内的固有变化。VxxPRIUV 参数在生产过程中经过单独测试，与 VxxPRIUV 限值有 +-1% 的容差。所有电压均在引脚上测量。
- 3) VRSTxx 参数仅与第一次冷 PORST 释放相关。随后，在器件以完整性能使用之前，复位电平由固件调整并反映为 VxxPRIUV 参数。冷 PORST 通过所有主监视器上的电压滞后释放，以避免连续的 PORST 切换行为。
- 4) 如果应用程序使用 3.3V 单电源（单电源模式 (e)，即当 VEXT 与 VDDP3 短接时，建议在通道 VDDP3 上使用二次电源监控，因为 VDDP3MON 参数的精度更高。
- 5) 对于未提供监测器电压电平的条件，OV 和 UV 阈值可以根据给定的点通过线性插值或外推生成。

表 3-33 供电斜坡

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
External $V_{EXT}$ & $V_{EVR5B}$ supply ramp-up and ramp-down slope <sup>1) 2) 3)</sup>	$dV_{EXT}/dt$ SR	8.3E-6	1	100	V/ms	
External $V_{DDP3}$ supply ramp-up and ramp-down slope <sup>1) 3)</sup>	$dV_{DDP3}/dt$ SR	8.3E-6	1	100	V/ms	
External $V_{DD}$ supply ramp-up and ramp-down slope <sup>1) 3)</sup>	$dV_{DD}/dt$ SR	8.3E-6	1	100	V/ms	
External $V_{DDM}$ supply ramp-up and ramp-down slope <sup>1) 3)</sup>	$dV_{DDM}/dt$ SR	8.3E-6	1	100	V/ms	

- 1) 该器件具有很强的抗残余电压上升能力，对于 VEXT、VEVR5B、VDDP3 和 VDDM，电压上升范围为 0 - 2.97V，对于 VDD，电压上升范围为 0-1V。稳健性验证涵盖 0.5V/min 至 120V/ms 之间的 VEXT 电压斜坡范围。
- 2) 在使用 EVR33 或 EVRC 的情况下也有效。产生的电压本身在 tSTR 时间内遵循软上升趋势，以避免过冲。
- 3) 斜率定义为 0% 至 100% 电压电平之间的最大切向斜率。实际波形可能不同于规格书。

TC39x 允许最多 1000000 次电源循环，符合“电源斜坡”表中定义的限制，且对可靠性没有任何限制。

表 3-34 EVRC SMPS

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input $V_{EXT}$ Voltage range	$V_{IN SR}$	2.97	-	5.5	V	Start-up $V_{EXT}$ voltage > 2.6 V
SMPS regulator output voltage range including load/line regulation and aging	$V_{DDDC CC}$	1.125	-	1.375	V	$V_{EXT} \geq 2.97V$ ; $V_{EXT} \leq 5.5V$ ; $I_{DDDC} \geq 1mA$ ; $I_{DDDC} \leq 1.5A$ ; untrimmed
SMPS regulator static voltage output accuracy after trimming without dynamic load/line regulation.	$V_{DDDC T CC}$	1.225	1.25	1.275	V	$V_{EXT} \geq 2.97V$ ; $V_{EXT} \leq 5.5V$ ; $I_{DDDC} \geq 1mA$ ; $I_{DDDC} \leq 1.5A$
Programmable switching frequency	$f_{DCDC SR}$	1.6	1.82	2.0	MHz	Start-up frequency switches from 500 KHz in open loop operation to 1.82 MHz in closed loop Operation.
		-	0.8	-	MHz	Start-up frequency switches from 500 KHz in open loop operation to 1.82 MHz in closed loop Operation. 0.8 MHz to be set in SW.
Startup time	$t_{STRDC CC}$	-	-	900	$\mu s$	SMPS Start-up Mode. It is defined between $V_{EXTPRIUV}$ reset threshold till PORST release, on condition that all other PORST requirements were released before. $I_{START} < 700mA$ .
Switching frequency modulation spread	$\Delta f_{DCSPR CC}$	-	1.8%	-	MHz	
Maximum ripple at $I_{MAX}$	$\Delta V_{DDDC CC}$	-	-	16	mV	$V_{EXT} \geq 2.97V$ ; $V_{EXT} \leq 5.5V$ ; $I_{DDDC} \geq 300mA$ ; $I_{DDDC} \leq 1.5A$ ; $\Delta V_{DDDC} = (\text{Peak to Peak ripple} / 2)$
No load current consumption of SMPS regulator	$I_{DCNL CC}$	-	15	19	mA	$f_{DCDC} = 1.82MHz$ ; $I_{DDDC} = I_{SLEEP}$ ; $V_{EXT} > 2.97V$ ; $T_j = 25^\circ C$
		-	5	-	mA	LPM mode; $I_{DDDC} = I_{SLEEP}$ ; $V_{EXT} > 2.97V$ ; $T_j = 25^\circ C$

表 3-34 EVRC SMPS (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SMPS regulator load transient response	$dV_{DDDC}/dl_{OUT\ CC}$	-50	-	87	mV	$dI < -450mA$ ; $I_{DDDC}=500-1500mA$ ; $t_r=0.1\mu s$ ; $t_f=0.1\mu s$ ; $V_{DDDC}=1.25V$ ; $T_{settle}=100\ \mu s$
		-100	-	145	mV	$dI < -700mA$ ; $I_{DDDC}=750-1500mA$ ; $t_r=0.1\mu s$ ; $t_f=0.1\mu s$ ; $V_{DDDC}=1.25V$ ; $T_{settle}=100\ \mu s$
		-26	-	26	mV	$dI < 100mA$ ; $I_{DDDC}=50-1500mA$ ; $t_r=0.1\mu s$ ; $t_f=0.1\mu s$ ; $V_{DDDC}=1.25V$ ; $T_{settle}=20\mu s$ ;
Maximum output current	$I_{MAX\ CC}$	100	-	-	mA	LPM mode. Typical current in LPM Mode = $I_{SLEEP}$
		1.5	-	-	A	limited by thermal constraints and component choice
SMPS regulator line transient response	$dV_{DDDC}/dV_{IN\ CC}$	-75	-	75	mV	$dV/dT=120V/ms$ ; $dV < 2.97 - 5.5V$ ; $I_{DDDC}=50-1500mA$ ;
		-12.5	-	12.5	mV	$dV/dT=1V/ms$ ; $dV < 2.97 - 5.5V$ ; $I_{DDDC}=50-1500mA$ ;
SMPS regulator efficiency	$n_{DC\ CC}$	-	80	-	%	$V_{IN}=3.3V$ ; $I_{DDDC}=1500mA$ ; $f_{DCDC}=1.82MHz$
		-	75	-	%	$V_{IN}=5V$ ; $I_{DDDC}=1500mA$ ; $f_{DCDC}=1.82MHz$
Input Synchronisation frequency	$f_{DCDC\ SYNC\ SR}$	1.6	1.82	2.0	MHz	

表 3-35 EVRC SMPS 外部组件

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
External output capacitor value <sup>1)</sup>	$C_{OUT\ SR}$	20.8	32	43.2	$\mu F$	$I_{DDDC}=1.5A$ ; $f_{DDDC} = 0.8MHz$
		15.4	22	29.7	$\mu F$	$I_{DDDC}=1.5A$ ; $f_{DDDC} = 1.82MHz$

表 3-35 EVRC SMPS 外部组件 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
External output capacitor ESR	$C_{OUT\_ESR}$ SR	-	-	50	mOhm	$f \geq 0.5\text{MHz}$ ; $f \leq 10\text{MHz}$
		-	-	100	Ohm	$f = 10\text{Hz}$
External input capacitor value <sup>1)</sup>	$C_{IN\_SR}$	6.5	10	13.5	$\mu\text{F}$	$I_{DDDC} = 1.5\text{A}$
External input capacitor ESR	$C_{IN\_ESR}$ SR	-	-	50	mOhm	$f \geq 0.5\text{MHz}$ ; $f \leq 10\text{MHz}$
		-	-	100	Ohm	$f = 100\text{Hz}$
External inductor value	$L_{DC}$ SR	3.29	4.7	6.11		$f_{DCDC} = 0.8\text{MHz}$
		2.31	3.3	4.29	$\mu\text{H}$	$f_{DCDC} = 1.82\text{MHz}$
External inductor DCR	$L_{DC\_DCR}$ SR	-	-	0.2	Ohm	
P + N-channel MOSFET logic level	$V_{LL}$ SR	-	-	2.5	V	
P + N-channel MOSFET drain source breakdown voltage	$ V_{BR\_DS} $ SR	+7	-	-	V	NMOS - $V_{GS} = 0$ .
		-	-	-7	V	PMOS - $V_{GS} = 0$ .
P + N-channel MOSFET drain source ON-state resistance	$R_{ON}$ SR	-	150	-	mOhm	$I_{DDDC} = 1.5\text{A}$ ; $ V_{GS}  = 2.5\text{V}$ ; $T_A = 25^\circ\text{C}$
P + N-channel MOSFET Gate Charge	$Q_G$ SR	-	-	8	nC	$I_{DDDC} = 1.5\text{A}$ ; NMOS- $ V_{GS}  = 5\text{V}$ ; 1.5A pulsed drain current
		-8	-	-	nC	$I_{DDDC} = 1.5\text{A}$ ; PMOS- $ V_{GS}  = 5\text{V}$ ; 1.5A pulsed drain current
External Inductor Saturation Current Margin	$\Delta I_{SAT}$ SR	400	-	-	mA	The saturation current of the coil must be larger than $I_{DDDC} + \Delta I_{SAT}$
P + N-channel MOSFET Gate threshold voltage	$V_{GTH}$ SR	-	1	-	V	NMOS
		-	-1	-	V	PMOS
N-channel MOSFET reverse diode forward voltage	$V_{RDN}$ SR	-	0.8	-	V	

1) 电容器最小-最大范围代表典型的  $\pm 35\%$  公差, 包括直流偏置效应。从电容器到电源或接地轨的走线电阻应限制为 25 mOhm。

### 3.16 系统锁相环 (SYS\_PLL)

表 3-36 PLL 系统

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DCO Input frequency range	$f_{REF} CC$	10	-	40	MHz	
Modulation Amplitude	$MA CC$	0	-	2	%	
Peak Period jitter	$DP CC$	-200	-	200	ps	without modulation (PLL output frequency)
Peak Accumulated Jitter	$D_{PP} CC$	-5	-	5	ns	without modulation
Total long term jitter	$J_{TOT} CC$	-	-	11.5	ns	including modulation; MA 1.25%; $f_{REF}$ 20MHz
System frequency deviation	$f_{SYSD} CC$	-	-	0.01	%	with active modulation
DCO frequency range	$f_{DCO} CC$	400	-	800	MHz	
PLL lock-in time	$t_L CC$	4	-	100	$\mu s$	

注释：如果每个引脚的电容负载在最大驱动器和锐边的情况下不超过  $C_L = 20 \text{ pF}$ ，则指定的PLL 抖动值有效。

注释：电源电压上的最大峰峰值噪声限制为噪声频率低于300 KHz时， $V_{pp} = 100 \text{ mV}$ ；噪声频率高于300 KHz时， $V_{pp} = 40 \text{ mV}$ 。这些条件可以通过在尽可能靠近电源引脚的位置适当阻断电源电压，并使用PCB 电源层和接地层来实现。

## 3.17 外设锁相环 (PER\_PLL)

表 3-37 PLL 外设

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Peak Accumulated jitter at SYSCLK pin	$D_{PP} CC$	-1000	-	1000	ps	Peak only
Peak accumulated jitter	$D_{PPI} CC$	-700	-	700	ps	Peak only
RMS Accumulated jitter	$D_{RMS} CC$	-100	-	100	ps	measured over 1 $\mu s$ ; $f_{REF} = 20$ MHz and $f_{DCO} = 640$ MHz or $f_{REF} = 25$ MHz and $f_{DCO} = 800$ MHz
Peak Period jitter	$DP CC$	-200	-	200	ps	$f_{DCO} = 640$ MHz or $f_{DCO} = 800$ MHz
Absolute RMS jitter (PLL out)	$J_{ABS10} CC$	-125	-	125	ps	$f_{REF} = 10$ MHz; $f_{DCO} = 640$ MHz
Absolute RMS jitter (PLL out)	$J_{ABS20} CC$	-85	-	85	ps	$f_{REF} = 20$ MHz; $f_{DCO} = 640$ MHz
Absolute RMS jitter (PLL out)	$J_{ABS25} CC$	-85	-	85	ps	$f_{REF} = 25$ MHz; $f_{DCO} = 800$ MHz
DCO frequency range	$f_{DCO} CC$	400	-	800	MHz	
DCO input frequency range	$f_{REF} CC$	10	-	40	MHz	
PLL lock-in time	$t_L CC$	4	-	100	$\mu s$	

注释: 如果每个引脚的电容负载在最大驱动器和锐边的情况下不超过  $C_L = 20$  pF, 则指定的PLL 抖动值有效。

注释: 电源电压上的最大峰峰值噪声限制为噪声频率低于300 KHz时,  $V_{PP} = 100$  mV; 噪声频率高于300 KHz时,  $V_{PP} = 40$  mV。这些条件可以通过在尽可能靠近电源引脚的位置适当阻断电源电压, 并使用PCB 电源层和接地层来实现。

### 3.18 交流规格

所有交流参数均由3.4章节中定义的完整操作范围指定，除非在“注释/测试条件”栏中另有说明。

除非图中另有说明，否则时间定义遵循以下准则：

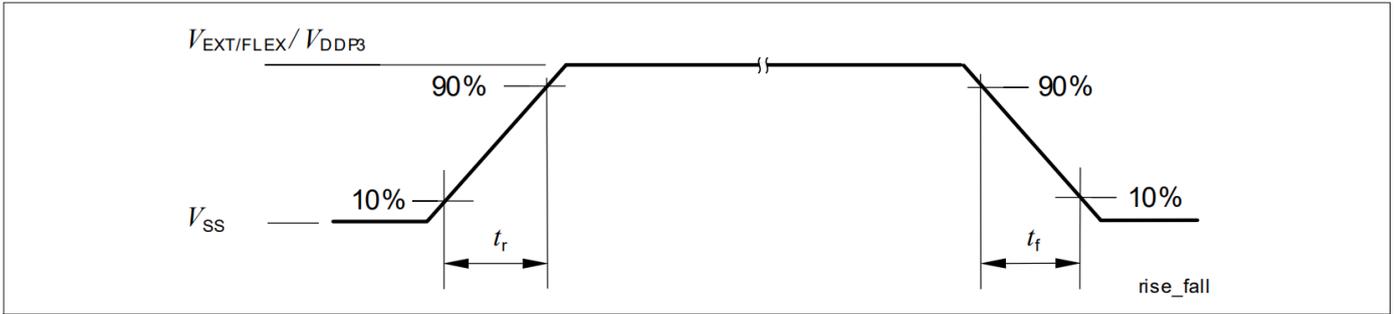


图 3-8 上升/下降时间的定义

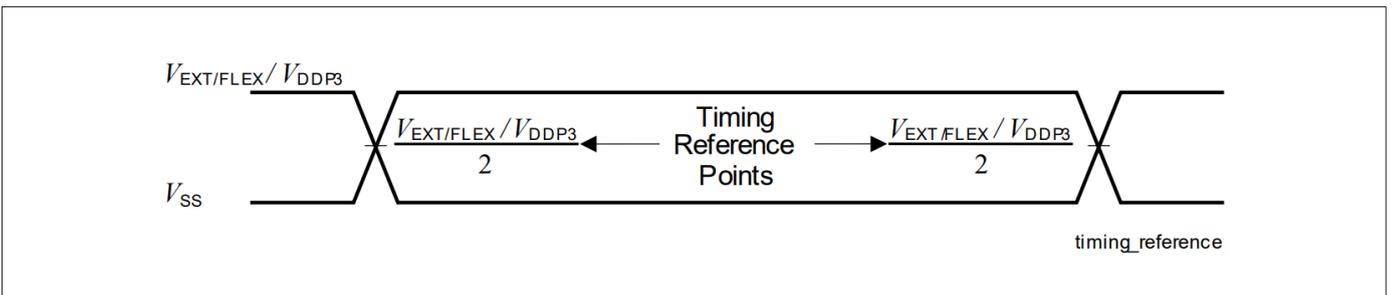


图 3-9 时间基准点定义

### 3.19 JTAG参数

以下参数适用于通过 JTAG 调试接口进行通信。JTAG模块完全符合IEEE1149.1-2000。

表 3-38 JTAG

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	$t_1$ SR	50	-	-	ns	
TCK high time	$t_2$ SR	10	-	-	ns	
TCK low time	$t_3$ SR	10	-	-	ns	
TCK clock rise time	$t_4$ SR	-	-	4	ns	
TCK clock fall time	$t_5$ SR	-	-	4	ns	
TDI/TMS setup to TCK rising edge	$t_6$ SR	6.0	-	-	ns	
TDI/TMS hold after TCK rising edge	$t_7$ SR	6.0	-	-	ns	
TDO valid after TCK falling edge (propagation delay)	$t_8$ CC	3.0	-	-	ns	$C_L \leq 20\text{pF}$
		-	-	25	ns	$C_L \leq 50\text{pF}$
TDO hold after TCK falling edge	$t_{18}$ CC	2	-	-	ns	
TDO high impedance to valid from TCK falling edge	$t_9$ CC	-	-	25	ns	$C_L \leq 50\text{pF}$
TDO valid output to high impedance from TCK falling edge	$t_{10}$ CC	-	-	25	ns	$C_L \leq 50\text{pF}$

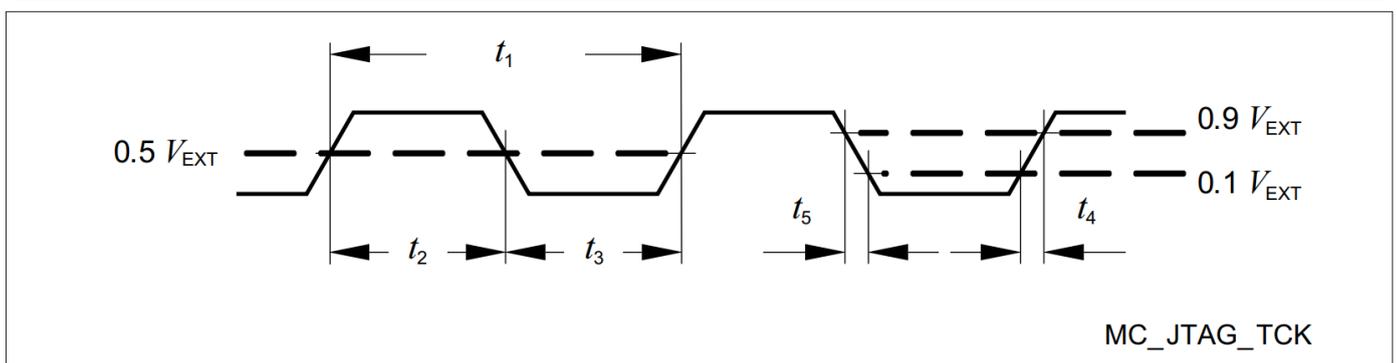


图3-10测试时钟时序 (TCK)

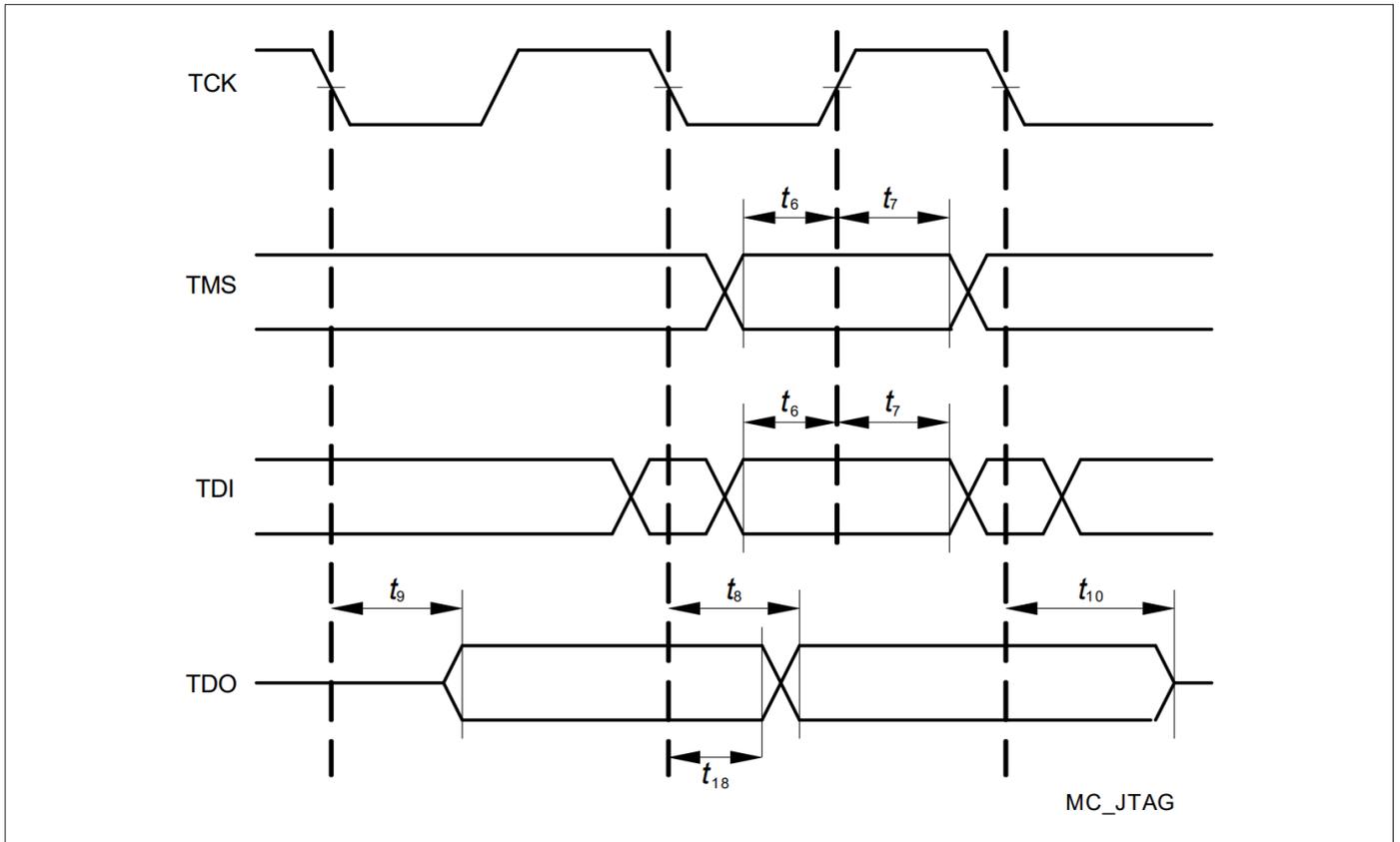


图 3-11 JTAG 时序

### 3.20 DAP 参数

以下参数适用于通过 DAP 调试接口进行通信。

表 3-39 DAP

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock rise time	$t_{14}$ SR	-	-	1	ns	f=160MHz
		-	-	4	ns	f=40MHz
		-	-	2	ns	f=80MHz
DAP0 clock fall time	$t_{15}$ SR	-	-	1	ns	f=160MHz
		-	-	4	ns	f=40MHz
		-	-	2	ns	f=80MHz
DAP1 setup to DAP0 rising edge	$t_{16}$ SR	4	-	-	ns	
		5	-	-	ns	f=40MHz
DAP1 hold after DAP0 rising edge	$t_{17}$ SR	2	-	-	ns	
DAP1 valid per DAP0 clock period	$t_{19}$ CC	4	-	-	ns	$C_L=20\text{pF}$ ; f=160MHz
		8	-	-	ns	$C_L=20\text{pF}$ ; f=80MHz
		10	-	-	ns	$C_L=50\text{pF}$ ; f=40MHz
DAP0 high time	$t_{12}$ SR	2	-	-	ns	
DAP0 low time	$t_{13}$ SR	2	-	-	ns	
DAP0 clock period	$t_{11}$ SR	6.25	-	-	ns	

表 3-40 SCR DAP

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock rise time	$t_{14}$ SR	-	-	8	ns	f=20MHz
DAP0 clock fall time	$t_{15}$ SR	-	-	8	ns	f=20MHz
DAP1 setup to DAP0 rising edge	$t_{16}$ SR	10	-	-	ns	
DAP1 hold after DAP0 rising edge	$t_{17}$ SR	10	-	-	ns	
DAP1 valid per DAP0 clock period	$t_{19}$ CC	30	-	-	ns	$C_L=20\text{pF}$ ; f=20MHz
DAP0 high time	$t_{12}$ SR	15	-	-	ns	
DAP0 low time	$t_{13}$ SR	15	-	-	ns	
DAP0 clock period	$t_{11}$ SR	50	-	-	ns	

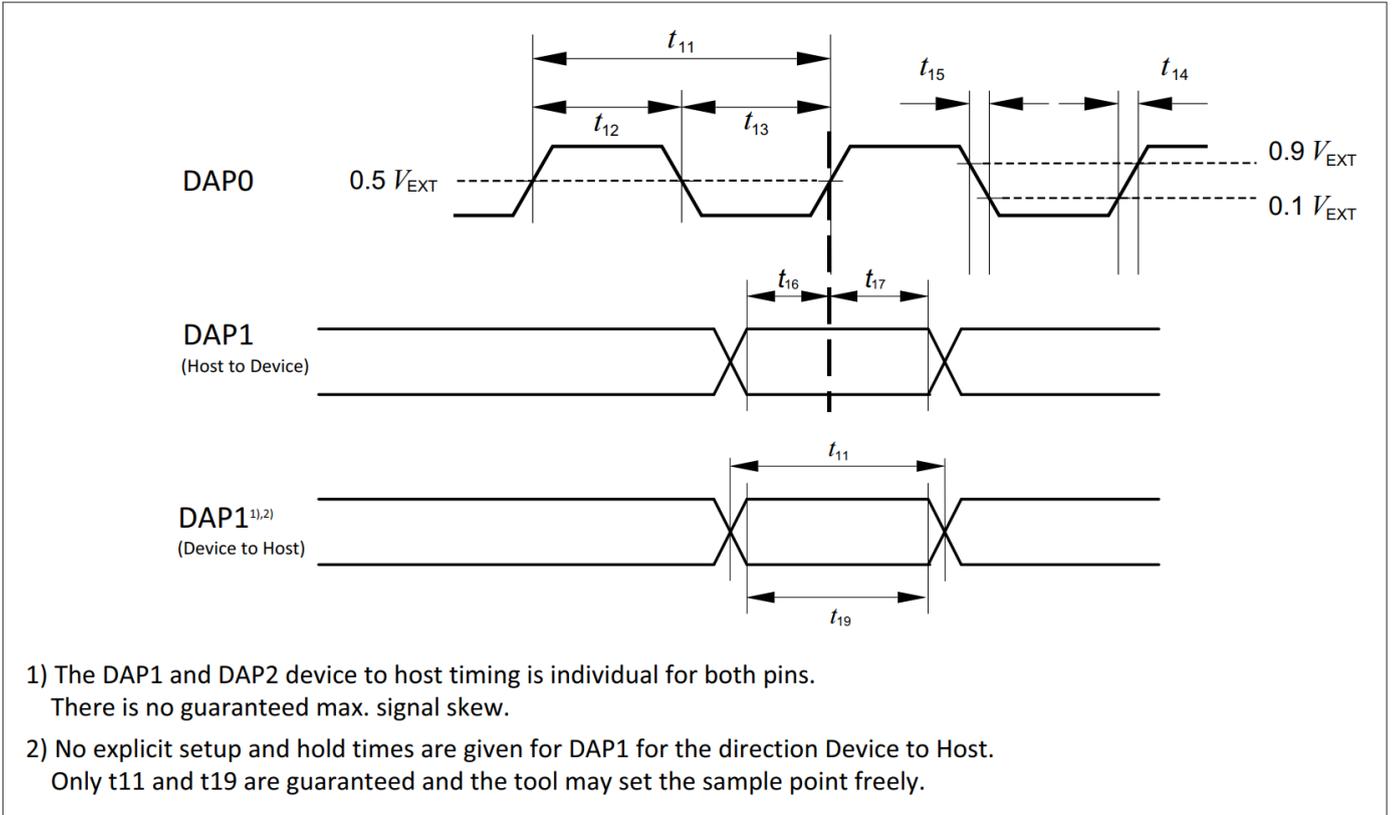


图 3-12 DAP 时序

注释: DAP1 和 DAP2 器件对主控器件的两个引脚都是单独的。没有确定的最大值信号偏差。

### 3.21 ASCLIN SPI 主时序

本节定义了 TC39x 中 ASCLIN 的时序。

注释：焊盘不对称已包含在以下时序中。

表 3-41 主模式强尖锐 (ss) 输出焊盘

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ASCLKO clock period	$t_{50}$ CC	20	-	-	ns	$C_L=25\text{pF}$
Deviation from ideal duty cycle	$t_{500}$ CC	-2	-	2	ns	$C_L=25\text{pF}$
MTSR delay from ASCLKO shifting edge	$t_{51}$ CC	-3.5	-	3.5	ns	$C_L=25\text{pF}$
ASLSON delay from the first ASCLKO edge	$t_{510}$ CC	-3	-	3.5	ns	$C_L=25\text{pF}$
MRST setup to ASCLKO latching edge	$t_{52}$ SR	25	-	-	ns	$C_L=25\text{pF}$
MRST hold from ASCLKO latching edge	$t_{53}$ SR	-2	-	-	ns	$C_L=25\text{pF}$

表 3-42 主模式强中型 (sm) 输出焊盘

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ASCLKO clock period	$t_{50}$ CC	50	-	-	ns	$C_L=50\text{pF}$
Deviation from ideal duty cycle	$t_{500}$ CC	-5	-	5	ns	$C_L=50\text{pF}$
MTSR delay from ASCLKO shifting edge	$t_{51}$ CC	-7	-	7	ns	$C_L=50\text{pF}$
ASLSON delay from the first ASCLKO edge	$t_{510}$ CC	-7	-	7	ns	$C_L=50\text{pF}$
MRST setup to ASCLKO latching edge	$t_{52}$ SR	35	-	-	ns	$C_L=50\text{pF}$
MRST hold from ASCLKO latching edge	$t_{53}$ SR	-5	-	-	ns	$C_L=50\text{pF}$

表 3-43 主模式中型 (m) 输出焊盘

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ASCLKO clock period	$t_{50}$ CC	160	-	-	ns	$C_L=50\text{pF}$
Deviation from ideal duty cycle	$t_{500}$ CC	-10	-	10	ns	$C_L=50\text{pF}$
MTSR delay from ASCLKO shifting edge	$t_{51}$ CC	-20	-	20	ns	$C_L=50\text{pF}$
ASLSON delay from the first ASCLKO edge	$t_{510}$ CC	-20	-	20	ns	$C_L=50\text{pF}$

表 3-43 主模式中型 (m) 输出焊盘 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MRST setup to ASCLKO latching edge	$t_{52}$ SR	80	-	-	ns	$C_L=50\text{pF}$
MRST hold from ASCLKO latching edge	$t_{53}$ SR	-15	-	-	ns	$C_L=50\text{pF}$

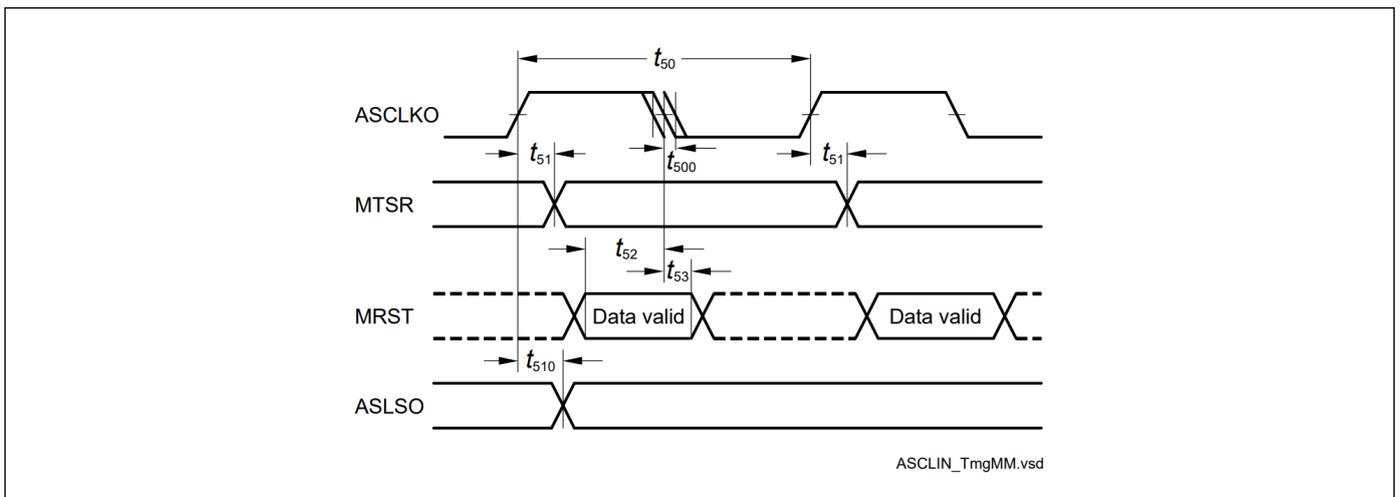


图 3-13 ASCLIN SPI 主机时序

### 3.22 QSPI 时序、主模式和从模式

本节定义了 TC39x 中 QSPI 的时序。

假设 SCLKO、MSTR 和 SLSO 焊盘具有相同的焊盘设置：

注释：焊盘不对称已包含在以下时序中。

表 3-44 主模式时序，LVDS 数据和时钟输出焊盘

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period	$t_{50}$ CC	20 <sup>1)</sup>	-	-	ns	CL=25pF
Deviation from the ideal duty cycle	$t_{500}$ CC	-1 <sup>1)</sup>	-	1 <sup>1)</sup>	ns	CL=25pF
MSTR delay from SCLKO shifting edge	$t_{51}$ CC	-3 <sup>1)</sup>	-	4 <sup>1)</sup>	ns	CL=25pF
SLSOn deviation from the ideal programmed position	$t_{510}$ CC	-4 <sup>1)</sup>	-	5.5 <sup>1)</sup>	ns	$C_L=25$ pF, driver strength ss
		-10 <sup>1)</sup>	-	10 <sup>1)</sup>	ns	$C_L=25$ pF, driver strength sm
		-30 <sup>1)</sup>	-	30 <sup>1)</sup>	ns	$C_L=25$ pF, driver strength m
MRST setup to SCLK latching edge	$t_{52}$ SR	18 <sup>1)</sup>	-	-	ns	CL=25pF; valid for LVDS Input pads of QSPI2 only
		19.5 <sup>1)</sup>	-	-	ns	CL=25pF; valid for LVDS Input pads of QSPI4 only
MRST hold from SCLK latching edge	$t_{53}$ SR	-1 <sup>1)</sup>	-	-	ns	CL=25pF; valid for LVDS Input pads only

1) 条件列表中定义的负载 ( $C_L=25$ pF) 是针对单端信号 SLSO 的负载定义，并不旨在在差分信号线内添加额外负载。对于单端信号，负载定义定义了 PCB 布局上信号的最大长度。对于 LVDS 焊盘，适用 IEEE Std 1596.3-1996 负载定义。

表 3-45 主模式强尖锐 (ss) 输出焊盘

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period	$t_{50}$ CC	50	-	-	ns	CL=25pF
Deviation from the ideal duty cycle	$t_{500}$ CC	-2	-	2	ns	CL=25pF
MSTR delay from SCLKO shifting edge	$t_{51}$ CC	-4	-	5	ns	CL=25pF
SLSOn deviation from the ideal programmed position	$t_{510}$ CC	-4	-	5	ns	CL=25pF
MRST setup to SCLK latching edge	$t_{52}$ SR	25 <sup>1)2)</sup>	-	-	ns	CL=25pF
MRST hold from SCLK latching edge	$t_{53}$ SR	-2 <sup>1)2)</sup>	-	-	ns	CL=25pF

## 电气规格 QSPI 时序、主从模式

- 1) 为了补偿平均片上延迟, QSPI 模块提供了位域 ECONZ.A、B 和 C。
- 2) 建立和保持时间对于输入焊盘阈值的两种设置均有效: TTL 和 AL。

表 3-46 主模式强中型 (sm) 输出焊盘

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period	$t_{50} CC$	50	-	-	ns	CL=50pF
Deviation from the ideal duty cycle	$t_{500} CC$	-5	-	5	ns	CL=50pF
MISR delay from SCLKO shifting edge	$t_{51} CC$	-7	-	7	ns	CL=50pF
SLSON deviation from the ideal programmed position	$t_{510} CC$	-7	-	7	ns	CL=50pF
MRST setup to SCLK latching edge	$t_{52} SR$	35 <sup>1)2)</sup>	-	-	ns	CL=50pF
MRST hold from SCLK latching edge	$t_{53} SR$	-5 <sup>1)2)</sup>	-	-	ns	CL=50pF

- 1) 为了补偿平均片上延迟, QSPI 模块提供了位域 ECONZ.A、B 和 C。
- 2) 建立和保持时间对于输入焊盘阈值的两种设置均有效: TTL 和 AL。

表 3-47 主模式中等 (m) 输出焊盘

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period	$t_{50} CC$	160	-	-	ns	CL=50pF
Deviation from the ideal duty cycle	$t_{500} CC$	-10	-	10	ns	CL=50pF
MISR delay from SCLKO shifting edge	$t_{51} CC$	-20	-	20	ns	CL=50pF
SLSON deviation from the ideal programmed position	$t_{510} CC$	-20	-	20	ns	CL=50pF
MRST setup to SCLK latching edge	$t_{52} SR$	80 <sup>1)2)</sup>	-	-	ns	CL=50pF
MRST hold from SCLK latching edge	$t_{53} SR$	-15 <sup>1)2)</sup>	-	-	ns	CL=50pF
		-13 <sup>1)2)</sup>	-	-	ns	CL=50pF; SCR SSC

- 1) 为了补偿平均片上延迟, QSPI 模块提供了位域 ECONZ.A、B 和 C。
- 2) 建立和保持时间对于输入焊盘阈值的两种设置均有效: TTL 和 AL。

表 3-48 从模式时序

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLK clock period	$t_{54} SR$	$4 \times T_{MAX}$	-	-	ns	
SCLK duty cycle	$t_{55}/t_{54} SR$	40	-	60	%	

表 3-48 从模式时序 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MTSR setup to SCLK latching edge	$t_{56}$ SR	6	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
MTSR hold from SCLK latching edge	$t_{57}$ SR	4	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
SLSI setup to first SCLK shift edge	$t_{58}$ SR	4	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
SLSI hold from last SCLK latching edge	$t_{59}$ SR	3	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
MRST delay from SCLK shift edge	$t_{60}$ CC	5	-	35	ns	driver = strong edge = medium ; $C_L=50\text{pF}$
		2	-	24	ns	driver = strong edge = sharp ; $C_L=50\text{pF}$
		15	-	80	ns	medium driver ; $C_L=50\text{pF}$
		14	-	-	ns	medium driver ; $C_L=50\text{pF}$ ; SCR SSC

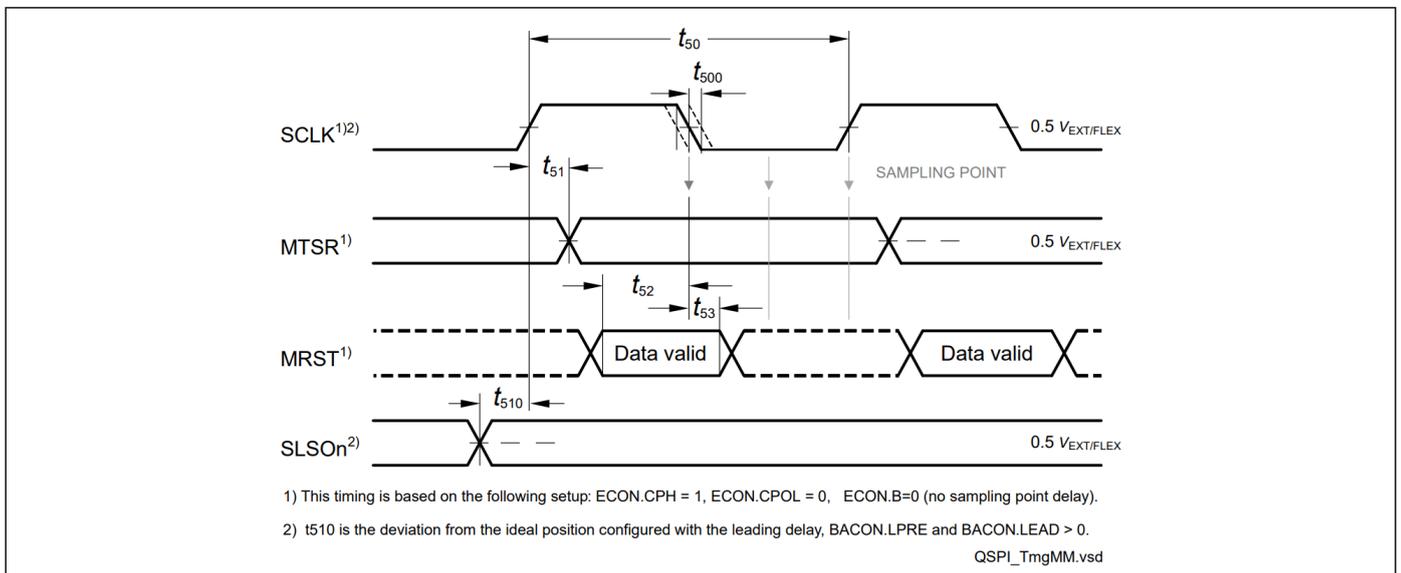


图 3-14 SSC 主模式时序

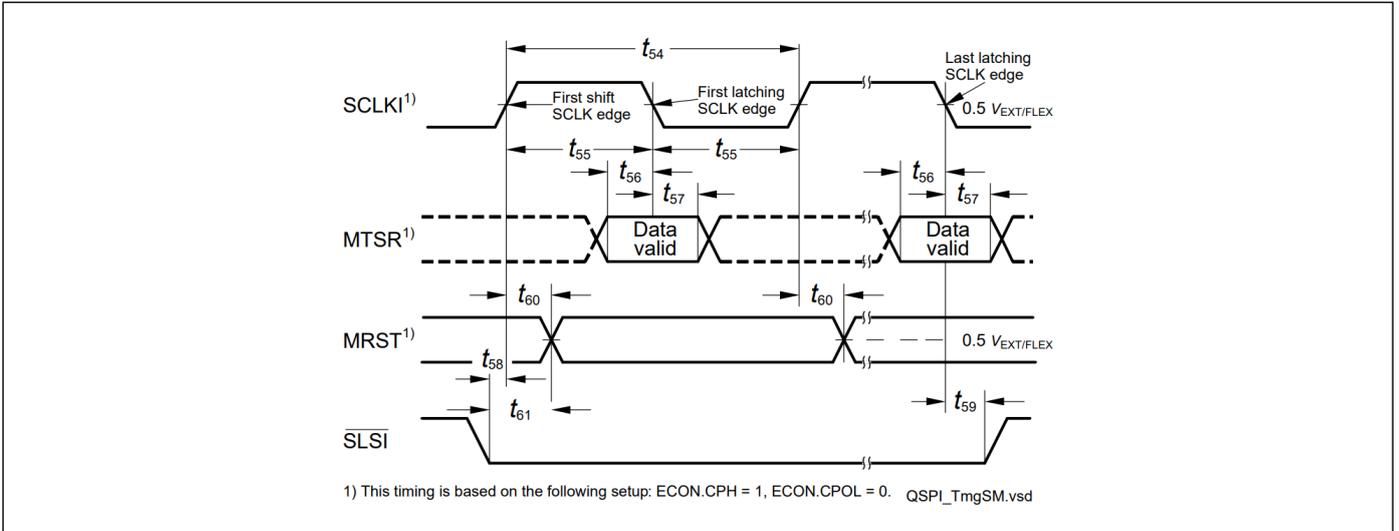


图3-15 从模式时序

### 3.23 MSC时序 5 V 操作

以下部分定义了时序。

注释：焊盘不对称已包含在以下时序中。

注释：LVDS焊盘的负载在下列时序中定义为差分负载。

表 3-49 5V下的LVDS 时钟/数据 (LVDS 模式下的 LVDS 焊盘)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FCLPx clock period	$t_{40\text{ CC}}$	$2 * T_{A(1)2}^{3)}$	-	-	ns	LVDS; $C_L=50\text{pF}$
Deviation from ideal duty cycle	$t_{400\text{ CC}}$	-1 <sup>3)</sup>	-	1 <sup>3)</sup>	ns	LVDS; $0 < C_L < 50\text{pF}$
SOPx output delay	$t_{44\text{ CC}}$	-3 <sup>3)</sup>	-	3 <sup>3)</sup>	ns	$CL=50\text{pF}$
ENx output delay	$t_{45\text{ CC}}$	-4 <sup>3)</sup>	-	5 <sup>3)</sup>	ns	ss; $C_L=50\text{pF}$ ; ABRA block bypassed
		-4 <sup>3)</sup>	-	4 <sup>3)</sup>	ns	ss; $C_L=50\text{pF}$ ; ABRA block used
		-2 <sup>3)</sup>	-	10 <sup>3)</sup>	ns	sm; $C_L=50\text{pF}$
		-30 <sup>3)</sup>	-	30 <sup>3)</sup>	ns	m; $C_L=50\text{pF}$

1)  $T_A$ 取决于为MSC的ABRA功能块中的波特率生成选择的时钟源。

2) LVDS引脚上的容性负载是差分的，CMOS引脚上的容性负载是单端的。

3) 条件列表中定义的负载 ( $C_L=50\text{pF}$ ) 是针对单端信号 EN 的负载定义，并不旨在在差分信号线内添加额外负载。对于单端信号，负载定义定义了 PCB 布局上信号的最大长度。对于 LVDS 焊盘，适用 IEEE Std 1596.3-1996 负载定义。

表 3-50 5V下的强尖锐 (ss) 时钟/数据驱动器

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FCLPx clock period	$t_{40\text{ CC}}$	$2 * T_A$	-	-	ns	$CL=50\text{pF}$
Deviation from ideal duty cycle	$t_{400\text{ CC}}$	-2	-	2	ns	$CL=50\text{pF}$
SOPx output delay	$t_{44\text{ CC}}$	-4	-	3.5	ns	$CL=50\text{pF}$
ENx output delay	$t_{45\text{ CC}}$	-4	-	3.5	ns	$CL=50\text{pF}$

表 3-51 5V下的强中型 (sm) 时钟/数据驱动器

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FCLPx clock period	$t_{40\text{ CC}}$	$2 * T_A$	-	-	ns	$CL=50\text{pF}$
Deviation from ideal duty cycle	$t_{400\text{ CC}}$	-5	-	5	ns	$CL=50\text{pF}$
SOPx output delay	$t_{44\text{ CC}}$	-7	-	7	ns	$CL=50\text{pF}$
ENx output delay	$t_{45\text{ CC}}$	-7	-	7	ns	$CL=50\text{pF}$

表 3-52 5V下的中等 (m) 时钟/数据驱动器

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FCLPx clock period	$t_{40}$ CC	$2 * T_A$	-	-	ns	CL=50pF
Deviation from ideal duty cycle	$t_{400}$ CC	-10	-	10	ns	CL=50pF
SOPx output delay	$t_{44}$ CC	-20	-	20	ns	CL=50pF
ENx output delay	$t_{45}$ CC	-20	-	20	ns	CL=50pF

表 3-53 上行接口

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SDI bit time	$t_{46}$ SR	$8 * t_{MSC}$	-	-	ns	
SDI rise time	$t_{48}$ SR	-	-	200	ns	
SDI fall time	$t_{49}$ SR	-	-	200	ns	

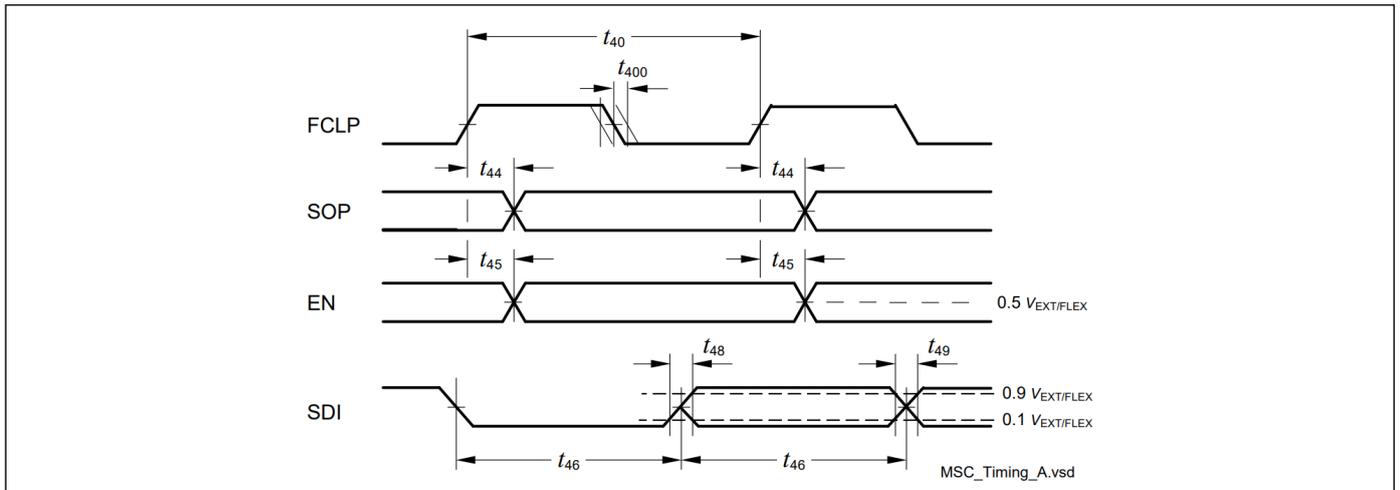


图 3-16 MSC 接口时序

注释: SOP 数据信号是在目标器件中的 FCLP 的下降沿进行采样的。

### 3.24 以太网接口 (ETH) 特性

#### 3.24.1 ETH 测量参考点

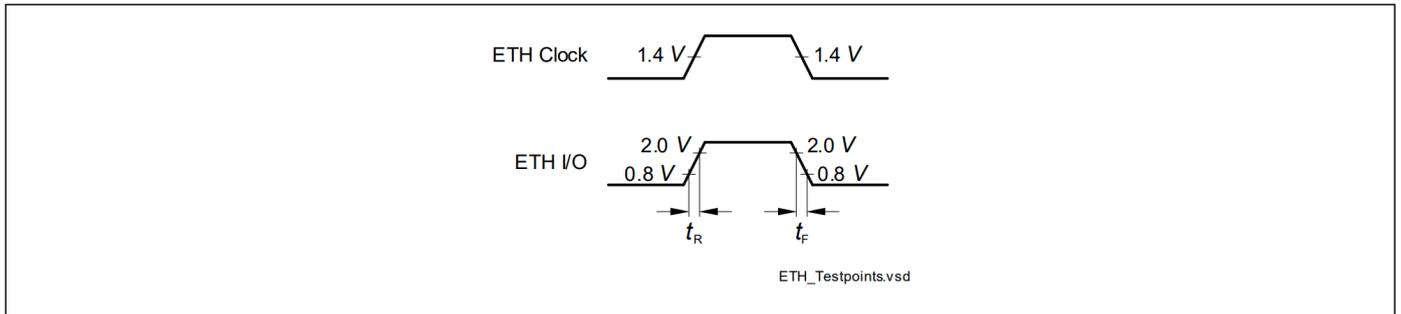


图 3-17 ETH 测量参考点

### 3.24.2 ETH管理信号参数 (ETH\_MDC、ETH\_MDIO)

表 3-54 适用于3.3 V的 ETH 管理信号参数

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ETH_MDC period	$t_1$ CC	400	-	-	ns	CL=25pF
ETH_MDC high time	$t_2$ CC	160	-	-	ns	CL=25pF
ETH_MDC low time	$t_3$ CC	160	-	-	ns	CL=25pF
ETH_MDIO setup time (output)	$t_4$ CC	10	-	-	ns	CL=25pF
ETH_MDIO hold time (output)	$t_5$ CC	10	-	-	ns	CL=25pF
ETH_MDIO data valid (input)	$t_6$ SR	0	-	300	ns	CL=25pF

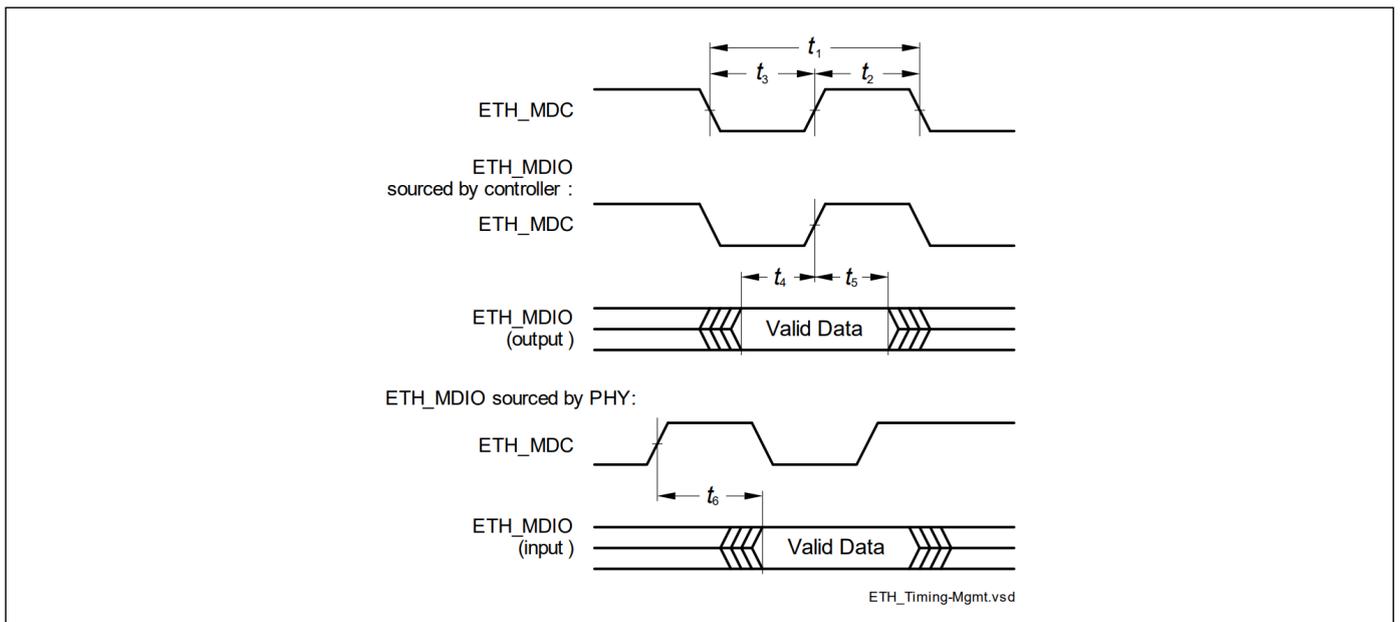


图 3-18 ETH 管理信号时序

### 3.24.3 ETH MII 参数

下面介绍MII（媒体独立接口）的参数。

表 3-55 ETH RMII 信号时序参数

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	$t_7$ SR	-	40	-	ns	CL=25pF ; baudrate=100Mbps
		-	400	-	ns	CL=25pF ; baudrate=10Mbps
Clock high time	$t_8$ SR	14	-	26	ns	CL=25pF ; baudrate=100Mbps
		140 <sup>1)</sup>	-	260 <sup>2)</sup>	ns	CL=25pF ; baudrate=10Mbps
Clock low time	$t_9$ SR	14	-	26	ns	CL=25pF ; baudrate=100Mbps
		140 <sup>1)</sup>	-	260 <sup>2)</sup>	ns	CL=25pF ; baudrate=10Mbps
Input setup time	$t_{10}$ SR	10	-	-	ns	CL=25pF
Input hold time	$t_{11}$ SR	10	-	-	ns	CL=25pF
Output valid time	$t_{12}$ CC	0	-	25	ns	CL=25pF

1) 按时钟周期的 35% 定义。

2) 按时钟周期的 65% 定义。

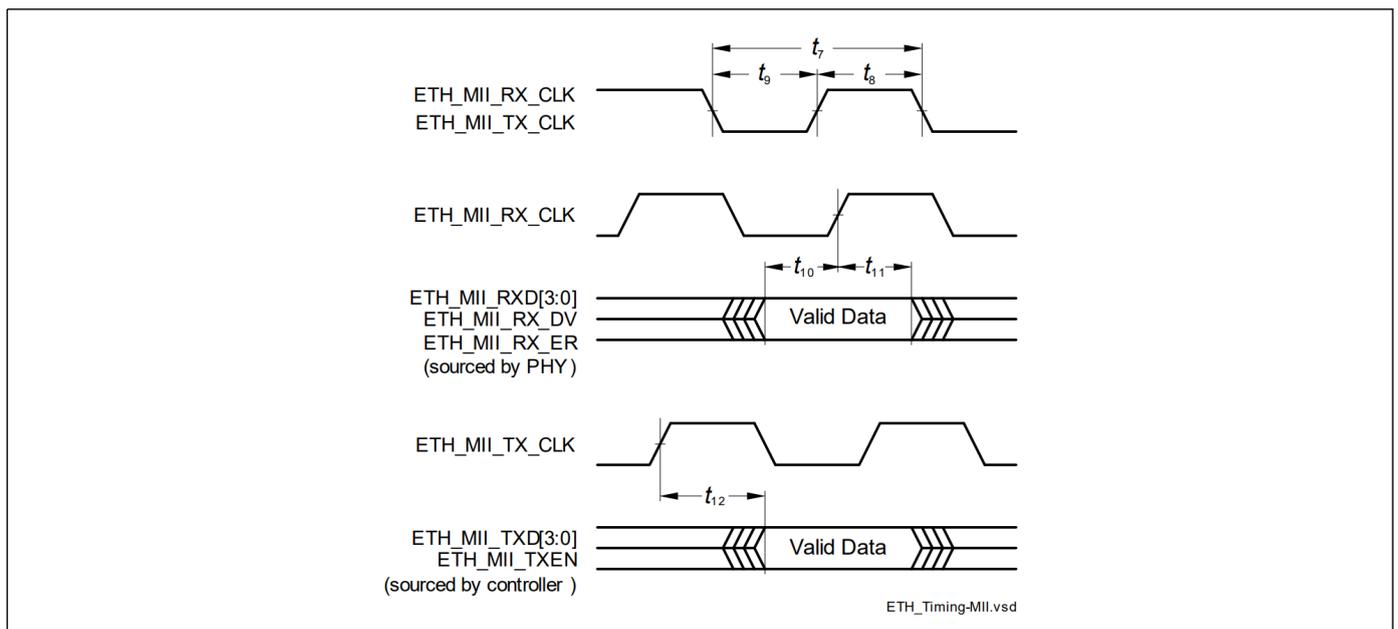


图 3-19 ETH MII 信号时序

### 3.24.4 ETH RMII 参数

下面介绍RMII（精简媒体独立接口）的参数。

表 3-56 适用于 3.3V 的ETH RMII 信号时序参数

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ETH_RMII_REF_CL clock period	$t_{13}$ SR	-	20	-	ns	50ppm ; CL=25pF
ETH_RMII_REF_CL clock high time	$t_{14}$ SR	7 <sup>1)</sup>	-	13 <sup>2)</sup>	ns	CL=25pF
ETH_RMII_REF_CL clock low time	$t_{15}$ SR	7 <sup>1)</sup>	-	13 <sup>2)</sup>	ns	CL=25pF
ETHTXEN, ETHTXD[1:0], ETHRXD[1:0], ETHCRSDV; setup time <sup>3)</sup>	$t_{16}$ CC	4	-	-	ns	CL=25pF
ETHTXEN, ETHTXD[1:0], ETHRXD[1:0], ETHCRSDV; hold time <sup>3)</sup>	$t_{17}$ CC	2	-	-	ns	CL=25pF

- 1) 按时钟周期的 35% 定义。
- 2) 按时钟周期的 65% 定义。
- 3) 对于 ETHRXD 和 ETHCRSDV 信号，此参数是 SR。

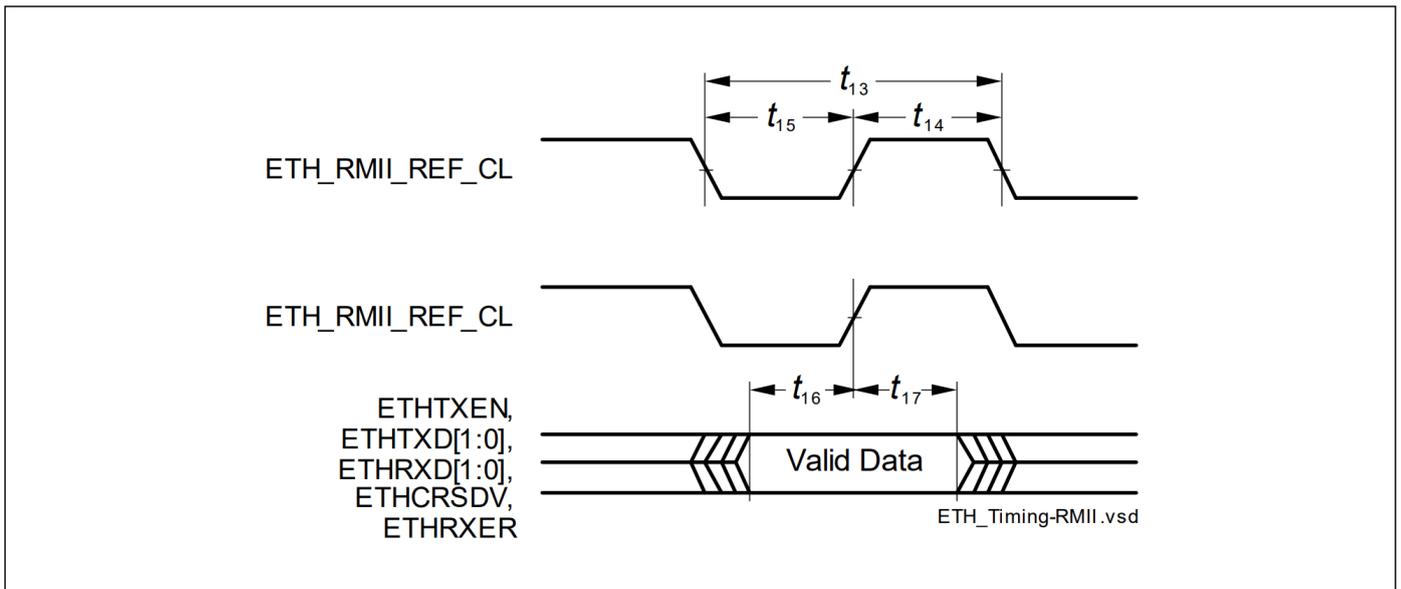


图 3-20 ETH RMII 信号时序

### 3.24.5 ETH RGMII 参数

下面介绍RGMII的参数。

表 3-57 适用于 3.3V 的ETH RGMII 信号时序参数

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TX Clock period	$t_{19}$ CC	36	40	44	ns	100Mbps
		360	400	440	ns	10Mbps
		7.2	8	8.8	ns	Gigabit
Data to Clock Output skew	$t_{20}$ CC	-500	0	500	ps	
Data to Clock input skew (at receiver)	$t_{21}$ SR	1	1.8	2.6	ns	SKEWCTL.RXCFG = 0; SKEWCTL.TXCFG = 0
Clock duty cycle	$t_{duty}$ CC	40	50	60	%	10/100Mbps
		45	50	55	%	Gigabit
GREFCLK duty cycle	$t_{duty\_in}$ SR	45	-	55	%	
GREFCLK Input accuracy	ACC SR	-0.005	-	0.005	%	

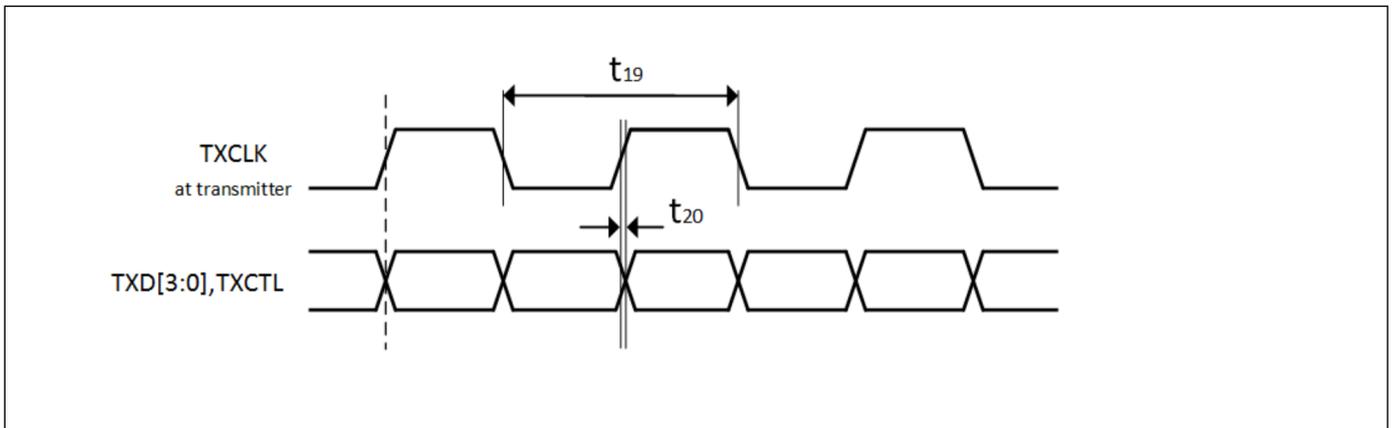


图 3-21 ETH RGMII TX 信号时序 (目的地延迟 (DoD))

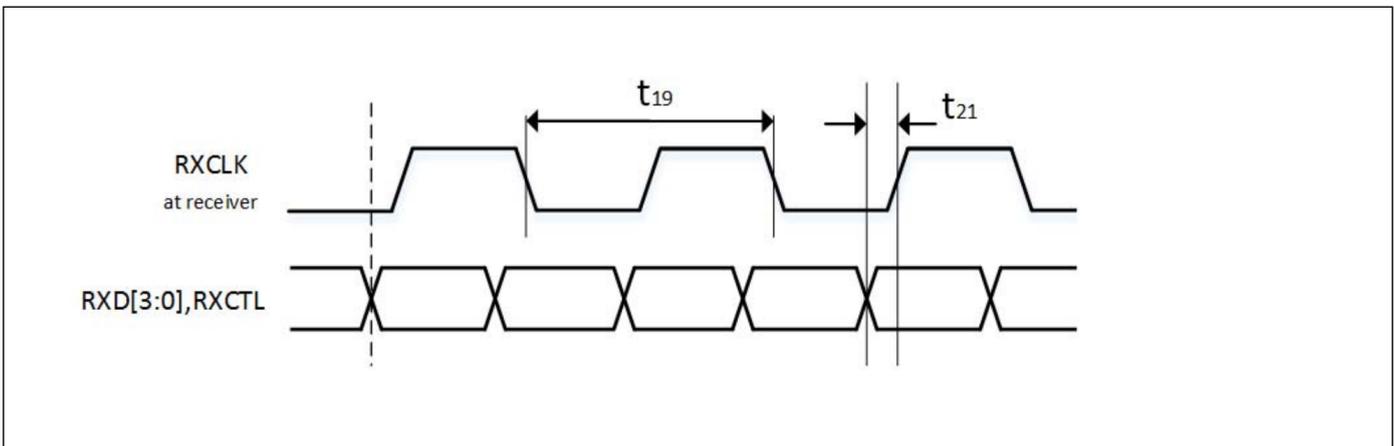


图 3-22 ETH RGMII RX 信号时序 (源延迟 (DoS))

### 3.25 E-Ray 参数

本节的时序适用于  $C_L = 25 \text{ pF}$  的输出驱动器的强驱动器和锐边设置。

表 3-58 发送参数

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise time of TxEN	$t_{dCCTxENRise25}^{CC}$	-	-	9	ns	$C_L=25\text{pF}$
Fall time of TxEN	$t_{dCCTxENFall25}^{CC}$	-	-	9	ns	$C_L=25\text{pF}$
Sum of rise and fall time	$t_{dCCTxRise25+d}^{CC}$ $t_{dCCTxFall25}^{CC}$	-	-	9	ns	20% - 80% ; $C_L=25\text{pF}$
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, rising edge of TxEN	$t_{dCCTxEN01}^{CC}$	-	-	25	ns	
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, falling edge of TxEN	$t_{dCCTxEN10}^{CC}$	-	-	25	ns	
Asymmetry of sending	$t_{tx\_asym}^{CC}$	-2.45	-	2.45	ns	$C_L=25\text{pF}$
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, rising edge of TxD	$t_{dCCTxD01}^{CC}$	-	-	25	ns	
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, falling edge of TxD	$t_{dCCTxD10}^{CC}$	-	-	25	ns	
TxD signal sum of rise and fall time at TP1_BD	$t_{txd\_sum}^{CC}$	-	-	9	ns	

表 3-59 接收参数

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Acceptance of asymmetry at receiving part	$t_{dCCTxAsymAcc}^{SR}$ ept25	-30.5	-	43.0	ns	$C_L=25\text{pF}$
Acceptance of asymmetry at receiving part	$t_{dCCTxAsymAcc}^{SR}$ ept15	-31.5	-	44.0	ns	$C_L=15\text{pF}$
Threshold for detecting logical high	$T_{uCCLogic1}^{SR}$	35	-	70	%	
Threshold for detecting logical low	$T_{uCCLogic0}^{SR}$	30	-	65	%	

表 3-59 接收参数 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Sum of delay between TP4_CC and TP4_FF and delays derived from TP4_FFi, rising edge of RxD	$t_{dCCRxD01}$ CC	-	-	10	ns	
Sum of delay between TP4_CC and TP4_FF and delays derived from TP4_FFi, falling edge of RxD	$t_{dCCRxD10}$ CC	-	-	10	ns	

## 3.26 HSCT 参数

表 3-60 HSCT - Rx 寄生参数和负载

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Capacitance total budget	$C_{total}$ CC	-	3.5	5	pF	Total Budget for complete receiver including silicon, package, pins and bond wire
Parasitic inductance budget	$H_{total}$ CC	-	5	-	nH	

表 3-61 HSCT - Rx/Tx 设置时序

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RX o/p duty cycle	$DC_{rx}$ CC	40	-	60	%	
Disable time of the LVDS pad	$t_{LVDS_{DIS}}$ CC	-	-	20	ns	
Enable time of the LVDS pad	$t_{LVDS_{SEN}}$ CC	-	-	400	ns	
Wakeup time from Sleep Mode	$t_{SWU}$ CC	-	-	250	ns	
Maximum length of a wake-up glitch that does not wake-up the receiver	$t_{WUP}$ CC	-	-	0.2	ns	
Bias startup time	$t_{bias}$ CC	-	5	10	$\mu$ s	Bias distributor waking up from power down and provide stable Bias.
RX startup time	$t_{rx}$ CC	-	-	600	ns	Wake-up RX from power down.
TX startup time	$t_{tx}$ CC	-	-	280	ns	Wake-up TX from power down.

表 3-62 HSCT

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Bit Error Rate based on 20 MHz reference clock at Slave PLL side	$BER_{20}$ CC	-	-	10EXP-12		Bit Error Rate based on 20 MHz reference clock at Slave PLL side
Transition time from Rx Disable to Rx Low Speed Mode	$t_{DISLS}$ CC	-	-	700	ns	Transition time from Rx Disable to Rx Low Speed Mode

表 3-62 HSCT (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Transistion time from Rx High/Low Speed Mode to Rx Medium Speed Mode	$t_{\text{HLSMS}}^{\text{CC}}$	-	-	500	ns	Transition time from Rx High/Low Speed Mode to Rx Medium Speed Mode
Transistion time from Rx High/Medium Speed Mode to Rx Low Speed Mode	$t_{\text{HMSLS}}^{\text{CC}}$	-	-	600	ns	Transition time from Rx High/Medium Speed Mode to Rx Low Speed Mode
Transistion time from Tx High Speed Mode to Tx Low Speed Mode	$t_{\text{HLSL}}^{\text{CC}}$	-	-	600	ns	Transition time from Tx High Speed Mode to Tx Low Speed Mode
Transistion time from Tx Low Speed Mode to Tx High Speed Mode	$t_{\text{LSHS}}^{\text{CC}}$	-	-	400	ns	Transition time from Tx Low Speed Mode to Tx High Speed Mode
Transistion time from Rx Medium/Low Speed Mode to Rx High Speed Mode	$t_{\text{MLSHS}}^{\text{CC}}$	-	-	400	ns	Transition time from Rx Medium/Low Speed Mode to Rx High Speed Mode
HSCT physical layer power-on	$t_{\text{PON}}^{\text{CC}}$	-	-	600	ns	HSCT physical layer power-on

### 3.27 Inter-IC (I2C) 接口时序

所有 I2C 时序参数均为主模式的 SR 和从模式的 CC。

表 3-63 I2C 标准模式时序

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	$t_1$	-	-	300	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Capacitive load for each bus line	$C_b$ SR	-	-	400	pF	
Bus free time between a STOP and ATART condition	$t_{10}$	4.7	-	-	$\mu$ s	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Rise time of both SDA and SCL	$t_2$	-	-	1000	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Data hold time	$t_3$	0	-	-	$\mu$ s	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Data set-up time	$t_4$	250	-	-	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Low period of SCL clock	$t_5$	4.7	-	-	$\mu$ s	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
High period of SCL clock	$t_6$	4	-	-	$\mu$ s	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Hold time for the (repeated) START condition	$t_7$	4	-	-	$\mu$ s	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Set-up time for (repeated) START condition	$t_8$	4.7	-	-	$\mu$ s	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Set-up time for STOP condition	$t_9$	4	-	-	$\mu$ s	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line

表 3-64 I2C 快速模式时序

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	$t_1$	$20+0.1 \cdot C_b$	-	300	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Capacitive load for each bus line	$C_b$ SR	-	-	400	pF	
Bus free time between a STOP and ATART condition	$t_{10}$	1.3	-	-	$\mu$ s	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Rise time of both SDA and SCL	$t_2$	$20+0.1 \cdot C_b$	-	300	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Data hold time	$t_3$	0	-	-	$\mu$ s	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Data set-up time	$t_4$	100	-	-	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Low period of SCL clock	$t_5$	1.3	-	-	$\mu$ s	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
High period of SCL clock	$t_6$	0.6	-	-	$\mu$ s	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Hold time for the (repeated) START condition	$t_7$	0.6	-	-	$\mu$ s	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Set-up time for (repeated) START condition	$t_8$	0.6	-	-	$\mu$ s	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Set-up time for STOP condition	$t_9$	0.6	-	-	$\mu$ s	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line

表 3-65 I2C 高速模式时序

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Capacitive load for each bus line	$C_b$ SR	-	-	400	pF	
Fall time of SCL	$t_{11}$	10 <sup>1)</sup>	-	40 <sup>1)</sup>	ns	bus line load of 100pF
Fall time of SDA	$t_{12}$	10 <sup>1)</sup>	-	80 <sup>1)</sup>	ns	bus line load of 100pF
Rise time of SCL	$t_{13}$	10 <sup>1)</sup>	-	40 <sup>1)</sup>	ns	bus line load of 100pF
Rise time of SDA	$t_{14}$	10 <sup>1)</sup>	-	80 <sup>1)</sup>	ns	bus line load of 100pF
Data hold time	$t_3$	0 <sup>1)</sup>	-	70 <sup>1)</sup>	ns	bus line load of 100pF
Data set-up time	$t_4$	10 <sup>1)</sup>	-	-	ns	bus line load of 100pF
Low period of SCL clock	$t_5$	160 <sup>1)</sup>	-	-	ns	bus line load of 100pF
High period of SCL clock	$t_6$	60 <sup>1)</sup>	-	-	ns	bus line load of 100pF
Hold time for the (repeated) START condition	$t_7$	160 <sup>1)</sup>	-	-	ns	bus line load of 100pF
Set-up time for (repeated) START condition	$t_8$	160 <sup>1)</sup>	-	-	ns	bus line load of 100pF
Set-up time for STOP condition	$t_9$	160 <sup>1)</sup>	-	-	ns	bus line load of 100pF

1) 电容值定义为  $C_b = 100\text{pF}$ ，有关  $C_b = 400\text{pF}$  的时序，请参阅 I2C 标准。

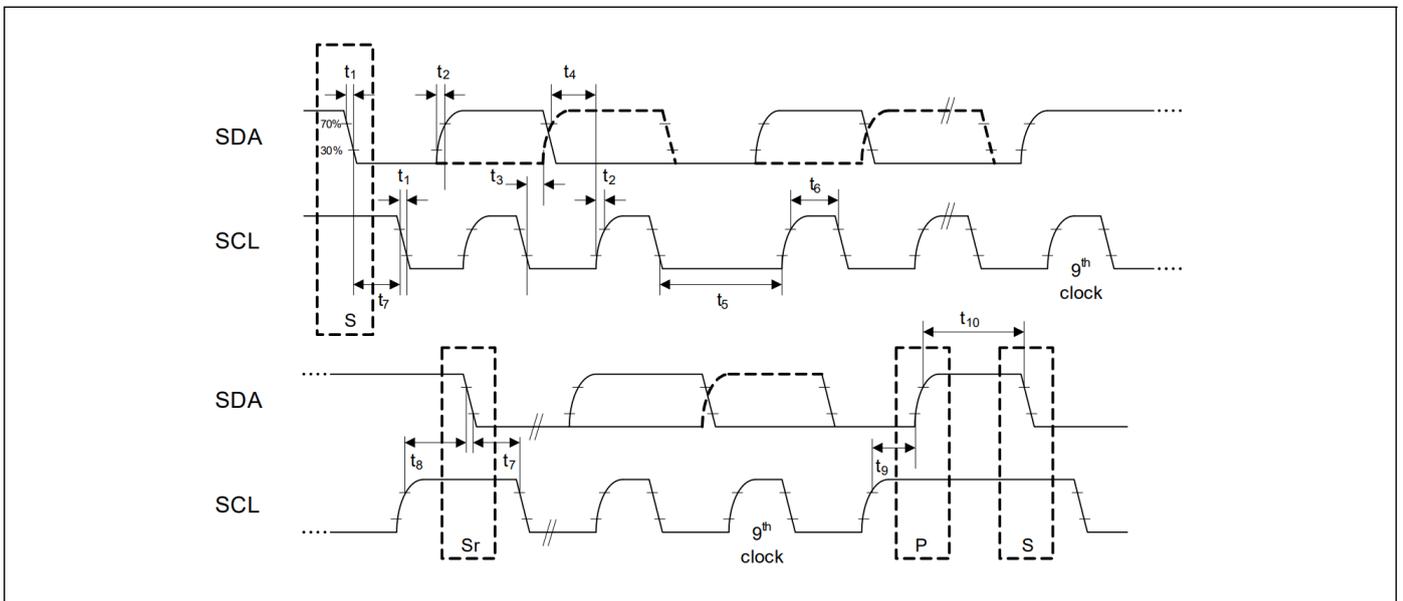


图 3-23 I2C 标准模式和快速模式时序

## 3.28 SDMMC 接口时序

表 3-66 SDMMC

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period Data Transfer Mode	$t_1$ CC	20	-	-	ns	push-pull, $C_L \leq 30\text{pF}$ , $V_{EXT} = 3.3\text{V}$
Clock period Indentification Mode	$t_2$ CC	-	-	2500	ns	open-drain, $C_L \leq 30\text{pF}$ , $V_{EXT} = 3.3\text{V}$
Clock low time	$t_3$ CC	6,5	-	-	ns	$C_L \leq 30\text{pF}$ , $V_{EXT} = 3.3\text{V}$
Clock high time	$t_4$ CC	6,5	-	-	ns	$C_L \leq 30\text{pF}$ , $V_{EXT} = 3.3\text{V}$
Data output valid time before rising clock edge	$t_5$ CC	3	-	-	ns	$C_L \leq 30\text{pF}$ , $V_{EXT} = 3.3\text{V}$
Data output valid time after rising clock edge	$t_6$ CC	3	-	-	ns	$C_L \leq 30\text{pF}$ , $V_{EXT} = 3.3\text{V}$
Data input hold time	$t_7$ SR	2,5	-	-	ns	$C_L \leq 30\text{pF}$ , $V_{EXT} = 3.3\text{V}$ , TTL levels
Data Input delay time	$t_8$ SR	-	-	13,7	ns	$C_L \leq 30\text{pF}$ , $V_{EXT} = 3.3\text{V}$ , TTL levels
Data Input setup time	$t_9$ SR	5,2	-	-	ns	$C_L \leq 30\text{pF}$ , $V_{EXT} = 3.3\text{V}$ , TTL levels

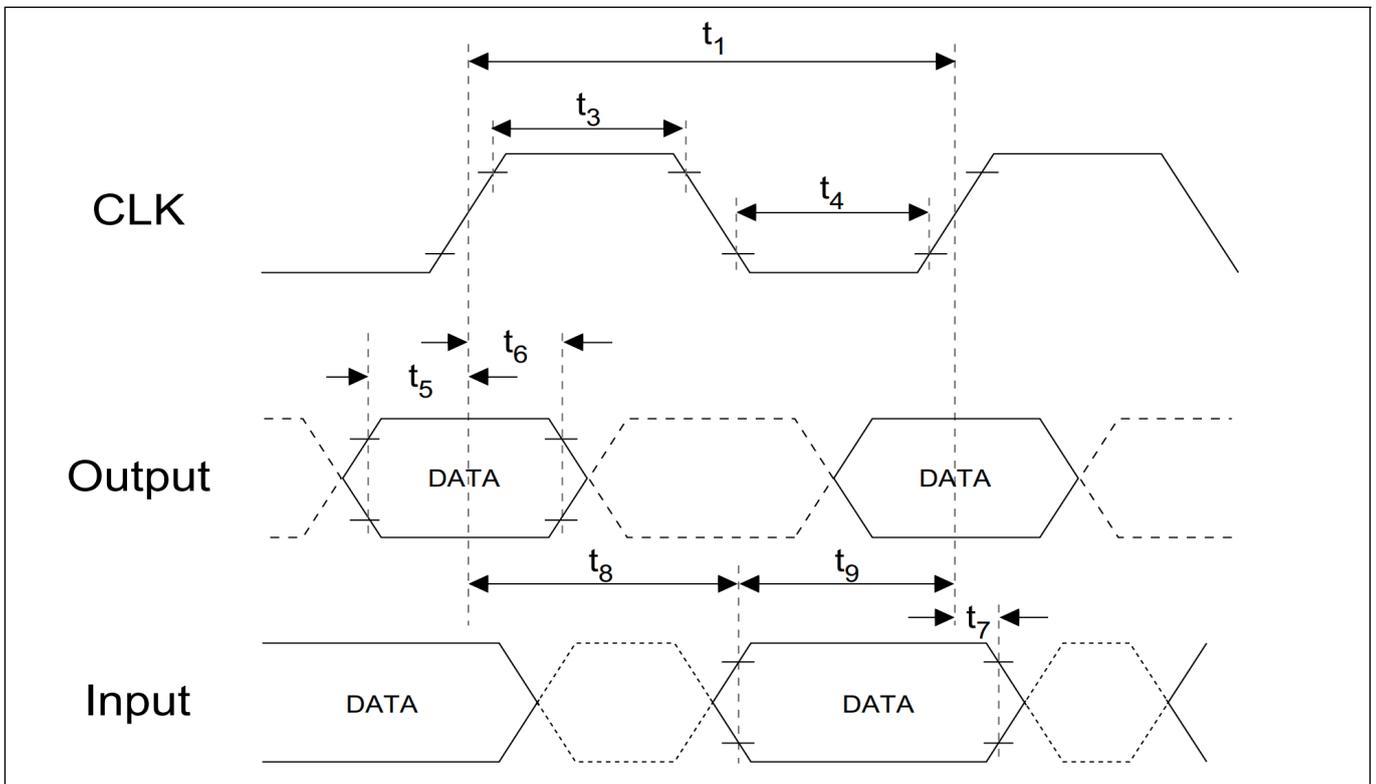


图 3-24 SDMMC 时序

## 3.29 FSP 参数

表 3-67 安全性

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Skew between FSP0 and FSP1	$t_{\text{FSPSKEW}}^{\text{CC}}$	-8	-	9	ns	$C_L=50\text{pF}$ , driver strength m
		-5	-	6	ns	$C_L=50\text{pF}$ , driver strength sm
		-4	-	5	ns	$C_L=50\text{pF}$ , driver strength ss

### 3.30 雷达接口时序

本节定义了 TC39x 中 RIF 的时序。

表 3-68 偏移校准相关

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Bit time	$t_{80}$ CC	2.5	-	-	ns	
Set-up time	$t_{82}$ SR	0.8	-	-	ns	
Hold time	$t_{83}$ SR	0.8	-	-	ns	
RAMP1 set-up time relative to the FRAME rising edge	$t_{88}$ SR	30	-	-	ns	
RAMP1 hold time relative to the FRAME rising edge	$t_{89}$ SR	30	-	-	ns	

### 3.31 EBU时序

#### 3.31.1 BFCLKO 输出时钟时序

$V_{SS} = 0\text{ V}; V_{DD} = 1.3\text{ V} \pm 5\%; 3.3\text{ V} \pm 5\%$ ,

表 3-69 BFCLKO 输出时钟时序参数<sup>1)</sup>

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
BFCLKO clock period	$t_{\text{BFCLKO}}$ CC	13.33 <sup>2)</sup>	-	-	ns	-
BFCLKO high time	$t_5$ CC	3	-	-	ns	-
BFCLKO low time	$t_6$ CC	3	-	-	ns	-
BFCLKO rise time	$t_7$ CC	-	-	3	ns	-
BFCLKO fall time	$t_8$ CC	-	-	3	ns	-
BFCLKO duty cycle $t_5/(t_5 + t_6)^{3)}$	DC	35	50	55	%	-

- 1) 未经过生产测试 - 经过设计/特性验证。
- 2) PLL 抖动特性根据应用设置添加到该值。查看 PLL 抖动参数。
- 3) 此参数不包含PLL抖动。如果BFCLKO频率等于 $f_{\text{CPU}}$ ，则必须考虑K分频器。

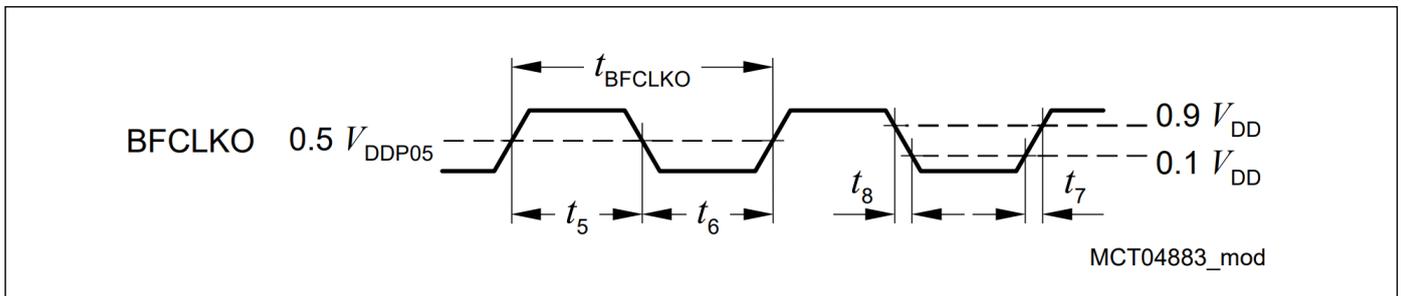


图 3-25 BFCLKO 输出时钟时序

#### 3.31.2 EBU 异步时序

对于每个时序，必须单独添加时钟周期数中编程持续时间的累积 PLL 抖动。

表 3-70 适用于 3.3V 的常见异步时序

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
AD(31:0) output delay to ADV# rising edge, multiplexed read / write	$t_{13}$ CC	-5.5	-	2.5	ns	$C_L=35\text{ pF}$
AD(31:0) output delay to ADV# rising edge, multiplexed read / write	$t_{14}$ CC	-5.5	-	2.5	ns	$C_L=35\text{ pF}$

表 3-70 适用于 3.3V 的常见异步时序 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Address valid to CS falling edge (deviation from programmed value)	$t_{15}$ CC	-2	-	2.5	ns	$C_L=35\text{pF}$
Address valid to ADV falling edge (deviation from programmed value)	$t_{16}$ CC	-2	-	2.5	ns	$C_L=35\text{pF}$
ADV falling edge -> CS falling edge (deviation from programmed value)	$t_{17}$ CC	-2	-	2.5	ns	$C_L=35\text{pF}$
Pulse width deviation from the ideal programmed width due to B pad asymmetry, rise delay - fall delay	$t_a$ CC	-0.8	-	0.8	ns	edge=medium; $C_L=35\text{pF}$
		-0.8	-	0.8	ns	edge=sharp; $C_L=35\text{pF}$

表 3-71 适用于 3.3V 的异步读取时序

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
A(23:0) output delay to $\overline{\text{RD}}$ rising edge, deviation from the ideal programmed value	$t_0$ CC	-2.5	-	2.5	ns	$C_L=35\text{pF}$
Data input Hold from CS rising edge	$t_{18}$ CC	-6	-	-	ns	$C_L=35\text{pF}$
Data input Setup to CS rising edge	$t_{19}$ CC	19	-	-	ns	$C_L=35\text{pF}$
A(23:0) output delay to RD rising edge, deviation from the ideal programmed value	$t_1$ CC	-2.5	-	2.5	ns	$C_L=35\text{pF}$
CS rising edge to RD rising edge, deviation from the ideal programmed value	$t_2$ CC	-2	-	2.5	ns	$C_L=35\text{pF}$
ADV rising edge to RD rising edge, deviation from the ideal programmed value	$t_3$ CC	-2	-	4.5	ns	$C_L=35\text{pF}$
BC rising edge to RD rising edge, deviation from the ideal programmed value	$t_4$ CC	-2.5	-	2.5	ns	$C_L=35\text{pF}$
WAIT input setup to RD rising edge, deviation from the ideal programmed value	$t_5$ SR	19	-	-	ns	$C_L=35\text{pF}$
WAIT input hold to RD rising edge, deviation from the ideal programmed value	$t_6$ SR	-4	-	-	ns	$C_L=35\text{pF}$

表 3-71 适用于 3.3V 的异步读取时序 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data input setup to RD rising edge, deviation from the ideal programmed value	$t_7$ SR	19	-	-	ns	$C_L=35\text{pF}$
Data input hold to RD rising edge, deviation from the ideal programmed value	$t_8$ SR	-4	-	-	ns	$C_L=35\text{pF}$
MR / W output delay to RD# rising edge, deviation from the ideal programmed value	$t_9$ CC	-2.5	-	1.5	ns	$C_L=35\text{pF}$

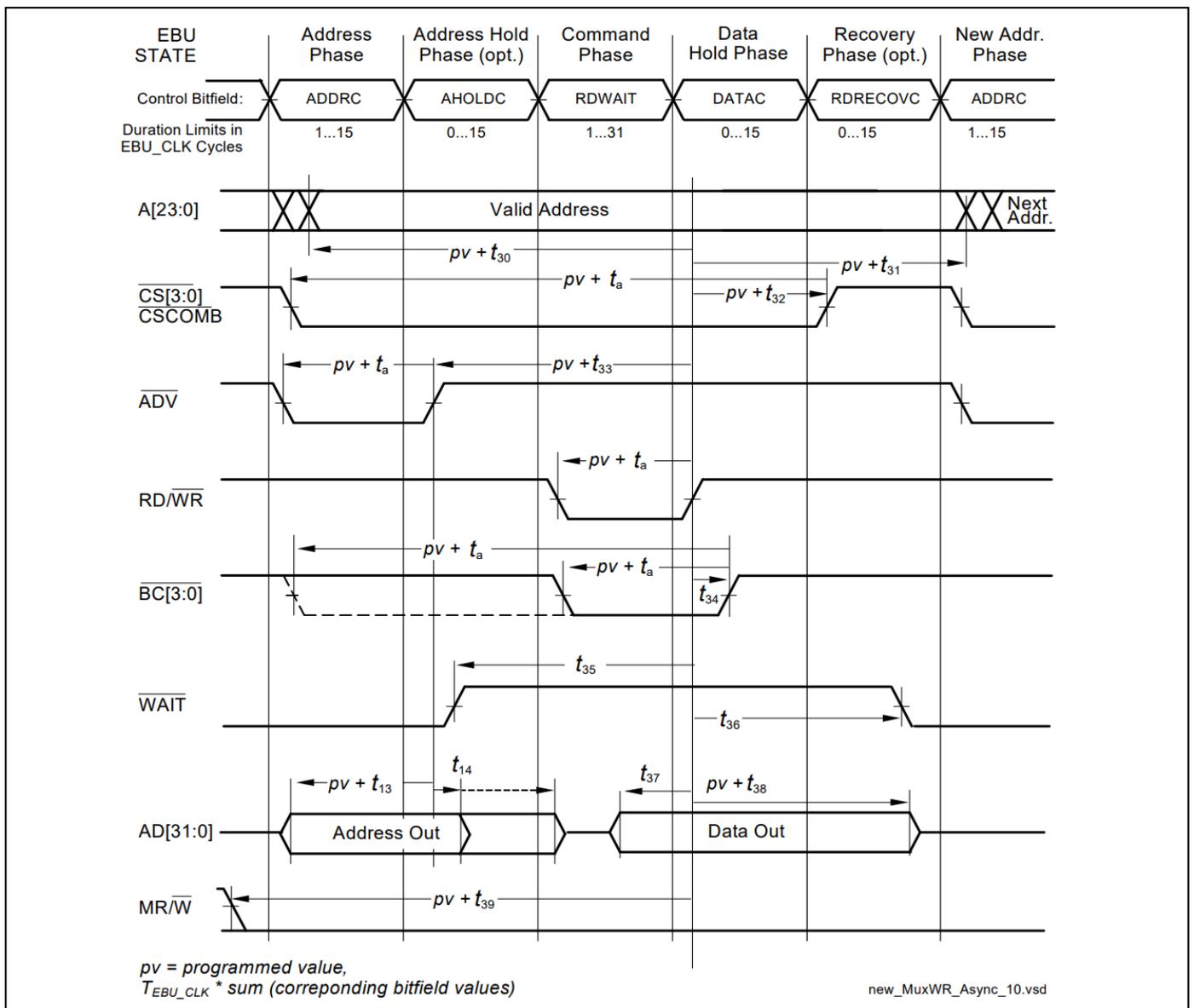


图 3-26 复用读取访问

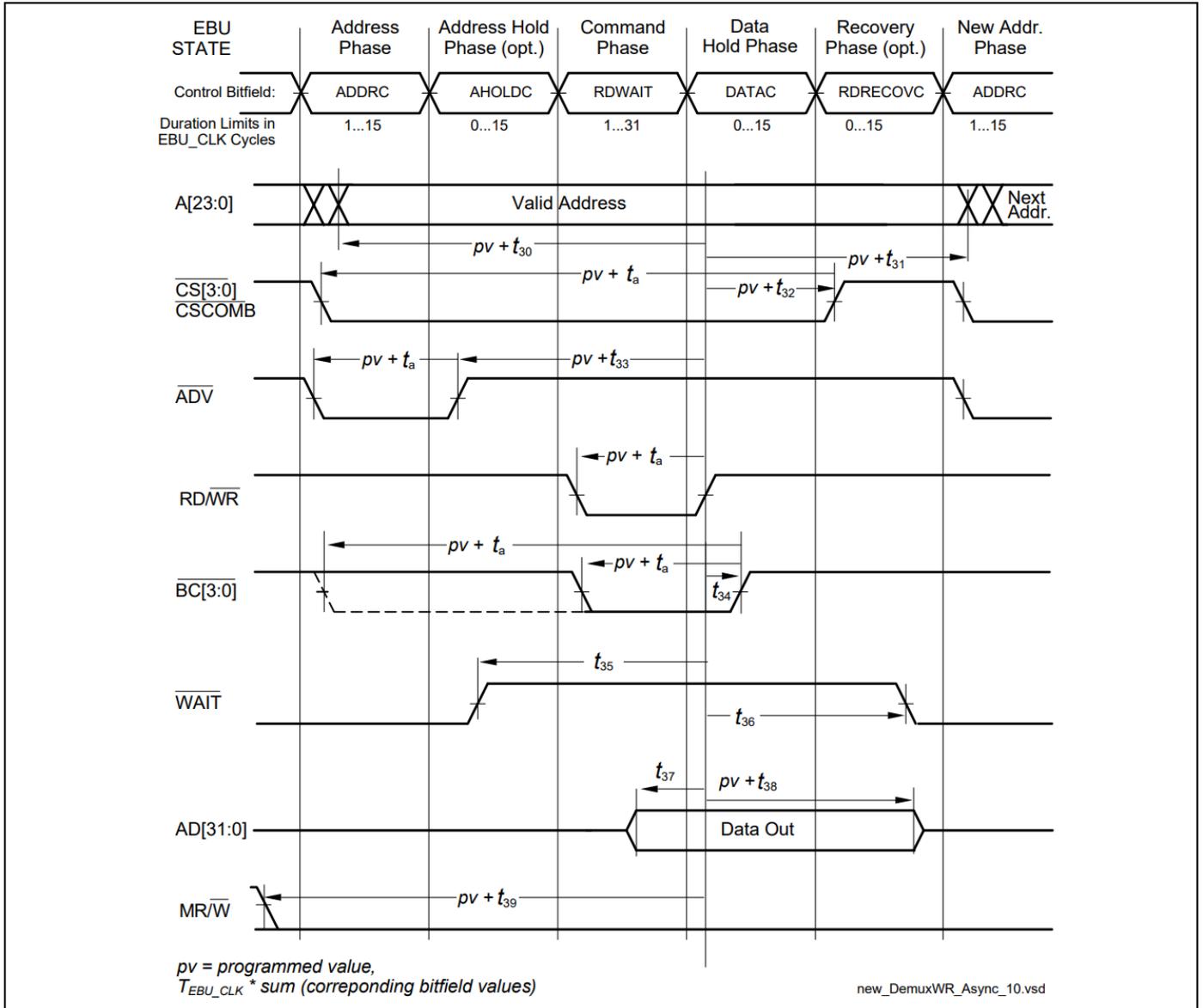


图 3-27 解复用读取访问

表 3-72 适用于 3.3V 异步写入时序

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
A(23:0) output delay to WR rising edge, deviation from the ideal programmed value	$t_{30}$ CC	-2.5	-	2.5	ns	$C_L=35\text{pF}$
A(23:0) output delay to WR rising edge, deviation from the ideal programmed value	$t_{31}$ CC	-2.5	-	2.5	ns	$C_L=35\text{pF}$
CS rising edge to WR rising edge, deviation from the ideal programmed value	$t_{32}$ CC	-2	-	2.5	ns	$C_L=35\text{pF}$

表 3-72 适用于 3.3V 的异步写入时序 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ADV rising edge to WR rising edge, deviation from the ideal programmed value	$t_{33}$ CC	-2.5	-	2	ns	$C_L=35\text{pF}$
BC rising edge to WR rising edge, deviation from the ideal programmed value	$t_{34}$ CC	-2.5	-	2	ns	$C_L=35\text{pF}$
WAIT input setup to WR rising edge, deviation from the ideal programmed value	$t_{35}$ SR	19	-	-	ns	$C_L=35\text{pF}$
WAIT input hold to WR rising edge, deviation from the ideal programmed value	$t_{36}$ SR	0	-	-	ns	$C_L=35\text{pF}$
Data output delay to WR rising edge, deviation from the ideal programmed value	$t_{37}$ CC	-5.5	-	2.5	ns	$C_L=35\text{pF}$
Data output delay to WR rising edge, deviation from the ideal programmed value	$t_{38}$ CC	-5.5	-	2.5	ns	$C_L=35\text{pF}$
MR / W output delay to WR rising edge, deviation from the ideal programmed value	$t_{39}$ CC	-2.5	-	1.5	ns	$C_L=35\text{pF}$

### 3.31.3 EBU 突发模式访问时序

$V_{SS} = 0\text{V}$ ;  $V_{DD} = 1.3\text{V} \pm 5\%$ ;  $V_{DDEBU} = 3.3\text{V} \pm 5\%$ ;

表 3-73 适用于 3.3V 的突发读取时序

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output delay from BFCLKO rising edge	$t_{10}$ CC	-2	-	2.5	ns	$C_L=35\text{pF}$
RD and RD/WR active/inactive after BFCLKO active edge	$t_{12}$ CC	-2	-	2	ns	$C_L=35\text{pF}$
CSx output delay from BFCLKO active edge	$t_{21}$ CC	-2.5	-	2.0	ns	$C_L=35\text{pF}$
ADV active/inactive after BFCLKO active edge	$t_{22}$ CC	-2	-	2	ns	$C_L=35\text{pF}$
BAA active/inactive after BFCLKO active edge	$t_{22a}$ CC	-2.5	-	2.0	ns	$C_L=35\text{pF}$
Data setup to BFCLKI rising edge	$t_{23}$ SR	5	-	-	ns	$C_L=35\text{pF}$
Data hold from BFCLKI rising edge	$t_{24}$ SR	0	-	-	ns	$C_L=35\text{pF}$

表 3-73 适用于 3.3V 的突发读取时序 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
WAIT setup (low or high) to BFCLKI rising edge	$t_{25}$ SR	5	-	-	ns	$C_L=35\text{pF}$
WAIT hold (low or high) from BFCLKI rising edge	$t_{26}$ SR	0	-	-	ns	$C_L=35\text{pF}$

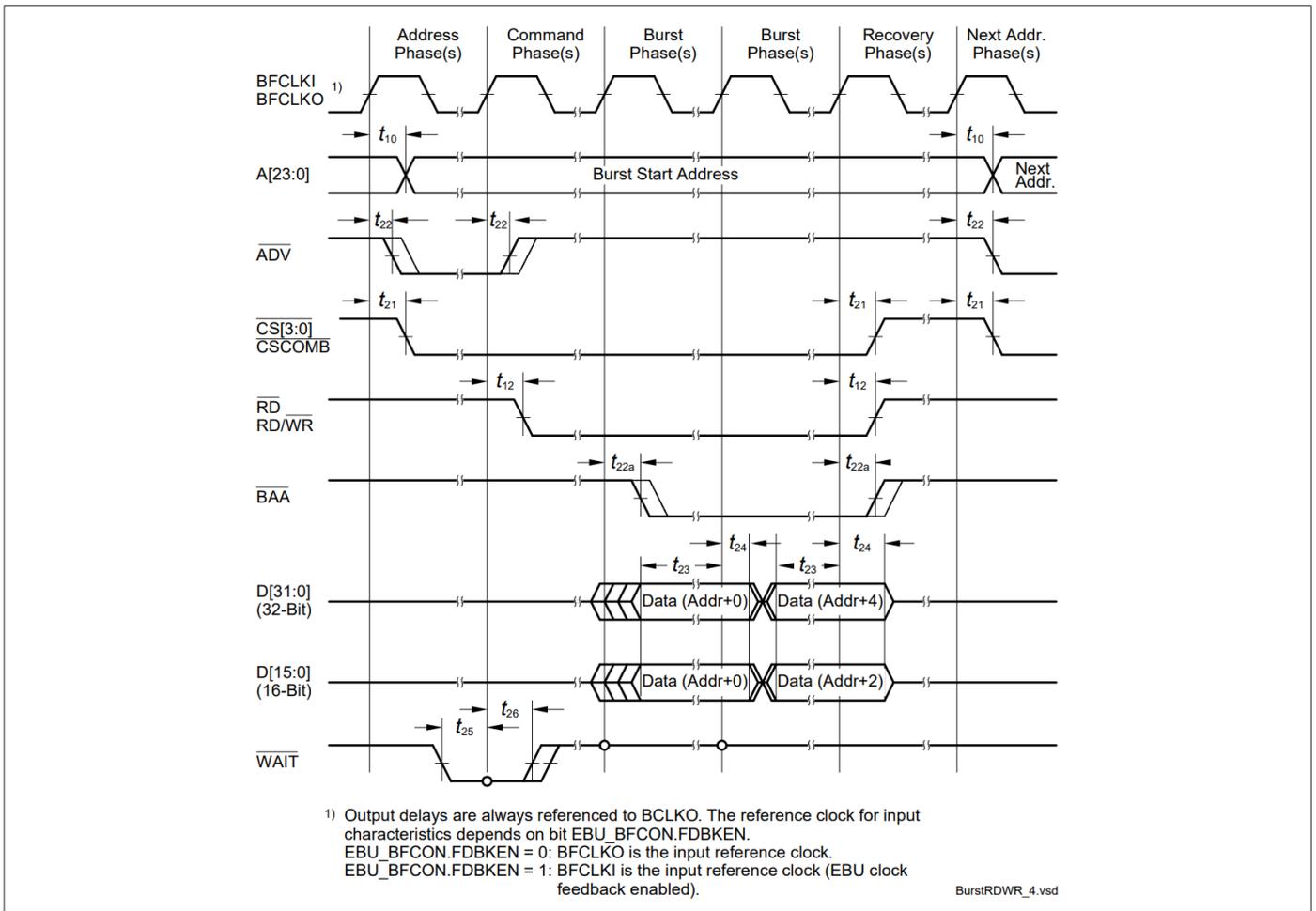


图 3-28 EBU 突发模式读/写访问时序

### 3.31.4 EBU 仲裁信号时序

$V_{SS} = 0\text{ V}; V_{DD} = 1.5\text{ V} \pm 5\%; V_{DDEBU} = 3.3\text{ V} \pm 5\%;$

表 3-74 适用于 3.3V 的 EBU 仲裁时序

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output delay from BFCLKO rising edge	$t_{27}$ CC	-	-	3	ns	$C_L = 35\text{ pF}$
Data setup to BFCLKO falling edge	$t_{28}$ SR	16	-	-	ns	$C_L = 35\text{ pF}$
Data hold from BFCLKO falling edge	$t_{29}$ SR	2	-	-	ns	$C_L = 35\text{ pF}$

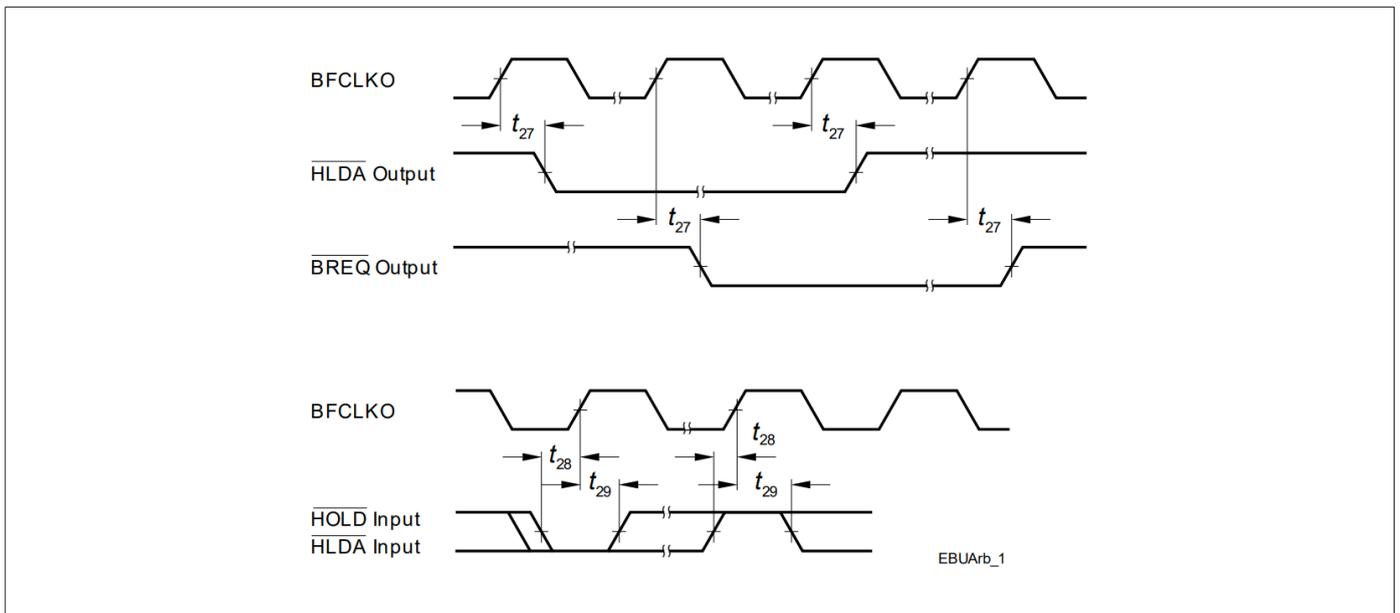


图3-29 EBU仲裁信号时序

### 3.32 Flash 目标参数

表 3-75 Flash

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Program Flash Erase Time per logical sector <sup>1)</sup>	$t_{ERP}$ CC	-	-	0.5	s	cycle count < 1000
Program Flash Erase Time per Multi-Sector Command <sup>1)</sup>	$t_{MERP}$ CC	-	-	0.5	s	For consecutive logical sectors in a physical sector with total range $\leq$ 512 kByte; cycle count < 1000
Program Flash program time per page in 5 V mode <sup>1)</sup>	$t_{PRP5}$ CC	-	-	80	$\mu$ s	32 Byte
Program Flash program time per page in 3.3 V mode <sup>1)</sup>	$t_{PRP3}$ CC	-	-	115	$\mu$ s	32 Byte
Program Flash program time per burst in 5 V mode <sup>1)</sup>	$t_{PRPB5}$ CC	-	-	220	$\mu$ s	256 Byte
Program Flash program time per burst in 3.3 V mode <sup>1)</sup>	$t_{PRPB3}$ CC	-	-	530	$\mu$ s	256 Byte
Program Flash program time for 1 MByte with burst programming in 3.3 V mode excluding communication <sup>1)</sup>	$t_{PRPB3\_1MB}$ CC	-	-	2.2	s	Derived value for documentation purpose
Program Flash program time for 1 MByte with burst programming in 5 V mode excluding communication <sup>1)</sup>	$t_{PRPB5\_1MB}$ CC	-	-	1	s	Derived value for documentation purpose
Program Flash program time for complete PFlash with burst programming in 5 V mode excluding communication <sup>1)</sup>	$t_{PRPB5\_PF}$ CC	-	-	16	s	Derived value for documentation purpose
Write Page Once adder <sup>1)</sup>	$t_{ADD}$ CC	-	-	20	$\mu$ s	Adder to Program Time when using Write Page Once
Program Flash suspend to read latency <sup>1)</sup>	$t_{SPNDP}$ CC	-	-	120	$\mu$ s	For Write Burst, Verify Erased and for multi-(logical) sector erase commands
Data Flash Erase Disturb Limit (single ended sensing mode)	$N_{DFD}$ CC	-	-	50	cycles	
Data Flash Erase Disturb Limit (complement sensing mode)	$N_{DFDC}$ CC	-	-	500	cycles	
UCB Erase Disturb Limit	$N_{UCBD}$ CC	-	-	500	cycles	

**表 3-75 Flash (续)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Program time data flash per page 1)2)	$t_{PRD}$ CC	-	-	75	$\mu$ s	8 Byte
Complete Device Flash Erase Time PFlash and DFlash 1)3) 4) 5)	$t_{ER\_Dev}$ CC	-	10.4	18.5 1)3)4)5)	s	Valid for less than 1000 cycles, w/o UCB. Derived value for documentation purpose.
Data Flash program time per burst 1)2)	$t_{PRDB}$ CC	-	-	140	$\mu$ s	32 Byte
Data Flash suspend to read latency 1)	$t_{SPNDD}$ CC	-	-	120	$\mu$ s	
Wait time after margin change	$t_{FL\_MarginDel}$ CC	-	-	2	$\mu$ s	
Program Flash Endurance per Logical Sector	$N_{E\_P}$ CC	-	-	1000	cycles	Replace logical sector command shall be used if a sector fails during erase or program
Number of erase operations per physical sector in program flash	$N_{ERP}$ CC	-	-	16000	cycles	
Program Flash Retention Time, Sector	$t_{RET}$ CC	20	-	-	years	Max. 1000 erase/program cycles
UCB Retention Time	$t_{RTU}$ CC	20	-	-	years	Max. 100 erase/program cycles per UCB, max 500 erase/program cycles for all UCBs together
Data Flash access delay	$t_{DF}$ CC	-	-	100	ns	see RFLASH of DMU register HF_DWAIT
Data Flash ECC Delay	$t_{DFECC}$ CC	-	-	20	ns	see RECC of DMU register HF_DWAIT
Program Flash access delay	$t_{PF}$ CC	-	-	30	ns	see RFLASH of DMU register HF_PWAIT
Program Flash ECC delay	$t_{PFECC}$ CC	-	-	10	ns	see RECC and CECC of DMU register HF_PWAIT
Number of erase operations on DF0 over lifetime (complement sensing mode) 6)	$N_{ERDOC}$ CC	-	-	4000000	cycles	
Number of erase operations on DF0 over lifetime (single ended sensing mode) 7)	$N_{ERDOS}$ CC	-	-	750000	cycles	

**表 3-75 Flash (续)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Number of erase operations on DF1 over lifetime (complement sensing mode) <sup>6)</sup>	$N_{ERD1C} CC$	-	-	2000000	cycles	
Number of erase operations on DF1 over lifetime (single ended sensing mode) <sup>7)</sup>	$N_{ERD1S} CC$	-	-	500000	cycles	
Data Flash Endurance per EEPROMx sector (complement sensing mode) <sup>8)</sup>	$N_{E\_EEP10C} CC$	-	-	500000	cycles	Max. data retention time 10 years
DataFlash Endurance per EEPROMx sector (single ended sensing mode) <sup>8)</sup>	$N_{E\_EEP10S} CC$	-	-	125000	cycles	Retention time and Tj according below example temperature profile
		-	-	125000	cycles	max data retention time 20y, Tj=110°C
		-	-	125000	cycles	max data retention time 8.2y, Tj=125°C
Data Flash Endurance per HSMx sector (complement sensing mode) <sup>8)</sup>	$N_{E\_HSMC} CC$	-	-	250000	cycles	Max. data retention time 10 years
Data Flash Endurance per HSMx sector (single ended sensing mode) <sup>8)</sup>	$N_{E\_HSMs} CC$	-	-	125000	cycles	Retention time and Tj according below example temperature profile
		-	-	125000	cycles	max data retention time 20y, Tj=110°C
		-	-	125000	cycles	max data retention time 8.2y, Tj=125°C
Junction temperature limit for PFlash program/erase operations	$T_{JPFlash} SR$	-	-	150	°C	
Data Flash Erase Time per Sector <sup>1)3)5)</sup>	$t_{ERD1} CC$	-	-	0.5	s	Max. 1000 erase/program cycles
Data Flash Erase Time per Sector <sup>1)3)5)</sup>	$t_{ERDM} CC$	-	-	1.5	s	Max allowed cycles, see NE_EEP10 and NE_HSM parameters
DataFlash Adder on Erase Time per 32kByte erase size when using complement sensing mode <sup>1)</sup>	$t_{ER\_ADDC32C} CC$	-	-	50	ms	Adder per 32 kByte on erase time; applicable only when using complement mode

**表3-75 Flash (续)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data Flash Erase Time per Multi-Sector Command <sup>1)3)5)</sup>	$t_{MERD1\ CC}$	-	-	0.5	s	Max 1000 erase/program cycles; For consecutive logical sectors $\leq 256\text{KBytes}$
Data Flash Erase Time per Multi-Sector Command <sup>1)3)5)</sup>	$t_{MERDM\ CC}$	-	-	1.5	s	Max allowed cycles, see NE_EEP10x and NE_HSMx Parameters; For consecutive logical sectors $\leq 256\text{kByte}$
Program Flash Access Delay at reduced VDDP3 voltage supply during cranking	$t_{PF\_low\_VDDP3\ CC}$	-	-	60	ns	see register DMU_HF_PWAIT.CFL ASH
Data Flash Erase Verify time per page (Complement Sensing) <sup>2)</sup>	$t_{VER\_PAGE\_DC\ CC}$	-	-	10	$\mu\text{s}$	Time per 8 Byte page for Verify Erased Page command
Data Flash Erase Verify time per page (Single Ended Sensing) <sup>1)</sup>	$t_{VER\_PAGE\_DS\ CC}$	-	-	10	$\mu\text{s}$	Time per 8 Byte page for Verify Erased Page command
Program Flash Erase Verify time per page <sup>1)</sup>	$t_{VER\_PAGE\_P\ CC}$	-	-	10	$\mu\text{s}$	Time per 32 Byte page for Verify Erased Page command
Data Flash Erase Verify time per sector (Complement Sensing) <sup>1)</sup>	$t_{VER\_SEC\_DC\ CC}$	-	-	200	$\mu\text{s}$	Time per 2 KB sector for Verify Erased Logical Sector Range command
Data Flash Erase Verify time per sector (Single Ended Sensing) <sup>1)</sup>	$t_{VER\_SEC\_DS\ CC}$	-	-	360	$\mu\text{s}$	Time per 4 KB sector for Verify Erased Logical Sector Range command
Program Flash Erase Verify time per sector <sup>1)</sup>	$t_{VER\_SEC\_P\ CC}$	-	-	360	$\mu\text{s}$	Time per 16KB sector for Verify Erased Logical Sector Range command
Data Flash Erase Verify time per wordline (Complement Sensing) <sup>1)</sup>	$t_{VER\_WL\_DC\ CC}$	-	-	30	$\mu\text{s}$	
Data Flash Erase Verify time per wordline (Single Ended Sensing) <sup>1)</sup>	$t_{VER\_WL\_DS\ CC}$	-	-	50	$\mu\text{s}$	
Program Flash Erase Verify time per wordline <sup>1)</sup>	$t_{VER\_WL\_P\ CC}$	-	-	30	$\mu\text{s}$	

1) 仅对  $f_{FSI} = 100\text{MHz}$  有效。

2) 时间不依赖于编程模式 (5V 或 3.3V)。

- 3) 在超出规格的条件下 (例如,由于过度循环)或激活WL定向缺陷, 擦除过程的持续时间可能会增加高达50%。
- 4) 使用 512 kByte / 256 kByte 擦除指令 (PFlash / DFlash)。
- 5) 如果 DataFlash 在互补感应模式下运行, 则擦除时间将增加  $\text{erasing\_size} / 32\text{kByte} \times t\text{ER\_ADDC32C}$
- 6) 允许将可寻址内存划分为 8 个逻辑扇区; 仍必须进行循环以考虑擦除干扰限制  $N_{\text{DFD}}$ 。
- 7) 允许将可寻址内存划分为 6 个逻辑扇区; 仍必须进行循环以考虑擦除干扰限制  $N_{\text{DFD}}$ 。
- 8) 仅在使用强大的 EEPROM 仿真算法时有效。欲了解更多详细信息, 请参阅用户手册。

### 3.33 质量声明

表 3-76 质量参数

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Moisture Sensitivity Level	$MSL_{CC}$	-	-	3		Conforming to Jedec J-STD--020C for 240C
ESD susceptibility according to Charged Device Model (CDM)	$V_{CDM_{SR}}$	-	-	500 <sup>1)</sup>	V	for all other balls/pins; conforming to JESD22-C101-C
		-	-	750	V	for corner balls/pins; conforming to JESD22-C101-C
ESD susceptibility according to Human Body Model (HBM)	$V_{HBM_{SR}}$	-	-	2000 <sup>2)</sup>	V	Conforming to JESD22-A114-B
ESD susceptibility of the LVDS pins according to Human Body Model (HBM)	$V_{HBM1_{SR}}$	-	-	2000	V	
Operation Lifetime	$t_{OP_{CC}}$	-	-	24500	hour	see below temperature profile as an example

1) AGBT 接口的焊盘最大电压限制为 250V。

2) AGBT 接口的焊盘最大电压限制为 1000V。

#### 温度曲线示例

以下温度曲线就是一个例子。为了满足质量和可靠性目标，特定应用的温度曲线需要经过英飞凌科技的验证。

表 3-77 温度曲线示例

$T_j =$	Duration [h]	Comment
$\leq 170^\circ\text{C}$	$\leq 30$	
$\leq 160^\circ\text{C}$	$\leq 120$	
$\leq 150^\circ\text{C}$	$\leq 220$	
$\leq 140^\circ\text{C}$	$\leq 350$	
$\leq 130^\circ\text{C}$	$\leq 780$	
$\leq 120^\circ\text{C}$	$\leq 1600$	
$\leq 110^\circ\text{C}$	$\leq 3000$	
$\leq 100^\circ\text{C}$	$\leq 7000$	
$\leq 90^\circ\text{C}$	$\leq 8000$	
$\leq 80^\circ\text{C}$	$\leq 2400$	
$\leq 70^\circ\text{C}$	$\leq 1000$	
	$\leq 24500$	total time

表 3-78 非活动寿命温度曲线示例

$T_j$ =	Duration [h]	Comment
$\leq 55^\circ\text{C}$	$\leq 150700$	

3.34 封装外形尺寸

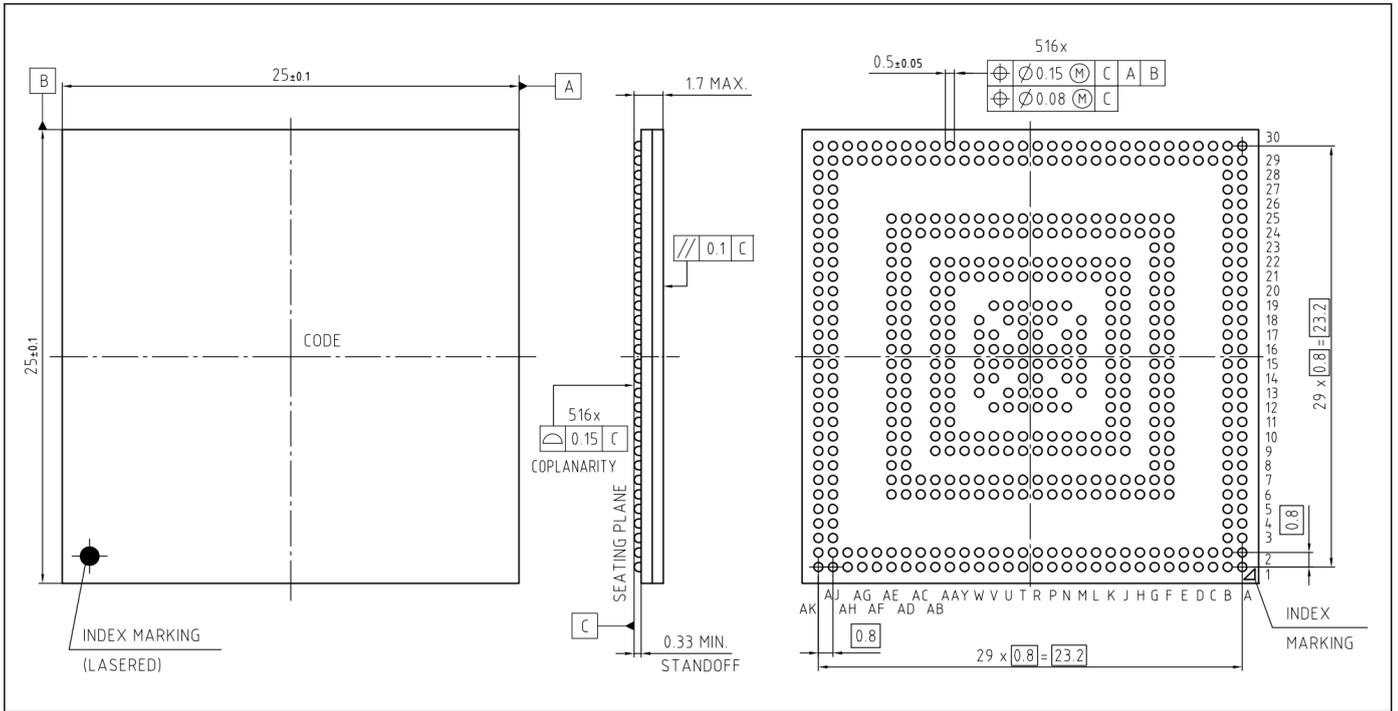


图 3-30 LFBGA-516 封装外形

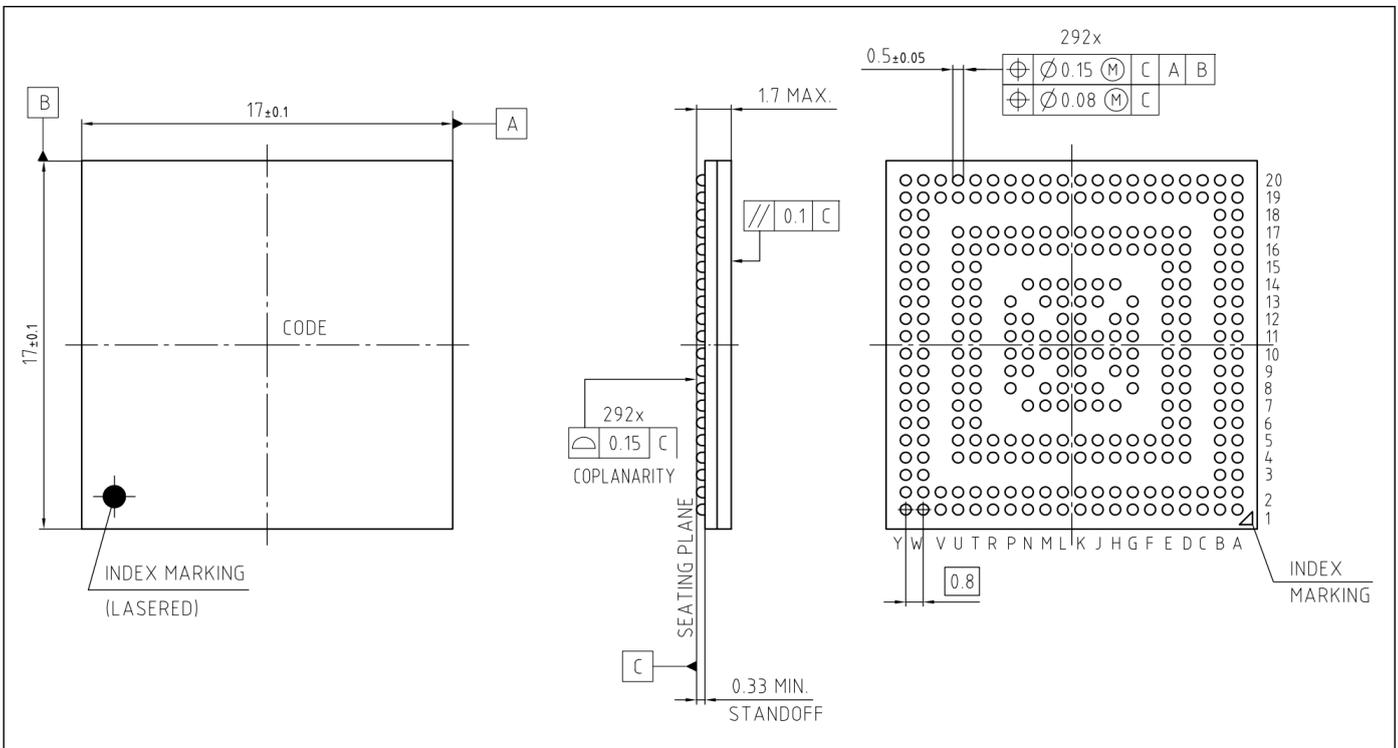


图 3-31 LFBGA-292 封装外形

您可以在我们的英飞凌互联网分页“产品”中找到我们所有的封装、包装种类和其他信息：

<http://www.infineon.com/products>

### 3.34.1 封装参数

表 3-79 封装参数

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance (junction to ambient) <sup>1)</sup>	RTH_JA	-	-	14	K/W	LFBGA292
	CC	-	-	12.2	K/W	LFBGA516
Thermal resistance (junction to case bottom) <sup>1)</sup>	RTH_JCB	-	-	4	K/W	LFBGA292
	CC	-	-	3	K/W	LFBGA516
Thermal resistance (junction to case top) <sup>1)</sup>	RTH_JCT	-	-	5	K/W	LFBGA292
	CC	-	-	5	K/W	LFBGA516

1) 外壳与环境之间的顶部和底部热阻 (RTH\_CTA, RTH\_CBA) 将与上面给出的结与外壳之间的热阻 (RTH\_JCT, RTH\_JCB) 相结合, 以计算结与环境之间的总热阻 (RTH\_JA)。外壳和环境之间的热阻 (RTH\_CTA、RTH\_CBA) 取决于外部系统 (PCB、外壳) 的特性, 由用户负责。结温可使用以下公式计算:  $T_J = T_A + RTH\_JA * P_D$ , 其中 RTH\_JA 是结点与环境之间的总热阻。采用“冷板法” (MIL SPEC-883 方法 1012.1) 测量的热阻。

## 4 记录

Version 0.4 is the first version of this document.

### 4.1 从0.4版本到0.6版本的变更

- Update table Platform Feature Overview
- Changes in Pin Definition and Functions
  - Add pad type RFAST to Legend
  - Corrected ball assignant to NC and NC1
  - P32.0 replace name from EVR13 to EVRC
  - P32.1 replace name from EVR13 to EVRC
  - Add Function description for GTM\_TIM\_INxx Symbols
  - Change numbering for GTM\_TIM\_INxx Symbols
  - Update Function description for CAN signals
  - Add missing Function description for EVADC
  - Add missing Function description for EDSADC
  - Add Function description for GTM\_DTMxx Symbols
  - Update Function description for SCU\_E\_REQ signals
  - Change Symbol for SCU\_E\_REQ signals
  - Update Function description for SCU\_PD\_HWCFGx signals
  - Add QSPI5\_SCLK to P14.10
  - Remove SDMMC\_DS from P15.2
  - Remove PLL\_WRAPPER\_ANA\_0\_PAD\_SYSCLK
  - Switch CBS\_TGyz from inverted to non inverted
  - Change Symbol from HSCTPHY\_1\_RXDx to HSCT1\_RXDx
  - Change Symbol from SCU\_EMGSTOP\_B\_RIQ to SCU\_EMGSTOP\_PORT\_B
  - Add CCUEXTCLK0
  - Add EDSADC\_EDS9NB to AN70
  - Add EDSADC\_EDS9NB to AN71
  - Add PMS\_DCDCSYNCO to P32.4
  - Add DAP3 to P21.6
  - Remove SDMMC\_DS from P15.2
  - ADD TDI to P21.6
  - Add DAPE1 to P21.6
  - Add DAP2 to P21.7
  - ADD TDO to P21.7
  - Remove DAP Function description from P21.7 Input
  - Change Symbol HSDPM\_HSDPM\_xxx to HSDPM\_xxx
  - Switch EBU\_x from inverted to non inverted
  - Add HSDPM\_MUTE to P22.3
  - Add HSDPM\_BS0 to P22.4

- Change P22.4 from SLOW to FAST
- Add HSDPM\_BS1 to P22.5
- Change P22.5 from SLOW to FAST
- Change Symbol from SCU\_EMGSTOP\_A\_RIQ to SCU\_EMGSTOP\_PORT\_A
- Add EVADC\_G5CH2 to AN50
- Add EDSADC\_EDS9PB to AN70
- Add EDSADC\_EDS9NB to AN71
- Add Buffer Type to ABGT Symbols
- Changes in table 'Overload Parameters' of Overload
  - Change max value of  $K_{OVND}$  from  $6 \cdot 10^{-4}$  to  $1 \cdot 10^{-4}$
  - Change note of KOVDN from 'Overload injected on GPIO non LVDS pad and affecting neighbor slow pads;  $-2\text{mA} < I_{IN} < 0\text{mA}$ ' to 'Overload injected on GPIO non LVDS pad and affecting neighbor slow pads;  $-5\text{mA} < I_{IN} < 0\text{mA}$ '
  - Change note of  $K_{OVND}$  from ' $1.7 \cdot 10^{-3}$ ' to ' $3 \cdot 10^{-4}$ '
  - Change max value of  $K_{OVND}$  from 0.3 to 0.5
  - Change note of  $K_{OVND}$  from 'Overload injected on LVDS pad and affecting neighbor LVDS pads' to 'Overload injected on LVDS TX pad and affecting neighbor LVDS pads'
  - Change max value of  $K_{OVDP}$  from  $5 \cdot 10^{-4}$  to  $5 \cdot 10^{-3}$
  - Change note of  $K_{OVDP}$  from 'Overload injected on LVDS pad and affecting neighbor LVDS pads' to 'Overload injected on LVDS TX pad and affecting neighbor LVDS pads'
  - Change note of  $K_{OVDP}$  from ' $1 \cdot 10^{-5}$ ' to ' $1.5 \cdot 10^{-3}$ '
  - Change max value of  $K_{OVAN}$  from  $1 \cdot 10^{-4}$  to  $1 \cdot 10^{-5}$
  - Change note of  $K_{OVAN}$  from 'Analog Inputs overlaid with class slow pads or pull down diagnostics;  $-1\text{mA} < I_{IN} < 0\text{mA}$ ' to 'Analog Inputs overlaid with class slow pads or pull down diagnostics;  $-5\text{mA} < I_{IN} < 0\text{mA}$ '
  - Change note of  $K_{OVAN}$  from ' $1 \cdot 10^{-3}$ ' to ' $1 \cdot 10^{-4}$ '
  - Change note of  $K_{OVAP}$  from ' $1 \cdot 10^{-5}$ ' to ' $2 \cdot 10^{-5}$ '
  - Change note of  $K_{OVAP}$  from ' $1 \cdot 10^{-4}$ ' to ' $2 \cdot 10^{-4}$ '
  - Add parameter  $I_{OUT}$
- Operating Conditions
  - Change note of  $V_{DDM}$  from 'Upper voltage range' to ''
  - Change note of  $V_{DDM}$  from 'Lower voltage range' to ''
  - Change note of  $V_{EVRSB}$  from ' $V_{EVRSB}$  is bonded together with  $V_{EXT}$  supply pin in smaller LQFP packages.' to ''
- Changes in table 'PORST Pad' of Standard Pads
  - Change note of HYS from 'non of the neighbor pads are used as output; TTL' to 'non of the neighbor pads are used as output;TTL (degraded, used for CIF)'
  - Change min value of HYS from  $0.1 \cdot V_{EXT/FLEX}$  V to  $0.055 \cdot V_{EXT/FLEX}$  V
  - Change min value of  $I_{PDL}$  from  $|18| \mu\text{A}$  to  $|15| \mu\text{A}$
  - Change note of HYS from 'two of the neighbor pads are used as output with driver=strong and edge=sharp; TTL' to 'two of the neighbor pads are used as output with driver=strong and edge=sharp; TTL (degraded, used for CIF)'
- Changes in table 'Fast 5V GPIO' of Standard Pads
  - Change note of HYS from ' $0.1 \cdot V_{EXT/FLEX}$  V' to ' $0.09 \cdot V_{EXT/FLEX}$  V'
  - Change min value of HYS from  $0.09 \cdot V_{EXT/FLEX}$  V to  $0.075 \cdot V_{EXT/FLEX}$  V

**修订记录 从0.4版本到0.6版本的变更**

- Change min value of  $R_{\text{DSON}}$  from 140 Ohm to 125 Ohm
- Change typ value of  $R_{\text{DSON}}$  from 200 Ohm to 225 Ohm
- Change max value of  $R_{\text{DSON}}$  from 260 Ohm to 320 Ohm
- Change note of  $R_{\text{DSON}}$  from '35 Ohm' to '31 Ohm'
- Change note of  $R_{\text{DSON}}$  from '50 Ohm' to '55 Ohm'
- Change max value of  $R_{\text{DSON}}$  from 65 Ohm to 80 Ohm
- Change note of  $t_{\text{RF}}$  from ' $C_L = 25\text{pF}$ ; driver = strong sharp edge' to ' $C_L = 25\text{pF}$ ; driver = strong sharp edge; from  $0.2 * V_{\text{EXT/FLEX}}$  to  $0.8 * V_{\text{EXT/FLEX}}$ '
- Change max value of  $t_{\text{RF}}$  from 2.8 ns to 3.2 ns
- Change min value of  $t_{\text{RF}}$  from  $0.5+0.075*C_L$  ns to  $0.5+0.08*C_L$  ns
- Change note of  $t_{\text{RF}}$  from ' $0.5+0.15*C_L$  ns' to ' $1.0+0.17*C_L$  ns'
- Change note of  $t_{\text{RF}}$  from ' $2.5+0.18*C_L$  ns' to ' $1.0+0.18*C_L$  ns'
- Change note of  $t_{\text{RF}}$  from ' $2.5+0.35*C_L$  ns' to ' $5.0+0.35*C_L$  ns'
- Change max value of  $t_{\text{RF}}$  from  $4+0.95*C_L$  ns to  $12+1.0*C_L$  ns
- Change note of  $I_{\text{OZ}}$  from '-3900 nA' to '-5000 nA'
- Change note of  $I_{\text{OZ}}$  from '-3600 nA' to '-5000 nA'
- Change note of  $I_{\text{OZ}}$  from '-6700 nA' to '-9000 nA'
- Change note of  $I_{\text{OZ}}$  from '3900 nA' to '5000 nA'
- Change max value of  $I_{\text{OZ}}$  from 3600 nA to 5000 nA
- Change note of  $I_{\text{OZ}}$  from '6700 nA' to '9000 nA'
- Change note of  $t_{\text{RF}}$  from ' $C_L = 25\text{pF}$ ; driver = strong sharp edge' to ' $C_L = 25\text{pF}$ ; driver = strong sharp edge; from  $0.2 * V_{\text{EXT/FLEX}}$  to  $0.8 * V_{\text{EXT/FLEX}}$ '
- Change note of  $f_{\text{IND}}$  from '' to 'AL and TTL'
- Change note of  $f_{\text{OUTD}}$  from '' to 'medium driver'
- Change note of  $I_{\text{PDL}}$  from ' $V_{\text{IL}}$ ; AL or TTL' to ' $V_{\text{IL}}$ ; AL'
- Changes in table 'Fast 3.3V GPIO' of Standard Pads
  - Change min value of  $HYS$  from  $0.065 * V_{\text{EXT/FLEX}}$  V to  $0.055 * V_{\text{EXT/FLEX}}$  V
  - Change min value of  $HYS$  from  $0.1 * V_{\text{EXT/FLEX}}$  V to  $0.09 * V_{\text{EXT/FLEX}}$  V
  - Change min value of  $HYS$  from  $0.07 * V_{\text{EXT/FLEX}}$  V to  $0.055 * V_{\text{EXT/FLEX}}$  V
  - Change note of  $R_{\text{DSON}}$  from '140 Ohm' to '125 Ohm'
  - Change typ value of  $R_{\text{DSON}}$  from 200 Ohm to 225 Ohm
  - Change note of  $R_{\text{DSON}}$  from '300 Ohm' to '320 Ohm'
  - Change min value of  $R_{\text{DSON}}$  from 35 Ohm to 31 Ohm
  - Change typ value of  $R_{\text{DSON}}$  from 50 Ohm to 55 Ohm
  - Change max value of  $R_{\text{DSON}}$  from 77 Ohm to 80 Ohm
  - Change note of  $t_{\text{RF}}$  from ' $C_L = 25\text{pF}$ ; driver = strong sharp edge' to ' $C_L = 25\text{pF}$ ; driver = strong sharp edge; from  $0.2 * V_{\text{EXT/FLEX}}$  to  $0.8 * V_{\text{EXT/FLEX}}$ '
  - Change min value of  $t_{\text{RF}}$  from 2 ns to 1.6 ns
  - Change note of  $t_{\text{RF}}$  from ' $0.75+0.15*C_L$  ns' to ' $2.5+0.21*C_L$  ns'
  - Change min value of  $t_{\text{RF}}$  from  $4+0.57*C_L$  ns to  $2+0.57*C_L$  ns
  - Change note of  $t_{\text{RF}}$  from ' $1.5+0.38*C_L$  ns' to ' $8+0.4*C_L$  ns'
  - Change note of  $t_{\text{RF}}$  from ' $7+1.1*C_L$  ns' to ' $10+1.25*C_L$  ns'

- Change note of  $I_{PUH}$  from '|19|  $\mu\text{A}$ ' to '|17|  $\mu\text{A}$ '
- Change min value of  $I_{PUH}$  from |9|  $\mu\text{A}$  to |11|  $\mu\text{A}$
- Change min value of  $I_{PDL}$  from |18|  $\mu\text{A}$  to |15|  $\mu\text{A}$
- Change min value of  $I_{OZ}$  from -4100 nA to -5000 nA
- Change note of  $I_{OZ}$  from '-3600 nA' to '-5000 nA'
- Change note of  $I_{OZ}$  from '-6700 nA' to '-9000 nA'
- Change note of  $I_{OZ}$  from '4100 nA' to '5000 nA'
- Change max value of  $I_{OZ}$  from 3600 nA to 5000 nA
- Change note of  $I_{OZ}$  from '6700 nA' to '9000 nA'
- Change note of  $t_{RF}$  from ' $C_L = 25\text{pF}$ ; driver = strong sharp edge' to ' $C_L = 25\text{pF}$ ; driver = strong sharp edge; from  $0.2 * V_{EXT/FLEX}$  to  $0.8 * V_{EXT/FLEX}$ '
- Change note of  $f_{OUTD}$  from '' to 'medium driver'
- Changes in table 'Slow 5V GPIO' of Standard Pads
  - Change note of  $HYS$  from ' $0.1 * V_{EXT/FLEX}$  V' to ' $0.09 * V_{EXT/FLEX}$  V'
  - Change note of  $HYS$  from ' $0.09 * V_{EXT/FLEX}$  V' to ' $0.075 * V_{EXT/FLEX}$  V'
  - Change min value of  $R_{DSON}$  from 140 Ohm to 125 Ohm
  - Change typ value of  $R_{DSON}$  from 200 Ohm to 225 Ohm
  - Change note of  $R_{DSON}$  from '260 Ohm' to '320 Ohm'
  - Change max value of  $t_{RF}$  from  $3.5 + 0.55 * C_L$  ns to  $7 + 0.55 * C_L$  ns
  - Change note of  $t_{RF}$  from ' $4 + 0.95 * C_L$  ns' to ' $12 + 1 * C_L$  ns'
  - Change note of  $I_{PUH}$  from ' $V_{IH}$ ; AL or TTL' to ' $V_{IH}$ ; AL or TTL; except VGATE1P and  $T_J > 150^\circ\text{C}$ '
  - Change note of  $I_{PUH}$  from ' $V_{IL}$ ; AL or TTL' to ' $V_{IL}$ ; AL or TTL; except VGATE1P and  $T_J > 150^\circ\text{C}$ '
  - Change note of  $I_{PDL}$  from ' $V_{IL}$ ; AL or TTL' to ' $V_{IL}$ ; AL'
- Changes in table 'Slow 3.3V GPIO' of Standard Pads
  - Change note of  $HYS$  from ' $0.1 * V_{EXT/FLEX}$  V' to ' $0.09 * V_{EXT/FLEX}$  V'
  - Change min value of  $HYS$  from  $0.065 * V_{EXT/FLEX}$  V to  $0.055 * V_{EXT/FLEX}$  V
  - Change min value of  $HYS$  from  $0.07 * V_{EXT/FLEX}$  V to  $0.055 * V_{EXT/FLEX}$  V
  - Change min value of  $R_{DSON}$  from 140 Ohm to 125 Ohm
  - Change typ value of  $R_{DSON}$  from 200 Ohm to 225 Ohm
  - Change note of  $R_{DSON}$  from '300 Ohm' to '320 Ohm'
  - Change note of  $t_{RF}$  from ' $4 + 0.57 * C_L$  ns' to ' $2 + 0.57 * C_L$  ns'
  - Change max value of  $t_{RF}$  from  $7 + 1.1 * C_L$  ns to  $10 + 1.25 * C_L$  ns
  - Change note of  $I_{PUH}$  from ' $V_{IH}$ ; AL and TTL (degraded, used for CIF)' to ' $V_{IH}$ ; AL and TTL (degraded, used for CIF); except VGATE1P and  $T_J > 150^\circ\text{C}$ '
  - Change min value of  $I_{PUH}$  from |19|  $\mu\text{A}$  to |17|  $\mu\text{A}$
  - Change note of  $I_{PUH}$  from ' $V_{IH}$ ; TTL' to ' $V_{IH}$ ; TTL; except VGATE1P and  $T_J > 150^\circ\text{C}$ '
  - Change min value of  $I_{PUH}$  from |9|  $\mu\text{A}$  to |11|  $\mu\text{A}$
  - Change note of  $I_{PDL}$  from '|18|  $\mu\text{A}$ ' to '|15|  $\mu\text{A}$ '
  - Change note of  $I_{PUH}$  from ' $V_{IL}$ ; AL and TTL and TTL (degraded, used for CIF)' to ' $V_{IL}$ ; AL and TTL and TTL (degraded, used for CIF); except VGATE1P and  $T_J > 150^\circ\text{C}$ '
  - Change note of  $f_{OUTD}$  from '' to 'medium driver'
- Changes in table 'Class S 5V' of Standard Pads

## 修订记录 从0.4版本到0.6版本的变更

- Change note of  $HYS$  from  $0.1 * V_{EXT/FLEX} V$  to  $0.09 * V_{EXT/FLEX} V$
- Change min value of  $HYS$  from  $0.09 * V_{EXT/FLEX} V$  to  $0.075 * V_{EXT/FLEX} V$
- Change note of  $I_{PDL}$  from ' $V_{IL}; AL$  or  $TTL$ ' to ' $V_{IL}; AL$ '
- Change note of  $I_{OZ}$  from ' $T_J \leq 150^\circ C$ ; PDD option available, or AltRef option available and EDSADC channel connected or AN70 or AN71' to ' $T_J \leq 150^\circ C$ ; PDD option available, or AltRef option available and EDSADC channel connected, or two EDSADC channels connected'
- Changes in table 'RFast 3.3V pad' of Standard Pads
  - Change note of  $HYS$  from  $0.065 * V_{EXT/FLEX} V$  to  $0.055 * V_{EXT/FLEX} V$
  - Change note of  $HYS$  from  $0.1 * V_{EXT/FLEX} V$  to  $0.09 * V_{EXT/FLEX} V$
  - Change note of  $HYS$  from  $0.07 * V_{EXT/FLEX} V$  to  $0.055 * V_{EXT/FLEX} V$
  - Change min value of  $R_{DSON}$  from 140 Ohm to 125 Ohm
  - Change note of  $R_{DSON}$  from '200 Ohm' to '225 Ohm'
  - Change note of  $R_{DSON}$  from '300 Ohm' to '320 Ohm'
  - Change min value of  $R_{DSON}$  from 35 Ohm to 31 Ohm
  - Change typ value of  $R_{DSON}$  from 50 Ohm to 55 Ohm
  - Change max value of  $R_{DSON}$  from 77 Ohm to 80 Ohm
  - Change min value of  $R_{DSON}$  from 10 Ohm to 8 Ohm
  - Change note of  $t_{RF}$  from ' $C_L = 25pF$ ; driver = strong sharp edge' to ' $C_L = 25pF$ ; driver = strong sharp edge; from  $0.2 * V_{EXT/FLEX}$  to  $0.8 * V_{EXT/FLEX}$ '
  - Change min value of  $t_{RF}$  from 2 ns to 1.6 ns
  - Change min value of  $t_{RF}$  from  $4+0.57*C_L$  ns to  $2+0.57*C_L$  ns
  - Change note of  $t_{RF}$  from ' $0.75+0.15*C_L$  ns' to ' $2.5+0.21*C_L$  ns'
  - Change max value of  $t_{RF}$  from  $1.5+0.38*C_L$  ns to  $8+0.4*C_L$  ns
  - Change note of  $t_{RF}$  from ' $7+1.1*C_L$  ns' to ' $10+1.25*C_L$  ns'
  - Change min value of  $I_{PUH}$  from |19|  $\mu A$  to |17|  $\mu A$
  - Change note of  $I_{PUH}$  from '|9|  $\mu A$ ' to '|11|  $\mu A$ '
  - Change note of  $I_{PDL}$  from '|18|  $\mu A$ ' to '|15|  $\mu A$ '
  - Change note of  $t_{RF}$  from ' $C_L = 25pF$ ; driver = strong sharp edge' to ' $C_L = 25pF$ ; driver = strong sharp edge; from  $0.2 * V_{EXT/FLEX}$  to  $0.8 * V_{EXT/FLEX}$ '
  - Change note of  $f_{OUTD}$  from '' to 'medium driver'
- Changes in table 'RFast 5V GPIO' of Standard Pads
  - Change min value of  $HYS$  from  $0.1 * V_{EXT/FLEX} V$  to  $0.09 * V_{EXT/FLEX} V$
  - Change note of  $HYS$  from  $0.09 * V_{EXT/FLEX} V$  to  $0.075 * V_{EXT/FLEX} V$
  - Change min value of  $R_{DSON}$  from 140 Ohm to 125 Ohm
  - Change note of  $R_{DSON}$  from '260 Ohm' to '320 Ohm'
  - Change note of  $R_{DSON}$  from '200 Ohm' to '225 Ohm'
  - Change note of  $R_{DSON}$  from '35 Ohm' to '31 Ohm'
  - Change max value of  $R_{DSON}$  from 65 Ohm to 80 Ohm
  - Change note of  $R_{DSON}$  from '50 Ohm' to '55 Ohm'
  - Change min value of  $t_{RF}$  from  $2.5+0.18*C_L$  ns to  $1.0+0.18*C_L$  ns
  - Change note of  $t_{RF}$  from '" $C_L = 25pF$ ; driver = strong sharp edge"' to '" $C_L = 25pF$ ; driver = strong sharp edge; from  $0.2 * V_{EXT/FLEX}$  to  $0.8 * V_{EXT/FLEX}$ "'
  - Change note of  $t_{RF}$  from '2.8 ns' to '3.2 ns'

**修订记录 从0.4版本到0.6版本的变更**

- Change note of  $t_{RF}$  from ' $0.5+0.075 \cdot C_L$  ns' to ' $0.5+0.08 \cdot C_L$  ns'
- Change max value of  $t_{RF}$  from  $0.5+0.15 \cdot C_L$  ns to  $1.0+0.17 \cdot C_L$  ns
- Change note of  $t_{RF}$  from ' $4+0.95 \cdot C_L$  ns' to ' $12+1.0 \cdot C_L$  ns'
- Change max value of  $t_{RF}$  from  $2.5+0.35 \cdot C_L$  ns to  $5.0+0.35 \cdot C_L$  ns
- Change note of  $t_{RF}$  from ' $C_L = 25$  pF; driver = strong sharp edge' to ' $C_L = 25$  pF; driver = strong sharp edge; from  $0.2 \cdot V_{EXT/FLEX}$  to  $0.8 \cdot V_{EXT/FLEX}$ '
- Change note of  $f_{IND}$  from '' to 'AL and TTL'
- Change note of  $f_{OUTD}$  from '' to 'medium driver'
- Change note of  $I_{PDL}$  from ' $V_{IL}$ ; AL or TTL' to ' $V_{IL}$ ; AL'
- Changes in table 'Class D' of Standard Pads
  - Update footnote of *Standard Pads* to 'For AN11 200 nA need to be added.'
  - Change note of  $I_{OZ}$  from ' $T_J \leq 150^\circ\text{C}$ ; PDD option available, or AltRef option available and EDSADC channel connected' to ' $T_J \leq 150^\circ\text{C}$ ; PDD option available, or AltRef option available and EDSADC channel connected, or two EDSADC channels connected'
- Changes in table 'LVDS - IEEE standard LVDS general purpose link (GPL)' of LVDS Pads
  - Change max value of  $t_{rise20}$  from 0.5 ns to 0.75 ns
  - Change max value of  $t_{fall20}$  from 0.5 ns to 0.75 ns
  - Change max value of  $V_{OD}$  from 450 mV to 500 mV
  - Change min value of  $V_{OD}$  from 360 mV to 380 mV
- VADC 5V
  - Change max value of  $dV_{CSD}$  from 20 % to 10 %
  - Change note of  $dV_{CSD}$  from '-20 %' to '-10 %'
  - Change note of  $f_{ADCI}$  from 'Upper voltage range' to ' $4.5\text{V} \leq V_{DDM} \leq 5.5\text{V}$ '
  - Change note of  $t_{SCAL}$  from 'Upper voltage range' to ' $4.5\text{V} \leq V_{DDM} \leq 5.5\text{V}$ '
  - Change note of  $f_{ADCI}$  from 'Lower voltage range' to ' $2.97\text{V} \leq V_{DDM} < 4.5\text{V}$ '
  - Change note of  $t_S$  from 'Primary group or fast compare channel, upper voltage range; input buffer disabled' to 'Primary group or fast compare channel,  $4.5\text{V} \leq V_{DDM} \leq 5.5\text{V}$ ; input buffer disabled'
  - Change note of  $t_{SCAL}$  from 'Lower voltage range' to ' $2.97\text{V} \leq V_{DDM} < 4.5\text{V}$ '
  - Change note of  $t_S$  from 'Primary group or fast compare channel, upper voltage range; input buffer enabled' to 'Primary group or fast compare channel,  $4.5\text{V} \leq V_{DDM} \leq 5.5\text{V}$ ; input buffer enabled'
  - Change note of  $t_S$  from 'Secondary group, upper voltage range; input buffer disabled' to 'Secondary group,  $4.5\text{V} \leq V_{DDM} \leq 5.5\text{V}$ ; input buffer disabled'
  - Change note of  $t_S$  from 'Secondary group, upper voltage range; input buffer enabled' to 'Secondary group,  $4.5\text{V} \leq V_{DDM} \leq 5.5\text{V}$ ; input buffer enabled'
  - Change note of  $t_S$  from 'Primary Group or fast compare channel, lower voltage range; input buffer disabled' to 'Primary Group or fast compare channel,  $2.97\text{V} \leq V_{DDM} < 4.5\text{V}$ ; input buffer disabled'
  - Change note of  $t_S$  from 'Primary group or fast compare channel, lower voltage range; input buffer enabled' to 'Primary group or fast compare channel,  $2.97\text{V} \leq V_{DDM} < 4.5\text{V}$ ; input buffer enabled'
  - Change note of  $t_S$  from 'Secondary group, lower voltage range; input buffer disabled' to 'Secondary group,  $2.97\text{V} \leq V_{DDM} < 4.5\text{V}$ ; input buffer disabled'
  - Change note of  $t_S$  from 'Secondary group, lower voltage range; input buffer enabled' to 'Secondary group,  $2.97\text{V} \leq V_{DDM} < 4.5\text{V}$ ; input buffer enabled'
- DSADC 5V
  - Update wording in front of table DSADC 5V

## 修订记录 从0.4版本到0.6版本的变更

- Change note of  $DCF$  from ' $10^{-5}f_D$ , offset compensation filter enabled (FCFGMx.OEN = 001<sub>B</sub>)' to ' $10^{-5}f_D$ , offset compensation filter enabled (FCFGMx.OCEN = 001<sub>B</sub>)'
- OSC\_XTAL
  - Change note of  $C_{L1}$  from '2.35 pF' to '3.35 pF'
  - Add parameter  $C_{XTAL1}$
- Changes in table 'DTS PMS' of DTS
  - Change max value of  $t_M$  from 2.6 ms to 2.7 ms
- Add table 'DTS Core'
- Current Consumption
  - Change max value of  $I_{DDRAIL}$  from 1370 mA to 1372 mA
  - Change  $T_J$  in real power pattern definition from 150°C to 160°C
- Changes in table 'Module Core Current Consumption' of Current Consumption
  - Change name of *Module Core Current Consumption* from Module Core Current Consumption to Module Core Current Consumption
  - Change note of  $I_{DDCX0}$  from 'real power pattern' to 'real power pattern; IPC=0.6'
  - Change max value of  $I_{DDCX0}$  from 40 mA to 45 mA
  - Change note of  $I_{DDCX0}$  from "max power pattern" to "max power pattern; IPC=1.2"
  - Change note of  $I_{DDCX0}$  from '60 mA' to '70 mA'
  - Change note of  $I_{DDCX}$  from "max power pattern" to "max power pattern; IPC=1.2"
  - Change note of  $I_{DDCX}$  from ' $I_{DDCX0} + 60$  mA' to ' $I_{DDCX0} + 50$  mA'
  - Change note of  $I_{DDGTM}$  from 'real power pattern; TIMx, TOMx, ATOMx, MCSx active. 5 clusters at 200 MHz.' to 'real power pattern; TIMx, TOMx, ATOMx, MCSx active. 3 clusters at 200 MHz.'
  - Change max value of  $I_{DDGTM}$  from 60 mA to 130 mA
  - Change note of  $I_{DDGTM}$  from '88 mA' to '160 mA'
  - Change note of  $I_{DDSPU}$  from "CTRL.DIV = 01 ; FFT clocked at half SPU Clock" to "CTRL.DIV = 01 ; FFT clocked at half SPU Clock; Both SPU modules are active."
  - Change note of  $I_{DDSPU}$  from '60 mA' to '70 mA'
  - Change note of  $I_{DDCIF}$  from '20 mA' to '30 mA'
  - Change note of  $I_{DDMBIST}$  from '100 mA' to '200 mA'
  - Change note of  $I_{DDCX}$  from 'real power pattern' to 'real power pattern; IPC=0.6'
  - Change note of  $I_{DDGTM}$  from 'TIMx, TOMx active at 100MHz. ATOMx, MCSx, DPLL inactive.' to 'TIMx, TOMx active at 100MHz. ATOMx, MCSx, DPLL inactive. 2 clusters at 100 MHz.'
  - Change max value of  $I_{DDGTM}$  from 20 mA to 60 mA
  - Change note of  $I_{EXTRAIL}$  from '58 mA' to '54 mA'
  - Change max value of  $I_{EXTRAIL}$  from t.b.d mA to 60 mA
  - Change max value of  $I_{EXTFLEX}$  from 30 mA to 22 mA
- Changes in table 'Module Current Consumption' of Current Consumption
  - Change max value of  $I_{EXTLVDS}$  from t.b.d mA to 20 mA
  - Change max value of  $I_{SCRSB}$  from 4 mA to 6.5 mA
  - Change description of  $I_{SCRSB}$  from 'SCR 8-bit Standby Controller in STANDBY Mode drawn at  $V_{EVRSB}$  supply pin' to 'SCR 8-bit Standby Controller current incl. PMS in STANDBY Mode drawn at  $V_{EVRSB}$  supply pin'

**修订记录 从0.4版本到0.6版本的变更**

- Change note of  $I_{SCR_{RSB}}$  from 'SCR power pattern;  $f_{SYS\_SCR} = 20\text{MHz}$ ;  $T_J = 150^\circ\text{C}$ ' to 'SCR power pattern incl. PMS current consumption with fback clock active;  $f_{SYS\_SCR} = 20\text{MHz}$ ;  $T_J = 150^\circ\text{C}$ '
- Change note of  $I_{SCR_{RSB}}$  from 'real power pattern;  $f_{SYS\_SCR} = 70\text{kHz}$ ;  $T_J = 25^\circ\text{C}$ ' to 'SCR power pattern incl. PMS current consumption with fback inactive;  $f_{SYS\_SCR} = 70\text{kHz}$ ;  $T_J = 25^\circ\text{C}$ '
- Change typ value of  $I_{SCR_{RSB}}$  from 0.025 mA to 0.190 mA
- Change description of  $I_{SCR_{RSB}}$  from 'SCR 8-bit Standby Controller in STANDBY Mode drawn at  $V_{EVR_{RSB}}$  supply pin' to 'SCR 8-bit Standby Controller current incl. PMS in STANDBY Mode drawn at  $V_{EVR_{RSB}}$  supply pin'
- Change note of  $I_{DDM}$  from "real power pattern ; current for EDSADC module only; 11 EDSADC channels active." to "real power pattern; current for EDSADC modules only and EVADC modules are inactive; 11 EDSADC channels active continuously."
- Change note of  $I_{DDM}$  from '66 mA' to '44 mA'
- Change note of  $I_{DDM}$  from 'max power pattern; All EDSADC channels active 100% time.' to 'max power pattern; current for EDSADC modules only and EVADC modules are inactive; all EDSADC channels active continuously.'
- Change max value of  $I_{DDM}$  from 84 mA to 63 mA
- Change note of  $I_{DDM}$  from 'real pattern; 12 EVADC modules active' to 'real power pattern; current for EVADC modules only and EDSADC modules are inactive; 12 EVADC modules active.'
- Change note of  $I_{DDM}$  from 'max power pattern; All EVADC modules are active 100% time' to 'max power pattern; current for EVADC modules only and EDSADC modules are inactive; all EVADC modules active.'
- Change max value of  $I_{DDM}$  from 26 mA to 20 mA
- Change max value of  $I_{DDM}$  from 82 mA to 60 mA
- Change max value of  $I_{DDTOT}$  from 1506 mA to 1536 mA
- Change note of  $I_{DDTOTDC3}$  from 'real power pattern;  $V_{EXT} = 3.3\text{V}$ ;  $T_J = 160^\circ\text{C}$ ' to 'real power pattern; EVRC reset settings with 72% efficiency;  $V_{EXT} = 3.3\text{V}$ ;  $T_J = 160^\circ\text{C}$ '
- Change max value of  $I_{DDTOTDC3}$  from 830 mA to 980 mA
- Change description of  $I_{DDTOTDC3}$  from ' $\Sigma$  Sum of all currents with DC-DC EVR13 regulator active' to ' $\Sigma$  Sum of all currents with DC-DC EVRC regulator active'
- Change note of  $I_{DDTOTDC5}$  from 'real power pattern;  $V_{EXT} = 5\text{V}$ ;  $T_J = 160^\circ\text{C}$ ' to 'real power pattern; EVRC reset settings with 72% efficiency;  $V_{EXT} = 5\text{V}$ ;  $T_J = 160^\circ\text{C}$ '
- Change max value of  $I_{DDTOTDC5}$  from 600 mA to 670 mA
- Change description of  $I_{DDTOTDC5}$  from ' $\Sigma$  Sum of all currents with DC-DC EVR13 regulator active' to ' $\Sigma$  Sum of all currents with DC-DC EVRC regulator active'
- Change note of  $I_{SLEEP}$  from '10 mA' to '25 mA'
- Change note of  $PD$  from 't.b.d. mW' to '3220 mW'
- Change max value of  $PD$  from 2560 mW to 2500 mW
- Change max value of  $I_{EVR_{RSB}}$  from 4 mA to 8 mA
- Change note of  $I_{EVR_{RSB}}$  from 'real power pattern; PMS/EVR module current considered without SCR and Standby RAM' to 'real power pattern; PMS/EVR module current considered without SCR and Standby RAM during RUN mode.'
- Change max value of  $I_{DDTOT}$  from 1690 mA to 1720 mA
- RESET
  - Change min value of  $t_{POH}$  from 100 ns to 150 ns
  - Change note of  $t_{BP}$  from ' $dV/dT = 1\text{V/ms}$ . including EVR ramp-up and Firmware execution time; RAM initialization and HSM boot time is not included' to ' $dV_{EXT}/dT = 1\text{V/ms}$ .  $V_{EXT} > VLVD_{RST5}$ . Boot time after

- Cold PORST including EVR ramp-up and Firmware execution time; RAM initialization and HSM boot time are not included.'
- Change note of  $t_B$  from 'operating with max. frequencies' to 'operating with max. frequencies, with valid BMI header'
  - Change note of  $t_{BS}$  from '' to 'RAM initialization and HSM boot time are not included, with valid BMI header'
  - Change note of  $t_{BP}$  from 'Firmware execution time; without EVR ramp-up; RAM initialization and HSM boot time is not included' to 'Firmware execution time after warm PORST without EVR ramp-up; RAM initialization and HSM boot time is not included'
  - Change type of  $t_{POA}$  from CC to SR
  - Change description of  $t_{POA}$  from 'Minimum PORST active hold time externally after power supplies are stable at operating levels' to 'Minimum PORST active hold time externally after power supplies are stable at operating levels after start-up'
- PMS/EVR33 LDO
    - Change note of  $dV_{out}/dI_{out}$  from 'Normal RUN mode;  $dI=10$  to  $60$  to  $100mA$ ;  $dt=20ns$ ;  $T_{settle}=20us$ ' to 'Normal RUN mode;  $dI=10$  to  $60mA$ ;  $dt=20ns$ ;  $T_{settle}=20us$ '
    - Change note of  $dV_{out}/dI_{out}$  from 'Normal RUN mode;  $dI=100$  to  $60$  to  $10mA$ ;  $dt=20ns$ ;  $T_{settle}=20us$ ' to 'Normal RUN mode;  $dI=60$  to  $10mA$ ;  $dt=20ns$ ;  $T_{settle}=20us$ '
    - Change note of  $dV_{out}/dV_{in}$  from ' $dV_{in}/dT=1V/ms$ ;  $dV=5$  to  $3.6V$ ' to ' $dV_{in}/dT=1V/ms$ ;  $dV=5$  to  $3.6V$ ;  $I_{MAX}=60mA$ '
    - Change note of  $dV_{out}/dV_{in}$  from ' $dV_{in}/dT=1V/ms$ ;  $dV=3.6$  to  $5V$ ' to ' $dV_{in}/dT=1V/ms$ ;  $dV=3.6$  to  $5V$ ;  $I_{MAX}=60mA$ '
    - Change typ value of  $C_{OUT}$  from  $1\ \mu F$  to  $2.2\ \mu F$
    - Change note of  $C_{OUT}$  from ' $1.35\ \mu F$ ' to ' $3\ \mu F$ '
    - Change min value of  $C_{OUT}$  from  $0.65\ \mu F$  to  $1.45\ \mu F$
    - Change min value of  $dV_{out}/dI_{out}$  from  $-100\ mV$  to  $-180\ mV$
    - Change max value of  $dV_{out}/dI_{out}$  from  $100\ mV$  to  $180\ mV$
    - Change note of  $I_{MAX}$  from ' $100\ mA$ ' to ' $60\ mA$ '
    - Change note of  $dV_{out}/dV_{in}$  from ' $dV_{in}/dT=50V/ms$ ;  $dV=5$  to  $3.6V$ ' to ' $dV_{in}/dT=50V/ms$ ;  $dV=5$  to  $3.6V$ ;  $I_{MAX}=60mA$ '
    - Change note of  $dV_{out}/dV_{in}$  from ' $dV_{in}/dT=50V/ms$ ;  $dV=3.6$  to  $5V$ ' to ' $dV_{in}/dT=50V/ms$ ;  $dV=3.6$  to  $5V$ ;  $I_{MAX}=60mA$ '
  - PMS/Supply Monitors
    - Change max value of  $V_{LVDRST5}$  from  $2.7\ V$  to  $2.75\ V$
    - Change note of  $V_{LVDRST5}$  from ' $2.67\ V$ ' to ' $2.72\ V$ '
    - Change note of  $V_{RST33}$  from 'by reset release before EVR trimming on supply ramp-up.' to 'by last cold PORST release on supply ramp-up including voltage hysteresis.'
    - Change note of  $V_{RSTC}$  from 'by reset release before trimming on supply ramp-up including 2 LSB voltage Hysteresis' to 'by last cold PORST release on supply ramp-up including voltage hysteresis.'
    - Change note of  $V_{RST5}$  from 'by reset release before trimming on supply ramp-up including 2 LSB voltage hysteresis' to 'by last cold PORST release on supply ramp-up including voltage hysteresis.'
  - PMS/Supply Ramp
    - Change description of  $SR\_V\_EXT$  from 'External  $V_{EXT}$  &  $V_{EVRSB}$  supply ramp' to 'External  $V_{EXT}$  &  $V_{EVRSB}$  supply ramp-up and ramp-down slope'
    - Change description of  $SR\_V\_DDP3$  from 'External  $V_{DDP3}$  supply ramp' to 'External  $V_{DDP3}$  supply ramp-up and ramp-down slope'

- Change description of  $SR\_V\_DD$  from 'External  $V_{DD}$  supply ramp' to 'External  $V_{DD}$  supply ramp-up and ramp-down slope'
- Change description of  $SR\_V\_DDM$  from 'External  $V_{DDM}$  supply ramp' to 'External  $V_{DDM}$  supply ramp-up and ramp-down slope'
- Changes in table 'EVRC SMPS' of PMS/EVRC SMPS
  - Change name of *EVRC SMPS* from EVR13 SMPS to EVRC SMPS
- Changes in table 'EVRC SMPS External components' of PMS/EVRC SMPS
  - Change name of *EVRC SMPS External components* from EVR13 SMPS External components to EVRC SMPS External components
- Changes in section JTAG Parameters
  - Update figure Test Clock Timing (TCK)
- Changes in section DAP Parameters
  - Combine figures Test Clock Timing (DAP0), DAP Timing Host to Device, and DAP Timing Device to Host (DAP1 and DAP2 pins) into single figure DAP Timing
  - Add  $t_{14}$  for condition F=40MHz
  - Add  $t_{15}$  for condition F=40MHz
  - Add  $t_{16}$  for condition F=40MHz
- Changes in table 'Master Mode strong sharp (ss) output pads' of ASCLIN
  - Change min value of  $t_{51}$  from -3 ns to -3.5 ns
  - Change note of  $t_{51}$  from '3 ns' to '3.5 ns'
  - Change max value of  $t_{510}$  from 3 ns to 3.5 ns
- Changes in table 'Master Mode Timing, LVDS output pads for data and clock' of QSPI
  - Change max value of  $t_{51}$  from 3 ns to 4 ns
  - Change min value of  $t_{52}$  from 17 ns to 18 ns
- Changes in table 'Strong sharp (ss) driver for clock/data valid for 5V' of MSC
  - Change note of  $t_{45}$  from '-3 ns' to '-4 ns'
  - Change min value of  $t_{44}$  from -3 ns to -4 ns
- Changes in table 'ETH RGMII Signal Timing Parameters valid for 3.3V' of Ethernet
  - Add parameter  $t_{21}$
- Changes in table 'ETH RMII Signal Timing Parameters valid for 3.3V' of Ethernet
  - Change description of  $t_{16}$  from 'ETHTXEN, ETHTXD[1:0], ETHRXD[1:0], ETHCRSDV, ETHRXER; setup time' to 'ETHTXEN, ETHTXD[1:0], ETHRXD[1:0], ETHCRSDV; setup time'
  - Change description of  $t_{17}$  from 'ETHTXEN, ETHTXD[1:0], ETHRXD[1:0], ETHCRSDV, ETHRXER; hold time' to 'ETHTXEN, ETHTXD[1:0], ETHRXD[1:0], ETHCRSDV; hold time'
- Changes in table 'HSCT - Rx/Tx setup timing' of LVDS Pads
  - Change max value of  $t_{tx}$  from 250 ns to 280 ns
- Removed section CIF
- SDMMC
  - Change note of  $t_5$  from ' $C_L \leq 30\text{pF}$ ' to ' $C_L \leq 30\text{pF}, V_{EXT} = 3.3\text{V}$ '
  - Change min value of  $t_5$  from -3 ns to 3 ns
  - Change description of  $t_5$  from 'Data output delay time' to 'Data output valid time before rising clock edge'
  - Change note of  $t_6$  from ' $C_L \leq 30\text{pF}$ ' to ' $C_L \leq 30\text{pF}, V_{EXT} = 3.3\text{V}$ '
  - Change note of  $t_6$  from 'max' to 'min'

- Change note of  $t_6$  from '13,7 ns' to '3 ns'
- Change description of  $t_6$  from 'Data input delay time' to 'Data output valid time after rising clock edge'
- Change description of  $t_8$  from 'Output hold time' to 'Data Input delay time'
- Add parameter  $t_9$
- Change note of  $t_1$  from 'push-pull,  $C_L \leq 30\text{pF}$ , tolerance  $\pm 100\text{kHz}$ ' to 'push-pull,  $C_L \leq 30\text{pF}$ ,  $V_{\text{EXT}} = 3.3\text{V}$ '
- Change predicate of  $t_1$  from max to min
- Change note of  $t_2$  from 'open-drain,  $C_L \leq 30\text{pF}$ , tolerance  $\pm 20\text{kHz}$ ' to 'open-drain,  $C_L \leq 30\text{pF}$ ,  $V_{\text{EXT}} = 3.3\text{V}$ '
- Change note of  $t_3$  from ' $C_L \leq 30\text{pF}$ ' to ' $C_L \leq 30\text{pF}$ ,  $V_{\text{EXT}} = 3.3\text{V}$ '
- Change note of  $t_4$  from ' $C_L \leq 30\text{pF}$ ' to ' $C_L \leq 30\text{pF}$ ,  $V_{\text{EXT}} = 3.3\text{V}$ '
- Change note of  $t_7$  from ' $C_L \leq 30\text{pF}$ ' to ' $C_L \leq 30\text{pF}$ ,  $V_{\text{EXT}} = 3.3\text{V}$ , TTL levels'
- Flash
  - Change note of  $t_{\text{ER\_Dev}}$  from '' to 'Valid for less than 1000 cycles, w/o UCB. Derived value for documentation purpose.'
  - Change note of  $t_{\text{ER\_Dev}}$  from 'Derived value for documentation purpose' to 'Valid for less than 1000 cycles, w/o UCB. Derived value for documentation purpose.'
- ED Current Consumption
  - Change max value of  $I_{\text{DDSB}}$  from 8 mA to 15 mA
  - Change note of  $I_{\text{DDSB}}$  from '27 mA' to '34 mA'
- Package Parameters
  - Update table Thermal Characteristics of the Package
  - Change package type from PG-LFBGA-516-9 to PG-LFBGA-516-10
  - Change package type from PG-LFBGA-292-9 to PG-LFBGA-292-10

#### 4.2 从0.6版本到0.7版本的变更

- Added preamble to AGBT stating that AGBT is lab-only interface without full test coverage
- Changes in table "Absolute Maximum Ratings"
  - Change value of Parameter "VDDM"
  - Change value of Parameter "VIN"
  - Change value of Parameter "VIN"
- Changes in table "Master Mode strong sharp (ss) output pads"
  - Change value of Parameter "t51"
  - Change value of Parameter "t510"
- Changes in table "Current Consumption"
  - Change condition of Parameter "IDDPORST"
  - Change value of Parameter "IDDRAIL"
  - Change value of Parameter "IEVRSB"
  - Change value of Parameter "IEXTFLEX"
  - Change value of Parameter "ISLEEP"
  - Change condition of Parameter "ISTANDBY"
  - Change value of Parameter "ISTANDBY"
  - Change of Parameter "IDDRAIL" description

- Footnote added to Parameter "IDDP3RAIL"
- Footnote added to Parameter "IEXTFLEX"
- Footnote added to Parameter "IEVRSB"
- Footnote added to Parameter "ISLEEP"
- Changes in table "Module Core Current Consumption"
  - Change condition of Parameter "IDDLBIST"
  - Change value of Parameter "IDDLBIST"
  - Footnote added to Parameter "IDDLBIST"
  - Change condition of Parameter "IDDMBIST"
  - Change value of Parameter "IDDMBIST"
  - Change condition of Parameter "IDDSPU1"
  - Change value of Parameter "IDDSPU1"
  - Change value of Parameter "IDDSPULJ1"
  - Parameter "IDDCIF" deleted
  - New Parameter "IDDSPU2" added
  - New Parameter "IDDSPULJ1" added
  - New Parameter "IDDSPULJ2" added
- Changes in table "Module Current Consumption"
  - Change value of Parameter "IDDP3PROG"
  - Change value of Parameter "ISCRIDLE"
  - Change condition of Parameter "ISCRSB"
  - Change value of Parameter "ISCRSB"
  - Footnote added to Parameter "IEXTLVDS"
  - New Parameter "IDDP3ERASE" added
- Changes in table "DSADC 5V"
  - Change preamble
  - Change value of Parameter "EDGAIN"
  - Change value of Parameter "EDOFF"
  - Change value of Parameter "IREF"
  - Change value of Parameter "IRMS"
  - Change of Parameter "IREF" description
  - Footnote added to Parameter "IRMS"
  - Footnote added to Parameter "EDGAIN"
  - Footnote added to Parameter "EDOFF"
  - Footnote added to Parameter "SNR"
  - Footnote added to Parameter "SFDR"
- Changes in table "DTS PMS"
  - Change value of Parameter "tM"
- Changes in table "ED Current Consumption"
  - Change value of Parameter "IEXTAGBT"
  - Parameter "VDDAGBT" deleted
  - Footnote changed of Parameter "VDDEEC"

**修订记录 从0.6版本到0.7版本的变更**

- Changes in table "Transmit Parameters"
  - Change of Parameter "tdCCxEN10" description
- Changes in table "EVR33 LDO"
  - Change value of Parameter "IMAX"
  - Change condition of Parameter "VinVoutRatio"
  - Change value of Parameter "VinVoutRatio"
  - Change condition of Parameter "VoutIOutRatio"
  - Change value of Parameter "VoutIOutRatio"
  - Change condition of Parameter "tSTR"
  - New Parameter "dVOUTTC" added
- Changes in table "EVRC SMPS"
  - Change value of Parameter "dVDDDC"
  - Change condition of Parameter "fDCDC"
- Changes in table "Flash"
  - Change condition of Parameter "NE\_EEP10S"
  - Change condition of Parameter "NE\_HSMS"
- Changes in table "HSCT - Rx/Tx setup timing"
  - Change value of Parameter "ttx"
- Changes in table "LVDS - IEEE standard LVDS general purpose link (GPL)"
  - Change condition of Parameter "Rin"
  - Change value of Parameter "VOD"
  - Change value of Parameter "tfall20"
  - Change value of Parameter "trise20"
  - New Parameter "tSET" added
  - Corrected "LVDSH" to "LVDS"
- Changes in table "LVDS clock/data (LVDS pads in LVDS mode) valid for 5V"
  - Change condition of Parameter "t40"
  - Change condition of Parameter "t400"
- Changes in table "Strong sharp (ss) driver for clock/data valid for 5V"
  - Change value of Parameter "t44"
  - Change value of Parameter "t45"
- Changes in table "Operating Conditions"
  - Change condition of Parameter "TA"
- Changes in table "OSC\_XTAL"
  - New Parameter "IHBX" added
  - Change value of Parameter "CXTAL1"
  - Remove Parameter VILBX
- Changes in table "Overload"
  - Change condition of Parameter "IINANA"
  - Parameter "IID" deleted
- Changes in table "Package Parameters"
  - Change value of Parameter "RTH\_JA"

## 修订记录 从0.6版本到0.7版本的变更

- Change value of Parameter "RTH\_JCB"
- Change value of Parameter "RTH\_JCT"
- Changes in table "PLL Peripheral"
  - Change condition of Parameter "DP"
  - Change condition of Parameter "DRMS"
  - Change value of Parameter "DPP"
  - Change Parameter description of "DPP"
  - New Parameter "JABS25" added
  - New Parameter "DPPI" added
- Changes in table "Master Mode Timing, LVDS output pads for data and clock"
  - Change value of Parameter "t51"
  - Change value of Parameter "t52"
- Changes in table "Quality"
  - Change of Parameter "VHBM1" description
  - Footnote added to Parameter "VCCM"
  - Footnote added to Parameter "VHBM"
- Changes in table "Reset"
  - Change condition of Parameter "tB"
  - Change value of Parameter "tB"
  - Change condition of Parameter "tBP"
  - Change value of Parameter "tBS"
  - Change value of Parameter "tBWP"
  - Change condition of Parameter "tLBIST"
  - Footnote added to Parameter "tBP"
  - Change of Parameter "tBP" description
  - Change of Parameter "tLBIST" description
- Changes in table "SDMMC"
  - Change condition of Parameter "t1"
  - Change condition of Parameter "t2"
  - Change condition of Parameter "t3"
  - Change condition of Parameter "t4"
  - Change condition of Parameter "t5"
  - Change value of Parameter "t5"
  - Change condition of Parameter "t6"
  - Change value of Parameter "t6"
  - Change condition of Parameter "t7"
- Changes in table "PORST pad"
  - Change condition of Parameter "IOZ"
  - Change value of Parameter "HYS"
- Changes in table "Class D"
  - Change condition of Parameter "IOZ"
  - Change value of Parameter "IOZ"

- Changes in table "Fast 3.3V GPIO"
  - Footnote changed of parameter "tRF"
  - Change value of Parameter "HYS"
  - Change condition of Parameter "IOZ"
  - Change value of Parameter "IOZ"
  - Change value of Parameter "VIH"
  - Change value of Parameter "VIL"
  - Change condition of Parameter "tRF"
  - Footnote added to Parameter "tRF"
  - Change of Parameter "tSET" description
  - Change condition of Parameter "VILD"
- Changes in table "Fast 5V GPIO"
  - Footnote changed of parameter "tRF"
  - Change value of Parameter "HYS"
  - Change condition of Parameter "IOZ"
  - Change value of Parameter "IOZ"
  - Change value of Parameter "VIH"
  - Change value of Parameter "VIL"
  - Change condition of Parameter "tRF"
  - Footnote added to Parameter "tRF"
  - Change of Parameter "tSET" description
  - Change condition of Parameter "VILD"
- Changes in table "RFast 3.3V pad"
  - Footnote changed of parameter "tRF"
  - Change value of Parameter "VIL"
  - Footnote added to Parameter "tRF"
  - Change of Parameter "tSET" description
  - Change condition of Parameter "tRF"
  - Change value of Parameter "HYS"
  - Change condition of Parameter "IOZ"
  - Change value of Parameter "VIH"
  - Change condition of Parameter "VILD"
- Changes in table "RFast 5V pad"
  - Footnote changed of parameter "tRF"
  - Footnote added to Parameter "tRF"
  - Change of Parameter "tSET" description
  - Change condition of Parameter "tRF"
  - Change value of Parameter "HYS"
  - Change condition of Parameter "IOZ"
  - Change value of Parameter "VIH"
  - Change condition of Parameter "VILD"
- Changes in table "Slow 3.3V GPIO"

- Footnote changed of parameter “tRF”
- Change value of Parameter "HYS"
- Change condition of Parameter "IOZ"
- Change value of Parameter "IOZ"
- Change condition of Parameter "IPUH"
- Change value of Parameter "VIH"
- Change value of Parameter "VIL"
- Footnote added to Parameter "tRF"
- Change of Parameter "tSET" description
- Change condition of Parameter "VILD"
- Changes in table "Slow 5V GPIO"
  - Footnote changed of parameter “tRF”
  - Change value of Parameter "HYS"
  - Change condition of Parameter "IOZ"
  - Change value of Parameter "IOZ"
  - Change condition of Parameter "IPUH"
  - Change value of Parameter "VIH"
  - Change value of Parameter "VIL"
  - Footnote added to Parameter "tRF"
  - Change of Parameter "tSET" description
  - Change condition of Parameter "VILD"
- Changes in table "Class S 5V"
  - Change condition of Parameter "IOZ"
  - Change value of Parameter "HYS"
  - Change value of Parameter "IOZ"
  - Change of Parameter "tSET" description
  - Change value of Parameter "VIH"
  - Change value of Parameter "VIL"
- Changes in table "ADC Reference Pads"
  - Change condition of Parameter "IOZ2"
  - Change value of Parameter "IOZ2"
  - Footnote added to Parameter “IOZ2”
- Changes in table "Supply Monitors"
  - Change condition of Parameter "VDDMON"
  - Change condition of Parameter "VDDP3MON"
  - Change condition of Parameter "VEXTMON"
  - Change condition of Parameter "VRST33"
  - Change condition of Parameter "VRST5"
  - Change condition of Parameter "VRSTC"
  - Change value of Parameter "VRSTC"
  - Change condition of Parameter "tMON"
  - Footnote added to Parameter "VEXTMON"

- Changes in table "Back-up Clock"
  - Footnote change in Parameter "fBACKT"
- Changes in table "DTS Core"
  - New Parameter "dT" added
- Changes in table "VADC 5V"
  - Changed preamble
  - Change condition of Parameter "RPDD"
  - Change condition of Parameter "VDDK"
  - Change condition of Parameter "fADCI"
  - Change condition of Parameter "tS"
  - Change condition of Parameter "tSCAL"
  - New Parameter "VDDK" added
  - New Parameter "dVDDK" added
  - Footnote added to Parameter "QCONV"

### 4.3 从0.7版本到1.0版本的变更

- Changes in table “Platform Feature Overview”
  - Removed feature for “ASIL”
- Changes in chapter “Pin Definition and Functions”
  - Changed naming from “BGA516” to “LFBGA-516”
  - Changed figure for “LFBGA-516”
  - Changed naming from “BGA292” to “LFBGA-292”
  - Changed figure for “LFBGA-292”
  - Changed naming from “BGA292 ADAS feature set” to “LFBGA-292 ADAS feature set”
  - Changed figure for “LFBGA-292 ADAS feature set”
- Changes in chapter 'TC39x Pin Definition and Functions' for package variant LFBGA-516
  - Changes in LFBGA-516 Package Variant 'Port 00 Functions' table; P00.0, P00.1, P00.2, P00.3, P00.4, P00.5, P00.11, P00.12
  - Changes in LFBGA-516 Package Variant 'Port 01 Functions' table; P01.0, P01.2, P01.3, P01.4, P01.8, P01.13
  - Changes in LFBGA-516 Package Variant 'Port 02 Functions' table; P02.0, P02.1, P02.2, P02.3, P02.4, P02.5, P02.8, P02.9, P02.10, P02.13, P02.14
  - Changes in LFBGA-516 Package Variant 'Port 10 Functions' table; P10.2, P10.3, P10.5, P10.6, P10.7, P10.8
  - Changes in LFBGA-516 Package Variant 'Port 11 Functions' table; P11.0, P11.1, P11.4, P11.5, P11.7, P11.8, P11.10, P11.12, P11.13, P11.14
  - Changes in LFBGA-516 Package Variant 'Port 12 Functions' table; P12.0, P12.1
  - Changes in LFBGA-516 Package Variant 'Port 13 Functions' table; P13.0, P13.1, P13.2, P13.4, P13.5, P13.9, P13.12
  - Changes in LFBGA-516 Package Variant 'Port 14 Functions' table; P14.0, P14.1, P14.6, P14.7, P14.8, P14.9, P14.10, P14.13, P14.14, P14.15

**修订记录 从0.7版本到1.0版本的变更**

- Changes in LFBGA-516 Package Variant 'Port 15 Functions' table; P15.0, P15.1, P15.2, P15.3, P15.4, P15.5
- Changes in LFBGA-516 Package Variant 'Port 20 Functions' table; P20.0, P20.3, P20.6, P20.7, P20.8, P20.9, P20.10
- Changes in LFBGA-516 Package Variant 'Port 21 Functions' table; P21.0, P21.1, P21.2, P21.3, P21.4, P21.5
- Changes in LFBGA-516 Package Variant 'Port 22 Functions' table; P22.2, P22.3, P22.4, P22.5, P22.6, P22.7, P22.8, P22.9, P22.10, P22.11
- Changes in LFBGA-516 Package Variant 'Port 23 Functions' table; P23.0, P23.1, P23.2, P23.3, P23.5, P23.6, P23.7
- Changes in LFBGA-516 Package Variant 'Port 32 Functions' table; P32.2, P32.3, P32.4, P32.5, P32.6, P32.7
- Changes in LFBGA-516 Package Variant 'Port 33 Functions' table; P33.0, P33.1, P33.2, P33.3, P33.4, P33.5, P33.7, P33.8, P33.9, P33.10, P33.12, P33.13
- Changes in LFBGA-516 Package Variant 'Port 34 Functions' table; P34.1, P34.2
- Changes in LFBGA-516 Package Variant 'Analog Inputs' table; Ball AD10, AB10
- Changes in chapter 'TC39x Pin Definition and Functions' for package variant LFBGA-292
  - Changes in LFBGA-292 Package Variant 'Port 00 Functions' table; P00.0, P00.1, P00.2, P00.3, P00.4, P00.5, P00.11, P00.12
  - Changes in LFBGA-292 Package Variant 'Port 01 Functions' table; P01.3, P01.4
  - Changes in LFBGA-292 Package Variant 'Port 02 Functions' table; P02.0, P02.1, P02.2, P02.3, P02.4, P02.5, P02.8, P02.9, P02.10
  - Changes in LFBGA-292 Package Variant 'Port 10 Functions' table; P10.2, P10.3, P10.5, P10.6, P10.7, P10.8
  - Changes in LFBGA-292 Package Variant 'Port 11 Functions' table; P11.0, P11.1, P11.4, P11.5, P11.7, P11.8, P11.10, P11.12, P11.13, P11.14
  - Changes in LFBGA-292 Package Variant 'Port 12 Functions' table; P12.0, P12.1
  - Changes in LFBGA-292 Package Variant 'Port 13 Functions' table; P13.0, P13.1, P13.2
  - Changes in LFBGA-292 Package Variant 'Port 14 Functions' table; P14.0, P14.1, P14.6, P14.7, P14.8, P14.9, P14.10
  - Changes in LFBGA-292 Package Variant 'Port 15 Functions' table; P15.0, P15.1, P15.2, P15.3, P15.4, P15.5
  - Changes in LFBGA-292 Package Variant 'Port 20 Functions' table; P20.0, P20.3, P20.6, P20.7, P20.8, P20.9, P20.10
  - Changes in LFBGA-292 Package Variant 'Port 21 Functions' table; P21.0, P21.1, P21.2, P21.3, P21.4, P21.5
  - Changes in LFBGA-292 Package Variant 'Port 22 Functions' table; P22.2, P22.3, P22.4, P22.5, P22.6, P22.7, P22.8, P22.9, P22.10, P22.11
  - Changes in LFBGA-292 Package Variant 'Port 23 Functions' table; P23.0, P23.1, P23.2, P23.3, P23.5, P23.6, P23.7
  - Changes in LFBGA-292 Package Variant 'Port 32 Functions' table; P32.2, P32.3, P32.4, P32.5, P32.6, P32.7
  - Changes in LFBGA-292 Package Variant 'Port 33 Functions' table; P33.0, P33.1, P33.2, P33.3, P33.4, P33.5, P33.7, P33.8, P33.9, P33.10, P33.12, P33.13
  - Changes in LFBGA-292 Package Variant 'Port 34 Functions' table; P34.1, P34.2

**修订记录 从0.7版本到1.0版本的变更**

- Changes in LFBGA-292 Package Variant 'Analog Inputs' table; Ball W5, U5
- Changes in chapter 'TC39x Pin Definition and Functions' for package variant LFBGA-292 ADAS
  - Changes in LFBGA-292 ADAS Package Variant 'Port 00 Functions' table; P00.0, P00.1, P00.2, P00.3, P00.4, P00.5, P00.11, P00.12
  - Changes in LFBGA-292 ADAS Package Variant 'Port 02 Functions' table; P02.0, P02.1, P02.2, P02.3, P02.4, P02.5, P02.8
  - Changes in LFBGA-292 ADAS Package Variant 'Port 10 Functions' table; P10.2, P10.3, P10.5, P10.6, P10.7, P10.8
  - Changes in LFBGA-292 ADAS Package Variant 'Port 11 Functions' table; P11.0, P11.1, P11.4, P11.5, P11.7, P11.8, P11.10, P11.12, P11.13, P11.14
  - Changes in LFBGA-292 ADAS Package Variant 'Port 12 Functions' table; P12.0, P12.1
  - Changes in LFBGA-292 ADAS Package Variant 'Port 14 Functions' table; P14.0, P14.1, P14.6, P14.7, P14.8, P14.9, P14.10
  - Changes in LFBGA-292 ADAS Package Variant 'Port 15 Functions' table; P15.0, P15.1, P15.2, P15.3, P15.4, P15.5
  - Changes in LFBGA-292 ADAS Package Variant 'Port 20 Functions' table; P20.0, P20.3, P20.6, P20.7, P20.8, P20.9, P20.10
  - Changes in LFBGA-292 ADAS Package Variant 'Port 21 Functions' table; P21.0, P21.1, P21.2, P21.3, P21.4, P21.5
  - Changes in LFBGA-292 ADAS Package Variant 'Port 22 Functions' table; P22.2, P22.3, P22.4, P22.5, P22.6, P22.7, P22.8, P22.9, P22.10, P22.11
  - Changes in LFBGA-292 ADAS Package Variant 'Port 23 Functions' table; P23.0, P23.1, P23.2, P23.3, P23.5, P23.6, P23.7
  - Changes in LFBGA-292 ADAS Package Variant 'Port 32 Functions' table; P32.2, P32.3, P32.4, P32.5, P32.6, P32.7
  - Changes in LFBGA-292 ADAS Package Variant 'Port 33 Functions' table; P33.0, P33.1, P33.2, P33.3, P33.4, P33.5, P33.7, P33.8, P33.9, P33.10, P33.12, P33.13
  - Changes in LFBGA-292 ADAS Package Variant 'Port 34 Functions' table; P34.1, P34.2
  - Changes in LFBGA-292 Package Variant 'Analog Inputs' table; Ball W5, U5
- Changes in chapter 'Pin Position Definition'
  - Changes in table “Pad List”, Number 206
- Changed description in chapter 'Legend'
  - Column “Buffer Type”: PU2
  - add link to Spirit file
- Changes in chapter “Electrical Specification”
- Changed wording in sub-chapter “Parameter Interpretation”
- Changes in table 'Absolute Maximum Ratings'
  - Added footnote 2) for  $V_{DD}$
  - Changed order of footnotes
- Changes in table "Overload Parameters"
  - Changed table numbers in description
  - Changed parameter condition of "KOVAN"
  - Changed parameter condition of "KOVAP"
  - Added footnote 2) for “KOVAN” and "KOVAP"

- Changes in table "Operating Conditions"
  - Added footnote 1) for "VDD"
  - Changed order of footnotes
- Changes in table 'PORST Pad'
  - Added values and notes for parameter  $V_{IH}$
  - Added values and notes for parameter  $V_{IL}$
  - Added footnote 2) for  $I_{PDL}$
- Changes in table 'Fast 5V GPIO' of Standard Pads
  - Removed values and conditions of parameter  $I_{OZ}$
  - Changed footnote 2) for  $t_{RF}$
  - Added footnote 4) for  $I_{PUH}$
  - Added footnote 5) for  $I_{PDL}$
- Changes in table 'Fast 3.3V GPIO' of Standard Pads
  - Combined equal values of  $I_{OZ}$  in single line
  - Changed footnote 2) for  $t_{RF}$
  - Added footnote 4) for  $I_{PUH}$
  - Added footnote 5) for  $I_{PDL}$
- Changes in table 'Slow 5V GPIO' of Standard Pads
  - Removed values and conditions of parameter  $I_{OZ}$
  - Combined equal values of  $I_{OZ}$  in single line
  - Changed footnote 2) for  $t_{RF}$
  - Added footnote 4) for  $I_{PUH}$
  - Added footnote 5) for  $I_{PDL}$
- Changes in table 'Slow 3.3V GPIO' of Standard Pads
  - Removed values and conditions of parameter  $I_{OZ}$
  - Combined equal values of  $I_{OZ}$  in single line
  - Changed footnote 2) for  $t_{RF}$
  - Added footnote 4) for  $I_{PUH}$
  - Added footnote 5) for  $I_{PDL}$
- Changes in table 'RFast 5V GPIO' of Standard Pads
  - Changed footnote 2) for  $t_{RF}$
  - Added footnote 4) for  $I_{PUH}$
  - Added footnote 5) for  $I_{PDL}$
- Changes in table 'RFast 3.3V pad' of Standard Pads
  - Changed footnote 2) for  $t_{RF}$
  - Added footnote 4) for  $I_{PUH}$
  - Added footnote 5) for  $I_{PDL}$
- Changes in table 'Class S 5V' of Standard Pads
  - Added footnote 2) for  $I_{PUH}$
  - Added footnote 3) for  $I_{PDL}$
- Add table 'Class S 3.3V'
- Changes in table 'ADC Reference Pads' of Standard Pads

- Changed values and notes of parameter  $I_{OZZ}$
- Added parameter and conditions for  $I_{OZZ}$
- Changes in table 'LVDS - IEEE standard LVDS general purpose link (GPL)' of LVDS Pads
  - Added footnote 1) for  $t_{RISE20}$
  - Added footnote 2) for  $t_{FALL20}$
  - Changed order of footnotes
- Changes in table 'VADC 5V'
  - Added values and conditions of parameter  $V_{AREF}$
  - Changed values and conditions of  $V_{AREF}$
  - Added footnote 1) for  $V_{AREF}$
  - Changed order of footnotes
- Changes in table 'DSADC 5V'
  - Changed value of parameter  $V_{AREF}$
  - Added value and condition of parameter  $I_{REF}$
- Changes in table 'OSC\_XTAL'
  - Added parameter for  $DC_{X1}$
  - Added parameter for  $J_{ABSX1}$
  - Added parameter for  $SR_{XTAL1}$
  - Added footnote 3) for  $DC_{X1}$ ,  $J_{ABSX1}$ ,  $SR_{XTAL1}$
- Changes in table 'Back-up Clock'
  - Changed value of parameter  $f_{SB}$
  - Changed footnote 1) for  $f_{BACKT}$
- Changes in table 'DTS PMS'
  - Added parameter conditions for  $T_{NL}$
- Changes in table 'DTS Core'
  - Added parameter conditions for  $T_{NL}$
- Changes in description of chapter 'Power Supply Current'
  - Changed information of real power pattern
  - Added peripherals information
  - Added max power pattern
  - Added ADAS power pattern
- Changes in table 'Current Consumption'
  - Added value and conditions for parameter  $I_{DDRAIL}$
  - Added parameter for parameter  $PD_{SR}$
  - Added conditions for parameter  $PD_{SR}$
  - Changed value for parameter  $I_{SLEEP}$
  - Added parameter for  $I_{DDP3RAIL}$
  - Remove footnote 1) for  $I_{DDP3RAIL}$
  - Changed footnote 1) for  $I_{DDPORST}$ ,  $I_{EXTFLEX}$ ,  $I_{EVRSB}$ ,  $I_{SLEEP}$
  - Mapped footnote 2) to all values of  $I_{DD3RAIL}$
  - Changed footnote 3) for  $I_{EXTFLEX}$
  - Changed order of footnotes

- Added footnote 5) for  $I_{EXTFLEX}$
- Changes in table 'Module Current Consumption'
  - Changed value and condition of parameter  $I_{EXTLVDS}$
  - Added footnote 3) to  $I_{EXTLVDS}$
  - Added footnote 5) to  $I_{DDM}$
  - Changed footnote 8) for  $I_{SCRIDLE}$
- Changes in table 'Module Core Current Consumption'
  - Changed footnote 1) for  $I_{DDHSM}$
  - Changed footnote for  $I_{DDSPU2}$
  - Removed parameter  $I_{DDSPU1}$
  - Removed parameter  $I_{DDSPULJ1}$
- Changes in chapter “Supply Ramp-up and Ramp-down Behavior”
  - Changed Figure and textual description for “Single supply mode (a)”
  - Changed Figure and textual description for “Single supply mode (e)”
  - Changed Figure and textual description for “Single supply mode (d)”
  - Changed Figure and textual description for “Single supply mode (h)”
- Changes in table 'Reset'
  - Added parameter  $t_{WARMRSTSEQ}$
  - Shift typ limit to max limits for mode0 and mode1 and removed typ limits for parameter  $t_{SCR}$
- Changes in table 'EVR33 LDO'
  - Added footnote 7) for  $dV_{OUT} / dI_{OUT}$
- Changes in table 'Supply Monitors'
  - Changed condition of parameter  $V_{RST33}$
  - Changed condition of parameter  $V_{RSTC}$
  - Changed values of parameter  $V_{EXTMON}$
  - Changed footnote 2) for  $V_{EXTPRIUV}$ ,  $V_{DDP3PRIUV}$ ,  $V_{DDPRIUV}$ ,
  - Changed footnote 3) for  $V_{DDP3PRIUV}$ ,  $V_{DDPRIUV}$ ,
  - Added footnote 5) for  $V_{EXTMON}$ ,  $V_{DDP3MON}$ ,  $V_{DDMON}$
- Changes in table 'EVRC SMPS External Components'
  - Add values of parameter ' $L_{DC}$ ' for condition 0.8MHz
- Changed chapter naming from 'Phase Locked Loop (PLL)' to 'System Phase Locked Loop (SYS\_PLL)'
- Changes in table 'PLL System'
  - Removed parameter values of ' $f_{MV}$ '
- Changes in table 'QSPI Master Mode Timing'
  - Added footnote 1) for all parameters
- Changes in table 'MSC LVDS clock/data'
  - Added footnote 3) for all parameters
- Changes in chapter 'HSCT Parameters'
  - Added table for “HSCT”
- Add chapter FSP Parameter
- Changes in table 'Flash'
  - Changed description of parameter of  $N_{DFD}$

## 修订记录 从1.0版本到1.1版本的变更

- Added parameter  $N_{DFDC}$
- Added parameter  $N_{UCBD}$
- Added parameter  $t_{VER\_PAGE\_DC}$
- Added parameter  $t_{VER\_PAGE\_DS}$
- Removed parameter  $t_{VER\_PAGE\_D}$
- Changed parameter note  $t_{RTU}$
- Removed chapter 'Parameters Specific to the Emulation Part Only'
- Changes in table 'Package Parameters'
  - Changed parameter value of RTH\_JCB
  - Changed parameter values of RTH\_JCT

#### 4.4 从1.0版本到1.1版本的变更

- Changes in table 'Platform Feature Overview' - changed package types.
- Changes in chapter 'Pin Position Definition' added definition of 'neighbor pads'
- Changes in chapter 'Legend' - changed explanation for PD2
- Changes in table 'Absolute Maximum Ratings'
  - Added footnote 5
  - Changed description of parameter  $I_{IN}$
- Changes in table 'Slow 5V GPIO' - Parameter  $I_{OZ}$ - removed note 'no analog input'
- Changes in table 'Slow 3.3V GPIO' - Parameter  $I_{OZ}$ - removed note 'no analog input'
- Changes in chapter 'High Performance LVDS Pads'- added two notes
- Changes in table 'LVDS - IEEE Standard LVDS general purpose link (GPL)' of LVDS pads
  - Changed value for parameter  $V_I$
  - Changed condition for parameter  $V_{idth}$
  - Added values for parameter  $V_{idth}$
  - Changed condition for parameter  $R_{in}$
- Changes in table 'VADC 5V' - Parameter  $V_{AIN}$  - added note to parameter
- Changes in table 'DSADC 5V' - added value for parameter  $I_{RMS}$
- Changes in table 'DSADC 5V' - Parameter  $ED_{Gain}$  - added footnote 4
- Changes in table 'OSC\_XTAL' - Parameter  $t_{OSCS}$  - changed footnote 1
- Changes in chapter 'Power Supply Current' - Section 'ADAS power pattern' - added SPU frequency
- Changes in table 'Current Consumption' - Parameter  $V_{EVRSB}$  - changed footnote 8
- Changes in table 'Module Core Current Consumption' - added Parameter  $I_{DDSPU1}$  and  $I_{IDDSPULJ1}$
- Changes in table 'Module Core Current Consumption' - Parameter  $I_{DDSPU2}$  and  $I_{IDDSPULJ2}$  changed footnote 2
- Changes in table 'Supply ramp' - added comment for power cycles
- Changed in chapter 'ETH RGMII Parameters' - added figures ETH RGMII TX Signal Timing (Delay on Destination ((DoD))
- Changed in chapter 'ETH RGMII Parameters' - added figures ETH RGMII RX Signal Timing (Delay on Source ((DoS))
- Changes in table 'Quality Parmeters' - Parameter  $V_{HBM1}$  - changed max. limit
- Changes in chapter 'Package Outline' - changed package types.

## 4.5 从1.1版本到1.2版本的变更

- Changes in chapter “Revision History”
  - Chronology completed
- Changes in chapter “Summary of Features”
  - Changed wording for “DFLASH”
  - Added description for “AEC-Q100”
  - Added description for “ISO 26262 Safety Element”
  - Added description for Data Flash in table “Platform Feature Overview”
  - Changed figure for GTM/CDTM modules in table “Platform Feature Overview”
  - Changed figures for FlexRay Channels in table “Platform Feature Overview”
  - Changed wording for HSPDM in table “Platform Feature Overview”
  - Added footnote 2) for AGBT feature in table “Platform Feature Overview”
- Changes in chapter “Pin Definition and Functions”
  - Changed EDSADC function description for Port 00 in “LFBGA-516 Package Variant” tables
  - Changed CCU\_EXTCLK function description for Port 00 in “LFBGA-516 Package Variant” tables
  - Changed EDSADC function description for Port 01 in “LFBGA-516 Package Variant” tables
  - Changed EDSADC function description for Port 02 in “LFBGA-516 Package Variant” tables
  - Deleted PMS\_PMS\_TESTGND\_PAD description for Port 02 in “LFBGA-516 Package Variant” tables
  - Changed wording for QSPI function at Port 10 in “LFBGA-516 Package Variant” tables
  - Deleted SCU function at Port 10 in “LFBGA-516 Package Variant” tables
  - Added PMS function at Port 10 in “LFBGA-516 Package Variant” tables
  - Changed Buffer Type description for P11.5, P11.7, P11.8, P11.9, P11.10, P11.11, P11.12 at Port 11 in “LFBGA-516 Package Variant” tables
  - Changed function description for GETH at Port 11 in “LFBGA-516 Package Variant” tables
  - Changed function description for CCU at Port 11 in “LFBGA-516 Package Variant” tables
  - Changed function description for I2C at Port 11 in “LFBGA-516 Package Variant” tables
  - Changed function description for GTM at Port 11 in “LFBGA-516 Package Variant” tables
  - Changed function description for GETH at Port 12 in “LFBGA-516 Package Variant” tables
  - Changed function description for I2C at Port 13 in “LFBGA-516 Package Variant” tables
  - Deleted function description for SCU at Port 14 in “LFBGA-516 Package Variant” tables
  - Added function description for PMS at Port 14 in “LFBGA-516 Package Variant” tables
  - Changed wording for QSPI function at Port 14 in “LFBGA-516 Package Variant” tables
  - Changed function description for I2C at Port 15 in “LFBGA-516 Package Variant” tables
  - Changed wording for QSPI function at Port 15 in “LFBGA-516 Package Variant” tables
  - Changed function description for CCU at Port 20 in “LFBGA-516 Package Variant” tables
  - Changed function description for GTM at Port 20 in “LFBGA-516 Package Variant” tables
  - Changed wording for QSPI function at Port 20 in “LFBGA-516 Package Variant” tables
  - Changed function description for DMU at Port 21 in “LFBGA-516 Package Variant” tables
  - Changed wording for QSPI function at Port 22 in “LFBGA-516 Package Variant” tables

**修订记录 从1.1版本到1.2版本的变更**

- Changed function description for HSPDM at Port 22 in “LFBGA-516 Package Variant”
- Changed function description for CCU at Port 23 in “LFBGA-516 Package Variant” tables
- Changed function description for GTM at Port 23 in “LFBGA-516 Package Variant” tables
- Changed function description for PMS at Port 32 in “LFBGA-516 Package Variant” tables
- Changed function description for CCU at Port 32 in “LFBGA-516 Package Variant” tables
- Changed function description for EDSADC at Port 33 in “LFBGA-516 Package Variant” tables
- Changed function description for PSI5S at Port 33 in “LFBGA-516 Package Variant” tables
- Changed wording for QSPI function at Port 33 in “LFBGA-516 Package Variant” tables
- Changed wording for QSPI function at Port 34 in “LFBGA-516 Package Variant” tables
- Changed function descriptions for EDSADC in table “Analog Inputs” in “LFBGA-516 Package Variant”
- Added notes to table “System I/O” for “LFBGA-516 Package Variant”
- Changed symbols, buffer types and functions for several balls in “System I/O” table for “LFBGA-516 Package Variant”
- Changed symbols and function descriptions for different balls in “Supply” table for “LFBGA-516 Package Variant”
- 
- Changed function descriptions for EDSADC at Port 00 in “LFBGA-292 Package Variant” tables
- Changed function descriptions for EDSADC at Port 01 in “LFBGA-292 Package Variant” tables
- Changed function descriptions for EDSADC at Port 02 in “LFBGA-292 Package Variant” tables
- Changed function descriptions for PSI5S at Port 02 in “LFBGA-292 Package Variant” tables
- Changed function descriptions for I2C at Port 02 in “LFBGA-292 Package Variant” tables
- Changed wording for QSPI function at Port 02 in “LFBGA-292 Package Variant” tables
- Changed GTM input channel at Port 02 in “LFBGA-292 Package Variant” tables
- Changed wording for QSPI function at Port 10 in “LFBGA-292 Package Variant” tables
- Deleted function description for SCU at Port 10 in “LFBGA-292 Package Variant” tables
- Added function description for PMS at Port 10 in “LFBGA-292 Package Variant” tables
- Changed Buffer Type description for P11.5, P11.7, P11.8, P11.9, P11.10, P11.11, P11.12 at Port 11 in “LFBGA-292 Package Variant” tables
- Changed function description for CCU at Port 11 in “LFBGA-292 Package Variant” tables
- Changed function descriptions for I2C at Port 11 in “LFBGA-292 Package Variant” tables
- Changed GTM input channel at Port 11 in “LFBGA-292 Package Variant” tables
- Changed function description for GETH at Port 12 in “LFBGA-292 Package Variant” tables
- Changed function description for I2C at Port 13 in “LFBGA-292 Package Variant” tables
- Deleted function descriptions for SCU at Port 14 in “LFBGA-292 Package Variant” tables
- Added function descriptions for PMS at Port 14 in “LFBGA-292 Package Variant” tables
- Changed wording for QSPI function at Port 14 in “LFBGA-292 Package Variant” tables
- Changed function description for I2C at Port 15 in “LFBGA-292 Package Variant” tables
- Changed wording for QSPI function at Port 15 in “LFBGA-292 Package Variant” tables
- Changed function description for CCU at Port 20 in “LFBGA-292 Package Variant” tables
- Changed GTM input channel at Port 20 in “LFBGA-292 Package Variant” tables
- Changed wording for QSPI function at Port 20 in “LFBGA-292 Package Variant” tables
- Added function description for DMU at Port 21 in “LFBGA-292 Package Variant” tables

**修订记录 从1.1版本到1.2版本的变更**

- Changed wording for QSPI function at Port 22 in “LFBGA-292 Package Variant” tables
- Changed function description for HSPDM at Port 22 in “LFBGA-292 Package Variant”
- Changed function description for CCU at Port 23 in “LFBGA-292 Package Variant” tables
- Changed GTM input channel at Port 23 in “LFBGA-292 Package Variant” tables
- Changed symbol at Port 32 for ball W17 in “LFBGA-292 Package Variant” tables
- Changed function descriptions for PMS at Port 32 in “LFBGA-292 Package Variant” tables
- Changed function description for CCU at Port 32 in “LFBGA-292 Package Variant” tables
- Changed function descriptions for EDSADC at Port 33 in “LFBGA-292 Package Variant” tables
- Changed GTM input channel at Port 33 in “LFBGA-292 Package Variant” tables
- Changed function descriptions for PSI5S at Port 33 in “LFBGA-292 Package Variant” tables
- Changed wording for QSPI function at Port 33 in “LFBGA-292 Package Variant” tables
- Changed wording for QSPI function at Port 34 in “LFBGA-292 Package Variant” tables
- Added notes to table “System I/O” for “LFBGA-292 Package Variant”
- Changed symbols, buffer types and functions for several balls in “System I/O” table for “LFBGA-292 Package Variant”
- Changed symbols and function descriptions for different balls in “Supply” table for “LFBGA-292 Package Variant”
- 
- Changed function descriptions for EDSADC at Port 00 in “LFBGA-292 ADAS Package Variant” tables
- Changed function descriptions for I2C at Port 02 in “LFBGA-292 ADAS Package Variant” tables
- Changed function descriptions for PSI5S at Port 02 in “LFBGA-292 ADAS Package Variant” tables
- Changed function descriptions for EDSADC at Port 02 in “LFBGA-292 ADAS Package Variant” tables
- Changed function descriptions for QSPI at Port 02 in “LFBGA-292 ADAS Package Variant” tables
- Changed GTM input channel at Port 02 in “LFBGA-292 ADAS Package Variant” tables
- Changed function descriptions for QSPI at Port 10 in “LFBGA-292 ADAS Package Variant” tables
- Deleted function descriptions for SCU at Port 10 in “LFBGA-292 ADAS Package Variant” tables
- Added function descriptions for PMS at Port 10 in “LFBGA-292 ADAS Package Variant” tables
- Changed Buffer Type description for P11.5, P11.7, P11.8, P11.9, P11.10, P11.11, P11.12 at Port 11 in “LFBGA-292 ADAS Package Variant” tables
- Changed function descriptions for QSPI at Port 11 in “LFBGA-292 ADAS Package Variant” tables
- Changed function descriptions for CCU at Port 11 in “LFBGA-292 ADAS Package Variant” tables
- Changed function descriptions for I2C at Port 11 in “LFBGA-292 ADAS Package Variant” tables
- Deleted I2C function (ball D7) at Port 11 in “LFBGA-292 ADAS Package Variant” tables
- Changed function descriptions for GETH at Port 11 in “LFBGA-292 ADAS Package Variant” tables
- Changed GTM input channel at Port 11 in “LFBGA-292 ADAS Package Variant” tables
- Changed function description for GETH at Port 12 in “LFBGA-292 ADAS Package Variant” tables
- Deleted function descriptions for SCU at Port 14 in “LFBGA-292 ADAS Package Variant” tables
- Added function descriptions for PMS at Port 14 in “LFBGA-292 ADAS Package Variant” tables
- Changed function description for QSPI at Port 14 in “LFBGA-292 ADAS Package Variant” tables
- Changed function descriptions for I2C at Port 15 in “LFBGA-292 ADAS Package Variant” tables
- Changed function descriptions for QSPI at Port 15 in “LFBGA-292 ADAS Package Variant” tables
- Changed function description for CCU at Port 20 in “LFBGA-292 ADAS Package Variant” tables

## 修订记录 从1.1版本到1.2版本的变更

- Changed GTM input channel at Port 20 in “LFBGA-292 ADAS Package Variant” tables
  - Changed function description for QSPI at Port 20 in “LFBGA-292 ADAS Package Variant” tables
  - Added function description for DMU at Port 21 in “LFBGA-292 ADAS Package Variant” tables
  - Changed function descriptions for QSPI at Port 22 in “LFBGA-292 ADAS Package Variant” tables
  - Changed function descriptions for HSPDM at Port 22 in “LFBGA-292 ADAS Package Variant” tables
  - Changed function description for CCU at Port 23 in “LFBGA-292 ADAS Package Variant” tables
  - Changed GTM input channel at Port 23 in “LFBGA-292 ADAS Package Variant” tables
  - Changed GTM input channel at Port 23 in “LFBGA-292 ADAS Package Variant” tables
  - Changed symbols at balls Y17 and W17 at Port 32 in “LFBGA-292 ADAS Package Variant” tables
  - Changed function description for CCU at Port 32 in “LFBGA-292 ADAS Package Variant” tables
  - Changed function description for PMS at Port 32 in “LFBGA-292 ADAS Package Variant” tables
  - Changed function description for EDSADC at Port 33 in “LFBGA-292 ADAS Package Variant” tables
  - Changed function description for PSI5S at Port 33 in “LFBGA-292 ADAS Package Variant” tables
  - Changed function description for QSPI at Port 33 in “LFBGA-292 ADAS Package Variant” tables
  - Changed function description for QSPI at Port 34 in “LFBGA-292 ADAS Package Variant” tables
  - Changed all function descriptions at Port 50 in “LFBGA-292 ADAS Package Variant” tables
  - Changed all function descriptions at Port 51 in “LFBGA-292 ADAS Package Variant” tables
  - Added notes to table “System I/O” for “LFBGA-292 ADAS Package Variant”
  - Changed symbols, Ctrl., buffer types and functions for several balls in “System I/O” table for “LFBGA-292 ADAS Package Variant”
  - Changed symbols and function descriptions for different balls in “Supply” table for “LFBGA-292 ADAS Package Variant”
  - 
  - Changed sub-chapter title from “Pin Position Definition” to “Sequence of Pads in Pad Frame”
  - Changed comments for pad name VDDP3 (51, 52) in Pad List of “Sequence of Pads in Pad Frame”
  - Changed pad type for pad names P11.5, P11.7, P11.9, P11.8, P11.10, P11.11, P11.12 in Pad List of “Sequence of Pads in Pad Frame”
  - Changed comment for pad 206 in Pad List of “Sequence of Pads in Pad Frame”
  - Changed comment and pad type for pad name AGBTCLKN in Pad List of “Sequence of Pads in Pad Frame”
  - Changed comment and pad type for pad name AGBTCLKP in Pad List of “Sequence of Pads in Pad Frame”
  - Changed comment and pad type for pad name AGBTTXN in Pad List of “Sequence of Pads in Pad Frame”
  - Changed comment and pad type for pad name AGBTTPX in Pad List of “Sequence of Pads in Pad Frame”
  - Changed comment for pad name AGBTERR in Pad List of “Sequence of Pads in Pad Frame”
  - Changed pad names for pads 371, 372, 374, 375 in Pad List of “Sequence of Pads in Pad Frame”
  - Changed comment for pad 381 in Pad List of “Sequence of Pads in Pad Frame”
  - Changed pad names for pads 505, 506, 509, 510 in Pad List of “Sequence of Pads in Pad Frame”
  - Changed pad types and comments for pads 507, 508 in Pad List of “Sequence of Pads in Pad Frame”
  - Changed comment for pad 562 in Pad List of “Sequence of Pads in Pad Frame”
  - Changed comment parts for table Pad List of “Sequence of Pads in Pad Frame”
- Changes in chapter “Electrical Specification”

- Typos corrected in footnotes for sub-chapter “Absolute Maximum Ratings”
- Typo corrected for parameter  $I_{INSA}$  in table “Overload Parameters” of sub-chapter “Pin Reliability in Overload”
- Changed values for parameter GETH frequency in table “Operating Conditions”
- Changed note for parameter  $t_{TX\_ASYM}$  in table “Fast 5V GPIO” of sub-chapter “5V/3.3V switchable Pads”
- Changed note for parameter  $t_{TX\_ASYM}$  in table “Fast 3.3V GPIO” of sub-chapter “5V/3.3V switchable Pads”
- Changed note for parameter  $t_{TX\_ASYM}$  in table “Slow 5V GPIO” of sub-chapter “5V/3.3V switchable Pads”
- Changed note for parameter  $t_{TX\_ASYM}$  in table “Slow 3.3V GPIO” of sub-chapter “5V/3.3V switchable Pads”
- Changed note for parameter  $t_{TX\_ASYM}$  in table “RFast 5V GPIO” of sub-chapter “5V/3.3V switchable Pads”
- Changed note for parameter  $t_{TX\_ASYM}$  in table “RFast 3.3V pad” of sub-chapter “5V/3.3V switchable Pads”
- Changed notes for parameter  $I_{OZZ}$  in table “ADC Reference Pads” of sub-chapter “5V/3.3V switchable Pads”
- Typos corrected in footnotes for table “LVDS – IEEE standard LVDS general purpose link (GPL)” in sub-chapter “High performance LVDS Pads”
- Added footnotes for table “LVDS – IEEE standard LVDS general purpose link (GPL)” in sub-chapter “High performance LVDS Pads”
- Typo corrected for parameter  $dV_{CSD}$  in table “VADC 5V” in sub-chapter “VADC Parameters”
- Changed footnote 7) of table “VADC 5V” in sub-chapter “VADC Parameters”
- Changed figure “Equivalent Circuitry for Analog Inputs” in sub-chapter “VADC Parameters”
- Changed footnotes 3) and 6) for table “VADC 5V” in sub-chapter “VADC Parameters”
- Changed value of parameter  $I_{RMS}$  in table “DSADC 5V” in sub-chapter “DSADC Parameters”
- Changed footnote 4) in sub-chapter “DSADC Parameters”
- Changed spelling in footnote 2) in sub-chapter “MHz Oscillator”
- Changed footnote 2) for table “Current Consumption” in sub-chapter “Power Supply Current”
- Added footnote 9) for table “Current Consumption” in sub-chapter “Power Supply Current”
- Typos corrected in sub-chapter “Calculating the 1.25V Current Consumption”
- Added sentence to sub-chapter “Supply Ramp-up and Ramp-down Behavior”
- Changed/added value for parameter  $t_{PI}$  in table “Reset” for sub-chapter “Reset Timing”
- Changed figure “DAP Timing” in sub-chapter “DAP Parameters”
- Changed values (from Min. to Typ.) for parameter  $t_7$  in table “ETH MII Signal Timing Parameters” for sub-chapter “ETH MII Parameters”
- Changed symbols for parameters  $t_{13}$ ,  $t_{14}$ ,  $t_{15}$  in table “ETH RMII Signal Timing Parameters valid for 3.3V” in sub-chapter “ETH RMII Parameters”
- Changed value (from Min. to Typ.) for parameter  $t_{13}$  in table “ETH RMII Signal Timing Parameters valid for 3.3V” in sub-chapter “ETH RMII Parameters”
- Added footnote 3) for table “ETH RMII Signal Timing Parameters valid for 3.3V” in sub-chapter “ETH RMII Parameters”
- Deleted parameter  $t_{81}$  in table “Skew Calibration Related” in sub-chapter “Radar Interface Timing”
- Changed values for parameters  $t_{82}$  and  $t_{83}$  in table “Skew Calibration Related” in sub-chapter “Radar Interface Timing”
- Deleted notes for parameters  $t_{82}$  and  $t_{83}$  in table “Skew Calibration Related” in sub-chapter “Radar Interface Timing”
- Added footnotes to Max. Value of parameter  $t_{ER\_Dev}$  in table “Flash” in sub-chapter “Flash Target Parameters”

- Changed figure “Package Outlines LFBGA-292” in sub-chapter “Package Outline”



## 免责声明

请注意，本文件的原文使用英文撰写，为方便客户浏览英飞凌提供了中文译文。该中文译文仅供参考，并不可作为任何论点之依据。

由于翻译过程中可能使用了自动化程序，以及语言翻译和转换过程中的差异，最后的中文译文与最新的英文版本原文含义可能存在不尽相同之处。

因此，我们同时提供该中文译文版本的最新英文原文供您阅读，请参见 <http://www.infineon.com>

英文原文和中文译文版本之间若存有任何歧异，以最新的英文版本为准，并且仅认可英文版本为正式文件。

**您如果使用本文件，即表示您同意并理解上述说明。英飞凌不对因翻译过程中可能存在的任何不完整或不准确信息而产生的任何直接或间接损失或损害负责。英飞凌不承担中文译文版本的完整性和准确性责任。如果您不同意上述说明，请不要使用本文件。**

## Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

## 重要通知

版本 2026-01-26

Infineon Technologies AG 出版，  
德国 Neubiberg 85579

版权 © 2025 Infineon Technologies AG  
及其关联公司。  
保留所有权利。

Do you have a question about this  
document?

Email:

[erratum@infineon.com](mailto:erratum@infineon.com)

Infineon Technologies AG 及其关联公司（以下简称“英飞凌”）销售或提供和交付的产品（可能也包括样品，且可能由硬件或软件或两者组成）（以下简称“产品”），应遵守客户与英飞凌签订的框架供应合同或其他书面协议的条款和条件，如无上合同或其他书面协议，则应遵守适用的英飞凌销售条件。只有在英飞凌明确书面同意的情况下，客户的一般条款和条件或对适用的英飞凌销售条件的偏离才对英飞凌具有约束力。

为避免疑义，英飞凌不承担不侵犯第三方权利的所有保证和默示保证，例如对特定用途/目的的适用性或适销性的保证。

英飞凌对与样品、应用或客户对任何产品的具体使用有关的任何信息或本文件中给出的任何示例或典型值概不负责。

本文件中包含的数据仅供具有技术资格和技能的客户代表使用。客户有责任评估产品对预期应用和客户特定用途的适用性，并在预期应用和客户特定用途中验证本文件中包含的所有相关技术数据。客户有责任正确设计、编程和测试预期应用的功能性和安全性，并遵守与其使用相关的法律要求。

除非英飞凌另行明确批准，否则产品不得用于任何因产品故障或使用产品的任何后果可合理预期会导致人身伤害的应用。但是，上述规定并不妨碍客户在英飞凌明确设计和销售的使用领域中使用任何产品，但是客户对应用负有全部责任。

英飞凌明确保留根据适用法律，如《德国版权法》（UrhG）第 44b 条，将其内容用于商业资料和数据探勘（TDM）的权利。

如果产品包含安全功能：

由于任何计算设备都不可能绝对安全，尽管产品采取了安全措施，但英飞凌不保证产品不会被入侵、数据不会被盗或遗失，或不会发生其他漏洞（以下简称“安全漏洞”），英飞凌对任何安全漏洞不承担任何责任。

如果本文件包含或引用软件：

根据美国、德国和世界其他国家的知识产权法律和条约，该软件归英飞凌所有。英飞凌保留所有权利。因此，您只能按照软件附带的软件授权协议的规定使用本软件。

如果没有适用的软件授权协议，英飞凌特此授予您个人的、非排他性的、不可转让的软件知识产权授权（无权转授权）：(a) 对于以源代码形式提供的软件，仅在贵组织内部修改和复制该软件用于英飞凌硬件产品；及 (b) 对于以二进制代码 (binary code) 形式对外向终端用户分发该软件，仅得用于英飞凌硬件产品。禁止对本软件进行任何其他使用、复制、修改、翻译或编译。有关产品、技术、交货条款和条件以及价格的详细信息，请联系离您最近的英飞凌办公室或访问 <https://www.infineon.com>。

[www.infineon.com](http://www.infineon.com)

Published by Infineon Technologies AG

OPEN MARKET VERSION