

# AURIX™ TC38x variants

## About this document

### Scope and purpose

This document is an addendum to the TC38x Product Data Sheet and User's Manual, listing all planned product variants, key parameters such as memory size and optional features.

The User's Manual lists functions implemented on the Silicon, but this document counts functions that are pinning dependent; that is functions are counted that are connected to at least one package pin. As pins are overlaid with several functions the pinning needs to be checked (see Product Data Sheet) to determine the number of usable functions in an application.

### Naming conventions

Prefix:

- SAK:  $T_{\text{ambient}}$  Temperature Range from -40°C up to +125°C
- SAL:  $T_{\text{ambient}}$  Temperature Range from -40°C up to +150°C (packaged device)

Feature Package:

- P: Standard feature
- E: Emulation device with all features of the emulated standard type, additionally full MCDS, overlay functionality for calibration, AGBT as trace interface for development (depending on the package)
- C,V,Z,M: Customer Specific
- A: ADAS ext. Memory
- T: ADAS + emulation
- X: Extended Feature device. These products contain the extended memory (EMEM) of the ADAS subsystem. The ADAS peripherals SPU and RIF are not available
- F: Extended Flash
- G: Additional Connectivity
- H: ADAS Standard feature
- N: Standard feature with AMU

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**1 TC38x AE step variants**

**1 TC38x AE step variants**

The following tables list the TC38x AE step variants.

**1.1 TC38x AE step (part 1)**

A table listing the TC38x AE step variants.

**Table 1 TC38x\_AE step (part 1)**

SAK-TC389QP-160 F300S	SAK-TC387QP-160 F300S	SAK-TC387TP-128 F300S	SAK-TC387QN-160 F300S	SAK-TC389QN-160 F300S	SAL-TC389QP-160 F300S	SAL-TC387QP-160 F300S
<b>Step</b>						
AE	AE	AE	AE	AE	AE	AE
<b>Production Status</b>						
Standard	Standard	Customer Specific	Customer Specific	Customer Specific	Standard	Standard
<b>Package Type</b>						
PG-FBGA-516	PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292	PG-FBGA-516	PG-FBGA-516	PG-LFBGA-292
<b>Pinout</b>						
LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm
<b>Reference Silicon</b>						
TC38x	TC38x	TC38x	TC38x	TC38x	TC38x	TC38x
<b>Temperature Range (Ambient)</b>						
SAK	SAK	SAK	SAK	SAK	SAL	SAL
<b>Chip ID</b>						
<i>Attention: The value of SCU_CHIPID in the UCODE field contains the default value 0 not the µCode version.</i>						
0x8C008984	0x8C008784	0xCB008784	0xAC008784	0xAC008984	0x8C008984	0x8C008784
<b>Cores / Checker Cores</b>						
4/2	4/2	3/2	4/2	4/2	4/2	4/2
<b>Max. Freq. (MHz)</b>						
300	300	300	300	300	300	300
<b>Program Flash (MB)</b>						
10	10	8	10	10	10	10
<b>Data Flash0 (single-ended) (KB)</b>						
512	512	512	512	512	512	512
<b>Total SRAM (without EMEM and Cache) (KB)</b>						
1376	1376	1152	1376	1376	1376	1376
<b>EMEM Size (KB)</b>						
<b>(table continues...)</b>						

1 TC38x AE step variants

Table 1 (continued) TC38x\_AE step (part 1)

SAK-TC389QP-160 F300S	SAK-TC387QP-160 F300S	SAK-TC387TP-128 F300S	SAK-TC387QN-160 F300S	SAK-TC389QN-160 F300S	SAL-TC389QP-160 F300S	SAL-TC387QP-160 F300S
0	0	0	0	0	0	0
<b>DSPR (KB)</b>						
240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other
<b>DLMU (KB)</b>						
64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU
<b>PSPR (KB)</b>						
64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU
<b>LMU (KB)</b>						
128	128	128	128	128	128	128
<b>DAM (KB)</b>						
64	64	64	64	64	64	64
<b>AMU<sup>1)</sup></b>						
No	No	No	Yes	Yes	No	No
<b>ADC (Primary Groups/Channels)</b>						
8/64	5/40	5/40	5/40	8/64	8/64	5/40
<b>ADC (Secondary Groups/Channels)</b>						
4/60	4/60	4/60	4/60	4/60	4/60	4/60
<b>ADC (Fast Compare Channels)</b>						
4	4	4	4	4	4	4
<b>ADC (EDSADC Channels)</b>						
10	6	6	6	10	10	6
<b>CAN (Modules/Nodes)</b>						
3/3x4	3/3x4	3/3x4	3/3x4	3/3x4	3/3x4	3/3x4
<b>FlexRay (Modules/Channels)</b>						
2/2x2	2/2x2	2/2x2	2/2x2	2/2x2	2/2x2	2/2x2
<b>HSSL Modules</b>						
1	1	1	1	1	1	1
<b>ASCLIN Modules / with ASC &amp; LIN / with 3-wire SPI</b>						
24/24/12	24/24/11	24/24/11	24/24/11	24/24/12	24/24/12	24/24/11

(table continues...)

<sup>1</sup> AMU is abbreviated as ASC Modeling Unit. For Additional details about AMU, Contact an Infineon Representative

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**1 TC38x AE step variants**
**Table 1 (continued) TC38x\_AE step (part 1)**

SAK-TC389QP-160 F300S	SAK-TC387QP-160 F300S	SAK-TC387TP-128 F300S	SAK-TC387QN-160 F300S	SAK-TC389QN-160 F300S	SAL-TC389QP-160 F300S	SAL-TC387QP-160 F300S
<b>QSPI Modules / with LVDS</b>						
5/2	5/2	5/2	5/2	5/2	5/2	5/2
<b>SENT Channels</b>						
25	20	20	20	25	25	20
<b>MSC Modules</b>						
3	2	2	2	3	3	2
<b>PSI5 Channels</b>						
4	4	4	4	4	4	4
<b>PSI5-S Module</b>						
Yes	Yes	Yes	Yes	Yes	Yes	Yes
<b>SDMMC Module</b>						
No	No	No	No	No	No	No
<b>Max. Ethernet Availability: 1Gbit/100Mbit/No</b>						
1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s
<b>MCDS Availability</b>						
miniMCDS	miniMCDS	miniMCDS	miniMCDS	miniMCDS	miniMCDS	miniMCDS
<b>ADAS Cluster Available</b>						
No	No	No	No	No	No	No
<b>CIF</b>						
No	No	No	No	No	No	No
<b>HSM Available</b>						
Yes	Yes	Yes	Yes	Yes	Yes	Yes

## 1 TC38x AE step variants

### 1.2 TC38x AE step (part 2)

A continuation table listing the TC38x AE step variants.

**Table 2** TC38x\_AE step (part 2)

SAL-TC387TP-128F300S	SAK-TC387TP-160F300S	SAL-TC387TP-160F300S	SAK-TC387QM-160F300S	SAK-TC389QP-160F400S	SAK-TC387QP-160F400S
<b>Step</b>					
AE	AE	AE	AE	AE	AE
<b>Production Status</b>					
Customer Specific	Customer Specific	Customer Specific	Customer Specific	Standard	Standard
<b>Package Type</b>					
PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292	PG-FBGA-516	PG-LFBGA-292
<b>Pinout</b>					
LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm
<b>Reference Silicon</b>					
TC38x	TC38x	TC38x	TC38x	TC38x	TC38x
<b>Temperature Range (Ambient)</b>					
SAL	SAK	SAL	SAK	SAK	SAK
<b>Chip ID</b>					
<i>Attention: The value of SCU_CHIPID in the UCODE field contains the default value 0 not the µCode version.</i>					
0xCB008784	0xFC008784	0xFC008784	0xDC008784	0x8C008984	0x8C008784
<b>Cores / Checker Cores</b>					
3/2	3/2	3/2	4/2	4/2	4/2
<b>Max. Freq. (MHz)</b>					
300	300	300	300	400	400
<b>Program Flash (MB)</b>					
8	10	10	10	10	10
<b>Data Flash0 (single-ended) (KB)</b>					
512	512	512	512	512	512
<b>Total SRAM (without EMEM and Cache) (KB)</b>					
1152	960	960	1376	1376	1376
<b>EMEM Size (KB)</b>					
0	0	0	0	0	0

**DSPR (KB)**

(table continues...)

## 1 TC38x AE step variants

Table 2 (continued) TC38x\_AE step (part 2)

SAL-TC387TP-128F30 OS	SAK-TC387TP-160F30 OS	SAL-TC387TP-160F30 OS	SAK-TC387QM-160F30 OS	SAK-TC389QP-160F40 OS	SAK-TC387QP-160F40 OS
240 in CPU0&1; 96 other	160 in CPU0; 128 in CPU1; 96 other	160 in CPU0; 128 in CPU1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other
<b>DLMU (KB)</b>					
64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU
<b>PSPR (KB)</b>					
64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU
<b>LMU (KB)</b>					
128	128	128	128	128	128
<b>DAM (KB)</b>					
64	64	64	64	64	64
<b>AMU<sup>2)</sup></b>					
No	No	No	No	No	No
<b>ADC (Primary Groups/Channels)</b>					
5/40	5/40	5/40	5/40	8/64	5/40
<b>ADC (Secondary Groups/Channels)</b>					
4/60	4/60	4/60	4/60	4/60	4/60
<b>ADC (Fast Compare Channels)</b>					
4	4	4	4	4	4
<b>ADC (EDSADC Channels)</b>					
6	6	6	6	10	6
<b>CAN (Modules/Nodes)</b>					
3/3x4	3/3x4	3/3x4	3/3x4	3/3x4	3/3x4
<b>FlexRay (Modules/Channels)</b>					
2/2x2	2/2x2	2/2x2	2/2x2	2/2x2	2/2x2
<b>HSSL Modules</b>					
1	1	1	1	1	1
<b>ASCLIN Modules / with ASC &amp; LIN / with 3-wire SPI</b>					
24/24/11	24/24/11	24/24/11	24/24/11	24/24/12	24/24/11
<b>QSPI Modules / with LVDS</b>					
5/2	5/2	5/2	5/2	5/2	5/2

(table continues...)

<sup>2)</sup> AMU is abbreviated as ASC Modeling Unit. For Additional details about AMU, Contact an Infineon Representative

1 TC38x AE step variants

Table 2 (continued) TC38x\_AE step (part 2)

SAL-TC387TP-128F300S	SAK-TC387TP-160F300S	SAL-TC387TP-160F300S	SAK-TC387QM-160F300S	SAK-TC389QP-160F400S	SAK-TC387QP-160F400S
<b>SENT Channels</b>					
20	20	20	20	25	20
<b>MSC Modules</b>					
2	2	2	2	3	2
<b>PSI5 Channels</b>					
4	4	4	4	4	4
<b>PSI5-S Module</b>					
Yes	Yes	Yes	Yes	Yes	Yes
<b>SDMMC Module</b>					
No	No	No	No	No	No
<b>Max. Ethernet Availability: 1Gbit/100Mbit/No</b>					
1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s
<b>MCDS Availability</b>					
miniMCDS	miniMCDS	miniMCDS	miniMCDS	miniMCDS	miniMCDS
<b>ADAS Cluster Available</b>					
No	No	No	No	No	No
<b>CIF</b>					
No	No	No	No	No	No
<b>HSM Available</b>					
Yes	Yes	Yes	Yes	Yes	Yes

## 2 TC38x AD step variants

### 2 TC38x AD step variants

The following tables list the TC38x AD step variants.

#### 2.1 TC38x AD step (part 1)

A table listing the TC38x AD step variants.

**Table 3** TC38x\_AD step (part 1)

SAL-TC389QP-160 F300S	SAL-TC387QP-160 F300S	SAK-TC389QP-160 F300S	SAK-TC387QP-160 F300S	SAK-TC387TP-128 F300S	SAL-TC387TP-128 F300S	SAK-TC387TP-160 F300S
<b>Step</b>						
AD	AD	AD	AD	AD	AD	AD
<b>Production Status</b>						
Standard	Standard	Standard	Standard	Customer Specific	Customer Specific	Customer Specific
<b>Package Type</b>						
PG-FBGA-516	PG-LFBGA-292	PG-FBGA-516	PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292
<b>Pinout</b>						
LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm
<b>Reference Silicon</b>						
TC38x	TC38x	TC38x	TC38x	TC38x	TC38x	TC38x
<b>Temperature Range (Ambient)</b>						
SAL	SAL	SAK	SAK	SAK	SAL	SAK
<b>Chip ID</b>						
<b>Attention:</b> The value of SCU_CHIPID in the UCODE field contains the default value 0 not the µCode version.						
0x8C008983	0x8C008783	0x8C008983	0x8C008783	0xCB008783	0xCB008783	0xFC008783
<b>Cores / Checker Cores</b>						
4/2	4/2	4/2	4/2	3/2	3/2	3/2
<b>Max. Freq. (MHz)</b>						
300	300	300	300	300	300	300
<b>Program Flash (MB)</b>						
10	10	10	10	8	8	10
<b>Data Flash0 (single-ended) (KB)</b>						
512	512	512	512	512	512	512
<b>Total SRAM (without EMEM and Cache) (KB)</b>						
1376	1376	1376	1376	1152	1152	960
<b>EMEM Size (KB)</b>						
<b>(table continues...)</b>						

## 2 TC38x AD step variants

Table 3 (continued) TC38x\_AD step (part 1)

SAL-TC389QP-160 F300S	SAL-TC387QP-160 F300S	SAK-TC389QP-160 F300S	SAK-TC387QP-160 F300S	SAK-TC387TP-128 F300S	SAL-TC387TP-128 F300S	SAK-TC387TP-160 F300S
0	0	0	0	0	0	0
<b>DSPR (KB)</b>						
240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	160 in CPU0; 128 in CPU1; 96 other
<b>DLMU (KB)</b>						
64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU
<b>PSPR (KB)</b>						
64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU
<b>LMU (KB)</b>						
128	128	128	128	128	128	128
<b>DAM (KB)</b>						
64	64	64	64	64	64	64
<b>AMU<sup>3)</sup></b>						
No	No	No	No	No	No	No
<b>ADC (Primary Groups/Channels)</b>						
8/64	5/40	8/64	5/40	5/40	5/40	5/40
<b>ADC (Secondary Groups/Channels)</b>						
4/60	4/60	4/60	4/60	4/60	4/60	4/60
<b>ADC (Fast Compare Channels)</b>						
4	4	4	4	4	4	4
<b>ADC (EDSADC Channels)</b>						
10	6	10	6	6	6	6
<b>CAN (Modules/Nodes)</b>						
3/3x4	3/3x4	3/3x4	3/3x4	3/3x4	3/3x4	3/3x4
<b>FlexRay (Modules/Channels)</b>						
2/2x2	2/2x2	2/2x2	2/2x2	2/2x2	2/2x2	2/2x2
<b>HSSL Modules</b>						
1	1	1	1	1	1	1
<b>ASCLIN Modules / with ASC &amp; LIN / with 3-wire SPI</b>						
24/24/12	24/24/11	24/24/12	24/24/11	24/24/11	24/24/11	24/24/11

(table continues...)

<sup>3</sup> AMU is abbreviated as ASC Modeling Unit. For Additional details about AMU, Contact an Infineon Representative

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**2 TC38x AD step variants**
**Table 3 (continued) TC38x\_AD step (part 1)**

SAL-TC389QP-160 F300S	SAL-TC387QP-160 F300S	SAK-TC389QP-160 F300S	SAK-TC387QP-160 F300S	SAK-TC387TP-128 F300S	SAL-TC387TP-128 F300S	SAK-TC387TP-160 F300S
<b>QSPI Modules / with LVDS</b>						
5/2	5/2	5/2	5/2	5/2	5/2	5/2
<b>SENT Channels</b>						
25	20	25	20	20	20	20
<b>MSC Modules</b>						
3	2	3	2	2	2	2
<b>PSI5 Channels</b>						
4	4	4	4	4	4	4
<b>PSI5-S Module</b>						
Yes	Yes	Yes	Yes	Yes	Yes	Yes
<b>SDMMC Module</b>						
No	No	No	No	No	No	No
<b>Max. Ethernet Availability: 1Gbit/100Mbit/No</b>						
1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s
<b>MCDS Availability</b>						
miniMCDS	miniMCDS	miniMCDS	miniMCDS	miniMCDS	miniMCDS	miniMCDS
<b>ADAS Cluster Available</b>						
No	No	No	No	No	No	No
<b>CIF</b>						
No	No	No	No	No	No	No
<b>HSM Available</b>						
Yes	Yes	Yes	Yes	Yes	Yes	Yes

## 2 TC38x AD step variants

### 2.2 TC38x AD step (part 2)

A continuation table listing the TC38x AD step variants.

**Table 4** TC38x\_AD step (part 2)

<b>SAL-TC387TP-160F300S</b>	
<b>Step</b>	AD
<b>Production Status</b>	Customer Specific
<b>Package Type</b>	PG-LFBGA-292
<b>Pinout</b>	LFBGA 0.8 mm
<b>Reference Silicon</b>	TC38x
<b>Temperature Range (Ambient)</b>	SAL
<b>Chip ID</b>	
<i>Attention: The value of SCU_CHIPID in the UCODE field contains the default value 0 not the µCode version.</i>	
	0xFC008783
<b>Cores / Checker Cores</b>	3/2
<b>Max. Freq. (MHz)</b>	300
<b>Program Flash (MB)</b>	10
<b>Data Flash0 (single-ended) (KB)</b>	512
<b>Total SRAM (without EMEM and Cache) (KB)</b>	960
<b>EMEM Size (KB)</b>	0
<b>DSPR (KB)</b>	160 in CPU0; 128 in CPU1; 96 other
<b>DLMU (KB)</b>	64 per CPU
<b>(table continues...)</b>	

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**2 TC38x AD step variants**
**Table 4 (continued) TC38x\_AD step (part 2)**

	<b>SAL-TC387TP-160F300S</b>
<b>PSPR (KB)</b>	64 per CPU
<b>LMU (KB)</b>	128
<b>DAM (KB)</b>	64
<b>AMU<sup>4)</sup></b>	No
<b>ADC (Primary Groups/Channels)</b>	5/40
<b>ADC (Secondary Groups/Channels)</b>	4/60
<b>ADC (Fast Compare Channels)</b>	4
<b>ADC (EDSADC Channels)</b>	6
<b>CAN (Modules/Nodes)</b>	3/3x4
<b>FlexRay (Modules/Channels)</b>	2/2x2
<b>HSSL Modules</b>	1
<b>ASCLIN Modules / with ASC &amp; LIN / with 3-wire SPI</b>	24/24/11
<b>QSPI Modules / with LVDS</b>	5/2
<b>SENT Channels</b>	20
<b>MSC Modules</b>	2
<b>PSI5 Channels</b>	4
<b>(table continues...)</b>	

<sup>4</sup> AMU is abbreviated as ASC Modeling Unit. For Additional details about AMU, Contact an Infineon Representative

2 TC38x AD step variants

Table 4 (continued) TC38x\_AD step (part 2)

	<b>SAL-TC387TP-160F300S</b>
<b>PSI5-S Module</b>	Yes
<b>SDMMC Module</b>	No
<b>Max. Ethernet Availability: 1Gbit/100Mbit/No</b>	1Gbit/s
<b>MCDS Availability</b>	miniMCDS
<b>ADAS Cluster Available</b>	No
<b>CIF</b>	No
<b>HSM Available</b>	Yes

3 Memory maps of TC38x variants

### 3 Memory maps of TC38x variants

This section shows the influence of above feature variants on the memory map.

#### Program Flash

Variants:

- 10 MB: umbrella (3 x 3 MB, 1 x 1 MB), see User's Manual
- 8 MB: following configurations are available. See Figure below.
  - 3 MB + 1 MB + 3 MB + 1 MB
  - 3 MB + 3 MB + 2 MB

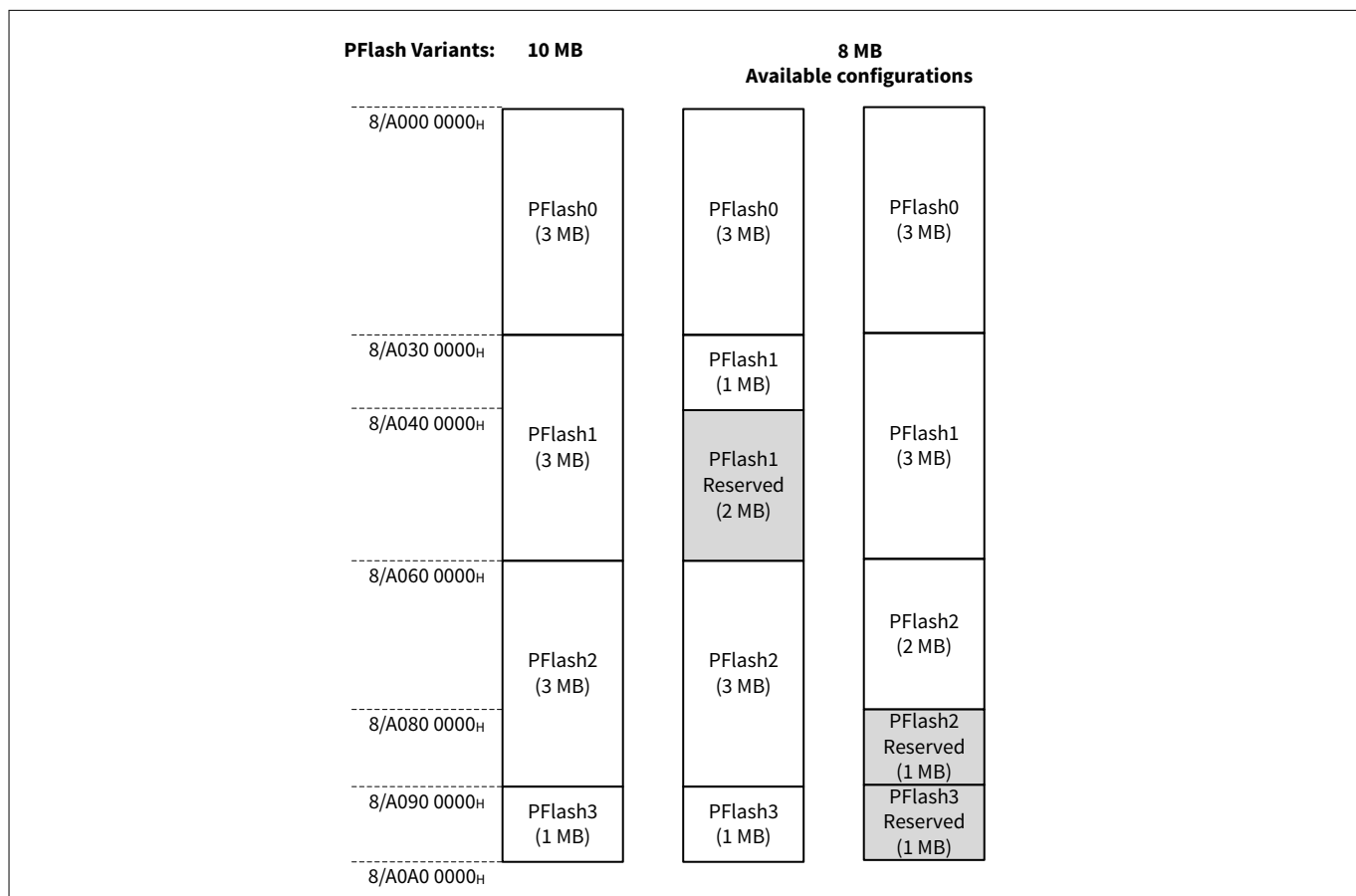


Figure 1 TC38x PFlash variants

#### Cores/Checker cores

Variants:

- 4/2: umbrella, see User's Manual
- 3/2: not available is CPU3 including its RAMs (DSPR, DCACHE, DTAG, PSPR, PCACHE, PTAG, DLMU)

#### CPU RAMs

Variants:

- DSPR: 240 KB in CPU0 & CPU1, 96 KB in CPU2 & CPU3: umbrella, see User's Manual
- DSPR: 240 KB in CPU0 & CPU1, 96 KB in CPU2: default for 3/2 Cores/Checker Cores configuration (see Figure below for available DSPR address ranges)
- DSPR: 160 KB in CPU0, 128 KB in CPU1, 96 KB in CPU2: reduced RAM variant of 3/2 Cores/Checker Cores configuration (see Figure below for available DSPR address ranges)

3 Memory maps of TC38x variants

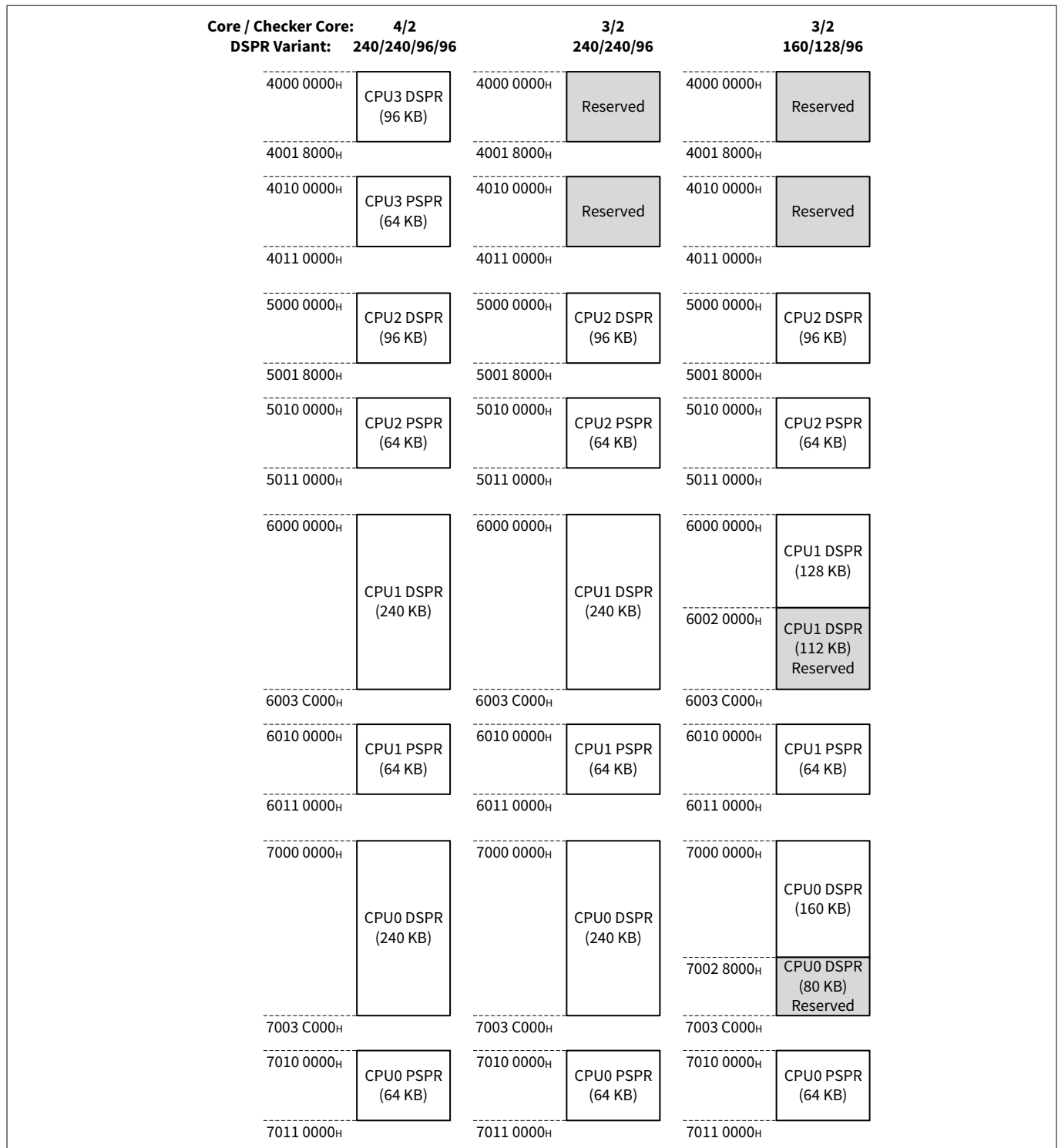


Figure 2 DSPR variants

ADC availability

- Limitation on availability of ADC channels are caused by pin limitations. See Data Sheet for the pinning table of the package

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**Revision history**
**Revision history**

Document version	Date of release	Description of changes
V1.0	2018-06-08	<ul style="list-style-type: none"> <li>First release</li> </ul>
V1.1	2018-08-06	<ul style="list-style-type: none"> <li>Added row "Reference Silicon" (needed e.g. for TC37x) to refer user to User's Manual Appx</li> </ul>
V1.2	2019-02-04	<ul style="list-style-type: none"> <li>Removed from "Memory Maps" the description for LMU and DAM variations as these are not varied</li> <li>"Variant Tables": added SAL-TC387TP-128F300S</li> </ul>
V1.3	2019-03-01	<ul style="list-style-type: none"> <li>"About this document": reduced list of described Feature Package to the used ones</li> <li>"Memory Maps": added hint to understand ADC device specific differences</li> <li>"Variant Tables": changed Production Status of several devices</li> <li>"Variant Tables": clarified Total SRAM value is without cache memories</li> </ul>
V1.4	2019-06-12	<ul style="list-style-type: none"> <li>Chapter 1: Added the TC38x AE step variants table</li> <li>Chapter 1 and 2: TC38x Ax step variants table format changed to fit all the contents</li> <li>Chapter 1 and 2: Added new row in the variant tables called "AMU" with the footnote for additional details</li> <li>Chapter: About this document: Feature package definitions are updated to consistent with the product naming nomenclature definition</li> </ul>
V1.5	2020-01-10	<ul style="list-style-type: none"> <li>Chapter 1,2: Total SRAM (without EMEM and Cache) size is corrected for SAK-TC387TP-160F300S and SAL-TC387TP-160F300S</li> <li>Page 1: About the document: Feature Package 'X' definition is updated to remove CIF</li> <li>Chapter 1 and 2: Added new row in the variant tables called "CIF" indicating the Camera Interface availability</li> </ul>
V1.6	2020-11-18	<ul style="list-style-type: none"> <li>Chapter 1,2: Package type name for SAK-TC389QP-160F300S, SAK-TC389QN-160F300S, SAL-TC389QP-160F300S is corrected from PG-LFBGA-516 to PG-FBGA-516</li> <li>Chapter 1 and 2: Removed Bare Die Marking variant SAL-TC380QP-160F300</li> </ul>
V1.7	2023-03-02	<ul style="list-style-type: none"> <li>Chapter 3 : Updated the Program flash variants memory figure</li> </ul>
V1.8	2025-08-19	<ul style="list-style-type: none"> <li>Chapter 1 : Added new variant: SAK-TC387QM-160F300S</li> </ul>
V1.9	2025-12-12	<ul style="list-style-type: none"> <li>Chapter 1 : Added new variants: SAK-TC389QP-160F400S, SAK-TC387QP-160F400S</li> </ul>

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