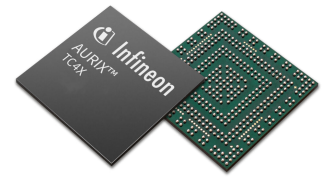


AURIX™ 3rd Generation 32-bit single-chip microcontroller**Features**

- High performance microcontroller with 5 CPU cores and a PPU
- CPUs are 32-bit super-scalar TriCore™ CPUs (TC1.8 LS) with virtual machine hardware support and double precision floating point arithmetic; 5 fully lockstepped cores
- Low latency SRAMs close to the CPUs and global SRAM
- 20 MB of embedded program memory with multiple parallel banks and A/B swap option
- Up to 1152 KB of embedded data NVM (includes both, DNVM 0 and DNVM 1)
- High performance cyber security architecture with 1 MB of program memory and 128 KB of data memory
- 2 DMA controllers each with 128/64 channels and 2 move engines
- ADC sub-system with 10 Delta-Sigma ADCs (DSADC), 8 external modulator channels (EXMOD), 14 SAR ADC cores. Each 2 SAR ADC cores share 16 inputs equipped with sample and hold stage (TMADC), 12 embedded DSP cores for flexible post processing of ADC results (CDSP), a fast compare cluster with 10 inputs (FC)
- A GTM timer unit with input and output channels
- An eGTM timer unit with input and output channels
- 4 GPT12 timer units
- High speed communication interfaces (LETH, CANXL, xSPI, HSSL, SDMMC)
- Low speed communication interfaces (CAN, FlexRay, QSPI, ASCLIN, I2C)
- Sensor interfaces (MSC, SENT, PSI5, PSI5-S)
- Sophisticated interrupt system with interrupt router and ECC
- Safety and security alarm Management Unit (SMU) handling safety and cyber security alarms
- Advanced debug and trace with support of run control debugging for multi-core and time aligned multi-core program and data trace for all CPUs in parallel, and 5 Gbps high speed serial trace interface
- Includes a DAP or JTAG port, with an optional DAPE port on select devices
- Digital programmable IO ports
- Volatile Memory Test (VMT) unit with ECC, memory initialization, and MBIST functions
- Power Management System and on-chip regulators
- Clock generation unit with system PLL and peripheral PLL
- Embedded voltage regulators

**Product validation**

Product validation according to AEC-Q100, Grade 1.

Qualified for automotive applications.

Table of contents

	Key features	1
	Product validation	1
	Table of contents	2
1	Device feature set	8
1.1	Device feature set description	8
1.2	Device feature set table	10
2	Marking options	14
2.1	Product name identifier	14
2.2	TC49xN AB step variants	16
2.2.1	TC49xN_AB step (part 1)	16
2.2.2	TC49xN_AB step (part 2)	19
2.2.3	TC49xN_AB step (part 3)	23
3	Pin definition and functions	27
3.1	Logic symbols for package variants	27
3.2	BGA436_STD package variant pin configuration	28
3.2.1	BGA436_STD port 00	28
3.2.2	BGA436_STD port 01	43
3.2.3	BGA436_STD port 02	55
3.2.4	BGA436_STD port 10	71
3.2.5	BGA436_STD port 11	86
3.2.6	BGA436_STD port 12	100
3.2.7	BGA436_STD port 13	102
3.2.8	BGA436_STD port 14	113
3.2.9	BGA436_STD port 15	127
3.2.10	BGA436_STD port 20	140
3.2.11	BGA436_STD port 21	151
3.2.12	BGA436_STD port 22	160
3.2.13	BGA436_STD port 23	170
3.2.14	BGA436_STD port 24	176
3.2.15	BGA436_STD port 25	181
3.2.16	BGA436_STD port 26	190
3.2.17	BGA436_STD port 30	191
3.2.18	BGA436_STD port 31	201
3.2.19	BGA436_STD port 32	206
3.2.20	BGA436_STD port 33	214
3.2.21	BGA436_STD port 34	239
3.2.22	BGA436_STD analog	246
3.2.23	BGA436_STD special	255

3.2.24	BGA436_STD system	255
3.2.25	BGA436_STD supply	256
3.3	BGA292_STD package variant pin configuration	258
3.3.1	BGA292_STD port 00	259
3.3.2	BGA292_STD port 01	271
3.3.3	BGA292_STD port 02	275
3.3.4	BGA292_STD port 10	289
3.3.5	BGA292_STD port 11	299
3.3.6	BGA292_STD port 12	313
3.3.7	BGA292_STD port 13	314
3.3.8	BGA292_STD port 14	318
3.3.9	BGA292_STD port 15	328
3.3.10	BGA292_STD port 20	336
3.3.11	BGA292_STD port 21	348
3.3.12	BGA292_STD port 22	357
3.3.13	BGA292_STD port 23	367
3.3.14	BGA292_STD port 32	373
3.3.15	BGA292_STD port 33	381
3.3.16	BGA292_STD port 34	406
3.3.17	BGA292_STD analog	414
3.3.18	BGA292_STD special	419
3.3.19	BGA292_STD system	420
3.3.20	BGA292_STD supply	420
3.4	Pad Sequence	422
3.4.1	Sequence of pads in pad frame	422
3.5	Legend	444
4	Electrical characteristics	446
4.1	Parameter interpretation	446
4.2	Absolute maximum ratings	447
4.2.1	Absolute maximum ratings	447
4.3	Pin reliability in overload	448
4.3.1	Overload characteristics	448
4.4	Operating conditions	451
4.4.1	Clock operating conditions	451
4.4.2	Supply operating conditions	453
4.4.3	Limitation of supply voltage over time	455
4.4.4	Temperature operating conditions	456
4.4.5	Example temperature profiles	457
4.5	Switchable pad characteristics	459
4.5.1	↪ PORST Pad characteristics	459
4.5.2	5 V switchable pad characteristics	460
4.5.2.1	Fast 5V GPIO characteristics	460

4.5.2.2	Slow 5V GPIO characteristics	463
4.5.2.3	Class S 5V characteristics	465
4.5.3	3.3 V switchable pad characteristics	466
4.5.3.1	Fast 3.3V GPIO characteristics	466
4.5.3.2	Slow 3.3V GPIO characteristics	469
4.5.3.3	Class S 3.3V characteristics	471
4.5.4	Class D characteristics	472
4.5.5	ADC reference pads characteristics	473
4.5.6	Driver mode selection for slow and fast pads	474
4.6	High performance LVDS pad characteristic	475
4.6.1	LVDS - IEEE standard LVDS general purpose link (GPL)	475
4.6.2	LVDS pad input model	477
4.7	TMADC characteristics	478
4.7.1	TMADC 5V characteristics	478
4.7.2	TMADC input structure figure	481
4.8	DSADC characteristics	481
4.8.1	DSADC 5V characteristics	482
4.9	FCC characteristics	483
4.9.1	FCC characteristics	484
4.10	High Resolution PWM characteristics	485
4.10.1	HRPWM characteristics	485
4.11	External clock sources	486
4.11.1	OSC_XTAL characteristics	486
4.11.2	RTC 32 kHz oscillator characteristics	487
4.12	Internal clock sources	489
4.12.1	Back-up oscillator characteristics	489
4.12.2	Standby oscillator characteristics	489
4.13	System Phase Locked Loop (SYS_PLL) characteristics	490
4.13.1	System PLL characteristics	490
4.14	Peripheral Phase Locked Loop (PER_PLL) characteristics	491
4.14.1	Peripheral PLL characteristics	491
4.15	Power supply topology and power supply characteristics	492
4.15.1	Power supply topology	492
4.15.2	Supply ramp-up and ramp-down behavior	493
4.15.3	LVD reset characteristics	494
4.15.4	Line Transients	495
4.16	PMS characteristics	497
4.16.1	VDDPMS0 and VDDSB RAM regulator characteristics	497
4.16.2	VDDPMS1 regulator characteristics	498
4.16.3	EVRC SMPS characteristics	499
4.16.4	EVRC SMPS external components	502
4.16.5	Internal supply voltage operating conditions	504

4.17	System mode dependent and reset timing characteristics	505
4.17.1	System state timings	505
4.17.2	Reset timings	507
4.17.3	Power, pad and reset timing figure	509
4.18	PMS voltage monitoring characteristics	509
4.18.1	Primary and secondary voltage monitor ADC characteristics	510
4.18.2	Primary voltage monitors	510
4.18.2.1	Primary voltage monitors parameters overview	510
4.18.2.2	Primary voltage monitors characteristics	512
4.18.3	Secondary voltage monitors	516
4.18.3.1	Secondary voltage monitors parameters overview	516
4.18.3.2	Secondary voltage monitors characteristics	517
4.19	Stand-by Controller (SCR)	522
4.19.1	SCR SAR ADC characteristics	522
4.20	Temperature sensor characteristics	523
4.20.1	VTMON DTS characteristics	523
4.20.2	PMS DTS characteristics	524
4.21	Current consumption characteristics	525
4.21.1	Definition of TC49xN application use cases	525
4.21.2	Current consumption and power dissipation overview in RUN mode	529
4.21.3	Respective supply rail currents in RUN mode	530
4.21.4	Current consumption in SLEEP and STANDBY modes	531
4.21.5	Load Transients	533
4.22	AC characteristics	534
4.23	ASCLIN SPI Master timing characteristics	535
4.23.1	ASCLIN Master Mode timing for strong sharp (ss) output pads	535
4.23.2	ASCLIN Master Mode timing for strong medium (sm) output pads	536
4.23.3	ASCLIN Master Mode timing for medium (m) output pads	537
4.23.4	ASCLIN SPI Master timing figures	538
4.24	Inter-IC (I2C) interface timing characteristics	539
4.24.1	I2C standard mode timing	539
4.24.2	I2C fast mode timing	540
4.24.3	I2C high speed mode timing	541
4.24.4	I2C standard and fast mode timing figures	542
4.25	CAN characteristics	542
4.25.1	CAN internal receive delay for all pads	542
4.25.2	CAN internal transmit delay for strong sharp (ss) output pads	543
4.25.3	CAN internal transmit delay for medium (m) output pads	543
4.25.4	CAN internal transmit delay for strong medium (sm) output pads	544
4.26	CAN XL characteristics	544
4.26.1	CANXL internal receive delay for all pads	544
4.26.2	CANXL internal transmit delay for strong sharp (ss) output pads	544

4.26.3	CANXL internal transmit delay for medium (m) output pads	545
4.26.4	CANXL internal transmit delay for strong medium (sm) output pads	545
4.27	MSC 5V timing characteristics	545
4.27.1	MSC clock/data timing for strong sharp (ss) 5V output pads	546
4.27.2	MSC clock/data timing for strong medium (sm) 5V output pads	546
4.27.3	MSC clock/data timing for medium (m) 5V output pads	547
4.27.4	MSC clock/data timing for LVDS 5V output pads	547
4.27.5	Upstream interface timing	548
4.27.6	MSC clock/data timing figures	548
4.28	E-Ray characteristics	549
4.28.1	Transmit characteristics	549
4.28.2	Receive characteristics	550
4.29	QSPI timing characteristics, Master and Slave Mode	551
4.29.1	QSPI Master Mode timing characteristics	551
4.29.1.1	QSPI Master Mode timing for strong sharp (ss) output pads	551
4.29.1.2	QSPI Master Mode timing for strong medium (sm) output pads	553
4.29.1.3	QSPI Master Mode timing for medium (m) output pads	554
4.29.1.4	QSPI Master Mode timing for LVDS output pads (clock/data)	555
4.29.1.5	QSPI Master Mode timing figures	556
4.29.2	QSPI Slave Mode timing characteristics	557
4.29.2.1	QSPI Slave Mode timing	557
4.29.2.2	QSPI Slave Mode timing figures	558
4.30	SDMMC Interface timing characteristics	559
4.30.1	SDMMC timing	559
4.30.2	SDMMC timing figure	560
4.31	HSCT characteristics	560
4.31.1	HSCT - Rx parasitics and loads	560
4.31.2	HSCT - Rx/Tx setup timing characteristics	561
4.31.3	HSCT characteristics	561
4.31.4	HSCT eye diagram	562
4.32	Ethernet Interface (ETH) timing characteristics	563
4.32.1	ETH definition of measurement reference points	563
4.32.2	ETH Management signal timing characteristics (ETH_MDC, ETH_MDIO)	563
4.32.2.1	ETH management signal timing	563
4.32.2.2	ETH management signal timing figures	564
4.32.3	ETH 10BASE-T1S signal timing characteristics	564
4.32.3.1	ETH 10BASE-T1S signal timing	564
4.32.3.2	ETH 10BASE-T1S signal timing figure	565
4.32.4	ETH MII timing characteristics	565
4.32.4.1	ETH MII signal timing	565
4.32.4.2	ETH MII signal timing figures	566
4.32.5	ETH RMII timing characteristics	566

4.32.5.1	ETH RMII signal timing valid for 3.3V	566
4.32.5.2	ETH RMII signal timing figures	567
4.32.6	ETH SERDES characteristics	567
4.32.6.1	ETH SERDES transmitter characteristics	568
4.32.6.2	ETH SERDES transmitter eye	569
4.32.6.3	ETH SERDES receiver characteristics	569
4.32.6.4	ETH SERDES receiver eye	570
4.33	FSP timing characteristics	570
4.34	Flash characteristics	571
4.35	xSPI timing characteristics	574
4.35.1	xSPI SDR timing without data strobe	575
4.35.2	xSPI SDR without data strobe timing figure	575
4.36	DAP timing characteristics	577
4.36.1	DAP timing	577
4.36.2	SCR DAP timing	577
4.36.3	DAP timing figures	578
4.37	JTAG timing characteristics	579
4.37.1	JTAG timing	579
4.37.2	JTAG timing figures	580
4.38	SGBT characteristics	580
4.38.1	SGBT transmitter characteristics	581
4.39	External components	582
4.39.1	HSPHY external components	582
4.39.2	Buffering and decoupling capacitors	583
4.40	Quality declarations	584
4.40.1	Quality parameters	584
4.40.2	SRAM related fault tolerance	584
5	Package information	585
5.1	PG-F2BGA-436	585
5.1.1	PG-F2BGA-436 outline	585
5.1.2	PG-F2BGA-436 characteristics	585
5.2	PG-F2BGA-292	587
5.2.1	PG-F2BGA-292 outline	587
5.2.2	PG-F2BGA-292 characteristics	587
6	Revision history	589
	Disclaimer	590

1 Device feature set

1.1 Device feature set description

The TC49xN product has the following features:

- High performance microcontroller with 5 CPU cores
- 5 fully lock-stepped 32-bit super-scalar TriCore™ CPUs (TC1.8 LS) with hardware virtualization, overlay support and double precision floating point arithmetic
- Parallel processing unit (PPU)
 - 416 KB of low latency memory (which includes VCCM, CSM and cache memory)
 - A local DMA to support data transfer from system memories to local PPU memories
 - Low latency peripheral interface to ADC and timer modules
- SRAM
 - Low latency SRAMs close to the CPUs with 3056 KB
 - Global SRAM with 3 MB
- Embedded flash
 - Data flash up to 1152 KB
 - Program flash up to 21 MB
 - Support of software over the air (SOTA) updates with improved A/B swap option
- High performance cyber security architecture
 - Cyber security real-time module (CSRM) with TriCore™ CPU with local low latency SRAM, private program and data flash and security hardware accelerators
 - Cyber security satellite (CSS) with accelerators for various symmetric cryptographic algorithms, such as AES, SHA, and ChaChaPoly, multi-channel architecture for high throughput and accessible for all CPUs
- 2 DMA controllers with 128/64 channels and 2 move engines each
- ADC sub-system with
 - 10 Delta-Sigma ADCs (DSADC)
 - 8 dedicated demodulator channels (EXMOD) for connecting external (single bit output) Delta-Sigma Modulator (DSM)
 - 14 SAR ADC cores. Each 2 ADC cores share 16 inputs equipped with sample and hold stage (TMADC)
 - 12 embedded DSP cores for flexible post processing of ADC results (CDSP)
 - Fast compare cluster with 10 inputs (FC)
- A GTM timer unit with 56 input and 160 output channels
- An eGTM timer unit with 24 input and 72 output channels optimized for xEV and chassis applications
- High speed communication interfaces
 - 3 x 10/100 Mbps and 1 x 10/100/1000 Mbps Ethernet ports (with 10BASE-T1S support) with advanced layer 2 bridging function
 - A data routing engine (DRE) for low latency CAN routing and CAN to IEEE 1722 Ethernet packet translation, Ethernet to Ethernet routing

1 Device feature set

- 2 CANXL nodes supporting up to 20* Mbps (*only with Fast pads)
- 2 HSSL links
- Memory interfaces
 - xSPI supporting up to Quad
 - 1 SDMMC interface supporting High Speed (HS) mode
- Low speed communication interfaces
 - 16 CAN nodes with integrated CAN-to-CAN packet routing
 - 2 FlexRay channels
 - 8 Queued SPI channels with up to 16 chip selects each
 - 8 ASCLIN channels
 - 2 I2C interfaces
- Sensor Interfaces
 - 3 MSC modules
 - 2 SENT modules with 15 channels each
 - 4 PSI5 channels, 2 PSI5-S modules
- Sophisticated interrupt system with interrupt router and ECC
- Safety and security alarm Management Unit (SMU) handling safety monitor alarms
- Advanced debug and trace
 - Rich support of run control debugging for multi-core, time aligned multi-core program and data trace for all CPUs in parallel
 - SGBT Interface based on Aurora protocol
 - Up to 5 Gbps high speed serial trace interface
 - Use of Ethernet ports for debug and trace purposes
 - Includes a DAP or JTAG port, with an optional DAPE port on select devices
 - DXCPL support (DAP interface over CAN)
- Digital programmable IO ports
- Volatile Memory Test with ECC, memory initialization and MBIST functions (VMT)
- Power Management System and on-chip regulators
- Clock Generation Unit with system PLL and peripheral PLL
- Embedded voltage regulators

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself. That is, its function set, the temperature range, and the supply voltage
- The package and the type of delivery

This document describes the derivatives of the device. The following tables enumerates these derivatives and summarizes the differences.

1.2 Device feature set table

Table 1 Device feature set table

Feature		TC49xN STD
CPUs	Type	TC1.8 LS
	Cores / checker cores	5 / 5
	Maximum frequency	400 MHz
Cache per CPU	Program	32 KB
	Data	16 KB
SRAM per CPU	PSPR	64 KB for CPU 0, 1, 2, 3, 4, and 5
	DSPR	240 KB for CPU 0, 1, and 2; 112 KB for CPU 3 and 4
	DLMU	512 KB for CPU 0, 1 and 2; 128 KB for CPU 3 and 4
SRAM global	LMU	3072 KB
Program memory	Size	4 MB (2x2 MB) each for CPU 0, 1, 2, 3, and 4
	Banks	10
Data memory	Size (single-ended)	DF0 1024 KB; DF1 128 KB
CPU-CS	Type	TC1.8 non LS
	Maximum frequency	200 MHz
Cache CPU-CS	Program	32 KB
	Data	16 KB
SRAM CPU-CS	PSPR	64 KB
	DSPR	240 KB
	DLMU	-
Program memory CPU-CS	Size	1 MB
CSS	AES engine	3
	Channel 0	204 bytes Input FIFO and 256 bytes Output FIFO
	Channel 1-2	1548 bytes Input FIFO and 1536 bytes Output FIFO
	Channel 3-20	268 bytes Input FIFO and 192 bytes Output FIFO
PPU	Scalar core	1
	Vector width	256 bits
	Cache	16 KB instruction + 16 KB data
	VCCM	128 KB

(table continues...)

Table 1 (continued) Device feature set table

Feature		TC49xN STD
	CSM	256 KB
	Vector DSP unit	Information is only available under NDA.
	Maximum frequency	400 MHz
DMA	Channels	DMA0 128 ch, DMA1 64 ch
TMADC	SAR cores	14
	Sample and hold circuitry per 2 SAR cores	16
FC	Channels	10
DSADC	Channels	10
EXMOD	Channels	8
CDSP	Cores	12
	Data SRAM per core	3 KB
	Program SRAM per core	3 KB
GTM Classic	TIM	7 TIM * 8 ch = 56 input ch
	TOM	5 TOM * 16 ch = 80 16-bit output ch
	ATOM	10 ATOM * 8 ch = 80 24-bit output ch
	MCS	7 MCS channel having 16 KB + 8 KB of RAM each
	PSM RAM (FIFO, 1024 x 29 bit)	2 x 3.63 KB
	TBU channels	4
	SPE	4
	BRC / DPLL	1
	DTM modules	10 @ TOM, 14 @ ATOM
eGTM	TIM	3 TIM * 8 ch = 24 input ch
	TOM	3 TOM * 16 ch = 48 16-bit output ch
	ATOM	3 ATOM * 8 ch = 24 24-bit output ch
	TBU channels	3
	SPE	3
	DTM modules	12 @ TOM, 6 @ ATOM
HRPWM	High Resolution PWM channels	3 x 8
Timer	GPT12	4

(table continues...)

Table 1 (continued) Device feature set table

Feature		TC49xN STD
STM	Modules	1 per CPU
FlexRay	Modules	1 module with A and B channel
	Channels	2
CAN	Modules	4 MCMCAN modules and 1 CANXL module
	Channels	4 channels per MCMCAN and 2 channels per CANXL
	Nodes	16 M_CAN and 2 X_CAN nodes
	Nodes which support TT-CAN	-
	CAN routing accelerator	Yes
	CAN to Ethernet	Yes
QSPI	Modules (up to 16 chip select per module)	8
	HSIC Channels	-
ASCLIN	Channels	8
I2C	Interfaces	2
SENT	Modules	2
	Channels	15 channels per module
Audio subsystem	I2S/TDM instances	-
	I2S/TDM sample rate range	-
	Mixer instances	-
	Mixer source:destination conversion ratios	-
	Mixer source sample rate range	-
	Mixer destination sample rate range	-
PSI5	Channels	4
PSI5-S	Modules	2
HSSL	Modules	2
MSC	Modules	3
xSPI	xSPI External Memory Interface (SDR support)	1
SDMMC	eMMC/SD Interface	1
LETH (10/100/1000 Mbps)	Modules	1
LETH (10/100 Mbps)	Modules	3
GETH	Modules	-
PCIe	Modules	-
HSPHY	MP8G PHY	1

(table continues...)

Table 1 (continued) Device feature set table

Feature		TC49xN STD
	DLL (used for xSPI and RGMII)	-
FCE	Modules	1
Safety support	SMU	Yes
	IOM	No
SPU	Modules	-
RIF	CSI2 Modules	-
Security	CSRM	1
Debug	OCDS	Yes
	MCDS	1 x MCDS 4P (32 KB TBUF); 1 x MCDS 2P (16 KB TBUF)
	SGBT	Yes for all ED
	DAPE	Yes for all ED
EVR	Type	EVRC Core Regulator
Low power features	Standby RAM	128 KB dLMU0 + 128 KB dLMU1
	SCR	Yes
Packages	Type	PG-F2BGA-292 and PG-F2BGA-436
IO	Type	5 V CMOS and 3.3 V CMOS, LVDS

2 Marking options

2.1 Product name identifier

The product name details the following information:

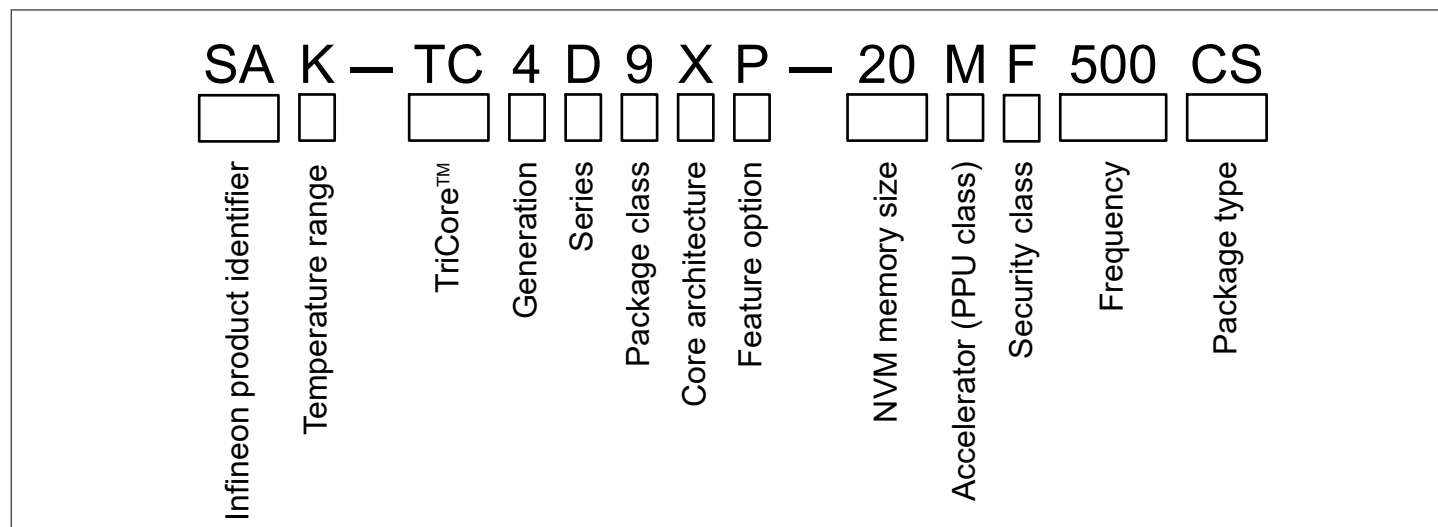


Figure 1 Example of a product name

Table 2 Encoding of the product name

Identifier	Encoding
Temperature range	
K	T_{ambient} Temperature Range from -40°C up to +125°C
A	T_{ambient} Temperature range from -40°C up to +105°C
L	T_{ambient} Temperature range from -40°C up to +150°C
Series	
D	D omain, Zone
Z	Z one
9	Real-time control
8	Domain, Zone
6	Real-time control
5	Radar
4	Chassis, Zone
2	Chassis, Safety
E	E lectrification
P	P ower conversion
S	S afety
Package class	
5	188 - PIN

(table continues...)

Table 2 (continued) Encoding of the product name

Identifier	Encoding
6	224 - PIN
7	292 - PIN
9	436 - PIN
Core architecture	
L	Single Core
D	Dual Core
T	Triple Core
Q	Quad Core
P	Penta Core
X	Hexa Core
Feature option	
P	Standard
Q	Standard + CAN-XL
C, M, V	Customer specific
E	Emulation device (available only up to engineering sample maturity)
X	Extended feature
NVM memory size	
03	3 MB
04	4 MB
05	5 MB
06	6 MB
08	8 MB
12	12 MB
16	16 MB
20	20 MB
24	24 MB
Accelerator (PPU class)	
N	No PPU
E	PPU 128 bits
M	PPU 256 bits
Security class	
F	Full CSRM (1x TC 1.8 + private NVM)

(table continues...)

Table 2 (continued) Encoding of the product name

Identifier	Encoding
O	Full CSRM + SMx (1x TC 1.8 + private NVM)
Frequency	
400	400 MHz
500	500 MHz
Package type	
CC	BGA - CuP COM
CS	BGA - CuP STD
MC	BGA - OvM COM
MS	BGA - OvM STD
MR	BGA - OvM (Radar)

2.2 TC49xN AB step variants

2.2.1 TC49xN_AB step (part 1)

A table listing the TC49xN AB step variants.

Table 3 TC49xN_AB step (part 1)

SAK- TC499PP-20MF 400MS	SAK- TC497PP-20M F400MS	SAK- TC499PQ-20M F400MS	SAK- TC497PQ-20M F400MS	SAK- TC499PP-20M O400MS	SAK- TC497PP-20M O400MS	SAK- TC499PQ-20M O400MS
Step						
AB	AB	AB	AB	AB	AB	AB
Production Status						
Standard	Standard	Standard	Standard	Standard	Standard	Standard
Package Type						
PG-F2BGA-436	PG-F2BGA-292	PG-F2BGA-436	PG-F2BGA-292	PG-F2BGA-436	PG-F2BGA-292	PG-F2BGA-436
Pinout						
BGA436_STD 0.8mm	BGA292_STD 0.8mm	BGA436_STD 0.8mm	BGA292_STD 0.8mm	BGA436_STD 0.8mm	BGA292_STD 0.8mm	BGA436_STD 0.8mm
Reference Silicon						
TC49x	TC49x	TC49x	TC49x	TC49x	TC49x	TC49x
Temperature Range (Ambient)						
SAK	SAK	SAK	SAK	SAK	SAK	SAK

(table continues...)

2 Marking options

Table 3 (continued) TC49xN_AB step (part 1)

SAK- TC499PP-20MF 400MS	SAK- TC497PP-20M F400MS	SAK- TC499PQ-20M F400MS	SAK- TC497PQ-20M F400MS	SAK- TC499PP-20M O400MS	SAK- TC497PP-20M O400MS	SAK- TC499PQ-20M O400MS
Chip ID						
0x66695523	0x65E95523	0x666AD523	0x65EAD523	0x666955A3	0x65E955A3	0x666AD5A3
Cores / Checker Cores						
5/5	5/5	5/5	5/5	5/5	5/5	5/5
Max. Freq. (MHz)						
400	400	400	400	400	400	400
NVM Type						
eFlash	eFlash	eFlash	eFlash	eFlash	eFlash	eFlash
Program NVM (MB)						
20	20	20	20	20	20	20
Data NVM0 (KB)						
1024	1024	1024	1024	1024	1024	1024
Total SRAM (without Cache) (KB)						
6560	6560	6560	6560	6560	6560	6560
Extension memory(KB)						
3072	3072	3072	3072	3072	3072	3072
DSPR (KB)						
240 in CPU0,1,2 and CSRM; 112 in others	240 in CPU0,1,2 and CSRM; 112 in others	240 in CPU0,1,2 and CSRM; 112 in others	240 in CPU0,1,2 and CSRM; 112 in others	240 in CPU0,1,2 and CSRM; 112 in others	240 in CPU0,1,2 and CSRM; 112 in others	240 in CPU0,1,2 and CSRM; 112 in others
DLMU (KB)						
512 in CPU 0,1 2; 128 in CPU3,4; 0 in CSRM	512 in CPU 0,1 2; 128 in CPU3,4; 0 in CSRM	512 in CPU 0,1 2; 128 in CPU3,4; 0 in CSRM	512 in CPU 0,1 2; 128 in CPU3,4; 0 in CSRM	512 in CPU 0,1 2; 128 in CPU3,4; 0 in CSRM	512 in CPU 0,1 2; 128 in CPU3,4; 0 in CSRM	512 in CPU 0,1 2; 128 in CPU3,4; 0 in CSRM
PSPR (KB)						
64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU
Hypervisor Support						
Yes	Yes	Yes	Yes	Yes	Yes	Yes
CSRM Available						
1	1	1	1	1	1	1
CSS Availability						
Yes	Yes	Yes	Yes	Yes	Yes	Yes

(table continues...)

2 Marking options

Table 3 (continued) TC49xN_AB step (part 1)

SAK- TC499PP-20MF 400MS	SAK- TC497PP-20M F400MS	SAK- TC499PQ-20M F400MS	SAK- TC497PQ-20M F400MS	SAK- TC499PP-20M O400MS	SAK- TC497PP-20M O400MS	SAK- TC499PQ-20M O400MS
PPU Availability						
1	1	1	1	1	1	1
ADC - TMADC (Instances / Cores)						
7/14	7/14	7/14	7/14	7/14	7/14	7/14
ADC - Fast Compare Converters						
10	10	10	10	10	10	10
ADC - DS Converters						
10	10	10	10	10	10	10
DSEXMOD						
8	8	8	8	8	8	8
CDSP Cores						
12	12	12	12	12	12	12
HRPWM Instances						
3	3	3	3	3	3	3
GTM Classic / eGTM availability						
Yes / Yes	Yes / Yes	Yes / Yes	Yes / Yes	Yes / Yes	Yes / Yes	Yes / Yes
Gigabit Ethernet (GETH) Instances (Gbps)						
0	0	0	0	0	0	0
Light Ethernet (LETH) Instances (Mbps)						
3x(10/100) + 1x(10/100/1000)	3x(10/100) + 1x(10/100/1000)	3x(10/100) + 1x(10/100/1000)	3x(10/100) + 1x(10/100/1000)	3x(10/100) + 1x(10/100/1000)	3x(10/100) + 1x(10/100/1000)	3x(10/100) + 1x(10/100/1000)
PCIe Instances						
0	0	0	0	0	0	0
CAN (Modules/Nodes)						
4/4x4	4/4x4	4/4x4	4/4x4	4/4x4	4/4x4	4/4x4
CANXL(Modules/Nodes)						
0/0	0/0	1/2	1/2	0/0	0/0	1/2
FlexRay (Modules/Channels)						
1/1x2	1/1x2	1/1x2	1/1x2	1/1x2	1/1x2	1/1x2
HSSL Modules						
2	2	2	2	2	2	2

(table continues...)

Table 3 (continued) TC49xN_AB step (part 1)

SAK- TC499PP-20MF 400MS	SAK- TC497PP-20M F400MS	SAK- TC499PQ-20M F400MS	SAK- TC497PQ-20M F400MS	SAK- TC499PP-20M O400MS	SAK- TC497PP-20M O400MS	SAK- TC499PQ-20M O400MS
ASCLIN Modules						
8	8	8	8	8	8	8
QSPI Modules						
8	8	8	8	8	8	8
I2C Interfaces						
2	2	2	2	2	2	2
xSPI Module						
1	1	1	1	1	1	1
SENT Channels						
30	30	30	30	30	30	30
MSC Modules						
3	2	3	2	3	2	3
PSI5 Channels						
4	4	4	4	4	4	4
PSI5-S Module						
2	2	2	2	2	2	2
SDMMC Module						
Yes	Yes	Yes	Yes	Yes	Yes	Yes
Audio-TDM/I2S interfaces						
0	0	0	0	0	0	0
SGBT availability						
No	No	No	No	No	No	No
MCDS availability						
Limited MCDS	Limited MCDS	Limited MCDS	Limited MCDS	Limited MCDS	Limited MCDS	Limited MCDS
DAPE availability						
No	No	No	No	No	No	No
CSI2 Interface						
0	0	0	0	0	0	0
Radar cluster(SPU, RIF)available / SPU instances / RIF Instance						
No/0/0	No/0/0	No/0/0	No/0/0	No/0/0	No/0/0	No/0/0

2.2.2 TC49xN_AB step (part 2)

A continuation table listing the TC49xN AB step variants.

Table 4 TC49xN_AB step (part 2)

SAK-TC497PQ-20M0400MS	
Step	AB
Production Status	Standard
Package Type	PG-F2BGA-292
Pinout	BGA292_STD 0.8mm
Reference Silicon	TC49x
Temperature Range (Ambient)	SAK
Chip ID	0x65EAD5A3
Cores / Checker Cores	5/5
Max. Freq. (MHz)	400
NVM Type	eFlash
Program NVM (MB)	20
Data NVM0 (KB)	1024
Total SRAM (without Cache) (KB)	6560
Extension memory(KB)	3072
DSPR (KB)	240 in CPU0,1,2 and CSRM; 112 in others
DLMU (KB)	512 in CPU 0,1 2; 128 in CPU3,4; 0 in CSRM

(table continues...)

Table 4 (continued) TC49xN_AB step (part 2)

	SAK-TC497PQ-20M0400MS
PSPR (KB)	64 per CPU
Hypervisor Support	Yes
CSRM Available	1
CSS Availability	Yes
PPU Availability	1
ADC - TMADC (Instances / Cores)	7/14
ADC - Fast Compare Converters	10
ADC - DS Converters	10
DSEXMOD	8
CDSP Cores	12
HRPWM Instances	3
GTM Classic / eGTM availability	Yes / Yes
Gigabit Ethernet (GETH) Instances (Gbps)	0
Light Ethernet (LETH) Instances (Mbps)	3x(10/100) + 1x(10/100/1000)
PCIe Instances	0
CAN (Modules/Nodes)	4/4x4

(table continues...)

Table 4 (continued) TC49xN_AB step (part 2)

	SAK-TC497PQ-20M0400MS
CANXL (Modules/Nodes)	1/2
FlexRay (Modules/Channels)	1/1x2
HSSL Modules	2
ASCLIN Modules	8
QSPI Modules	8
I2C Interfaces	2
xSPI Module	1
SENT Channels	30
MSC Modules	2
PSI5 Channels	4
PSI5-S Module	2
SDMMC Module	Yes
Audio-TDM/I2S interfaces	0
SGBT availability	No
MCDS availability	Limited MCDS
DAPE availability	No
(table continues...)	

Table 4 (continued) TC49xN_AB step (part 2)

SAK-TC497PQ-20M0400MS	
CSI2 Interface	0
Radar cluster(SPU, RIF)available / SPU instances / RIF Instance	No/0/0

2.2.3 TC49xN_AB step (part 3)

A continuation table listing the TC49xN AB step variants.

Table 5 TC49xN_AB step (part 3)

SAK-TC499PE-20MF400MS		SAK-TC497PE-20MF400MS	
Step			
AB		AB	
Production Status			
Emulation device		Emulation device	
Package Type			
PG-F2BGA-436		PG-F2BGA-292	
Pinout			
BGA436_STD 0.8mm		BGA292_STD 0.8mm	
Reference Silicon			
TC49x		TC49x	
Temperature Range (Ambient)			
SAK		SAK	
Chip ID			
0x666C5523		0x65EC5523	
Cores / Checker Cores			
5/5		5/5	
Max. Freq. (MHz)			
400		400	
NVM Type			
eFlash		eFlash	
Program NVM (MB)			
20		20	
Data NVM0 (KB)			
1024		1024	

(table continues...)

Table 5 (continued) TC49xN_AB step (part 3)

SAK-TC499PE-20MF400MS	SAK-TC497PE-20MF400MS
Total SRAM (without Cache) (KB)	
6560	6560
Extension memory(KB)	
3072	3072
DSPR (KB)	
240 in CPU0,1,2 and CSRM; 112 in others	240 in CPU0,1,2 and CSRM; 112 in others
DLMU (KB)	
512 in CPU 0,1 2; 128 in CPU3,4; 0 in CSRM	512 in CPU 0,1 2; 128 in CPU3,4; 0 in CSRM
PSPR (KB)	
64 per CPU	64 per CPU
Hypervisor Support	
Yes	Yes
CSRM Available	
1	1
CSS Availability	
Yes	Yes
PPU Availability	
1	1
ADC - TMADC (Instances / Cores)	
7/14	7/14
ADC - Fast Compare Converters	
10	10
ADC - DS Converters	
10	10
DSEXMOD	
8	8
CDSP Cores	
12	12
HRPWM Instances	
3	3
GTM Classic / eGTM availability	
Yes / Yes	Yes / Yes

(table continues...)

Table 5 (continued) TC49xN_AB step (part 3)

SAK-TC499PE-20MF400MS	SAK-TC497PE-20MF400MS
Gigabit Ethernet (GETH) Instances (Gbps)	
0	0
Light Ethernet (LETH) Instances (Mbps)	
$3 \times (10/100) + 1 \times (10/100/1000)$	$3 \times (10/100) + 1 \times (10/100/1000)$
PCIe Instances	
0	0
CAN (Modules/Nodes)	
4/4x4	4/4x4
CANXL(Modules/Nodes)	
1/2	1/2
FlexRay (Modules/Channels)	
1/1x2	1/1x2
HSSL Modules	
2	2
ASCLIN Modules	
8	8
QSPI Modules	
8	8
I2C Interfaces	
2	2
xSPI Module	
1	1
SENT Channels	
30	30
MSC Modules	
3	2
PSI5 Channels	
4	4
PSI5-S Module	
2	2
SDMMC Module	
Yes	Yes

(table continues...)

Table 5 (continued) TC49xN_AB step (part 3)

	SAK-TC499PE-20MF400MS	SAK-TC497PE-20MF400MS
Audio-TDM/I2S interfaces		
	0	0
SGBT availability		
	Yes	Yes
MCDS availability		
	MCDS 4P, MCDS 2P	MCDS 4P, MCDS 2P
DAPE availability		
	Yes	Yes
CSI2 Interface		
	0	0
Radar cluster(SPU, RIF)available / SPU instances / RIF Instance		
	No/0/0	No/0/0

3 Pin definition and functions

Note: Functions listed in the largest package of this device might not be available for smaller packages because of pin limitations.

Note: *To fulfill the specified RMII timing requirements, it is necessary to select the correct alternate output function signal (e.g. LETH0_P2_RMIB_TXEN) and the registered output signals of this (e.g. LETH0_P2_RMIIRB_TXEN) by writing the corresponding PCSR bitfield inside the PCSRSEL register of the pin slice.

3.1 Logic symbols for package variants

The following figures show the logic symbols for the package variants.

- BGA-436 STD, see [Figure 2](#)
- BGA-292 STD, see [Figure 3](#)

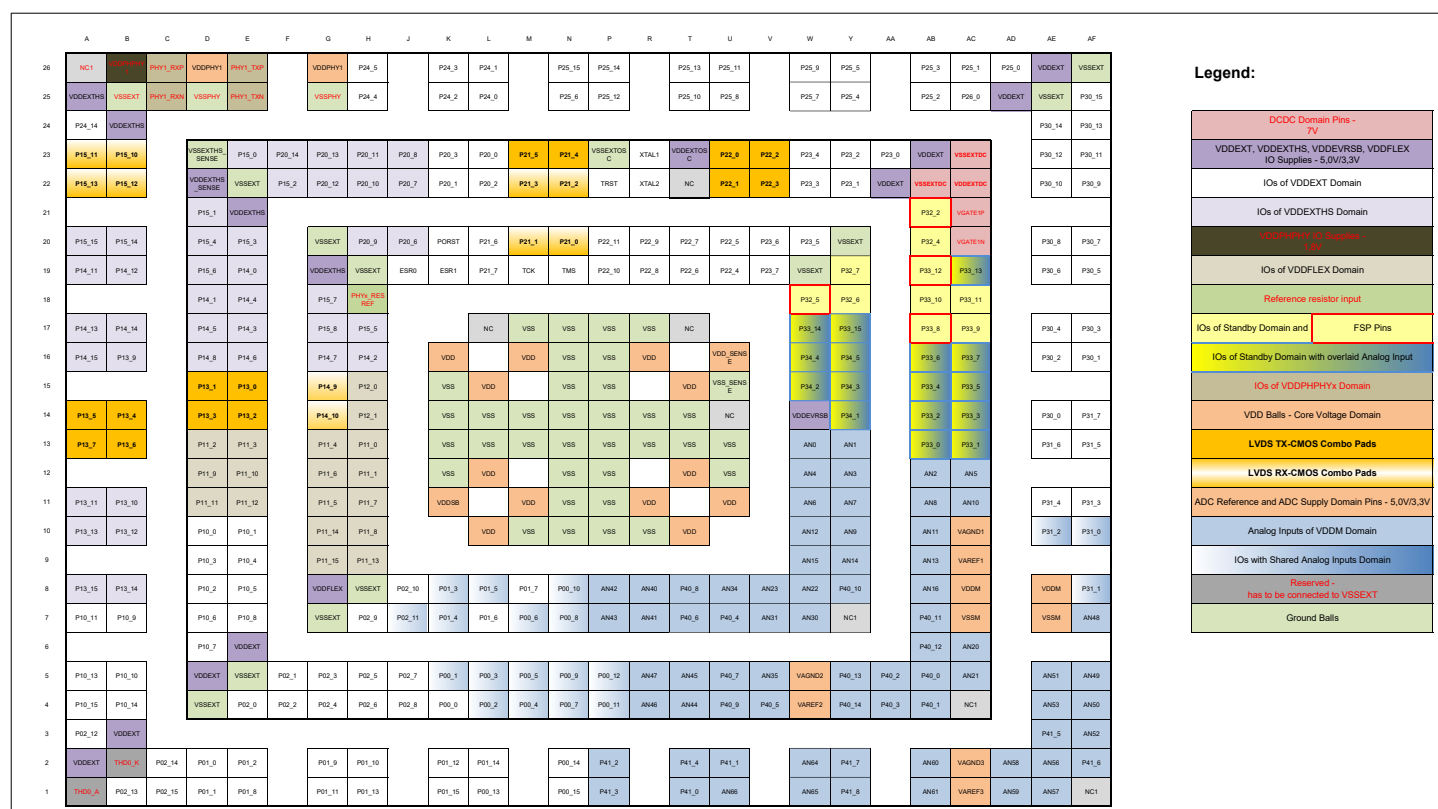


Figure 2 Logic symbol for the package variant BGA-436 STD

3 Pin definition and functions

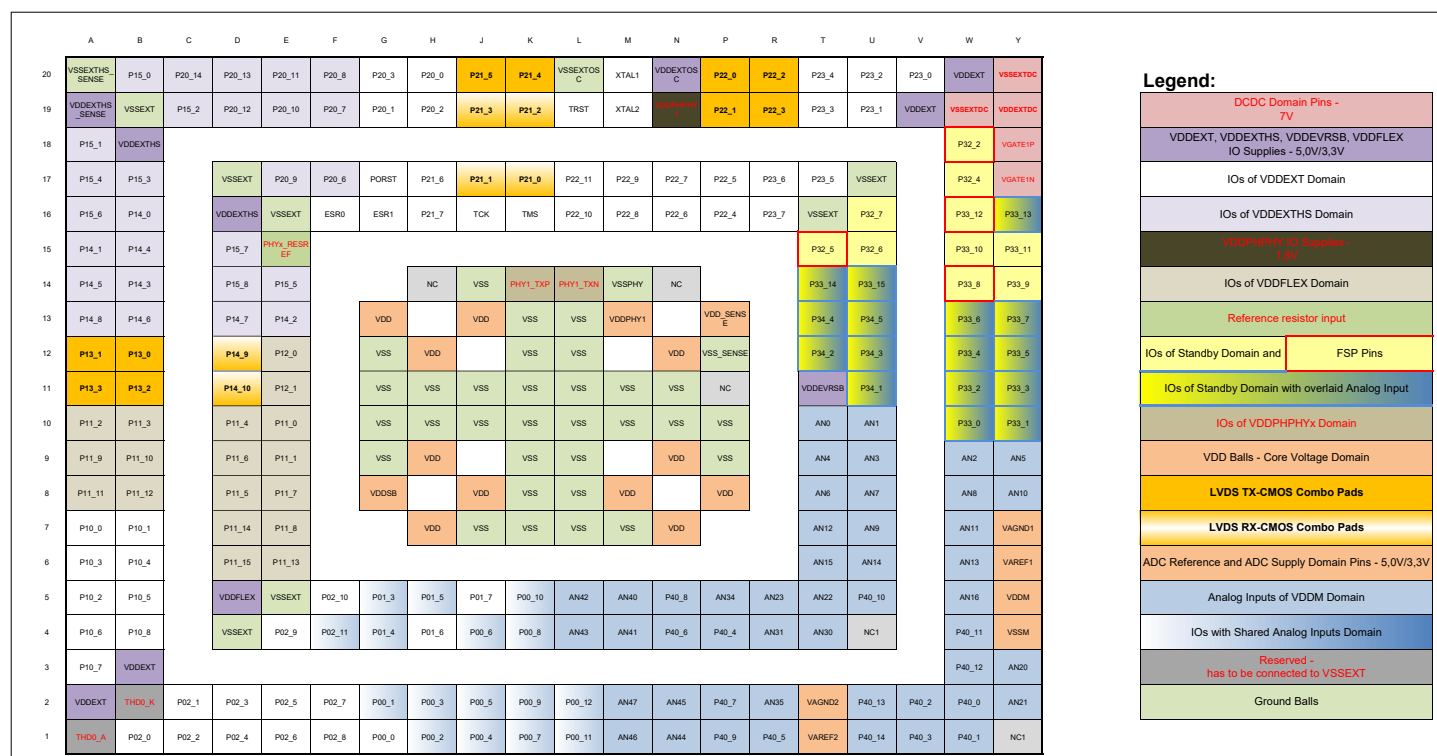


Figure 3 Logic symbol for the package variant BGA-292 STD

Related information

[BGA436_STD package variant pin configuration](#) on page 28

[BGA292_STD package variant pin configuration](#) on page 258

[Pad Sequence](#) on page 422

[Legend](#) on page 444

3.2 BGA436_STD package variant pin configuration

Related information

[Logic symbols for package variants](#) on page 27

[BGA292_STD package variant pin configuration](#) on page 258

[Pad Sequence](#) on page 422

[Legend](#) on page 444

3.2.1 BGA436_STD port 00

Table 6 Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
K4	P00.0	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN4_10			Mux input channel 4 of TIM module 0
	GTM_TIM2_IN0_1			Mux input channel 0 of TIM module 2

(table continues...)

Table 6 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TIM3_IN0_1			Mux input channel 0 of TIM module 3
	GTM_TIM5_IN4_9			Mux input channel 4 of TIM module 5
	MSC0_INJ0			Injection signal from port
	GPT121_CAPINA			Trigger input to capture value of timer T5 into CAPREL register (input A)
	GTM_CDTM1_DTM0_5			Input mux of CDTM1_DTM0_AUXIN0/1
	GTM_CDTM1_DTM4_5			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM0_5			Input mux of CDTM1_DTM0_AUXIN0/1
	EGTM_CDTM1_DTM4_5			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_TIM0_IN4_10			Mux input channel 4 of TIM module 0
	EGTM_TIM2_IN0_1			Mux input channel 0 of TIM module 2
	P00.0	O0		General-purpose output
	GTM_TOUT9	O1		GTM muxed output
	ASCLIN3_ASCLK	O2		Shift clock output
	ASCLIN3_ATX	O3		Transmit output
	—	O4		Reserved
	CAN10_TXD	O5		CAN transmit output node 0
	PSI5_TX0	O6		TXD outputs (send data)
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT9	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
K5	P00.1	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN4_11			Mux input channel 4 of TIM module 0
	GTM_TIM1_IN2_11			Mux input channel 2 of TIM module 1
	GTM_TIM2_IN1_1			Mux input channel 1 of TIM module 2
	GTM_TIM3_IN1_1			Mux input channel 1 of TIM module 3
	GTM_TIM5_IN5_11			Mux input channel 5 of TIM module 5

(table continues...)

Table 6 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN3_ARXE			Receive input
	CAN10_RXDA			CAN receive input node 0
	PSI5_RX0A			RXD inputs (receive data) channel 0
	GPT121_T2INA			Trigger/gate input of timer T2
	GTM_CDTM1_DTM1_5			Input mux of CDTM1_DTM1_AUXIN0/1
	SENT0_SENT0B			Receive input channel 0
	EGTM_CDTM1_DTM1_5			Input mux of CDTM1_DTM1_AUXIN0/1
	GTM_CDTM3_DTM1_1			Input mux of CDTM3_DTM1_AUXIN0/1
	EGTM_TIM0_IN4_11			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN2_11			Mux input channel 2 of TIM module 1
	EGTM_TIM2_IN1_1			Mux input channel 1 of TIM module 2
	ADC_TMADC2CH11	AI		Analog Input for TMADC2 Channel 11
	ADC_DSADC5NA			Analog Input for DSADC5 Negative Input A
	P00.1	O0		General-purpose output
	GTM_TOUT10	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	SENT0_SPC0	O3		Transmit output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT10	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
L4	P00.2	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	GTM_TIM2_IN1_2			Mux input channel 1 of TIM module 2
	GTM_TIM3_IN1_2			Mux input channel 1 of TIM module 3
	GTM_TIM5_IN6_11			Mux input channel 6 of TIM module 5

(table continues...)

Table 6 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	I2C0_SCLG			Serial Clock Input 6
	SENT1_SENT0B			Receive input channel 0
	GPT121_T2EUDA			Count direction control input of timer T2
	EGTM_CDTM1_DTM2_5			Input mux of CDTM1_DTM2_AUXIN0/1
	EGTM_CDTM1_DTM3_5			Input mux of CDTM1_DTM3_AUXIN0/1
	EGTM_TIM2_IN1_2			Mux input channel 1 of TIM module 2
	ADC_TMADC2CH10	AI		Analog Input for TMADC2 Channel 10
	ADC_DSADC5PA			Analog Input for DSADC5 Positive Input A
	ADC_FCC5			Analog Input for FCC5
	P00.2	O0		General-purpose output
	GTM_TOUT11	O1		GTM muxed output
	ASCLIN3_ASCLK	O2		Shift clock output
	CAN21_TXD	O3		CAN transmit output node 1
	PSI5_TX0	O4		TXD outputs (send data)
	CAN03_TXD	O5		CAN transmit output node 3
	QSPI3_SLSO4	O6		Master slave select output
	I2C0_SCL	O7		Serial Clock Output
	—	O8		Reserved
	EGTM_TOUT11	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
L5	P00.3	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	GTM_TIM1_IN3_11			Mux input channel 3 of TIM module 1
	GTM_TIM2_IN2_1			Mux input channel 2 of TIM module 2
	GTM_TIM3_IN2_1			Mux input channel 2 of TIM module 3
	GTM_TIM5_IN7_10			Mux input channel 7 of TIM module 5
	GPT121_T4EUDA			Count direction control input of timer T4
	I2C0_SDAG			Serial Data Input 6
	PSI5_RX1A			RXD inputs (receive data) channel 1

(table continues...)

Table 6 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CAN03_RXDA			CAN receive input node 3
	CAN21_RXDA			CAN receive input node 1
	PSI5S0_RXA			RX data input
	SENT0_SENT1B			Receive input channel 1
	GTM_CDTM1_DTM5_5			Input mux of CDTM1_DTM5_AUXIN0/1
	EGTM_CDTM1_DTM5_5			Input mux of CDTM1_DTM5_AUXIN0/1
	EGTM_TIM1_IN3_11			Mux input channel 3 of TIM module 1
	EGTM_TIM2_IN2_1			Mux input channel 2 of TIM module 2
	ADC_TMADC2CH9	AI		Analog Input for TMADC2 Channel 9
	ADC_DSADC5NB			Analog Input for DSADC5 Negative Input B
	P00.3	O0		General-purpose output
	GTM_TOUT12	O1		GTM muxed output
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	SENT0_SPC1	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	I2C0_SDA	O7		Serial Data Output
	—	O8		Reserved
	EGTM_TOUT12	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
M4	P00.4	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	GTM_TIM2_IN3_1			Mux input channel 3 of TIM module 2
	GTM_TIM3_IN3_1			Mux input channel 3 of TIM module 3
	GTM_TIM6_IN4_1			Mux input channel 4 of TIM module 6
	SCU_E_REQ2C			ERU channel 2 input C
	SENT1_SENT1B			Receive input channel 1
	GPT121_T5INA			Trigger/gate input of timer T5

(table continues...)

Table 6 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_CDTM3_DTM0_1			Input mux of CDTM3_DTM0_AUXIN0/1
	GTM_CDTM5_DTM4_1			Input mux of CDTM5_DTM4_AUXIN0/1
	EGTM_TIM2_IN3_1			Mux input channel 3 of TIM module 2
	ADC_TMADC2CH8	AI		Analog Input for TMADC2 Channel 8
	ADC_DSADC5PB			Analog Input for DSADC5 Positive Input B
	P00.4	O0		General-purpose output
	GTM_TOUT13	O1		GTM muxed output
	PSI5S0_TX	O2		TX data output
	CAN11_TXD	O3		CAN transmit output node 1
	PSI5_TX1	O4		TXD outputs (send data)
	—	O5		Reserved
	SENT1_SPC1	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT13	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
M5	P00.5	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	GTM_TIM0_IN6_11			Mux input channel 6 of TIM module 0
	GTM_TIM1_IN6_10			Mux input channel 6 of TIM module 1
	GTM_TIM2_IN4_1			Mux input channel 4 of TIM module 2
	GTM_TIM3_IN0_11			Mux input channel 0 of TIM module 3
	GTM_TIM3_IN4_1			Mux input channel 4 of TIM module 3
	PSI5_RX2A			RXD inputs (receive data) channel 2
	SENT0_SENT2B			Receive input channel 2
	GPT121_T5EUDA			Count direction control input of timer T5
	CAN11_RXDB			CAN receive input node 1
	GTM_CDTM1_DTM0_2			Input mux of CDTM1_DTM0_AUXIN0/1
	GTM_CDTM1_DTM1_2			Input mux of CDTM1_DTM1_AUXIN0/1

(table continues...)

Table 6 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_CDTM4_DTM0_3			Input mux of CDTM4_DTM0_AUXIN0/1
	GTM_CDTM4_DTM1_3			Input mux of CDTM4_DTM1_AUXIN0/1
	EGTM_CDTM1_DTM0_2			Input mux of CDTM1_DTM0_AUXIN0/1
	EGTM_CDTM1_DTM1_2			Input mux of CDTM1_DTM1_AUXIN0/1
	EGTM_CDTM1_DTM2_2			Input mux of CDTM1_DTM2_AUXIN0/1
	EGTM_TIM0_IN6_11			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN6_10			Mux input channel 6 of TIM module 1
	EGTM_TIM2_IN4_1			Mux input channel 4 of TIM module 2
	ADC_TMADC2CH7	AI		Analog Input for TMADC2 Channel 7
	P00.5	O0		General-purpose output
	GTM_TOUT14	O1		GTM muxed output
	ADC_PWM1	O2		Negative PWM
	QSPI3_SLSO3	O3		Master slave select output
	—	O4		Reserved
	ADC_BFL0	O5		Boundary flags from FCC
	SENT0_SPC2	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT14	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
M7	P00.6	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	GTM_TIM2_IN5_1			Mux input channel 5 of TIM module 2
	GTM_TIM3_IN1_13			Mux input channel 1 of TIM module 3
	GTM_TIM3_IN5_1			Mux input channel 5 of TIM module 3
	SENT1_SENT2B			Receive input channel 2
	ASCLIN5_ARXA			Receive input
	GPT121_T6EUDA			Count direction control input of core timer T6
	GTM_CDTM3_DTM0_2			Input mux of CDTM3_DTM0_AUXIN0/1

(table continues...)

Table 6 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_CDTM5_DTM5_1			Input mux of CDTM5_DTM5_AUXIN0/1
	EGTM_TIM2_IN5_1			Mux input channel 5 of TIM module 2
	ADC_TMADC2CH6	AI		Analog Input for TMADC2 Channel 6
	P00.6	O0		General-purpose output
	GTM_TOUT15	O1		GTM muxed output
	ADC_PWM0	O2		Positive PWM
	—	O3		Reserved
	PSI5_TX2	O4		TXD outputs (send data)
	ADC_EMUXCTRL10	O5		EMUX1 Control from TMADC to PORTS
	SENT1_SPC2	O6		Transmit output
	GPT121_T3OUT	O7		External output for overflow/underflow detection of core timer T3
	—	O8		Reserved
	EGTM_TOUT15	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
N4	P00.7	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	GTM_TIM1_IN6_11			Mux input channel 6 of TIM module 1
	GTM_TIM2_IN6_1			Mux input channel 6 of TIM module 2
	GTM_TIM3_IN2_11			Mux input channel 2 of TIM module 3
	GTM_TIM3_IN6_1			Mux input channel 6 of TIM module 3
	SENT0_SENT3B			Receive input channel 3
	GPT120_T2INA			Trigger/gate input of timer T2
	GPT121_T6INA			Trigger/gate input of core timer T6
	GTM_CDTM0_DTM0_3			Input mux of CDTM0_DTM0_AUXIN0/1
	GTM_CDTM0_DTM1_3			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM0_DTM0_3			Input mux of CDTM0_DTM0_AUXIN0/1
	EGTM_CDTM0_DTM1_3			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM0_DTM2_3			Input mux of CDTM0_DTM2_AUXIN0/1

(table continues...)

Table 6 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_CDTM0_DTM3_3			Input mux of CDTM0_DTM3_AUXIN0/1
	EGTM_TIM1_IN6_11			Mux input channel 6 of TIM module 1
	EGTM_TIM2_IN6_1			Mux input channel 6 of TIM module 2
	ADC_TMADC2CH5	AI		Analog Input for TMADC2 Channel 5
	ADC_DSADC4NA			Analog Input for DSADC4 Negative Input A
	P00.7	O0		General-purpose output
	GTM_TOUT16	O1		GTM muxed output
	ASCLIN5_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	ADC_EMUXCTRL11	O5		EMUX1 Control from TMADC to PORTS
	SENT0_SPC3	O6		Transmit output
	PSI5S1_TX	O7		TX data output
	—	O8		Reserved
	EGTM_TOUT16	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
N7	P00.8	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	GTM_TIM0_IN7_10			Mux input channel 7 of TIM module 0
	GTM_TIM1_IN7_10			Mux input channel 7 of TIM module 1
	GTM_TIM2_IN7_1			Mux input channel 7 of TIM module 2
	GTM_TIM3_IN3_11			Mux input channel 3 of TIM module 3
	GTM_TIM3_IN7_1			Mux input channel 7 of TIM module 3
	SENT1_SENT3B			Receive input channel 3
	GPT120_T2EUDA			Count direction control input of timer T2
	PSI5S1_RXB			RX data input
	GTM_CDTM6_DTM5_1			Input mux of CDTM6_DTM5_AUXIN0/1
	EGTM_CDTM1_DTM3_2			Input mux of CDTM1_DTM3_AUXIN0/1
	EGTM_TIM0_IN7_10			Mux input channel 7 of TIM module 0

(table continues...)

Table 6 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM1_IN7_10	AI		Mux input channel 7 of TIM module 1
	EGTM_TIM2_IN7_1			Mux input channel 7 of TIM module 2
	ADC_TMADC2CH4			Analog Input for TMADC2 Channel 4
	ADC_DSADC4PA			Analog Input for DSADC4 Positive Input A
	ADC_FCC4			Analog Input for FCC4
	P00.8	O0		General-purpose output
	GTM_TOUT17	O1		GTM muxed output
	QSPI3_SLSO6	O2		Master slave select output
	—	O3		Reserved
	—	O4		Reserved
	ADC_EMUXCTRL12	O5		EMUX1 Control from TMADC to PORTS
	SENT1_SPC3	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT17	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
N5	P00.9	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	GTM_TIM0_IN0_1			Mux input channel 0 of TIM module 0
	GTM_TIM1_IN0_1			Mux input channel 0 of TIM module 1
	GTM_TIM1_IN7_11			Mux input channel 7 of TIM module 1
	GTM_TIM4_IN0_7			Mux input channel 0 of TIM module 4
	SENT0_SENT4B			Receive input channel 4
	GPT120_T4EUDA			Count direction control input of timer T4
	GTM_CDTM3_DTM1_2			Input mux of CDTM3_DTM1_AUXIN0/1
	GTM_CDTM6_DTM4_1			Input mux of CDTM6_DTM4_AUXIN0/1
	ASCLIN4_ARXG			Receive input
	EGTM_TIM0_IN0_1			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_1			Mux input channel 0 of TIM module 1

(table continues...)

Table 6 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM1_IN7_11			Mux input channel 7 of TIM module 1
	ADC_TMADC2CH3	AI		Analog Input for TMADC2 Channel 3
	ADC_DSADC4NB			Analog Input for DSADC4 Negative Input B
	P00.9	O0		General-purpose output
	GTM_TOUT18	O1		GTM muxed output
	QSPI3_SLS07	O2		Master slave select output
	ASCLIN3_ARTS	O3		Ready to send output
	ADC_EMUXCTRL13	O4		EMUX1 Control from TMADC to PORTS
	ASCLIN4_ATX	O5		Transmit output
	SENT0_SPC4	O6		Transmit output
	GPT121_T6OUT	O7		External output for overflow/underflow detection of core timer T6
	—	O8		Reserved
	EGTM_TOUT18	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
N8	P00.10	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	GTM_TIM0_IN1_1			Mux input channel 1 of TIM module 0
	GTM_TIM1_IN1_1			Mux input channel 1 of TIM module 1
	GTM_TIM4_IN1_11			Mux input channel 1 of TIM module 4
	SENT1_SENT4B			Receive input channel 4
	GPT121_T3EUDA			Count direction control input of core timer T3
	GTM_CDTM0_DTM1_5			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM0_DTM1_5			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_TIM0_IN1_1			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_1			Mux input channel 1 of TIM module 1
	ADC_TMADC2CH2	AI		Analog Input for TMADC2 Channel 2
	ADC_DSADC4PB			Analog Input for DSADC4 Positive Input B
	P00.10	O0		General-purpose output

(table continues...)

Table 6 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TOUT19	O1		GTM muxed output
	ASCLIN4_ASCLK	O2		Shift clock output
	—	O3		Reserved
	ASCLIN4_ATX	O4		Transmit output
	—	O5		Reserved
	SENT1_SPC4	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT19	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
P4	P00.11	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	GTM_TIM0_IN2_1			Mux input channel 2 of TIM module 0
	GTM_TIM1_IN2_1			Mux input channel 2 of TIM module 1
	GTM_TIM4_IN2_11			Mux input channel 2 of TIM module 4
	SENT0_SENT5B			Receive input channel 5
	GPT121_T3INA			Trigger/gate input of core timer T3 (input A, B and C)
	GTM_CDTM0_DTM0_5			Input mux of CDTM0_DTM0_AUXIN0/1
	GTM_CDTM0_DTM4_5			Input mux of CDTM0_DTM4_AUXIN0/1
	GTM_CDTM0_DTM5_5			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_CDTM0_DTM0_5			Input mux of CDTM0_DTM0_AUXIN0/1
	EGTM_CDTM0_DTM4_5			Input mux of CDTM0_DTM4_AUXIN0/1
	EGTM_CDTM0_DTM5_5			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_TIM0_IN2_1			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_1			Mux input channel 2 of TIM module 1
	ADC_TMADC2CH1	AI		Analog Input for TMADC2 Channel 1
	P00.11	O0		General-purpose output
	GTM_TOUT20	O1		GTM muxed output
	ASCLIN4_ASLSO	O2		Slave select signal output

(table continues...)

Table 6 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O3		Reserved
	ADC_CLKOUT0	O4		Clock output from EXMOD
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT20	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
P5	P00.12	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	GTM_TIM0_IN3_1			Mux input channel 3 of TIM module 0
	GTM_TIM1_IN3_1			Mux input channel 3 of TIM module 1
	GTM_TIM4_IN3_11			Mux input channel 3 of TIM module 4
	ASCLIN3_ACTSA			Clear to send input
	ASCLIN4_ARXA			Receive input
	SENT1_SENT5B			Receive input channel 5
	GPT121_T4INA			Trigger/gate input of timer T4
	EGTM_CDTM0_DTM2_5			Input mux of CDTM0_DTM2_AUXIN0/1
	EGTM_CDTM0_DTM3_5			Input mux of CDTM0_DTM3_AUXIN0/1
	EGTM_TIM0_IN3_1			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_1			Mux input channel 3 of TIM module 1
	ADC_TMADC2CH0	AI		Analog Input for TMADC2 Channel 0
	P00.12	O0		General-purpose output
	GTM_TOUT21	O1		GTM muxed output
	ADC_EMUXCTRL30	O2		EMUX3 Control from TMADC to PORTS
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved

(table continues...)

Table 6 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT21	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
L1	P00.13	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN0_1			Mux input channel 0 of TIM module 4
	GTM_TIM5_IN0_1			Mux input channel 0 of TIM module 5
	GTM_TIM6_IN5_2			Mux input channel 5 of TIM module 6
	P00.13	O0		General-purpose output
	GTM_TOUT167	O1		GTM muxed output
	ADC_EMUXCTRL31	O2		EMUX3 Control from TMADC to PORTS
	—	O3		Reserved
	CLOCK_EXTCLK1	O4		External clock output 1
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT167	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
N2	P00.14	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN7_1			Mux input channel 7 of TIM module 4
	GTM_TIM5_IN7_1			Mux input channel 7 of TIM module 5
	GTM_TIM6_IN6_2			Mux input channel 6 of TIM module 6

(table continues...)

Table 6 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	P00.14	O0		General-purpose output
	GTM_TOUT166	O1		GTM muxed output
	ADC_EMUXCTRL32	O2		EMUX3 Control from TMADC to PORTS
	—	O3		Reserved
	ASCLIN6_ATX	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT166	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
N1	P00.15	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN1_1			Mux input channel 1 of TIM module 4
	GTM_TIM5_IN1_1			Mux input channel 1 of TIM module 5
	GTM_TIM6_IN7_2			Mux input channel 7 of TIM module 6
	P00.15	O0		General-purpose output
	GTM_TOUT168	O1		GTM muxed output
	ADC_EMUXCTRL33	O2		EMUX3 Control from TMADC to PORTS
	—	O3		Reserved
	CLOCK_EXTCLK0	O4		External clock output 0
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT168	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved

(table continues...)

Table 6 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

3.2.2 BGA436_STD port 01

Table 7 Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
D2	P01.0	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM2_IN6_13			Mux input channel 6 of TIM module 2
	GTM_TIM4_IN4_1			Mux input channel 4 of TIM module 4
	GTM_TIM5_IN4_1			Mux input channel 4 of TIM module 5
	CAN21_RXDE			CAN receive input node 1
	CAN03_RXDF			CAN receive input node 3
	ASCLIN6_ARXB			Receive input
	EGTM_TIM2_IN6_13			Mux input channel 6 of TIM module 2
	P01.0	O0		General-purpose output
	GTM_TOUT155	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	LETH0_P2_TXD	O7		LETH PortX TC14 interface transmit data output
	—	O8		Reserved
	EGTM_TOUT155	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 7 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
D1	P01.1	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN1_2			Mux input channel 1 of TIM module 4
	GTM_TIM5_IN1_2			Mux input channel 1 of TIM module 5
	SENT0_SENT3C			Receive input channel 3
	LETH0_P2_RXDA			LETH PortX TC14 interface receive data input
	P01.1	O0		General-purpose output
	GTM_TOUT159	O1		GTM muxed output
	ADC_EMUXCTRL20	O2		EMUX2 Control from TMADC to PORTS
	—	O3		Reserved
	ASCLIN6_ATX	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT159	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
E2	P01.2	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN5_1			Mux input channel 5 of TIM module 4
	GTM_TIM5_IN5_1			Mux input channel 5 of TIM module 5
	LETH0_P2_EDE			LETH PortX TC14 interface energy detection input
	LETH0_P2_MDIOE			LETH PortX MDIO interface data input
	P01.2	O0		General-purpose output
	GTM_TOUT156	O1		GTM muxed output
	CAN32_TXD	O2		CAN transmit output node 2
	CAN03_TXD	O3		CAN transmit output node 3
	—	O4		Reserved

(table continues...)

Table 7 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CAN21_TXD	O5		CAN transmit output node 1
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT156	O9		eGTM muxed output
	LETH0_P2_PPS	O10		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
K8	P01.3	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN5_8			Mux input channel 5 of TIM module 0
	GTM_TIM2_IN0_11			Mux input channel 0 of TIM module 2
	GTM_TIM4_IN5_2			Mux input channel 5 of TIM module 4
	QSPI3_SLSIB			Slave select input
	SENT1_SENT12A			Receive input channel 12
	CAN32_RXDA			CAN receive input node 2
	LETH0_P0_MDIOB			LETH PortX MDIO interface data input
	LETH0_P0_EDB			LETH PortX TC14 interface energy detection input
	EGTM_TIM0_IN5_8			Mux input channel 5 of TIM module 0
	EGTM_TIM2_IN0_11			Mux input channel 0 of TIM module 2
	ADC_TMADC2CH14	AI		Analog Input for TMADC2 Channel 14
	P01.3	O0		General-purpose output
	GTM_TOUT111	O1		GTM muxed output
	CAN31_TXD	O2		CAN transmit output node 1
	ADC_CLKOUT7	O3		Clock output from EXMOD
	QSPI3_SLSO9	O4		Master slave select output
	CAN01_TXD	O5		CAN transmit output node 1
	—	O6		Reserved

(table continues...)

Table 7 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SENT1_SPC12	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT111	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
K7	P01.4	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN6_8			Mux input channel 6 of TIM module 0
	GTM_TIM2_IN1_10			Mux input channel 1 of TIM module 2
	GTM_TIM4_IN6_2			Mux input channel 6 of TIM module 4
	CAN01_RXDC			CAN receive input node 1
	SENT0_SENT13A			Receive input channel 13
	EGTM_TIM0_IN6_8			Mux input channel 6 of TIM module 0
	EGTM_TIM2_IN1_10			Mux input channel 1 of TIM module 2
	ADC_TMADC2CH13	AI		Analog Input for TMADC2 Channel 13
	P01.4	O0		General-purpose output
	GTM_TOUT112	O1		GTM muxed output
	ADC_EMUXCTRL21	O2		EMUX2 Control from TMADC to PORTS
	—	O3		Reserved
	QSPI3_SLSO10	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	LETH0_P0_TXD	O7		LETH PortX TC14 interface transmit data output
	CANXL00_TXD	O8		CANXL transmit output node 0
	EGTM_TOUT112	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved

(table continues...)

Table 7 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
L8	P01.5	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM2_IN2_7			Mux input channel 2 of TIM module 2
	GTM_TIM2_IN3_7			Mux input channel 3 of TIM module 2
	GTM_TIM5_IN3_2			Mux input channel 3 of TIM module 5
	QSPI3_MRSTC			Master SPI data input
	SENT1_SENT13A			Receive input channel 13
	CANXL00_RXDG			CANXL receive input node 0
	EGTM_TIM2_IN2_7			Mux input channel 2 of TIM module 2
	EGTM_TIM2_IN3_7			Mux input channel 3 of TIM module 2
	LETH0_P0_RXDG			LETH PortX TC14 interface receive data input
	ADC_TMADC2CH12	AI		Analog Input for TMADC2 Channel 12
	P01.5	O0		General-purpose output
	GTM_TOUT113	O1		GTM muxed output
	ADC_EMUXCTRL22	O2		EMUX2 Control from TMADC to PORTS
	—	O3		Reserved
	QSPI3_MRST	O4		Slave SPI data output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT113	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface

(table continues...)

Table 7 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
L7	P01.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM2_IN5_7			Mux input channel 5 of TIM module 2
	GTM_TIM5_IN5_3			Mux input channel 5 of TIM module 5
	GTM_TIM5_IN6_2			Mux input channel 6 of TIM module 5
	QSPI3_MTSRC			Slave SPI data input
	CAN32_RXDD			CAN receive input node 2
	EGTM_TIM2_IN5_7			Mux input channel 5 of TIM module 2
	P01.6	O0		General-purpose output
	GTM_TOUT114	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	QSPI3_MTSR	O4		Master SPI data output
	—	O5		Reserved
	ADC_CLKOUT6	O6		Clock output from EXMOD
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT114	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
M8	P01.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM2_IN7_7			Mux input channel 7 of TIM module 2
	GTM_TIM5_IN7_2			Mux input channel 7 of TIM module 5
	QSPI3_SCLKC			Slave SPI clock inputs
	EGTM_TIM2_IN7_7			Mux input channel 7 of TIM module 2
	P01.7	O0		General-purpose output
	GTM_TOUT115	O1		GTM muxed output
	ADC_EMUXCTRL23	O2		EMUX2 Control from TMADC to PORTS
	—	O3		Reserved
	QSPI3_SCLK	O4		Master SPI clock output

(table continues...)

Table 7 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT115	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
E1	P01.8	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN4_2			Mux input channel 4 of TIM module 4
	GTM_TIM5_IN0_10			Mux input channel 0 of TIM module 5
	GTM_TIM5_IN4_2			Mux input channel 4 of TIM module 5
	CAN00_RXDF			CAN receive input node 0
	SENT0_SENT4C			Receive input channel 4
	ASCLIN0_ARXC			Receive input
	CAN20_RXDE			CAN receive input node 0
	ASCLIN7_ARXB			Receive input
	P01.8	O0		General-purpose output
	GTM_TOUT162	O1		GTM muxed output
	SENT0_SPC4	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	ADC_BFL4	O7		Boundary flags from FCC
	—	O8		Reserved
	EGTM_TOUT162	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved

(table continues...)

Table 7 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
G2	P01.9	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN2_1			Mux input channel 2 of TIM module 4
	GTM_TIM5_IN1_11			Mux input channel 1 of TIM module 5
	GTM_TIM5_IN2_1			Mux input channel 2 of TIM module 5
	SENT1_SENT3C			Receive input channel 3
	LETH0_P2_MII_RXERD			LETH0 PortX MII receive error (to be used with LETH0_P2_RXCLKD)
	P01.9	O0		General-purpose output
	GTM_TOUT160	O1		GTM muxed output
	ASCLIN7_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	ADC_BFL5	O7		Boundary flags from FCC
	—	O8		Reserved
	EGTM_TOUT160	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
H2	P01.10	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN5_3			Mux input channel 5 of TIM module 4
	GTM_TIM5_IN2_9			Mux input channel 2 of TIM module 5
	GTM_TIM5_IN5_2			Mux input channel 5 of TIM module 5
	SENT1_SENT4C			Receive input channel 4
	GTM_CDTM3_DTM0_3			Input mux of CDTM3_DTM0_AUXIN0/1
	GTM_CDTM3_DTM1_3			Input mux of CDTM3_DTM1_AUXIN0/1

(table continues...)

Table 7 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_CDTM4_DTM0_1			Input mux of CDTM4_DTM0_AUXIN0/1
	GTM_CDTM4_DTM1_1			Input mux of CDTM4_DTM1_AUXIN0/1
	P01.10	O0		General-purpose output
	GTM_TOUT163	O1		GTM muxed output
	ASCLIN7_ASCLK	O2		Shift clock output
	SENT1_SPC4	O3		Transmit output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	ADC_BFL6	O7		Boundary flags from FCC
	—	O8		Reserved
	EGTM_TOUT163	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
G1	P01.11	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN7_2			Mux input channel 7 of TIM module 4
	GTM_TIM5_IN3_11			Mux input channel 3 of TIM module 5
	GTM_TIM5_IN7_3			Mux input channel 7 of TIM module 5
	SENT1_SENT6C			Receive input channel 6
	GTM_CDTM4_DTM0_2			Input mux of CDTM4_DTM0_AUXIN0/1
	GTM_CDTM4_DTM1_2			Input mux of CDTM4_DTM1_AUXIN0/1
	GTM_CDTM5_DTM4_2			Input mux of CDTM5_DTM4_AUXIN0/1
	GTM_CDTM5_DTM5_2			Input mux of CDTM5_DTM5_AUXIN0/1
	GTM_CDTM6_DTM4_2			Input mux of CDTM6_DTM4_AUXIN0/1
	GTM_CDTM6_DTM5_2			Input mux of CDTM6_DTM5_AUXIN0/1
	LETH0_P2_COLB			LETH PortX MII collision detection
	P01.11	O0		General-purpose output
	GTM_TOUT165	O1		GTM muxed output
	ASCLIN7_ASLSO	O2		Slave select signal output

(table continues...)

Table 7 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SENT1_SPC6	O3		Transmit output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	ADC_BFL7	O7		Boundary flags from FCC
	—	O8		Reserved
	EGTM_TOUT165	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
K2	P01.12	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN0_2			Mux input channel 0 of TIM module 4
	GTM_TIM5_IN0_2			Mux input channel 0 of TIM module 5
	GTM_TIM6_IN0_3			Mux input channel 0 of TIM module 6
	QSPI3_MRSTH			Master SPI data input
	P01.12	O0		General-purpose output
	GTM_TOUT158	O1		GTM muxed output
	ASCLIN7_ATX	O2		Transmit output
	ADC_CLKOUT5	O3		Clock output from EXMOD
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	LETH0_P2_TXD	O7		LETH PortX TC14 interface transmit data output
	—	O8		Reserved
	EGTM_TOUT158	O9		eGTM muxed output
	LETH1_P0_PPS0	O10		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved

(table continues...)

Table 7 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O14		Reserved
	—	O15		Reserved
H1	P01.13	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN3_1			Mux input channel 3 of TIM module 4
	GTM_TIM5_IN3_1			Mux input channel 3 of TIM module 5
	GTM_TIM6_IN1_3			Mux input channel 1 of TIM module 6
	LETH0_P2_COLD			LETH PortX MII collision detection
	P01.13	O0		General-purpose output
	GTM_TOUT161	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	—	O3		Reserved
	CAN00_TXD	O4		CAN transmit output node 0
	CAN20_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT161	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
L2	P01.14	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN6_3			Mux input channel 6 of TIM module 4
	GTM_TIM5_IN6_3			Mux input channel 6 of TIM module 5
	GTM_TIM6_IN2_3			Mux input channel 2 of TIM module 6
	LETH0_P2_EDA			LETH PortX TC14 interface energy detection input
	LETH0_P2_MDIOA			LETH PortX MDIO interface data input
	P01.14	O0		General-purpose output
	GTM_TOUT164	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved

(table continues...)

Table 7 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT164	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
K1	P01.15	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN6_1			Mux input channel 6 of TIM module 4
	GTM_TIM5_IN6_1			Mux input channel 6 of TIM module 5
	GTM_TIM6_IN3_3			Mux input channel 3 of TIM module 6
	P01.15	O0		General-purpose output
	GTM_TOUT157	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT157	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

3.2.3 BGA436_STD port 02

Table 8 Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
E4	P02.0	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN0_2			Mux input channel 0 of TIM module 0
	GTM_TIM1_IN0_2			Mux input channel 0 of TIM module 1
	LETH1_P0_AUX			LETH PortX auxiliary snapshot signal
	ASCLIN2_ARXG			Receive input
	GTM_CDTM0_DTM4_1			Input mux of CDTM0_DTM4_AUXIN0/1
	SCU_E_REQ3C			ERU channel 3 input C
	CAN31_RXDC			CAN receive input node 1
	ADC_TRIG56			Triggers from PORTS to ADC
	GTM_CDTM1_DTM0_6			Input mux of CDTM1_DTM0_AUXIN0/1
	GTM_CDTM3_DTM0_6			Input mux of CDTM3_DTM0_AUXIN0/1
	GTM_CDTM4_DTM0_6			Input mux of CDTM4_DTM0_AUXIN0/1
	GTM_CDTM4_DTM4_6			Input mux of CDTM4_DTM4_AUXIN0/1
	GTM_CDTM4_DTM5_6			Input mux of CDTM4_DTM5_AUXIN0/1
	EGTM_CDTM0_DTM4_1			Input mux of CDTM0_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM0_6			Input mux of CDTM1_DTM0_AUXIN0/1
	EGTM_TIM0_IN0_2			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_2			Mux input channel 0 of TIM module 1
	P02.0	O0		General-purpose output
	GTM_TOUT0	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	QSPI3_SLS01_F	O3		Master slave select output
	ADC_PWM1	O4		Negative PWM
	CAN00_TXD	O5		CAN transmit output node 0
	ERAY0_TXDA	O6		Transmit Channel A
	LETH0_P0_TXD	O7		LETH PortX TC14 interface transmit data output
	CANXL00_TXD	O8		CANXL transmit output node 0
	EGTM_TOUT0_F	O9		eGTM muxed output
	—	O10		Reserved
	QSPI3_SLS05_F	O11		Master slave select output
	—	O12		Reserved
	—	O13		Reserved

(table continues...)

Table 8 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM0_CH0_F	PO		High resolution PWM 0 output channels
F5	P02.1	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN1_2			Mux input channel 1 of TIM module 0
	GTM_TIM1_IN1_2			Mux input channel 1 of TIM module 1
	ERAY0_RXDA2			Receive Channel A2
	ASCLIN2_ARXB			Receive input
	CAN00_RXDA			CAN receive input node 0
	SCU_E_REQ2B			ERU channel 2 input B
	SENT0_SENT14A			Receive input channel 14
	ADC_TRIG57			Triggers from PORTS to ADC
	ADC_CLKIN4			Clock input to EXMOD
	GTM_CDTM0_DTM1_6			Input mux of CDTM0_DTM1_AUXIN0/1
	GTM_CDTM1_DTM1_6			Input mux of CDTM1_DTM1_AUXIN0/1
	GTM_CDTM3_DTM1_6			Input mux of CDTM3_DTM1_AUXIN0/1
	GTM_CDTM4_DTM1_6			Input mux of CDTM4_DTM1_AUXIN0/1
	EGTM_CDTM0_DTM1_6			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM1_DTM1_6			Input mux of CDTM1_DTM1_AUXIN0/1
	EGTM_TIM0_IN1_2			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_2			Mux input channel 1 of TIM module 1
	QSPI3_MRSTG_F			Master SPI data input
	CANXL00_RXDC			CANXL receive input node 0
	GPT121_CAPINB3			Trigger input to capture value of timer T5 into CAPREL register (input B)
	LETH0_P0_RXDC			LETH PortX TC14 interface receive data input
	P02.1	O0		General-purpose output
	GTM_TOUT1	O1		GTM muxed output
	QSPI4_SLSO7	O2		Master slave select output
	QSPI3_SLSO2	O3		Master slave select output
	ADC_PWM0	O4		Positive PWM
	—	O5		Reserved
	ADC_CLKOUT1	O6		Clock output from EXMOD

(table continues...)

Table 8 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT1_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
F4	P02.2	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN2_2			Mux input channel 2 of TIM module 0
	GTM_TIM1_IN2_2			Mux input channel 2 of TIM module 1
	SENT0_SENT7B			Receive input channel 7
	GTM_CDTM0_DTM0_6			Input mux of CDTM0_DTM0_AUXIN0/1
	GTM_CDTM2_DTM1_7			Input mux of CDTM2_DTM1_AUXIN0/1
	GTM_CDTM3_DTM5_7			Input mux of CDTM3_DTM5_AUXIN0/1
	GTM_CDTM5_DTM5_7			Input mux of CDTM5_DTM5_AUXIN0/1
	GTM_CDTM6_DTM5_7			Input mux of CDTM6_DTM5_AUXIN0/1
	EGTM_CDTM0_DTM0_6			Input mux of CDTM0_DTM0_AUXIN0/1
	EGTM_CDTM0_DTM2_6			Input mux of CDTM0_DTM2_AUXIN0/1
	EGTM_TIM0_IN2_2			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_2			Mux input channel 2 of TIM module 1
	EGTM_CDTM2_DTM1_7			Input mux of CDTM2_DTM1_AUXIN0/1
	P02.2	O0		General-purpose output
	GTM_TOUT2	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	QSPI3_SLSO3_F	O3		Master slave select output
	PSI5_TX0	O4		TXD outputs (send data)
	CAN02_TXD	O5		CAN transmit output node 2
	ERAY0_TXDB	O6		Transmit Channel B
	LETH0_P1_TXD	O7		LETH PortX TC14 interface transmit data output

(table continues...)

Table 8 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CANXL01_TXD	O8		CANXL transmit output node 1
	EGTM_TOUT2_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM0_CH1_F	PO		High resolution PWM 0 output channels
G5	P02.3	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN3_2			Mux input channel 3 of TIM module 0
	GTM_TIM1_IN3_2			Mux input channel 3 of TIM module 1
	ADC_CLKIN5			Clock input to EXMOD
	ERAY0_RXDB2			Receive Channel B2
	CAN02_RXDB			CAN receive input node 2
	ASCLIN1_ARXG			Receive input
	MSC1_SDI1			Upstream asynchronous input signal
	PSI5_RX0B			RXD inputs (receive data) channel 0
	GTM_CDTM2_DTM0_7			Input mux of CDTM2_DTM0_AUXIN0/1
	SENT1_SENT6B			Receive input channel 6
	GTM_CDTM3_DTM4_7			Input mux of CDTM3_DTM4_AUXIN0/1
	GTM_CDTM5_DTM4_7			Input mux of CDTM5_DTM4_AUXIN0/1
	EGTM_CDTM0_DTM3_6			Input mux of CDTM0_DTM3_AUXIN0/1
	EGTM_CDTM1_DTM3_6			Input mux of CDTM1_DTM3_AUXIN0/1
	EGTM_CDTM2_DTM0_7			Input mux of CDTM2_DTM0_AUXIN0/1
	EGTM_TIM0_IN3_2			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_2			Mux input channel 3 of TIM module 1
	SENT0_SENT12A			Receive input channel 12
	CANXL01_RXDC			CANXL receive input node 1
	LETH0_P1_RXDC			LETH PortX TC14 interface receive data input
	P02.3	O0		General-purpose output
	GTM_TOUT3	O1		GTM muxed output
	ASCLIN2_ASLSO	O2		Slave select signal output

(table continues...)

Table 8 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI3_SLSO4	O3		Master slave select output
	ADC_CLKOUT2	O4		Clock output from EXMOD
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT3_F	O9		eGTM muxed output
	—	O10		Reserved
	LETH1_P0_PPS1	O11		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
G4	P02.4	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN4_1			Mux input channel 4 of TIM module 0
	GTM_TIM1_IN4_1			Mux input channel 4 of TIM module 1
	SENT0_SENT6B			Receive input channel 6
	ADC_DATA5			Modulated data to EXMOD
	QSPI3_SLSIA_F			Slave select input
	GTM_CDTM0_DTM4_6			Input mux of CDTM0_DTM4_AUXIN0/1
	I2C0_SDAA			Serial Data Input 0
	CAN11_RXDA			CAN receive input node 1
	GTM_CDTM1_DTM4_6			Input mux of CDTM1_DTM4_AUXIN0/1
	GTM_CDTM2_DTM5_7			Input mux of CDTM2_DTM5_AUXIN0/1
	GTM_CDTM3_DTM4_6			Input mux of CDTM3_DTM4_AUXIN0/1
	GTM_CDTM5_DTM4_6			Input mux of CDTM5_DTM4_AUXIN0/1
	GTM_CDTM6_DTM4_6			Input mux of CDTM6_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM4_6			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_CDTM2_DTM5_7			Input mux of CDTM2_DTM5_AUXIN0/1
	EGTM_TIM0_IN4_1			Mux input channel 4 of TIM module 0

(table continues...)

Table 8 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM1_IN4_1			Mux input channel 4 of TIM module 1
	EGTM_CDTM0_DTM4_6			Input mux of CDTM0_DTM4_AUXIN0/1
	LETH0_P0_EDC			LETH PortX TC14 interface energy detection input
	LETH0_P0_MDIOC			LETH PortX MDIO interface data input
	P02.4	O0		General-purpose output
	GTM_TOUT4	O1		GTM muxed output
	ASCLIN2_ASCLK	O2		Shift clock output
	QSPI3_SLSO0_F	O3		Master slave select output
	PSI5S0_CLK	O4		PSI5S CLK is a clock that can be used on a pin to drive the external PHY.
	I2C0_SDA	O5		Serial Data Output
	ERAY0_TXENA	O6		Transmit Enable Channel A
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT4_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM0_CH2_F	PO	High resolution PWM 0 output channels	
	LETH0_P0_MDIO	O	LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface	
H5	P02.5	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN5_1			Mux input channel 5 of TIM module 0
	GTM_TIM1_IN5_1			Mux input channel 5 of TIM module 1
	SENT1_SENT1C			Receive input channel 1
	I2C0_SCLA			Serial Clock Input 0
	PSI5_RX1B			RXD inputs (receive data) channel 1
	PSI5S0_RXB			RX data input
	QSPI3_MRSTA_F			Master SPI data input
	GTM_CDTM1_DTM5_6			Input mux of CDTM1_DTM5_AUXIN0/1

(table continues...)

Table 8 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_CDTM2_DTM5_6			Input mux of CDTM2_DTM5_AUXIN0/1
	GTM_CDTM3_DTM5_6			Input mux of CDTM3_DTM5_AUXIN0/1
	GTM_CDTM5_DTM5_6			Input mux of CDTM5_DTM5_AUXIN0/1
	EGTM_CDTM1_DTM3_7			Input mux of CDTM1_DTM3_AUXIN0/1
	EGTM_CDTM1_DTM5_6			Input mux of CDTM1_DTM5_AUXIN0/1
	EGTM_CDTM2_DTM5_6			Input mux of CDTM2_DTM5_AUXIN0/1
	EGTM_TIM0_IN5_1			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_1			Mux input channel 5 of TIM module 1
	GTM_CDTM6_DTM5_6			Input mux of CDTM6_DTM5_AUXIN0/1
	LETH0_P1_EDC			LETH PortX TC14 interface energy detection input
	LETH0_P1_MDIOC			LETH PortX MDIO interface data input
	P02.5	O0		General-purpose output
	GTM_TOUT5	O1		GTM muxed output
	CAN11_TXD	O2		CAN transmit output node 1
	QSPI3_MRST_F	O3		Slave SPI data output
	—	O4		Reserved
	I2C0_SCL	O5		Serial Clock Output
	ERAY0_TXENB	O6		Transmit Enable Channel B
	QSPI3_MTSR_F	O7		Master SPI data output
	—	O8		Reserved
	EGTM_TOUT5_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM0_CH3_F	PO		High resolution PWM 0 output channels
	LETH0_P1_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
H4	P02.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN6_1			Mux input channel 6 of TIM module 0
	GTM_TIM1_IN1_13			Mux input channel 1 of TIM module 1

(table continues...)

Table 8 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TIM1_IN6_1			Mux input channel 6 of TIM module 1
	GTM_TIM3_IN0_10			Mux input channel 0 of TIM module 3
	LETH0_P0_AUX			LETH PortX auxiliary snapshot signal
	SENT1_SENT0C			Receive input channel 0
	ADC_DATA4			Modulated data to EXMOD
	GPT120_T3INA			Trigger/gate input of core timer T3 (input A, B and C)
	GTM_CDTM0_DTM5_1			Input mux of CDTM0_DTM5_AUXIN0/1
	GTM_CDTM2_DTM4_6			Input mux of CDTM2_DTM4_AUXIN0/1
	QSPI3_MTSRA_F			Slave SPI data input
	GTM_CDTM4_DTM5_7			Input mux of CDTM4_DTM5_AUXIN0/1
	EGTM_CDTM0_DTM2_7			Input mux of CDTM0_DTM2_AUXIN0/1
	EGTM_CDTM0_DTM5_1			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_CDTM1_DTM2_7			Input mux of CDTM1_DTM2_AUXIN0/1
	EGTM_CDTM2_DTM4_6			Input mux of CDTM2_DTM4_AUXIN0/1
	EGTM_TIM0_IN6_1			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN1_13			Mux input channel 1 of TIM module 1
	EGTM_TIM1_IN6_1			Mux input channel 6 of TIM module 1
	P02.6	O0		General-purpose output
	GTM_TOUT6	O1		GTM muxed output
	PSI5S0_TX	O2		TX data output
	QSPI3_MTSR_F	O3		Master SPI data output
	PSI5_TX1	O4		TXD outputs (send data)
	ADC_EMUXCTRL00	O5		EMUX0 Control from TMADC to PORTS
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT6_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 8 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_HRPWM0_CH4_F	PO		High resolution PWM 0 output channels
J5	P02.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN3_13			Mux input channel 3 of TIM module 0
	GTM_TIM0_IN7_1			Mux input channel 7 of TIM module 0
	GTM_TIM1_IN7_1			Mux input channel 7 of TIM module 1
	GTM_TIM3_IN1_10			Mux input channel 1 of TIM module 3
	CAN02_RXDH			CAN receive input node 2
	SENT0_SENT1C			Receive input channel 1
	GPT120_T3EUDA			Count direction control input of core timer T3
	PSI5_RX2B			RXD inputs (receive data) channel 2
	SCU_E_REQ0F			ERU channel 0 input F
	GTM_CDTM1_DTM1_7			Input mux of CDTM1_DTM1_AUXIN0/1
	QSPI3_SCLKA_F			Slave SPI clock inputs
	ADC_TRIG58			Triggers from PORTS to ADC
	GTM_CDTM3_DTM1_7			Input mux of CDTM3_DTM1_AUXIN0/1
	EGTM_CDTM1_DTM1_7			Input mux of CDTM1_DTM1_AUXIN0/1
	EGTM_TIM0_IN3_13			Mux input channel 3 of TIM module 0
	EGTM_TIM0_IN7_1			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_1			Mux input channel 7 of TIM module 1
	GTM_CDTM4_DTM1_7			Input mux of CDTM4_DTM1_AUXIN0/1
	EGTM_CDTM2_DTM3_6			Input mux of CDTM2_DTM3_AUXIN0/1
	P02.7	O0		General-purpose output
	GTM_TOUT7	O1		GTM muxed output
	—	O2		Reserved
	QSPI3_SCLK_F	O3		Master SPI clock output
	—	O4		Reserved
	ADC_EMUXCTRL01	O5		EMUX0 Control from TMADC to PORTS
	SENT1_SPC0	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT7_F	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 8 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH1_P0_PPS1	O11		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM0_CH5_F	PO		High resolution PWM 0 output channels
J4	P02.8	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN7_13			Mux input channel 7 of TIM module 0
	GTM_TIM1_IN0_13			Mux input channel 0 of TIM module 1
	GTM_TIM2_IN0_2			Mux input channel 0 of TIM module 2
	GTM_TIM3_IN0_2			Mux input channel 0 of TIM module 3
	GTM_TIM3_IN2_10			Mux input channel 2 of TIM module 3
	SENT0_SENT0C			Receive input channel 0
	GTM_CDTM0_DTM4_2			Input mux of CDTM0_DTM4_AUXIN0/1
	ADC_DATA3			Modulated data to EXMOD
	GPT120_T4INA			Trigger/gate input of timer T4
	CAN30_RXDB			CAN receive input node 0
	SCU_E_REQ5G			ERU channel 5 input G
	ADC_TRIG59			Triggers from PORTS to ADC
	EGTM_CDTM0_DTM4_2			Input mux of CDTM0_DTM4_AUXIN0/1
	GTM_CDTM1_DTM0_7			Input mux of CDTM1_DTM0_AUXIN0/1
	GTM_CDTM4_DTM0_7			Input mux of CDTM4_DTM0_AUXIN0/1
	EGTM_CDTM1_DTM0_7			Input mux of CDTM1_DTM0_AUXIN0/1
	EGTM_TIM0_IN7_13			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN0_13			Mux input channel 0 of TIM module 1
	EGTM_TIM2_IN0_2			Mux input channel 0 of TIM module 2
	GTM_CDTM4_DTM4_7			Input mux of CDTM4_DTM4_AUXIN0/1
	P02.8	O0		General-purpose output
	GTM_TOUT8	O1		GTM muxed output
	QSPI3_SLSO5_F	O2		Master slave select output
	—	O3		Reserved
	PSI5_TX2	O4		TXD outputs (send data)

(table continues...)

Table 8 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ADC_EMUXCTRL02	O5		EMUX0 Control from TMADC to PORTS
	—	O6		Reserved
	PSI5S1_CLK	O7		PSI5S CLK is a clock that can be used on a pin to drive the external PHY.
	—	O8		Reserved
	EGTM_TOUT8_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM0_CH6_F	PO		High resolution PWM 0 output channels
H7	P02.9	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN2_10			Mux input channel 2 of TIM module 0
	GTM_TIM3_IN3_10			Mux input channel 3 of TIM module 3
	GTM_TIM4_IN2_2			Mux input channel 2 of TIM module 4
	SENT0_SENT10B			Receive input channel 10
	GTM_CDTM0_DTM4_7			Input mux of CDTM0_DTM4_AUXIN0/1
	GTM_CDTM2_DTM4_7			Input mux of CDTM2_DTM4_AUXIN0/1
	GTM_CDTM2_DTM0_6			Input mux of CDTM2_DTM0_AUXIN0/1
	GTM_CDTM0_DTM5_2			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_CDTM0_DTM4_7			Input mux of CDTM0_DTM4_AUXIN0/1
	EGTM_CDTM2_DTM4_7			Input mux of CDTM2_DTM4_AUXIN0/1
	EGTM_CDTM0_DTM5_2			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_TIM0_IN2_10			Mux input channel 2 of TIM module 0
	EGTM_CDTM2_DTM0_6			Input mux of CDTM2_DTM0_AUXIN0/1
	EGTM_CDTM2_DTM3_7			Input mux of CDTM2_DTM3_AUXIN0/1
	P02.9	O0		General-purpose output
	GTM_TOUT116	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	—	O3		Reserved
	CAN30_TXD	O4		CAN transmit output node 0

(table continues...)

Table 8 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CAN01_TXD	O5		CAN transmit output node 1
	SENT0_SPC10	O6		Transmit output
	ADC_EMUXCTRL03	O7		EMUX0 Control from TMADC to PORTS
	—	O8		Reserved
	EGTM_TOUT116_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM0_CH7_F	PO		High resolution PWM 0 output channels
J8	P02.10	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN3_10			Mux input channel 3 of TIM module 0
	GTM_TIM3_IN4_11			Mux input channel 4 of TIM module 3
	GTM_TIM4_IN3_2			Mux input channel 3 of TIM module 4
	ASCLIN2_ARXC			Receive input
	CAN01_RXDE			CAN receive input node 1
	SENT1_SENT10B			Receive input channel 10
	GTM_CDTM0_DTM1_7			Input mux of CDTM0_DTM1_AUXIN0/1
	GTM_CDTM1_DTM4_7			Input mux of CDTM1_DTM4_AUXIN0/1
	GTM_CDTM2_DTM1_6			Input mux of CDTM2_DTM1_AUXIN0/1
	LETH0_P2_CRSD			LETH PortX MII carrier sense
	EGTM_CDTM0_DTM1_7			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM1_DTM4_7			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM2_6			Input mux of CDTM1_DTM2_AUXIN0/1
	EGTM_CDTM2_DTM1_6			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_TIM0_IN3_10			Mux input channel 3 of TIM module 0
	EGTM_CDTM2_DTM2_7			Input mux of CDTM2_DTM2_AUXIN0/1
	P02.10	O0		General-purpose output
	GTM_TOUT117	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved

(table continues...)

Table 8 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O4		Reserved
	—	O5		Reserved
	SENT1_SPC10	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT117_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
J7	P02.11	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN7_7			Mux input channel 7 of TIM module 0
	GTM_TIM3_IN5_13			Mux input channel 5 of TIM module 3
	GTM_TIM4_IN4_3			Mux input channel 4 of TIM module 4
	SENT0_SENT11B			Receive input channel 11
	CAN30_RXDD			CAN receive input node 0
	SCU_E_REQ7G			ERU channel 7 input G
	GTM_CDTM0_DTM5_7			Input mux of CDTM0_DTM5_AUXIN0/1
	GTM_CDTM1_DTM5_7			Input mux of CDTM1_DTM5_AUXIN0/1
	GTM_CDTM6_DTM4_7			Input mux of CDTM6_DTM4_AUXIN0/1
	EGTM_CDTM0_DTM5_7			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_CDTM1_DTM5_7			Input mux of CDTM1_DTM5_AUXIN0/1
	EGTM_TIM0_IN7_7			Mux input channel 7 of TIM module 0
	ADC_TMADC2CH15	AI		Analog Input for TMADC2 Channel 15
	P02.11	O0		General-purpose output
	GTM_TOUT118	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	SENT0_SPC11	O6		Transmit output

(table continues...)

Table 8 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT118_F	O9		eGTM muxed output
	LETH0_P2_PPS	O10		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
A3	P02.12	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM3_IN6_13			Mux input channel 6 of TIM module 3
	GTM_TIM4_IN0_3			Mux input channel 0 of TIM module 4
	GTM_TIM5_IN0_3			Mux input channel 0 of TIM module 5
	ADC_DATA6			Modulated data to EXMOD
	SENT0_SENT7C			Receive input channel 7
	GTM_CDTM0_DTM0_7			Input mux of CDTM0_DTM0_AUXIN0/1
	GTM_CDTM0_DTM5_6			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_CDTM0_DTM0_7			Input mux of CDTM0_DTM0_AUXIN0/1
	EGTM_CDTM0_DTM5_6			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_CDTM0_DTM3_7			Input mux of CDTM0_DTM3_AUXIN0/1
	P02.12	O0		General-purpose output
	GTM_TOUT151	O1		GTM muxed output
	QSPI3_SLSO11	O2		Master slave select output
	QSPI4_SLSO4	O3		Master slave select output
	ASCLIN6_ASLSO	O4		Slave select signal output
	ERAY0_TXDB	O5		Transmit Channel B
	SENT0_SPC7	O6		Transmit output
	ASCLIN2_ATX	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT151_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved

(table continues...)

Table 8 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
B1	P02.13	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM3_IN7_11			Mux input channel 7 of TIM module 3
	GTM_TIM4_IN2_3			Mux input channel 2 of TIM module 4
	GTM_TIM5_IN2_2			Mux input channel 2 of TIM module 5
	ADC_CLKIN6			Clock input to EXMOD
	SENT0_SENT2C			Receive input channel 2
	P02.13	O0		General-purpose output
	GTM_TOUT153	O1		GTM muxed output
	QSPI3_SLS07_F	O2		Master slave select output
	QSPI4_SLS06	O3		Master slave select output
	CAN00_TXD	O4		CAN transmit output node 0
	CAN20_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	ADC_CLKOUT3	O7		Clock output from EXMOD
	—	O8		Reserved
	EGTM_TOUT153_F	O9		eGTM muxed output
	LETH0_P0_PPS	O10		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
C2	P02.14	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM2_IN4_11			Mux input channel 4 of TIM module 2
	GTM_TIM4_IN3_3			Mux input channel 3 of TIM module 4
	GTM_TIM5_IN3_3			Mux input channel 3 of TIM module 5
	CAN20_RXDD			CAN receive input node 0
	CAN00_RXDH			CAN receive input node 0

(table continues...)

Table 8 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ADC_DATA7			Modulated data to EXMOD
	GTM_CDTM3_DTM0_7			Input mux of CDTM3_DTM0_AUXIN0/1
	EGTM_CDTM2_DTM2_6			Input mux of CDTM2_DTM2_AUXIN0/1
	EGTM_TIM2_IN4_11			Mux input channel 4 of TIM module 2
	P02.14	O0		General-purpose output
	GTM_TOUT154	O1		GTM muxed output
	ASCLIN6_ASCLK	O2		Shift clock output
	ASCLIN7_ATX	O3		Transmit output
	ADC_CLKOUT4	O4		Clock output from EXMOD
	ERAY0_TXENB	O5		Transmit Enable Channel B
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT154_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
C1	P02.15	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM2_IN5_13			Mux input channel 5 of TIM module 2
	GTM_TIM4_IN1_3			Mux input channel 1 of TIM module 4
	GTM_TIM5_IN1_3			Mux input channel 1 of TIM module 5
	ADC_CLKIN7			Clock input to EXMOD
	EGTM_TIM2_IN5_13			Mux input channel 5 of TIM module 2
	P02.15	O0		General-purpose output
	GTM_TOUT152	O1		GTM muxed output
	QSPI3_SLSO12_F	O2		Master slave select output
	QSPI4_SLSO5	O3		Master slave select output
	ASCLIN6_ATX	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—			

(table continues...)

Table 8 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ADC_CLKOUT0	O7		Clock output from EXMOD
	—	O8		Reserved
	EGTM_TOUT152_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

3.2.4 BGA436_STD port 10

Table 9 Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
D10	P10.0	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN4_2			Mux input channel 4 of TIM module 0
	GTM_TIM1_IN4_2			Mux input channel 4 of TIM module 1
	GTM_TIM4_IN0_13			Mux input channel 0 of TIM module 4
	GPT120_T6EUDB			Count direction control input of core timer T6
	SENT0_SENT13B			Receive input channel 13
	QSPI7_MRSTB			Master SPI data input
	GTM_CDTM3_DTM0_5			Input mux of CDTM3_DTM0_AUXIN0/1
	GTM_CDTM4_DTM0_5			Input mux of CDTM4_DTM0_AUXIN0/1
	GTM_CDTM5_DTM4_3			Input mux of CDTM5_DTM4_AUXIN0/1
	ADC_CLKIN3			Clock input to EXMOD
	GTM_CDTM5_DTM5_3			Input mux of CDTM5_DTM5_AUXIN0/1
	GTM_CDTM6_DTM4_3			Input mux of CDTM6_DTM4_AUXIN0/1
	GTM_CDTM6_DTM5_3			Input mux of CDTM6_DTM5_AUXIN0/1
	EGTM_TIM0_IN4_2			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_2			Mux input channel 4 of TIM module 1
	SENT1_SENT10C			Receive input channel 10
	LETH0_P2_MII_RMII_RXD0B			LETH0 PortX MII and RMII receive data bit 0 (to be used with LETH0_P2_RXCLKB or LETH0_P2_REFCLKB)

(table continues...)

Table 9 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P2_MII_RMII_RXD0D			LETH0 PortX MII and RMII receive data bit 0 (to be used with LETH0_P2_RXCLKD or LETH0_P2_REFCLKD)
	LETH0_P2_RXDF			LETH PortX TC14 interface receive data input
	P10.0	O0		General-purpose output
	GTM_TOUT102	O1		GTM muxed output
	—	O2		Reserved
	QSPI1_SLSO10_F	O3		Master slave select output
	CAN30_TXD	O4		CAN transmit output node 0
	ADC_CLKOUT0	O5		Clock output from EXMOD
	—	O6		Reserved
	CANXL00_TXD	O7		CANXL transmit output node 0
	QSPI7_SLSO0	O8		Master slave select output
	EGTM_TOUT102	O9		eGTM muxed output
	ASCLIN0_ATX	O10		Transmit output
	—	O11		Reserved
	ERAY0_TXDA	O12		Transmit Channel A
	—	O13		Reserved
	CAN01_TXD	O14		CAN transmit output node 1
	ASCLIN0_ASCLK	O15		Shift clock output
	LETH0_P2_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
E10	P10.1	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN1_3			Mux input channel 1 of TIM module 0
	GTM_TIM1_IN1_3			Mux input channel 1 of TIM module 1
	GTM_TIM4_IN4_13			Mux input channel 4 of TIM module 4
	GPT120_T5EUDB			Count direction control input of timer T5
	QSPI1_MRSTA_F			Master SPI data input
	GTM_CDTM0_DTM0_2			Input mux of CDTM0_DTM0_AUXIN0/1
	GTM_CDTM1_DTM4_3			Input mux of CDTM1_DTM4_AUXIN0/1
	GTM_CDTM1_DTM5_3			Input mux of CDTM1_DTM5_AUXIN0/1
	GTM_CDTM2_DTM1_5			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_CDTM0_DTM0_2			Input mux of CDTM0_DTM0_AUXIN0/1
	EGTM_CDTM0_DTM2_2			Input mux of CDTM0_DTM2_AUXIN0/1

(table continues...)

Table 9 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_CDTM1_DTM4_3			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM5_3			Input mux of CDTM1_DTM5_AUXIN0/1
	GTM_CDTM3_DTM1_5			Input mux of CDTM3_DTM1_AUXIN0/1
	GTM_CDTM4_DTM1_5			Input mux of CDTM4_DTM1_AUXIN0/1
	EGTM_CDTM2_DTM1_5			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_TIM0_IN1_3			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_3			Mux input channel 1 of TIM module 1
	LETH0_P2_MII_RXD3B			LETH0 PortX MII receive data bit 3 (to be used with LETH0_P2_RXCLKB)
	ASCLIN0_ARXF			Receive input
	SENT0_SENT10C			Receive input channel 10
	P10.1	O0		General-purpose output
	GTM_TOUT103	O1		GTM muxed output
	QSPI1_MTSR_F	O2		Master SPI data output
	QSPI1_MRST_F	O3		Slave SPI data output
	MSC0_EN1	O4		Chip Select
	ADC_BFL1	O5		Boundary flags from FCC
	ASCLIN0_ATX	O6		Transmit output
	—	O7		Reserved
	QSPI7_SLSO1	O8		Master slave select output
	EGTM_TOUT103	O9		eGTM muxed output
	LETH0_P2_TXD	O10		LETH PortX TC14 interface transmit data output
	—	O11		Reserved
	—	O12		Reserved
	ASCLIN2_ARTS_F	O13		Ready to send output
	LETH0_P2_MIID_TXEN	O14		LETH0 PortX MII transmit enable (to be used with LETH0_P2_TXCLKD)
	LETH0_P2_RMIID_TXEN	O15		LETH0 PortX RMII transmit enable (to be used with LETH0_P2_REFCLKD)
	LETH0_P2_RMIIRD_TXEN	PO		LETH0 PortX RMII transmit enable (to be used with LETH0_P2_REFCLKD - registered*)
D8	P10.2	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN2_3			Mux input channel 2 of TIM module 0
	GTM_TIM1_IN2_3			Mux input channel 2 of TIM module 1

(table continues...)

Table 9 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TIM4_IN5_13			Mux input channel 5 of TIM module 4
	CAN02_RXDE			CAN receive input node 2
	MSC0_SDI1			Upstream asynchronous input signal
	QSPI1_SCLKA_F			Slave SPI clock inputs
	GPT120_T6INB			Trigger/gate input of core timer T6
	SCU_E_REQ2A			ERU channel 2 input A
	GTM_CDTM0_DTM4_3			Input mux of CDTM0_DTM4_AUXIN0/1
	GTM_CDTM0_DTM5_3			Input mux of CDTM0_DTM5_AUXIN0/1
	GTM_CDTM2_DTM0_3			Input mux of CDTM2_DTM0_AUXIN0/1
	GTM_CDTM2_DTM1_3			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_CDTM0_DTM4_3			Input mux of CDTM0_DTM4_AUXIN0/1
	EGTM_CDTM0_DTM5_3			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_CDTM2_DTM0_3			Input mux of CDTM2_DTM0_AUXIN0/1
	EGTM_CDTM2_DTM1_3			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_TIM0_IN2_3			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_3			Mux input channel 2 of TIM module 1
	LETH0_P2_MII_RXD2B			LETH0 PortX MII receive data bit 2 (to be used with LETH0_P2_RXCLKB)
	LETH1_P0_MDIOB			LETH PortX MDIO interface data input
	P10.2	O0		General-purpose output
	GTM_TOUT104	O1		GTM muxed output
	CAN32_TXD	O2		CAN transmit output node 2
	QSPI1_SCLK_F	O3		Master SPI clock output
	MSC0_EN0	O4		Chip Select
	ADC_BFL3	O5		Boundary flags from FCC
	ASCLIN2_ASCLK_F	O6		Shift clock output
	—	O7		Reserved
	QSPI7_SLSO2	O8		Master slave select output
	EGTM_TOUT104	O9		eGTM muxed output
	ASCLIN2_ATX_F	O10		Transmit output
	—	O11		Reserved
	QSPI2_SLSO1	O12		Master slave select output

(table continues...)

Table 9 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P2_MIID_TXD0	O13		LETH0 PortX MII transmit data bit 0 (to be used with LETH0_P2_TXCLKD)
	—	O14		Reserved
	LETH0_P2_RMIID_TXD0	O15		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P2_REFCLKD)
	LETH0_P2_RMIIRD_TXD0	PO		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P2_REFCLKD - registered*)
	LETH1_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
D9	P10.3	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN3_3			Mux input channel 3 of TIM module 0
	GTM_TIM1_IN3_3			Mux input channel 3 of TIM module 1
	GTM_TIM4_IN6_10			Mux input channel 6 of TIM module 4
	QSPI1_MTSRA_F			Slave SPI data input
	SCU_E_REQ3A			ERU channel 3 input A
	GPT120_T5INB			Trigger/gate input of timer T5
	ASCLIN2_ARXH_F			Receive input
	MSC0_SDI5			Upstream asynchronous input signal
	GTM_CDTM2_DTM0_5			Input mux of CDTM2_DTM0_AUXIN0/1
	GTM_CDTM0_DTM1_2			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM0_DTM3_2			Input mux of CDTM0_DTM3_AUXIN0/1
	EGTM_CDTM0_DTM1_2			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM2_DTM0_5			Input mux of CDTM2_DTM0_AUXIN0/1
	EGTM_CDTM2_DTM2_5			Input mux of CDTM2_DTM2_AUXIN0/1
	EGTM_TIM0_IN3_3			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_3			Mux input channel 3 of TIM module 1
	EGTM_CDTM2_DTM3_3			Input mux of CDTM2_DTM3_AUXIN0/1
	LETH0_P2_MII_RXDVD			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	LETH0_P2_RMII_CRSDVD			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	P10.3	O0		General-purpose output
	GTM_TOUT105	O1		GTM muxed output
	CAN31_TXD	O2		CAN transmit output node 1

(table continues...)

Table 9 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI1_MTSR_F	O3		Master SPI data output
	MSC0_EN0	O4		Chip Select
	ADC_BFL8	O5		Boundary flags from FCC
	CAN02_TXD	O6		CAN transmit output node 2
	ASCLIN2_ASLSO_F	O7		Slave select signal output
	QSPI7_SCLK	O8		Master SPI clock output
	EGTM_TOUT105	O9		eGTM muxed output
	ASCLIN2_ATX_F	O10		Transmit output
	—	O11		Reserved
	QSPI2_SLSO15	O12		Master slave select output
	ASCLIN1_ASLSO	O13		Slave select signal output
	ASCLIN3_ASLSO	O14		Slave select signal output
	—	O15		Reserved
	—	—		—
E9	P10.4	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN6_2			Mux input channel 6 of TIM module 0
	GTM_TIM1_IN6_2			Mux input channel 6 of TIM module 1
	GTM_TIM4_IN7_3			Mux input channel 7 of TIM module 4
	QSPI1_MTSRC_F			Slave SPI data input
	GPT120_T3INB			Trigger/gate input of core timer T3 (input A, B and C)
	CAN30_RXDA			CAN receive input node 0
	GTM_CDTM3_DTM4_5			Input mux of CDTM3_DTM4_AUXIN0/1
	GTM_CDTM4_DTM4_5			Input mux of CDTM4_DTM4_AUXIN0/1
	EGTM_CDTM2_DTM2_3			Input mux of CDTM2_DTM2_AUXIN0/1
	LETH0_P2_CRSB			LETH PortX MII carrier sense
	EGTM_CDTM2_DTM3_5			Input mux of CDTM2_DTM3_AUXIN0/1
	EGTM_TIM0_IN6_2			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN6_2			Mux input channel 6 of TIM module 1
	P10.4	O0		General-purpose output
	GTM_TOUT106	O1		GTM muxed output
	—	O2		Reserved
	QSPI1_SLSO8_F	O3		Master slave select output
	QSPI1_MTSR_F	O4		Master SPI data output
	MSC0_EN0	O5		Chip Select
	—	—		—
	—	—		—
	—	—		—

(table continues...)

Table 9 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ADC_BFL9	O6		Boundary flags from FCC
	ASCLIN2_ASLSO_F	O7		Slave select signal output
	QSPI7_MTSR	O8		Master SPI data output
	EGTM_TOUT106	O9		eGTM muxed output
	GPT123_T3OUT	O10		External output for overflow/underflow detection of core timer T3
	—	O11		Reserved
	LETH0_P2_MIID_TXD1	O12		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P2_TXCLKD)
	LETH0_P2_MIID_TXD3	O13		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P2_TXCLKD)
	ASCLIN3_ASLSO	O14		Slave select signal output
	LETH0_P2_RMIID_TXD1	O15		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P2_REFCLKD)
	LETH0_P2_RMIIRD_TXD1	PO		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P2_REFCLKD - registered*)
E8	P10.5	I	FAST / PU2 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN2_4			Mux input channel 2 of TIM module 0
	GTM_TIM1_IN2_4			Mux input channel 2 of TIM module 1
	GTM_TIM4_IN3_14			Mux input channel 3 of TIM module 4
	QSPI1_MRSTE_F			Master SPI data input
	CAN20_RXDA			CAN receive input node 0
	MSC0_INJ1			Injection signal from port
	GTM_CDTM2_DTM4_5			Input mux of CDTM2_DTM4_AUXIN0/1
	GTM_CDTM3_DTM5_5			Input mux of CDTM3_DTM5_AUXIN0/1
	GTM_CDTM4_DTM5_5			Input mux of CDTM4_DTM5_AUXIN0/1
	GTM_CDTM5_DTM4_5			Input mux of CDTM5_DTM4_AUXIN0/1
	GTM_CDTM6_DTM4_5			Input mux of CDTM6_DTM4_AUXIN0/1
	EGTM_CDTM2_DTM4_5			Input mux of CDTM2_DTM4_AUXIN0/1
	QSPI5_MRSTE			Master SPI data input
	EGTM_TIM0_IN2_4			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_4			Mux input channel 2 of TIM module 1
	PMS_HWCFG4IN			HWCFG4 pin input
	P10.5	O0		General-purpose output

(table continues...)

Table 9 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TOUT107	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	QSPI3_SLSO8	O3		Master slave select output
	QSPI1_SLSO9	O4		Master slave select output
	GPT120_T6OUT	O5		External output for overflow/underflow detection of core timer T6
	—	O6		Reserved
	PSI5_TX3	O7		TXD outputs (send data)
	QSPI1_MRST	O8		Slave SPI data output
	EGTM_TOUT107	O9		eGTM muxed output
	QSPI5_MRST	O10		Slave SPI data output
	—	O11		Reserved
	LETH0_P2_MIID_TXEN	O12		LETH0 PortX MII transmit enable (to be used with LETH0_P2_TXCLKD)
	ERAY0_TXDB	O13		Transmit Channel B
	—	O14		Reserved
	LETH0_P2_RMIID_TXEN	O15		LETH0 PortX RMII transmit enable (to be used with LETH0_P2_REFCLKD)
	LETH0_P2_RMIIRD_TXEN	PO		LETH0 PortX RMII transmit enable (to be used with LETH0_P2_REFCLKD - registered*)
D7	P10.6	I	FAST / PU2 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN3_4			Mux input channel 3 of TIM module 0
	GTM_TIM1_IN3_4			Mux input channel 3 of TIM module 1
	GTM_TIM4_IN2_14			Mux input channel 2 of TIM module 4
	PSI5_RX3C			RXD inputs (receive data) channel 3
	ASCLIN2_ARXD_F			Receive input
	QSPI3_MTSRB			Slave SPI data input
	ASCLIN7_ARXH			Receive input
	SENT1_SENT12B			Receive input channel 12
	GTM_CDTM2_DTM5_5			Input mux of CDTM2_DTM5_AUXIN0/1
	GTM_CDTM5_DTM5_5			Input mux of CDTM5_DTM5_AUXIN0/1
	GTM_CDTM6_DTM5_5			Input mux of CDTM6_DTM5_AUXIN0/1
	EGTM_CDTM2_DTM5_5			Input mux of CDTM2_DTM5_AUXIN0/1
	QSPI1_MRSTC_F			Master SPI data input

(table continues...)

Table 9 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM0_IN3_4			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_4			Mux input channel 3 of TIM module 1
	PMS_HWCFG5IN			HWCFG5 pin input
	P10.6	O0		General-purpose output
	GTM_TOUT108	O1		GTM muxed output
	ASCLIN2_ASCLK_F	O2		Shift clock output
	QSPI3_MTSR	O3		Master SPI data output
	GPT120_T3OUT	O4		External output for overflow/underflow detection of core timer T3
	CAN20_TXD	O5		CAN transmit output node 0
	QSPI1_MRST_F	O6		Slave SPI data output
	—	O7		Reserved
	SENT1_SPC12	O8		Transmit output
	EGTM_TOUT108	O9		eGTM muxed output
	QSPI5_MTSR	O10		Master SPI data output
	LETH0_P2_MIID_TXD2	O11		LETH0 PortX MII transmit data bit 2 (to be used with LETH0_P2_TXCLKD)
	QSPI2_SLSO14	O12		Master slave select output
	CAN13_TXD	O13		CAN transmit output node 3
	ERAY0_TXENB	O14		Transmit Enable Channel B
	—	O15		Reserved
D6	P10.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN0_3			Mux input channel 0 of TIM module 0
	GTM_TIM1_IN0_3			Mux input channel 0 of TIM module 1
	GPT120_T3EUDB			Count direction control input of core timer T3
	ASCLIN2_ACTSA_F			Clear to send input
	QSPI3_MRSTB			Master SPI data input
	SCU_E_REQ0B			ERU channel 0 input B
	CAN10_RXDH			CAN receive input node 0
	CAN13_RXDH			CAN receive input node 3
	CANXL00_RXDE			CANXL receive input node 0
	QSPI7_MTSRD			Slave SPI data input
	EGTM_TIM0_IN0_3			Mux input channel 0 of TIM module 0

(table continues...)

Table 9 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM1_IN0_3			Mux input channel 0 of TIM module 1
	LETH0_P2_REFCLKB			LETH PortX RMII reference clock
	LETH0_P2_RXCLKB			LETH PortX MII receive clock
	LETH0_P2_REFCLKD			LETH0 PortX RMII reference clock
	LETH0_P2_RXCLKD			LETH PortX MII receive clock
	P10.7	O0		General-purpose output
	GTM_TOUT109	O1		GTM muxed output
	—	O2		Reserved
	QSPI3_MRST	O3		Slave SPI data output
	—	O4		Reserved
	CAN20_TXD	O5		CAN transmit output node 0
	CAN12_TXD	O6		CAN transmit output node 2
	QSPI7_SCLK	O7		Master SPI clock output
	QSPI7_MRST	O8		Slave SPI data output
	EGTM_TOUT109	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	ASCLIN0_ARTS	O12		Ready to send output
	QSPI2_SLSO13	O13		Master slave select output
	—	O14		Reserved
	—	O15		Reserved
E7	P10.8	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN5_2			Mux input channel 5 of TIM module 0
	GTM_TIM1_IN5_2			Mux input channel 5 of TIM module 1
	GTM_TIM4_IN0_14			Mux input channel 0 of TIM module 4
	CAN12_RXDB			CAN receive input node 2
	GPT120_T4INB			Trigger/gate input of timer T4
	QSPI3_SCLKB			Slave SPI clock inputs
	SCU_E_REQ1B			ERU channel 1 input B
	QSPI1_SLSIC_F			Slave select input
	CAN20_RXDB			CAN receive input node 0
	SENT1_SENT14A			Receive input channel 14
	CAN02_RXDG			CAN receive input node 2

(table continues...)

Table 9 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI7_MRSTG			Master SPI data input
	EGTM_TIM0_IN5_2			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_2			Mux input channel 5 of TIM module 1
	LETH0_P2_MII_RMII_RXD 1B			LETH0 PortX MII and RMII receive data bit 1 (to be used with LETH0_P2_RXCLKB or LETH0_P2_REFCLKB)
	LETH0_P2_MII_RMII_RXD 1D			LETH0 PortX MII and RMII receive data bit 1 (to be used with LETH0_P2_RXCLKD or LETH0_P2_REFCLKD)
	P10.8	O0		General-purpose output
	GTM_TOUT110	O1		GTM muxed output
	ASCLIN2_ARTS	O2		Ready to send output
	QSPI3_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	ASCLIN5_ASLSO	O5		Slave select signal output
	ASCLIN7_ASLSO	O6		Slave select signal output
	—	O7		Reserved
	QSPI1_SLSO11	O8		Master slave select output
	EGTM_TOUT110	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
B7	P10.9	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN1_10			Mux input channel 1 of TIM module 0
	GTM_TIM4_IN1_4			Mux input channel 1 of TIM module 4
	GTM_TIM6_IN0_5			Mux input channel 0 of TIM module 6
	SENT1_SENT7C			Receive input channel 7
	ASCLIN6_ARXD			Receive input
	QSPI5_MTSRF			Slave SPI data input
	LETH0_P2_MDIOB			LETH PortX MDIO interface data input
	LETH0_P2_EDB			LETH PortX TC14 interface energy detection input
	EGTM_TIM0_IN1_10			Mux input channel 1 of TIM module 0

(table continues...)

Table 9 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P2_MII_RXD3D			LETH0 PortX MII receive data bit 3 (to be used with LETH0_P2_RXCLKD)
	P10.9	O0		General-purpose output
	GTM_TOUT265	O1		GTM muxed output
	CAN23_TXD	O2		CAN transmit output node 3
	MSC0_EN1	O3		Chip Select
	CAN10_TXD	O4		CAN transmit output node 0
	ERAY0_TXENB	O5		Transmit Enable Channel B
	ERAY0_TXENA	O6		Transmit Enable Channel A
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT265	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
B5	P10.10	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN2_11			Mux input channel 2 of TIM module 0
	GTM_TIM4_IN2_4			Mux input channel 2 of TIM module 4
	GTM_TIM6_IN1_5			Mux input channel 1 of TIM module 6
	SENT0_SENT8C			Receive input channel 8
	CAN23_RXDH			CAN receive input node 3
	QSPI2_MRSTH			Master SPI data input
	LETH0_P2_COLA			LETH PortX MII collision detection
	EGTM_TIM0_IN2_11			Mux input channel 2 of TIM module 0
	P10.10	O0		General-purpose output
	GTM_TOUT266	O1		GTM muxed output
	ASCLIN6_ATX	O2		Transmit output
	MSC0_EN0	O3		Chip Select

(table continues...)

Table 9 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN1_ATX	O4		Transmit output
	CAN02_TXD	O5		CAN transmit output node 2
	ERAY0_TXDA	O6		Transmit Channel A
	—	O7		Reserved
	QSPI1_SLSO11	O8		Master slave select output
	EGTM_TOUT266	O9		eGTM muxed output
	LETH0_P2_MIID_TXD2	O10		LETH0 PortX MII transmit data bit 2 (to be used with LETH0_P2_TXCLKD)
	LETH0_P2_TXD	O11		LETH PortX TC14 interface transmit data output
	—	O12		Reserved
	LETH0_P2_MIID_TXD0	O13		LETH0 PortX MII transmit data bit 0 (to be used with LETH0_P2_TXCLKD)
	—	O14		Reserved
	LETH0_P2_RMIID_TXD0	O15		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P2_REFCLKD)
	LETH0_P2_RMIIRD_TXD0	PO		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P2_REFCLKD - registered*)
A7	P10.11	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN5_9			Mux input channel 5 of TIM module 0
	GTM_TIM4_IN5_4			Mux input channel 5 of TIM module 4
	GTM_TIM6_IN2_5			Mux input channel 2 of TIM module 6
	SENT1_SENT9C			Receive input channel 9
	EGTM_TIM0_IN5_9			Mux input channel 5 of TIM module 0
	LETH0_P2_MII_RXD2D			LETH0 PortX MII receive data bit 2 (to be used with LETH0_P2_RXCLKD)
	LETH0_P2_RXDB			LETH PortX TC14 interface receive data input
	P10.11	O0		General-purpose output
	GTM_TOUT269	O1		GTM muxed output
	ASCLIN6_ASCLK	O2		Shift clock output
	—	O3		Reserved
	MSC2_EN2	O4		Chip Select
	MSC2_SOP	O5		Data output - direct part of the differential signal
	—	O6		Reserved
	—	O7		Reserved

(table continues...)

Table 9 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O8		Reserved
	EGTM_TOUT269	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
A5	P10.13	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN4_9			Mux input channel 4 of TIM module 0
	GTM_TIM4_IN4_4			Mux input channel 4 of TIM module 4
	GTM_TIM6_IN3_5			Mux input channel 3 of TIM module 6
	SENT0_SENT9C			Receive input channel 9
	QSPI5_SCLKC			Slave SPI clock inputs
	EGTM_TIM0_IN4_9			Mux input channel 4 of TIM module 0
	P10.13	O0		General-purpose output
	GTM_TOUT268	O1		GTM muxed output
	ASCLIN6_ASLSO	O2		Slave select signal output
	QSPI5_SCLK	O3		Master SPI clock output
	MSC2_EN1	O4		Chip Select
	CAN22_TXD	O5		CAN transmit output node 2
	ASCLIN2_ARTS_F	O6		Ready to send output
	—	O7		Reserved
	QSPI7_SLSO14	O8		Master slave select output
	EGTM_TOUT268	O9		eGTM muxed output
	LETH0_P2_MIID_TXD3	O10		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P2_TXCLKD)
	—	O11		Reserved
	—	O12		Reserved
	LETH0_P2_MIID_TXD1	O13		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P2_TXCLKD)
	—	O14		Reserved

(table continues...)

Table 9 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P2_RMIID_TXD1	O15		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P2_REFCLKD)
	LETH0_P2_RMIIRD_TXD1	PO		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P2_REFCLKD - registered*)
B4	P10.14	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN3_11			Mux input channel 3 of TIM module 0
	GTM_TIM4_IN3_4			Mux input channel 3 of TIM module 4
	SENT1_SENT8C			Receive input channel 8
	CAN22_RXDG			CAN receive input node 2
	MSC0_SDI6			Upstream asynchronous input signal
	EGTM_TIM0_IN3_11			Mux input channel 3 of TIM module 0
	LETH0_P2_TXCLKB			LETH PortX MII transmit clock
	P10.14	O0		General-purpose output
	GTM_TOUT267	O1		GTM muxed output
	ASCLIN5_ATX	O2		Transmit output
	ASCLIN7_ATX	O3		Transmit output
	MSC2_EN0	O4		Chip Select
	CAN23_TXD	O5		CAN transmit output node 3
	QSPI5_SLSO15	O6		Master slave select output
	—	O7		Reserved
	QSPI7_SLSO13	O8		Master slave select output
	EGTM_TOUT267	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	LETH0_P2_MIID_TXER	O13		LETH0 PortX MII transmit error (to be used with LETH0_P2_TXCLKD)
	—	O14		Reserved
	—	O15		Reserved
A4	P10.15	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN6_9			Mux input channel 6 of TIM module 0
	GTM_TIM4_IN6_4			Mux input channel 6 of TIM module 4
	ASCLIN5_ARXF			Receive input
	ASCLIN7_ARXG			Receive input

(table continues...)

Table 9 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CAN23_RXDG			CAN receive input node 3
	LETH0_P2_MDIOF			LETH PortX MDIO interface data input
	LETH0_P2_EDF			LETH PortX TC14 interface energy detection input
	QSPI1_MRSTF_F			Master SPI data input
	EGTM_TIM0_IN6_9			Mux input channel 6 of TIM module 0
	LETH0_P2_TXCLKD			LETH PortX MII transmit clock
	P10.15	O0		General-purpose output
	GTM_TOUT270	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	QSPI5_SLSO14	O6		Master slave select output
	—	O7		Reserved
	QSPI7_SLSO12	O8		Master slave select output
	EGTM_TOUT270	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface

3.2.5 BGA436_STD port 11

Table 10 Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
H13	P11.0	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM2_IN0_7			Mux input channel 0 of TIM module 2
	GTM_TIM4_IN0_4			Mux input channel 0 of TIM module 4
	ASCLIN3_ARXB			Receive input

(table continues...)

Table 10 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_CDTM2_DTM4_2			Input mux of CDTM2_DTM4_AUXIN0/1
	GTM_CDTM2_DTM5_2			Input mux of CDTM2_DTM5_AUXIN0/1
	EGTM_CDTM2_DTM4_2			Input mux of CDTM2_DTM4_AUXIN0/1
	EGTM_CDTM2_DTM5_2			Input mux of CDTM2_DTM5_AUXIN0/1
	XSPIO_RXD3C			Receive data
	EGTM_TIM2_IN0_7			Mux input channel 0 of TIM module 2
	P11.0	O0		General-purpose output
	GTM_TOUT119	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	CAN11_TXD	O5		CAN transmit output node 1
	LETH0_P0_MIIA_TXD3	O6		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P0_TXCLKA)
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT119	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	LETH1_P0_MIIA_TXD3	O13		LETH1 PortX MII transmit data bit 3 (to be used with LETH1_P0_TXCLKA)
	—	O14		Reserved
	—	O15		Reserved
	XSPIO_TXDC3	O		Transmit data
H12	P11.1	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM2_IN1_6			Mux input channel 1 of TIM module 2
	GTM_TIM4_IN1_5			Mux input channel 1 of TIM module 4
	XSPIO_RXD2C			Receive data
	EGTM_TIM2_IN1_6			Mux input channel 1 of TIM module 2
	P11.1	O0		General-purpose output
	GTM_TOUT120	O1		GTM muxed output
	ASCLIN3_ASCLK	O2		Shift clock output

(table continues...)

Table 10 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN3_ATX	O3		Transmit output
	—	O4		Reserved
	CAN12_TXD	O5		CAN transmit output node 2
	LETH0_P0_MIIA_TXD2	O6		LETH0 PortX MII transmit data bit 2 (to be used with LETH0_P0_TXCLKA)
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT120	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	LETH1_P0_MIIA_TXD2	O13		LETH1 PortX MII transmit data bit 2 (to be used with LETH1_P0_TXCLKA)
	—	O14		Reserved
	—	O15		Reserved
	XSPIO_TXDC2	O		Transmit data
D13	P11.2	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM2_IN1_3			Mux input channel 1 of TIM module 2
	GTM_TIM3_IN1_3			Mux input channel 1 of TIM module 3
	GPT121_T3INB			Trigger/gate input of core timer T3 (input A, B and C)
	EGTM_TIM2_IN1_3			Mux input channel 1 of TIM module 2
	P11.2	O0		General-purpose output
	GTM_TOUT95	O1		GTM muxed output
	ASCLIN0_ASLSO	O2		Slave select signal output
	QSPIO_SLSO5	O3		Master slave select output
	QSPI1_SLSO5	O4		Master slave select output
	MSC0_EN1	O5		Chip Select
	LETH0_P0_MIIA_TXD1	O6		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P0_TXCLKA)
	LETH0_P0_RMIIA_TXD1	O7		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P0_REFCLKA)
	—	O8		Reserved
	EGTM_TOUT95	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 10 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O11		Reserved
	—	O12		Reserved
	LETH1_P0_MIIA_TXD1	O13		LETH1 PortX MII transmit data bit 1 (to be used with LETH1_P0_TXCLKA)
	LETH1_P0_RMIIA_TXD1	O14		LETH1 PortX RMII transmit data bit 1 (to be used with LETH1_P0_REFCLKA)
	CAN13_TXD	O15		CAN transmit output node 3
	LETH0_P0_RMIIRA_TXD1	PO		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P0_REFCLKA - registered*)
	LETH1_P0_RMIIRA_TXD1	PO		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P0_REFCLKA - registered*)
E13	P11.3	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM2_IN2_2			Mux input channel 2 of TIM module 2
	GTM_TIM3_IN2_2			Mux input channel 2 of TIM module 3
	MSC0_SDI3			Upstream asynchronous input signal
	QSPI1_MRSTB			Master SPI data input
	CAN31_RXDD			CAN receive input node 1
	GPT121_T3EUDB			Count direction control input of core timer T3
	EGTM_TIM2_IN2_2			Mux input channel 2 of TIM module 2
	P11.3	O0		General-purpose output
	GTM_TOUT96	O1		GTM muxed output
	LETH0_P0_TXD	O2		LETH PortX TC14 interface transmit data output
	QSPI1_MRST	O3		Slave SPI data output
	ERAY0_TXDA	O4		Transmit Channel A
	CANXL00_TXD	O5		CANXL transmit output node 0
	LETH0_P0_MIIA_TXD0	O6		LETH0 PortX MII transmit data bit 0 (to be used with LETH0_P0_TXCLKA)
	LETH0_P0_RMIIA_TXD0	O7		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P0_REFCLKA)
	—	O8		Reserved
	EGTM_TOUT96	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved

(table continues...)

Table 10 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH1_P0_MIIA_TXD0	O13		LETH1 PortX MII transmit data bit 0 (to be used with LETH1_P0_TXCLKA)
	LETH1_P0_RMIIA_TXD0	O14		LETH1 PortX RMII transmit data bit 0 (to be used with LETH1_P0_REFCLKA)
	LETH1_P0_TXD	O15		LETH PortX TC14 interface transmit data output
	LETH0_P0_RMIIRA_TXD0	PO		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P0_REFCLKA - registered*)
	LETH1_P0_RMIIRA_TXD0	PO		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P0_REFCLKA - registered*)
G13	P11.4	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM2_IN2_6			Mux input channel 2 of TIM module 2
	GTM_TIM4_IN2_5			Mux input channel 2 of TIM module 4
	EGTM_TIM2_IN2_6			Mux input channel 2 of TIM module 2
	P11.4	O0		General-purpose output
	GTM_TOUT121	O1		GTM muxed output
	ASCLIN3_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	CAN13_TXD	O5		CAN transmit output node 3
	LETH0_P0_MIIA_TXER	O6		LETH0 PortX MII transmit error (to be used with LETH0_P0_TXCLKA)
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT121	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	LETH1_P0_MIIA_TXER	O13		LETH1 PortX MII transmit error (to be used with LETH1_P0_TXCLKA)
	—	O14		Reserved
	XSPIO_CLKC	O15		Clock output
G11	P11.5	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM2_IN3_8			Mux input channel 3 of TIM module 2
	GTM_TIM4_IN3_5			Mux input channel 3 of TIM module 4
	XSPIO_RXD1C			Receive data

(table continues...)

Table 10 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM2_IN3_8			Mux input channel 3 of TIM module 2
	LETH0_P0_TXCLKA			LETH PortX MII transmit clock
	LETH1_P0_TXCLKA			LETH PortX MII transmit clock
	P11.5	O0		General-purpose output
	GTM_TOUT122	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	CAN20_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT122	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPI0_TXDC1	O		Transmit data
G12	P11.6	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM2_IN3_2			Mux input channel 3 of TIM module 2
	GTM_TIM3_IN3_2			Mux input channel 3 of TIM module 3
	QSPI1_SCLKB			Slave SPI clock inputs
	GPT121_T4INB			Trigger/gate input of timer T4
	LETH0_P1_EDD			LETH PortX TC14 interface energy detection input
	LETH0_P1_MDIOD			LETH PortX MDIO interface data input
	EGTM_TIM2_IN3_2			Mux input channel 3 of TIM module 2
	P11.6	O0		General-purpose output
	GTM_TOUT97	O1		GTM muxed output
	ERAY0_TXENB	O2		Transmit Enable Channel B
	QSPI1_SCLK	O3		Master SPI clock output
	ERAY0_TXENA	O4		Transmit Enable Channel A

(table continues...)

Table 10 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	MSC0_FCLP	O5		Shift-clock direct part of the differential signal
	LETH0_P0_MIIA_TXEN	O6		LETH0 PortX MII transmit enable (to be used with LETH0_P0_TXCLKA)
	LETH0_P0_RMIIA_TXEN	O7		LETH0 PortX RMII transmit enable (to be used with LETH0_P0_REFCLKA)
	—	O8		Reserved
	EGTM_TOUT97	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	LETH1_P0_MIIA_TXEN	O13		LETH1 PortX MII transmit enable (to be used with LETH1_P0_TXCLKA)
	LETH1_P0_RMIIA_TXEN	O14		LETH1 PortX RMII transmit enable (to be used with LETH1_P0_REFCLKA)
	CAN00_TXD	O15		CAN transmit output node 0
	LETH0_P0_RMIIRA_TXEN	PO		LETH0 PortX RMII transmit enable (to be used with LETH0_P0_REFCLKA - registered*)
	LETH1_P0_RMIIRA_TXEN	PO		LETH0 PortX RMII transmit enable (to be used with LETH0_P0_REFCLKA - registered*)
	LETH0_P1_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
H11	P11.7	I	SLOW / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM2_IN4_7			Mux input channel 4 of TIM module 2
	GTM_TIM4_IN4_5			Mux input channel 4 of TIM module 4
	CAN11_RXDD			CAN receive input node 1
	XSPIO_RXD0C			Receive data
	EGTM_TIM2_IN4_7			Mux input channel 4 of TIM module 2
	LETH0_P0_MII_RXD3A			LETH0 PortX MII receive data bit 3 (to be used with LETH0_P0_RXCLKA)
	LETH1_P0_MII_RXD3A			LETH1 PortX MII receive data bit 3 (to be used with LETH1_P0_RXCLKA)
	P11.7	O0		General-purpose output
	GTM_TOUT123	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved

(table continues...)

Table 10 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT123	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPIO_TXDC0	O		Transmit data
H10	P11.8	I	SLOW / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM2_IN5_8			Mux input channel 5 of TIM module 2
	GTM_TIM4_IN5_5			Mux input channel 5 of TIM module 4
	CAN12_RXDD			CAN receive input node 2
	GPT121_T5INB			Trigger/gate input of timer T5
	EGTM_TIM2_IN5_8			Mux input channel 5 of TIM module 2
	LETH0_P0_MII_RXD2A			LETH0 PortX MII receive data bit 2 (to be used with LETH0_P0_RXCLKA)
	LETH1_P0_MII_RXD2A			LETH1 PortX MII receive data bit 2 (to be used with LETH1_P0_RXCLKA)
	P11.8	O0		General-purpose output
	GTM_TOUT124	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT124	O9		eGTM muxed output

(table continues...)

Table 10 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	XSPI0_CSC1_N	O15		Chip select
D12	P11.9	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM2_IN4_2			Mux input channel 4 of TIM module 2
	GTM_TIM3_IN4_2			Mux input channel 4 of TIM module 3
	QSPI1_MTSRB			Slave SPI data input
	ERAY0_RXDA1			Receive Channel A1
	GPT121_T5EUDB			Count direction control input of timer T5
	CANXL00_RXDD			CANXL receive input node 0
	EGTM_TIM2_IN4_2			Mux input channel 4 of TIM module 2
	LETH0_P0_MII_RMII_RXD 1A			LETH0 PortX MII and RMII receive data bit 1 (to be used with LETH0_P0_RXCLKA or LETH0_P0_REFCLKA)
	LETH1_P0_MII_RMII_RXD 1A			LETH1 PortX MII and RMII receive data bit 1 (to be used with LETH1_P0_RXCLKA or LETH1_P0_REFCLKA)
	LETH0_P0_RXDD			LETH PortX TC14 interface receive data input
	P11.9	O0		General-purpose output
	GTM_TOUT98	O1		GTM muxed output
	—	O2		Reserved
	QSPI1_MTSR	O3		Master SPI data output
	—	O4		Reserved
	MSC0_SOP	O5		Data output - direct part of the differential signal
	GPT121_T3OUT	O6		External output for overflow/underflow detection of core timer T3
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT98	O9		eGTM muxed output
	—	O10		Reserved
	LETH1_P0_MDC	O11		LETH PortX MDIO interface clock output
	—	O12		Reserved
	—	O13		Reserved

(table continues...)

Table 10 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_MDC	O14		LETH PortX MDIO interface clock output
	—	O15		Reserved
	LETH0_P0_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
E12	P11.10	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM2_IN0_9			Mux input channel 0 of TIM module 2
	GTM_TIM2_IN5_2			Mux input channel 5 of TIM module 2
	GTM_TIM3_IN5_2			Mux input channel 5 of TIM module 3
	CAN03_RXDD			CAN receive input node 3
	ERAY0_RXDB1			Receive Channel B1
	ASCLIN1_ARXE			Receive input
	SCU_E_REQ6B			ERU channel 6 input B
	MSC0_SDI0			Upstream asynchronous input signal
	QSPI1_SLSIA			Slave select input
	GPT121_T2INB			Trigger/gate input of timer T2
	CANXL01_RXDB			CANXL receive input node 1
	EGTM_TIM2_IN0_9			Mux input channel 0 of TIM module 2
	EGTM_TIM2_IN5_2			Mux input channel 5 of TIM module 2
	LETH0_P0_MII_RMII_RXD 0A			LETH0 PortX MII and RMII receive data bit 0 (to be used with LETH0_P0_RXCLKA or LETH0_P0_REFCLKA)
	LETH1_P0_MII_RMII_RXD 0A			LETH1 PortX MII and RMII receive data bit 0 (to be used with LETH1_P0_RXCLKA or LETH1_P0_REFCLKA)
	LETH1_P0_RXDD			LETH PortX TC14 interface receive data input
	P11.10	O0		General-purpose output
	GTM_TOUT99	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO3	O3		Master slave select output
	QSPI1_SLSO3	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT99	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 10 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	LETH0_P1_MDC	O14		LETH PortX MDIO interface clock output
	—	O15		Reserved
	LETH1_P0_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
D11	P11.11	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM2_IN6_2			Mux input channel 6 of TIM module 2
	GTM_TIM3_IN0_15			Mux input channel 0 of TIM module 3
	GTM_TIM3_IN6_2			Mux input channel 6 of TIM module 3
	LETH0_P1_MDIOA			LETH PortX MDIO interface data input
	GPT121_T2EUDB			Count direction control input of timer T2
	LETH0_P1_EDA			LETH PortX TC14 interface energy detection input
	EGTM_TIM2_IN6_2			Mux input channel 6 of TIM module 2
	LETH0_P0_CRSA			LETH PortX MII carrier sense
	LETH1_P0_CRSA			LETH PortX MII carrier sense
	P11.11	O0		General-purpose output
	GTM_TOUT100	O1		GTM muxed output
	—	O2		Reserved
	QSPIO_SLSO4	O3		Master slave select output
	QSPI1_SLSO4	O4		Master slave select output
	MSC0_EN0	O5		Chip Select
	ERAY0_TXENB	O6		Transmit Enable Channel B
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT100	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 10 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
E11	P11.12	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM2_IN7_2			Mux input channel 7 of TIM module 2
	GTM_TIM3_IN7_2			Mux input channel 7 of TIM module 3
	GPT121_T4EUIDB			Count direction control input of timer T4
	EGTM_TIM2_IN7_2			Mux input channel 7 of TIM module 2
	LETH0_P0_REFCLKA			LETH0 PortX RMII reference clock
	LETH0_P0_RXCLKA			LETH PortX MII receive clock
	LETH1_P0_REFCLKA			LETH PortX RMII reference clock
	LETH1_P0_RXCLKA			LETH PortX MII receive clock
	P11.12	O0		General-purpose output
	GTM_TOUT101	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	GTM_ECLK2	O3		CGM generated clock
	ERAY0_TXDB	O4		Transmit Channel B
	CAN03_TXD	O5		CAN transmit output node 3
	CLOCK_EXTCLK1	O6		External clock output 1
	—	O7		Reserved
	EGTM_ECLK2	O8		CGM generated clock
	EGTM_TOUT101	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P1_TXD	O11		LETH PortX TC14 interface transmit data output
	CANXL01_TXD	O12		CANXL transmit output node 1
	LETH1_P0_TXD	O13		LETH PortX TC14 interface transmit data output
	—	O14		Reserved
	—	O15		Reserved
H9	P11.13	I	SLOW / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM2_IN6_7			Mux input channel 6 of TIM module 2
	GTM_TIM4_IN6_5			Mux input channel 6 of TIM module 4
	I2C1_SDAA			Serial Data Input 0
	CAN13_RXDD			CAN receive input node 3
	CAN31_RXDA			CAN receive input node 1

(table continues...)

Table 10 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P0_MII_RXERA			LETH0 PortX MII receive error (to be used with LETH0_P0_RXCLKA)
	LETH1_P0_MII_RXERA			LETH1 PortX MII receive error (to be used with LETH1_P0_RXCLKA)
	EGTM_TIM2_IN6_7			Mux input channel 6 of TIM module 2
	LETH1_P0_RXDA			LETH PortX TC14 interface receive data input
	P11.13	O0		General-purpose output
	GTM_TOUT125	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	I2C1_SDA	O6		Serial Data Output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT125	O9		eGTM muxed output
	—	O10		Reserved
	LETH1_P0_MDC	O11		LETH PortX MDIO interface clock output
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH1_P0_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
G10	P11.14	I	SLOW / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM2_IN7_8			Mux input channel 7 of TIM module 2
	GTM_TIM4_IN7_4			Mux input channel 7 of TIM module 4
	I2C1_SCLA			Serial Clock Input 0
	CAN20_RXDF			CAN receive input node 0
	LETH0_P0_CRSB			LETH PortX MII carrier sense
	LETH1_P0_CRSB			LETH PortX MII carrier sense
	EGTM_TIM2_IN7_8			Mux input channel 7 of TIM module 2
	LETH0_P0_MII_RXDVA			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV

(table continues...)

Table 10 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH1_P0_MII_RXDVA			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	LETH0_P0_RMII_CRSDVA			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	LETH1_P0_RMII_CRSDVA			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	P11.14	O0		General-purpose output
	GTM_TOUT126	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	I2C1_SCL	O6		Serial Clock Output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT126	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
G9	P11.15	I	SLOW / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM0_IN7_8			Mux input channel 7 of TIM module 0
	GTM_TIM4_IN7_5			Mux input channel 7 of TIM module 4
	LETH1_P0_EDE			LETH PortX TC14 interface energy detection input
	LETH1_P0_MDIOE			LETH PortX MDIO interface data input
	LETH0_P0_COLA			LETH PortX MII collision detection
	LETH1_P0_COLA			LETH PortX MII collision detection
	EGTM_TIM0_IN7_8			Mux input channel 7 of TIM module 0
	P11.15	O0		General-purpose output
	GTM_TOUT127	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved

(table continues...)

Table 10 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT127	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH1_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface

3.2.6 BGA436_STD port 12

Table 11 Port 12 functions

Ball	Symbol	Ctrl.	Buffer type	Function
H15	P12.0	I	SLOW / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM3_IN0_7			Mux input channel 0 of TIM module 3
	GTM_TIM4_IN0_5			Mux input channel 0 of TIM module 4
	CAN00_RXDC			CAN receive input node 0
	LETH1_P0_EDA			LETH PortX TC14 interface energy detection input
	LETH1_P0_MDIOA			LETH PortX MDIO interface data input
	GTM_CDTM4_DTM4_1			Input mux of CDTM4_DTM4_AUXIN0/1
	GTM_CDTM4_DTM5_1			Input mux of CDTM4_DTM5_AUXIN0/1
	LETH1_P0_REFCLKC			LETH PortX RMII reference clock
	LETH1_P0_RXCLKC			LETH PortX MII receive clock
	P12.0	O0		General-purpose output
	GTM_TOUT128	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved

(table continues...)

Table 11 (continued) Port 12 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT128	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P0_MDC	O11		LETH PortX MDIO interface clock output
	LETH1_P0_MDC	O12		LETH PortX MDIO interface clock output
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH1_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
H14	P12.1	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM3_IN1_6			Mux input channel 1 of TIM module 3
	GTM_TIM4_IN1_6			Mux input channel 1 of TIM module 4
	LETH0_P0_MDIOE			LETH PortX MDIO interface data input
	LETH0_P0_EDE			LETH PortX TC14 interface energy detection input
	P12.1	O0		General-purpose output
	GTM_TOUT129	O1		GTM muxed output
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	CAN00_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT129	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved

(table continues...)

Table 11 (continued) Port 12 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface

3.2.7 BGA436_STD port 13

Table 12 Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
E15	P13.0	I	LVDS_TX / FAST / PU1 / VDDEXT HS / ES	General-purpose input
	GTM_TIM2_IN5_3			Mux input channel 5 of TIM module 2
	GTM_TIM3_IN5_3			Mux input channel 5 of TIM module 3
	QSPI2_MRSTG_F			Master SPI data input
	GPT121_T6INB			Trigger/gate input of core timer T6
	CAN11_RXDG			CAN receive input node 1
	EGTM_TIM2_IN5_3			Mux input channel 5 of TIM module 2
	P13.0	O0		General-purpose output
	GTM_TOUT91	O1		GTM muxed output
	—	O2		Reserved
	QSPI2_SCLKN_F	O3		Master SPI clock output (LVDS N line)
	MSC0_EN1	O4		Chip Select
	MSC0_FCLN	O5		Shift-clock inverted part of the differential signal
	—	O6		Reserved
	CAN10_TXD	O7		CAN transmit output node 0
	—	O8		Reserved
	EGTM_TOUT91	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P2_MIIC_TXD2	O12		LETH0 PortX MII transmit data bit 2 (to be used with LETH0_P2_TXCLKC)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 12 (continued) Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
D15	P13.1	I	LVDS_TX / FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM2_IN6_3			Mux input channel 6 of TIM module 2
	GTM_TIM3_IN6_3			Mux input channel 6 of TIM module 3
	I2C0_SCLB			Serial Clock Input 1
	CAN10_RXDD			CAN receive input node 0
	LETH1_P0_MDIOC			LETH PortX MDIO interface data input
	LETH1_P0_EDC			LETH PortX TC14 interface energy detection input
	QSPI2_SCLKC_F			Slave SPI clock inputs
	LETH0_P2_COLC			LETH PortX MII collision detection
	EGTM_TIM2_IN6_3			Mux input channel 6 of TIM module 2
	P13.1	O0		General-purpose output
	GTM_TOUT92	O1		GTM muxed output
	—	O2		Reserved
	QSPI2_SCLKP_F	O3		Master SPI clock output
	—	O4		Reserved
	MSC0_FCLP	O5		Shift-clock direct part of the differential signal
	I2C0_SCL	O6		Serial Clock Output
	GPT121_T6OUT	O7		External output for overflow/underflow detection of core timer T6
	QSPI2_SCLK_F	O8		Master SPI clock output
	EGTM_TOUT92	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH1_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
E14	P13.2	I	LVDS_TX / FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM2_IN7_3			Mux input channel 7 of TIM module 2
	GTM_TIM3_IN7_3			Mux input channel 7 of TIM module 3
	GPT120_CAPINA			Trigger input to capture value of timer T5 into CAPREL register (input A)

(table continues...)

Table 12 (continued) Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	I2C0_SDAB			Serial Data Input 1
	CAN33_RXDA			CAN receive input node 3
	LETH1_P0_COLB			LETH PortX MII collision detection
	GPT121_T6EUDB			Count direction control input of core timer T6
	LETH0_P2_CRSC			LETH PortX MII carrier sense
	EGTM_TIM2_IN7_3			Mux input channel 7 of TIM module 2
	P13.2	O0		General-purpose output
	GTM_TOUT93	O1		GTM muxed output
	—	O2		Reserved
	QSPI2_MTSRN_F	O3		Master SPI data output (LVDS N line)
	MSC0_FCLP	O4		Shift-clock direct part of the differential signal
	MSC0_SON	O5		Data output - inverted part of the differential signal
	I2C0_SDA	O6		Serial Data Output
	—	O7		Reserved
	QSPI2_MTSR_F	O8		Master SPI data output
	EGTM_TOUT93	O9		eGTM muxed output
	QSPI2_MRST_F	O10		Slave SPI data output
	—	O11		Reserved
	—	O12		Reserved
	LETH1_P0_TXD	O13		LETH PortX TC14 interface transmit data output
	—	O14		Reserved
	—	O15		Reserved
D14	P13.3	I	LVDS_TX / FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM2_IN0_3			Mux input channel 0 of TIM module 2
	GTM_TIM3_IN0_3			Mux input channel 0 of TIM module 3
	QSPI2_SLSIC_F			Slave select input
	EGTM_TIM2_IN0_3			Mux input channel 0 of TIM module 2
	LETH1_P0_RXDC			LETH PortX TC14 interface receive data input
	P13.3	O0		General-purpose output
	GTM_TOUT94	O1		GTM muxed output
	—	O2		Reserved
	QSPI2_MTSRP_F	O3		Master SPI data output
	ASCLIN7_ASLSO_F	O4		Slave select signal output

(table continues...)

Table 12 (continued) Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	MSC0_SOP	O5		Data output - direct part of the differential signal
	—	O6		Reserved
	CAN33_TXD	O7		CAN transmit output node 3
	QSPI2_SLSO3_F	O8		Master slave select output
	EGTM_TOUT94	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P2_MIIA_TXD3	O12		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P2_TXCLKA)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH1_P0_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
B14	P13.4	I	LVDS_TX / FAST / PU1 / VDDEXT HS / ES	General-purpose input
	GTM_TIM3_IN3_8			Mux input channel 3 of TIM module 3
	GTM_TIM5_IN3_4			Mux input channel 3 of TIM module 5
	GTM_TIM6_IN0_4			Mux input channel 0 of TIM module 6
	I2C0_SCLF			Serial Clock Input 5
	P13.4	O0		General-purpose output
	GTM_TOUT253	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	MSC2_EN0	O4		Chip Select
	MSC2_FCLN	O5		Shift-clock inverted part of the differential signal
	I2C0_SCL	O6		Serial Clock Output
	CAN23_TXD	O7		CAN transmit output node 3
	—	O8		Reserved
	EGTM_TOUT253	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved

(table continues...)

Table 12 (continued) Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O14		Reserved
	—	O15		Reserved
A14	P13.5	I	LVDS_TX / FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM3_IN4_9			Mux input channel 4 of TIM module 3
	GTM_TIM5_IN4_3			Mux input channel 4 of TIM module 5
	GTM_TIM6_IN1_4			Mux input channel 1 of TIM module 6
	CAN23_RXDD			CAN receive input node 3
	I2C0_SDAF			Serial Data Input 5
	P13.5	O0		General-purpose output
	GTM_TOUT254	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	MSC2_FCLP	O5		Shift-clock direct part of the differential signal
	I2C0_SDA	O6		Serial Data Output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT254	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
B13	P13.6	I	LVDS_TX / FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM3_IN5_10			Mux input channel 5 of TIM module 3
	GTM_TIM5_IN5_4			Mux input channel 5 of TIM module 5
	GTM_TIM6_IN2_4			Mux input channel 2 of TIM module 6
	CAN10_RXDF			CAN receive input node 0
	P13.6	O0		General-purpose output
	GTM_TOUT255	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—			

(table continues...)

Table 12 (continued) Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN7_ATX_F	O4		Transmit output
	MSC2_SON	O5		Data output - inverted part of the differential signal
	—	O6		Reserved
	—	O7		Reserved
	QSPI7_MTSR	O8		Master SPI data output
	EGTM_TOUT255	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
A13	P13.7	I	LVDS_TX / FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM3_IN6_10			Mux input channel 6 of TIM module 3
	GTM_TIM5_IN6_4			Mux input channel 6 of TIM module 5
	GTM_TIM6_IN3_4			Mux input channel 3 of TIM module 6
	P13.7	O0		General-purpose output
	GTM_TOUT256	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	—	O3		Reserved
	ASCLIN7_ASCLK_F	O4		Shift clock output
	MSC2_SOP	O5		Data output - direct part of the differential signal
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT256	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 12 (continued) Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
B16	P13.9	I	FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM2_IN7_10			Mux input channel 7 of TIM module 2
	GTM_TIM4_IN7_6			Mux input channel 7 of TIM module 4
	GTM_TIM6_IN4_4			Mux input channel 4 of TIM module 6
	I2C1_SCLB			Serial Clock Input 1
	CAN33_RXDE			CAN receive input node 3
	EGTM_TIM2_IN7_10			Mux input channel 7 of TIM module 2
	P13.9	O0		General-purpose output
	GTM_TOUT248	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	QSPI5_SLSO5	O3		Master slave select output
	PSI5S1_TX	O4		TX data output
	CAN21_TXD	O5		CAN transmit output node 1
	I2C1_SCL	O6		Serial Clock Output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT248	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	LETH0_P2_TXD	O13		LETH PortX TC14 interface transmit data output
	—	O14		Reserved
	—	O15		Reserved
B11	P13.10	I	FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM3_IN1_8			Mux input channel 1 of TIM module 3
	GTM_TIM5_IN1_5			Mux input channel 1 of TIM module 5
	GTM_TIM6_IN5_4			Mux input channel 5 of TIM module 6
	PSI5_RX3A			RXD inputs (receive data) channel 3
	QSPI5_MRSTH			Master SPI data input
	QSPI7_SCLKA			Slave SPI clock inputs
	LETH0_P2_RXDG			LETH PortX TC14 interface receive data input
	P13.10	O0		General-purpose output
	GTM_TOUT251	O1		GTM muxed output

(table continues...)

Table 12 (continued) Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN0_ATX	O2		Transmit output
	QSPI5_MRST	O3		Slave SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT251	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
A11	P13.11	I	SLOW / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM3_IN0_9			Mux input channel 0 of TIM module 3
	GTM_TIM5_IN0_9			Mux input channel 0 of TIM module 5
	GTM_TIM6_IN6_4			Mux input channel 6 of TIM module 6
	ASCLIN0_ARXE			Receive input
	ASCLIN7_ARXD_F			Receive input
	QSPI5_SLSIC			Slave select input
	P13.11	O0		General-purpose output
	GTM_TOUT250	O1		GTM muxed output
	—	O2		Reserved
	QSPI5_SLSO2	O3		Master slave select output
	PSI5_TX3	O4		TXD outputs (send data)
	MSC0_EN1	O5		Chip Select
	—	O6		Reserved
	CAN33_TXD	O7		CAN transmit output node 3
	—	O8		Reserved
	EGTM_TOUT250	O9		eGTM muxed output

(table continues...)

Table 12 (continued) Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P2_MIIC_TXER	O12		LETH0 PortX MII transmit error (to be used with LETH0_P2_TXCLKC)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
B10	P13.12	I	SLOW / PU1 / VDDEXT S / ES	General-purpose input
	GTM_TIM0_IN0_11			Mux input channel 0 of TIM module 0
	GTM_TIM4_IN0_6			Mux input channel 0 of TIM module 4
	GTM_TIM6_IN7_4			Mux input channel 7 of TIM module 6
	ASCLIN3_ARXH			Receive input
	I2C1_SDAB			Serial Data Input 1
	CAN21_RXDB			CAN receive input node 1
	I2C1_SDAF			Serial Data Input 5
	EGTM_TIM0_IN0_11			Mux input channel 0 of TIM module 0
	P13.12	O0		General-purpose output
	GTM_TOUT249	O1		GTM muxed output
	ASCLIN7_ATX	O2		Transmit output
	QSPI5_SLSO1	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	I2C1_SDA	O6		Serial Data Output
	—	O7		Reserved
	I2C1_SDA	O8		Serial Data Output
	EGTM_TOUT249	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P2_MIIC_TXD3	O12		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P2_TXCLKC)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 12 (continued) Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
A10	P13.13	I	SLOW / PU1 / VDDEXT S / ES	General-purpose input
	GTM_TIM3_IN5_9			Mux input channel 5 of TIM module 3
	GTM_TIM5_IN5_5			Mux input channel 5 of TIM module 5
	MSC2_INJ0			Injection signal from port
	PSI5_RX3B			RXD inputs (receive data) channel 3
	I2C1_SCLF			Serial Clock Input 5
	CAN33_RXDD			CAN receive input node 3
	P13.13	O0		General-purpose output
	GTM_TOUT262	O1		GTM muxed output
	ASCLIN7_ASCLK	O2		Shift clock output
	QSPI5_SLSO0	O3		Master slave select output
	PSI5S1_CLK	O4		PSI5S CLK is a clock that can be used on a pin to drive the external PHY.
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	I2C1_SCL	O8		Serial Clock Output
	EGTM_TOUT262	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P2_MIIC_TXD2	O12		LETH0 PortX MII transmit data bit 2 (to be used with LETH0_P2_TXCLKC)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
B8	P13.14	I	SLOW / PU1 / VDDEXT S / ES	General-purpose input
	GTM_TIM3_IN2_7			Mux input channel 2 of TIM module 3
	GTM_TIM5_IN2_4			Mux input channel 2 of TIM module 5
	QSPI5_MTSRC			Slave SPI data input
	P13.14	O0		General-purpose output
	GTM_TOUT252	O1		GTM muxed output
	—	O2		Reserved
	QSPI5_MTSR	O3		Master SPI data output

(table continues...)

Table 12 (continued) Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	QSPI5_SLSO4	O8		Master slave select output
	EGTM_TOUT252	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
A8	P13.15	I	SLOW / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM3_IN7_9			Mux input channel 7 of TIM module 3
	GTM_TIM5_IN7_4			Mux input channel 7 of TIM module 5
	QSPI5_SCLKD			Slave SPI clock inputs
	P13.15	O0		General-purpose output
	GTM_TOUT264	O1		GTM muxed output
	ASCLIN7_ASLSO	O2		Slave select signal output
	QSPI5_SCLK	O3		Master SPI clock output
	PSI5_TX3	O4		TXD outputs (send data)
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT264	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

3.2.8 BGA436_STD port 14

Table 13 Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
E19	P14.0	I	FAST / PU1 / VDDEXTHS / ES2	General-purpose input
	GTM_TIM0_IN3_5			Mux input channel 3 of TIM module 0
	GTM_TIM1_IN3_5			Mux input channel 3 of TIM module 1
	SENT1_SENT8D			Receive input channel 8
	LETH0_P2_EDH			LETH PortX TC14 interface energy detection input
	LETH0_P2_MDIOH			LETH PortX MDIO interface data input
	EGTM_TIM0_IN3_5			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_5			Mux input channel 3 of TIM module 1
	LETH0_P2_REFCLKA			LETH0 PortX RMII reference clock
	LETH0_P2_RXCLKA			LETH PortX MII receive clock
	LETH0_P2_REFCLKC			LETH PortX RMII reference clock
	LETH0_P2_RXCLKC			LETH PortX MII receive clock
	P14.0	O0		General-purpose output
	GTM_TOUT80	O1		GTM muxed output
	ASCLIN0_ATX_F	O2		Transmit output
	ERAY0_TXDA	O3		Transmit Channel A
	ERAY0_TXDB	O4		Transmit Channel B
	CAN01_TXD	O5		CAN transmit output node 1
	ASCLIN0_ASCLK_F	O6		Shift clock output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT80	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P0_TXD	O12		LETH PortX TC14 interface transmit data output
	CANXL00_TXD	O13		CANXL transmit output node 0
	LETH0_P1_TXD	O14		LETH PortX TC14 interface transmit data output
	CANXL01_TXD	O15		CANXL transmit output node 1
	EGTM_HRPWM1_CH0	PO		High resolution PWM 1 output channels
	LETH0_P2_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface

(table continues...)

Table 13 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
D18	P14.1	I	FAST / PU1 / VDDEXTH S / ES2	General-purpose input
	GTM_TIM0_IN4_3			Mux input channel 4 of TIM module 0
	GTM_TIM1_IN4_3			Mux input channel 4 of TIM module 1
	ERAY0_RXDA3			Receive Channel A3
	ASCLIN0_ARXA_F			Receive input
	SENT0_SENT9D			Receive input channel 9
	ERAY0_RXDB3			Receive Channel B3
	CAN01_RXDB			CAN receive input node 1
	SCU_E_REQ3B			ERU channel 3 input B
	CANXL00_RXDB			CANXL receive input node 0
	EGTM_TIM0_IN4_3			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_3			Mux input channel 4 of TIM module 1
	PMS_PINAWKP			PINA (P14.1) pin input
	LETH0_P2_MII_RMII_RXD 0A			LETH0 PortX MII and RMII receive data bit 0 (to be used with LETH0_P2_RXCLKA or LETH0_P2_REFCLKA)
	LETH0_P2_MII_RMII_RXD 0C			LETH0 PortX MII and RMII receive data bit 0 (to be used with LETH0_P2_RXCLKC or LETH0_P2_REFCLKC)
	LETH0_P0_RXDB			LETH PortX TC14 interface receive data input
	P14.1	O0		General-purpose output
	GTM_TOUT81	O1		GTM muxed output
	ASCLIN0_ATX_F	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT81	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved

(table continues...)

Table 13 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O15		Reserved
	EGTM_HRPWM1_CH1	PO		High resolution PWM 1 output channels
	LETH0_P0_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
H16	P14.2	I	SLOW / PU2 / VDDEXTH S / ES	General-purpose input
	GTM_TIM0_IN5_3			Mux input channel 5 of TIM module 0
	GTM_TIM1_IN5_3			Mux input channel 5 of TIM module 1
	CANXL01_RXDD			CANXL receive input node 1
	LETH0_P2_MII_RXERA			LETH0 PortX MII receive error (to be used with LETH0_P2_RXCLKA)
	LETH0_P2_MII_RXERC			LETH0 PortX MII receive error (to be used with LETH0_P2_RXCLKC)
	EGTM_TIM0_IN5_3			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_3			Mux input channel 5 of TIM module 1
	PMS_HWCFG2IN			HWCFG2 pin input
	LETH0_P1_RXDD			LETH PortX TC14 interface receive data input
	P14.2	O0		General-purpose output
	GTM_TOUT82	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	QSPI2_SLSO1	O3		Master slave select output
	—	O4		Reserved
	ASCLIN0_ASLSO	O5		Slave select signal output
	ASCLIN2_ASCLK	O6		Shift clock output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT82	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	LETH0_P0_PPS	O13		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 13 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
E17	P14.3	I	SLOW / PU2 / VDDEXT S / ES	General-purpose input
	GTM_TIM0_IN6_3			Mux input channel 6 of TIM module 0
	GTM_TIM1_IN6_3			Mux input channel 6 of TIM module 1
	ASCLIN2_ARXA			Receive input
	MSC0_SDI2			Upstream asynchronous input signal
	SCU_E_REQ1A			ERU channel 1 input A
	LETH0_P1_EDB			LETH PortX TC14 interface energy detection input
	LETH0_P1_MDIOB			LETH PortX MDIO interface data input
	EGTM_TIM0_IN6_3			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN6_3			Mux input channel 6 of TIM module 1
	PMS_HWCFG3IN			HWCFG3 pin input
	LETH0_P2_MII_RMII_RXD1A			LETH0 PortX MII and RMII receive data bit 1 (to be used with LETH0_P2_RXCLKA or LETH0_P2_REFCLKA)
	LETH0_P2_MII_RMII_RXD1C			LETH0 PortX MII and RMII receive data bit 1 (to be used with LETH0_P2_RXCLKC or LETH0_P2_REFCLKC)
	P14.3	O0		General-purpose output
	GTM_TOUT83	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	QSPI2_SLSO3	O3		Master slave select output
	ASCLIN1_ASLSO	O4		Slave select signal output
	ASCLIN3_ASLSO	O5		Slave select signal output
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT83	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P1_TXD	O12		LETH PortX TC14 interface transmit data output
	CANXL01_TXD	O13		CANXL transmit output node 1
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 13 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
E18	P14.4	I	SLOW / PU2 / VDDEXT S / ES	General-purpose input
	GTM_TIM0_IN7_2			Mux input channel 7 of TIM module 0
	GTM_TIM1_IN7_2			Mux input channel 7 of TIM module 1
	CANXL01_RXDA			CANXL receive input node 1
	GTM_CDTM0_DTM0_1			Input mux of CDTM0_DTM0_AUXIN0/1
	GTM_CDTM0_DTM1_1			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM0_DTM0_1			Input mux of CDTM0_DTM0_AUXIN0/1
	EGTM_CDTM0_DTM1_1			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM0_DTM2_1			Input mux of CDTM0_DTM2_AUXIN0/1
	EGTM_CDTM0_DTM3_1			Input mux of CDTM0_DTM3_AUXIN0/1
	LETH0_P1_MII_RXERA			LETH0 PortX MII receive error (to be used with LETH0_P1_RXCLKA)
	EGTM_TIM0_IN7_2			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_2			Mux input channel 7 of TIM module 1
	PMS_HWC6G6IN			HWC6G6 pin input
	LETH0_P1_RXDA			LETH PortX TC14 interface receive data input
	P14.4	O0		General-purpose output
	GTM_TOUT84	O1		GTM muxed output
	GPT123_T3OUT	O2		External output for overflow/underflow detection of core timer T3
	ASCLIN0_ARTS	O3		Ready to send output
	QSPI2_SLSO4	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT84	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIA_TXD3	O11		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P2_TXCLKA)
	LETH0_P2_MIIC_TXD3	O12		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P2_TXCLKC)

(table continues...)

Table 13 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
D17	P14.5	I	FAST / PU2 / VDDEXTH S / ES	General-purpose input
	GTM_TIM0_IN0_4			Mux input channel 0 of TIM module 0
	GTM_TIM1_IN0_4			Mux input channel 0 of TIM module 1
	QSPI5_MRSTB			Master SPI data input
	GTM_CDTM2_DTM4_1			Input mux of CDTM2_DTM4_AUXIN0/1
	GTM_CDTM2_DTM5_1			Input mux of CDTM2_DTM5_AUXIN0/1
	EGTM_CDTM2_DTM4_1			Input mux of CDTM2_DTM4_AUXIN0/1
	EGTM_CDTM2_DTM5_1			Input mux of CDTM2_DTM5_AUXIN0/1
	LETH0_P2_MII_RXD3C			LETH0 PortX MII receive data bit 3 (to be used with LETH0_P2_RXCLKC)
	EGTM_TIM0_IN0_4			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_4			Mux input channel 0 of TIM module 1
	PMS_HWCFG1IN			HWCFG1 pin input
	P14.5	O0		General-purpose output
	GTM_TOUT85	O1		GTM muxed output
	ASCLIN0_ATX_F	O2		Transmit output
	QSPI5_MRST	O3		Slave SPI data output
	QSPI2_SLSO4_F	O4		Master slave select output
	—	O5		Reserved
	ERAY0_TXDB	O6		Transmit Channel B
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT85	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_TXD	O11		LETH PortX TC14 interface transmit data output
	LETH0_P1_TXD	O12		LETH PortX TC14 interface transmit data output
	CANXL01_TXD	O13		CANXL transmit output node 1
	—	O14		Reserved

(table continues...)

Table 13 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O15		Reserved
	EGTM_HRPWM1_CH2	PO		High resolution PWM 1 output channels
E16	P14.6	I	FAST / PU1 / VDDEXT S / ES	General-purpose input
	GTM_TIM0_IN1_4			Mux input channel 1 of TIM module 0
	GTM_TIM1_IN1_4			Mux input channel 1 of TIM module 1
	QSPI5_MTSRB			Slave SPI data input
	LETH0_P2_EDC			LETH PortX TC14 interface energy detection input
	GPT123_T3INB			Trigger/gate input of core timer T3 (input A, B and C)
	LETH0_P2_MDIOC			LETH PortX MDIO interface data input
	LETH0_P2_MII_RXD2C			LETH0 PortX MII receive data bit 2 (to be used with LETH0_P2_RXCLKC)
	EGTM_TIM0_IN1_4			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_4			Mux input channel 1 of TIM module 1
	P14.6	O0		General-purpose output
	GTM_TOUT86	O1		GTM muxed output
	QSPI5_MTSR	O2		Master SPI data output
	QSPI2_SLSO2_F	O3		Master slave select output
	CAN13_TXD	O4		CAN transmit output node 3
	ASCLIN0_ASLSO_F	O5		Slave select signal output
	ERAY0_TXENB	O6		Transmit Enable Channel B
	—	O7		Reserved
	ASCLIN0_ATX_F	O8		Transmit output
	EGTM_TOUT86	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM1_CH3	PO		High resolution PWM 1 output channels
	LETH0_P2_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
G16	P14.7	I	FAST / PU1 /	General-purpose input

(table continues...)

Table 13 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TIM0_IN0_5		VDDEXTH S / ES	Mux input channel 0 of TIM module 0
	GTM_TIM1_IN0_5			Mux input channel 0 of TIM module 1
	GTM_TIM4_IN7_10			Mux input channel 7 of TIM module 4
	ERAY0_RXDB0			Receive Channel B0
	CAN10_RXDB			CAN receive input node 0
	CAN13_RXDA			CAN receive input node 3
	QSPI7_MTSRA			Slave SPI data input
	EGTM_TIM0_IN0_5			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_5			Mux input channel 0 of TIM module 1
	LETH0_P2_RXDC			LETH PortX TC14 interface receive data input
	P14.7	O0		General-purpose output
	GTM_TOUT87	O1		GTM muxed output
	ASCLIN0_ARTS_F	O2		Ready to send output
	QSPI2_SLSO4_F	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT87	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIA_TXEN	O11		LETH0 PortX MII transmit enable (to be used with LETH0_P2_TXCLKA)
	LETH0_P2_MIIC_TXEN	O12		LETH0 PortX MII transmit enable (to be used with LETH0_P2_TXCLKC)
	LETH0_P2_RMIIA_TXEN	O13		LETH0 PortX RMII transmit enable (to be used with LETH0_P2_REFCLKA)
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_RMIIRA_TXEN	PO		LETH0 PortX RMII transmit enable (to be used with LETH0_P2_REFCLKA - registered*)
	LETH0_P2_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface

(table continues...)

Table 13 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
D16	P14.8	I	FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM2_IN2_3			Mux input channel 2 of TIM module 2
	GTM_TIM3_IN2_3			Mux input channel 2 of TIM module 3
	ERAY0_RXDA0			Receive Channel A0
	CAN02_RXDD			CAN receive input node 2
	ASCLIN1_ARXD			Receive input
	GPT123_T3EUDB			Count direction control input of core timer T3
	CANXL00_RXDA			CANXL receive input node 0
	QSPI7_MRSTA			Master SPI data input
	EGTM_TIM2_IN2_3			Mux input channel 2 of TIM module 2
	LETH0_P0_RXDA			LETH PortX TC14 interface receive data input
	LETH0_P2_TXCLKA			LETH PortX MII transmit clock
	LETH0_P2_TXCLKC			LETH PortX MII transmit clock
	P14.8	O0		General-purpose output
	GTM_TOUT88	O1		GTM muxed output
	ASCLIN5_ASLSO	O2		Slave select signal output
	ASCLIN7_ASLSO	O3		Slave select signal output
	ASCLIN0_ASLSO	O4		Slave select signal output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT88	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
G15	P14.9	I	LVDS_RX / FAST / PU1 /	General-purpose input
	GTM_TIM2_IN3_3			Mux input channel 3 of TIM module 2

(table continues...)

Table 13 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TIM3_IN3_3		VDDEXTH S / ES	Mux input channel 3 of TIM module 3
	ASCLIN0_ACTSA_F			Clear to send input
	QSPI2_MRSTFN_F			Master SPI data input
	LETH0_P0_EDA			LETH PortX TC14 interface energy detection input
	LETH0_P0_MDIOA			LETH PortX MDIO interface data input
	EGTM_TIM2_IN3_3			Mux input channel 3 of TIM module 2
	P14.9	O0		General-purpose output
	GTM_TOUT89	O1		GTM muxed output
	CAN23_TXD	O2		CAN transmit output node 3
	MSC0_EN1	O3		Chip Select
	CAN10_TXD	O4		CAN transmit output node 0
	ERAY0_TXENB	O5		Transmit Enable Channel B
	ERAY0_TXENA	O6		Transmit Enable Channel A
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT89	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIA_TXD1	O11		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P2_TXCLKA)
	LETH0_P2_MIIC_TXD1	O12		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P2_TXCLKC)
	LETH0_P2_RMIIA_TXD1	O13		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P2_REFCLKA)
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_RMIIRA_TXD1	PO		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P2_REFCLKA - registered*)
	LETH0_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
G14	P14.10	I	LVDS_RX / FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM2_IN4_3			Mux input channel 4 of TIM module 2
	GTM_TIM3_IN4_3			Mux input channel 4 of TIM module 3
	CAN23_RXDA			CAN receive input node 3
	QSPI2_MRSTFP_F			Master SPI data input

(table continues...)

Table 13 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GPT123_T4INB			Trigger/gate input of timer T4
	EGTM_TIM2_IN4_3			Mux input channel 4 of TIM module 2
	P14.10	O0		General-purpose output
	GTM_TOUT90	O1		GTM muxed output
	QSPI5_SCLK	O2		Master SPI clock output
	MSC0_EN0	O3		Chip Select
	ASCLIN1_ATX	O4		Transmit output
	CAN02_TXD	O5		CAN transmit output node 2
	ERAY0_TXDA	O6		Transmit Channel A
	—	O7		Reserved
	LETH0_P2_RMIIA_TXD0	O8		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P2_REFCLKA)
	EGTM_TOUT90	O9		eGTM muxed output
	LETH0_P2_MIIA_TXD0	O10		LETH0 PortX MII transmit data bit 0 (to be used with LETH0_P2_TXCLKA)
	LETH0_P2_MIIC_TXD0	O11		LETH0 PortX MII transmit data bit 0 (to be used with LETH0_P2_TXCLKC)
	LETH0_P0_TXD	O12		LETH PortX TC14 interface transmit data output
	CANXL00_TXD	O13		CANXL transmit output node 0
	LETH0_P2_TXD	O14		LETH PortX TC14 interface transmit data output
	—	O15		Reserved
	LETH0_P2_RMIIRA_TXD0	PO		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P2_REFCLKA - registered*)
A19	P14.11	I	SLOW / PU1 / VDDEXT S / ES	General-purpose input
	GTM_TIM3_IN1_9			Mux input channel 1 of TIM module 3
	GTM_TIM5_IN1_4			Mux input channel 1 of TIM module 5
	MSC2_SDI1			Upstream asynchronous input signal
	MSC0_SDI4			Upstream asynchronous input signal
	P14.11	O0		General-purpose output
	GTM_TOUT258	O1		GTM muxed output
	CAN23_TXD	O2		CAN transmit output node 3
	—	O3		Reserved
	MSC2_EN2	O4		Chip Select
	MSC2_SOP	O5		Data output - direct part of the differential signal

(table continues...)

Table 13 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT258	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIA_TXER	O11		LETH0 PortX MII transmit error (to be used with LETH0_P2_TXCLKA)
	LETH0_P2_MIIC_TXER	O12		LETH0 PortX MII transmit error (to be used with LETH0_P2_TXCLKC)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
B19	P14.12	I	SLOW / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM3_IN4_8			Mux input channel 4 of TIM module 3
	GTM_TIM5_IN4_4			Mux input channel 4 of TIM module 5
	GTM_TIM6_IN4_3			Mux input channel 4 of TIM module 6
	MSC2_SDI0			Upstream asynchronous input signal
	CANXL00_RXDH			CANXL receive input node 0
	LETH0_P0_RXDH			LETH PortX TC14 interface receive data input
	P14.12	O0		General-purpose output
	GTM_TOUT261	O1		GTM muxed output
	ASCLIN5_ASCLK	O2		Shift clock output
	ASCLIN7_ASCLK	O3		Shift clock output
	—	O4		Reserved
	—	O5		Reserved
	QSPI5_SLSO6	O6		Master slave select output
	—	O7		Reserved
	QSPI7_SLSO4	O8		Master slave select output
	EGTM_TOUT261	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIA_TXD3	O11		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P2_TXCLKA)
	LETH0_P2_MIIC_TXD3	O12		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P2_TXCLKC)

(table continues...)

Table 13 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
A17	P14.13	I	FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM3_IN3_6			Mux input channel 3 of TIM module 3
	GTM_TIM5_IN3_5			Mux input channel 3 of TIM module 5
	GTM_TIM6_IN5_3			Mux input channel 5 of TIM module 6
	QSPI5_SCLKB			Slave SPI clock inputs
	LETH0_P0_MDIOG			LETH PortX MDIO interface data input
	LETH0_P0_EDG			LETH PortX TC14 interface energy detection input
	P14.13	O0		General-purpose output
	GTM_TOUT260	O1		GTM muxed output
	—	O2		Reserved
	QSPI5_SCLK	O3		Master SPI clock output
	MSC2_EN1	O4		Chip Select
	CAN22_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	ASCLIN0_ATX_F	O7		Transmit output
	QSPI7_SLSO3	O8		Master slave select output
	EGTM_TOUT260	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIA_TXD2	O11		LETH0 PortX MII transmit data bit 2 (to be used with LETH0_P2_TXCLKA)
	LETH0_P2_MIIC_TXD2	O12		LETH0 PortX MII transmit data bit 2 (to be used with LETH0_P2_TXCLKC)
	—	O13		Reserved
	MSC0_EN1	O14		Chip Select
	—	O15		Reserved
	LETH0_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
B17	P14.14	I	FAST / PU1 /	General-purpose input
	GTM_TIM3_IN2_8			Mux input channel 2 of TIM module 3

(table continues...)

Table 13 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TIM5_IN2_3		VDDEXTH S / ES	Mux input channel 2 of TIM module 5
	GTM_TIM6_IN6_3			Mux input channel 6 of TIM module 6
	CAN22_RXDD			CAN receive input node 2
	LETH0_P2_MII_RXD2A			LETH0 PortX MII receive data bit 2 (to be used with LETH0_P2_RXCLKA)
	P14.14	O0		General-purpose output
	GTM_TOUT259	O1		GTM muxed output
	ASCLIN5_ATX	O2		Transmit output
	ASCLIN7_ATX_F	O3		Transmit output
	MSC2_EN0	O4		Chip Select
	CAN23_TXD	O5		CAN transmit output node 3
	QSPI5_SLSO7	O6		Master slave select output
	ASCLIN0_ASCLK_F	O7		Shift clock output
	QSPI7_SLSO6	O8		Master slave select output
	EGTM_TOUT259	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	MSC0_EN0	O14		Chip Select
	LETH0_P1_MDC	O15		LETH PortX MDIO interface clock output
A16	P14.15	I	SLOW / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM3_IN6_9			Mux input channel 6 of TIM module 3
	GTM_TIM5_IN6_5			Mux input channel 6 of TIM module 5
	GTM_TIM6_IN7_3			Mux input channel 7 of TIM module 6
	MSC2_INJ1			Injection signal from port
	ASCLIN5_ARXD			Receive input
	ASCLIN7_ARXA_F			Receive input
	CAN23_RXDC			CAN receive input node 3
	LETH0_P2_MII_RXD3A			LETH0 PortX MII receive data bit 3 (to be used with LETH0_P2_RXCLKA)
	P14.15	O0		General-purpose output
	GTM_TOUT263	O1		GTM muxed output

(table continues...)

Table 13 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN1_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	QSPI5_SLSO8	O6		Master slave select output
	—	O7		Reserved
	QSPI7_SLSO7	O8		Master slave select output
	EGTM_TOUT263	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

3.2.9 BGA436_STD port 15

Table 14 Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
E23	P15.0	I	FAST / PU1 / VDDEXT S / ES	General-purpose input
	GTM_TIM2_IN3_4			Mux input channel 3 of TIM module 2
	GTM_TIM3_IN3_4			Mux input channel 3 of TIM module 3
	SDMMC0_DAT7_IN			Read data in
	GPT123_T2INB			Trigger/gate input of timer T2
	EGTM_TIM2_IN3_4			Mux input channel 3 of TIM module 2
	LETH0_P1_REFCLKA			LETH PortX RMII reference clock
	LETH0_P1_RXCLKA			LETH PortX MII receive clock
	P15.0	O0		General-purpose output
	GTM_TOUT71	O1		GTM muxed output
	ASCLIN1_ATX_F	O2		Transmit output
	QSPI0_SLSO13	O3		Master slave select output
	—	O4		Reserved
	CAN02_TXD	O5		CAN transmit output node 2

(table continues...)

Table 14 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN1_ASCLK_F	O6		Shift clock output
	—	O7		Reserved
	LETH0_P0_TXD	O8		LETH PortX TC14 interface transmit data output
	EGTM_TOUT71	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM1_CH4	PO		High resolution PWM 1 output channels
	SDMMC0_DAT7	O		Write data out
D21	P15.1	I	FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM2_IN4_4			Mux input channel 4 of TIM module 2
	GTM_TIM3_IN4_4			Mux input channel 4 of TIM module 3
	CAN02_RXDA			CAN receive input node 2
	ASCLIN1_ARXA_F			Receive input
	QSPI2_SLSIB			Slave select input
	SCU_E_REQ7B			ERU channel 7 input B
	GPT123_T2EUDB			Count direction control input of timer T2
	EGTM_TIM2_IN4_4			Mux input channel 4 of TIM module 2
	LETH0_P0_RXDE			LETH PortX TC14 interface receive data input
	LETH0_P1_MII_RXDVA			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	LETH0_P1_RMII_CRSDVA			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	P15.1	O0		General-purpose output
	GTM_TOUT72	O1		GTM muxed output
	ASCLIN1_ATX_F	O2		Transmit output
	QSPI2_SLSO5	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved

(table continues...)

Table 14 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SDMMC0_CLK	O7		Card clock
	—	O8		Reserved
	EGTM_TOUT72	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM1_CH5	PO		High resolution PWM 1 output channels
F22	P15.2	I	FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM2_IN5_4			Mux input channel 5 of TIM module 2
	GTM_TIM3_IN5_4			Mux input channel 5 of TIM module 3
	QSPI2_SLSIA			Slave select input
	SENT0_SENT5D			Receive input channel 5
	QSPI2_MRSTE			Master SPI data input
	GPT123_T4EUDB			Count direction control input of timer T4
	EGTM_TIM2_IN5_4			Mux input channel 5 of TIM module 2
	XSPIO_RXD3B			Receive data
	LETH0_P1_TXCLKA			LETH PortX MII transmit clock
	P15.2	O0		General-purpose output
	GTM_TOUT73	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	QSPI2_SLSO0	O3		Master slave select output
	ASCLIN1_ATX_F	O4		Transmit output
	CAN01_TXD	O5		CAN transmit output node 1
	ASCLIN0_ASCLK	O6		Shift clock output
	QSPI7_SCLK_F	O7		Master SPI clock output
	ASCLIN1_ASLSO_F	O8		Slave select signal output
	EGTM_TOUT73	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved

(table continues...)

Table 14 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPIO_TXDB3	O		Transmit data
E20	P15.3	I	FAST / PU1 / VDDEXT S / ES	General-purpose input
	GTM_TIM2_IN6_4			Mux input channel 6 of TIM module 2
	GTM_TIM3_IN6_4			Mux input channel 6 of TIM module 3
	CAN01_RXDA			CAN receive input node 1
	ASCLIN0_ARXB			Receive input
	QSPI2_SCLKA			Slave SPI clock inputs
	SDMMC0_CMD_IN			Command in
	GPT123_T5EUDB			Count direction control input of timer T5
	ASCLIN1_ACTSC_F			Clear to send input
	QSPI7_SCLKC_F			Slave SPI clock inputs
	EGTM_TIM2_IN6_4			Mux input channel 6 of TIM module 2
	LETH0_P2_MII_RXDVC			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	LETH0_P2_RMII_CRSDVC			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	P15.3	O0		General-purpose output
	GTM_TOUT74	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	MSC0_EN1	O5		Chip Select
	—	O6		Reserved
	QSPI7_SCLK_F	O7		Master SPI clock output
	—	O8		Reserved
	EGTM_TOUT74	O9		eGTM muxed output
	LETH0_P1_MIIA_TXER	O10		LETH0 PortX MII transmit error (to be used with LETH0_P1_TXCLKA)
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved

(table continues...)

Table 14 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM1_CH6	PO		High resolution PWM 1 output channels
	SDMMC0_CMD	O		Command out
D20	P15.4	I	FAST / PU1 / VDDEXT S / ES	General-purpose input
	GTM_TIM2_IN7_4			Mux input channel 7 of TIM module 2
	GTM_TIM3_IN7_4			Mux input channel 7 of TIM module 3
	I2C0_SCLC			Serial Clock Input 2
	QSPI2_MRSTA			Master SPI data input
	SCU_E_REQ0A			ERU channel 0 input A
	SENT1_SENT5D			Receive input channel 5
	GPT123_T5INB			Trigger/gate input of timer T5
	QSPI7_MRSTF_F			Master SPI data input
	EGTM_TIM2_IN7_4			Mux input channel 7 of TIM module 2
	P15.4	O0		General-purpose output
	GTM_TOUT75	O1		GTM muxed output
	ASCLIN1_ATX_F	O2		Transmit output
	QSPI2_MRST	O3		Slave SPI data output
	—	O4		Reserved
	—	O5		Reserved
	I2C0_SCL	O6		Serial Clock Output
	QSPI7_MTSR_F	O7		Master SPI data output
	QSPI7_MRST_F	O8		Slave SPI data output
	EGTM_TOUT75	O9		eGTM muxed output
	LETH0_P1_MIIA_TXEN	O10		LETH0 PortX MII transmit enable (to be used with LETH0_P1_TXCLKA)
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	LETH0_P1_RMIIA_TXEN	O15		LETH0 PortX RMII transmit enable (to be used with LETH0_P1_REFCLKA)
H17	P15.5	I	FAST / PU1 /	General-purpose input

(table continues...)

Table 14 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TIM2_IN0_4		VDDEXT HS / ES	Mux input channel 0 of TIM module 2
	GTM_TIM3_IN0_4			Mux input channel 0 of TIM module 3
	ASCLIN1_ARXB_F			Receive input
	I2C0_SDAC			Serial Data Input 2
	QSPI2_MTSRA			Slave SPI data input
	SCU_E_REQ4D			ERU channel 4 input D
	QSPI7_MTSRE_F			Slave SPI data input
	GPT123_T6INB			Trigger/gate input of core timer T6
	EGTM_TIM2_IN0_4			Mux input channel 0 of TIM module 2
	P15.5	O0		General-purpose output
	GTM_TOUT76	O1		GTM muxed output
	ASCLIN1_ATX_F	O2		Transmit output
	QSPI2_MTSR	O3		Master SPI data output
	—	O4		Reserved
	MSC0_EN0	O5		Chip Select
	I2C0_SDA	O6		Serial Data Output
	LETH0_P1_TXD	O7		LETH PortX TC14 interface transmit data output
	LETH0_P0_TXD	O8		LETH PortX TC14 interface transmit data output
	EGTM_TOUT76	O9		eGTM muxed output
	LETH0_P1_MIIA_TXD0	O10		LETH0 PortX MII transmit data bit 0 (to be used with LETH0_P1_TXCLKA)
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	LETH0_P1_RMIIA_TXD0	O15		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P1_REFCLKA)
	EGTM_HRPWM1_CH7	PO		High resolution PWM 1 output channels
D19	P15.6	I	FAST / PU1 / VDDEXT HS / ES	General-purpose input
	GTM_TIM0_IN0_6			Mux input channel 0 of TIM module 0
	GTM_TIM1_IN0_6			Mux input channel 0 of TIM module 1
	GTM_TIM2_IN2_10			Mux input channel 2 of TIM module 2
	QSPI2_MTSRB			Slave SPI data input

(table continues...)

Table 14 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_MDIOG			LETH PortX MDIO interface data input
	GPT123_T6EUDB			Count direction control input of core timer T6
	LETH0_P1_EDG			LETH PortX TC14 interface energy detection input
	EGTM_TIM0_IN0_6			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_6			Mux input channel 0 of TIM module 1
	EGTM_TIM2_IN2_10			Mux input channel 2 of TIM module 2
	LETH0_P1_MII_RMII_RXD 1A			LETH0 PortX MII and RMII receive data bit 1 (to be used with LETH0_P1_RXCLKA or LETH0_P1_REFCLKA)
	P15.6	O0		General-purpose output
	GTM_TOUT77	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	QSPI2_MTSR	O3		Master SPI data output
	QSPI5_SLSO3	O4		Master slave select output
	QSPI2_SCLK	O5		Master SPI clock output
	ASCLIN3_ASCLK	O6		Shift clock output
	QSPI7_MTSR_F	O7		Master SPI data output
	ASCLIN1_ASLSO_F	O8		Slave select signal output
	EGTM_TOUT77	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
G18	P15.7	I	FAST / PU1 / VDDEXT HS / ES	General-purpose input
	GTM_TIM0_IN1_5			Mux input channel 1 of TIM module 0
	GTM_TIM1_IN1_5			Mux input channel 1 of TIM module 1
	ASCLIN3_ARXA			Receive input
	QSPI2_MRSTB			Master SPI data input
	GPT123_CAPINB3			Trigger input to capture value of timer T5 into CAPREL register (input B)
	QSPI7_MRSTE_F			Master SPI data input

(table continues...)

Table 14 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM0_IN1_5			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_5			Mux input channel 1 of TIM module 1
	LETH0_P1_RXDB			LETH PortX TC14 interface receive data input
	P15.7	O0		General-purpose output
	GTM_TOUT78	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	QSPI2_MRST	O3		Slave SPI data output
	—	O4		Reserved
	ASCLIN1_ARTS_F	O5		Ready to send output
	—	O6		Reserved
	QSPI7_SLSO10_F	O7		Master slave select output
	—	O8		Reserved
	EGTM_TOUT78	O9		eGTM muxed output
	LETH0_P1_MIIA_TXD1	O10		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P1_TXCLKA)
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	LETH0_P1_RMIIA_TXD1	O15		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P1_REFCLKA)
	LETH0_P1_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
G17	P15.8	I	FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM0_IN2_5			Mux input channel 2 of TIM module 0
	GTM_TIM1_IN2_5			Mux input channel 2 of TIM module 1
	QSPI2_SCLKB			Slave SPI clock inputs
	SCU_E_REQ5A			ERU channel 5 input A
	EGTM_TIM0_IN2_5			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_5			Mux input channel 2 of TIM module 1
	LETH0_P1_MII_RMII_RXD0A			LETH0 PortX MII and RMII receive data bit 0 (to be used with LETH0_P1_RXCLKA or LETH0_P1_REFCLKA)
	P15.8	O0		General-purpose output
	GTM_TOUT79	O1		GTM muxed output

(table continues...)

Table 14 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O2		Reserved
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	ASCLIN3_ASCLK	O6		Shift clock output
	QSPI7_SLS011_F	O7		Master slave select output
	—	O8		Reserved
	EGTM_TOUT79	O9		eGTM muxed output
	GPT123_T6OUT	O10		External output for overflow/underflow detection of core timer T6
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
B23	P15.10	I	FAST / PU1 / VDDEXT S / ES6	General-purpose input
	GTM_TIM2_IN1_8			Mux input channel 1 of TIM module 2
	GTM_TIM4_IN1_7			Mux input channel 1 of TIM module 4
	QSPI5_MRSTA			Master SPI data input
	I2C1_SDAC			Serial Data Input 2
	EGTM_TIM2_IN1_8			Mux input channel 1 of TIM module 2
	P15.10	O0		General-purpose output
	GTM_TOUT242	O1		GTM muxed output
	—	O2		Reserved
	QSPI5_MRST	O3		Slave SPI data output
	—	O4		Reserved
	—	O5		Reserved
	I2C1_SDA	O6		Serial Data Output
	QSPI7_SLS09_F	O7		Master slave select output
	—	O8		Reserved
	EGTM_TOUT242	O9		eGTM muxed output
	LETH0_P1_MIIA_TXD2	O10		LETH0 PortX MII transmit data bit 2 (to be used with LETH0_P1_TXCLKA)

(table continues...)

Table 14 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
A23	P15.11	I	FAST / PU1 / VDDEXTH S / ES6	General-purpose input
	GTM_TIM2_IN2_8			Mux input channel 2 of TIM module 2
	GTM_TIM4_IN2_6			Mux input channel 2 of TIM module 4
	QSPI5_SLSIA			Slave select input
	I2C1_SCLC			Serial Clock Input 2
	LETH0_P0_EDF			LETH PortX TC14 interface energy detection input
	LETH0_P0_MDIOF			LETH PortX MDIO interface data input
	EGTM_TIM2_IN2_8			Mux input channel 2 of TIM module 2
	P15.11	O0		General-purpose output
	GTM_TOUT243	O1		GTM muxed output
	—	O2		Reserved
	QSPI5_SLSO2	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	I2C1_SCL	O6		Serial Clock Output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT243	O9		eGTM muxed output
	LETH0_P1_MIIA_TXD3	O10		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P1_TXCLKA)
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
B22	P15.12	I	FAST / PU1 /	General-purpose input

(table continues...)

Table 14 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TIM2_IN3_6		VDDEXTH S / ES6	Mux input channel 3 of TIM module 2
	GTM_TIM4_IN3_6			Mux input channel 3 of TIM module 4
	CANXL00_RXDF			CANXL receive input node 0
	LETH0_P0_COLB			LETH PortX MII collision detection
	LETH0_P1_CRSA			LETH PortX MII carrier sense
	EGTM_TIM2_IN3_6			Mux input channel 3 of TIM module 2
	LETH0_P0_RXDF			LETH PortX TC14 interface receive data input
	P15.12	O0		General-purpose output
	GTM_TOUT244	O1		GTM muxed output
	—	O2		Reserved
	QSPI5_SLSO1	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT244	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
A22	P15.13	I	FAST / PU1 / VDDEXTH S / ES6	General-purpose input
	GTM_TIM2_IN4_9			Mux input channel 4 of TIM module 2
	GTM_TIM4_IN4_6			Mux input channel 4 of TIM module 4
	EGTM_TIM2_IN4_9			Mux input channel 4 of TIM module 2
	LETH0_P2_MII_RXDVA			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	LETH0_P2_RMII_CRSDVA			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	P15.13	O0		General-purpose output

(table continues...)

Table 14 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TOUT245	O1		GTM muxed output
	—	O2		Reserved
	QSPI5_SLSO0	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	ASCLIN1_ASCLK_F	O6		Shift clock output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT245	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P0_TXD	O12		LETH PortX TC14 interface transmit data output
	CANXL00_TXD	O13		CANXL transmit output node 0
	LETH1_P0_TXD	O14		LETH PortX TC14 interface transmit data output
	—	O15		Reserved
B20	P15.14	I	FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM2_IN5_10			Mux input channel 5 of TIM module 2
	GTM_TIM4_IN5_6			Mux input channel 5 of TIM module 4
	QSPI5_MTSRA			Slave SPI data input
	LETH0_P1_MII_RXD2A			LETH0 PortX MII receive data bit 2 (to be used with LETH0_P1_RXCLKA)
	EGTM_TIM2_IN5_10			Mux input channel 5 of TIM module 2
	P15.14	O0		General-purpose output
	GTM_TOUT246	O1		GTM muxed output
	—	O2		Reserved
	QSPI5_MTSR	O3		Master SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT246	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 14 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
A20	P15.15	I	FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM2_IN6_9			Mux input channel 6 of TIM module 2
	GTM_TIM4_IN6_6			Mux input channel 6 of TIM module 4
	QSPI5_SCLKA			Slave SPI clock inputs
	LETH0_P1_MII_RXD3A			LETH0 PortX MII receive data bit 3 (to be used with LETH0_P1_RXCLKA)
	EGTM_TIM2_IN6_9			Mux input channel 6 of TIM module 2
	P15.15	O0		General-purpose output
	GTM_TOUT247	O1		GTM muxed output
	—	O2		Reserved
	QSPI5_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT247	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

3.2.10 BGA436_STD port 20

Table 15 Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
L23	P20.0	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN6_7			Mux input channel 6 of TIM module 0
	GTM_TIM1_IN4_9			Mux input channel 4 of TIM module 1
	GTM_TIM1_IN6_7			Mux input channel 6 of TIM module 1
	CAN03_RXDC			CAN receive input node 3
	CAN21_RXDC			CAN receive input node 1
	CBS_TGI0			Trigger input
	SCU_E_REQ6A			ERU channel 6 input A
	GPT120_T6EUDA			Count direction control input of core timer T6
	SENT1_SENT1D			Receive input channel 1
	GPT122_T2INB			Trigger/gate input of timer T2
	LETH0_P0_MII_RXERB			LETH0 PortX MII receive error (to be used with LETH0_P0_RXCLKB)
	LETH1_P0_MII_RXERB			LETH1 PortX MII receive error (to be used with LETH1_P0_RXCLKB)
	EGTM_TIM0_IN6_7			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN4_9			Mux input channel 4 of TIM module 1
	EGTM_TIM1_IN6_7			Mux input channel 6 of TIM module 1
	CLOCK_CLKA_SYSCLK			System clock input
	P20.0	O0		General-purpose output
	GTM_TOUT59	O1		GTM muxed output
	ASCLIN3_ATX_F	O2		Transmit output
	ASCLIN3_ASCLK_F	O3		Shift clock output
	SENT1_SPC1	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT59	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P0_MIIB_TXD2	O11		LETH0 PortX MII transmit data bit 2 (to be used with LETH0_P0_TXCLKB)

(table continues...)

Table 15 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_MDC	O12		LETH PortX MDIO interface clock output
	LETH1_P0_MIIB_TXD2	O13		LETH1 PortX MII transmit data bit 2 (to be used with LETH1_P0_TXCLKB)
	—	O14		Reserved
	XSPIO_CSB1_N	O15		Chip select
	HSCT0_SYSCLK_OUT	PO		sys clock output
	CBS_TGO0	O		Trigger output
K22	P20.1	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM2_IN3_5			Mux input channel 3 of TIM module 2
	GTM_TIM3_IN3_5			Mux input channel 3 of TIM module 3
	GTM_TIM4_IN4_11			Mux input channel 4 of TIM module 4
	CBS_TGI1			Trigger input
	GTM_CDTM1_DTM4_2			Input mux of CDTM1_DTM4_AUXIN0/1
	GTM_CDTM1_DTM5_2			Input mux of CDTM1_DTM5_AUXIN0/1
	EGTM_CDTM1_DTM4_2			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM5_2			Input mux of CDTM1_DTM5_AUXIN0/1
	LETH0_P0_CRSC			LETH PortX MII carrier sense
	EGTM_TIM2_IN3_5			Mux input channel 3 of TIM module 2
	P20.1	O0		General-purpose output
	GTM_TOUT60	O1		GTM muxed output
	ASCLIN3_ASLSO_F	O2		Slave select signal output
	CAN32_TXD	O3		CAN transmit output node 2
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT60	O9		eGTM muxed output
	LETH1_P0_MIIB_TXD3	O10		LETH1 PortX MII transmit data bit 3 (to be used with LETH1_P0_TXCLKB)
	LETH0_P0_MIIB_TXD3	O11		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_MIIB_TXD0	O12		LETH0 PortX MII transmit data bit 0 (to be used with LETH0_P0_TXCLKB)

(table continues...)

Table 15 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P0_RMIIB_TXD0	O13		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P0_REFCLKB)
	LETH1_P0_MIIB_TXD0	O14		LETH1 PortX MII transmit data bit 0 (to be used with LETH1_P0_TXCLKB)
	LETH1_P0_RMIIB_TXD0	O15		LETH1 PortX RMII transmit data bit 0 (to be used with LETH1_P0_REFCLKB)
	LETH0_P0_RMIIRB_TXD0	PO		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P0_REFCLKB - registered*)
	LETH1_P0_RMIIRB_TXD0	PO		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P0_REFCLKB - registered*)
	CBS_TGO1	O		Trigger output
L22	P20.2	I	S / PU / VDDEXT	General-purpose input
	TESTMODE			Testmode Enable Input
	PMS_TESTMODEIN			TESTMODE pin input
K23	P20.3	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM2_IN4_5			Mux input channel 4 of TIM module 2
	GTM_TIM3_IN4_5			Mux input channel 4 of TIM module 3
	GTM_TIM4_IN5_11			Mux input channel 5 of TIM module 4
	ASCLIN3_ARXC_F			Receive input
	GPT120_T6INA			Trigger/gate input of core timer T6
	SENT0_SENT3D			Receive input channel 3
	GPT122_T2EUDB			Count direction control input of timer T2
	EGTM_TIM2_IN4_5			Mux input channel 4 of TIM module 2
	XSPIO_RXD0B			Receive data
	LETH0_P0_TXCLKB			LETH PortX MII transmit clock
	LETH1_P0_TXCLKB			LETH PortX MII transmit clock
	P20.3	O0		General-purpose output
	GTM_TOUT61	O1		GTM muxed output
	ASCLIN3_ATX_F	O2		Transmit output
	QSPIO_SLSO9_F	O3		Master slave select output
	QSPIO_SLSO9	O4		Master slave select output
	CAN03_TXD	O5		CAN transmit output node 3
	CAN21_TXD	O6		CAN transmit output node 1
	—	O7		Reserved

(table continues...)

Table 15 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SENT0_SPC3	O8		Transmit output
	EGTM_TOUT61	O9		eGTM muxed output
	LETH0_P0_TXD	O10		LETH PortX TC14 interface transmit data output
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPIO_TXDB0	O		Transmit data
J20	P20.6	I	FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM2_IN6_5			Mux input channel 6 of TIM module 2
	GTM_TIM3_IN6_5			Mux input channel 6 of TIM module 3
	GTM_TIM6_IN0_1			Mux input channel 0 of TIM module 6
	CAN12_RXDA			CAN receive input node 2
	SENT1_SENT3D			Receive input channel 3
	CAN32_RXDB			CAN receive input node 2
	GPT122_T4EUDB			Count direction control input of timer T4
	EGTM_TIM2_IN6_5			Mux input channel 6 of TIM module 2
	XSPIO_RXD1B			Receive data
	P20.6	O0		General-purpose output
	GTM_TOUT62	O1		GTM muxed output
	ASCLIN1_ARTS	O2		Ready to send output
	QSPI0_SLSO8_F	O3		Master slave select output
	QSPI2_SLSO8	O4		Master slave select output
	ASCLIN3_ASLSO_F	O5		Slave select signal output
	SENT1_SPC3	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT62	O9		eGTM muxed output
	LETH1_P0_MIIB_TXER	O10		LETH1 PortX MII transmit error (to be used with LETH1_P0_TXCLKB)
	LETH0_P0_MIIB_TXER	O11		LETH0 PortX MII transmit error (to be used with LETH0_P0_TXCLKB)

(table continues...)

Table 15 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P0_MIIB_TXEN	O12		LETH0 PortX MII transmit enable (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_RMIIB_TXEN	O13		LETH0 PortX RMII transmit enable (to be used with LETH0_P0_REFCLKB)
	LETH1_P0_MIIB_TXEN	O14		LETH1 PortX MII transmit enable (to be used with LETH1_P0_TXCLKB)
	LETH1_P0_RMIIB_TXEN	O15		LETH1 PortX RMII transmit enable (to be used with LETH1_P0_REFCLKB)
	LETH0_P0_RMIIRB_TXEN	PO		LETH0 PortX RMII transmit enable (to be used with LETH0_P0_REFCLKB - registered*)
	LETH1_P0_RMIIRB_TXEN	PO		LETH0 PortX RMII transmit enable (to be used with LETH0_P0_REFCLKB - registered*)
	XSPIO_TXDB1	O		Transmit data
J22	P20.7	I	FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM1_IN5_8			Mux input channel 5 of TIM module 1
	GTM_TIM2_IN7_5			Mux input channel 7 of TIM module 2
	GTM_TIM3_IN7_5			Mux input channel 7 of TIM module 3
	GTM_TIM6_IN1_1			Mux input channel 1 of TIM module 6
	CAN00_RXDB			CAN receive input node 0
	ASCLIN1_ACTSA			Clear to send input
	SDMMC0_DAT0_IN			Read data in
	SENT1_SENT0D			Receive input channel 0
	EGTM_TIM1_IN5_8			Mux input channel 5 of TIM module 1
	EGTM_TIM2_IN7_5			Mux input channel 7 of TIM module 2
	P20.7	O0		General-purpose output
	GTM_TOUT63	O1		GTM muxed output
	—	O2		Reserved
	ASCLIN3_ARTS_F	O3		Ready to send output
	—	O4		Reserved
	CAN12_TXD	O5		CAN transmit output node 2
	SENT1_SPC0	O6		Transmit output
	LETH1_P0_MIIB_TXD2	O7		LETH1 PortX MII transmit data bit 2 (to be used with LETH1_P0_TXCLKB)
	—	O8		Reserved
	EGTM_TOUT63	O9		eGTM muxed output

(table continues...)

Table 15 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH1_P0_MIIB_TXD3	O10		LETH1 PortX MII transmit data bit 3 (to be used with LETH1_P0_TXCLKB)
	LETH0_P0_MIIB_TXD3	O11		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_MIIB_TXD1	O12		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_RMIIB_TXD1	O13		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P0_REFCLKB)
	LETH1_P0_MIIB_TXD1	O14		LETH1 PortX MII transmit data bit 1 (to be used with LETH1_P0_TXCLKB)
	LETH1_P0_RMIIB_TXD1	O15		LETH1 PortX RMII transmit data bit 1 (to be used with LETH1_P0_REFCLKB)
	EGTM_HRPWM2_CH7	PO		High resolution PWM 2 output channels
	SDMMC0_DAT0	O		Write data out
J23	P20.8	I	FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM0_IN7_3			Mux input channel 7 of TIM module 0
	GTM_TIM1_IN7_3			Mux input channel 7 of TIM module 1
	GTM_TIM6_IN2_1			Mux input channel 2 of TIM module 6
	SDMMC0_DAT1_IN			Read data in
	LETH0_P0_CRSD			LETH PortX MII carrier sense
	LETH1_P0_CRSD			LETH PortX MII carrier sense
	EGTM_TIM0_IN7_3			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_3			Mux input channel 7 of TIM module 1
	LETH0_P0_MII_RXDVB			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	LETH0_P0_RMII_CRSDVB			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	LETH1_P0_MII_RXDVB			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	LETH1_P0_RMII_CRSDVB			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	P20.8	O0		General-purpose output
	GTM_TOUT64	O1		GTM muxed output
	ASCLIN1_ASLSO	O2		Slave select signal output
	QSPI0_SLSO0_F	O3		Master slave select output
	QSPI1_SLSO0	O4		Master slave select output

(table continues...)

Table 15 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CAN00_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT64	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM2_CH0	PO		High resolution PWM 2 output channels
	SDMMC0_DAT1	O		Write data out
H20	P20.9	I	FAST / PU1 / VDDEXT S / ES	General-purpose input
	GTM_TIM2_IN5_5			Mux input channel 5 of TIM module 2
	GTM_TIM3_IN5_5			Mux input channel 5 of TIM module 3
	GTM_TIM6_IN3_1			Mux input channel 3 of TIM module 6
	CAN03_RXDE			CAN receive input node 3
	ASCLIN1_ARXC			Receive input
	QSPI0_SLSIB_F			Slave select input
	SCU_E_REQ7A			ERU channel 7 input A
	ADC_TRIG62			Triggers from PORTS to ADC
	LETH0_P0_COLD			LETH PortX MII collision detection
	EGTM_TIM2_IN5_5			Mux input channel 5 of TIM module 2
	XSPI0_RXD2B			Receive data
	P20.9	O0		General-purpose output
	GTM_TOUT65	O1		GTM muxed output
	CAN32_TXD	O2		CAN transmit output node 2
	QSPI0_SLSO1_F	O3		Master slave select output
	QSPI1_SLSO1	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

(table continues...)

Table 15 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O8		Reserved
	EGTM_TOUT65	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P0_MIIB_TXD1	O11		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_RMIIB_TXD1	O12		LETH0 PortX RMIIB transmit data bit 1 (to be used with LETH0_P0_REFCLKB)
	—	O13		Reserved
	LETH1_P0_MIIB_TXD1	O14		LETH1 PortX MII transmit data bit 1 (to be used with LETH1_P0_TXCLKB)
	LETH1_P0_RMIIB_TXD1	O15		LETH1 PortX RMIIB transmit data bit 1 (to be used with LETH1_P0_REFCLKB)
	EGTM_HRPWM2_CH1	PO		High resolution PWM 2 output channels
	XSPIO_TXDB2	O		Transmit data
H22	P20.10	I	FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM2_IN6_6			Mux input channel 6 of TIM module 2
	GTM_TIM3_IN6_6			Mux input channel 6 of TIM module 3
	SDMMC0_DAT2_IN			Read data in
	EGTM_TIM2_IN6_6			Mux input channel 6 of TIM module 2
	P20.10	O0		General-purpose output
	GTM_TOUT66	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	QSPI0_SLSO6_F	O3		Master slave select output
	QSPI2_SLSO7	O4		Master slave select output
	CAN03_TXD	O5		CAN transmit output node 3
	ASCLIN1_ASCLK	O6		Shift clock output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT66	O9		eGTM muxed output
	LETH1_P0_TXD	O10		LETH PortX TC14 interface transmit data output
	LETH0_P0_MIIB_TXD0	O11		LETH0 PortX MII transmit data bit 0 (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_RMIIB_TXD0	O12		LETH0 PortX RMIIB transmit data bit 0 (to be used with LETH0_P0_REFCLKB)
	LETH0_P0_TXD	O13		LETH PortX TC14 interface transmit data output

(table continues...)

Table 15 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH1_P0_MIIB_TXD0	O14		LETH1 PortX MII transmit data bit 0 (to be used with LETH1_P0_TXCLKB)
	LETH1_P0_RMIIB_TXD0	O15		LETH1 PortX RMII transmit data bit 0 (to be used with LETH1_P0_REFCLKB)
	EGTM_HRPWM2_CH2	PO		High resolution PWM 2 output channels
	SDMMC0_DAT2	O		Write data out
H23	P20.11	I	FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM2_IN7_6			Mux input channel 7 of TIM module 2
	GTM_TIM3_IN7_6			Mux input channel 7 of TIM module 3
	QSPI0_SCLKA_F			Slave SPI clock inputs
	SDMMC0_DAT3_IN			Read data in
	ASCLIN3_ACTSB_F			Clear to send input
	EGTM_TIM2_IN7_6			Mux input channel 7 of TIM module 2
	LETH0_P0_MII_RMII_RXD1B			LETH0 PortX MII and RMII receive data bit 1 (to be used with LETH0_P0_RXCLKB or LETH0_P0_REFCLKB)
	LETH1_P0_MII_RMII_RXD1B			LETH1 PortX MII and RMII receive data bit 1 (to be used with LETH1_P0_RXCLKB or LETH1_P0_REFCLKB)
	P20.11	O0		General-purpose output
	GTM_TOUT67	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SCLK_F	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT67	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM2_CH3	PO		High resolution PWM 2 output channels

(table continues...)

Table 15 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SDMMC0_DAT3	O		Write data out
G22	P20.12	I	FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM2_IN0_5			Mux input channel 0 of TIM module 2
	GTM_TIM3_IN0_5			Mux input channel 0 of TIM module 3
	QSPI0_MRSTA_F			Master SPI data input
	SDMMC0_DAT4_IN			Read data in
	EGTM_TIM2_IN0_5			Mux input channel 0 of TIM module 2
	LETH0_P0_MII_RMII_RXD 0B			LETH0 PortX MII and RMII receive data bit 0 (to be used with LETH0_P0_RXCLKB or LETH0_P0_REFCLKB)
	LETH1_P0_MII_RMII_RXD 0B			LETH1 PortX MII and RMII receive data bit 0 (to be used with LETH1_P0_RXCLKB or LETH1_P0_REFCLKB)
	P20.12	O0		General-purpose output
	GTM_TOUT68	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_MRST_F	O3		Slave SPI data output
	QSPI0_MTSR_F	O4		Master SPI data output
	—	O5		Reserved
	—	O6		Reserved
	LETH0_P0_MDC	O7		LETH PortX MDIO interface clock output
	—	O8		Reserved
	EGTM_TOUT68	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM2_CH4	PO		High resolution PWM 2 output channels
	SDMMC0_DAT4	O		Write data out
G23	P20.13	I	FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM2_IN1_4			Mux input channel 1 of TIM module 2
	GTM_TIM3_IN1_4			Mux input channel 1 of TIM module 3
	QSPI0_SLSIA_F			Slave select input

(table continues...)

Table 15 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SDMMC0_DAT5_IN			Read data in
	LETH0_P0_MII_RXD2B			LETH0 PortX MII receive data bit 2 (to be used with LETH0_P0_RXCLKB)
	LETH1_P0_MII_RXD2B			LETH1 PortX MII receive data bit 2 (to be used with LETH1_P0_RXCLKB)
	EGTM_TIM2_IN1_4			Mux input channel 1 of TIM module 2
	P20.13	O0		General-purpose output
	GTM_TOUT69	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO2_F	O3		Master slave select output
	QSPI1_SLSO2	O4		Master slave select output
	QSPI0_SCLK_F	O5		Master SPI clock output
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT69	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	XSPI0_CLKB	O15		Clock output
	EGTM_HRPWM2_CH5	PO		High resolution PWM 2 output channels
	SDMMC0_DAT5	O		Write data out
F23	P20.14	I	FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM2_IN2_4			Mux input channel 2 of TIM module 2
	GTM_TIM3_IN2_4			Mux input channel 2 of TIM module 3
	QSPI0_MTSRA_F			Slave SPI data input
	SDMMC0_DAT6_IN			Read data in
	QSPI4_MRSTH			Master SPI data input
	LETH0_P0_MII_RXD3B			LETH0 PortX MII receive data bit 3 (to be used with LETH0_P0_RXCLKB)
	LETH1_P0_MII_RXD3B			LETH1 PortX MII receive data bit 3 (to be used with LETH1_P0_RXCLKB)

(table continues...)

Table 15 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM2_IN2_4			Mux input channel 2 of TIM module 2
	P20.14	O0		General-purpose output
	GTM_TOUT70	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_MTSR_F	O3		Master SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT70	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	XSPI0_CSB0_N	O15		Chip select
	EGTM_HRPWM2_CH6	PO		High resolution PWM 2 output channels
	SDMMC0_DAT6	O		Write data out

3.2.11 BGA436_STD port 21

Table 16 Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
N20	P21.0	I	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM2_IN4_6			Mux input channel 4 of TIM module 2
	GTM_TIM3_IN4_6			Mux input channel 4 of TIM module 3
	GTM_TIM4_IN0_11			Mux input channel 0 of TIM module 4
	QSPI4_MRSTDN_F			Master SPI data input
	DMU_FDEST			FDEST for NVM
	HSCT1_RXDN			Rx data
	QSPI0_SCLKEN			Slave SPI clock inputs (LVDS N line)
	QSPI4_MRSTE			Master SPI data input

(table continues...)

Table 16 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GPT123_T6EUDA			Count direction control input of core timer T6
	EGTM_TIM2_IN4_6			Mux input channel 4 of TIM module 2
	QSPI0_SCLKD			Slave SPI clock inputs
	P21.0	O0		General-purpose output
	GTM_TOUT51	O1		GTM muxed output
	—	O2		Reserved
	GPT123_T6OUT	O3		External output for overflow/underflow detection of core timer T6
	—	O4		Reserved
	—	O5		Reserved
	QSPI0_SLSO8_F	O6		Master slave select output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT51	O9		eGTM muxed output
	LETH0_P0_MIIB_TXD1	O10		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P0_TXCLKB)
	LETH0_P1_PPS	O11		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	LETH0_P0_RMIIB_TXD1	O12		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P0_REFCLKB)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_RMIIRB_TXD1	PO		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P0_REFCLKB - registered*)
	CSCU_CSRM1	O		Pin Output Value
M20	P21.1	I	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM2_IN5_6			Mux input channel 5 of TIM module 2
	GTM_TIM3_IN5_6			Mux input channel 5 of TIM module 3
	GTM_TIM4_IN1_13			Mux input channel 1 of TIM module 4
	QSPI4_MRSTDP_F			Master SPI data input
	HSCT1_RXDP			Rx data
	QSPI0_SCLKEP			Slave SPI clock inputs (LVDS P line)
	GTM_CDTM4_DTM4_2			Input mux of CDTM4_DTM4_AUXIN0/1

(table continues...)

Table 16 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_CDTM4_DTM5_2			Input mux of CDTM4_DTM5_AUXIN0/1
	EGTM_TIM2_IN5_6			Mux input channel 5 of TIM module 2
	QSPI0_SCLKF			Slave SPI clock inputs
	P21.1	O0		General-purpose output
	GTM_TOUT52	O1		GTM muxed output
	—	O2		Reserved
	GPT122_T3OUT	O3		External output for overflow/underflow detection of core timer T3
	—	O4		Reserved
	—	O5		Reserved
	QSPI0_SCLK_F	O6		Master SPI clock output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT52	O9		eGTM muxed output
	LETH0_P0_MIIB_TXER	O10		LETH0 PortX MII transmit error (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_MIIB_TXEN	O11		LETH0 PortX MII transmit enable (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_RMIIB_TXEN	O12		LETH0 PortX RMII transmit enable (to be used with LETH0_P0_REFCLKB)
	LETH1_P0_MIIB_TXEN	O13		LETH1 PortX MII transmit enable (to be used with LETH1_P0_TXCLKB)
	LETH1_P0_RMIIB_TXEN	O14		LETH1 PortX RMII transmit enable (to be used with LETH1_P0_REFCLKB)
	—	O15		Reserved
	LETH0_P0_RMIIRB_TXEN	PO		LETH0 PortX RMII transmit enable (to be used with LETH0_P0_REFCLKB - registered*)
	LETH1_P0_RMIIRB_TXEN	PO		LETH0 PortX RMII transmit enable (to be used with LETH0_P0_REFCLKB - registered*)
	CSCU_CSRM2	O		Pin Output Value
N22	P21.2	I	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN0_7			Mux input channel 0 of TIM module 0
	GTM_TIM1_IN0_7			Mux input channel 0 of TIM module 1
	GTM_TIM5_IN4_10			Mux input channel 4 of TIM module 5
	QSPI2_MRSTCN			Master SPI data input (LVDS N line)

(table continues...)

Table 16 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SMU_EXT_EMERGENCYSTOP_REQ			Emergency Stop External Request B
	ASCLIN3_ARXGN			Differential Receive input (low active)
	HSCT0_RXDN			Rx data
	QSPI4_MRSTCN_F			Master SPI data input
	QSPI0_MTSRDN			Slave SPI data input (LVDS N line)
	SENT0_SENT2D			Receive input channel 2
	GPT123_T3INA			Trigger/gate input of core timer T3 (input A, B and C)
	GTM_CDTM1_DTM4_1			Input mux of CDTM1_DTM4_AUXIN0/1
	GTM_CDTM1_DTM5_1			Input mux of CDTM1_DTM5_AUXIN0/1
	EGTM_CDTM1_DTM4_1			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM5_1			Input mux of CDTM1_DTM5_AUXIN0/1
	EGTM_TIM0_IN0_7			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_7			Mux input channel 0 of TIM module 1
	QSPI0_MTSRE			Slave SPI data input
	QSPI4_MTSRC			Slave SPI data input
	LETH0_P0_MDIOH			LETH PortX MDIO interface data input
	LETH0_P0_EDH			LETH PortX TC14 interface energy detection input
	P21.2	O0		General-purpose output
	GTM_TOUT53	O1		GTM muxed output
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	SENT0_SPC2	O4		Transmit output
	—	O5		Reserved
	QSPI0_MTSR_F	O6		Master SPI data output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT53	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved

(table continues...)

Table 16 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O15		Reserved
	LETH0_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
M22	P21.3	I	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN1_6			Mux input channel 1 of TIM module 0
	GTM_TIM1_IN1_6			Mux input channel 1 of TIM module 1
	GTM_TIM5_IN5_13			Mux input channel 5 of TIM module 5
	QSPI2_MRSTCP			Master SPI data input (LVDS P line)
	ASCLIN3_ARXGP			Differential Receive input (high active)
	HSCT0_RXDP			Rx data
	QSPI4_MRSTCP_F			Master SPI data input
	QSPI0_MTSRDP			Slave SPI data input (LVDS P line)
	SENT1_SENT2D			Receive input channel 2
	GPT123_T3EUDA			Count direction control input of core timer T3
	EGTM_TIM0_IN1_6			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_6			Mux input channel 1 of TIM module 1
	QSPI0_MTSRF			Slave SPI data input
	P21.3	O0		General-purpose output
	GTM_TOUT54	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	SENT1_SPC2	O4		Transmit output
	—	O5		Reserved
	QSPI0_SLSO9_F	O6		Master slave select output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT54	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 16 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
N23	P21.4	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	GTM_TIM0_IN2_6			Mux input channel 2 of TIM module 0
	GTM_TIM1_IN2_6			Mux input channel 2 of TIM module 1
	GTM_TIM5_IN6_13			Mux input channel 6 of TIM module 5
	SENT0_SENT0D			Receive input channel 0
	GPT123_T4INA			Trigger/gate input of timer T4
	EGTM_TIM0_IN2_6			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_6			Mux input channel 2 of TIM module 1
	LETH0_P0_REFCLKB			LETH0 PortX RMII reference clock
	LETH0_P0_RXCLKB			LETH PortX MII receive clock
	LETH1_P0_REFCLKB			LETH PortX RMII reference clock
	LETH1_P0_RXCLKB			LETH PortX MII receive clock
	P21.4	O0		General-purpose output
	GTM_TOUT55	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	SENT0_SPC0	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	QSPI0_MRSTN	O8		Slave SPI inverted data output
	EGTM_TOUT55	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	HSCT0_TXDN	PO		Tx data
M23	P21.5	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	GTM_TIM0_IN3_6			Mux input channel 3 of TIM module 0
	GTM_TIM1_IN3_6			Mux input channel 3 of TIM module 1
	GTM_TIM5_IN7_11			Mux input channel 7 of TIM module 5

(table continues...)

Table 16 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SENT0_SENT1D			Receive input channel 1
	QSPI0_MRSTE_F			Master SPI data input
	GPT123_T6INA			Trigger/gate input of core timer T6
	EGTM_TIM0_IN3_6			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_6			Mux input channel 3 of TIM module 1
	P21.5	O0		General-purpose output
	GTM_TOUT56	O1		GTM muxed output
	ASCLIN3_ASCLK	O2		Shift clock output
	—	O3		Reserved
	SENT0_SPC1	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	QSPI0_MRSTP	O8		Slave SPI data output
	EGTM_TOUT56	O9		eGTM muxed output
	GPT123_T3OUT	O10		External output for overflow/underflow detection of core timer T3
	LETH0_P0_MIIB_TXEN	O11		LETH0 PortX MII transmit enable (to be used with LETH0_P0_TXCLKB)
	—	O12		Reserved
	—	O13		Reserved
	LETH1_P0_MIIB_TXEN	O14		LETH1 PortX MII transmit enable (to be used with LETH1_P0_TXCLKB)
	—	O15		Reserved
	HSCT0_TXDP	PO		Tx data
L20	P21.6	I	FAST / PD3 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN4_8			Mux input channel 4 of TIM module 0
	GTM_TIM1_IN4_8			Mux input channel 4 of TIM module 1
	GTM_TIM4_IN2_13			Mux input channel 2 of TIM module 4
	CAN33_RXDB			CAN receive input node 3
	GPT120_T5EUDA			Count direction control input of timer T5
	ASCLIN3_ARXF_F			Receive input
	CBS_TGI2			Trigger input
	TDI			JTAG Module Data Input

(table continues...)

Table 16 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI0_SLSIC			Slave select input
	LETH0_P0_COLC			LETH PortX MII collision detection
	LETH1_P0_COLC			LETH PortX MII collision detection
	EGTM_TIM0_IN4_8			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_8			Mux input channel 4 of TIM module 1
	P21.6	O0		General-purpose output
	GTM_TOUT57	O1		GTM muxed output
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	GPT120_T3OUT	O7		External output for overflow/underflow detection of core timer T3
	—	O8		Reserved
	EGTM_TOUT57	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	DAP3	I/PO		DAP:DAP3 Data I/O
	DAPE1	I/PO		DAPE: DAPE1 Data I/O DAPE: DAPE1 Data I/O (PD Devices: VSS)
	CBS_TGO2	O		Trigger output
L19	P21.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN5_7			Mux input channel 5 of TIM module 0
	GTM_TIM1_IN5_7			Mux input channel 5 of TIM module 1
	GTM_TIM4_IN3_13			Mux input channel 3 of TIM module 4
	GPT120_T5INA			Trigger/gate input of timer T5
	CBS_TGI3			Trigger input
	LETH0_P0_MII_RXERC			LETH0 PortX MII receive error (to be used with LETH0_P0_RXCLKC)

(table continues...)

Table 16 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM0_IN5_7			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_7			Mux input channel 5 of TIM module 1
	P21.7	O0		General-purpose output
	GTM_TOUT58	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	ASCLIN3_ASCLK	O3		Shift clock output
	CAN33_TXD	O4		CAN transmit output node 3
	—	O5		Reserved
	—	O6		Reserved
	GPT120_T6OUT	O7		External output for overflow/underflow detection of core timer T6
	—	O8		Reserved
	EGTM_TOUT58	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	DAP2	I/PO		DAP:DAP2 Data I/O
	DAPE2	I/PO		DAPE: DAPE2 Data I/O DAPE: DAPE2 Data I/O (PD Devices: VSS)
	TDO	PO		PU/TRIST controlled through PMS_PADCON.ALLTRIST (HWCFG6 P14.4) during reset (PORST=0). The default state after PORST release in DAP mode is controlled through PMS_PADCON.ALLTRIST (HWCFG6 P14.4) . The default state after PORST release in JTAG mode is HighZ. In Standby Mode it is controlled through PMS_PADCON.ALLTRIST (HWCFG6 P14.4)
	CBS_TGO3	O		Trigger output

3.2.12 BGA436_STD port 22

Table 17 Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
U23	P22.0	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	GTM_TIM0_IN1_7			Mux input channel 1 of TIM module 0
	GTM_TIM1_IN1_7			Mux input channel 1 of TIM module 1
	QSPI4_MTSRB_F			Slave SPI data input
	ASCLIN6_ARXE			Receive input
	QSPI5_MRSTC			Master SPI data input
	GPT123_T2INA			Trigger/gate input of timer T2
	EGTM_TIM0_IN1_7			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_7			Mux input channel 1 of TIM module 1
	LETH0_P1_MII_RXDVB			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	LETH0_P1_RMII_CRSDVB			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	P22.0	O0		General-purpose output
	GTM_TOUT47	O1		GTM muxed output
	ASCLIN3_ATXN	O2		Differential Transmit output (low active)
	QSPI4_MTSR_F	O3		Master SPI data output
	QSPI4_SCLKN_F	O4		Master SPI clock output (LVDS N line)
	MSC1_FCLN	O5		Shift-clock inverted part of the differential signal
	—	O6		Reserved
	ASCLIN6_ATX	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT47	O9		eGTM muxed output
	ASCLIN4_ASCLK_F	O10		Shift clock output
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
U22	P22.1	I	LVDS_TX / FAST / PU1 /	General-purpose input
	GTM_TIM0_IN0_8			Mux input channel 0 of TIM module 0
	GTM_TIM1_IN0_8			Mux input channel 0 of TIM module 1

(table continues...)

Table 17 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI4_MRSTB_F		VDDEXT / ES6	Master SPI data input
	ASCLIN7_ARXE			Receive input
	GPT123_T2EUDA			Count direction control input of timer T2
	EGTM_TIM0_IN0_8			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_8			Mux input channel 0 of TIM module 1
	LETH0_P1_REFCLKB			LETH0 PortX RMII reference clock
	LETH0_P1_RXCLKB			LETH PortX MII receive clock
	P22.1	O0		General-purpose output
	GTM_TOUT48	O1		GTM muxed output
	ASCLIN3_ATXP	O2		Differential Transmit output (high active)
	QSPI4_MRST_F	O3		Slave SPI data output
	QSPI4_SCLKP_F	O4		Master SPI clock output
	MSC1_FCLP	O5		Shift-clock direct part of the differential signal
	QSPI5_SLSO9	O6		Master slave select output
	ASCLIN7_ATX	O7		Transmit output
	QSPI4_SLSO9	O8		Master slave select output
	EGTM_TOUT48	O9		eGTM muxed output
	ASCLIN4_ATX_F	O10		Transmit output
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
V23	P22.2	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	GTM_TIM0_IN3_7			Mux input channel 3 of TIM module 0
	GTM_TIM1_IN3_7			Mux input channel 3 of TIM module 1
	QSPI4_SLSIB_F			Slave select input
	ASCLIN4_ARXH_F			Receive input
	GPT123_T4EUDA			Count direction control input of timer T4
	LETH0_P1_COLA			LETH PortX MII collision detection
	LETH0_P1_MII_RXERC			LETH0 PortX MII receive error (to be used with LETH0_P1_RXCLKC)
	EGTM_TIM0_IN3_7			Mux input channel 3 of TIM module 0

(table continues...)

Table 17 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM1_IN3_7			Mux input channel 3 of TIM module 1
	P22.2	O0		General-purpose output
	GTM_TOUT49	O1		GTM muxed output
	ASCLIN5_ATX	O2		Transmit output
	QSPI4_SLSO3_F	O3		Master slave select output
	QSPI4_MTSRN_F	O4		Master SPI data output (LVDS N line)
	MSC1_SON	O5		Data output - inverted part of the differential signal
	QSPI5_MTSR	O6		Master SPI data output
	QSPI4_MTSR_F	O7		Master SPI data output
	—	O8		Reserved
	EGTM_TOUT49	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	LETH0_P1_MIIB_TXEN	O13		LETH0 PortX MII transmit enable (to be used with LETH0_P1_TXCLKB)
	—	O14		Reserved
	LETH0_P1_RMIIB_TXEN	O15		LETH0 PortX RMII transmit enable (to be used with LETH0_P1_REFCLKB)
	LETH0_P1_RMIIRB_TXEN	PO		LETH0 PortX RMII transmit enable (to be used with LETH0_P1_REFCLKB - registered*)
	HSCT1_TXDN	PO		Tx data
V22	P22.3	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	GTM_TIM0_IN4_4			Mux input channel 4 of TIM module 0
	GTM_TIM1_IN4_4			Mux input channel 4 of TIM module 1
	QSPI4_SCLKB_F			Slave SPI clock inputs
	ASCLIN5_ARXC			Receive input
	GPT123_T5INA			Trigger/gate input of timer T5
	LETH0_P1_MII_RMII_RXD 0B			LETH0 PortX MII and RMII receive data bit 0 (to be used with LETH0_P1_RXCLKB or LETH0_P1_REFCLKB)
	EGTM_TIM0_IN4_4			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_4			Mux input channel 4 of TIM module 1
	LETH0_P1_REFCLKC			LETH0 PortX RMII reference clock
	LETH0_P1_RXCLKC			LETH PortX MII receive clock

(table continues...)

Table 17 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	P22.3	O0		General-purpose output
	GTM_TOUT50	O1		GTM muxed output
	QSPI5_SCLK	O2		Master SPI clock output
	QSPI4_SCLK_F	O3		Master SPI clock output
	QSPI4_MTSRP_F	O4		Master SPI data output
	MSC1_SOP	O5		Data output - direct part of the differential signal
	—	O6		Reserved
	ASCLIN7_ATX	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT50	O9		eGTM muxed output
	ASCLIN4_ASLSO_F	O10		Slave select signal output
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	HSCT1_TXDP	PO		Tx data
U19	P22.4	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM3_IN0_8			Mux input channel 0 of TIM module 3
	SCU_E_REQ5E			ERU channel 5 input E
	ASCLIN7_ARXF			Receive input
	GPT123_T5EUDA			Count direction control input of timer T5
	LETH0_P1_MII_RMII_RXD0C			LETH0 PortX MII and RMII receive data bit 0 (to be used with LETH0_P1_RXCLKC or LETH0_P1_REFCLKC)
	GTM_CDTM3_DTM4_1			Input mux of CDTM3_DTM4_AUXIN0/1
	GTM_CDTM3_DTM5_1			Input mux of CDTM3_DTM5_AUXIN0/1
	LETH0_P1_RXDH			LETH PortX TC14 interface receive data input
	P22.4	O0		General-purpose output
	GTM_TOUT130	O1		GTM muxed output
	ASCLIN4_ASCLK_F	O2		Shift clock output
	—	O3		Reserved
	QSPI0_SLSO12	O4		Master slave select output
	—	O5		Reserved

(table continues...)

Table 17 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CAN13_TXD	O6		CAN transmit output node 3
	QSPI6_SLSO15_F	O7		Master slave select output
	—	O8		Reserved
	EGTM_TOUT130	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
U20	P22.5	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM3_IN1_7			Mux input channel 1 of TIM module 3
	QSPI0_MTSRC			Slave SPI data input
	CAN13_RXDC			CAN receive input node 3
	GPT122_T3INB			Trigger/gate input of core timer T3 (input A, B and C)
	P22.5	O0		General-purpose output
	GTM_TOUT131	O1		GTM muxed output
	ASCLIN4_ATX_F	O2		Transmit output
	—	O3		Reserved
	QSPI0_MTSR	O4		Master SPI data output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT131	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 17 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
T19	P22.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM2_IN6_11			Mux input channel 6 of TIM module 2
	GTM_TIM3_IN2_6			Mux input channel 2 of TIM module 3
	QSPI0_MRSTC			Master SPI data input
	ASCLIN4_ARXC_F			Receive input
	GPT122_T3EUDB			Count direction control input of core timer T3
	LETH0_P1_CRSB			LETH PortX MII carrier sense
	EGTM_TIM2_IN6_11			Mux input channel 6 of TIM module 2
	LETH0_P1_MII_RXDVC			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	LETH0_P1_RMII_CRSDVC			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	P22.6	O0		General-purpose output
	GTM_TOUT132	O1		GTM muxed output
	ASCLIN4_ASLSO_F	O2		Slave select signal output
	—	O3		Reserved
	QSPI0_MRST	O4		Slave SPI data output
	CAN21_TXD	O5		CAN transmit output node 1
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT132	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
T20	P22.7	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM3_IN3_7			Mux input channel 3 of TIM module 3
	QSPI0_SCLKC			Slave SPI clock inputs
	CAN21_RXDF			CAN receive input node 1
	GPT122_T4INB			Trigger/gate input of timer T4

(table continues...)

Table 17 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_TXCLKB			LETH PortX MII transmit clock
	LETH0_P1_TXCLKC			LETH PortX MII transmit clock
	P22.7	O0		General-purpose output
	GTM_TOUT133	O1		GTM muxed output
	ASCLIN4_ASCLK	O2		Shift clock output
	—	O3		Reserved
	QSPI0_SCLK	O4		Master SPI clock output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT133	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
R19	P22.8	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM3_IN4_7			Mux input channel 4 of TIM module 3
	GTM_TIM5_IN0_4			Mux input channel 0 of TIM module 5
	QSPI0_SCLKB			Slave SPI clock inputs
	GPT122_T5INB			Trigger/gate input of timer T5
	LETH0_P1_COLC			LETH PortX MII collision detection
	LETH0_P1_RXDE			LETH PortX TC14 interface receive data input
	P22.8	O0		General-purpose output
	GTM_TOUT134	O1		GTM muxed output
	ASCLIN5_ASCLK	O2		Shift clock output
	—	O3		Reserved
	QSPI0_SCLK	O4		Master SPI clock output
	CAN22_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	—	O7		Reserved

(table continues...)

Table 17 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O8		Reserved
	EGTM_TOUT134	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
R20	P22.9	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM3_IN5_7			Mux input channel 5 of TIM module 3
	GTM_TIM5_IN1_10			Mux input channel 1 of TIM module 5
	QSPI0_MRSTB			Master SPI data input
	ASCLIN4_ARXD_F			Receive input
	CAN22_RXDE			CAN receive input node 2
	LETH0_P1_EDE			LETH PortX TC14 interface energy detection input
	GPT122_T5EUDB			Count direction control input of timer T5
	GTM_CDTM3_DTM4_2			Input mux of CDTM3_DTM4_AUXIN0/1
	GTM_CDTM3_DTM5_2			Input mux of CDTM3_DTM5_AUXIN0/1
	LETH0_P1_MDIOE			LETH PortX MDIO interface data input
	P22.9	O0		General-purpose output
	GTM_TOUT135	O1		GTM muxed output
	GPT122_T6OUT	O2		External output for overflow/underflow detection of core timer T6
	—	O3		Reserved
	QSPI0_MRST	O4		Slave SPI data output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT135	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 17 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_MIIC_TXD1	O11		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P1_TXCLKC)
	LETH0_P1_RMIIC_TXD1	O12		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P1_REFCLKC)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_RMIIRC_TXD1	PO		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P1_REFCLKC - registered*)
	LETH0_P1_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
P19	P22.10	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM3_IN6_7			Mux input channel 6 of TIM module 3
	GTM_TIM5_IN2_8			Mux input channel 2 of TIM module 5
	QSPI0_MTSRB			Slave SPI data input
	GPT122_T6INB			Trigger/gate input of core timer T6
	P22.10	O0		General-purpose output
	GTM_TOUT136	O1		GTM muxed output
	ASCLIN4_ATX_F	O2		Transmit output
	—	O3		Reserved
	QSPI0_MTSR	O4		Master SPI data output
	CAN23_TXD	O5		CAN transmit output node 3
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT136	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P1_MIIC_TXD0	O11		LETH0 PortX MII transmit data bit 0 (to be used with LETH0_P1_TXCLKC)
	LETH0_P1_RMIIC_TXD0	O12		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P1_REFCLKC)
	—	O13		Reserved
	—	O14		Reserved
	LETH0_P1_TXD	O15		LETH PortX TC14 interface transmit data output

(table continues...)

Table 17 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_RMIIRC_TXD0	PO		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P1_REFCLKC - registered*)
P20	P22.11	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM3_IN7_7			Mux input channel 7 of TIM module 3
	GTM_TIM5_IN3_10			Mux input channel 3 of TIM module 5
	CAN23_RXDE			CAN receive input node 3
	GPT122_T6EUDB			Count direction control input of core timer T6
	LETH0_P1_MII_RXD3B			LETH0 PortX MII receive data bit 3 (to be used with LETH0_P1_RXCLKB)
	P22.11	O0		General-purpose output
	GTM_TOUT137	O1		GTM muxed output
	ASCLIN4_ASLSO_F	O2		Slave select signal output
	—	O3		Reserved
	QSPI0_SLSO10	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT137	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P1_MIIC_TXEN	O11		LETH0 PortX MII transmit enable (to be used with LETH0_P1_TXCLKC)
	LETH0_P1_RMIIC_TXEN	O12		LETH0 PortX RMII transmit enable (to be used with LETH0_P1_REFCLKC)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_RMIIRC_TXEN	PO		LETH0 PortX RMII transmit enable (to be used with LETH0_P1_REFCLKC - registered*)

3.2.13 BGA436_STD port 23

Table 18 Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
AA23	P23.0	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN5_4			Mux input channel 5 of TIM module 0
	GTM_TIM1_IN5_4			Mux input channel 5 of TIM module 1
	GTM_TIM6_IN7_1			Mux input channel 7 of TIM module 6
	CAN10_RXDC			CAN receive input node 0
	QSPI6_SLSID_F			Slave select input
	EGTM_TIM0_IN5_4			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_4			Mux input channel 5 of TIM module 1
	P23.0	O0		General-purpose output
	GTM_TOUT41	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	QSPI6_SCLK	O7		Master SPI clock output
	QSPI6_MTSR	O8		Master SPI data output
	EGTM_TOUT41	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P1_MIIB_TXER	O12		LETH0 PortX MII transmit error (to be used with LETH0_P1_TXCLKB)
	LETH0_P1_MIIC_TXER	O13		LETH0 PortX MII transmit error (to be used with LETH0_P1_TXCLKC)
	—	O14		Reserved
	—	O15		Reserved
Y22	P23.1	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN6_4			Mux input channel 6 of TIM module 0
	GTM_TIM1_IN6_4			Mux input channel 6 of TIM module 1
	GTM_TIM6_IN6_1			Mux input channel 6 of TIM module 6
	MSC1_SDI0			Upstream asynchronous input signal
	ASCLIN6_ARXF_F			Receive input

(table continues...)

Table 18 (continued) Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GPT123_CAPINA			Trigger input to capture value of timer T5 into CAPREL register (input A)
	SCU_E_REQ6F			ERU channel 6 input F
	ADC_TRIG61			Triggers from PORTS to ADC
	QSPI0_MRSTD			Master SPI data input
	LETH0_P1_MII_RMII_RXD1B			LETH0 PortX MII and RMII receive data bit 1 (to be used with LETH0_P1_RXCLKB or LETH0_P1_REFCLKB)
	EGTM_TIM0_IN6_4			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN6_4			Mux input channel 6 of TIM module 1
	LETH0_P1_RXDG			LETH PortX TC14 interface receive data input
	P23.1	O0		General-purpose output
	GTM_TOUT42	O1		GTM muxed output
	ASCLIN1_ARTS	O2		Ready to send output
	QSPI4_SLSO6_F	O3		Master slave select output
	GTM_ECLK0	O4		CGM generated clock
	CAN10_TXD	O5		CAN transmit output node 0
	CLOCK_EXTCLK0	O6		External clock output 0
	ASCLIN6_ASCLK_F	O7		Shift clock output
	QSPI6_MTSR_F	O8		Master SPI data output
	EGTM_TOUT42	O9		eGTM muxed output
	EGTM_ECLK0	O10		CGM generated clock
	—	O11		Reserved
	QSPI6_SCLK_F	O12		Master SPI clock output
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
Y23	P23.2	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN6_5			Mux input channel 6 of TIM module 0
	GTM_TIM1_IN6_5			Mux input channel 6 of TIM module 1
	GTM_TIM6_IN5_1			Mux input channel 5 of TIM module 6
	ASCLIN7_ARXC			Receive input
	QSPI6_MRSTE_F			Master SPI data input

(table continues...)

Table 18 (continued) Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM0_IN6_5			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN6_5			Mux input channel 6 of TIM module 1
	P23.2	O0		General-purpose output
	GTM_TOUT43	O1		GTM muxed output
	—	O2		Reserved
	ASCLIN6_ASCLK_F	O3		Shift clock output
	CAN23_TXD	O4		CAN transmit output node 3
	CAN12_TXD	O5		CAN transmit output node 2
	CAN10_TXD	O6		CAN transmit output node 0
	QSPI6_SCLK_F	O7		Master SPI clock output
	QSPI6_SLSO3_F	O8		Master slave select output
	EGTM_TOUT43	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P1_MIIB_TXD3	O12		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P1_TXCLKB)
	LETH0_P1_MIIC_TXD3	O13		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P1_TXCLKC)
	—	O14		Reserved
	QSPI6_MTSR_F	O15		Master SPI data output
W22	P23.3	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN7_4			Mux input channel 7 of TIM module 0
	GTM_TIM1_IN7_4			Mux input channel 7 of TIM module 1
	GTM_TIM6_IN4_2			Mux input channel 4 of TIM module 6
	MSC1_INJ0			Injection signal from port
	ASCLIN6_ARXA_F			Receive input
	CAN12_RXDC			CAN receive input node 2
	CAN23_RXDB			CAN receive input node 3
	GPT122_CAPINB3			Trigger input to capture value of timer T5 into CAPREL register (input B)
	QSPI6_MTSRB_F			Slave SPI data input
	EGTM_TIM0_IN7_4			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_4			Mux input channel 7 of TIM module 1
	P23.3	O0		General-purpose output

(table continues...)

Table 18 (continued) Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TOUT44	O1		GTM muxed output
	ASCLIN7_ATX	O2		Transmit output
	—	O3		Reserved
	CAN23_TXD	O4		CAN transmit output node 3
	CAN12_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	QSPI6_SLSO0	O7		Master slave select output
	QSPI6_SCLK	O8		Master SPI clock output
	EGTM_TOUT44	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P1_MIIB_TXD2	O12		LETH0 PortX MII transmit data bit 2 (to be used with LETH0_P1_TXCLKB)
	LETH0_P1_MIIC_TXD2	O13		LETH0 PortX MII transmit data bit 2 (to be used with LETH0_P1_TXCLKC)
	—	O14		Reserved
	—	O15		Reserved
W23	P23.4	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN7_5			Mux input channel 7 of TIM module 0
	GTM_TIM1_IN7_5			Mux input channel 7 of TIM module 1
	GTM_TIM6_IN3_2			Mux input channel 3 of TIM module 6
	QSPI6_MRSTD_F			Master SPI data input
	EGTM_TIM0_IN7_5			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_5			Mux input channel 7 of TIM module 1
	P23.4	O0		General-purpose output
	GTM_TOUT45	O1		GTM muxed output
	ASCLIN6_ASLSO_F	O2		Slave select signal output
	QSPI4_SLSO5_F	O3		Master slave select output
	—	O4		Reserved
	MSC1_EN0	O5		Chip Select
	—	O6		Reserved
	—	O7		Reserved
	QSPI6_SLSO1_F	O8		Master slave select output

(table continues...)

Table 18 (continued) Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TOUT45	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P1_MIIB_TXD1	O12		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P1_TXCLKB)
	—	O13		Reserved
	LETH0_P1_RMIIB_TXD1	O14		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P1_REFCLKB)
	QSPI6_MTSR_F	O15		Master SPI data output
	LETH0_P1_RMIIRB_TXD1	PO		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P1_REFCLKB - registered*)
W20	P23.5	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN2_7			Mux input channel 2 of TIM module 0
	GTM_TIM1_IN2_7			Mux input channel 2 of TIM module 1
	GTM_TIM6_IN2_2			Mux input channel 2 of TIM module 6
	LETH0_P1_MII_RXD3C			LETH0 PortX MII receive data bit 3 (to be used with LETH0_P1_RXCLKC)
	EGTM_TIM0_IN2_7			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_7			Mux input channel 2 of TIM module 1
	P23.5	O0		General-purpose output
	GTM_TOUT46	O1		GTM muxed output
	ASCLIN6_ATX_F	O2		Transmit output
	QSPI4_SLSO4_F	O3		Master slave select output
	—	O4		Reserved
	MSC1_EN1	O5		Chip Select
	CAN22_TXD	O6		CAN transmit output node 2
	—	O7		Reserved
	QSPI6_SLSO2_F	O8		Master slave select output
	EGTM_TOUT46	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P1_MIIB_TXD0	O12		LETH0 PortX MII transmit data bit 0 (to be used with LETH0_P1_TXCLKB)
	—	O13		Reserved

(table continues...)

Table 18 (continued) Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_RMIIB_TXD0	O14		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P1_REFCLKB)
	LETH0_P1_TXD	O15		LETH0 PortX TC14 interface transmit data output
	LETH0_P1_RMIIRB_TXD0	PO		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P1_REFCLKB - registered*)
V20	P23.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM1_IN2_10			Mux input channel 2 of TIM module 1
	GTM_TIM4_IN2_7			Mux input channel 2 of TIM module 4
	GTM_TIM6_IN1_2			Mux input channel 1 of TIM module 6
	CAN22_RXDC			CAN receive input node 2
	QSPI6_MRSTA_F			Master SPI data input
	LETH0_P1_MII_RXD2B			LETH0 PortX MII receive data bit 2 (to be used with LETH0_P1_RXCLKB)
	LETH0_P1_MII_RXD2C			LETH0 PortX MII receive data bit 2 (to be used with LETH0_P1_RXCLKC)
	EGTM_TIM1_IN2_10			Mux input channel 2 of TIM module 1
	P23.6	O0		General-purpose output
	GTM_TOUT138	O1		GTM muxed output
	—	O2		Reserved
	ASCLIN6_ASLSO_F	O3		Slave select signal output
	QSPI0_SLSO11	O4		Master slave select output
	CAN11_TXD	O5		CAN transmit output node 1
	—	O6		Reserved
	QSPI6_SLSO14_F	O7		Master slave select output
	QSPI6_MRST_F	O8		Slave SPI data output
	EGTM_TOUT138	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	QSPI6_MTSR_F	O15		Master SPI data output
V19	P23.7	I	SLOW / PU1 /	General-purpose input
	GTM_TIM1_IN3_10			Mux input channel 3 of TIM module 1

(table continues...)

Table 18 (continued) Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TIM4_IN3_7		VDDEXT / ES	Mux input channel 3 of TIM module 4
	GTM_TIM6_IN0_2			Mux input channel 0 of TIM module 6
	CAN11_RXDC			CAN receive input node 1
	QSPI6_SCLKA_F			Slave SPI clock inputs
	LETH0_P1_MII_RMII_RXD1C			LETH0 PortX MII and RMII receive data bit 1 (to be used with LETH0_P1_RXCLKC or LETH0_P1_REFCLKC)
	EGTM_TIM1_IN3_10			Mux input channel 3 of TIM module 1
	P23.7	O0		General-purpose output
	GTM_TOUT139	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	QSPI6_SCLK	O8		Master SPI clock output
	EGTM_TOUT139	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

3.2.14 BGA436_STD port 24

Table 19 Port 24 functions

Ball	Symbol	Ctrl.	Buffer type	Function
L25	P24.0	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN0_8			Mux input channel 0 of TIM module 4
	GTM_TIM6_IN0_6			Mux input channel 0 of TIM module 6
	LETH0_P1_CRSC			LETH PortX MII carrier sense
	P24.0	O0		General-purpose output

(table continues...)

Table 19 (continued) Port 24 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TOUT222	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT222	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
L26	P24.1	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN1_8			Mux input channel 1 of TIM module 4
	GTM_TIM6_IN1_6			Mux input channel 1 of TIM module 6
	P24.1	O0		General-purpose output
	GTM_TOUT223	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT223	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved

(table continues...)

Table 19 (continued) Port 24 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O15		Reserved
K25	P24.2	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN2_8			Mux input channel 2 of TIM module 4
	GTM_TIM6_IN2_6			Mux input channel 2 of TIM module 6
	P24.2	O0		General-purpose output
	GTM_TOUT224	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT224	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
K26	P24.3	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN3_8			Mux input channel 3 of TIM module 4
	GTM_TIM6_IN3_6			Mux input channel 3 of TIM module 6
	P24.3	O0		General-purpose output
	GTM_TOUT225	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT225	O9		eGTM muxed output

(table continues...)

Table 19 (continued) Port 24 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
H25	P24.4	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN4_7			Mux input channel 4 of TIM module 4
	GTM_TIM6_IN4_5			Mux input channel 4 of TIM module 6
	P24.4	O0		General-purpose output
	GTM_TOUT226	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT226	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
H26	P24.5	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN5_7			Mux input channel 5 of TIM module 4
	GTM_TIM6_IN5_5			Mux input channel 5 of TIM module 6
	P24.5	O0		General-purpose output
	GTM_TOUT227	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved

(table continues...)

Table 19 (continued) Port 24 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT227	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
A24	P24.14	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM5_IN6_6			Mux input channel 6 of TIM module 5
	P24.14	O0		General-purpose output
	GTM_TOUT236	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT236	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

3.2.15 BGA436_STD port 25

Table 20 Port 25 functions

Ball	Symbol	Ctrl.	Buffer type	Function
AD26	P25.0	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM3_IN0_13			Mux input channel 0 of TIM module 3
	GTM_TIM6_IN0_7			Mux input channel 0 of TIM module 6
	P25.0	O0		General-purpose output
	GTM_TOUT206	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT206	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
AC26	P25.1	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM3_IN1_11			Mux input channel 1 of TIM module 3
	GTM_TIM6_IN1_7			Mux input channel 1 of TIM module 6
	SCU_E_REQ4G			ERU channel 4 input G
	QSPI6_MRSTB			Master SPI data input
	P25.1	O0		General-purpose output
	GTM_TOUT207	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

(table continues...)

Table 20 (continued) Port 25 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O8		Reserved
	EGTM_TOUT207	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
AB25	P25.2	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM3_IN2_9			Mux input channel 2 of TIM module 3
	GTM_TIM6_IN2_7			Mux input channel 2 of TIM module 6
	QSPI6_SCLKB			Slave SPI clock inputs
	P25.2	O0		General-purpose output
	GTM_TOUT208	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	QSPI6_SCLK	O8		Master SPI clock output
	EGTM_TOUT208	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
AB26	P25.3	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM3_IN3_9			Mux input channel 3 of TIM module 3
	GTM_TIM6_IN3_7			Mux input channel 3 of TIM module 6
	P25.3	O0		General-purpose output
	GTM_TOUT209	O1		GTM muxed output

(table continues...)

Table 20 (continued) Port 25 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	QSPI6_MTSR	O8		Master SPI data output
	EGTM_TOUT209	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
Y25	P25.4	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM3_IN4_10			Mux input channel 4 of TIM module 3
	GTM_TIM6_IN4_6			Mux input channel 4 of TIM module 6
	P25.4	O0		General-purpose output
	GTM_TOUT210	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	QSPI6_SLSO11	O8		Master slave select output
	EGTM_TOUT210	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 20 (continued) Port 25 functions

Ball	Symbol	Ctrl.	Buffer type	Function
Y26	P25.5	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM3_IN5_11			Mux input channel 5 of TIM module 3
	GTM_TIM6_IN5_6			Mux input channel 5 of TIM module 6
	P25.5	O0		General-purpose output
	GTM_TOUT211	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	QSPI6_SLSO12	O8		Master slave select output
	EGTM_TOUT211	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
N25	P25.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM3_IN6_15			Mux input channel 6 of TIM module 3
	GTM_TIM6_IN6_6			Mux input channel 6 of TIM module 6
	P25.6	O0		General-purpose output
	GTM_TOUT212	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	QSPI6_SLSO9	O8		Master slave select output
	EGTM_TOUT212	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 20 (continued) Port 25 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
W25	P25.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM3_IN7_10			Mux input channel 7 of TIM module 3
	GTM_TIM6_IN7_6			Mux input channel 7 of TIM module 6
	P25.7	O0		General-purpose output
	GTM_TOUT213	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	QSPI6_SLSO8	O8		Master slave select output
	EGTM_TOUT213	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
U25	P25.8	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN0_9			Mux input channel 0 of TIM module 4
	P25.8	O0		General-purpose output
	GTM_TOUT214	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—			

(table continues...)

Table 20 (continued) Port 25 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT214	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
W26	P25.9	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN1_9			Mux input channel 1 of TIM module 4
	P25.9	O0		General-purpose output
	GTM_TOUT215	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT215	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
T25	P25.10	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN2_9			Mux input channel 2 of TIM module 4
	P25.10	O0		General-purpose output
	GTM_TOUT216	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved

(table continues...)

Table 20 (continued) Port 25 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT216	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
U26	P25.11	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN3_9			Mux input channel 3 of TIM module 4
	P25.11	O0		General-purpose output
	GTM_TOUT217	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT217	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
P25	P25.12	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN4_8			Mux input channel 4 of TIM module 4
	P25.12	O0		General-purpose output

(table continues...)

Table 20 (continued) Port 25 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TOUT218	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT218	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
T26	P25.13	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN5_8			Mux input channel 5 of TIM module 4
	P25.13	O0		General-purpose output
	GTM_TOUT219	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT219	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 20 (continued) Port 25 functions

Ball	Symbol	Ctrl.	Buffer type	Function
P26	P25.14	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN6_8			Mux input channel 6 of TIM module 4
	P25.14	O0		General-purpose output
	GTM_TOUT220	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT220	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
N26	P25.15	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN7_8			Mux input channel 7 of TIM module 4
	P25.15	O0		General-purpose output
	GTM_TOUT221	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT221	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved

(table continues...)

Table 20 (continued) Port 25 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

3.2.16 BGA436_STD port 26

Table 21 Port 26 functions

Ball	Symbol	Ctrl.	Buffer type	Function
AC25	P26.0	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM3_IN6_11			Mux input channel 6 of TIM module 3
	GTM_TIM6_IN6_9			Mux input channel 6 of TIM module 6
	P26.0	O0		General-purpose output
	GTM_TOUT212	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT212	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

3.2.17 BGA436_STD port 30

Table 22 Port 30 functions

Ball	Symbol	Ctrl.	Buffer type	Function
AE14	P30.0	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN0_10			Mux input channel 0 of TIM module 4
	CAN10_RXDE			CAN receive input node 0
	LETH0_P1_REFCLKD			LETH0 PortX RMII reference clock
	LETH0_P1_RXCLKD			LETH PortX MII receive clock
	P30.0	O0		General-purpose output
	GTM_TOUT190	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT190	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
AF16	P30.1	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN1_10			Mux input channel 1 of TIM module 4
	LETH0_P1_MII_RXDVD			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	LETH0_P1_RMII_CRSDVD			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	P30.1	O0		General-purpose output
	GTM_TOUT191	O1		GTM muxed output
	—	O2		Reserved
	QSPI4_SLSO12	O3		Master slave select output
	—	O4		Reserved

(table continues...)

Table 22 (continued) Port 30 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CAN10_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	—	O7		Reserved
	QSPI6_MTSR	O8		Master SPI data output
	EGTM_TOUT191	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
AE16	P30.2	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN2_10			Mux input channel 2 of TIM module 4
	QSPI6_MRSTH			Master SPI data input
	LETH0_P1_MII_RXD3D			LETH0 PortX MII receive data bit 3 (to be used with LETH0_P1_RXCLKD)
	P30.2	O0		General-purpose output
	GTM_TOUT192	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	CAN21_TXD	O4		CAN transmit output node 1
	CAN12_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT192	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 22 (continued) Port 30 functions

Ball	Symbol	Ctrl.	Buffer type	Function
AF17	P30.3	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN3_10			Mux input channel 3 of TIM module 4
	ASCLIN6_ARXG			Receive input
	CAN12_RXDF			CAN receive input node 2
	CAN21_RXDH			CAN receive input node 1
	LETH0_P1_MII_RXD2D			LETH0 PortX MII receive data bit 2 (to be used with LETH0_P1_RXCLKD)
	P30.3	O0		General-purpose output
	GTM_TOUT193	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	QSPI6_SCLK	O8		Master SPI clock output
	EGTM_TOUT193	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
AE17	P30.4	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN4_9			Mux input channel 4 of TIM module 4
	LETH0_P1_MII_RMII_RXD1D			LETH0 PortX MII and RMII receive data bit 1 (to be used with LETH0_P1_RXCLKD or LETH0_P1_REFCLKD)
	P30.4	O0		General-purpose output
	GTM_TOUT194	O1		GTM muxed output
	—	O2		Reserved
	QSPI4_SLSO13	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved

(table continues...)

Table 22 (continued) Port 30 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT194	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
AF19	P30.5	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN5_9			Mux input channel 5 of TIM module 4
	LETH0_P1_MII_RMII_RXD0D			LETH0 PortX MII and RMII receive data bit 0 (to be used with LETH0_P1_RXCLKD or LETH0_P1_REFCLKD)
	LETH0_P1_RXDF			LETH PortX TC14 interface receive data input
	P30.5	O0		General-purpose output
	GTM_TOUT195	O1		GTM muxed output
	ASCLIN6_ATX	O2		Transmit output
	QSPI4_SLSO14	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	CAN22_TXD	O6		CAN transmit output node 2
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT195	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface

(table continues...)

Table 22 (continued) Port 30 functions

Ball	Symbol	Ctrl.	Buffer type	Function
AE19	P30.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN6_9			Mux input channel 6 of TIM module 4
	CAN22_RXDH			CAN receive input node 2
	QSPI6_MRSTG			Master SPI data input
	P30.6	O0		General-purpose output
	GTM_TOUT196	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	QSPI0_SLSO14	O4		Master slave select output
	CAN11_TXD	O5		CAN transmit output node 1
	—	O6		Reserved
	QSPI6_MRST	O7		Slave SPI data output
	—	O8		Reserved
	EGTM_TOUT196	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P1_MIID_TXD2	O11		LETH0 PortX MII transmit data bit 2 (to be used with LETH0_P1_TXCLKD)
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
AF20	P30.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM4_IN7_9			Mux input channel 7 of TIM module 4
	CAN11_RXDF			CAN receive input node 1
	QSPI6_SCLKD			Slave SPI clock inputs
	P30.7	O0		General-purpose output
	GTM_TOUT197	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	QSPI6_SCLK	O7		Master SPI clock output

(table continues...)

Table 22 (continued) Port 30 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O8		Reserved
	EGTM_TOUT197	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P1_MIID_TXD3	O11		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P1_TXCLKD)
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
AE20	P30.8	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM5_IN0_6			Mux input channel 0 of TIM module 5
	GTM_TIM6_IN0_8			Mux input channel 0 of TIM module 6
	P30.8	O0		General-purpose output
	GTM_TOUT198	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT198	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P1_MIID_TXER	O11		LETH0 PortX MII transmit error (to be used with LETH0_P1_TXCLKD)
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
AF22	P30.9	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM5_IN1_7			Mux input channel 1 of TIM module 5
	GTM_TIM6_IN1_8			Mux input channel 1 of TIM module 6
	P30.9	O0		General-purpose output

(table continues...)

Table 22 (continued) Port 30 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TOUT199	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT199	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P1_MIID_TXD0	O11		LETH0 PortX MII transmit data bit 0 (to be used with LETH0_P1_TXCLKD)
	LETH0_P1_RMIID_TXD0	O12		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P1_REFCLKD)
	LETH0_P1_TXD	O13		LETH PortX TC14 interface transmit data output
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_RMIIRD_TXD0	PO		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P1_REFCLKD - registered*)
AE22	P30.10	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM5_IN2_6			Mux input channel 2 of TIM module 5
	GTM_TIM6_IN2_8			Mux input channel 2 of TIM module 6
	P30.10	O0		General-purpose output
	GTM_TOUT200	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT200	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 22 (continued) Port 30 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_MIID_TXD1	O11		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P1_TXCLKD)
	LETH0_P1_RMIID_TXD1	O12		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P1_REFCLKD)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_RMIIRD_TXD1	PO		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P1_REFCLKD - registered*)
AF23	P30.11	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM5_IN3_7			Mux input channel 3 of TIM module 5
	GTM_TIM6_IN3_8			Mux input channel 3 of TIM module 6
	P30.11	O0		General-purpose output
	GTM_TOUT201	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	QSPI6_MRST	O7		Slave SPI data output
	—	O8		Reserved
	EGTM_TOUT201	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P1_MIID_TXEN	O11		LETH0 PortX MII transmit enable (to be used with LETH0_P1_TXCLKD)
	LETH0_P1_RMIID_TXEN	O12		LETH0 PortX RMII transmit enable (to be used with LETH0_P1_REFCLKD)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_RMIIRD_TXEN	PO		LETH0 PortX RMII transmit enable (to be used with LETH0_P1_REFCLKD - registered*)
AE23	P30.12	I	FAST / PU1 /	General-purpose input
	GTM_TIM5_IN4_6			Mux input channel 4 of TIM module 5

(table continues...)

Table 22 (continued) Port 30 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TIM6_IN4_7		VDDEXT / ES	Mux input channel 4 of TIM module 6
	LETH0_P1_MDIOF			LETH PortX MDIO interface data input
	LETH0_P1_EDF			LETH PortX TC14 interface energy detection input
	LETH0_P1_CRSD			LETH PortX MII carrier sense
	P30.12	O0	General-purpose output	
	GTM_TOUT202	O1	GTM muxed output	
	—	O2	Reserved	
	—	O3	Reserved	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	—	O7	Reserved	
	—	O8	Reserved	
	EGTM_TOUT202	O9	eGTM muxed output	
	—	O10	Reserved	
	—	O11	Reserved	
	—	O12	Reserved	
	—	O13	Reserved	
	—	O14	Reserved	
	—	O15	Reserved	
		LETH0_P1_MDIO	O	LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
AF24	P30.13	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM5_IN5_7			Mux input channel 5 of TIM module 5
	GTM_TIM6_IN5_7			Mux input channel 5 of TIM module 6
	P30.13	O0		General-purpose output
	GTM_TOUT203	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

(table continues...)

Table 22 (continued) Port 30 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O8		Reserved
	EGTM_TOUT203	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
AE24	P30.14	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM5_IN6_7			Mux input channel 6 of TIM module 5
	GTM_TIM6_IN6_7			Mux input channel 6 of TIM module 6
	P30.14	O0		General-purpose output
	GTM_TOUT204	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT204	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
AF25	P30.15	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM5_IN7_6			Mux input channel 7 of TIM module 5
	GTM_TIM6_IN7_7			Mux input channel 7 of TIM module 6
	P30.15	O0		General-purpose output
	GTM_TOUT205	O1		GTM muxed output
	—	O2		Reserved

(table continues...)

Table 22 (continued) Port 30 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT205	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

3.2.18 BGA436_STD port 31

Table 23 Port 31 functions

Ball	Symbol	Ctrl.	Buffer type	Function
AF10	P31.0	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM2_IN0_10			Mux input channel 0 of TIM module 2
	EGTM_TIM2_IN0_10			Mux input channel 0 of TIM module 2
	ADC_TMADC4CH2	AI		Analog Input for TMADC4 Channel 2
	P31.0	O0		General-purpose output
	GTM_TOUT174	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT174	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 23 (continued) Port 31 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
AF8	P31.1	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM2_IN1_9			Mux input channel 1 of TIM module 2
	EGTM_TIM2_IN1_9			Mux input channel 1 of TIM module 2
	ADC_TMADC4CH1	AI		Analog Input for TMADC4 Channel 1
	P31.1	O0		General-purpose output
	GTM_TOUT175	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT175	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
AE10	P31.2	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM2_IN2_9			Mux input channel 2 of TIM module 2
	LETH0_P1_COLD			LETH PortX MII collision detection
	EGTM_TIM2_IN2_9			Mux input channel 2 of TIM module 2
	ADC_TMADC4CH0	AI		Analog Input for TMADC4 Channel 0
	P31.2	O0		General-purpose output
	GTM_TOUT176	O1		GTM muxed output
	—	O2		Reserved

(table continues...)

Table 23 (continued) Port 31 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT176	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
AF11	P31.3	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM2_IN3_10			Mux input channel 3 of TIM module 2
	EGTM_TIM2_IN3_10			Mux input channel 3 of TIM module 2
	P31.3	O0		General-purpose output
	GTM_TOUT177	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT177	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 23 (continued) Port 31 functions

Ball	Symbol	Ctrl.	Buffer type	Function
AE11	P31.4	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM2_IN4_10			Mux input channel 4 of TIM module 2
	EGTM_TIM2_IN4_10			Mux input channel 4 of TIM module 2
	P31.4	O0		General-purpose output
	GTM_TOUT178	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT178	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
AF13	P31.5	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM2_IN5_11			Mux input channel 5 of TIM module 2
	EGTM_TIM2_IN5_11			Mux input channel 5 of TIM module 2
	P31.5	O0		General-purpose output
	GTM_TOUT179	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT179	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 23 (continued) Port 31 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
AE13	P31.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM2_IN6_10			Mux input channel 6 of TIM module 2
	SENT1_SENT13D			Receive input channel 13
	LETH0_P1_MII_RXERD			LETH0 PortX MII receive error (to be used with LETH0_P1_RXCLKD)
	EGTM_TIM2_IN6_10			Mux input channel 6 of TIM module 2
	P31.6	O0		General-purpose output
	GTM_TOUT180	O1		GTM muxed output
	SENT1_SPC13	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	CAN32_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT180	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
AF14	P31.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM2_IN7_11			Mux input channel 7 of TIM module 2
	SENT0_SENT14C			Receive input channel 14
	CAN32_RXDE			CAN receive input node 2
	EGTM_TIM2_IN7_11			Mux input channel 7 of TIM module 2
	LETH0_P1_TXCLKD			LETH PortX MII transmit clock

(table continues...)

Table 23 (continued) Port 31 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	P31.7	O0		General-purpose output
	GTM_TOUT181	O1		GTM muxed output
	SENT0_SPC14	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT181	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

3.2.19 BGA436_STD port 32

Table 24 Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
AB21	P32.2	I	FAST / PU1 / VDDEVRS B / ES	General-purpose input
	GTM_TIM0_IN3_8			Mux input channel 3 of TIM module 0
	GTM_TIM1_IN3_8			Mux input channel 3 of TIM module 1
	CAN03_RXDB			CAN receive input node 3
	ASCLIN3_ARXD			Receive input
	CAN21_RXDD			CAN receive input node 1
	SMU_FSPIN2			FSP Status Input - Shows the actual state of the FSP ErrroPin
	EGTM_TIM0_IN3_8			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_8			Mux input channel 3 of TIM module 1
	UART_RXDH	I#	Receive input H	
	WCAN_RXDF		Wake-up input F	
	T0D		T0 capture input D	

(table continues...)

Table 24 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	T21EXG			T21 interrupt input G
	EXINT7			Interrupt 7 input
	P32.2	O0		General-purpose output
	GTM_TOUT38	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	PMS_DCDCSYNCO	O6		DC-DC synchronization output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT38	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P2.0	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_4	O#5		T2 PWM channel 04
	—	O#6		Reserved
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved

(table continues...)

Table 24 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#15		Reserved
	SMU_FSP2	O		FSP Output Signal - Generated by SMU
AB20	P32.4	I	FAST / PU1 / VDDEVRS B / ES	General-purpose input
	GTM_TIM0_IN5_5			Mux input channel 5 of TIM module 0
	GTM_TIM1_IN5_5			Mux input channel 5 of TIM module 1
	ASCLIN1_ACTSB			Clear to send input
	MSC1_SDI2			Upstream assynchronous input signal
	I2C0_SCLD			Serial Clock Input 3
	EGTM_TIM0_IN5_5			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_5			Mux input channel 5 of TIM module 1
	SSC_MRSTD	I#		Master SPI data input D
	T21EXA			T21 interrupt input A
	T2CCU1_0A			T2 capture 1 input 0A
	EXINT8A			Interrupt 8 input A
	EXINT12A			Interrupt 12 input A
	I2CSCLA			Serial clock input A
	P32.4	O0		General-purpose output
	GTM_TOUT40	O1		GTM muxed output
	ASCLIN6_ATX	O2		Transmit output
	CAN03_TXD	O3		CAN transmit output node 3
	GTM_ECLK1	O4		CGM generated clock
	MSC1_EN0	O5		Chip Select
	CLOCK_EXTCLK1	O6		External clock output 1
	CAN21_TXD	O7		CAN transmit output node 1
	I2C0_SCL	O8		Serial Clock Output
	EGTM_TOUT40	O9		eGTM muxed output
	EGTM_ECLK1	O10		CGM generated clock
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P2.1	O#0		General-purpose output

(table continues...)

Table 24 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#1		Reserved
	SSC_MRST	O#2		Slave SPI data output
	T20EXF2	O#3		Timer 20 external overflow
	—	O#4		Reserved
	T2CCU0_5	O#5		T2 PWM channel 05
	T2CCU1_0	O#6		T2 PWM channel 10
	I2CSCL	O#7		Serial clock output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	PMS_DCDCSYNCO	O		DC-DC synchronization output
W18	P32.5	I	FAST / PU1 / VDDEVRS B / ES	General-purpose input
	GTM_TIM3_IN5_8			Mux input channel 5 of TIM module 3
	GTM_TIM4_IN1_14			Mux input channel 1 of TIM module 4
	GTM_TIM5_IN5_9			Mux input channel 5 of TIM module 5
	SENT0_SENT5C			Receive input channel 5
	SMU_FSPIN3			FSP Status Input - Shows the actual state of the FSP ErroPin
	EGTM_TIM0_IN4_5			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_5			Mux input channel 4 of TIM module 1
	SSC_MTSRD	I#		Slave SPI data input D
	PINRSTC			Reset input C
	T20EXO			T20 interrupt input O
	T2CCU1_1A			T2 capture 1 input 1A
	EXINT9A			Interrupt 9 input A
	EXINT13A			Interrupt 13 input A
	P32.5	O0		General-purpose output
	GTM_TOUT140	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output

(table continues...)

Table 24 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SENT0_SPC5	O3		Transmit output
	ASCLIN5_ASLSO_F	O4		Slave select signal output
	—	O5		Reserved
	CAN02_TXD	O6		CAN transmit output node 2
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT140	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P2.2	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	SSC_MTSR	O#2		Master SPI data output
	—	O#3		Reserved
	T21EXF2	O#4		Timer 21 external overflow
	—	O#5		Reserved
	T2CCU1_1	O#6		T2 PWM channel 11
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	SMU_FSP3	O		FSP Output Signal - Generated by SMU
Y18	P32.6	I	SLOW / PU1 / VDDEVRS B / ES	General-purpose input
	GTM_TIM3_IN6_8			Mux input channel 6 of TIM module 3
	GTM_TIM4_IN4_15			Mux input channel 4 of TIM module 4

(table continues...)

Table 24 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TIM5_IN6_9			Mux input channel 6 of TIM module 5
	CAN02_RXDC			CAN receive input node 2
	CBS_TGI4			Trigger input
	ASCLIN2_ARXF			Receive input
	ASCLIN6_ARXC			Receive input
	SENT1_SENT5C			Receive input channel 5
	I2C0_SDAD			Serial Data Input 3
	UART_RXDI	I#		Receive input I
	T1D			T1 capture input D
	T21A			T21 capture input A
	T2CCU1_2A			T2 capture 1 input 2A
	EXINT10A			Interrupt 10 input A
	EXINT14A			Interrupt 14 input A
	I2CSDAA			Serial data input A
	P32.6	O0		General-purpose output
	GTM_TOUT141	O1		GTM muxed output
	—	O2		Reserved
	SENT1_SPC5	O3		Transmit output
	—	O4		Reserved
	CAN22_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	—	O7		Reserved
	I2C0_SDA	O8		Serial Data Output
	EGTM_TOUT141	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P1_PPS	O12		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P2.3	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional receive pin O

(table continues...)

Table 24 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	—	O#5		Reserved
	T2CCU1_2	O#6		T2 PWM channel 12
	I2CSDA	O#7		Serial data output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	CBS_TGO4	O		Trigger output
Y19	P32.7	I	SLOW / PU1 / VDDEVRS B / ES	General-purpose input
	GTM_TIM3_IN7_8			Mux input channel 7 of TIM module 3
	GTM_TIM4_IN0_15			Mux input channel 0 of TIM module 4
	GTM_TIM5_IN7_8			Mux input channel 7 of TIM module 5
	CBS_TGI5			Trigger input
	CAN22_RXDB			CAN receive input node 2
	SENT0_SENT6C			Receive input channel 6
	ADC_SIGN0			Sign for Carrier Cancellation
	LETH0_P1_MII_RXERB			LETH0 PortX MII receive error (to be used with LETH0_P1_RXCLKB)
	WCAN_RXDH	I#		Wake-up input H
	T20EXH			T20 interrupt input H
	T2CCU1_3A			T2 capture 1 input 3A
	EXINT11A			Interrupt 11 input A
	EXINT15A			Interrupt 15 input A
	P32.7	O0		General-purpose output
	GTM_TOUT142	O1		GTM muxed output
	ASCLIN6_ATX	O2		Transmit output

(table continues...)

Table 24 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SENT0_SPC6	O3		Transmit output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT142	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P2.4	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	—	O#5		Reserved
	T2CCU1_3	O#6		T2 PWM channel 13
	PMSRTC32_OUT	O#7		RTC oscillator output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	CBS_TGO5	O		Trigger output

3.2.20 BGA436_STD port 33

Table 25 Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function	
AB13	P33.0	I	SLOW / PU1 / VDDEVRS B / ES5	General-purpose input	
	GTM_TIM0_IN4_6			Mux input channel 4 of TIM module 0	
	GTM_TIM1_IN4_6			Mux input channel 4 of TIM module 1	
	GTM_TIM3_IN0_14			Mux input channel 0 of TIM module 3	
	SENT1_SENT9B			Receive input channel 9	
	GPT122_T6INA			Trigger/gate input of core timer T6	
	GTM_CDTM1_DTM0_3			Input mux of CDTM1_DTM0_AUXIN0/1	
	GTM_CDTM1_DTM1_3			Input mux of CDTM1_DTM1_AUXIN0/1	
	EGTM_CDTM1_DTM0_3			Input mux of CDTM1_DTM0_AUXIN0/1	
	EGTM_CDTM1_DTM1_3			Input mux of CDTM1_DTM1_AUXIN0/1	
	EGTM_CDTM1_DTM2_3			Input mux of CDTM1_DTM2_AUXIN0/1	
	EGTM_CDTM1_DTM3_3			Input mux of CDTM1_DTM3_AUXIN0/1	
	EGTM_TIM0_IN4_6			Mux input channel 4 of TIM module 0	
	EGTM_TIM1_IN4_6			Mux input channel 4 of TIM module 1	
	T21EXB			I#	T20 interrupt input B
	T2CCU0_0A				T2 capture 0 input 0A
	EXINT3A	Interrupt 3 input A			
	EXINT12B	Interrupt 12 input B			
	ADCOMPCH0	Analog input channel 0			
	ADC_TMADC4CH10	AI	Analog Input for TMADC4 Channel 10		
	P33.0	O0		General-purpose output	
	GTM_TOUT22	O1		GTM muxed output	
	ASCLIN5_ATX	O2		Transmit output	
	SENT1_SPC9	O3		Transmit output	
	—	O4		Reserved	
	ADC_EMUXCTRL03	O5		EMUX0 Control from TMADC to PORTS	
	ADC_BFL2	O6		Boundary flags from FCC	
	PSI5S1_TX	O7		TX data output	
	—	O8		Reserved	
	EGTM_TOUT22	O9		eGTM muxed output	
	—	O10		Reserved	
	—	O11		Reserved	

(table continues...)

Table 25 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.0	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_0	O#5		T2 PWM channel 00
	T2CCU1_4	O#6		T2 PWM channel 14
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
AC13	P33.1	I	SLOW / PU1 / VDDEVRS B / ES5	General-purpose input
	GTM_TIM0_IN5_6			Mux input channel 5 of TIM module 0
	GTM_TIM1_IN5_6			Mux input channel 5 of TIM module 1
	GTM_TIM3_IN1_14			Mux input channel 1 of TIM module 3
	PSI5_RX0C			RXD inputs (receive data) channel 0
	ADC_CLKIN2			Clock input to EXMOD
	SENT0_SENT9B			Receive input channel 9
	GPT122_CAPINA			Trigger input to capture value of timer T5 into CAPREL register (input A)
	EGTM_TIM0_IN5_6			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_6			Mux input channel 5 of TIM module 1
	UART_RXDK			I#
	SSC_SCLKD	Slave SPI clock input D		

(table continues...)

Table 25 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	T0A			T0 capture input A
	T20EXA			T2 interrupt input A
	T2CCU0_1A			T2 capture 0 input 1A
	EXINT4A			Interrupt 4 input A
	EXINT13B			Interrupt 13 input B
	ADCOMPCH1			Analog input channel 1
	ADC_TMADC4CH9	AI		Analog Input for TMADC4 Channel 9
	P33.1	O0		General-purpose output
	GTM_TOUT23	O1		GTM muxed output
	ASCLIN3_ASLSO	O2		Slave select signal output
	QSPI2_SCLK	O3		Master SPI clock output
	ADC_CLKOUT1	O4		Clock output from EXMOD
	ADC_EMUXCTRL02	O5		EMUX0 Control from TMADC to PORTS
	ADC_BFL4	O6		Boundary flags from FCC
	SENT0_SPC9	O7		Transmit output
	PSI5S1_CLK	O8		PSI5S CLK is a clock that can be used on a pin to drive the external PHY.
	EGTM_TOUT23	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.1	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional receive pin O
	SSC_SCLK	O#2		Clock output
	—	O#3		Reserved
	T21EXF2	O#4		Timer 21 external overflow
	T2CCU0_1	O#5		T2 PWM channel 01
	T2CCU1_5	O#6		T2 PWM channel 15
	—	O#7		Reserved
	—	O#8		Reserved

(table continues...)

Table 25 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
AB14	P33.2	I	SLOW / PU1 / VDDEVRS B / ES5	General-purpose input
	GTM_TIM0_IN6_6			Mux input channel 6 of TIM module 0
	GTM_TIM1_IN6_6			Mux input channel 6 of TIM module 1
	GTM_TIM3_IN2_13			Mux input channel 2 of TIM module 3
	SENT1_SENT8B			Receive input channel 8
	ADC_DATA2			Modulated data to EXMOD
	GPT120_CAPINB3			Trigger input to capture value of timer T5 into CAPREL register (input B)
	EGTM_TIM0_IN6_6			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN6_6			Mux input channel 6 of TIM module 1
	WCAN_RXDE	I#		Wake-up input E
	SCRDAP0_1			SCRDAP0 input
	T21B			T21 capture input B
	T2CCU0_2A			T2 capture 0 input 2A
	EXINT5A			Interrupt 5 input A
	EXINT14B			Interrupt 14 input B
	ADCOMPCH2			Analog input channel 2
	ADC_TMADC4CH8	AI		Analog Input for TMADC4 Channel 8
	P33.2	O0		General-purpose output
	GTM_TOUT24	O1		GTM muxed output
	ASCLIN3_ASCLK	O2		Shift clock output
	QSPI2_SLSO10	O3		Master slave select output
	PSI5_TX0	O4		TXD outputs (send data)
	ADC_EMUXCTRL01	O5		EMUX0 Control from TMADC to PORTS
	ADC_BFL3	O6		Boundary flags from FCC
	—	O7		Reserved

(table continues...)

Table 25 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SENT1_SPC8	O8		Transmit output
	EGTM_TOUT24	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	GPT122_T3OUT	O12		External output for overflow/underflow detection of core timer T3
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.2	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	—	O#2		Reserved
	T20EXF2	O#3		Timer 20 external overflow
	—	O#4		Reserved
	T2CCU0_2	O#5		T2 PWM channel 02
	—	O#6		Reserved
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
AC14	P33.3	I	SLOW / PU1 / VDDEVRS B / ES5	General-purpose input
	GTM_TIM0_IN7_6			Mux input channel 7 of TIM module 0
	GTM_TIM1_IN7_6			Mux input channel 7 of TIM module 1
	GTM_TIM3_IN3_13			Mux input channel 3 of TIM module 3
	PSI5_RX1C			RXD inputs (receive data) channel 1
	SENT0_SENT8B			Receive input channel 8
	ADC_CLKIN1			Clock input to EXMOD
	EGTM_TIM0_IN7_6			Mux input channel 7 of TIM module 0

(table continues...)

Table 25 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM1_IN7_6			Mux input channel 7 of TIM module 1
	UART_RXDP	I#		Receive input P
	T20A			T20 capture input A
	T2CCU0_3A			T2 capture 0 input 3A
	EXINT6A			Interrupt 6 input A
	EXINT15B			Interrupt 15 input B
	ADCOMPCH3			Analog input channel 3
	ADC_TMADC4CH7	AI		Analog Input for TMADC4 Channel 7
	P33.3	O0		General-purpose output
	GTM_TOUT25	O1		GTM muxed output
	ASCLIN5_ASCLK	O2		Shift clock output
	QSPI4_SLSO2	O3		Master slave select output
	ADC_CLKOUT2	O4		Clock output from EXMOD
	ADC_EMUXCTRL00	O5		EMUX0 Control from TMADC to PORTS
	ADC_BFL5	O6		Boundary flags from FCC
	—	O7		Reserved
	SENT0_SPC8	O8		Transmit output
	EGTM_TOUT25	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	GPT122_T6OUT	O12		External output for overflow/underflow detection of core timer T6
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.3	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional receive pin O
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_3	O#5		T2 PWM channel 03
	—	O#6		Reserved
	—	O#7		Reserved

(table continues...)

Table 25 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	SCRDAP1_1	I/O		SCRDAP1 input
	SPD_1	I/O		Single pin DAP1
AB15	P33.4	I	SLOW / PU1 / VDDEVRS B / ES5	General-purpose input
	GTM_TIM0_IN0_10			Mux input channel 0 of TIM module 0
	GTM_TIM1_IN0_10			Mux input channel 0 of TIM module 1
	GTM_TIM4_IN4_10			Mux input channel 4 of TIM module 4
	SENT1_SENT7B			Receive input channel 7
	ADC_DATA1			Modulated data to EXMOD
	ASCLIN5_ARXB_F			Receive input
	GTM_CDTM2_DTM0_1			Input mux of CDTM2_DTM0_AUXIN0/1
	GTM_CDTM2_DTM1_1			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_CDTM2_DTM0_1			Input mux of CDTM2_DTM0_AUXIN0/1
	EGTM_CDTM2_DTM1_1			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_CDTM2_DTM2_1			Input mux of CDTM2_DTM2_AUXIN0/1
	EGTM_CDTM2_DTM3_1			Input mux of CDTM2_DTM3_AUXIN0/1
	EGTM_TIM0_IN0_10			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_10			Mux input channel 0 of TIM module 1
	UART_RXDC	I#		Receive input C
	WCAN_RXDP			Wake-up input P
	T1B			T1 capture input B
	T2CCU0_3D			T2 capture 0 input 3D
	EXINT0A			Interrupt 0 input A
	EXINT6D			Interrupt 6 input D
	EXINT12C			Interrupt 12 input C
	ADCOMPCH4			Analog input channel 4

(table continues...)

Table 25 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ADC_TMADC4CH6	AI		Analog Input for TMADC4 Channel 6
	P33.4	O0		General-purpose output
	GTM_TOUT26	O1		GTM muxed output
	ASCLIN2_ARTS	O2		Ready to send output
	QSPI2_SLSO12	O3		Master slave select output
	PSI5_TX1	O4		TXD outputs (send data)
	ADC_EMUXCTRL12	O5		EMUX1 Control from TMADC to PORTS
	ADC_BFL0	O6		Boundary flags from FCC
	CAN13_TXD	O7		CAN transmit output node 3
	SENT1_SPC7	O8		Transmit output
	EGTM_TOUT26	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.4	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional receive pin O
	—	O#2		Reserved
	—	O#3		Reserved
	T21EXF2	O#4		Timer 21 external overflow
	T2CCU0_4	O#5		T2 PWM channel 04
	—	O#6		Reserved
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved

(table continues...)

Table 25 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function	
AC15	P33.5	I	SLOW / PU1 / VDDEVRS B / ES5	General-purpose input	
	GTM_TIM0_IN1_8			Mux input channel 1 of TIM module 0	
	GTM_TIM1_IN1_8			Mux input channel 1 of TIM module 1	
	GTM_TIM4_IN5_10			Mux input channel 5 of TIM module 4	
	ADC_CLKIN0			Clock input to EXMOD	
	GPT120_T4EUDB			Count direction control input of timer T4	
	PSI5S0_RXC			RX data input	
	ASCLIN2_ACTSB			Clear to send input	
	PSI5_RX2C			RXD inputs (receive data) channel 2	
	SENT1_SENT2C			Receive input channel 2	
	CAN13_RXDB			CAN receive input node 3	
	QSPI4_MRSTG			Master SPI data input	
	EGTM_TIM0_IN1_8			Mux input channel 1 of TIM module 0	
	EGTM_TIM1_IN1_8			Mux input channel 1 of TIM module 1	
	WCAN_RXDD			I#	Wake-up input D
	SSC_MRSTA				Master SPI data input A
	T0B	T0 capture input B			
	T20EXB	T20 interrupt input B			
	EXINT1A	Interrupt 1 input A			
	EXINT13C	Interrupt 13 input C			
	ADCOMPCH5	Analog input channel 5			
	ADC_TMADC4CH5	AI	Analog Input for TMADC4 Channel 5		
	P33.5	O0	General-purpose output		
	GTM_TOUT27	O1	GTM muxed output		
	QSPI0_SLSO7	O2	Master slave select output		
	QSPI1_SLSO7	O3	Master slave select output		
	ADC_CLKOUT3	O4	Clock output from EXMOD		
	ADC_EMUXCTRL11	O5	EMUX1 Control from TMADC to PORTS		
	ADC_BFL2	O6	Boundary flags from FCC		
	ASCLIN5_ASLSO	O7	Slave select signal output		
	—	O8	Reserved		
	EGTM_TOUT27	O9	eGTM muxed output		
	—	O10	Reserved		

(table continues...)

Table 25 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.5	O#0		General-purpose output
	—	O#1		Reserved
	SSC_MRST	O#2		Slave SPI data output
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_5	O#5		T2 PWM channel 05
	—	O#6		Reserved
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
AB16	P33.6	I	SLOW / PU1 / VDDEVRS B / ES5	General-purpose input
	GTM_TIM0_IN2_9			Mux input channel 2 of TIM module 0
	GTM_TIM1_IN2_9			Mux input channel 2 of TIM module 1
	GPT120_T2EUDB			Count direction control input of timer T2
	SENT0_SENT12B			Receive input channel 12
	ADC_DATA0			Modulated data to EXMOD
	GPT122_T2INA			Trigger/gate input of timer T2
	GTM_CDTM2_DTM0_2			Input mux of CDTM2_DTM0_AUXIN0/1
	GTM_CDTM2_DTM1_2			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_CDTM2_DTM0_2			Input mux of CDTM2_DTM0_AUXIN0/1
	EGTM_CDTM2_DTM1_2			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_CDTM2_DTM2_2			Input mux of CDTM2_DTM2_AUXIN0/1

(table continues...)

Table 25 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_CDTM2_DTM3_2	I#		Input mux of CDTM2_DTM3_AUXIN0/1
	EGTM_TIM0_IN2_9			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_9			Mux input channel 2 of TIM module 1
	UART_RXDL			Receive input L
	SSC_MTSRA			Slave SPI data input A
	SCRDAP0_0			SCRDAP0 input
	T2CCU1_0B			T2 capture 1 input 0B
	EXINT2A			Interrupt 2 input A
	EXINT8B			Interrupt 8 input B
	ADCOMPCH6			Analog input channel 6
	ADC_TMADC4CH4	AI		Analog Input for TMADC4 Channel 4
	P33.6	O0		General-purpose output
	GTM_TOUT28	O1		GTM muxed output
	ASCLIN2_ASLSO	O2		Slave select signal output
	QSPI2_SLSO11	O3		Master slave select output
	PSI5_TX2	O4		TXD outputs (send data)
	ADC_EMUXCTRL10	O5		EMUX1 Control from TMADC to PORTS
	ADC_BFL1	O6		Boundary flags from FCC
	PSI5S0_TX	O7		TX data output
	SENT0_SPC12	O8		Transmit output
	EGTM_TOUT28	O9		eGTM muxed output
	QSPI4_MTSR	O10		Master SPI data output
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.6	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional receive pin O
	SSC_MTSR	O#2		Master SPI data output
	T20EXF2	O#3		Timer 20 external overflow
	—	O#4		Reserved
	—	O#5		Reserved

(table continues...)

Table 25 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	T2CCU1_0	O#6		T2 PWM channel 10
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
AC16	P33.7	I	SLOW / PU1 / VDDEVRS B / ES5	General-purpose input
	GTM_TIM0_IN3_9			Mux input channel 3 of TIM module 0
	GTM_TIM1_IN3_9			Mux input channel 3 of TIM module 1
	CAN00_RXDE			CAN receive input node 0
	GPT120_T2INB			Trigger/gate input of timer T2
	PSI5S0_RXD			RX data input
	SCU_E_REQ4A			ERU channel 4 input A
	SENT1_SENT11B			Receive input channel 11
	GPT122_T2EUDA			Count direction control input of timer T2
	ADC_TRIG60			Triggers from PORTS to ADC
	EGTM_TIM0_IN3_9			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_9			Mux input channel 3 of TIM module 1
	WCAN_RXDB	I#		Wake-up input B
	SSC_SCLKA			Slave SPI clock input A
	T20B			T20 capture input B
	T21EXH			T21 interrupt input H
	T2CCU1_1B			T2 capture 1 input 1B
	EXINT0B			Interrupt 0 input B
	EXINT9B			Interrupt 9 input B
	ADCOMPCH7			Analog input channel 7
	ADC_TMADC4CH3	AI		Analog Input for TMADC4 Channel 3
	P33.7	O0		General-purpose output
	GTM_TOUT29	O1		GTM muxed output

(table continues...)

Table 25 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN2_ASCLK	O2		Shift clock output
	QSPI4_SLSO7	O3		Master slave select output
	—	O4		Reserved
	ADC_EMUXCTRL13	O5		EMUX1 Control from TMADC to PORTS
	—	O6		Reserved
	QSPI5_SLSO10	O7		Master slave select output
	SENT1_SPC11	O8		Transmit output
	EGTM_TOUT29	O9		eGTM muxed output
	QSPI4_SCLK	O10		Master SPI clock output
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.7	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	SSC_SCLK	O#2		Clock output
	—	O#3		Reserved
	—	O#4		Reserved
	—	O#5		Reserved
	T2CCU1_1	O#6		T2 PWM channel 11
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	SCRDAP1_0	I/O		SCRDAP1 input
	SPD_0	I/O		Single pin DAP0

(table continues...)

Table 25 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
AB17	P33.8	I	FAST / HighZ / VDDEVRS B	General-purpose input
	GTM_TIM0_IN4_7			Mux input channel 4 of TIM module 0
	GTM_TIM1_IN4_7			Mux input channel 4 of TIM module 1
	ASCLIN2_ARXE			Receive input
	SMU_EXT_EMERGENCYSTOP_A_REQ			Emergency Stop External Request A
	SMU_FSPIN0			FSP Status Input - Shows the actual state of the FSP ErroPin
	EGTM_TIM0_IN4_7			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_7			Mux input channel 4 of TIM module 1
	UART_RXDF	I#		Receive input F
	WCAN_RXDO			Wake-up input O
	T21EXN			T21 interrupt input N
	T2CCU1_3D			T2 capture 1 input 3D
	EXINT1B			Interrupt 1 input B
	EXINT11D			Interrupt 11 input D
	I2CSDAD			Serial clock input D
	P33.8	O0		General-purpose output
	GTM_TOUT30	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	QSPI4_SLSO2	O3		Master slave select output
	—	O4		Reserved
	CAN00_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	QSPI5_SLSO11_F	O7		Master slave select output
	QSPI6_SLSO13	O8		Master slave select output
	EGTM_TOUT30	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.0	O#0		General-purpose output

(table continues...)

Table 25 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#1		Reserved
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	—	O#5		Reserved
	—	O#6		Reserved
	I2CSDA	O#7		Serial data output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	SMU_FSP0	O		FSP Output Signal - Generated by SMU
AC17	P33.9	I	SLOW / PU1 / VDDEVRS B / ES5	General-purpose input
	GTM_TIM0_IN1_9			Mux input channel 1 of TIM module 0
	GTM_TIM1_IN1_9			Mux input channel 1 of TIM module 1
	XTAL3			XTAL3.RTC Oscillator
	GPT122_T4EUDA			Count direction control input of timer T4
	EGTM_TIM0_IN1_9			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_9			Mux input channel 1 of TIM module 1
	T1A	I#		T1 capture input A
	T20EXC			T2 interrupt input C
	T2CCU0_0B			T2 capture 0 input 0B
	EXINT3B			Interrupt 3 input B
	EXINT14C			Interrupt 14 input C
	I2CSCLD			Serial clock input D
	P33.9	O0		General-purpose output
	GTM_TOUT31	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	QSPI4_SLSO1	O3		Master slave select output

(table continues...)

Table 25 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN2_ASCLK	O4		Shift clock output
	CAN01_TXD	O5		CAN transmit output node 1
	ASCLIN0_ATX	O6		Transmit output
	QSPI5_SLSO12	O7		Master slave select output
	QSPI6_SLSO10	O8		Master slave select output
	EGTM_TOUT31	O9		eGTM muxed output
	—	O10		Reserved
	ADC_BFL8	O11		Boundary flags from FCC
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.1	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_0	O#5		T2 PWM channel 00
	—	O#6		Reserved
	I2CSCL	O#7		Serial clock output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
AB18	P33.10	I	SLOW / PU1 / VDDEVRS B / ES5	General-purpose input
	GTM_TIM0_IN0_9			Mux input channel 0 of TIM module 0
	GTM_TIM1_IN0_9			Mux input channel 0 of TIM module 1
	GTM_TIM4_IN4_14			Mux input channel 4 of TIM module 4
	QSPI4_SLSIA			Slave select input

(table continues...)

Table 25 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CAN01_RXDD	I#		CAN receive input node 1
	ASCLIN0_ARXD			Receive input
	EGTM_TIM0_IN0_9			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_9			Mux input channel 0 of TIM module 1
	UART_RXDA			Receive input A
	WCAN_RXDA			Wake-up input A
	RTC32_IN			RTC oscillator input
	T20EXP			T20 interrupt input P
	T21EXK			T21 interrupt input K
	EXINT2B			Interrupt 2 input B
	EXINT15C			Interrupt 15 input C
	P33.10	O0		General-purpose output
	GTM_TOUT32	O1		GTM muxed output
	QSPI1_SLSO6	O2		Master slave select output
	QSPI4_SLSO0	O3		Master slave select output
	ASCLIN1_ASLSO	O4		Slave select signal output
	PSI5S0_CLK	O5		PSI5S CLK is a clock that can be used on a pin to drive the external PHY.
	—	O6		Reserved
	QSPI5_SLSO13	O7		Master slave select output
	—	O8		Reserved
	EGTM_TOUT32	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.2	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional receive pin O
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved

(table continues...)

Table 25 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#5		Reserved
	—	O#6		Reserved
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	XTAL4	PO		XTAL4. RTC Oscillator
AC18	P33.11	I	FAST / PU1 / VDDEVRS B / ES5	General-purpose input
	GTM_TIM0_IN2_8			Mux input channel 2 of TIM module 0
	GTM_TIM1_IN2_8			Mux input channel 2 of TIM module 1
	QSPI4_SCLKA			Slave SPI clock inputs
	SMM_ESR2_PORT_IN			ESR2 pad data from PIN Slice
	QSPI5_SCLKF_F			Slave SPI clock inputs
	GPT122_T5INA			Trigger/gate input of timer T5
	EGTM_TIM0_IN2_8			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_8			Mux input channel 2 of TIM module 1
	PMS_ESR2WKP			ESR2 pin input
	SSC_SCLKB	I#		Slave SPI clock input B
	PINRSTA			Reset input A
	T20C			T20 capture input C
	T2CCU0_1B			T2 capture 0 input 1B
	T2CCU1_2B			T2 capture 1 input 2B
	EXINT4B			Interrupt 4 input B
	EXINT10B			Interrupt 10 input B
	P33.11	O0		General-purpose output
	GTM_TOUT33	O1		GTM muxed output
	ASCLIN1_ASCLK	O2		Shift clock output
	QSPI4_SCLK	O3		Master SPI clock output

(table continues...)

Table 25 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O4		Reserved
	ASCLIN5_ASCLK_F	O5		Shift clock output
	ADC_PWM1	O6		Negative PWM
	QSPI5_SCLK_F	O7		Master SPI clock output
	—	O8		Reserved
	EGTM_TOUT33	O9		eGTM muxed output
	—	O10		Reserved
	ADC_BFL9	O11		Boundary flags from FCC
	PMS_RTCOUT	O12		RTC output for P33.11
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.3	O#0		General-purpose output
	—	O#1		Reserved
	SSC_SCLK	O#2		Clock output
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_1	O#5		T2 PWM channel 01
	T2CCU1_2	O#6		T2 PWM channel 12
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	PMS_ESR2PORST	PO		ESR2 reset output. For details please refer to the PMS/SMM chapter.
AB19	P33.12	I	FAST / PU1 / VDDEVRS B / ES5	General-purpose input
	GTM_TIM2_IN0_6			Mux input channel 0 of TIM module 2
	GTM_TIM3_IN0_6			Mux input channel 0 of TIM module 3

(table continues...)

Table 25 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI4_MTSRA			Slave SPI data input
	CAN00_RXDD			CAN receive input node 0
	GPT122_T5EUDA			Count direction control input of timer T5
	SMU_FSPIN1			FSP Status Input - Shows the actual state of the FSP ErroPin
	EGTM_TIM2_IN0_6			Mux input channel 0 of TIM module 2
	PMS_PINCWKP			PINC (P33.12) pin input
	UART_RXDG	I#		Receive input G
	WCAN_RXDG			Wake-up input G
	SSC_MTSRB			Slave SPI data input B
	T1C			T1 capture input C
	T21C			T21 capture input C
	T2CCU0_2B			T2 capture 0 input 2B
	T2CCU1_3B			T2 capture 1 input 3B
	EXINT5B			Interrupt 5 input B
	EXINT11B			Interrupt 11 input B
	P33.12	O0		General-purpose output
	GTM_TOUT34	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	QSPI4_MTSR	O3		Master SPI data output
	ASCLIN1_ASCLK	O4		Shift clock output
	CAN22_TXD	O5		CAN transmit output node 2
	ADC_PWM0	O6		Positive PWM
	QSPI5_MTSR_F	O7		Master SPI data output
	ASCLIN5_ATX_F	O8		Transmit output
	EGTM_TOUT34	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.4	O#0		General-purpose output
	UART_TXD	O#1		Transmit output

(table continues...)

Table 25 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function	
	SSC_MTSR	O#2		Master SPI data output	
	—	O#3		Reserved	
	—	O#4		Reserved	
	T2CCU0_2	O#5		T2 PWM channel 02	
	T2CCU1_3	O#6		T2 PWM channel 13	
	—	O#7		Reserved	
	—	O#8		Reserved	
	—	O#9		Reserved	
	—	O#10		Reserved	
	—	O#11		Reserved	
	—	O#12		Reserved	
	—	O#13		Reserved	
	—	O#14		Reserved	
	—	O#15		Reserved	
	SMU_FSP1	O		FSP Output Signal - Generated by SMU	
AC19	P33.13	I	FAST / PU1 / VDDEVRS B / ES5	General-purpose input	
	GTM_TIM2_IN1_5			Mux input channel 1 of TIM module 2	
	GTM_TIM3_IN1_5			Mux input channel 1 of TIM module 3	
	ASCLIN1_ARXF			Receive input	
	ADC_SIGN1			Sign for Carrier Cancellation	
	QSPI4_MRSTA			Master SPI data input	
	MSC1_INJ1			Injection signal from port	
	CAN22_RXDA			CAN receive input node 2	
	GPT122_T6EUDA			Count direction control input of core timer T6	
	QSPI5_MRSTD_F			Master SPI data input	
	PSI5S1_RXD			RX data input	
	EGTM_TIM2_IN1_5			Mux input channel 1 of TIM module 2	
	PMS_PINBWKP			PINB (P33.13) pin input	
	UART_RXDB			I#	Receive input B
	WCAN_RXDC				Wake-up input C
	SSC_MRSTB	Master SPI data input B			
	T0C	T0 capture input C			
	T20EXD	T20 interrupt input D			

(table continues...)

Table 25 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	T2CCU0_3B			T2 capture 0 input 3B
	EXINT0C			Interrupt 0 input C
	EXINT6B			Interrupt 6 input B
	ADCOMPCH8			Analog input channel 8
	P33.13	O0		General-purpose output
	GTM_TOUT35	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	QSPI4_MRST	O3		Slave SPI data output
	QSPI2_SLSO6	O4		Master slave select output
	CAN00_TXD	O5		CAN transmit output node 0
	ASCLIN5_ASLSO_F	O6		Slave select signal output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT35	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.5	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional receive pin O
	SSC_MRST	O#2		Slave SPI data output
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_3	O#5		T2 PWM channel 03
	T2CCU1_4	O#6		T2 PWM channel 14
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved

(table continues...)

Table 25 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
W17	P33.14	I	FAST / PU1 / VDDEVRS B / ES5	General-purpose input
	GTM_TIM2_IN0_8			Mux input channel 0 of TIM module 2
	GTM_TIM4_IN5_14			Mux input channel 5 of TIM module 4
	GTM_TIM5_IN0_8			Mux input channel 0 of TIM module 5
	QSPI2_SCLKD			Slave SPI clock inputs
	CBS_TGI6			Trigger input
	CAN31_RXDB			CAN receive input node 1
	QSPI5_MRSTF_F			Master SPI data input
	EGTM_TIM2_IN0_8			Mux input channel 0 of TIM module 2
	SSC_SCLKC	I#		Slave SPI clock input C
	EXTNMI			NMI input
	T21EXC			T21 interrupt input C
	EXINT1C			Interrupt 1 input C
	ADCOMPCH9			Analog input channel 9
	P33.14	O0		General-purpose output
	GTM_TOUT143	O1		GTM muxed output
	—	O2		Reserved
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	QSPI5_MRST	O7		Slave SPI data output
	—	O8		Reserved
	EGTM_TOUT143	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 25 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SCR_P1.6	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	SSC_SCLK	O#2		Clock output
	—	O#3		Reserved
	—	O#4		Reserved
	—	O#5		Reserved
	T2CCU1_5	O#6		T2 PWM channel 15
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	CBS_TGO6	O		Trigger output
Y17	P33.15	I	FAST / PU1 / VDDEVRS B / ES5	General-purpose input
	GTM_TIM2_IN1_7			Mux input channel 1 of TIM module 2
	GTM_TIM4_IN6_11			Mux input channel 6 of TIM module 4
	GTM_TIM5_IN1_9			Mux input channel 1 of TIM module 5
	CBS_TGI7			Trigger input
	QSPI5_SLSIB_F			Slave select input
	SENT1_SENT14D			Receive input channel 14
	QSPI4_MTSRD			Slave SPI data input
	EGTM_TIM2_IN1_7			Mux input channel 1 of TIM module 2
	UART_RXDE	I#		Receive input E
	PINRSTB	Reset input B		
	T20EXE	T20 interrupt input E		
	T2CCU0_0C	T2 capture 0 input 0C		
	T2CCU1_0C	T2 capture 1 input 0C		
	EXINT2C	Interrupt 2 input C		
	EXINT3C	Interrupt 3 input C		

(table continues...)

Table 25 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EXINT8C			Interrupt 8 input C
	ADCOMPCH10			Analog input channel 10
	P33.15	O0		General-purpose output
	GTM_TOUT144	O1		GTM muxed output
	CAN31_TXD	O2		CAN transmit output node 1
	QSPI2_SLSO11	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	SENT1_SPC14	O8		Transmit output
	EGTM_TOUT144	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.7	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional receive pin O
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_0	O#5		T2 PWM channel 00
	T2CCU1_0	O#6		T2 PWM channel 10
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved

(table continues...)

Table 25 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#15		Reserved
	CBS_TGO7	O		Trigger output

3.2.21 BGA436_STD port 34

Table 26 Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
Y14	P34.1	I	SLOW / PU1 / VDDEVRS B / ES5	General-purpose input
	GTM_TIM2_IN3_9			Mux input channel 3 of TIM module 2
	GTM_TIM3_IN4_13			Mux input channel 4 of TIM module 3
	GTM_TIM5_IN3_9			Mux input channel 3 of TIM module 5
	SENT0_SENT12D			Receive input channel 12
	GPT122_T3INA			Trigger/gate input of core timer T3 (input A, B and C)
	EGTM_TIM2_IN3_9			Mux input channel 3 of TIM module 2
	UART_RXDD	I#		Receive input D
	T21EXD			T21 interrupt input D
	T2CCU0_1C			T2 capture 0 input 1C
	T2CCU1_1C			T2 capture 1 input 1C
	EXINT4C			Interrupt 4 input C
	EXINT9C			Interrupt 9 input C
	ADCOMPCH11			Analog input channel 11
	ADC_TMADC4CH15	AI		Analog Input for TMADC4 Channel 15
	P34.1	O0		General-purpose output
	GTM_TOUT146	O1		GTM muxed output
	ASCLIN4_ATX	O2		Transmit output
	—	O3		Reserved
	CAN00_TXD	O4		CAN transmit output node 0
	CAN20_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	SENT0_SPC12	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT146	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 26 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P3.0	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional receive pin O
	—	O#2		Reserved
	T20EXF2	O#3		Timer 20 external overflow
	—	O#4		Reserved
	T2CCU0_1	O#5		T2 PWM channel 01
	T2CCU1_1	O#6		T2 PWM channel 11
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	PMS_DEBUG0	O		PMS debugging power mode K
W15	P34.2	I	SLOW / PU1 / VDDEVRS B / ES	General-purpose input
	GTM_TIM2_IN4_8			Mux input channel 4 of TIM module 2
	GTM_TIM3_IN5_15			Mux input channel 5 of TIM module 3
	GTM_TIM5_IN4_8			Mux input channel 4 of TIM module 5
	ASCLIN4_ARXB			Receive input
	CAN00_RXDG			CAN receive input node 0
	CAN20_RXDC			CAN receive input node 0
	SENT0_SENT14B			Receive input channel 14
	GPT122_T3EUDA			Count direction control input of core timer T3
	I2C1_SDAD			Serial Data Input 3
	EGTM_TIM2_IN4_8			Mux input channel 4 of TIM module 2

(table continues...)

Table 26 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	WCAN_RXDI	I#		Wake-up input I
	T20EXF			T20 interrupt input F
	T2CCU0_2C			T2 capture 0 input 2C
	EXINT5C			Interrupt 5 input C
	ADCOMPCH12			Analog input channel 12
	I2CSDAB			Serial data input B
	ADC_TMADC4CH14	AI		Analog Input for TMADC4 Channel 14
	P34.2	O0		General-purpose output
	GTM_TOUT147	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	I2C1_SDA	O8		Serial Data Output
	EGTM_TOUT147	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P3.1	O#0		General-purpose output
	—	O#1		Reserved
	—	O#2		Reserved
	—	O#3		Reserved
	T21EXF2	O#4		Timer 21 external overflow
	T2CCU0_2	O#5		T2 PWM channel 02
	T2CCU1_2	O#6		T2 PWM channel 12
	I2CSDA	O#7		Serial data output
	—	O#8		Reserved
	—	O#9		Reserved

(table continues...)

Table 26 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	PMS_DEBUG1	O		PMS debugging power mode K
Y15	P34.3	I	SLOW / PU1 / VDDEVRS B / ES	General-purpose input
	GTM_TIM2_IN5_9			Mux input channel 5 of TIM module 2
	GTM_TIM3_IN6_14			Mux input channel 6 of TIM module 3
	GTM_TIM5_IN5_10			Mux input channel 5 of TIM module 5
	ASCLIN4_ARXE			Receive input
	SENT1_SENT14B			Receive input channel 14
	GPT122_T4INA			Trigger/gate input of timer T4
	I2C1_SCLD			Serial Clock Input 3
	EGTM_TIM2_IN5_9			Mux input channel 5 of TIM module 2
	PINRSTD	I#		Reset input D
	T21EXE			T21 interrupt input E
	T2CCU0_3C			T2 capture 0 input 3C
	EXINT0D			Interrupt 0 input D
	EXINT6C			Interrupt 6 input C
	ADCOMPCH13			Analog input channel 13
	I2CSCLB			Serial clock input B
	ADC_TMADC4CH13	AI		Analog Input for TMADC4 Channel 13
	P34.3	O0		General-purpose output
	GTM_TOUT148	O1		GTM muxed output
	ASCLIN4_ASCLK	O2		Shift clock output
	ASCLIN4_ATX	O3		Transmit output
	CAN00_TXD	O4		CAN transmit output node 0
	CAN20_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	—	O7		Reserved
	I2C1_SCL	O8		Serial Clock Output

(table continues...)

Table 26 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TOUT148	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P3.2	O#0		General-purpose output
	—	O#1		Reserved
	—	O#2		Reserved
	T20EXF2	O#3		Timer 20 external overflow
	—	O#4		Reserved
	T2CCU0_3	O#5		T2 PWM channel 03
	T2CCU1_3	O#6		T2 PWM channel 13
	I2CSCL	O#7		Serial clock output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	PMS_DEBUG2	O		PMS debugging power mode K
W16	P34.4	I	SLOW / PU1 / VDDEVRS B / ES	General-purpose input
	GTM_TIM2_IN6_8			Mux input channel 6 of TIM module 2
	GTM_TIM3_IN7_13			Mux input channel 7 of TIM module 3
	GTM_TIM5_IN6_10			Mux input channel 6 of TIM module 5
	QSPI2_MRSTD			Master SPI data input
	SENT1_SENT13B			Receive input channel 13
	EGTM_TIM2_IN6_8			Mux input channel 6 of TIM module 2
	UART_RXDJ	I#		Receive input J
	SSC_MRSTC			Master SPI data input C

(table continues...)

Table 26 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	T20EXG			T20 interrupt input P
	T2CCU1_2C			T2 capture 1 input 2C
	EXINT1D			Interrupt 1 input D
	EXINT10C			Interrupt 10 input C
	ADCOMPCH14			Analog input channel 14
	ADC_TMADC4CH12	AI		Analog Input for TMADC4 Channel 12
	P34.4	O0		General-purpose output
	GTM_TOUT149	O1		GTM muxed output
	ASCLIN4_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	QSPI2_MRST	O4		Slave SPI data output
	—	O5		Reserved
	ADC_BFL6	O6		Boundary flags from FCC
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT149	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P3.3	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional receive pin O
	SSC_MRST	O#2		Slave SPI data output
	—	O#3		Reserved
	T21EXF2	O#4		Timer 21 external overflow
	T2CCU0_4	O#5		T2 PWM channel 04
	T2CCU1_4	O#6		T2 PWM channel 14
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved

(table continues...)

Table 26 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	PMS_DEBUG3	O		PMS debugging power mode K
Y16	P34.5	I	FAST / PU1 / VDDEVRS B / ES	General-purpose input
	GTM_TIM2_IN7_9			Mux input channel 7 of TIM module 2
	GTM_TIM4_IN7_11			Mux input channel 7 of TIM module 4
	GTM_TIM5_IN7_9			Mux input channel 7 of TIM module 5
	QSPI2_MTSRD			Slave SPI data input
	QSPI4_MRSTF			Master SPI data input
	SENT0_SENT13C			Receive input channel 13
	EGTM_TIM2_IN7_9			Mux input channel 7 of TIM module 2
	WCAN_RXDJ	I#		Wake-up input J
	SSC_MTSRC			Slave SPI data input C
	T21EXF			T21 interrupt input F
	T2CCU1_3C			T2 capture 1 input 3C
	EXINT2D			Interrupt 2 input D
	EXINT11C			Interrupt 11 input C
	ADCOMPCH15			Analog input channel 15
	ADC_TMADC4CH11	AI		Analog Input for TMADC4 Channel 11
	P34.5	O0		General-purpose output
	GTM_TOUT150	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	QSPI2_MTSR	O4		Master SPI data output
	—	O5		Reserved
	ADC_BFL7	O6		Boundary flags from FCC
	SENT0_SPC13	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT150	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 26 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P3.4	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	SSC_MTSR	O#2		Master SPI data output
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_5	O#5		T2 PWM channel 05
	T2CCU1_5	O#6		T2 PWM channel 15
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	PMS_DEBUG4	O		PMS debugging power mode K

3.2.22 BGA436_STD analog

Table 27 Analog Inputs functions

Ball	Symbol	Ctrl.	Buffer type	Function
W13	AN0	I	D / HighZ / VDDM	Analog Input 0
	ADC_TMADC0CH0			Analog Input for TMADC0 Channel 0
	ADC_DSADC1PA			Analog Input for DSADC1 Positive Input A
	ADC_FCC1			Analog Input for FCC1
Y13	AN1	I	D / HighZ / VDDM	Analog Input 1
	ADC_TMADC0CH1			Analog Input for TMADC0 Channel 1

(table continues...)

Table 27 (continued) Analog Inputs functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ADC_DSADC1NA			Analog Input for DSADC1 Negative Input A
AB12	AN2	I	D / HighZ / VDDM	Analog Input 2
	ADC_TMADC0CH2			Analog Input for TMADC0 Channel 2
	ADC_DSADC0PA			Analog Input for DSADC0 Positive Input A
	ADC_FCC0			Analog Input for FCC0
Y12	AN3	I	D / HighZ / VDDM	Analog Input 3
	ADC_TMADC0CH3			Analog Input for TMADC0 Channel 3
	ADC_DSADC0NA			Analog Input for DSADC0 Negative Input A
W12	AN4	I	D / HighZ / VDDM	Analog Input 4
	ADC_TMADC0CH4			Analog Input for TMADC0 Channel 4
	ADC_TMADC1CH0			Analog Input for TMADC1 Channel 0
AC12	AN5	I	D / HighZ / VDDM	Analog Input 5
	ADC_TMADC0CH5			Analog Input for TMADC0 Channel 5
	ADC_TMADC1CH1			Analog Input for TMADC1 Channel 1
W11	AN6	I	D / HighZ / VDDM	Analog Input 6
	ADC_TMADC0CH6			Analog Input for TMADC0 Channel 6
	ADC_TMADC1CH2			Analog Input for TMADC1 Channel 2
Y11	AN7	I	D / HighZ / VDDM	Analog Input 7
	ADC_TMADC0CH7			Analog Input for TMADC0 Channel 7
	ADC_TMADC1CH3			Analog Input for TMADC1 Channel 3
AB11	AN8	I	D / HighZ / VDDM	Analog Input 8
	ADC_TMADC0CH8			Analog Input for TMADC0 Channel 8
	ADC_TMADC5CH0			Analog Input for TMADC5 Channel 0
Y10	AN9	I	D / HighZ / VDDM	Analog Input 9
	ADC_TMADC0CH9			Analog Input for TMADC0 Channel 9
	ADC_TMADC5CH1			Analog Input for TMADC5 Channel 1
AC11	AN10	I	D / HighZ / VDDM	Analog Input 10
	ADC_TMADC0CH10			Analog Input for TMADC0 Channel 10
	ADC_TMADC5CH2			Analog Input for TMADC5 Channel 2
AB10	AN11	I	D / HighZ / VDDM	Analog Input 11
	ADC_TMADC0CH11			Analog Input for TMADC0 Channel 11
	ADC_TMADC5CH3			Analog Input for TMADC5 Channel 3

(table continues...)

Table 27 (continued) Analog Inputs functions

Ball	Symbol	Ctrl.	Buffer type	Function
W10	AN12	I	D / HighZ / VDDM	Analog Input 12
	ADC_TMADC0CH12			Analog Input for TMADC0 Channel 12
	ADC_DSADC0PB			Analog Input for DSADC0 Positive Input B
	ADC_DSADC3PB			Analog Input for DSADC3 Positive Input B
	ADC_FCC3			Analog Input for FCC3
AB9	AN13	I	D / HighZ / VDDM	Analog Input 13
	ADC_TMADC0CH13			Analog Input for TMADC0 Channel 13
	ADC_DSADC0NB			Analog Input for DSADC0 Negative Input B
	ADC_DSADC3NB			Analog Input for DSADC3 Negative Input B
Y9	AN14	I	D / HighZ / VDDM	Analog Input 14
	ADC_TMADC0CH14			Analog Input for TMADC0 Channel 14
	ADC_DSADC1PB			Analog Input for DSADC1 Positive Input B
	ADC_DSADC9PB			Analog Input for DSADC9 Positive Input B
	ADC_FCC9			Analog Input for FCC9
W9	AN15	I	D / HighZ / VDDM	Analog Input 15
	ADC_TMADC0CH15			Analog Input for TMADC0 Channel 15
	ADC_DSADC1NB			Analog Input for DSADC1 Negative Input B
	ADC_DSADC9NB			Analog Input for DSADC9 Negative Input B
AB8	AN16	I	D / HighZ / VDDM	Analog Input 16
	ADC_TMADC1CH4			Analog Input for TMADC1 Channel 4
	ADC_DSADC6PC			Analog Input for DSADC6 Positive Input C
	ADC_FCC6			Analog Input for FCC6
Y8	AN17 / P40.10	I	S / PU1 / VDDM	Analog Input 17
				General-purpose input
	ADC_TMADC1CH5			Analog Input for TMADC1 Channel 5
	ADC_DSADC6NC			Analog Input for DSADC6 Negative Input C
	SENT0_SENT5A			Receive input channel 5
AB7	AN18 / P40.11	I	S / PU1 / VDDM	Analog Input 18
				General-purpose input
	ADC_TMADC1CH6			Analog Input for TMADC1 Channel 6
	ADC_TMADC5CH4			Analog Input for TMADC5 Channel 4
	ADC_DSADC7PC			Analog Input for DSADC7 Positive Input C
	ADC_FCC7			Analog Input for FCC7

(table continues...)

Table 27 (continued) Analog Inputs functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SENT1_SENT5A			Receive input channel 5
AB6	AN19 / P40.12	I	S / PU1 / VDDM	Analog Input 19
				General-purpose input
	ADC_TMADC1CH7			Analog Input for TMADC1 Channel 7
	ADC_TMADC5CH5			Analog Input for TMADC5 Channel 5
	ADC_DSADC7NC			Analog Input for DSADC7 Negative Input C
	SENT0_SENT6A			Receive input channel 6
AC6	AN20	I	D / HighZ / VDDM	Analog Input 20
	ADC_TMADC1CH8			Analog Input for TMADC1 Channel 8
	ADC_DSADC2PA			Analog Input for DSADC2 Positive Input A
	ADC_FCC2			Analog Input for FCC2
AC5	AN21	I	D / HighZ / VDDM	Analog Input 21
	ADC_TMADC1CH9			Analog Input for TMADC1 Channel 9
	ADC_DSADC2NA			Analog Input for DSADC2 Negative Input A
W8	AN22	I	D / HighZ / VDDM	Analog Input 22
	ADC_TMADC1CH10			Analog Input for TMADC1 Channel 10
	ADC_TMADC5CH6			Analog Input for TMADC5 Channel 6
V8	AN23	I	D / HighZ / VDDM	Analog Input 23
	ADC_TMADC1CH11			Analog Input for TMADC1 Channel 11
	ADC_TMADC5CH7			Analog Input for TMADC5 Channel 7
AB5	AN24 / P40.0	I	S / PU1 / VDDM	Analog Input 24
				General-purpose input
	ADC_TMADC1CH12			Analog Input for TMADC1 Channel 12
	ADC_DSADC2PB			Analog Input for DSADC2 Positive Input B
	SENT0_SENT0A			Receive input channel 0
AB4	AN25 / P40.1	I	S / PU1 / VDDM	Analog Input 25
				General-purpose input
	ADC_TMADC1CH13			Analog Input for TMADC1 Channel 13
	ADC_DSADC2NB			Analog Input for DSADC2 Negative Input B
	SENT1_SENT0A			Receive input channel 0
AA5	AN26 / P40.2	I	S / PU1 / VDDM	Analog Input 26
				General-purpose input
	ADC_TMADC1CH14			Analog Input for TMADC1 Channel 14

(table continues...)

Table 27 (continued) Analog Inputs functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ADC_TMADC5CH8			Analog Input for TMADC5 Channel 8
	SENT0_SENT1A			Receive input channel 1
AA4	AN27 / P40.3	I	S / PU1 / VDDM	Analog Input 27
				General-purpose input
	ADC_TMADC1CH15			Analog Input for TMADC1 Channel 15
	ADC_TMADC5CH9			Analog Input for TMADC5 Channel 9
	SENT1_SENT1A			Receive input channel 1
Y5	AN28 / P40.13	I	S / PU1 / VDDM	Analog Input 28
				General-purpose input
	ADC_TMADC3CH0			Analog Input for TMADC3 Channel 0
	ADC_TMADC5CH10			Analog Input for TMADC5 Channel 10
	SENT1_SENT6A			Receive input channel 6
Y4	AN29 / P40.14	I	S / PU1 / VDDM	Analog Input 29
				General-purpose input
	ADC_TMADC3CH1			Analog Input for TMADC3 Channel 1
	ADC_TMADC5CH11			Analog Input for TMADC5 Channel 11
	SENT0_SENT7A			Receive input channel 7
W7	AN30	I	D / HighZ / VDDM	Analog Input 30
	ADC_TMADC3CH2			Analog Input for TMADC3 Channel 2
	ADC_TMADC5CH12			Analog Input for TMADC5 Channel 12
V7	AN31	I	D / HighZ / VDDM	Analog Input 31
	ADC_TMADC3CH3			Analog Input for TMADC3 Channel 3
	ADC_TMADC5CH13			Analog Input for TMADC5 Channel 13
U7	AN32 / P40.4	I	S / PU1 / VDDM	Analog Input 32
				General-purpose input
	ADC_TMADC3CH4			Analog Input for TMADC3 Channel 4
	ADC_TMADC5CH14			Analog Input for TMADC5 Channel 14
	SENT0_SENT2A			Receive input channel 2
V4	AN33 / P40.5	I	S / PU1 / VDDM	Analog Input 33
				General-purpose input
	ADC_TMADC3CH5			Analog Input for TMADC3 Channel 5
	ADC_TMADC5CH15			Analog Input for TMADC5 Channel 15
	SENT1_SENT2A			Receive input channel 2

(table continues...)

Table 27 (continued) Analog Inputs functions

Ball	Symbol	Ctrl.	Buffer type	Function
U8	AN34	I	D / HighZ / VDDM	Analog Input 34
	ADC_TMADC3CH6			Analog Input for TMADC3 Channel 6
	ADC_DSADC7PD			Analog Input for DSADC7 Positive Input D
V5	AN35	I	D / HighZ / VDDM	Analog Input 35
	ADC_TMADC3CH7			Analog Input for TMADC3 Channel 7
	ADC_DSADC7ND			Analog Input for DSADC7 Negative Input D
T7	AN36 / P40.6	I	S / PU1 / VDDM	Analog Input 36
				General-purpose input
	ADC_TMADC3CH8			Analog Input for TMADC3 Channel 8
	ADC_DSADC8PA			Analog Input for DSADC8 Positive Input
	ADC_FCC8			Analog Input for FCC8
	SENT0_SENT3A			Receive input channel 3
U5	AN37 / P40.7	I	S / PU1 / VDDM	Analog Input 37
				General-purpose input
	ADC_TMADC3CH9			Analog Input for TMADC3 Channel 9
	ADC_DSADC8NA			Analog Input for DSADC8 Negative Input
	SENT1_SENT3A			Receive input channel 3
T8	AN38 / P40.8	I	S / PU1 / VDDM	Analog Input 38
				General-purpose input
	ADC_TMADC3CH10			Analog Input for TMADC3 Channel 10
	ADC_DSADC8PB			Analog Input for DSADC8 Positive Input B
	SENT0_SENT4A			Receive input channel 4
U4	AN39 / P40.9	I	S / PU1 / VDDM	Analog Input 39
				General-purpose input
	ADC_TMADC3CH11			Analog Input for TMADC3 Channel 11
	ADC_DSADC8NB			Analog Input for DSADC8 Negative Input B
	SENT1_SENT4A			Receive input channel 4
R8	AN40	I	D / HighZ / VDDM	Analog Input 40
	ADC_TMADC3CH12			Analog Input for TMADC3 Channel 12
	ADC_TMADC6CH0			Analog Input for TMADC6 Channel 0
R7	AN41	I	D / HighZ / VDDM	Analog Input 41
	ADC_TMADC3CH13			Analog Input for TMADC3 Channel 13
	ADC_TMADC6CH1			Analog Input for TMADC6 Channel 1

(table continues...)

Table 27 (continued) Analog Inputs functions

Ball	Symbol	Ctrl.	Buffer type	Function
P8	AN42	I	D / HighZ / VDDM	Analog Input 42
	ADC_TMADC3CH14			Analog Input for TMADC3 Channel 14
	ADC_TMADC6CH2			Analog Input for TMADC6 Channel 2
P7	AN43	I	D / HighZ / VDDM	Analog Input 43
	ADC_TMADC3CH15			Analog Input for TMADC3 Channel 15
	ADC_TMADC6CH3			Analog Input for TMADC6 Channel 3
T4	AN44	I	D / HighZ / VDDM	Analog Input 44
	ADC_TMADC6CH4			Analog Input for TMADC6 Channel 4
	ADC_DSADC8PC			Analog Input for DSADC8 Positive Input C
T5	AN45	I	D / HighZ / VDDM	Analog Input 45
	ADC_TMADC6CH5			Analog Input for TMADC6 Channel 5
	ADC_DSADC8NC			Analog Input for DSADC8 Negative Input C
R4	AN46	I	D / HighZ / VDDM	Analog Input 46
	ADC_TMADC6CH6			Analog Input for TMADC6 Channel 6
	ADC_DSADC8PD			Analog Input for DSADC8 Positive Input D
R5	AN47	I	D / HighZ / VDDM	Analog Input 47
	ADC_TMADC6CH7			Analog Input for TMADC6 Channel 7
	ADC_DSADC8ND			Analog Input for DSADC8 Negative Input D
AF7	AN48	I	D / HighZ / VDDM	Analog Input 48
	ADC_TMADC6CH8			Analog Input for TMADC6 Channel 8
	ADC_DSADC6PD			Analog Input for DSADC6 Positive Input D
AF5	AN49	I	D / HighZ / VDDM	Analog Input 49
	ADC_TMADC6CH9			Analog Input for TMADC6 Channel
	ADC_DSADC6ND			Analog Input for DSADC6 Negative Input D
AF4	AN50	I	D / HighZ / VDDM	Analog Input 50
	ADC_TMADC6CH10			Analog Input for TMADC6 Channel 10
	ADC_DSADC9PA			Analog Input for DSADC9 Positive Input
AE5	AN51	I	D / HighZ / VDDM	Analog Input 51
	ADC_TMADC6CH11			Analog Input for TMADC6 Channel 11
	ADC_DSADC9NA			Analog Input for DSADC9 Negative Input
AF3	AN52	I	D / HighZ / VDDM	Analog Input 52
	ADC_TMADC6CH12			Analog Input for TMADC6 Channel 12
	ADC_DSADC6PA			Analog Input for DSADC6 Positive Input A

(table continues...)

Table 27 (continued) Analog Inputs functions

Ball	Symbol	Ctrl.	Buffer type	Function
AE4	AN53	I	D / HighZ / VDDM	Analog Input 53
	ADC_TMADC6CH13			Analog Input for TMADC6 Channel 13
	ADC_DSADC6NA			Analog Input for DSADC6 Negative Input A
AE3	AN54 / P41.5	I	S / PU1 / VDDM	Analog Input 54
				General-purpose input
	ADC_TMADC6CH14			Analog Input for TMADC6 Channel 14
	ADC_DSADC6PB			Analog Input for DSADC6 Positive Input B
	SENT0_SENT10A			Receive input channel 10
AF2	AN55 / P41.6	I	S / PU1 / VDDM	Analog Input 55
				General-purpose input
	ADC_TMADC6CH15			Analog Input for TMADC6 Channel 15
	ADC_DSADC6NB			Analog Input for DSADC6 Negative Input B
	SENT1_SENT10A			Receive input channel 10
AE2	AN56	I	D / HighZ / VDDM	Analog Input 56
	ADC_DSADC1PC			Analog Input for DSADC1 Positive Input C
AE1	AN57	I	D / HighZ / VDDM	Analog Input 57
	ADC_DSADC1NC			Analog Input for DSADC1 Negative Input C
AD2	AN58	I	D / HighZ / VDDM	Analog Input 58
	ADC_DSADC3PC			Analog Input for DSADC3 Positive Input C
AD1	AN59	I	D / HighZ / VDDM	Analog Input 59
	ADC_DSADC3NC			Analog Input for DSADC3 Negative Input C
AB2	AN60	I	D / HighZ / VDDM	Analog Input 60
	ADC_DSADC7PA			Analog Input for DSADC7 Positive Input A
AB1	AN61	I	D / HighZ / VDDM	Analog Input 61
	ADC_DSADC7NA			Analog Input for DSADC7 Negative Input A
Y2	AN62 / P41.7	I	S / PU1 / VDDM	Analog Input 62
				General-purpose input
	ADC_DSADC7PB			Analog Input for DSADC7 Positive Input B
	SENT0_SENT11A			Receive input channel 11
Y1	AN63 / P41.8	I	S / PU1 / VDDM	Analog Input 63
				General-purpose input
	ADC_DSADC7NB			Analog Input for DSADC7 Negative Input B
	SENT1_SENT11A			Receive input channel 11

(table continues...)

Table 27 (continued) Analog Inputs functions

Ball	Symbol	Ctrl.	Buffer type	Function
W2	AN64	I	D / HighZ / VDDM	Analog Input 64
	ADC_DSADC3PD			Analog Input for DSADC3 Positive Input D
W1	AN65	I	D / HighZ / VDDM	Analog Input 65
	ADC_DSADC3ND			Analog Input for DSADC3 Negative Input D
U1	AN66	I	D / HighZ / VDDM	Analog Input 66
	ADC_DSADC2PC			Analog Input for DSADC2 Positive Input C
T1	AN67 / P41.0	I	S / PU1 / VDDM	Analog Input 67
				General-purpose input
	ADC_DSADC2NC			Analog Input for DSADC2 Negative Input C
	SENT1_SENT7A			Receive input channel 7
U2	AN68 / P41.1	I	S / PU1 / VDDM	Analog Input 68
				General-purpose input
	ADC_DSADC3PA			Analog Input for DSADC3 Positive Input A
	SENT0_SENT8A			Receive input channel 8
P2	AN69 / P41.2	I	S / PU1 / VDDM	Analog Input 69
				General-purpose input
	ADC_DSADC3NA			Analog Input for DSADC3 Negative Input A
	SENT1_SENT8A			Receive input channel 8
P1	AN70 / P41.3	I	S / PU1 / VDDM	Analog Input 70
				General-purpose input
	ADC_DSADC2PD			Analog Input for DSADC2 Positive Input D
	SENT0_SENT9A			Receive input channel 9
T2	AN71 / P41.4	I	S / PU1 / VDDM	Analog Input 71
				General-purpose input
	ADC_DSADC2ND			Analog Input for DSADC2 Negative Input D
	SENT1_SENT9A			Receive input channel 9

3.2.23 BGA436_STD special

Table 28 Special I/O functions

Ball	Symbol	Ctrl.	Buffer type	Function
E26	PHY1_TXP	O	PHY / VDDPHPH Y1	(Ball name)
	SGBT_TXP0	O		Transmit data (P line)
	SGMII1_TXP	O		Transmit data (P line)
C26	PHY1_RXP	I	PHY / VDDPHPH Y1	(Ball name)
	SGMII1_RXP	I		Receive data (P line)
E25	PHY1_TXN	O	PHY / VDDPHPH Y1	(Ball name)
	SGBT_TXN0	O		Transmit data (N line)
	SGMII1_TXN	O		Transmit data (N line)
C25	PHY1_RXN	I	PHY / VDDPHPH Y1	(Ball name)
	SGMII1_RXN	I		Receive data (N line)

3.2.24 BGA436_STD system

Table 29 System I/O functions

Ball	Symbol	Ctrl.	Buffer type	Function
A1	THD0_A	I	—	Reserved - has to be connected to VSSEXT
R22	XTAL2	O	XTAL / VDDEXT0 SC	XTAL2. Main Oscillator/PLL/Clock generator output
R23	XTAL1	I	XTAL / VDDEXT0 SC	XTAL1. Main Oscillator/PLL/Clock generator input
P22	TRST	I	FAST / PU2 / VDDEXT	JTAG Module Reset/Enable Input
	DAPE0	I		DAPE: DAPE0 Data I/O DAPE: DAPE0 Data I/O (PD Devices: VSS)
M19	TCK	I	FAST / PD3 / VDDEXT	JTAG Module Clock Input
	DAP0	I		DAP:DAP0 Clock Input
N19	TMS	I	FAST / PD3 / VDDEXT	JTAG Module State Machine Control Input
	DAP1	I/O		DAP:DAP1 Data I/O
K19	ESR1	I/O	FAST / PU1 / VDDEXT	ESR1 pad data
	SMM_ESR1_PORT_IN	I		ESR1 pad data from PIN Slice

(table continues...)

Table 29 (continued) System I/O functions

Ball	Symbol	Ctrl.	Buffer type	Function
	PMS_ESR1WKP	I		ESR1 pin input
J19	ESR0	I/O	FAST / OD / VDDEXT	ESR0 pad data
	SMM_ESR0_PORT_IN	I		ESR0 pad data from PIN Slice
	PMS_ESR0WKP	I		ESR0 pin input
K20	PORST	I/O	PORST / PD / VDDEXT	Power on Reset. Additional strong PD in case of power fail.
	PMS_PORSTOUT	O		Power On Reset Output. Additional strong PD in case of power fail.
	PMS_PORSTIN	I		Power On Reset Input. Additional strong PD in case of power fail.
B2	THD0_K	I	—	Reserved - has to be connected to VSSEXT

3.2.25 BGA436_STD supply

Table 30 Supply functions

Ball	Symbol	Ctrl.	Buffer type	Function
A26	NC1_A26	I	—	Not connected. These pins are not connected on package level and will not be used for future extensions
AC4	NC1_AC4	I	—	Not connected. These pins are not connected on package level and will not be used for future extensions
AF1	NC1_AF1	I	—	Not connected. These pins are not connected on package level and will not be used for future extensions
L17	NC1_L17	I	—	Not connected. These pins are not connected on package level and will not be used for future extensions
T17	NC1_T17	I	—	Not connected. These pins are not connected on package level and will not be used for future extensions
T22	NC1_T22	I	—	Not connected. These pins are not connected on package level and will not be used for future extensions
U14	NC1_U14	I	—	Not connected. These pins are not connected on package level and will not be used for future extensions
Y7	NC1_Y7	I	—	Not connected. These pins are not connected on package level and will not be used for future extensions
H18	PHYx_RESREF	I	—	PHYx Resistor Reference
AC10	VAGND1	I	—	Negative Analog Reference Voltage 1
W5	VAGND2	I	—	Negative Analog Reference Voltage 2
AC2	VAGND3	I	—	Negative Analog Reference Voltage 3
AC9	VAREF1	I	—	Positive Analog Reference Voltage 1

(table continues...)

Table 30 (continued) Supply functions

Ball	Symbol	Ctrl.	Buffer type	Function
W4	VAREF2	I	—	Positive Analog Reference Voltage 2
AC1	VAREF3	I	—	Positive Analog Reference Voltage 3
K16, L10, L12, L15, M11, M16, R11, R16, T10, T12, T15, U11	VDD	I	—	Digital Core Power Supply (0.9V / 0.95V / 1V)
W14	VDDEVRSB	I	—	Standby Power Supply (5V / 3.3V) for the Standby SRAM
A2, AA22, AB23, AD25, AE26, B3, D5, E6	VDDEXT	I	—	External Power Supply (5V / 3.3V)
AC22	VDDEXTDC	I	—	External DCDC Supply (3.3V / 5.0V / 5.5V / 6.5V)
A25, B24, E21, G19	VDDEXTHS	I	—	External Power Supply (5V / 3.3V)
D22	VDDEXTHS_SENSE	I/O	—	External Power Supply (5V / 3.3V)
T23	VDDEXTOSC	I	—	External Power Supply for Oscillator (shall be supplied with same level as used for VDDEXT)
G8	VDDFLEX	I	—	External Power Supply for FLEX Port Pads (5V / 3.3V)
AC8, AE8	VDDM	I	—	External Power Supply (5V / 3.3V)
B26	VDDPHPHY1	I	—	PHY1 External Power Supply (1.8V)
D26, G26	VDDPHY1	I	—	PHY1 Digital Core Power Supply (0.9V / 0.95V / 1V)
K11	VDDSB	I	—	Retention Power Supply (1V) for the Standby SRAM
U16	VDD_SENSE	I/O	—	Digital Core Power Supply (0.9V / 0.95V / 1V)
AC20	VGATE1N	O	—	DCDC N ch MOSFET gate driver output
AC21	VGATE1P	O	—	DCDC P ch MOSFET gate driver output

(table continues...)

Table 30 (continued) Supply functions

Ball	Symbol	Ctrl.	Buffer type	Function
K12, K13, K14, K15, L13, L14, M10, M13, M14, M17, N10, N11, N12, N13, N14, N15, N16, N17, P10, P11, P12, P13, P14, P15, P16, P17, R10, R13, R14, R17, T13, T14, U12, U13	VSS	I	—	Digital Ground
AE25, AF26, B25, D4, E22, E5, G20, G7, H19, H8, W19, Y20	VSSEXT	I	—	External Vss
AB22, AC23	VSSEXTDC	I	—	DCDC Ground
D23	VSSEXTHS_SENSE	I/O	—	External Vss
P23	VSSEXTOSC	I	—	Oscillator Ground
AC7, AE7	VSSM	I	—	External Vss
D25, G25	VSSPHY	I	—	PHY Digital Ground
U15	VSS_SENSE	I/O	—	Digital Ground

3.3 BGA292_STD package variant pin configuration

Related information

[Logic symbols for package variants](#) on page 27

[BGA436_STD package variant pin configuration](#) on page 28

[Pad Sequence](#) on page 422

[Legend](#) on page 444

3.3.1 BGA292_STD port 00

Table 31 Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
G1	P00.0	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN4_10			Mux input channel 4 of TIM module 0
	GTM_TIM2_IN0_1			Mux input channel 0 of TIM module 2
	GTM_TIM3_IN0_1			Mux input channel 0 of TIM module 3
	GTM_TIM5_IN4_9			Mux input channel 4 of TIM module 5
	MSC0_INJ0			Injection signal from port
	GPT121_CAPINA			Trigger input to capture value of timer T5 into CAPREL register (input A)
	GTM_CDTM1_DTM0_5			Input mux of CDTM1_DTM0_AUXIN0/1
	GTM_CDTM1_DTM4_5			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM0_5			Input mux of CDTM1_DTM0_AUXIN0/1
	EGTM_CDTM1_DTM4_5			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_TIM0_IN4_10			Mux input channel 4 of TIM module 0
	EGTM_TIM2_IN0_1			Mux input channel 0 of TIM module 2
	P00.0	O0		General-purpose output
	GTM_TOUT9	O1		GTM muxed output
	ASCLIN3_ASCLK	O2		Shift clock output
	ASCLIN3_ATX	O3		Transmit output
	—	O4		Reserved
	CAN10_TXD	O5		CAN transmit output node 0
	PSI5_TX0	O6		TXD outputs (send data)
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT9	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
G2	P00.1	I	SLOW / PU1 /	General-purpose input
	GTM_TIM0_IN4_11			Mux input channel 4 of TIM module 0

(table continues...)

Table 31 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TIM1_IN2_11		VDDEXT / ES	Mux input channel 2 of TIM module 1
	GTM_TIM2_IN1_1			Mux input channel 1 of TIM module 2
	GTM_TIM3_IN1_1			Mux input channel 1 of TIM module 3
	GTM_TIM5_IN5_11			Mux input channel 5 of TIM module 5
	ASCLIN3_ARXE			Receive input
	CAN10_RXDA			CAN receive input node 0
	PSI5_RX0A			RXD inputs (receive data) channel 0
	GPT121_T2INA			Trigger/gate input of timer T2
	GTM_CDTM1_DTM1_5			Input mux of CDTM1_DTM1_AUXIN0/1
	SENT0_SENT0B			Receive input channel 0
	EGTM_CDTM1_DTM1_5			Input mux of CDTM1_DTM1_AUXIN0/1
	GTM_CDTM3_DTM1_1			Input mux of CDTM3_DTM1_AUXIN0/1
	EGTM_TIM0_IN4_11			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN2_11			Mux input channel 2 of TIM module 1
	EGTM_TIM2_IN1_1			Mux input channel 1 of TIM module 2
	ADC_TMADC2CH11	AI		Analog Input for TMADC2 Channel 11
	ADC_DSADC5NA			Analog Input for DSADC5 Negative Input A
	P00.1	O0		General-purpose output
	GTM_TOUT10	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	SENT0_SPC0	O3		Transmit output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT10	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 31 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
H1	P00.2	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	GTM_TIM2_IN1_2			Mux input channel 1 of TIM module 2
	GTM_TIM3_IN1_2			Mux input channel 1 of TIM module 3
	GTM_TIM5_IN6_11			Mux input channel 6 of TIM module 5
	I2C0_SCLG			Serial Clock Input 6
	SENT1_SENT0B			Receive input channel 0
	GPT121_T2EUDA			Count direction control input of timer T2
	EGTM_CDTM1_DTM2_5			Input mux of CDTM1_DTM2_AUXIN0/1
	EGTM_CDTM1_DTM3_5			Input mux of CDTM1_DTM3_AUXIN0/1
	EGTM_TIM2_IN1_2			Mux input channel 1 of TIM module 2
	ADC_TMADC2CH10	AI		Analog Input for TMADC2 Channel 10
	ADC_DSADC5PA			Analog Input for DSADC5 Positive Input A
	ADC_FCC5			Analog Input for FCC5
	P00.2	O0		General-purpose output
	GTM_TOUT11	O1		GTM muxed output
	ASCLIN3_ASCLK	O2		Shift clock output
	CAN21_TXD	O3		CAN transmit output node 1
	PSI5_TX0	O4		TXD outputs (send data)
	CAN03_TXD	O5		CAN transmit output node 3
	QSPI3_SLSO4	O6		Master slave select output
	I2C0_SCL	O7		Serial Clock Output
	—	O8		Reserved
	EGTM_TOUT11	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
H2	P00.3	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	GTM_TIM1_IN3_11			Mux input channel 3 of TIM module 1
	GTM_TIM2_IN2_1			Mux input channel 2 of TIM module 2
	GTM_TIM3_IN2_1			Mux input channel 2 of TIM module 3

(table continues...)

Table 31 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TIM5_IN7_10			Mux input channel 7 of TIM module 5
	GPT121_T4EUDA			Count direction control input of timer T4
	I2C0_SDAG			Serial Data Input 6
	PSI5_RX1A			RXD inputs (receive data) channel 1
	CAN03_RXDA			CAN receive input node 3
	CAN21_RXDA			CAN receive input node 1
	PSI5S0_RXA			RX data input
	SENT0_SENT1B			Receive input channel 1
	GTM_CDTM1_DTM5_5			Input mux of CDTM1_DTM5_AUXIN0/1
	EGTM_CDTM1_DTM5_5			Input mux of CDTM1_DTM5_AUXIN0/1
	EGTM_TIM1_IN3_11			Mux input channel 3 of TIM module 1
	EGTM_TIM2_IN2_1			Mux input channel 2 of TIM module 2
	ADC_TMADC2CH9	AI		Analog Input for TMADC2 Channel 9
	ADC_DSADC5NB			Analog Input for DSADC5 Negative Input B
	P00.3	O0		General-purpose output
	GTM_TOUT12	O1		GTM muxed output
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	SENT0_SPC1	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	I2C0_SDA	O7		Serial Data Output
	—	O8		Reserved
	EGTM_TOUT12	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
J1	P00.4	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	GTM_TIM2_IN3_1			Mux input channel 3 of TIM module 2
	GTM_TIM3_IN3_1			Mux input channel 3 of TIM module 3

(table continues...)

Table 31 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TIM6_IN4_1			Mux input channel 4 of TIM module 6
	SCU_E_REQ2C			ERU channel 2 input C
	SENT1_SENT1B			Receive input channel 1
	GPT121_T5INA			Trigger/gate input of timer T5
	GTM_CDTM3_DTM0_1			Input mux of CDTM3_DTM0_AUXIN0/1
	GTM_CDTM5_DTM4_1			Input mux of CDTM5_DTM4_AUXIN0/1
	EGTM_TIM2_IN3_1			Mux input channel 3 of TIM module 2
	ADC_TMADC2CH8	AI		Analog Input for TMADC2 Channel 8
	ADC_DSADC5PB			Analog Input for DSADC5 Positive Input B
	P00.4	O0		General-purpose output
	GTM_TOUT13	O1		GTM muxed output
	PSI5S0_TX	O2		TX data output
	CAN11_TXD	O3		CAN transmit output node 1
	PSI5_TX1	O4		TXD outputs (send data)
	—	O5		Reserved
	SENT1_SPC1	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT13	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
J2	P00.5	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	GTM_TIM0_IN6_11			Mux input channel 6 of TIM module 0
	GTM_TIM1_IN6_10			Mux input channel 6 of TIM module 1
	GTM_TIM2_IN4_1			Mux input channel 4 of TIM module 2
	GTM_TIM3_IN0_11			Mux input channel 0 of TIM module 3
	GTM_TIM3_IN4_1			Mux input channel 4 of TIM module 3
	PSI5_RX2A			RXD inputs (receive data) channel 2
	SENT0_SENT2B			Receive input channel 2

(table continues...)

Table 31 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GPT121_T5EUDA			Count direction control input of timer T5
	CAN11_RXDB			CAN receive input node 1
	GTM_CDTM1_DTM0_2			Input mux of CDTM1_DTM0_AUXIN0/1
	GTM_CDTM1_DTM1_2			Input mux of CDTM1_DTM1_AUXIN0/1
	GTM_CDTM4_DTM0_3			Input mux of CDTM4_DTM0_AUXIN0/1
	GTM_CDTM4_DTM1_3			Input mux of CDTM4_DTM1_AUXIN0/1
	EGTM_CDTM1_DTM0_2			Input mux of CDTM1_DTM0_AUXIN0/1
	EGTM_CDTM1_DTM1_2			Input mux of CDTM1_DTM1_AUXIN0/1
	EGTM_CDTM1_DTM2_2			Input mux of CDTM1_DTM2_AUXIN0/1
	EGTM_TIM0_IN6_11			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN6_10			Mux input channel 6 of TIM module 1
	EGTM_TIM2_IN4_1			Mux input channel 4 of TIM module 2
	ADC_TMADC2CH7	AI		Analog Input for TMADC2 Channel 7
	P00.5	O0		General-purpose output
	GTM_TOUT14	O1		GTM muxed output
	ADC_PWM1	O2		Negative PWM
	QSPI3_SLSO3	O3		Master slave select output
	—	O4		Reserved
	ADC_BFL0	O5		Boundary flags from FCC
	SENT0_SPC2	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT14	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
J4	P00.6	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	GTM_TIM2_IN5_1			Mux input channel 5 of TIM module 2
	GTM_TIM3_IN1_13			Mux input channel 1 of TIM module 3
	GTM_TIM3_IN5_1			Mux input channel 5 of TIM module 3

(table continues...)

Table 31 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SENT1_SENT2B			Receive input channel 2
	ASCLIN5_ARXA			Receive input
	GPT121_T6EUDA			Count direction control input of core timer T6
	GTM_CDTM3_DTM0_2			Input mux of CDTM3_DTM0_AUXIN0/1
	GTM_CDTM5_DTM5_1			Input mux of CDTM5_DTM5_AUXIN0/1
	EGTM_TIM2_IN5_1			Mux input channel 5 of TIM module 2
	ADC_TMADC2CH6	AI		Analog Input for TMADC2 Channel 6
	P00.6	O0		General-purpose output
	GTM_TOUT15	O1		GTM muxed output
	ADC_PWM0	O2		Positive PWM
	—	O3		Reserved
	PSI5_TX2	O4		TXD outputs (send data)
	ADC_EMUXCTRL10	O5		EMUX1 Control from TMADC to PORTS
	SENT1_SPC2	O6		Transmit output
	GPT121_T3OUT	O7		External output for overflow/underflow detection of core timer T3
	—	O8		Reserved
	EGTM_TOUT15	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
K1	P00.7	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	GTM_TIM1_IN6_11			Mux input channel 6 of TIM module 1
	GTM_TIM2_IN6_1			Mux input channel 6 of TIM module 2
	GTM_TIM3_IN2_11			Mux input channel 2 of TIM module 3
	GTM_TIM3_IN6_1			Mux input channel 6 of TIM module 3
	SENT0_SENT3B			Receive input channel 3
	GPT120_T2INA			Trigger/gate input of timer T2
	GPT121_T6INA			Trigger/gate input of core timer T6
	GTM_CDTM0_DTM0_3			Input mux of CDTM0_DTM0_AUXIN0/1

(table continues...)

Table 31 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_CDTM0_DTM1_3			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM0_DTM0_3			Input mux of CDTM0_DTM0_AUXIN0/1
	EGTM_CDTM0_DTM1_3			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM0_DTM2_3			Input mux of CDTM0_DTM2_AUXIN0/1
	EGTM_CDTM0_DTM3_3			Input mux of CDTM0_DTM3_AUXIN0/1
	EGTM_TIM1_IN6_11			Mux input channel 6 of TIM module 1
	EGTM_TIM2_IN6_1			Mux input channel 6 of TIM module 2
	ADC_TMADC2CH5	AI		Analog Input for TMADC2 Channel 5
	ADC_DSADC4NA			Analog Input for DSADC4 Negative Input A
	P00.7	O0		General-purpose output
	GTM_TOUT16	O1		GTM muxed output
	ASCLIN5_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	ADC_EMUXCTRL11	O5		EMUX1 Control from TMADC to PORTS
	SENT0_SPC3	O6		Transmit output
	PSI5S1_TX	O7		TX data output
	—	O8		Reserved
	EGTM_TOUT16	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
K4	P00.8	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	GTM_TIM0_IN7_10			Mux input channel 7 of TIM module 0
	GTM_TIM1_IN7_10			Mux input channel 7 of TIM module 1
	GTM_TIM2_IN7_1			Mux input channel 7 of TIM module 2
	GTM_TIM3_IN3_11			Mux input channel 3 of TIM module 3
	GTM_TIM3_IN7_1			Mux input channel 7 of TIM module 3
	SENT1_SENT3B			Receive input channel 3
	GPT120_T2EUDA			Count direction control input of timer T2

(table continues...)

Table 31 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	PSI5S1_RXB			RX data input
	GTM_CDTM6_DTM5_1			Input mux of CDTM6_DTM5_AUXIN0/1
	EGTM_CDTM1_DTM3_2			Input mux of CDTM1_DTM3_AUXIN0/1
	EGTM_TIM0_IN7_10			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_10			Mux input channel 7 of TIM module 1
	EGTM_TIM2_IN7_1			Mux input channel 7 of TIM module 2
	ADC_TMADC2CH4	AI		Analog Input for TMADC2 Channel 4
	ADC_DSADC4PA			Analog Input for DSADC4 Positive Input A
	ADC_FCC4			Analog Input for FCC4
	P00.8	O0		General-purpose output
	GTM_TOUT17	O1		GTM muxed output
	QSPI3_SLSO6	O2		Master slave select output
	—	O3		Reserved
	—	O4		Reserved
	ADC_EMUXCTRL12	O5		EMUX1 Control from TMADC to PORTS
	SENT1_SPC3	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT17	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
K2	P00.9	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	GTM_TIM0_IN0_1			Mux input channel 0 of TIM module 0
	GTM_TIM1_IN0_1			Mux input channel 0 of TIM module 1
	GTM_TIM1_IN7_11			Mux input channel 7 of TIM module 1
	GTM_TIM4_IN0_7			Mux input channel 0 of TIM module 4
	SENT0_SENT4B			Receive input channel 4
	GPT120_T4EUDA			Count direction control input of timer T4
	GTM_CDTM3_DTM1_2			Input mux of CDTM3_DTM1_AUXIN0/1

(table continues...)

Table 31 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_CDTM6_DTM4_1			Input mux of CDTM6_DTM4_AUXIN0/1
	ASCLIN4_ARXG			Receive input
	EGTM_TIM0_IN0_1			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_1			Mux input channel 0 of TIM module 1
	EGTM_TIM1_IN7_11			Mux input channel 7 of TIM module 1
	ADC_TMADC2CH3	AI		Analog Input for TMADC2 Channel 3
	ADC_DSADC4NB			Analog Input for DSADC4 Negative Input B
	P00.9	O0		General-purpose output
	GTM_TOUT18	O1		GTM muxed output
	QSPI3_SLS07	O2		Master slave select output
	ASCLIN3_ARTS	O3		Ready to send output
	ADC_EMUXCTRL13	O4		EMUX1 Control from TMADC to PORTS
	ASCLIN4_ATX	O5		Transmit output
	SENT0_SPC4	O6		Transmit output
	GPT121_T6OUT	O7		External output for overflow/underflow detection of core timer T6
	—	O8		Reserved
	EGTM_TOUT18	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
K5	P00.10	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	GTM_TIM0_IN1_1			Mux input channel 1 of TIM module 0
	GTM_TIM1_IN1_1			Mux input channel 1 of TIM module 1
	GTM_TIM4_IN1_11			Mux input channel 1 of TIM module 4
	SENT1_SENT4B			Receive input channel 4
	GPT121_T3EUDA			Count direction control input of core timer T3
	GTM_CDTM0_DTM1_5			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM0_DTM1_5			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_TIM0_IN1_1			Mux input channel 1 of TIM module 0

(table continues...)

Table 31 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM1_IN1_1	AI		Mux input channel 1 of TIM module 1
	ADC_TMADC2CH2			Analog Input for TMADC2 Channel 2
	ADC_DSADC4PB			Analog Input for DSADC4 Positive Input B
	P00.10	O0		General-purpose output
	GTM_TOUT19	O1		GTM muxed output
	ASCLIN4_ASCLK	O2		Shift clock output
	—	O3		Reserved
	ASCLIN4_ATX	O4		Transmit output
	—	O5		Reserved
	SENT1_SPC4	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT19	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
L1	P00.11	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	GTM_TIM0_IN2_1			Mux input channel 2 of TIM module 0
	GTM_TIM1_IN2_1			Mux input channel 2 of TIM module 1
	GTM_TIM4_IN2_11			Mux input channel 2 of TIM module 4
	SENT0_SENT5B			Receive input channel 5
	GPT121_T3INA			Trigger/gate input of core timer T3 (input A, B and C)
	GTM_CDTM0_DTM0_5			Input mux of CDTM0_DTM0_AUXIN0/1
	GTM_CDTM0_DTM4_5			Input mux of CDTM0_DTM4_AUXIN0/1
	GTM_CDTM0_DTM5_5			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_CDTM0_DTM0_5			Input mux of CDTM0_DTM0_AUXIN0/1
	EGTM_CDTM0_DTM4_5			Input mux of CDTM0_DTM4_AUXIN0/1
	EGTM_CDTM0_DTM5_5			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_TIM0_IN2_1			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_1			Mux input channel 2 of TIM module 1

(table continues...)

Table 31 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ADC_TMADC2CH1	AI		Analog Input for TMADC2 Channel 1
	P00.11	O0		General-purpose output
	GTM_TOUT20	O1		GTM muxed output
	ASCLIN4_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	ADC_CLKOUT0	O4		Clock output from EXMOD
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT20	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
L2	P00.12	I	SLOW / PU1 / VDDEXT / ES1	General-purpose input
	GTM_TIM0_IN3_1			Mux input channel 3 of TIM module 0
	GTM_TIM1_IN3_1			Mux input channel 3 of TIM module 1
	GTM_TIM4_IN3_11			Mux input channel 3 of TIM module 4
	ASCLIN3_ACTSA			Clear to send input
	ASCLIN4_ARXA			Receive input
	SENT1_SENT5B			Receive input channel 5
	GPT121_T4INA			Trigger/gate input of timer T4
	EGTM_CDTM0_DTM2_5			Input mux of CDTM0_DTM2_AUXIN0/1
	EGTM_CDTM0_DTM3_5			Input mux of CDTM0_DTM3_AUXIN0/1
	EGTM_TIM0_IN3_1			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_1			Mux input channel 3 of TIM module 1
	ADC_TMADC2CH0	AI		Analog Input for TMADC2 Channel 0
	P00.12	O0		General-purpose output
	GTM_TOUT21	O1		GTM muxed output
	ADC_EMUXCTRL30	O2		EMUX3 Control from TMADC to PORTS

(table continues...)

Table 31 (continued) Port 00 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT21	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

3.3.2 BGA292_STD port 01

Table 32 Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
G5	P01.3	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN5_8			Mux input channel 5 of TIM module 0
	GTM_TIM2_IN0_11			Mux input channel 0 of TIM module 2
	GTM_TIM4_IN5_2			Mux input channel 5 of TIM module 4
	QSPI3_SLSIB			Slave select input
	SENT1_SENT12A			Receive input channel 12
	CAN32_RXDA			CAN receive input node 2
	LETH0_P0_MDIOB			LETH PortX MDIO interface data input
	LETH0_P0_EDB			LETH PortX TC14 interface energy detection input
	EGTM_TIM0_IN5_8			Mux input channel 5 of TIM module 0
	EGTM_TIM2_IN0_11			Mux input channel 0 of TIM module 2
	ADC_TMADC2CH14	AI		Analog Input for TMADC2 Channel 14
	P01.3	O0		General-purpose output
	GTM_TOUT111	O1		GTM muxed output
	CAN31_TXD	O2		CAN transmit output node 1

(table continues...)

Table 32 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ADC_CLKOUT7	O3		Clock output from EXMOD
	QSPI3_SLSO9	O4		Master slave select output
	CAN01_TXD	O5		CAN transmit output node 1
	—	O6		Reserved
	SENT1_SPC12	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT111	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
G4	P01.4	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN6_8			Mux input channel 6 of TIM module 0
	GTM_TIM2_IN1_10			Mux input channel 1 of TIM module 2
	GTM_TIM4_IN6_2			Mux input channel 6 of TIM module 4
	CAN01_RXDC			CAN receive input node 1
	SENT0_SENT13A			Receive input channel 13
	EGTM_TIM0_IN6_8			Mux input channel 6 of TIM module 0
	EGTM_TIM2_IN1_10			Mux input channel 1 of TIM module 2
	ADC_TMADC2CH13	AI		Analog Input for TMADC2 Channel 13
	P01.4	O0		General-purpose output
	GTM_TOUT112	O1		GTM muxed output
	ADC_EMUXCTRL21	O2		EMUX2 Control from TMADC to PORTS
	—	O3		Reserved
	QSPI3_SLSO10	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	LETH0_P0_TXD	O7		LETH PortX TC14 interface transmit data output
	CANXL00_TXD	O8		CANXL transmit output node 0

(table continues...)

Table 32 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TOUT112	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	—			
H5	P01.5	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM2_IN2_7			Mux input channel 2 of TIM module 2
	GTM_TIM2_IN3_7			Mux input channel 3 of TIM module 2
	GTM_TIM5_IN3_2			Mux input channel 3 of TIM module 5
	QSPI3_MRSTC			Master SPI data input
	SENT1_SENT13A			Receive input channel 13
	CANXL00_RXDG			CANXL receive input node 0
	EGTM_TIM2_IN2_7			Mux input channel 2 of TIM module 2
	EGTM_TIM2_IN3_7			Mux input channel 3 of TIM module 2
	LETH0_P0_RXDG			LETH PortX TC14 interface receive data input
	ADC_TMADC2CH12	AI		Analog Input for TMADC2 Channel 12
	P01.5	O0		General-purpose output
	GTM_TOUT113	O1		GTM muxed output
	ADC_EMUXCTRL22	O2		EMUX2 Control from TMADC to PORTS
	—	O3		Reserved
	QSPI3_MRST	O4		Slave SPI data output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT113	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—			
	—			
	—			
	—			
	—			
	—			
	—			

(table continues...)

Table 32 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O15		Reserved
	LETH0_P0_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
H4	P01.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM2_IN5_7			Mux input channel 5 of TIM module 2
	GTM_TIM5_IN5_3			Mux input channel 5 of TIM module 5
	GTM_TIM5_IN6_2			Mux input channel 6 of TIM module 5
	QSPI3_MTSRC			Slave SPI data input
	CAN32_RXDD			CAN receive input node 2
	EGTM_TIM2_IN5_7			Mux input channel 5 of TIM module 2
	P01.6	O0		General-purpose output
	GTM_TOUT114	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	QSPI3_MTSR	O4		Master SPI data output
	—	O5		Reserved
	ADC_CLKOUT6	O6		Clock output from EXMOD
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT114	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
J5	P01.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM2_IN7_7			Mux input channel 7 of TIM module 2
	GTM_TIM5_IN7_2			Mux input channel 7 of TIM module 5
	QSPI3_SCLKC			Slave SPI clock inputs
	EGTM_TIM2_IN7_7			Mux input channel 7 of TIM module 2
	P01.7	O0		General-purpose output
	GTM_TOUT115	O1		GTM muxed output

(table continues...)

Table 32 (continued) Port 01 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ADC_EMUXCTRL23	O2		EMUX2 Control from TMADC to PORTS
	—	O3		Reserved
	QSPI3_SCLK	O4		Master SPI clock output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT115	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

3.3.3 BGA292_STD port 02

Table 33 Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
B1	P02.0	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN0_2			Mux input channel 0 of TIM module 0
	GTM_TIM1_IN0_2			Mux input channel 0 of TIM module 1
	LETH1_P0_AUX			LETH PortX auxiliary snapshot signal
	ASCLIN2_ARXG			Receive input
	GTM_CDTM0_DTM4_1			Input mux of CDTM0_DTM4_AUXIN0/1
	SCU_E_REQ3C			ERU channel 3 input C
	CAN31_RXDC			CAN receive input node 1
	ADC_TRIG56			Triggers from PORTS to ADC
	GTM_CDTM1_DTM0_6			Input mux of CDTM1_DTM0_AUXIN0/1
	GTM_CDTM3_DTM0_6			Input mux of CDTM3_DTM0_AUXIN0/1
	GTM_CDTM4_DTM0_6			Input mux of CDTM4_DTM0_AUXIN0/1
	GTM_CDTM4_DTM4_6			Input mux of CDTM4_DTM4_AUXIN0/1
	GTM_CDTM4_DTM5_6			Input mux of CDTM4_DTM5_AUXIN0/1

(table continues...)

Table 33 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_CDTM0_DTM4_1			Input mux of CDTM0_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM0_6			Input mux of CDTM1_DTM0_AUXIN0/1
	EGTM_TIM0_IN0_2			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_2			Mux input channel 0 of TIM module 1
	P02.0	O0		General-purpose output
	GTM_TOUT0	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	QSPI3_SLSO1_F	O3		Master slave select output
	ADC_PWM1	O4		Negative PWM
	CAN00_TXD	O5		CAN transmit output node 0
	ERAY0_TXDA	O6		Transmit Channel A
	LETH0_P0_TXD	O7		LETH PortX TC14 interface transmit data output
	CANXL00_TXD	O8		CANXL transmit output node 0
	EGTM_TOUT0_F	O9		eGTM muxed output
	—	O10		Reserved
	QSPI3_SLSO5_F	O11		Master slave select output
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM0_CH0_F	PO		High resolution PWM 0 output channels
C2	P02.1	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN1_2			Mux input channel 1 of TIM module 0
	GTM_TIM1_IN1_2			Mux input channel 1 of TIM module 1
	ERAY0_RXDA2			Receive Channel A2
	ASCLIN2_ARXB			Receive input
	CAN00_RXDA			CAN receive input node 0
	SCU_E_REQ2B			ERU channel 2 input B
	SENT0_SENT14A			Receive input channel 14
	ADC_TRIG57			Triggers from PORTS to ADC
	ADC_CLKIN4			Clock input to EXMOD
	GTM_CDTM0_DTM1_6			Input mux of CDTM0_DTM1_AUXIN0/1
	GTM_CDTM1_DTM1_6			Input mux of CDTM1_DTM1_AUXIN0/1

(table continues...)

Table 33 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_CDTM3_DTM1_6			Input mux of CDTM3_DTM1_AUXIN0/1
	GTM_CDTM4_DTM1_6			Input mux of CDTM4_DTM1_AUXIN0/1
	EGTM_CDTM0_DTM1_6			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM1_DTM1_6			Input mux of CDTM1_DTM1_AUXIN0/1
	EGTM_TIM0_IN1_2			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_2			Mux input channel 1 of TIM module 1
	QSPI3_MRSTG_F			Master SPI data input
	CANXL00_RXDC			CANXL receive input node 0
	GPT121_CAPINB3			Trigger input to capture value of timer T5 into CAPREL register (input B)
	LETH0_P0_RXDC			LETH PortX TC14 interface receive data input
	P02.1	O0		General-purpose output
	GTM_TOUT1	O1		GTM muxed output
	QSPI4_SLSO7	O2		Master slave select output
	QSPI3_SLSO2	O3		Master slave select output
	ADC_PWM0	O4		Positive PWM
	—	O5		Reserved
	ADC_CLKOUT1	O6		Clock output from EXMOD
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT1_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
C1	P02.2	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN2_2			Mux input channel 2 of TIM module 0
	GTM_TIM1_IN2_2			Mux input channel 2 of TIM module 1
	SENT0_SENT7B			Receive input channel 7

(table continues...)

Table 33 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_CDTM0_DTM0_6			Input mux of CDTM0_DTM0_AUXIN0/1
	GTM_CDTM2_DTM1_7			Input mux of CDTM2_DTM1_AUXIN0/1
	GTM_CDTM3_DTM5_7			Input mux of CDTM3_DTM5_AUXIN0/1
	GTM_CDTM5_DTM5_7			Input mux of CDTM5_DTM5_AUXIN0/1
	GTM_CDTM6_DTM5_7			Input mux of CDTM6_DTM5_AUXIN0/1
	EGTM_CDTM0_DTM0_6			Input mux of CDTM0_DTM0_AUXIN0/1
	EGTM_CDTM0_DTM2_6			Input mux of CDTM0_DTM2_AUXIN0/1
	EGTM_TIM0_IN2_2			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_2			Mux input channel 2 of TIM module 1
	EGTM_CDTM2_DTM1_7			Input mux of CDTM2_DTM1_AUXIN0/1
	P02.2	O0		General-purpose output
	GTM_TOUT2	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	QSPI3_SLSO3_F	O3		Master slave select output
	PSI5_TX0	O4		TXD outputs (send data)
	CAN02_TXD	O5		CAN transmit output node 2
	ERAY0_TXDB	O6		Transmit Channel B
	LETH0_P1_TXD	O7		LETH PortX TC14 interface transmit data output
	CANXL01_TXD	O8		CANXL transmit output node 1
	EGTM_TOUT2_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM0_CH1_F	PO		High resolution PWM 0 output channels
D2	P02.3	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN3_2			Mux input channel 3 of TIM module 0
	GTM_TIM1_IN3_2			Mux input channel 3 of TIM module 1
	ADC_CLKIN5			Clock input to EXMOD
	ERAY0_RXDB2			Receive Channel B2
	CAN02_RXDB			CAN receive input node 2

(table continues...)

Table 33 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN1_ARXG			Receive input
	MSC1_SDI1			Upstream asynchronous input signal
	PSI5_RX0B			RXD inputs (receive data) channel 0
	GTM_CDTM2_DTM0_7			Input mux of CDTM2_DTM0_AUXIN0/1
	SENT1_SENT6B			Receive input channel 6
	GTM_CDTM3_DTM4_7			Input mux of CDTM3_DTM4_AUXIN0/1
	GTM_CDTM5_DTM4_7			Input mux of CDTM5_DTM4_AUXIN0/1
	EGTM_CDTM0_DTM3_6			Input mux of CDTM0_DTM3_AUXIN0/1
	EGTM_CDTM1_DTM3_6			Input mux of CDTM1_DTM3_AUXIN0/1
	EGTM_CDTM2_DTM0_7			Input mux of CDTM2_DTM0_AUXIN0/1
	EGTM_TIM0_IN3_2			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_2			Mux input channel 3 of TIM module 1
	SENT0_SENT12A			Receive input channel 12
	CANXL01_RXDC			CANXL receive input node 1
	LETH0_P1_RXDC			LETH PortX TC14 interface receive data input
	P02.3	O0		General-purpose output
	GTM_TOUT3	O1		GTM muxed output
	ASCLIN2_ASLSO	O2		Slave select signal output
	QSPI3_SLSO4	O3		Master slave select output
	ADC_CLKOUT2	O4		Clock output from EXMOD
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT3_F	O9		eGTM muxed output
	—	O10		Reserved
	LETH1_P0_PPS1	O11		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 33 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
D1	P02.4	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN4_1			Mux input channel 4 of TIM module 0
	GTM_TIM1_IN4_1			Mux input channel 4 of TIM module 1
	SENT0_SENT6B			Receive input channel 6
	ADC_DATA5			Modulated data to EXMOD
	QSPI3_SLSIA_F			Slave select input
	GTM_CDTM0_DTM4_6			Input mux of CDTM0_DTM4_AUXIN0/1
	I2C0_SDAA			Serial Data Input 0
	CAN11_RXDA			CAN receive input node 1
	GTM_CDTM1_DTM4_6			Input mux of CDTM1_DTM4_AUXIN0/1
	GTM_CDTM2_DTM5_7			Input mux of CDTM2_DTM5_AUXIN0/1
	GTM_CDTM3_DTM4_6			Input mux of CDTM3_DTM4_AUXIN0/1
	GTM_CDTM5_DTM4_6			Input mux of CDTM5_DTM4_AUXIN0/1
	GTM_CDTM6_DTM4_6			Input mux of CDTM6_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM4_6			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_CDTM2_DTM5_7			Input mux of CDTM2_DTM5_AUXIN0/1
	EGTM_TIM0_IN4_1			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_1			Mux input channel 4 of TIM module 1
	EGTM_CDTM0_DTM4_6			Input mux of CDTM0_DTM4_AUXIN0/1
	LETH0_P0_EDC			LETH PortX TC14 interface energy detection input
	LETH0_P0_MDIOC			LETH PortX MDIO interface data input
	P02.4	O0		General-purpose output
	GTM_TOUT4	O1		GTM muxed output
	ASCLIN2_ASCLK	O2		Shift clock output
	QSPI3_SLSO0_F	O3		Master slave select output
	PSI5S0_CLK	O4		PSI5S CLK is a clock that can be used on a pin to drive the external PHY.
	I2C0_SDA	O5		Serial Data Output
	ERAY0_TXENA	O6		Transmit Enable Channel A
	—	O7		Reserved
	—	O8		Reserved

(table continues...)

Table 33 (continued) **Port 02 functions**

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TOUT4_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM0_CH2_F	PO		High resolution PWM 0 output channels
	LETH0_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
E2	P02.5	I	FAST / PU1 / VDDEXT / ES	General-purpose input
GTM_TIM0_IN5_1	Mux input channel 5 of TIM module 0			
GTM_TIM1_IN5_1	Mux input channel 5 of TIM module 1			
SENT1_SENT1C	Receive input channel 1			
I2C0_SCLA	Serial Clock Input 0			
PSI5_RX1B	RXD inputs (receive data) channel 1			
PSI5S0_RXB	RX data input			
QSPI3_MRSTA_F	Master SPI data input			
GTM_CDTM1_DTM5_6	Input mux of CDTM1_DTM5_AUXIN0/1			
GTM_CDTM2_DTM5_6	Input mux of CDTM2_DTM5_AUXIN0/1			
GTM_CDTM3_DTM5_6	Input mux of CDTM3_DTM5_AUXIN0/1			
GTM_CDTM5_DTM5_6	Input mux of CDTM5_DTM5_AUXIN0/1			
EGTM_CDTM1_DTM3_7	Input mux of CDTM1_DTM3_AUXIN0/1			
EGTM_CDTM1_DTM5_6	Input mux of CDTM1_DTM5_AUXIN0/1			
EGTM_CDTM2_DTM5_6	Input mux of CDTM2_DTM5_AUXIN0/1			
EGTM_TIM0_IN5_1	Mux input channel 5 of TIM module 0			
EGTM_TIM1_IN5_1	Mux input channel 5 of TIM module 1			
GTM_CDTM6_DTM5_6	Input mux of CDTM6_DTM5_AUXIN0/1			
LETH0_P1_EDC	LETH PortX TC14 interface energy detection input			
LETH0_P1_MDIOC	LETH PortX MDIO interface data input			
P02.5	O0			General-purpose output
GTM_TOUT5	O1			GTM muxed output
CAN11_TXD	O2			CAN transmit output node 1

(table continues...)

Table 33 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI3_MRST_F	O3		Slave SPI data output
	—	O4		Reserved
	I2C0_SCL	O5		Serial Clock Output
	ERAY0_TXENB	O6		Transmit Enable Channel B
	QSPI3_MTSR_F	O7		Master SPI data output
	—	O8		Reserved
	EGTM_TOUT5_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM0_CH3_F	PO		High resolution PWM 0 output channels
	LETH0_P1_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
E1	P02.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN6_1			Mux input channel 6 of TIM module 0
	GTM_TIM1_IN1_13			Mux input channel 1 of TIM module 1
	GTM_TIM1_IN6_1			Mux input channel 6 of TIM module 1
	GTM_TIM3_IN0_10			Mux input channel 0 of TIM module 3
	LETH0_P0_AUX			LETH PortX auxiliary snapshot signal
	SENT1_SENT0C			Receive input channel 0
	ADC_DATA4			Modulated data to EXMOD
	GPT120_T3INA			Trigger/gate input of core timer T3 (input A, B and C)
	GTM_CDTM0_DTM5_1			Input mux of CDTM0_DTM5_AUXIN0/1
	GTM_CDTM2_DTM4_6			Input mux of CDTM2_DTM4_AUXIN0/1
	QSPI3_MTSRA_F			Slave SPI data input
	GTM_CDTM4_DTM5_7			Input mux of CDTM4_DTM5_AUXIN0/1
	EGTM_CDTM0_DTM2_7			Input mux of CDTM0_DTM2_AUXIN0/1
	EGTM_CDTM0_DTM5_1			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_CDTM1_DTM2_7			Input mux of CDTM1_DTM2_AUXIN0/1
	EGTM_CDTM2_DTM4_6			Input mux of CDTM2_DTM4_AUXIN0/1

(table continues...)

Table 33 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM0_IN6_1			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN1_13			Mux input channel 1 of TIM module 1
	EGTM_TIM1_IN6_1			Mux input channel 6 of TIM module 1
	P02.6	O0		General-purpose output
	GTM_TOUT6	O1		GTM muxed output
	PSI5S0_TX	O2		TX data output
	QSPI3_MTSR_F	O3		Master SPI data output
	PSI5_TX1	O4		TXD outputs (send data)
	ADC_EMUXCTRL00	O5		EMUX0 Control from TMADC to PORTS
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT6_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM0_CH4_F	PO		High resolution PWM 0 output channels
F2	P02.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN3_13			Mux input channel 3 of TIM module 0
	GTM_TIM0_IN7_1			Mux input channel 7 of TIM module 0
	GTM_TIM1_IN7_1			Mux input channel 7 of TIM module 1
	GTM_TIM3_IN1_10			Mux input channel 1 of TIM module 3
	CAN02_RXDH			CAN receive input node 2
	SENT0_SENT1C			Receive input channel 1
	GPT120_T3EUDA			Count direction control input of core timer T3
	PSI5_RX2B			RXD inputs (receive data) channel 2
	SCU_E_REQ0F			ERU channel 0 input F
	GTM_CDTM1_DTM1_7			Input mux of CDTM1_DTM1_AUXIN0/1
	QSPI3_SCLKA_F			Slave SPI clock inputs
	ADC_TRIG58			Triggers from PORTS to ADC

(table continues...)

Table 33 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_CDTM3_DTM1_7			Input mux of CDTM3_DTM1_AUXIN0/1
	EGTM_CDTM1_DTM1_7			Input mux of CDTM1_DTM1_AUXIN0/1
	EGTM_TIM0_IN3_13			Mux input channel 3 of TIM module 0
	EGTM_TIM0_IN7_1			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_1			Mux input channel 7 of TIM module 1
	GTM_CDTM4_DTM1_7			Input mux of CDTM4_DTM1_AUXIN0/1
	EGTM_CDTM2_DTM3_6			Input mux of CDTM2_DTM3_AUXIN0/1
	P02.7	O0		General-purpose output
	GTM_TOUT7	O1		GTM muxed output
	—	O2		Reserved
	QSPI3_SCLK_F	O3		Master SPI clock output
	—	O4		Reserved
	ADC_EMUXCTRL01	O5		EMUX0 Control from TMADC to PORTS
	SENT1_SPC0	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT7_F	O9		eGTM muxed output
	—	O10		Reserved
	LETH1_P0_PPS1	O11		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM0_CH5_F	PO		High resolution PWM 0 output channels
F1	P02.8	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN7_13			Mux input channel 7 of TIM module 0
	GTM_TIM1_IN0_13			Mux input channel 0 of TIM module 1
	GTM_TIM2_IN0_2			Mux input channel 0 of TIM module 2
	GTM_TIM3_IN0_2			Mux input channel 0 of TIM module 3
	GTM_TIM3_IN2_10			Mux input channel 2 of TIM module 3
	SENT0_SENT0C			Receive input channel 0
	GTM_CDTM0_DTM4_2			Input mux of CDTM0_DTM4_AUXIN0/1

(table continues...)

Table 33 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ADC_DATA3			Modulated data to EXMOD
	GPT120_T4INA			Trigger/gate input of timer T4
	CAN30_RXDB			CAN receive input node 0
	SCU_E_REQ5G			ERU channel 5 input G
	ADC_TRIG59			Triggers from PORTS to ADC
	EGTM_CDTM0_DTM4_2			Input mux of CDTM0_DTM4_AUXIN0/1
	GTM_CDTM1_DTM0_7			Input mux of CDTM1_DTM0_AUXIN0/1
	GTM_CDTM4_DTM0_7			Input mux of CDTM4_DTM0_AUXIN0/1
	EGTM_CDTM1_DTM0_7			Input mux of CDTM1_DTM0_AUXIN0/1
	EGTM_TIM0_IN7_13			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN0_13			Mux input channel 0 of TIM module 1
	EGTM_TIM2_IN0_2			Mux input channel 0 of TIM module 2
	GTM_CDTM4_DTM4_7			Input mux of CDTM4_DTM4_AUXIN0/1
	P02.8	O0		General-purpose output
	GTM_TOUT8	O1		GTM muxed output
	QSPI3_SLSO5_F	O2		Master slave select output
	—	O3		Reserved
	PSI5_TX2	O4		TXD outputs (send data)
	ADC_EMUXCTRL02	O5		EMUX0 Control from TMADC to PORTS
	—	O6		Reserved
	PSI5S1_CLK	O7		PSI5S CLK is a clock that can be used on a pin to drive the external PHY.
	—	O8		Reserved
	EGTM_TOUT8_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM0_CH6_F	PO		High resolution PWM 0 output channels
E4	P02.9	I	FAST / PU1 /	General-purpose input
	GTM_TIM0_IN2_10			Mux input channel 2 of TIM module 0

(table continues...)

Table 33 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TIM3_IN3_10		VDDEXT / ES	Mux input channel 3 of TIM module 3
	GTM_TIM4_IN2_2			Mux input channel 2 of TIM module 4
	SENT0_SENT10B			Receive input channel 10
	GTM_CDTM0_DTM4_7			Input mux of CDTM0_DTM4_AUXIN0/1
	GTM_CDTM2_DTM4_7			Input mux of CDTM2_DTM4_AUXIN0/1
	GTM_CDTM2_DTM0_6			Input mux of CDTM2_DTM0_AUXIN0/1
	GTM_CDTM0_DTM5_2			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_CDTM0_DTM4_7			Input mux of CDTM0_DTM4_AUXIN0/1
	EGTM_CDTM2_DTM4_7			Input mux of CDTM2_DTM4_AUXIN0/1
	EGTM_CDTM0_DTM5_2			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_TIM0_IN2_10			Mux input channel 2 of TIM module 0
	EGTM_CDTM2_DTM0_6			Input mux of CDTM2_DTM0_AUXIN0/1
	EGTM_CDTM2_DTM3_7			Input mux of CDTM2_DTM3_AUXIN0/1
	P02.9	O0		General-purpose output
	GTM_TOUT116	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	—	O3		Reserved
	CAN30_TXD	O4		CAN transmit output node 0
	CAN01_TXD	O5		CAN transmit output node 1
	SENT0_SPC10	O6		Transmit output
	ADC_EMUXCTRL03	O7		EMUX0 Control from TMADC to PORTS
	—	O8		Reserved
	EGTM_TOUT116_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM0_CH7_F	PO		High resolution PWM 0 output channels
F5	P02.10	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN3_10			Mux input channel 3 of TIM module 0
	GTM_TIM3_IN4_11			Mux input channel 4 of TIM module 3

(table continues...)

Table 33 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TIM4_IN3_2			Mux input channel 3 of TIM module 4
	ASCLIN2_ARXC			Receive input
	CAN01_RXDE			CAN receive input node 1
	SENT1_SENT10B			Receive input channel 10
	GTM_CDTM0_DTM1_7			Input mux of CDTM0_DTM1_AUXIN0/1
	GTM_CDTM1_DTM4_7			Input mux of CDTM1_DTM4_AUXIN0/1
	GTM_CDTM2_DTM1_6			Input mux of CDTM2_DTM1_AUXIN0/1
	LETH0_P2_CRSD			LETH PortX MII carrier sense
	EGTM_CDTM0_DTM1_7			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM1_DTM4_7			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM2_6			Input mux of CDTM1_DTM2_AUXIN0/1
	EGTM_CDTM2_DTM1_6			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_TIM0_IN3_10			Mux input channel 3 of TIM module 0
	EGTM_CDTM2_DTM2_7			Input mux of CDTM2_DTM2_AUXIN0/1
	P02.10	O0		General-purpose output
	GTM_TOUT117	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	SENT1_SPC10	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT117_F	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
F4	P02.11	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN7_7			Mux input channel 7 of TIM module 0
	GTM_TIM3_IN5_13			Mux input channel 5 of TIM module 3

(table continues...)

Table 33 (continued) Port 02 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TIM4_IN4_3			Mux input channel 4 of TIM module 4
	SENT0_SENT11B			Receive input channel 11
	CAN30_RXDD			CAN receive input node 0
	SCU_E_REQ7G			ERU channel 7 input G
	GTM_CDTM0_DTM5_7			Input mux of CDTM0_DTM5_AUXIN0/1
	GTM_CDTM1_DTM5_7			Input mux of CDTM1_DTM5_AUXIN0/1
	GTM_CDTM6_DTM4_7			Input mux of CDTM6_DTM4_AUXIN0/1
	EGTM_CDTM0_DTM5_7			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_CDTM1_DTM5_7			Input mux of CDTM1_DTM5_AUXIN0/1
	EGTM_TIM0_IN7_7			Mux input channel 7 of TIM module 0
	ADC_TMADC2CH15	AI		Analog Input for TMADC2 Channel 15
	P02.11	O0		General-purpose output
	GTM_TOUT118	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	SENT0_SPC11	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT118_F	O9		eGTM muxed output
	LETH0_P2_PPS	O10		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

3.3.4 BGA292_STD port 10

Table 34 Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
A7	P10.0	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN4_2			Mux input channel 4 of TIM module 0
	GTM_TIM1_IN4_2			Mux input channel 4 of TIM module 1
	GTM_TIM4_IN0_13			Mux input channel 0 of TIM module 4
	GPT120_T6EUDB			Count direction control input of core timer T6
	SENT0_SENT13B			Receive input channel 13
	QSPI7_MRSTB			Master SPI data input
	GTM_CDTM3_DTM0_5			Input mux of CDTM3_DTM0_AUXIN0/1
	GTM_CDTM4_DTM0_5			Input mux of CDTM4_DTM0_AUXIN0/1
	GTM_CDTM5_DTM4_3			Input mux of CDTM5_DTM4_AUXIN0/1
	ADC_CLKIN3			Clock input to EXMOD
	GTM_CDTM5_DTM5_3			Input mux of CDTM5_DTM5_AUXIN0/1
	GTM_CDTM6_DTM4_3			Input mux of CDTM6_DTM4_AUXIN0/1
	GTM_CDTM6_DTM5_3			Input mux of CDTM6_DTM5_AUXIN0/1
	EGTM_TIM0_IN4_2			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_2			Mux input channel 4 of TIM module 1
	SENT1_SENT10C			Receive input channel 10
	LETH0_P2_MII_RMII_RXD 0B			LETH0 PortX MII and RMII receive data bit 0 (to be used with LETH0_P2_RXCLKB or LETH0_P2_REFCLKB)
	LETH0_P2_MII_RMII_RXD 0D			LETH0 PortX MII and RMII receive data bit 0 (to be used with LETH0_P2_RXCLKD or LETH0_P2_REFCLKD)
	LETH0_P2_RXDF			LETH PortX TC14 interface receive data input
	P10.0	O0		General-purpose output
	GTM_TOUT102	O1		GTM muxed output
	—	O2		Reserved
	QSPI1_SLSO10_F	O3		Master slave select output
	CAN30_TXD	O4		CAN transmit output node 0
	ADC_CLKOUT0	O5		Clock output from EXMOD
	—	O6		Reserved
	CANXL00_TXD	O7		CANXL transmit output node 0
	QSPI7_SLSO0	O8		Master slave select output
	EGTM_TOUT102	O9		eGTM muxed output

(table continues...)

Table 34 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN0_ATX	O10		Transmit output
	—	O11		Reserved
	ERAY0_TXDA	O12		Transmit Channel A
	—	O13		Reserved
	CAN01_TXD	O14		CAN transmit output node 1
	ASCLIN0_ASCLK	O15		Shift clock output
	LETH0_P2_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
B7	P10.1	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN1_3			Mux input channel 1 of TIM module 0
	GTM_TIM1_IN1_3			Mux input channel 1 of TIM module 1
	GTM_TIM4_IN4_13			Mux input channel 4 of TIM module 4
	GPT120_T5EUDB			Count direction control input of timer T5
	QSPI1_MRSTA_F			Master SPI data input
	GTM_CDTM0_DTM0_2			Input mux of CDTM0_DTM0_AUXIN0/1
	GTM_CDTM1_DTM4_3			Input mux of CDTM1_DTM4_AUXIN0/1
	GTM_CDTM1_DTM5_3			Input mux of CDTM1_DTM5_AUXIN0/1
	GTM_CDTM2_DTM1_5			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_CDTM0_DTM0_2			Input mux of CDTM0_DTM0_AUXIN0/1
	EGTM_CDTM0_DTM2_2			Input mux of CDTM0_DTM2_AUXIN0/1
	EGTM_CDTM1_DTM4_3			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM5_3			Input mux of CDTM1_DTM5_AUXIN0/1
	GTM_CDTM3_DTM1_5			Input mux of CDTM3_DTM1_AUXIN0/1
	GTM_CDTM4_DTM1_5			Input mux of CDTM4_DTM1_AUXIN0/1
	EGTM_CDTM2_DTM1_5			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_TIM0_IN1_3			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_3			Mux input channel 1 of TIM module 1
	LETH0_P2_MII_RXD3B			LETH0 PortX MII receive data bit 3 (to be used with LETH0_P2_RXCLKB)
	ASCLIN0_ARXF			Receive input
	SENT0_SENT10C			Receive input channel 10
	P10.1	O0		General-purpose output
	GTM_TOUT103	O1		GTM muxed output

(table continues...)

Table 34 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI1_MTSR_F	O2		Master SPI data output
	QSPI1_MRST_F	O3		Slave SPI data output
	MSC0_EN1	O4		Chip Select
	ADC_BFL1	O5		Boundary flags from FCC
	ASCLIN0_ATX	O6		Transmit output
	—	O7		Reserved
	QSPI7_SLSO1	O8		Master slave select output
	EGTM_TOUT103	O9		eGTM muxed output
	LETH0_P2_TXD	O10		LETH PortX TC14 interface transmit data output
	—	O11		Reserved
	—	O12		Reserved
	ASCLIN2_ARTS_F	O13		Ready to send output
	LETH0_P2_MIID_TXEN	O14		LETH0 PortX MII transmit enable (to be used with LETH0_P2_TXCLKD)
	LETH0_P2_RMIID_TXEN	O15		LETH0 PortX RMII transmit enable (to be used with LETH0_P2_REFCLKD)
	LETH0_P2_RMIIRD_TXEN	PO		LETH0 PortX RMII transmit enable (to be used with LETH0_P2_REFCLKD - registered*)
A5	P10.2	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN2_3			Mux input channel 2 of TIM module 0
	GTM_TIM1_IN2_3			Mux input channel 2 of TIM module 1
	GTM_TIM4_IN5_13			Mux input channel 5 of TIM module 4
	CAN02_RXDE			CAN receive input node 2
	MSC0_SDI1			Upstream asynchronous input signal
	QSPI1_SCLKA_F			Slave SPI clock inputs
	GPT120_T6INB			Trigger/gate input of core timer T6
	SCU_E_REQ2A			ERU channel 2 input A
	GTM_CDTM0_DTM4_3			Input mux of CDTM0_DTM4_AUXIN0/1
	GTM_CDTM0_DTM5_3			Input mux of CDTM0_DTM5_AUXIN0/1
	GTM_CDTM2_DTM0_3			Input mux of CDTM2_DTM0_AUXIN0/1
	GTM_CDTM2_DTM1_3			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_CDTM0_DTM4_3			Input mux of CDTM0_DTM4_AUXIN0/1
	EGTM_CDTM0_DTM5_3			Input mux of CDTM0_DTM5_AUXIN0/1
	EGTM_CDTM2_DTM0_3			Input mux of CDTM2_DTM0_AUXIN0/1

(table continues...)

Table 34 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_CDTM2_DTM1_3			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_TIM0_IN2_3			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_3			Mux input channel 2 of TIM module 1
	LETH0_P2_MII_RXD2B			LETH0 PortX MII receive data bit 2 (to be used with LETH0_P2_RXCLKB)
	LETH1_P0_MDIOB			LETH PortX MDIO interface data input
	P10.2	O0		General-purpose output
	GTM_TOUT104	O1		GTM muxed output
	CAN32_TXD	O2		CAN transmit output node 2
	QSPI1_SCLK_F	O3		Master SPI clock output
	MSC0_EN0	O4		Chip Select
	ADC_BFL3	O5		Boundary flags from FCC
	ASCLIN2_ASCLK_F	O6		Shift clock output
	—	O7		Reserved
	QSPI7_SLSO2	O8		Master slave select output
	EGTM_TOUT104	O9		eGTM muxed output
	ASCLIN2_ATX_F	O10		Transmit output
	—	O11		Reserved
	QSPI2_SLSO1	O12		Master slave select output
	LETH0_P2_MIID_TXD0	O13		LETH0 PortX MII transmit data bit 0 (to be used with LETH0_P2_TXCLKD)
	—	O14		Reserved
	LETH0_P2_RMIID_TXD0	O15		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P2_REFCLKD)
	LETH0_P2_RMIIRD_TXD0	PO		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P2_REFCLKD - registered*)
	LETH1_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
A6	P10.3	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN3_3			Mux input channel 3 of TIM module 0
	GTM_TIM1_IN3_3			Mux input channel 3 of TIM module 1
	GTM_TIM4_IN6_10			Mux input channel 6 of TIM module 4
	QSPI1_MTSRA_F			Slave SPI data input
	SCU_E_REQ3A			ERU channel 3 input A

(table continues...)

Table 34 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GPT120_T5INB			Trigger/gate input of timer T5
	ASCLIN2_ARXH_F			Receive input
	MSC0_SDI5			Upstream asynchronous input signal
	GTM_CDTM2_DTM0_5			Input mux of CDTM2_DTM0_AUXIN0/1
	GTM_CDTM0_DTM1_2			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM0_DTM3_2			Input mux of CDTM0_DTM3_AUXIN0/1
	EGTM_CDTM0_DTM1_2			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM2_DTM0_5			Input mux of CDTM2_DTM0_AUXIN0/1
	EGTM_CDTM2_DTM2_5			Input mux of CDTM2_DTM2_AUXIN0/1
	EGTM_TIM0_IN3_3			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_3			Mux input channel 3 of TIM module 1
	EGTM_CDTM2_DTM3_3			Input mux of CDTM2_DTM3_AUXIN0/1
	LETH0_P2_MII_RXDVD			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	LETH0_P2_RMII_CRSDVD			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	P10.3	O0		General-purpose output
	GTM_TOUT105	O1		GTM muxed output
	CAN31_TXD	O2		CAN transmit output node 1
	QSPI1_MTSR_F	O3		Master SPI data output
	MSC0_EN0	O4		Chip Select
	ADC_BFL8	O5		Boundary flags from FCC
	CAN02_TXD	O6		CAN transmit output node 2
	ASCLIN2_ASLSO_F	O7		Slave select signal output
	QSPI7_SCLK	O8		Master SPI clock output
	EGTM_TOUT105	O9		eGTM muxed output
	ASCLIN2_ATX_F	O10		Transmit output
	—	O11		Reserved
	QSPI2_SLSO15	O12		Master slave select output
	ASCLIN1_ASLSO	O13		Slave select signal output
	ASCLIN3_ASLSO	O14		Slave select signal output
	—	O15		Reserved
B6	P10.4	I	FAST / PU1 /	General-purpose input

(table continues...)

Table 34 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TIM0_IN6_2		VDDEXT / ES	Mux input channel 6 of TIM module 0
	GTM_TIM1_IN6_2			Mux input channel 6 of TIM module 1
	GTM_TIM4_IN7_3			Mux input channel 7 of TIM module 4
	QSPI1_MTSRC_F			Slave SPI data input
	GPT120_T3INB			Trigger/gate input of core timer T3 (input A, B and C)
	CAN30_RXDA			CAN receive input node 0
	GTM_CDTM3_DTM4_5			Input mux of CDTM3_DTM4_AUXIN0/1
	GTM_CDTM4_DTM4_5			Input mux of CDTM4_DTM4_AUXIN0/1
	EGTM_CDTM2_DTM2_3			Input mux of CDTM2_DTM2_AUXIN0/1
	LETH0_P2_CRSB			LETH PortX MII carrier sense
	EGTM_CDTM2_DTM3_5			Input mux of CDTM2_DTM3_AUXIN0/1
	EGTM_TIM0_IN6_2			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN6_2			Mux input channel 6 of TIM module 1
	P10.4	O0		General-purpose output
	GTM_TOUT106	O1		GTM muxed output
	—	O2		Reserved
	QSPI1_SLSO8_F	O3		Master slave select output
	QSPI1_MTSR_F	O4		Master SPI data output
	MSC0_EN0	O5		Chip Select
	ADC_BFL9	O6		Boundary flags from FCC
	ASCLIN2_ASLSO_F	O7		Slave select signal output
	QSPI7_MTSR	O8		Master SPI data output
	EGTM_TOUT106	O9		eGTM muxed output
	GPT123_T3OUT	O10		External output for overflow/underflow detection of core timer T3
	—	O11		Reserved
	LETH0_P2_MIID_TXD1	O12		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P2_TXCLKD)
	LETH0_P2_MIID_TXD3	O13		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P2_TXCLKD)
	ASCLIN3_ASLSO	O14		Slave select signal output
	LETH0_P2_RMIID_TXD1	O15		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P2_REFCLKD)

(table continues...)

Table 34 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P2_RMIIRD_TXD1	PO		LETH0 PortX RMI transmit data bit 1 (to be used with LETH0_P2_REFCLKD - registered*)
B5	P10.5	I	FAST / PU2 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN2_4			Mux input channel 2 of TIM module 0
	GTM_TIM1_IN2_4			Mux input channel 2 of TIM module 1
	GTM_TIM4_IN3_14			Mux input channel 3 of TIM module 4
	QSPI1_MRSTE_F			Master SPI data input
	CAN20_RXDA			CAN receive input node 0
	MSC0_INJ1			Injection signal from port
	GTM_CDTM2_DTM4_5			Input mux of CDTM2_DTM4_AUXIN0/1
	GTM_CDTM3_DTM5_5			Input mux of CDTM3_DTM5_AUXIN0/1
	GTM_CDTM4_DTM5_5			Input mux of CDTM4_DTM5_AUXIN0/1
	GTM_CDTM5_DTM4_5			Input mux of CDTM5_DTM4_AUXIN0/1
	GTM_CDTM6_DTM4_5			Input mux of CDTM6_DTM4_AUXIN0/1
	EGTM_CDTM2_DTM4_5			Input mux of CDTM2_DTM4_AUXIN0/1
	QSPI5_MRSTE			Master SPI data input
	EGTM_TIM0_IN2_4			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_4			Mux input channel 2 of TIM module 1
	PMS_HWCFG4IN			HWCFG4 pin input
	P10.5	O0		General-purpose output
	GTM_TOUT107	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	QSPI3_SLSO8	O3		Master slave select output
	QSPI1_SLSO9	O4		Master slave select output
	GPT120_T6OUT	O5		External output for overflow/underflow detection of core timer T6
	—	O6		Reserved
	PSI5_TX3	O7		TXD outputs (send data)
	QSPI1_MRST	O8		Slave SPI data output
	EGTM_TOUT107	O9		eGTM muxed output
	QSPI5_MRST	O10		Slave SPI data output
	—	O11		Reserved
	LETH0_P2_MIID_TXEN	O12		LETH0 PortX MII transmit enable (to be used with LETH0_P2_TXCLKD)

(table continues...)

Table 34 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ERAY0_TXDB	O13		Transmit Channel B
	—	O14		Reserved
	LETH0_P2_RMIID_TXEN	O15		LETH0 PortX RMII transmit enable (to be used with LETH0_P2_REFCLKD)
	LETH0_P2_RMIIRD_TXEN	PO		LETH0 PortX RMII transmit enable (to be used with LETH0_P2_REFCLKD - registered*)
A4	P10.6	I	FAST / PU2 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN3_4			Mux input channel 3 of TIM module 0
	GTM_TIM1_IN3_4			Mux input channel 3 of TIM module 1
	GTM_TIM4_IN2_14			Mux input channel 2 of TIM module 4
	PSI5_RX3C			RXD inputs (receive data) channel 3
	ASCLIN2_ARXD_F			Receive input
	QSPI3_MTSRB			Slave SPI data input
	ASCLIN7_ARXH			Receive input
	SENT1_SENT12B			Receive input channel 12
	GTM_CDTM2_DTM5_5			Input mux of CDTM2_DTM5_AUXIN0/1
	GTM_CDTM5_DTM5_5			Input mux of CDTM5_DTM5_AUXIN0/1
	GTM_CDTM6_DTM5_5			Input mux of CDTM6_DTM5_AUXIN0/1
	EGTM_CDTM2_DTM5_5			Input mux of CDTM2_DTM5_AUXIN0/1
	QSPI1_MRSTC_F			Master SPI data input
	EGTM_TIM0_IN3_4			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_4			Mux input channel 3 of TIM module 1
	PMS_HWCFG5IN			HWCFG5 pin input
	P10.6	O0		General-purpose output
	GTM_TOUT108	O1		GTM muxed output
	ASCLIN2_ASCLK_F	O2		Shift clock output
	QSPI3_MTSR	O3		Master SPI data output
	GPT120_T3OUT	O4		External output for overflow/underflow detection of core timer T3
	CAN20_TXD	O5		CAN transmit output node 0
	QSPI1_MRST_F	O6		Slave SPI data output
	—	O7		Reserved
	SENT1_SPC12	O8		Transmit output
	EGTM_TOUT108	O9		eGTM muxed output

(table continues...)

Table 34 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI5_MTSR	O10		Master SPI data output
	LETH0_P2_MIID_TXD2	O11		LETH0 PortX MII transmit data bit 2 (to be used with LETH0_P2_TXCLKD)
	QSPI2_SLSO14	O12		Master slave select output
	CAN13_TXD	O13		CAN transmit output node 3
	ERAY0_TXENB	O14		Transmit Enable Channel B
	—	O15		Reserved
A3	P10.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN0_3			Mux input channel 0 of TIM module 0
	GTM_TIM1_IN0_3			Mux input channel 0 of TIM module 1
	GPT120_T3EUDB			Count direction control input of core timer T3
	ASCLIN2_ACTSA_F			Clear to send input
	QSPI3_MRSTB			Master SPI data input
	SCU_E_REQ0B			ERU channel 0 input B
	CAN10_RXDH			CAN receive input node 0
	CAN13_RXDH			CAN receive input node 3
	CANXL00_RXDE			CANXL receive input node 0
	QSPI7_MTSRD			Slave SPI data input
	EGTM_TIM0_IN0_3			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_3			Mux input channel 0 of TIM module 1
	LETH0_P2_REFCLKB			LETH PortX RMII reference clock
	LETH0_P2_RXCLKB			LETH PortX MII receive clock
	LETH0_P2_REFCLKD			LETH0 PortX RMII reference clock
	LETH0_P2_RXCLKD			LETH PortX MII receive clock
	P10.7	O0		General-purpose output
	GTM_TOUT109	O1		GTM muxed output
	—	O2		Reserved
	QSPI3_MRST	O3		Slave SPI data output
	—	O4		Reserved
	CAN20_TXD	O5		CAN transmit output node 0
	CAN12_TXD	O6		CAN transmit output node 2
	QSPI7_SCLK	O7		Master SPI clock output
	QSPI7_MRST	O8		Slave SPI data output

(table continues...)

Table 34 (continued) Port 10 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TOUT109	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	ASCLIN0_ARTS	O12		Ready to send output
	QSPI2_SLSO13	O13		Master slave select output
	—	O14		Reserved
	—	O15		Reserved
	—	—		—
B4	P10.8	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN5_2			Mux input channel 5 of TIM module 0
	GTM_TIM1_IN5_2			Mux input channel 5 of TIM module 1
	GTM_TIM4_IN0_14			Mux input channel 0 of TIM module 4
	CAN12_RXDB			CAN receive input node 2
	GPT120_T4INB			Trigger/gate input of timer T4
	QSPI3_SCLKB			Slave SPI clock inputs
	SCU_E_REQ1B			ERU channel 1 input B
	QSPI1_SLSIC_F			Slave select input
	CAN20_RXDB			CAN receive input node 0
	SENT1_SENT14A			Receive input channel 14
	CAN02_RXDG			CAN receive input node 2
	QSPI7_MRSTG			Master SPI data input
	EGTM_TIM0_IN5_2			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_2			Mux input channel 5 of TIM module 1
	LETH0_P2_MII_RMII_RXD 1B			LETH0 PortX MII and RMII receive data bit 1 (to be used with LETH0_P2_RXCLKB or LETH0_P2_REFCLKB)
	LETH0_P2_MII_RMII_RXD 1D			LETH0 PortX MII and RMII receive data bit 1 (to be used with LETH0_P2_RXCLKD or LETH0_P2_REFCLKD)
	P10.8	O0		General-purpose output
	GTM_TOUT110	O1		GTM muxed output
	ASCLIN2_ARTS	O2		Ready to send output
	QSPI3_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	ASCLIN5_ASLSO	O5		Slave select signal output
	ASCLIN7_ASLSO	O6		Slave select signal output
	—	—		—
	—	—		—
	—	—		—
	—	—		—

(table continues...)

Table 34 (continued) **Port 10 functions**

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O7		Reserved
	QSPI1_SLSO11	O8		Master slave select output
	EGTM_TOUT110	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

3.3.5 BGA292_STD port 11

Table 35 **Port 11 functions**

Ball	Symbol	Ctrl.	Buffer type	Function
E10	P11.0	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM2_IN0_7			Mux input channel 0 of TIM module 2
	GTM_TIM4_IN0_4			Mux input channel 0 of TIM module 4
	ASCLIN3_ARXB			Receive input
	GTM_CDTM2_DTM4_2			Input mux of CDTM2_DTM4_AUXIN0/1
	GTM_CDTM2_DTM5_2			Input mux of CDTM2_DTM5_AUXIN0/1
	EGTM_CDTM2_DTM4_2			Input mux of CDTM2_DTM4_AUXIN0/1
	EGTM_CDTM2_DTM5_2			Input mux of CDTM2_DTM5_AUXIN0/1
	XSPI0_RXD3C			Receive data
	EGTM_TIM2_IN0_7			Mux input channel 0 of TIM module 2
	P11.0	O0		General-purpose output
	GTM_TOUT119	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	CAN11_TXD	O5		CAN transmit output node 1
	LETH0_P0_MIIA_TXD3	O6		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P0_TXCLKA)
	—	O7		Reserved

(table continues...)

Table 35 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O8		Reserved
	EGTM_TOUT119	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	LETH1_P0_MIIA_TXD3	O13		LETH1 PortX MII transmit data bit 3 (to be used with LETH1_P0_TXCLKA)
	—	O14		Reserved
	—	O15		Reserved
	XSPIO_TXDC3	O		Transmit data
E9	P11.1	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM2_IN1_6			Mux input channel 1 of TIM module 2
	GTM_TIM4_IN1_5			Mux input channel 1 of TIM module 4
	XSPIO_RXD2C			Receive data
	EGTM_TIM2_IN1_6			Mux input channel 1 of TIM module 2
	P11.1	O0		General-purpose output
	GTM_TOUT120	O1		GTM muxed output
	ASCLIN3_ASCLK	O2		Shift clock output
	ASCLIN3_ATX	O3		Transmit output
	—	O4		Reserved
	CAN12_TXD	O5		CAN transmit output node 2
	LETH0_P0_MIIA_TXD2	O6		LETH0 PortX MII transmit data bit 2 (to be used with LETH0_P0_TXCLKA)
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT120	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	LETH1_P0_MIIA_TXD2	O13		LETH1 PortX MII transmit data bit 2 (to be used with LETH1_P0_TXCLKA)
	—	O14		Reserved
	—	O15		Reserved
	XSPIO_TXDC2	O		Transmit data

(table continues...)

Table 35 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
A10	P11.2	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM2_IN1_3			Mux input channel 1 of TIM module 2
	GTM_TIM3_IN1_3			Mux input channel 1 of TIM module 3
	GPT121_T3INB			Trigger/gate input of core timer T3 (input A, B and C)
	EGTM_TIM2_IN1_3			Mux input channel 1 of TIM module 2
	P11.2	O0		General-purpose output
	GTM_TOUT95	O1		GTM muxed output
	ASCLIN0_ASLSO	O2		Slave select signal output
	QSPI0_SLSO5	O3		Master slave select output
	QSPI1_SLSO5	O4		Master slave select output
	MSC0_EN1	O5		Chip Select
	LETH0_P0_MIIA_TXD1	O6		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P0_TXCLKA)
	LETH0_P0_RMIIA_TXD1	O7		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P0_REFCLKA)
	—	O8		Reserved
	EGTM_TOUT95	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	LETH1_P0_MIIA_TXD1	O13		LETH1 PortX MII transmit data bit 1 (to be used with LETH1_P0_TXCLKA)
	LETH1_P0_RMIIA_TXD1	O14		LETH1 PortX RMII transmit data bit 1 (to be used with LETH1_P0_REFCLKA)
	CAN13_TXD	O15		CAN transmit output node 3
	LETH0_P0_RMIIRA_TXD1	PO		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P0_REFCLKA - registered*)
	LETH1_P0_RMIIRA_TXD1	PO		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P0_REFCLKA - registered*)
B10	P11.3	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM2_IN2_2			Mux input channel 2 of TIM module 2
	GTM_TIM3_IN2_2			Mux input channel 2 of TIM module 3
	MSC0_SDI3			Upstream asynchronous input signal
	QSPI1_MRSTB			Master SPI data input
	CAN31_RXDD			CAN receive input node 1

(table continues...)

Table 35 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GPT121_T3EUDB			Count direction control input of core timer T3
	EGTM_TIM2_IN2_2			Mux input channel 2 of TIM module 2
	P11.3	O0		General-purpose output
	GTM_TOUT96	O1		GTM muxed output
	LETH0_P0_TXD	O2		LETH PortX TC14 interface transmit data output
	QSPI1_MRST	O3		Slave SPI data output
	ERAY0_TXDA	O4		Transmit Channel A
	CANXL00_TXD	O5		CANXL transmit output node 0
	LETH0_P0_MIIA_TXD0	O6		LETH0 PortX MII transmit data bit 0 (to be used with LETH0_P0_TXCLKA)
	LETH0_P0_RMIIA_TXD0	O7		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P0_REFCLKA)
	—	O8		Reserved
	EGTM_TOUT96	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	LETH1_P0_MIIA_TXD0	O13		LETH1 PortX MII transmit data bit 0 (to be used with LETH1_P0_TXCLKA)
	LETH1_P0_RMIIA_TXD0	O14		LETH1 PortX RMII transmit data bit 0 (to be used with LETH1_P0_REFCLKA)
	LETH1_P0_TXD	O15		LETH PortX TC14 interface transmit data output
	LETH0_P0_RMIIRA_TXD0	PO		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P0_REFCLKA - registered*)
	LETH1_P0_RMIIRA_TXD0	PO		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P0_REFCLKA - registered*)
D10	P11.4	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM2_IN2_6			Mux input channel 2 of TIM module 2
	GTM_TIM4_IN2_5			Mux input channel 2 of TIM module 4
	EGTM_TIM2_IN2_6			Mux input channel 2 of TIM module 2
	P11.4	O0		General-purpose output
	GTM_TOUT121	O1		GTM muxed output
	ASCLIN3_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved

(table continues...)

Table 35 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CAN13_TXD	O5		CAN transmit output node 3
	LETH0_P0_MIIA_TXER	O6		LETH0 PortX MII transmit error (to be used with LETH0_P0_TXCLKA)
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT121	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	LETH1_P0_MIIA_TXER	O13		LETH1 PortX MII transmit error (to be used with LETH1_P0_TXCLKA)
	—	O14		Reserved
	XSPI0_CLKC	O15		Clock output
D8	P11.5	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM2_IN3_8			Mux input channel 3 of TIM module 2
	GTM_TIM4_IN3_5			Mux input channel 3 of TIM module 4
	XSPI0_RXD1C			Receive data
	EGTM_TIM2_IN3_8			Mux input channel 3 of TIM module 2
	LETH0_P0_TXCLKA			LETH PortX MII transmit clock
	LETH1_P0_TXCLKA			LETH PortX MII transmit clock
	P11.5	O0		General-purpose output
	GTM_TOUT122	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	CAN20_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT122	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved

(table continues...)

Table 35 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPIO_TXDC1	O		Transmit data
D9	P11.6	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM2_IN3_2			Mux input channel 3 of TIM module 2
	GTM_TIM3_IN3_2			Mux input channel 3 of TIM module 3
	QSPI1_SCLKB			Slave SPI clock inputs
	GPT121_T4INB			Trigger/gate input of timer T4
	LETH0_P1_EDD			LETH PortX TC14 interface energy detection input
	LETH0_P1_MDIOD			LETH PortX MDIO interface data input
	EGTM_TIM2_IN3_2			Mux input channel 3 of TIM module 2
	P11.6	O0		General-purpose output
	GTM_TOUT97	O1		GTM muxed output
	ERAY0_TXENB	O2		Transmit Enable Channel B
	QSPI1_SCLK	O3		Master SPI clock output
	ERAY0_TXENA	O4		Transmit Enable Channel A
	MSC0_FCLP	O5		Shift-clock direct part of the differential signal
	LETH0_P0_MIIA_TXEN	O6		LETH0 PortX MII transmit enable (to be used with LETH0_P0_TXCLKA)
	LETH0_P0_RMIIA_TXEN	O7		LETH0 PortX RMII transmit enable (to be used with LETH0_P0_REFCLKA)
	—	O8		Reserved
	EGTM_TOUT97	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	LETH1_P0_MIIA_TXEN	O13		LETH1 PortX MII transmit enable (to be used with LETH1_P0_TXCLKA)
	LETH1_P0_RMIIA_TXEN	O14		LETH1 PortX RMII transmit enable (to be used with LETH1_P0_REFCLKA)
	CAN00_TXD	O15		CAN transmit output node 0
	LETH0_P0_RMIIRA_TXEN	PO		LETH0 PortX RMII transmit enable (to be used with LETH0_P0_REFCLKA - registered*)

(table continues...)

Table 35 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH1_P0_RMIIRA_TXEN	PO		LETH0 PortX RMII transmit enable (to be used with LETH0_P0_REFCLKA - registered*)
	LETH0_P1_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
E8	P11.7	I	SLOW / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM2_IN4_7			Mux input channel 4 of TIM module 2
	GTM_TIM4_IN4_5			Mux input channel 4 of TIM module 4
	CAN11_RXDD			CAN receive input node 1
	XSPIO_RXD0C			Receive data
	EGTM_TIM2_IN4_7			Mux input channel 4 of TIM module 2
	LETH0_P0_MII_RXD3A			LETH0 PortX MII receive data bit 3 (to be used with LETH0_P0_RXCLKA)
	LETH1_P0_MII_RXD3A			LETH1 PortX MII receive data bit 3 (to be used with LETH1_P0_RXCLKA)
	P11.7	O0		General-purpose output
	GTM_TOUT123	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT123	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPIO_TXDC0	O		Transmit data
E7	P11.8	I	SLOW / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM2_IN5_8			Mux input channel 5 of TIM module 2
	GTM_TIM4_IN5_5			Mux input channel 5 of TIM module 4

(table continues...)

Table 35 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CAN12_RXDD			CAN receive input node 2
	GPT121_T5INB			Trigger/gate input of timer T5
	EGTM_TIM2_IN5_8			Mux input channel 5 of TIM module 2
	LETH0_P0_MII_RXD2A			LETH0 PortX MII receive data bit 2 (to be used with LETH0_P0_RXCLKA)
	LETH1_P0_MII_RXD2A			LETH1 PortX MII receive data bit 2 (to be used with LETH1_P0_RXCLKA)
	P11.8	O0		General-purpose output
	GTM_TOUT124	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT124	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	XSPI0_CSC1_N	O15		Chip select
A9	P11.9	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM2_IN4_2			Mux input channel 4 of TIM module 2
	GTM_TIM3_IN4_2			Mux input channel 4 of TIM module 3
	QSPI1_MTSRB			Slave SPI data input
	ERAY0_RXDA1			Receive Channel A1
	GPT121_T5EUDB			Count direction control input of timer T5
	CANXL00_RXDD			CANXL receive input node 0
	EGTM_TIM2_IN4_2			Mux input channel 4 of TIM module 2
	LETH0_P0_MII_RMII_RXD1A			LETH0 PortX MII and RMII receive data bit 1 (to be used with LETH0_P0_RXCLKA or LETH0_P0_REFCLKA)

(table continues...)

Table 35 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH1_P0_MII_RMII_RXD1A			LETH1 PortX MII and RMII receive data bit 1 (to be used with LETH1_P0_RXCLKA or LETH1_P0_REFCLKA)
	LETH0_P0_RXDD			LETH PortX TC14 interface receive data input
	P11.9	O0		General-purpose output
	GTM_TOUT98	O1		GTM muxed output
	—	O2		Reserved
	QSPI1_MTSR	O3		Master SPI data output
	—	O4		Reserved
	MSC0_SOP	O5		Data output - direct part of the differential signal
	GPT121_T3OUT	O6		External output for overflow/underflow detection of core timer T3
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT98	O9		eGTM muxed output
	—	O10		Reserved
	LETH1_P0_MDC	O11		LETH PortX MDIO interface clock output
	—	O12		Reserved
	—	O13		Reserved
	LETH0_P1_MDC	O14		LETH PortX MDIO interface clock output
	—	O15		Reserved
	LETH0_P0_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
B9	P11.10	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM2_IN0_9			Mux input channel 0 of TIM module 2
	GTM_TIM2_IN5_2			Mux input channel 5 of TIM module 2
	GTM_TIM3_IN5_2			Mux input channel 5 of TIM module 3
	CAN03_RXDD			CAN receive input node 3
	ERAY0_RXDB1			Receive Channel B1
	ASCLIN1_ARXE			Receive input
	SCU_E_REQ6B			ERU channel 6 input B
	MSC0_SDI0			Upstream asynchronous input signal
	QSPI1_SLSIA			Slave select input
	GPT121_T2INB			Trigger/gate input of timer T2
	CANXL01_RXDB			CANXL receive input node 1

(table continues...)

Table 35 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM2_IN0_9			Mux input channel 0 of TIM module 2
	EGTM_TIM2_IN5_2			Mux input channel 5 of TIM module 2
	LETH0_P0_MII_RMII_RXD 0A			LETH0 PortX MII and RMII receive data bit 0 (to be used with LETH0_P0_RXCLKA or LETH0_P0_REFCLKA)
	LETH1_P0_MII_RMII_RXD 0A			LETH1 PortX MII and RMII receive data bit 0 (to be used with LETH1_P0_RXCLKA or LETH1_P0_REFCLKA)
	LETH1_P0_RXDD			LETH PortX TC14 interface receive data input
	P11.10	O0		General-purpose output
	GTM_TOUT99	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO3	O3		Master slave select output
	QSPI1_SLSO3	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT99	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	LETH0_P1_MDC	O14		LETH PortX MDIO interface clock output
	—	O15		Reserved
	LETH1_P0_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
A8	P11.11	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM2_IN6_2			Mux input channel 6 of TIM module 2
	GTM_TIM3_IN0_15			Mux input channel 0 of TIM module 3
	GTM_TIM3_IN6_2			Mux input channel 6 of TIM module 3
	LETH0_P1_MDIOA			LETH PortX MDIO interface data input
	GPT121_T2EUDB			Count direction control input of timer T2
	LETH0_P1_EDA			LETH PortX TC14 interface energy detection input
	EGTM_TIM2_IN6_2			Mux input channel 6 of TIM module 2
	LETH0_P0_CRSA			LETH PortX MII carrier sense

(table continues...)

Table 35 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH1_P0_CRSA			LETH PortX MII carrier sense
	P11.11	O0		General-purpose output
	GTM_TOUT100	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO4	O3		Master slave select output
	QSPI1_SLSO4	O4		Master slave select output
	MSC0_EN0	O5		Chip Select
	ERAY0_TXENB	O6		Transmit Enable Channel B
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT100	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
B8	P11.12	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM2_IN7_2			Mux input channel 7 of TIM module 2
	GTM_TIM3_IN7_2			Mux input channel 7 of TIM module 3
	GPT121_T4EUDB			Count direction control input of timer T4
	EGTM_TIM2_IN7_2			Mux input channel 7 of TIM module 2
	LETH0_P0_REFCLKA			LETH0 PortX RMII reference clock
	LETH0_P0_RXCLKA			LETH PortX MII receive clock
	LETH1_P0_REFCLKA			LETH PortX RMII reference clock
	LETH1_P0_RXCLKA			LETH PortX MII receive clock
	P11.12	O0		General-purpose output
	GTM_TOUT101	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	GTM_ECLK2	O3		CGM generated clock
	ERAY0_TXDB	O4		Transmit Channel B

(table continues...)

Table 35 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CAN03_TXD	O5		CAN transmit output node 3
	CLOCK_EXTCLK1	O6		External clock output 1
	—	O7		Reserved
	EGTM_ECLK2	O8		CGM generated clock
	EGTM_TOUT101	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P1_TXD	O11		LETH PortX TC14 interface transmit data output
	CANXL01_TXD	O12		CANXL transmit output node 1
	LETH1_P0_TXD	O13		LETH PortX TC14 interface transmit data output
	—	O14		Reserved
	—	O15		Reserved
E6	P11.13	I	SLOW / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM2_IN6_7			Mux input channel 6 of TIM module 2
	GTM_TIM4_IN6_5			Mux input channel 6 of TIM module 4
	I2C1_SDAA			Serial Data Input 0
	CAN13_RXDD			CAN receive input node 3
	CAN31_RXDA			CAN receive input node 1
	LETH0_P0_MII_RXERA			LETH0 PortX MII receive error (to be used with LETH0_P0_RXCLKA)
	LETH1_P0_MII_RXERA			LETH1 PortX MII receive error (to be used with LETH1_P0_RXCLKA)
	EGTM_TIM2_IN6_7			Mux input channel 6 of TIM module 2
	LETH1_P0_RXDA			LETH PortX TC14 interface receive data input
	P11.13	O0		General-purpose output
	GTM_TOUT125	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	I2C1_SDA	O6		Serial Data Output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT125	O9		eGTM muxed output

(table continues...)

Table 35 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O10		Reserved
	LETH1_P0_MDC	O11		LETH PortX MDIO interface clock output
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH1_P0_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
D7	P11.14	I	SLOW / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM2_IN7_8			Mux input channel 7 of TIM module 2
	GTM_TIM4_IN7_4			Mux input channel 7 of TIM module 4
	I2C1_SCLA			Serial Clock Input 0
	CAN20_RXDF			CAN receive input node 0
	LETH0_P0_CRSB			LETH PortX MII carrier sense
	LETH1_P0_CRSB			LETH PortX MII carrier sense
	EGTM_TIM2_IN7_8			Mux input channel 7 of TIM module 2
	LETH0_P0_MII_RXDVA			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	LETH1_P0_MII_RXDVA			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	LETH0_P0_RMII_CRSDVA			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	LETH1_P0_RMII_CRSDVA			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	P11.14	O0		General-purpose output
	GTM_TOUT126	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	I2C1_SCL	O6		Serial Clock Output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT126	O9		eGTM muxed output

(table continues...)

Table 35 (continued) Port 11 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	—	O15		Reserved
D6	P11.15	I	SLOW / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM0_IN7_8			Mux input channel 7 of TIM module 0
	GTM_TIM4_IN7_5			Mux input channel 7 of TIM module 4
	LETH1_P0_EDE			LETH PortX TC14 interface energy detection input
	LETH1_P0_MDIOE			LETH PortX MDIO interface data input
	LETH0_P0_COLA			LETH PortX MII collision detection
	LETH1_P0_COLA			LETH PortX MII collision detection
	EGTM_TIM0_IN7_8			Mux input channel 7 of TIM module 0
	P11.15	O0		General-purpose output
	GTM_TOUT127	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT127	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH1_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface

3.3.6 BGA292_STD port 12

Table 36 Port 12 functions

Ball	Symbol	Ctrl.	Buffer type	Function
E12	P12.0	I	SLOW / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM3_IN0_7			Mux input channel 0 of TIM module 3
	GTM_TIM4_IN0_5			Mux input channel 0 of TIM module 4
	CAN00_RXDC			CAN receive input node 0
	LETH1_P0_EDA			LETH PortX TC14 interface energy detection input
	LETH1_P0_MDIOA			LETH PortX MDIO interface data input
	GTM_CDTM4_DTM4_1			Input mux of CDTM4_DTM4_AUXIN0/1
	GTM_CDTM4_DTM5_1			Input mux of CDTM4_DTM5_AUXIN0/1
	LETH1_P0_REFCLKC			LETH PortX RMII reference clock
	LETH1_P0_RXCLKC			LETH PortX MII receive clock
	P12.0	O0		General-purpose output
	GTM_TOUT128	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT128	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P0_MDC	O11		LETH PortX MDIO interface clock output
	LETH1_P0_MDC	O12		LETH PortX MDIO interface clock output
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH1_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
E11	P12.1	I	FAST / PU1 / VDDFLEX / ES	General-purpose input
	GTM_TIM3_IN1_6			Mux input channel 1 of TIM module 3
	GTM_TIM4_IN1_6			Mux input channel 1 of TIM module 4
	LETH0_P0_MDIOE			LETH PortX MDIO interface data input

(table continues...)

Table 36 (continued) Port 12 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P0_EDE			LETH PortX TC14 interface energy detection input
	P12.1	O0		General-purpose output
	GTM_TOUT129	O1		GTM muxed output
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	CAN00_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT129	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface

3.3.7 BGA292_STD port 13

Table 37 Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
B12	P13.0	I	LVDS_TX / FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM2_IN5_3			Mux input channel 5 of TIM module 2
	GTM_TIM3_IN5_3			Mux input channel 5 of TIM module 3
	QSPI2_MRSTG_F			Master SPI data input
	GPT121_T6INB			Trigger/gate input of core timer T6
	CAN11_RXDG			CAN receive input node 1
	EGTM_TIM2_IN5_3			Mux input channel 5 of TIM module 2
	P13.0	O0		General-purpose output
	GTM_TOUT91	O1		GTM muxed output

(table continues...)

Table 37 (continued) Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O2		Reserved
	QSPI2_SCLKN_F	O3		Master SPI clock output (LVDS N line)
	MSC0_EN1	O4		Chip Select
	MSC0_FCLN	O5		Shift-clock inverted part of the differential signal
	—	O6		Reserved
	CAN10_TXD	O7		CAN transmit output node 0
	—	O8		Reserved
	EGTM_TOUT91	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P2_MIIC_TXD2	O12		LETH0 PortX MII transmit data bit 2 (to be used with LETH0_P2_TXCLKC)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
A12	P13.1	I	LVDS_TX / FAST / PU1 / VDDEXT HS / ES	General-purpose input
	GTM_TIM2_IN6_3			Mux input channel 6 of TIM module 2
	GTM_TIM3_IN6_3			Mux input channel 6 of TIM module 3
	I2C0_SCLB			Serial Clock Input 1
	CAN10_RXDD			CAN receive input node 0
	LETH1_P0_MDIOC			LETH PortX MDIO interface data input
	LETH1_P0_EDC			LETH PortX TC14 interface energy detection input
	QSPI2_SCLKC_F			Slave SPI clock inputs
	LETH0_P2_COLC			LETH PortX MII collision detection
	EGTM_TIM2_IN6_3			Mux input channel 6 of TIM module 2
	P13.1	O0		General-purpose output
	GTM_TOUT92	O1		GTM muxed output
	—	O2		Reserved
	QSPI2_SCLKP_F	O3		Master SPI clock output
	—	O4		Reserved
	MSC0_FCLP	O5		Shift-clock direct part of the differential signal
	I2C0_SCL	O6		Serial Clock Output

(table continues...)

Table 37 (continued) Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GPT121_T6OUT	O7		External output for overflow/underflow detection of core timer T6
	QSPI2_SCLK_F	O8		Master SPI clock output
	EGTM_TOUT92	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH1_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
B11	P13.2	I	LVDS_TX / FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM2_IN7_3			Mux input channel 7 of TIM module 2
	GTM_TIM3_IN7_3			Mux input channel 7 of TIM module 3
	GPT120_CAPINA			Trigger input to capture value of timer T5 into CAPREL register (input A)
	I2C0_SDAB			Serial Data Input 1
	CAN33_RXDA			CAN receive input node 3
	LETH1_P0_COLB			LETH PortX MII collision detection
	GPT121_T6EUDB			Count direction control input of core timer T6
	LETH0_P2_CRSC			LETH PortX MII carrier sense
	EGTM_TIM2_IN7_3			Mux input channel 7 of TIM module 2
	P13.2	O0		General-purpose output
	GTM_TOUT93	O1		GTM muxed output
	—	O2		Reserved
	QSPI2_MTSRN_F	O3		Master SPI data output (LVDS N line)
	MSC0_FCLP	O4		Shift-clock direct part of the differential signal
	MSC0_SON	O5		Data output - inverted part of the differential signal
	I2C0_SDA	O6		Serial Data Output
	—	O7		Reserved
	QSPI2_MTSR_F	O8		Master SPI data output
	EGTM_TOUT93	O9		eGTM muxed output
	QSPI2_MRST_F	O10		Slave SPI data output

(table continues...)

Table 37 (continued) Port 13 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O11		Reserved
	—	O12		Reserved
	LETH1_P0_TXD	O13		LETH PortX TC14 interface transmit data output
	—	O14		Reserved
	—	O15		Reserved
A11	P13.3	I	LVDS_TX / FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM2_IN0_3			Mux input channel 0 of TIM module 2
	GTM_TIM3_IN0_3			Mux input channel 0 of TIM module 3
	QSPI2_SLSIC_F			Slave select input
	EGTM_TIM2_IN0_3			Mux input channel 0 of TIM module 2
	LETH1_P0_RXDC			LETH PortX TC14 interface receive data input
	P13.3	O0		General-purpose output
	GTM_TOUT94	O1		GTM muxed output
	—	O2		Reserved
	QSPI2_MTSRP_F	O3		Master SPI data output
	ASCLIN7_ASLSO_F	O4		Slave select signal output
	MSC0_SOP	O5		Data output - direct part of the differential signal
	—	O6		Reserved
	CAN33_TXD	O7		CAN transmit output node 3
	QSPI2_SLSO3_F	O8		Master slave select output
	EGTM_TOUT94	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P2_MIIA_TXD3	O12		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P2_TXCLKA)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH1_P0_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface

3.3.8 BGA292_STD port 14

Table 38 Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
B16	P14.0	I	FAST / PU1 / VDDEXTHS / ES2	General-purpose input
	GTM_TIM0_IN3_5			Mux input channel 3 of TIM module 0
	GTM_TIM1_IN3_5			Mux input channel 3 of TIM module 1
	SENT1_SENT8D			Receive input channel 8
	LETH0_P2_EDH			LETH PortX TC14 interface energy detection input
	LETH0_P2_MDIOH			LETH PortX MDIO interface data input
	EGTM_TIM0_IN3_5			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_5			Mux input channel 3 of TIM module 1
	LETH0_P2_REFCLKA			LETH0 PortX RMII reference clock
	LETH0_P2_RXCLKA			LETH PortX MII receive clock
	LETH0_P2_REFCLKC			LETH PortX RMII reference clock
	LETH0_P2_RXCLKC			LETH PortX MII receive clock
	P14.0	O0		General-purpose output
	GTM_TOUT80	O1		GTM muxed output
	ASCLIN0_ATX_F	O2		Transmit output
	ERAY0_TXDA	O3		Transmit Channel A
	ERAY0_TXDB	O4		Transmit Channel B
	CAN01_TXD	O5		CAN transmit output node 1
	ASCLIN0_ASCLK_F	O6		Shift clock output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT80	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P0_TXD	O12		LETH PortX TC14 interface transmit data output
	CANXL00_TXD	O13		CANXL transmit output node 0
	LETH0_P1_TXD	O14		LETH PortX TC14 interface transmit data output
	CANXL01_TXD	O15		CANXL transmit output node 1
	EGTM_HRPWM1_CH0	PO		High resolution PWM 1 output channels
	LETH0_P2_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface

(table continues...)

Table 38 (continued) **Port 14 functions**

Ball	Symbol	Ctrl.	Buffer type	Function
A15	P14.1	I	FAST / PU1 / VDDEXTH S / ES2	General-purpose input
	GTM_TIM0_IN4_3			Mux input channel 4 of TIM module 0
	GTM_TIM1_IN4_3			Mux input channel 4 of TIM module 1
	ERAY0_RXDA3			Receive Channel A3
	ASCLIN0_ARXA_F			Receive input
	SENT0_SENT9D			Receive input channel 9
	ERAY0_RXDB3			Receive Channel B3
	CAN01_RXDB			CAN receive input node 1
	SCU_E_REQ3B			ERU channel 3 input B
	CANXL00_RXDB			CANXL receive input node 0
	EGTM_TIM0_IN4_3			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_3			Mux input channel 4 of TIM module 1
	PMS_PINAWKP			PINA (P14.1) pin input
	LETH0_P2_MII_RMII_RXD 0A			LETH0 PortX MII and RMII receive data bit 0 (to be used with LETH0_P2_RXCLKA or LETH0_P2_REFCLKA)
	LETH0_P2_MII_RMII_RXD 0C			LETH0 PortX MII and RMII receive data bit 0 (to be used with LETH0_P2_RXCLKC or LETH0_P2_REFCLKC)
	LETH0_P0_RXDB			LETH PortX TC14 interface receive data input
	P14.1	O0		General-purpose output
	GTM_TOUT81	O1		GTM muxed output
	ASCLIN0_ATX_F	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT81	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved

(table continues...)

Table 38 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O15		Reserved
	EGTM_HRPWM1_CH1	PO		High resolution PWM 1 output channels
	LETH0_P0_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
E13	P14.2	I	SLOW / PU2 / VDDEXTH S / ES	General-purpose input
	GTM_TIM0_IN5_3			Mux input channel 5 of TIM module 0
	GTM_TIM1_IN5_3			Mux input channel 5 of TIM module 1
	CANXL01_RXDD			CANXL receive input node 1
	LETH0_P2_MII_RXERA			LETH0 PortX MII receive error (to be used with LETH0_P2_RXCLKA)
	LETH0_P2_MII_RXERC			LETH0 PortX MII receive error (to be used with LETH0_P2_RXCLKC)
	EGTM_TIM0_IN5_3			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_3			Mux input channel 5 of TIM module 1
	PMS_HWCFG2IN			HWCFG2 pin input
	LETH0_P1_RXDD			LETH PortX TC14 interface receive data input
	P14.2	O0		General-purpose output
	GTM_TOUT82	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	QSPI2_SLSO1	O3		Master slave select output
	—	O4		Reserved
	ASCLIN0_ASLSO	O5		Slave select signal output
	ASCLIN2_ASCLK	O6		Shift clock output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT82	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	LETH0_P0_PPS	O13		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 38 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
B14	P14.3	I	SLOW / PU2 / VDDEXTH S / ES	General-purpose input
	GTM_TIM0_IN6_3			Mux input channel 6 of TIM module 0
	GTM_TIM1_IN6_3			Mux input channel 6 of TIM module 1
	ASCLIN2_ARXA			Receive input
	MSC0_SDI2			Upstream asynchronous input signal
	SCU_E_REQ1A			ERU channel 1 input A
	LETH0_P1_EDB			LETH PortX TC14 interface energy detection input
	LETH0_P1_MDIOB			LETH PortX MDIO interface data input
	EGTM_TIM0_IN6_3			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN6_3			Mux input channel 6 of TIM module 1
	PMS_HWCFG3IN			HWCFG3 pin input
	LETH0_P2_MII_RMII_RXD1A			LETH0 PortX MII and RMII receive data bit 1 (to be used with LETH0_P2_RXCLKA or LETH0_P2_REFCLKA)
	LETH0_P2_MII_RMII_RXD1C			LETH0 PortX MII and RMII receive data bit 1 (to be used with LETH0_P2_RXCLKC or LETH0_P2_REFCLKC)
	P14.3	O0		General-purpose output
	GTM_TOUT83	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	QSPI2_SLSO3	O3		Master slave select output
	ASCLIN1_ASLSO	O4		Slave select signal output
	ASCLIN3_ASLSO	O5		Slave select signal output
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT83	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P1_TXD	O12		LETH PortX TC14 interface transmit data output
	CANXL01_TXD	O13		CANXL transmit output node 1
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 38 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
B15	P14.4	I	SLOW / PU2 / VDDEXT S / ES	General-purpose input
	GTM_TIM0_IN7_2			Mux input channel 7 of TIM module 0
	GTM_TIM1_IN7_2			Mux input channel 7 of TIM module 1
	CANXL01_RXDA			CANXL receive input node 1
	GTM_CDTM0_DTM0_1			Input mux of CDTM0_DTM0_AUXIN0/1
	GTM_CDTM0_DTM1_1			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM0_DTM0_1			Input mux of CDTM0_DTM0_AUXIN0/1
	EGTM_CDTM0_DTM1_1			Input mux of CDTM0_DTM1_AUXIN0/1
	EGTM_CDTM0_DTM2_1			Input mux of CDTM0_DTM2_AUXIN0/1
	EGTM_CDTM0_DTM3_1			Input mux of CDTM0_DTM3_AUXIN0/1
	LETH0_P1_MII_RXERA			LETH0 PortX MII receive error (to be used with LETH0_P1_RXCLKA)
	EGTM_TIM0_IN7_2			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_2			Mux input channel 7 of TIM module 1
	PMS_HWC6G6IN			HWC6G6 pin input
	LETH0_P1_RXDA			LETH PortX TC14 interface receive data input
	P14.4	O0		General-purpose output
	GTM_TOUT84	O1		GTM muxed output
	GPT123_T3OUT	O2		External output for overflow/underflow detection of core timer T3
	ASCLIN0_ARTS	O3		Ready to send output
	QSPI2_SLSO4	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT84	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIA_TXD3	O11		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P2_TXCLKA)
	LETH0_P2_MIIC_TXD3	O12		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P2_TXCLKC)

(table continues...)

Table 38 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
A14	P14.5	I	FAST / PU2 / VDDEXTH S / ES	General-purpose input
	GTM_TIM0_IN0_4			Mux input channel 0 of TIM module 0
	GTM_TIM1_IN0_4			Mux input channel 0 of TIM module 1
	QSPI5_MRSTB			Master SPI data input
	GTM_CDTM2_DTM4_1			Input mux of CDTM2_DTM4_AUXIN0/1
	GTM_CDTM2_DTM5_1			Input mux of CDTM2_DTM5_AUXIN0/1
	EGTM_CDTM2_DTM4_1			Input mux of CDTM2_DTM4_AUXIN0/1
	EGTM_CDTM2_DTM5_1			Input mux of CDTM2_DTM5_AUXIN0/1
	LETH0_P2_MII_RXD3C			LETH0 PortX MII receive data bit 3 (to be used with LETH0_P2_RXCLKC)
	EGTM_TIM0_IN0_4			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_4			Mux input channel 0 of TIM module 1
	PMS_HWCFG1IN			HWCFG1 pin input
	P14.5	O0		General-purpose output
	GTM_TOUT85	O1		GTM muxed output
	ASCLIN0_ATX_F	O2		Transmit output
	QSPI5_MRST	O3		Slave SPI data output
	QSPI2_SLSO4_F	O4		Master slave select output
	—	O5		Reserved
	ERAY0_TXDB	O6		Transmit Channel B
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT85	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_TXD	O11		LETH PortX TC14 interface transmit data output
	LETH0_P1_TXD	O12		LETH PortX TC14 interface transmit data output
	CANXL01_TXD	O13		CANXL transmit output node 1
	—	O14		Reserved

(table continues...)

Table 38 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O15		Reserved
	EGTM_HRPWM1_CH2	PO		High resolution PWM 1 output channels
B13	P14.6	I	FAST / PU1 / VDDEXT S / ES	General-purpose input
	GTM_TIM0_IN1_4			Mux input channel 1 of TIM module 0
	GTM_TIM1_IN1_4			Mux input channel 1 of TIM module 1
	QSPI5_MTSRB			Slave SPI data input
	LETH0_P2_EDC			LETH PortX TC14 interface energy detection input
	GPT123_T3INB			Trigger/gate input of core timer T3 (input A, B and C)
	LETH0_P2_MDIOC			LETH PortX MDIO interface data input
	LETH0_P2_MII_RXD2C			LETH0 PortX MII receive data bit 2 (to be used with LETH0_P2_RXCLKC)
	EGTM_TIM0_IN1_4			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_4			Mux input channel 1 of TIM module 1
	P14.6	O0		General-purpose output
	GTM_TOUT86	O1		GTM muxed output
	QSPI5_MTSR	O2		Master SPI data output
	QSPI2_SLSO2_F	O3		Master slave select output
	CAN13_TXD	O4		CAN transmit output node 3
	ASCLIN0_ASLSO_F	O5		Slave select signal output
	ERAY0_TXENB	O6		Transmit Enable Channel B
	—	O7		Reserved
	ASCLIN0_ATX_F	O8		Transmit output
	EGTM_TOUT86	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM1_CH3	PO		High resolution PWM 1 output channels
	LETH0_P2_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
D13	P14.7	I	FAST / PU1 /	General-purpose input

(table continues...)

Table 38 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TIM0_IN0_5		VDDEXTH S / ES	Mux input channel 0 of TIM module 0
	GTM_TIM1_IN0_5			Mux input channel 0 of TIM module 1
	GTM_TIM4_IN7_10			Mux input channel 7 of TIM module 4
	ERAY0_RXDB0			Receive Channel B0
	CAN10_RXDB			CAN receive input node 0
	CAN13_RXDA			CAN receive input node 3
	QSPI7_MTSRA			Slave SPI data input
	EGTM_TIM0_IN0_5			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_5			Mux input channel 0 of TIM module 1
	LETH0_P2_RXDC			LETH PortX TC14 interface receive data input
	P14.7	O0		General-purpose output
	GTM_TOUT87	O1		GTM muxed output
	ASCLIN0_ARTS_F	O2		Ready to send output
	QSPI2_SLSO4_F	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT87	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIA_TXEN	O11		LETH0 PortX MII transmit enable (to be used with LETH0_P2_TXCLKA)
	LETH0_P2_MIIC_TXEN	O12		LETH0 PortX MII transmit enable (to be used with LETH0_P2_TXCLKC)
	LETH0_P2_RMIIA_TXEN	O13		LETH0 PortX RMII transmit enable (to be used with LETH0_P2_REFCLKA)
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_RMIIRA_TXEN	PO		LETH0 PortX RMII transmit enable (to be used with LETH0_P2_REFCLKA - registered*)
	LETH0_P2_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface

(table continues...)

Table 38 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
A13	P14.8	I	FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM2_IN2_3			Mux input channel 2 of TIM module 2
	GTM_TIM3_IN2_3			Mux input channel 2 of TIM module 3
	ERAY0_RXDA0			Receive Channel A0
	CAN02_RXDD			CAN receive input node 2
	ASCLIN1_ARXD			Receive input
	GPT123_T3EUDB			Count direction control input of core timer T3
	CANXL00_RXDA			CANXL receive input node 0
	QSPI7_MRSTA			Master SPI data input
	EGTM_TIM2_IN2_3			Mux input channel 2 of TIM module 2
	LETH0_P0_RXDA			LETH PortX TC14 interface receive data input
	LETH0_P2_TXCLKA			LETH PortX MII transmit clock
	LETH0_P2_TXCLKC			LETH PortX MII transmit clock
	P14.8	O0		General-purpose output
	GTM_TOUT88	O1		GTM muxed output
	ASCLIN5_ASLSO	O2		Slave select signal output
	ASCLIN7_ASLSO	O3		Slave select signal output
	ASCLIN0_ASLSO	O4		Slave select signal output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT88	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
D12	P14.9	I	LVDS_RX / FAST / PU1 /	General-purpose input
	GTM_TIM2_IN3_3			Mux input channel 3 of TIM module 2

(table continues...)

Table 38 (continued) Port 14 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TIM3_IN3_3		VDDEXTH S / ES	Mux input channel 3 of TIM module 3
	ASCLIN0_ACTSA_F			Clear to send input
	QSPI2_MRSTFN_F			Master SPI data input
	LETH0_P0_EDA			LETH PortX TC14 interface energy detection input
	LETH0_P0_MDIOA			LETH PortX MDIO interface data input
	EGTM_TIM2_IN3_3			Mux input channel 3 of TIM module 2
	P14.9	O0		General-purpose output
	GTM_TOUT89	O1		GTM muxed output
	CAN23_TXD	O2		CAN transmit output node 3
	MSC0_EN1	O3		Chip Select
	CAN10_TXD	O4		CAN transmit output node 0
	ERAY0_TXENB	O5		Transmit Enable Channel B
	ERAY0_TXENA	O6		Transmit Enable Channel A
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT89	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P2_MIIA_TXD1	O11		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P2_TXCLKA)
	LETH0_P2_MIIC_TXD1	O12		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P2_TXCLKC)
	LETH0_P2_RMIIA_TXD1	O13		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P2_REFCLKA)
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P2_RMIIRA_TXD1	PO		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P2_REFCLKA - registered*)
	LETH0_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
D11	P14.10	I	LVDS_RX / FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM2_IN4_3			Mux input channel 4 of TIM module 2
	GTM_TIM3_IN4_3			Mux input channel 4 of TIM module 3
	CAN23_RXDA			CAN receive input node 3
	QSPI2_MRSTFP_F			Master SPI data input

(table continues...)

Table 38 (continued) **Port 14 functions**

Ball	Symbol	Ctrl.	Buffer type	Function
	GPT123_T4INB			Trigger/gate input of timer T4
	EGTM_TIM2_IN4_3			Mux input channel 4 of TIM module 2
	P14.10	O0		General-purpose output
	GTM_TOUT90	O1		GTM muxed output
	QSPI5_SCLK	O2		Master SPI clock output
	MSC0_EN0	O3		Chip Select
	ASCLIN1_ATX	O4		Transmit output
	CAN02_TXD	O5		CAN transmit output node 2
	ERAY0_TXDA	O6		Transmit Channel A
	—	O7		Reserved
	LETH0_P2_RMIIA_TXD0	O8		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P2_REFCLKA)
	EGTM_TOUT90	O9		eGTM muxed output
	LETH0_P2_MIIA_TXD0	O10		LETH0 PortX MII transmit data bit 0 (to be used with LETH0_P2_TXCLKA)
	LETH0_P2_MIIC_TXD0	O11		LETH0 PortX MII transmit data bit 0 (to be used with LETH0_P2_TXCLKC)
	LETH0_P0_TXD	O12		LETH PortX TC14 interface transmit data output
	CANXL00_TXD	O13		CANXL transmit output node 0
	LETH0_P2_TXD	O14		LETH PortX TC14 interface transmit data output
	—	O15		Reserved
	LETH0_P2_RMIIRA_TXD0	PO		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P2_REFCLKA - registered*)

3.3.9 BGA292 STD port 15

Table 39 **Port 15 functions**

Ball	Symbol	Ctrl.	Buffer type	Function
B20	P15.0	I	FAST / PU1 / VDDEXT S / ES	General-purpose input
	GTM_TIM2_IN3_4			Mux input channel 3 of TIM module 2
	GTM_TIM3_IN3_4			Mux input channel 3 of TIM module 3
	SDMMC0_DAT7_IN			Read data in
	GPT123_T2INB			Trigger/gate input of timer T2
	EGTM_TIM2_IN3_4			Mux input channel 3 of TIM module 2

(table continues...)

Table 39 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_REFCLKA			LETH PortX RMII reference clock
	LETH0_P1_RXCLKA			LETH PortX MII receive clock
	P15.0	O0		General-purpose output
	GTM_TOUT71	O1		GTM muxed output
	ASCLIN1_ATX_F	O2		Transmit output
	QSPI0_SLSO13	O3		Master slave select output
	—	O4		Reserved
	CAN02_TXD	O5		CAN transmit output node 2
	ASCLIN1_ASCLK_F	O6		Shift clock output
	—	O7		Reserved
	LETH0_P0_TXD	O8		LETH PortX TC14 interface transmit data output
	EGTM_TOUT71	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM1_CH4	PO		High resolution PWM 1 output channels
	SDMMC0_DAT7	O		Write data out
A18	P15.1	I	FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM2_IN4_4			Mux input channel 4 of TIM module 2
	GTM_TIM3_IN4_4			Mux input channel 4 of TIM module 3
	CAN02_RXDA			CAN receive input node 2
	ASCLIN1_ARXA_F			Receive input
	QSPI2_SLSIB			Slave select input
	SCU_E_REQ7B			ERU channel 7 input B
	GPT123_T2EUDB			Count direction control input of timer T2
	EGTM_TIM2_IN4_4			Mux input channel 4 of TIM module 2
	LETH0_P0_RXDE			LETH PortX TC14 interface receive data input
	LETH0_P1_MII_RXDVA			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV

(table continues...)

Table 39 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_RMII_CRSDVA			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	P15.1	O0		General-purpose output
	GTM_TOUT72	O1		GTM muxed output
	ASCLIN1_ATX_F	O2		Transmit output
	QSPI2_SLSO5	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	SDMMC0_CLK	O7		Card clock
	—	O8		Reserved
	EGTM_TOUT72	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM1_CH5	PO		High resolution PWM 1 output channels
C19	P15.2	I	FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM2_IN5_4			Mux input channel 5 of TIM module 2
	GTM_TIM3_IN5_4			Mux input channel 5 of TIM module 3
	QSPI2_SLSIA			Slave select input
	SENT0_SENT5D			Receive input channel 5
	QSPI2_MRSTE			Master SPI data input
	GPT123_T4EUDB			Count direction control input of timer T4
	EGTM_TIM2_IN5_4			Mux input channel 5 of TIM module 2
	XSPI0_RXD3B			Receive data
	LETH0_P1_TXCLKA			LETH PortX MII transmit clock
	P15.2	O0		General-purpose output
	GTM_TOUT73	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	QSPI2_SLSO0	O3		Master slave select output

(table continues...)

Table 39 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN1_ATX_F	O4		Transmit output
	CAN01_TXD	O5		CAN transmit output node 1
	ASCLIN0_ASCLK	O6		Shift clock output
	QSPI7_SCLK_F	O7		Master SPI clock output
	ASCLIN1_ASLSO_F	O8		Slave select signal output
	EGTM_TOUT73	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPI0_TXDB3	O		Transmit data
B17	P15.3	I	FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM2_IN6_4			Mux input channel 6 of TIM module 2
	GTM_TIM3_IN6_4			Mux input channel 6 of TIM module 3
	CAN01_RXDA			CAN receive input node 1
	ASCLIN0_ARXB			Receive input
	QSPI2_SCLKA			Slave SPI clock inputs
	SDMMC0_CMD_IN			Command in
	GPT123_T5EUDB			Count direction control input of timer T5
	ASCLIN1_ACTSC_F			Clear to send input
	QSPI7_SCLKC_F			Slave SPI clock inputs
	EGTM_TIM2_IN6_4			Mux input channel 6 of TIM module 2
	LETH0_P2_MII_RXDVC			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	LETH0_P2_RMII_CRSDVC			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	P15.3	O0		General-purpose output
	GTM_TOUT74	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved

(table continues...)

Table 39 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	MSC0_EN1	O5		Chip Select
	—	O6		Reserved
	QSPI7_SCLK_F	O7		Master SPI clock output
	—	O8		Reserved
	EGTM_TOUT74	O9		eGTM muxed output
	LETH0_P1_MIIA_TXER	O10		LETH0 PortX MII transmit error (to be used with LETH0_P1_TXCLKA)
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM1_CH6	PO		High resolution PWM 1 output channels
	SDMMC0_CMD	O		Command out
A17	P15.4	I	FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM2_IN7_4			Mux input channel 7 of TIM module 2
	GTM_TIM3_IN7_4			Mux input channel 7 of TIM module 3
	I2C0_SCLC			Serial Clock Input 2
	QSPI2_MRSTA			Master SPI data input
	SCU_E_REQ0A			ERU channel 0 input A
	SENT1_SENT5D			Receive input channel 5
	GPT123_T5INB			Trigger/gate input of timer T5
	QSPI7_MRSTF_F			Master SPI data input
	EGTM_TIM2_IN7_4			Mux input channel 7 of TIM module 2
	P15.4	O0		General-purpose output
	GTM_TOUT75	O1		GTM muxed output
	ASCLIN1_ATX_F	O2		Transmit output
	QSPI2_MRST	O3		Slave SPI data output
	—	O4		Reserved
	—	O5		Reserved
	I2C0_SCL	O6		Serial Clock Output
	QSPI7_MTSR_F	O7		Master SPI data output
	QSPI7_MRST_F	O8		Slave SPI data output

(table continues...)

Table 39 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TOUT75	O9		eGTM muxed output
	LETH0_P1_MIIA_TXEN	O10		LETH0 PortX MII transmit enable (to be used with LETH0_P1_TXCLKA)
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	LETH0_P1_RMIIA_TXEN	O15		LETH0 PortX RMII transmit enable (to be used with LETH0_P1_REFCLKA)
E14	P15.5	I	FAST / PU1 / VDDEXT S / ES	General-purpose input
	GTM_TIM2_IN0_4			Mux input channel 0 of TIM module 2
	GTM_TIM3_IN0_4			Mux input channel 0 of TIM module 3
	ASCLIN1_ARXB_F			Receive input
	I2C0_SDAC			Serial Data Input 2
	QSPI2_MTSRA			Slave SPI data input
	SCU_E_REQ4D			ERU channel 4 input D
	QSPI7_MTSRE_F			Slave SPI data input
	GPT123_T6INB			Trigger/gate input of core timer T6
	EGTM_TIM2_IN0_4			Mux input channel 0 of TIM module 2
	P15.5	O0		General-purpose output
	GTM_TOUT76	O1		GTM muxed output
	ASCLIN1_ATX_F	O2		Transmit output
	QSPI2_MTSR	O3		Master SPI data output
	—	O4		Reserved
	MSC0_EN0	O5		Chip Select
	I2C0_SDA	O6		Serial Data Output
	LETH0_P1_TXD	O7		LETH PortX TC14 interface transmit data output
	LETH0_P0_TXD	O8		LETH PortX TC14 interface transmit data output
	EGTM_TOUT76	O9		eGTM muxed output
	LETH0_P1_MIIA_TXD0	O10		LETH0 PortX MII transmit data bit 0 (to be used with LETH0_P1_TXCLKA)
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved

(table continues...)

Table 39 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
A16	—	O14		Reserved
	LETH0_P1_RMIIA_TXD0	O15		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P1_REFCLKA)
	EGTM_HRPWM1_CH7	PO		High resolution PWM 1 output channels
	P15.6	I	FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM0_IN0_6			Mux input channel 0 of TIM module 0
	GTM_TIM1_IN0_6			Mux input channel 0 of TIM module 1
	GTM_TIM2_IN2_10			Mux input channel 2 of TIM module 2
	QSPI2_MTSRB			Slave SPI data input
	LETH0_P1_MDIOG			LETH PortX MDIO interface data input
	GPT123_T6EUDB			Count direction control input of core timer T6
	LETH0_P1_EDG			LETH PortX TC14 interface energy detection input
	EGTM_TIM0_IN0_6			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_6			Mux input channel 0 of TIM module 1
	EGTM_TIM2_IN2_10			Mux input channel 2 of TIM module 2
	LETH0_P1_MII_RMII_RXD1A			LETH0 PortX MII and RMII receive data bit 1 (to be used with LETH0_P1_RXCLKA or LETH0_P1_REFCLKA)
	P15.6	O0		General-purpose output
	GTM_TOUT77	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	QSPI2_MTSR	O3		Master SPI data output
	QSPI5_SLSO3	O4		Master slave select output
	QSPI2_SCLK	O5		Master SPI clock output
	ASCLIN3_ASCLK	O6		Shift clock output
	QSPI7_MTSR_F	O7		Master SPI data output
	ASCLIN1_ASLSO_F	O8		Slave select signal output
	EGTM_TOUT77	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 39 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
D15	P15.7	I	FAST / PU1 / VDDEXT S / ES	General-purpose input
	GTM_TIM0_IN1_5			Mux input channel 1 of TIM module 0
	GTM_TIM1_IN1_5			Mux input channel 1 of TIM module 1
	ASCLIN3_ARXA			Receive input
	QSPI2_MRSTB			Master SPI data input
	GPT123_CAPINB3			Trigger input to capture value of timer T5 into CAPREL register (input B)
	QSPI7_MRSTE_F			Master SPI data input
	EGTM_TIM0_IN1_5			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_5			Mux input channel 1 of TIM module 1
	LETH0_P1_RXDB			LETH PortX TC14 interface receive data input
	P15.7	O0		General-purpose output
	GTM_TOUT78	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	QSPI2_MRST	O3		Slave SPI data output
	—	O4		Reserved
	ASCLIN1_ARTS_F	O5		Ready to send output
	—	O6		Reserved
	QSPI7_SLSO10_F	O7		Master slave select output
	—	O8		Reserved
	EGTM_TOUT78	O9		eGTM muxed output
	LETH0_P1_MIIA_TXD1	O10		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P1_TXCLKA)
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	LETH0_P1_RMIIA_TXD1	O15		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P1_REFCLKA)
	LETH0_P1_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
D14	P15.8	I	FAST / PU1 /	General-purpose input

(table continues...)

Table 39 (continued) Port 15 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TIM0_IN2_5		VDDEXT S / ES	Mux input channel 2 of TIM module 0
	GTM_TIM1_IN2_5			Mux input channel 2 of TIM module 1
	QSPI2_SCLKB			Slave SPI clock inputs
	SCU_E_REQ5A			ERU channel 5 input A
	EGTM_TIM0_IN2_5			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_5			Mux input channel 2 of TIM module 1
	LETH0_P1_MII_RMII_RXD 0A			LETH0 PortX MII and RMII receive data bit 0 (to be used with LETH0_P1_RXCLKA or LETH0_P1_REFCLKA)
	P15.8	O0		General-purpose output
	GTM_TOUT79	O1		GTM muxed output
	—	O2		Reserved
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	ASCLIN3_ASCLK	O6		Shift clock output
	QSPI7_SLSO11_F	O7		Master slave select output
	—	O8		Reserved
	EGTM_TOUT79	O9		eGTM muxed output
	GPT123_T6OUT	O10		External output for overflow/underflow detection of core timer T6
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

3.3.10 BGA292_STD port 20

Table 40 Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
H20	P20.0	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN6_7			Mux input channel 6 of TIM module 0
	GTM_TIM1_IN4_9			Mux input channel 4 of TIM module 1

(table continues...)

Table 40 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TIM1_IN6_7			Mux input channel 6 of TIM module 1
	CAN03_RXDC			CAN receive input node 3
	CAN21_RXDC			CAN receive input node 1
	CBS_TGI0			Trigger input
	SCU_E_REQ6A			ERU channel 6 input A
	GPT120_T6EUDA			Count direction control input of core timer T6
	SENT1_SENT1D			Receive input channel 1
	GPT122_T2INB			Trigger/gate input of timer T2
	LETH0_P0_MII_RXERB			LETH0 PortX MII receive error (to be used with LETH0_P0_RXCLKB)
	LETH1_P0_MII_RXERB			LETH1 PortX MII receive error (to be used with LETH1_P0_RXCLKB)
	EGTM_TIM0_IN6_7			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN4_9			Mux input channel 4 of TIM module 1
	EGTM_TIM1_IN6_7			Mux input channel 6 of TIM module 1
	CLOCK_CLKA_SYSClk			System clock input
	P20.0	O0		General-purpose output
	GTM_TOUT59	O1		GTM muxed output
	ASCLIN3_ATX_F	O2		Transmit output
	ASCLIN3_ASCLK_F	O3		Shift clock output
	SENT1_SPC1	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT59	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P0_MIIB_TXD2	O11		LETH0 PortX MII transmit data bit 2 (to be used with LETH0_P0_TXCLKB)
	LETH0_P1_MDC	O12		LETH PortX MDIO interface clock output
	LETH1_P0_MIIB_TXD2	O13		LETH1 PortX MII transmit data bit 2 (to be used with LETH1_P0_TXCLKB)
	—	O14		Reserved
	XSPIO_CSB1_N	O15		Chip select

(table continues...)

Table 40 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	HSCT0_SYSCLK_OUT	PO		sys clock output
	CBS_TGO0	O		Trigger output
G19	P20.1	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM2_IN3_5			Mux input channel 3 of TIM module 2
	GTM_TIM3_IN3_5			Mux input channel 3 of TIM module 3
	GTM_TIM4_IN4_11			Mux input channel 4 of TIM module 4
	CBS_TGI1			Trigger input
	GTM_CDTM1_DTM4_2			Input mux of CDTM1_DTM4_AUXIN0/1
	GTM_CDTM1_DTM5_2			Input mux of CDTM1_DTM5_AUXIN0/1
	EGTM_CDTM1_DTM4_2			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM5_2			Input mux of CDTM1_DTM5_AUXIN0/1
	LETH0_P0_CRSC			LETH PortX MII carrier sense
	EGTM_TIM2_IN3_5			Mux input channel 3 of TIM module 2
	P20.1	O0		General-purpose output
	GTM_TOUT60	O1		GTM muxed output
	ASCLIN3_ASLSO_F	O2		Slave select signal output
	CAN32_TXD	O3		CAN transmit output node 2
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT60	O9		eGTM muxed output
	LETH1_P0_MIIB_TXD3	O10		LETH1 PortX MII transmit data bit 3 (to be used with LETH1_P0_TXCLKB)
	LETH0_P0_MIIB_TXD3	O11		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_MIIB_TXD0	O12		LETH0 PortX MII transmit data bit 0 (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_RMIIB_TXD0	O13		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P0_REFCLKB)
	LETH1_P0_MIIB_TXD0	O14		LETH1 PortX MII transmit data bit 0 (to be used with LETH1_P0_TXCLKB)

(table continues...)

Table 40 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH1_P0_RMIIB_TXD0	O15		LETH1 PortX RMII transmit data bit 0 (to be used with LETH1_P0_REFCLKB)
	LETH0_P0_RMIIRB_TXD0	PO		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P0_REFCLKB - registered*)
	LETH1_P0_RMIIRB_TXD0	PO		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P0_REFCLKB - registered*)
	CBS_TGO1	O		Trigger output
H19	P20.2	I	S / PU / VDDEXT	General-purpose input
	TESTMODE			Testmode Enable Input
	PMS_TESTMODEIN			TESTMODE pin input
G20	P20.3	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM2_IN4_5			Mux input channel 4 of TIM module 2
	GTM_TIM3_IN4_5			Mux input channel 4 of TIM module 3
	GTM_TIM4_IN5_11			Mux input channel 5 of TIM module 4
	ASCLIN3_ARXC_F			Receive input
	GPT120_T6INA			Trigger/gate input of core timer T6
	SENT0_SENT3D			Receive input channel 3
	GPT122_T2EUDB			Count direction control input of timer T2
	EGTM_TIM2_IN4_5			Mux input channel 4 of TIM module 2
	XSPIO_RXD0B			Receive data
	LETH0_P0_TXCLKB			LETH PortX MII transmit clock
	LETH1_P0_TXCLKB			LETH PortX MII transmit clock
	P20.3	O0		General-purpose output
	GTM_TOUT61	O1		GTM muxed output
	ASCLIN3_ATX_F	O2		Transmit output
	QSPIO_SLSO9_F	O3		Master slave select output
	QSPI2_SLSO9	O4		Master slave select output
	CAN03_TXD	O5		CAN transmit output node 3
	CAN21_TXD	O6		CAN transmit output node 1
	—	O7		Reserved
	SENT0_SPC3	O8		Transmit output
	EGTM_TOUT61	O9		eGTM muxed output
	LETH0_P0_TXD	O10		LETH PortX TC14 interface transmit data output
	—	O11		Reserved

(table continues...)

Table 40 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	XSPIO_TXDB0	O		Transmit data
F17	P20.6	I	FAST / PU1 / VDDEXT S / ES	General-purpose input
	GTM_TIM2_IN6_5			Mux input channel 6 of TIM module 2
	GTM_TIM3_IN6_5			Mux input channel 6 of TIM module 3
	GTM_TIM6_IN0_1			Mux input channel 0 of TIM module 6
	CAN12_RXDA			CAN receive input node 2
	SENT1_SENT3D			Receive input channel 3
	CAN32_RXDB			CAN receive input node 2
	GPT122_T4EUDB			Count direction control input of timer T4
	EGTM_TIM2_IN6_5			Mux input channel 6 of TIM module 2
	XSPIO_RXD1B			Receive data
	P20.6	O0		General-purpose output
	GTM_TOUT62	O1		GTM muxed output
	ASCLIN1_ARTS	O2		Ready to send output
	QSPIO_SLSO8_F	O3		Master slave select output
	QSPI2_SLSO8	O4		Master slave select output
	ASCLIN3_ASLSO_F	O5		Slave select signal output
	SENT1_SPC3	O6		Transmit output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT62	O9		eGTM muxed output
	LETH1_P0_MIIB_TXER	O10		LETH1 PortX MII transmit error (to be used with LETH1_P0_TXCLKB)
	LETH0_P0_MIIB_TXER	O11		LETH0 PortX MII transmit error (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_MIIB_TXEN	O12		LETH0 PortX MII transmit enable (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_RMIIB_TXEN	O13		LETH0 PortX RMII transmit enable (to be used with LETH0_P0_REFCLKB)

(table continues...)

Table 40 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH1_P0_MIIB_TXEN	O14		LETH1 PortX MII transmit enable (to be used with LETH1_P0_TXCLKB)
	LETH1_P0_RMIIB_TXEN	O15		LETH1 PortX RMII transmit enable (to be used with LETH1_P0_REFCLKB)
	LETH0_P0_RMIIRB_TXEN	PO		LETH0 PortX RMII transmit enable (to be used with LETH0_P0_REFCLKB - registered*)
	LETH1_P0_RMIIRB_TXEN	PO		LETH0 PortX RMII transmit enable (to be used with LETH0_P0_REFCLKB - registered*)
	XSPIO_TXDB1	O		Transmit data
F19	P20.7	I	FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM1_IN5_8			Mux input channel 5 of TIM module 1
	GTM_TIM2_IN7_5			Mux input channel 7 of TIM module 2
	GTM_TIM3_IN7_5			Mux input channel 7 of TIM module 3
	GTM_TIM6_IN1_1			Mux input channel 1 of TIM module 6
	CAN00_RXDB			CAN receive input node 0
	ASCLIN1_ACTSA			Clear to send input
	SDMMC0_DAT0_IN			Read data in
	SENT1_SENT0D			Receive input channel 0
	EGTM_TIM1_IN5_8			Mux input channel 5 of TIM module 1
	EGTM_TIM2_IN7_5			Mux input channel 7 of TIM module 2
	P20.7	O0		General-purpose output
	GTM_TOUT63	O1		GTM muxed output
	—	O2		Reserved
	ASCLIN3_ARTS_F	O3		Ready to send output
	—	O4		Reserved
	CAN12_TXD	O5		CAN transmit output node 2
	SENT1_SPC0	O6		Transmit output
	LETH1_P0_MIIB_TXD2	O7		LETH1 PortX MII transmit data bit 2 (to be used with LETH1_P0_TXCLKB)
	—	O8		Reserved
	EGTM_TOUT63	O9		eGTM muxed output
	LETH1_P0_MIIB_TXD3	O10		LETH1 PortX MII transmit data bit 3 (to be used with LETH1_P0_TXCLKB)
	LETH0_P0_MIIB_TXD3	O11		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P0_TXCLKB)

(table continues...)

Table 40 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P0_MIIB_TXD1	O12		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_RMIIB_TXD1	O13		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P0_REFCLKB)
	LETH1_P0_MIIB_TXD1	O14		LETH1 PortX MII transmit data bit 1 (to be used with LETH1_P0_TXCLKB)
	LETH1_P0_RMIIB_TXD1	O15		LETH1 PortX RMII transmit data bit 1 (to be used with LETH1_P0_REFCLKB)
	EGTM_HRPWM2_CH7	PO		High resolution PWM 2 output channels
	SDMMC0_DAT0	O		Write data out
F20	P20.8	I	FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM0_IN7_3			Mux input channel 7 of TIM module 0
	GTM_TIM1_IN7_3			Mux input channel 7 of TIM module 1
	GTM_TIM6_IN2_1			Mux input channel 2 of TIM module 6
	SDMMC0_DAT1_IN			Read data in
	LETH0_P0_CRSD			LETH PortX MII carrier sense
	LETH1_P0_CRSD			LETH PortX MII carrier sense
	EGTM_TIM0_IN7_3			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_3			Mux input channel 7 of TIM module 1
	LETH0_P0_MII_RXDVB			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	LETH0_P0_RMII_CRSDVB			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	LETH1_P0_MII_RXDVB			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	LETH1_P0_RMII_CRSDVB			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	P20.8	O0		General-purpose output
	GTM_TOUT64	O1		GTM muxed output
	ASCLIN1_ASLSO	O2		Slave select signal output
	QSPI0_SLSO0_F	O3		Master slave select output
	QSPI1_SLSO0	O4		Master slave select output
	CAN00_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	—	O7		Reserved

(table continues...)

Table 40 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O8		Reserved
	EGTM_TOUT64	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM2_CH0	PO		High resolution PWM 2 output channels
	SDMMC0_DAT1	O		Write data out
E17	P20.9	I	FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM2_IN5_5			Mux input channel 5 of TIM module 2
	GTM_TIM3_IN5_5			Mux input channel 5 of TIM module 3
	GTM_TIM6_IN3_1			Mux input channel 3 of TIM module 6
	CAN03_RXDE			CAN receive input node 3
	ASCLIN1_ARXC			Receive input
	QSPI0_SLSIB_F			Slave select input
	SCU_E_REQ7A			ERU channel 7 input A
	ADC_TRIG62			Triggers from PORTS to ADC
	LETH0_P0_COLD			LETH PortX MII collision detection
	EGTM_TIM2_IN5_5			Mux input channel 5 of TIM module 2
	XSPI0_RXD2B			Receive data
	P20.9	O0		General-purpose output
	GTM_TOUT65	O1		GTM muxed output
	CAN32_TXD	O2		CAN transmit output node 2
	QSPI0_SLSO1_F	O3		Master slave select output
	QSPI1_SLSO1	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT65	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 40 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P0_MIIB_TXD1	O11		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_RMIIB_TXD1	O12		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P0_REFCLKB)
	—	O13		Reserved
	LETH1_P0_MIIB_TXD1	O14		LETH1 PortX MII transmit data bit 1 (to be used with LETH1_P0_TXCLKB)
	LETH1_P0_RMIIB_TXD1	O15		LETH1 PortX RMII transmit data bit 1 (to be used with LETH1_P0_REFCLKB)
	EGTM_HRPWM2_CH1	PO		High resolution PWM 2 output channels
	XSPIO_TXDB2	O		Transmit data
E19	P20.10	I	FAST / PU1 / VDDEXT S / ES	General-purpose input
	GTM_TIM2_IN6_6			Mux input channel 6 of TIM module 2
	GTM_TIM3_IN6_6			Mux input channel 6 of TIM module 3
	SDMMC0_DAT2_IN			Read data in
	EGTM_TIM2_IN6_6			Mux input channel 6 of TIM module 2
	P20.10	O0		General-purpose output
	GTM_TOUT66	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	QSPIO_SLSO6_F	O3		Master slave select output
	QSPIO2_SLSO7	O4		Master slave select output
	CAN03_TXD	O5		CAN transmit output node 3
	ASCLIN1_ASCLK	O6		Shift clock output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT66	O9		eGTM muxed output
	LETH1_P0_TXD	O10		LETH PortX TC14 interface transmit data output
	LETH0_P0_MIIB_TXD0	O11		LETH0 PortX MII transmit data bit 0 (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_RMIIB_TXD0	O12		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P0_REFCLKB)
	LETH0_P0_TXD	O13		LETH PortX TC14 interface transmit data output
	LETH1_P0_MIIB_TXD0	O14		LETH1 PortX MII transmit data bit 0 (to be used with LETH1_P0_TXCLKB)

(table continues...)

Table 40 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH1_P0_RMII_TXD0	O15		LETH1 PortX RMII transmit data bit 0 (to be used with LETH1_P0_REFCLKB)
	EGTM_HRPWM2_CH2	PO		High resolution PWM 2 output channels
	SDMMC0_DAT2	O		Write data out
E20	P20.11	I	FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM2_IN7_6			Mux input channel 7 of TIM module 2
	GTM_TIM3_IN7_6			Mux input channel 7 of TIM module 3
	QSPI0_SCLKA_F			Slave SPI clock inputs
	SDMMC0_DAT3_IN			Read data in
	ASCLIN3_ACTSB_F			Clear to send input
	EGTM_TIM2_IN7_6			Mux input channel 7 of TIM module 2
	LETH0_P0_MII_RMII_RXD 1B			LETH0 PortX MII and RMII receive data bit 1 (to be used with LETH0_P0_RXCLKB or LETH0_P0_REFCLKB)
	LETH1_P0_MII_RMII_RXD 1B			LETH1 PortX MII and RMII receive data bit 1 (to be used with LETH1_P0_RXCLKB or LETH1_P0_REFCLKB)
	P20.11	O0		General-purpose output
	GTM_TOUT67	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SCLK_F	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT67	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM2_CH3	PO		High resolution PWM 2 output channels
	SDMMC0_DAT3	O		Write data out

(table continues...)

Table 40 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
D19	P20.12	I	FAST / PU1 / VDDEXT S / ES	General-purpose input
	GTM_TIM2_IN0_5			Mux input channel 0 of TIM module 2
	GTM_TIM3_IN0_5			Mux input channel 0 of TIM module 3
	QSPI0_MRSTA_F			Master SPI data input
	SDMMC0_DAT4_IN			Read data in
	EGTM_TIM2_IN0_5			Mux input channel 0 of TIM module 2
	LETH0_P0_MII_RMII_RXD 0B			LETH0 PortX MII and RMII receive data bit 0 (to be used with LETH0_P0_RXCLKB or LETH0_P0_REFCLKB)
	LETH1_P0_MII_RMII_RXD 0B			LETH1 PortX MII and RMII receive data bit 0 (to be used with LETH1_P0_RXCLKB or LETH1_P0_REFCLKB)
	P20.12	O0		General-purpose output
	GTM_TOUT68	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_MRST_F	O3		Slave SPI data output
	QSPI0_MTSR_F	O4		Master SPI data output
	—	O5		Reserved
	—	O6		Reserved
	LETH0_P0_MDC	O7		LETH PortX MDIO interface clock output
	—	O8		Reserved
	EGTM_TOUT68	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	EGTM_HRPWM2_CH4	PO		High resolution PWM 2 output channels
	SDMMC0_DAT4	O		Write data out
D20	P20.13	I	FAST / PU1 / VDDEXT S / ES	General-purpose input
	GTM_TIM2_IN1_4			Mux input channel 1 of TIM module 2
	GTM_TIM3_IN1_4			Mux input channel 1 of TIM module 3
	QSPI0_SLSIA_F			Slave select input
	SDMMC0_DAT5_IN			Read data in

(table continues...)

Table 40 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P0_MII_RXD2B	O0		LETH0 PortX MII receive data bit 2 (to be used with LETH0_P0_RXCLKB)
	LETH1_P0_MII_RXD2B			LETH1 PortX MII receive data bit 2 (to be used with LETH1_P0_RXCLKB)
	EGTM_TIM2_IN1_4			Mux input channel 1 of TIM module 2
	P20.13			General-purpose output
	GTM_TOUT69			GTM muxed output
	—			Reserved
	QSPIO_SLSO2_F			Master slave select output
	QSPI1_SLSO2			Master slave select output
	QSPIO_SCLK_F			Master SPI clock output
	—			Reserved
	—			Reserved
	—			Reserved
	EGTM_TOUT69			eGTM muxed output
	—			Reserved
	—			Reserved
	—			Reserved
	—			Reserved
	—			Reserved
	XSPIO_CLKB			Clock output
	EGTM_HRPWM2_CH5			High resolution PWM 2 output channels
	SDMMC0_DAT5			Write data out
C20	P20.14	I	FAST / PU1 / VDDEXTH S / ES	General-purpose input
	GTM_TIM2_IN2_4			Mux input channel 2 of TIM module 2
	GTM_TIM3_IN2_4			Mux input channel 2 of TIM module 3
	QSPIO_MTSRA_F			Slave SPI data input
	SDMMC0_DAT6_IN			Read data in
	QSPI4_MRSTH			Master SPI data input
	LETH0_P0_MII_RXD3B			LETH0 PortX MII receive data bit 3 (to be used with LETH0_P0_RXCLKB)
	LETH1_P0_MII_RXD3B			LETH1 PortX MII receive data bit 3 (to be used with LETH1_P0_RXCLKB)
	EGTM_TIM2_IN2_4			Mux input channel 2 of TIM module 2

(table continues...)

Table 40 (continued) Port 20 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	P20.14	O0		General-purpose output
	GTM_TOUT70	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_MTSR_F	O3		Master SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT70	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	XSPI0_CSB0_N	O15		Chip select
	EGTM_HRPWM2_CH6	PO		High resolution PWM 2 output channels
	SDMMC0_DAT6	O		Write data out

3.3.11 BGA292_STD port 21

Table 41 Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
K17	P21.0	I	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM2_IN4_6			Mux input channel 4 of TIM module 2
	GTM_TIM3_IN4_6			Mux input channel 4 of TIM module 3
	GTM_TIM4_IN0_11			Mux input channel 0 of TIM module 4
	QSPI4_MRSTDN_F			Master SPI data input
	DMU_FDEST			FDEST for NVM
	HSCT1_RXDN			Rx data
	QSPI0_SCLKEN			Slave SPI clock inputs (LVDS N line)
	QSPI4_MRSTE			Master SPI data input
	GPT123_T6EUDA			Count direction control input of core timer T6

(table continues...)

Table 41 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM2_IN4_6			Mux input channel 4 of TIM module 2
	QSPI0_SCLKD			Slave SPI clock inputs
	P21.0	O0		General-purpose output
	GTM_TOUT51	O1		GTM muxed output
	—	O2		Reserved
	GPT123_T6OUT	O3		External output for overflow/underflow detection of core timer T6
	—	O4		Reserved
	—	O5		Reserved
	QSPI0_SLSO8_F	O6		Master slave select output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT51	O9		eGTM muxed output
	LETH0_P0_MIIB_TXD1	O10		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P0_TXCLKB)
	LETH0_P1_PPS	O11		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	LETH0_P0_RMIIB_TXD1	O12		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P0_REFCLKB)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P0_RMIIRB_TXD1	PO		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P0_REFCLKB - registered*)
	CSCU_CSRM1	O		Pin Output Value
J17	P21.1	I	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM2_IN5_6			Mux input channel 5 of TIM module 2
	GTM_TIM3_IN5_6			Mux input channel 5 of TIM module 3
	GTM_TIM4_IN1_13			Mux input channel 1 of TIM module 4
	QSPI4_MRSTDP_F			Master SPI data input
	HSCT1_RXDP			Rx data
	QSPI0_SCLKEP			Slave SPI clock inputs (LVDS P line)
	GTM_CDTM4_DTM4_2			Input mux of CDTM4_DTM4_AUXIN0/1
	GTM_CDTM4_DTM5_2			Input mux of CDTM4_DTM5_AUXIN0/1

(table continues...)

Table 41 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM2_IN5_6			Mux input channel 5 of TIM module 2
	QSPIO_SCLKF			Slave SPI clock inputs
	P21.1	O0		General-purpose output
	GTM_TOUT52	O1		GTM muxed output
	—	O2		Reserved
	GPT122_T3OUT	O3		External output for overflow/underflow detection of core timer T3
	—	O4		Reserved
	—	O5		Reserved
	QSPIO_SCLK_F	O6		Master SPI clock output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT52	O9		eGTM muxed output
	LETH0_P0_MIIB_TXER	O10		LETH0 PortX MII transmit error (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_MIIB_TXEN	O11		LETH0 PortX MII transmit enable (to be used with LETH0_P0_TXCLKB)
	LETH0_P0_RMIIB_TXEN	O12		LETH0 PortX RMII transmit enable (to be used with LETH0_P0_REFCLKB)
	LETH1_P0_MIIB_TXEN	O13		LETH1 PortX MII transmit enable (to be used with LETH1_P0_TXCLKB)
	LETH1_P0_RMIIB_TXEN	O14		LETH1 PortX RMII transmit enable (to be used with LETH1_P0_REFCLKB)
	—	O15		Reserved
	LETH0_P0_RMIIRB_TXEN	PO		LETH0 PortX RMII transmit enable (to be used with LETH0_P0_REFCLKB - registered*)
	LETH1_P0_RMIIRB_TXEN	PO		LETH0 PortX RMII transmit enable (to be used with LETH0_P0_REFCLKB - registered*)
	CSCU_CSRM2	O		Pin Output Value
K19	P21.2	I	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN0_7			Mux input channel 0 of TIM module 0
	GTM_TIM1_IN0_7			Mux input channel 0 of TIM module 1
	GTM_TIM5_IN4_10			Mux input channel 4 of TIM module 5
	QSPI2_MRSTCN			Master SPI data input (LVDS N line)

(table continues...)

Table 41 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SMU_EXT_EMERGENCYSTOP_REQ			Emergency Stop External Request B
	ASCLIN3_ARXGN			Differential Receive input (low active)
	HSCT0_RXDN			Rx data
	QSPI4_MRSTCN_F			Master SPI data input
	QSPI0_MTSRDN			Slave SPI data input (LVDS N line)
	SENT0_SENT2D			Receive input channel 2
	GPT123_T3INA			Trigger/gate input of core timer T3 (input A, B and C)
	GTM_CDTM1_DTM4_1			Input mux of CDTM1_DTM4_AUXIN0/1
	GTM_CDTM1_DTM5_1			Input mux of CDTM1_DTM5_AUXIN0/1
	EGTM_CDTM1_DTM4_1			Input mux of CDTM1_DTM4_AUXIN0/1
	EGTM_CDTM1_DTM5_1			Input mux of CDTM1_DTM5_AUXIN0/1
	EGTM_TIM0_IN0_7			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_7			Mux input channel 0 of TIM module 1
	QSPI0_MTSRE			Slave SPI data input
	QSPI4_MTSRC			Slave SPI data input
	LETH0_P0_MDIOH			LETH PortX MDIO interface data input
	LETH0_P0_EDH			LETH PortX TC14 interface energy detection input
	P21.2	O0		General-purpose output
	GTM_TOUT53	O1		GTM muxed output
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	SENT0_SPC2	O4		Transmit output
	—	O5		Reserved
	QSPI0_MTSR_F	O6		Master SPI data output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT53	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved

(table continues...)

Table 41 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O15		Reserved
	LETH0_P0_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
J19	P21.3	I	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN1_6			Mux input channel 1 of TIM module 0
	GTM_TIM1_IN1_6			Mux input channel 1 of TIM module 1
	GTM_TIM5_IN5_13			Mux input channel 5 of TIM module 5
	QSPI2_MRSTCP			Master SPI data input (LVDS P line)
	ASCLIN3_ARXGP			Differential Receive input (high active)
	HSCT0_RXDP			Rx data
	QSPI4_MRSTCP_F			Master SPI data input
	QSPI0_MTSRDP			Slave SPI data input (LVDS P line)
	SENT1_SENT2D			Receive input channel 2
	GPT123_T3EUDA			Count direction control input of core timer T3
	EGTM_TIM0_IN1_6			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_6			Mux input channel 1 of TIM module 1
	QSPI0_MTSRF			Slave SPI data input
	P21.3	O0		General-purpose output
	GTM_TOUT54	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	SENT1_SPC2	O4		Transmit output
	—	O5		Reserved
	QSPI0_SLSO9_F	O6		Master slave select output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT54	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 41 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
K20	P21.4	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	GTM_TIM0_IN2_6			Mux input channel 2 of TIM module 0
	GTM_TIM1_IN2_6			Mux input channel 2 of TIM module 1
	GTM_TIM5_IN6_13			Mux input channel 6 of TIM module 5
	SENT0_SENT0D			Receive input channel 0
	GPT123_T4INA			Trigger/gate input of timer T4
	EGTM_TIM0_IN2_6			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_6			Mux input channel 2 of TIM module 1
	LETH0_P0_REFCLKB			LETH0 PortX RMII reference clock
	LETH0_P0_RXCLKB			LETH PortX MII receive clock
	LETH1_P0_REFCLKB			LETH PortX RMII reference clock
	LETH1_P0_RXCLKB			LETH PortX MII receive clock
	P21.4	O0		General-purpose output
	GTM_TOUT55	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	SENT0_SPC0	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	QSPI0_MRSTN	O8		Slave SPI inverted data output
	EGTM_TOUT55	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	HSCT0_TXDN	PO		Tx data
J20	P21.5	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	GTM_TIM0_IN3_6			Mux input channel 3 of TIM module 0
	GTM_TIM1_IN3_6			Mux input channel 3 of TIM module 1
	GTM_TIM5_IN7_11			Mux input channel 7 of TIM module 5

(table continues...)

Table 41 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SENT0_SENT1D			Receive input channel 1
	QSPIO_MRSTE_F			Master SPI data input
	GPT123_T6INA			Trigger/gate input of core timer T6
	EGTM_TIM0_IN3_6			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_6			Mux input channel 3 of TIM module 1
	P21.5	O0		General-purpose output
	GTM_TOUT56	O1		GTM muxed output
	ASCLIN3_ASCLK	O2		Shift clock output
	—	O3		Reserved
	SENT0_SPC1	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	QSPIO_MRSTP	O8		Slave SPI data output
	EGTM_TOUT56	O9		eGTM muxed output
	GPT123_T3OUT	O10		External output for overflow/underflow detection of core timer T3
	LETH0_P0_MIIB_TXEN	O11		LETH0 PortX MII transmit enable (to be used with LETH0_P0_TXCLKB)
	—	O12		Reserved
	—	O13		Reserved
	LETH1_P0_MIIB_TXEN	O14		LETH1 PortX MII transmit enable (to be used with LETH1_P0_TXCLKB)
	—	O15		Reserved
	HSCT0_TXDP	PO		Tx data
H17	P21.6	I	FAST / PD3 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN4_8			Mux input channel 4 of TIM module 0
	GTM_TIM1_IN4_8			Mux input channel 4 of TIM module 1
	GTM_TIM4_IN2_13			Mux input channel 2 of TIM module 4
	CAN33_RXDB			CAN receive input node 3
	GPT120_T5EUDA			Count direction control input of timer T5
	ASCLIN3_ARXF_F			Receive input
	CBS_TGI2			Trigger input
	TDI			JTAG Module Data Input

(table continues...)

Table 41 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPIO_SLSIC			Slave select input
	LETH0_P0_COLC			LETH PortX MII collision detection
	LETH1_P0_COLC			LETH PortX MII collision detection
	EGTM_TIM0_IN4_8			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_8			Mux input channel 4 of TIM module 1
	P21.6	O0		General-purpose output
	GTM_TOUT57	O1		GTM muxed output
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	GPT120_T3OUT	O7		External output for overflow/underflow detection of core timer T3
	—	O8		Reserved
	EGTM_TOUT57	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	DAP3	I/PO		DAP:DAP3 Data I/O
	DAPE1	I/PO		DAPE: DAPE1 Data I/O DAPE: DAPE1 Data I/O (PD Devices: VSS)
	CBS_TGO2	O		Trigger output
H16	P21.7	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN5_7			Mux input channel 5 of TIM module 0
	GTM_TIM1_IN5_7			Mux input channel 5 of TIM module 1
	GTM_TIM4_IN3_13			Mux input channel 3 of TIM module 4
	GPT120_T5INA			Trigger/gate input of timer T5
	CBS_TGI3			Trigger input
	LETH0_P0_MII_RXERC			LETH0 PortX MII receive error (to be used with LETH0_P0_RXCLKC)

(table continues...)

Table 41 (continued) Port 21 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM0_IN5_7			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_7			Mux input channel 5 of TIM module 1
	P21.7	O0		General-purpose output
	GTM_TOUT58	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	ASCLIN3_ASCLK	O3		Shift clock output
	CAN33_TXD	O4		CAN transmit output node 3
	—	O5		Reserved
	—	O6		Reserved
	GPT120_T6OUT	O7		External output for overflow/underflow detection of core timer T6
	—	O8		Reserved
	EGTM_TOUT58	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	DAP2	I/PO		DAP:DAP2 Data I/O
	DAPE2	I/PO		DAPE: DAPE2 Data I/O DAPE: DAPE2 Data I/O (PD Devices: VSS)
	TDO	PO		PU/TRIST controlled through PMS_PADCON.ALLTRIST (HWCFG6 P14.4) during reset (PORST=0). The default state after PORST release in DAP mode is controlled through PMS_PADCON.ALLTRIST (HWCFG6 P14.4) . The default state after PORST release in JTAG mode is HighZ. In Standby Mode it is controlled through PMS_PADCON.ALLTRIST (HWCFG6 P14.4)
	CBS_TGO3	O		Trigger output

3.3.12 BGA292_STD port 22

Table 42 Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
P20	P22.0	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	GTM_TIM0_IN1_7			Mux input channel 1 of TIM module 0
	GTM_TIM1_IN1_7			Mux input channel 1 of TIM module 1
	QSPI4_MTSRB_F			Slave SPI data input
	ASCLIN6_ARXE			Receive input
	QSPI5_MRSTC			Master SPI data input
	GPT123_T2INA			Trigger/gate input of timer T2
	EGTM_TIM0_IN1_7			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_7			Mux input channel 1 of TIM module 1
	LETH0_P1_MII_RXDVB			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	LETH0_P1_RMII_CRSDVB			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	P22.0	O0		General-purpose output
	GTM_TOUT47	O1		GTM muxed output
	ASCLIN3_ATXN	O2		Differential Transmit output (low active)
	QSPI4_MTSR_F	O3		Master SPI data output
	QSPI4_SCLKN_F	O4		Master SPI clock output (LVDS N line)
	MSC1_FCLN	O5		Shift-clock inverted part of the differential signal
	—	O6		Reserved
	ASCLIN6_ATX	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT47	O9		eGTM muxed output
	ASCLIN4_ASCLK_F	O10		Shift clock output
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
P19	P22.1	I	LVDS_TX / FAST / PU1 /	General-purpose input
	GTM_TIM0_IN0_8			Mux input channel 0 of TIM module 0
	GTM_TIM1_IN0_8			Mux input channel 0 of TIM module 1

(table continues...)

Table 42 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI4_MRSTB_F		VDDEXT / ES6	Master SPI data input
	ASCLIN7_ARXE			Receive input
	GPT123_T2EUDA			Count direction control input of timer T2
	EGTM_TIM0_IN0_8			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_8			Mux input channel 0 of TIM module 1
	LETH0_P1_REFCLKB			LETH0 PortX RMII reference clock
	LETH0_P1_RXCLKB			LETH PortX MII receive clock
	P22.1	O0		General-purpose output
	GTM_TOUT48	O1		GTM muxed output
	ASCLIN3_ATXP	O2		Differential Transmit output (high active)
	QSPI4_MRST_F	O3		Slave SPI data output
	QSPI4_SCLKP_F	O4		Master SPI clock output
	MSC1_FCLP	O5		Shift-clock direct part of the differential signal
	QSPI5_SLSO9	O6		Master slave select output
	ASCLIN7_ATX	O7		Transmit output
	QSPI4_SLSO9	O8		Master slave select output
	EGTM_TOUT48	O9		eGTM muxed output
	ASCLIN4_ATX_F	O10		Transmit output
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
R20	P22.2	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	GTM_TIM0_IN3_7			Mux input channel 3 of TIM module 0
	GTM_TIM1_IN3_7			Mux input channel 3 of TIM module 1
	QSPI4_SLSIB_F			Slave select input
	ASCLIN4_ARXH_F			Receive input
	GPT123_T4EUDA			Count direction control input of timer T4
	LETH0_P1_COLA			LETH PortX MII collision detection
	LETH0_P1_MII_RXERC			LETH0 PortX MII receive error (to be used with LETH0_P1_RXCLKC)
	EGTM_TIM0_IN3_7			Mux input channel 3 of TIM module 0

(table continues...)

Table 42 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM1_IN3_7			Mux input channel 3 of TIM module 1
	P22.2	O0		General-purpose output
	GTM_TOUT49	O1		GTM muxed output
	ASCLIN5_ATX	O2		Transmit output
	QSPI4_SLSO3_F	O3		Master slave select output
	QSPI4_MTSRN_F	O4		Master SPI data output (LVDS N line)
	MSC1_SON	O5		Data output - inverted part of the differential signal
	QSPI5_MTSR	O6		Master SPI data output
	QSPI4_MTSR_F	O7		Master SPI data output
	—	O8		Reserved
	EGTM_TOUT49	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	LETH0_P1_MIIB_TXEN	O13		LETH0 PortX MII transmit enable (to be used with LETH0_P1_TXCLKB)
	—	O14		Reserved
	LETH0_P1_RMIIB_TXEN	O15		LETH0 PortX RMII transmit enable (to be used with LETH0_P1_REFCLKB)
	LETH0_P1_RMIIRB_TXEN	PO		LETH0 PortX RMII transmit enable (to be used with LETH0_P1_REFCLKB - registered*)
	HSCT1_TXDN	PO		Tx data
R19	P22.3	I	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose input
	GTM_TIM0_IN4_4			Mux input channel 4 of TIM module 0
	GTM_TIM1_IN4_4			Mux input channel 4 of TIM module 1
	QSPI4_SCLKB_F			Slave SPI clock inputs
	ASCLIN5_ARXC			Receive input
	GPT123_T5INA			Trigger/gate input of timer T5
	LETH0_P1_MII_RMII_RXD 0B			LETH0 PortX MII and RMII receive data bit 0 (to be used with LETH0_P1_RXCLKB or LETH0_P1_REFCLKB)
	EGTM_TIM0_IN4_4			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_4			Mux input channel 4 of TIM module 1
	LETH0_P1_REFCLKC			LETH0 PortX RMII reference clock
	LETH0_P1_RXCLKC			LETH PortX MII receive clock

(table continues...)

Table 42 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	P22.3	O0		General-purpose output
	GTM_TOUT50	O1		GTM muxed output
	QSPI5_SCLK	O2		Master SPI clock output
	QSPI4_SCLK_F	O3		Master SPI clock output
	QSPI4_MTSRP_F	O4		Master SPI data output
	MSC1_SOP	O5		Data output - direct part of the differential signal
	—	O6		Reserved
	ASCLIN7_ATX	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT50	O9		eGTM muxed output
	ASCLIN4_ASLSO_F	O10		Slave select signal output
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	HSCT1_TXDP	PO		Tx data
P16	P22.4	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM3_IN0_8			Mux input channel 0 of TIM module 3
	SCU_E_REQ5E			ERU channel 5 input E
	ASCLIN7_ARXF			Receive input
	GPT123_T5EUDA			Count direction control input of timer T5
	LETH0_P1_MII_RMII_RXD0C			LETH0 PortX MII and RMII receive data bit 0 (to be used with LETH0_P1_RXCLKC or LETH0_P1_REFCLKC)
	GTM_CDTM3_DTM4_1			Input mux of CDTM3_DTM4_AUXIN0/1
	GTM_CDTM3_DTM5_1			Input mux of CDTM3_DTM5_AUXIN0/1
	LETH0_P1_RXDH			LETH PortX TC14 interface receive data input
	P22.4	O0		General-purpose output
	GTM_TOUT130	O1		GTM muxed output
	ASCLIN4_ASCLK_F	O2		Shift clock output
	—	O3		Reserved
	QSPI0_SLSO12	O4		Master slave select output
	—	O5		Reserved

(table continues...)

Table 42 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CAN13_TXD	O6		CAN transmit output node 3
	QSPI6_SLSO15_F	O7		Master slave select output
	—	O8		Reserved
	EGTM_TOUT130	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
P17	P22.5	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM3_IN1_7			Mux input channel 1 of TIM module 3
	QSPI0_MTSRC			Slave SPI data input
	CAN13_RXDC			CAN receive input node 3
	GPT122_T3INB			Trigger/gate input of core timer T3 (input A, B and C)
	P22.5	O0		General-purpose output
	GTM_TOUT131	O1		GTM muxed output
	ASCLIN4_ATX_F	O2		Transmit output
	—	O3		Reserved
	QSPI0_MTSR	O4		Master SPI data output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT131	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 42 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
N16	P22.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM2_IN6_11			Mux input channel 6 of TIM module 2
	GTM_TIM3_IN2_6			Mux input channel 2 of TIM module 3
	QSPI0_MRSTC			Master SPI data input
	ASCLIN4_ARXC_F			Receive input
	GPT122_T3EUDB			Count direction control input of core timer T3
	LETH0_P1_CRSB			LETH PortX MII carrier sense
	EGTM_TIM2_IN6_11			Mux input channel 6 of TIM module 2
	LETH0_P1_MII_RXDVC			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	LETH0_P1_RMII_CRSDVC			MII receive data valid RXDV and RMII carrier sense and receive data valid CRSDV
	P22.6	O0		General-purpose output
	GTM_TOUT132	O1		GTM muxed output
	ASCLIN4_ASLSO_F	O2		Slave select signal output
	—	O3		Reserved
	QSPI0_MRST	O4		Slave SPI data output
	CAN21_TXD	O5		CAN transmit output node 1
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT132	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
N17	P22.7	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM3_IN3_7			Mux input channel 3 of TIM module 3
	QSPI0_SCLKC			Slave SPI clock inputs
	CAN21_RXDF			CAN receive input node 1
	GPT122_T4INB			Trigger/gate input of timer T4

(table continues...)

Table 42 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_TXCLKB			LETH PortX MII transmit clock
	LETH0_P1_TXCLKC			LETH PortX MII transmit clock
	P22.7	O0		General-purpose output
	GTM_TOUT133	O1		GTM muxed output
	ASCLIN4_ASCLK	O2		Shift clock output
	—	O3		Reserved
	QSPI0_SCLK	O4		Master SPI clock output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT133	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
M16	P22.8	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM3_IN4_7			Mux input channel 4 of TIM module 3
	GTM_TIM5_IN0_4			Mux input channel 0 of TIM module 5
	QSPI0_SCLKB			Slave SPI clock inputs
	GPT122_T5INB			Trigger/gate input of timer T5
	LETH0_P1_COLC			LETH PortX MII collision detection
	LETH0_P1_RXDE			LETH PortX TC14 interface receive data input
	P22.8	O0		General-purpose output
	GTM_TOUT134	O1		GTM muxed output
	ASCLIN5_ASCLK	O2		Shift clock output
	—	O3		Reserved
	QSPI0_SCLK	O4		Master SPI clock output
	CAN22_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	—	O7		Reserved

(table continues...)

Table 42 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O8		Reserved
	EGTM_TOUT134	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
M17	P22.9	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM3_IN5_7			Mux input channel 5 of TIM module 3
	GTM_TIM5_IN1_10			Mux input channel 1 of TIM module 5
	QSPI0_MRSTB			Master SPI data input
	ASCLIN4_ARXD_F			Receive input
	CAN22_RXDE			CAN receive input node 2
	LETH0_P1_EDE			LETH PortX TC14 interface energy detection input
	GPT122_T5EUDB			Count direction control input of timer T5
	GTM_CDTM3_DTM4_2			Input mux of CDTM3_DTM4_AUXIN0/1
	GTM_CDTM3_DTM5_2			Input mux of CDTM3_DTM5_AUXIN0/1
	LETH0_P1_MDIOE			LETH PortX MDIO interface data input
	P22.9	O0		General-purpose output
	GTM_TOUT135	O1		GTM muxed output
	GPT122_T6OUT	O2		External output for overflow/underflow detection of core timer T6
	—	O3		Reserved
	QSPI0_MRST	O4		Slave SPI data output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT135	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 42 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_MIIC_TXD1	O11		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P1_TXCLKC)
	LETH0_P1_RMIIC_TXD1	O12		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P1_REFCLKC)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_RMIIRC_TXD1	PO		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P1_REFCLKC - registered*)
	LETH0_P1_MDIO	O		LETH PortX MDIO interface data output combined with energy detection input (ED) of TC14 interface
L16	P22.10	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM3_IN6_7			Mux input channel 6 of TIM module 3
	GTM_TIM5_IN2_8			Mux input channel 2 of TIM module 5
	QSPI0_MTSRB			Slave SPI data input
	GPT122_T6INB			Trigger/gate input of core timer T6
	P22.10	O0		General-purpose output
	GTM_TOUT136	O1		GTM muxed output
	ASCLIN4_ATX_F	O2		Transmit output
	—	O3		Reserved
	QSPI0_MTSR	O4		Master SPI data output
	CAN23_TXD	O5		CAN transmit output node 3
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT136	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P1_MIIC_TXD0	O11		LETH0 PortX MII transmit data bit 0 (to be used with LETH0_P1_TXCLKC)
	LETH0_P1_RMIIC_TXD0	O12		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P1_REFCLKC)
	—	O13		Reserved
	—	O14		Reserved
	LETH0_P1_TXD	O15		LETH PortX TC14 interface transmit data output

(table continues...)

Table 42 (continued) Port 22 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_RMIIRC_TXD0	PO		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P1_REFCLKC - registered*)
L17	P22.11	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM3_IN7_7			Mux input channel 7 of TIM module 3
	GTM_TIM5_IN3_10			Mux input channel 3 of TIM module 5
	CAN23_RXDE			CAN receive input node 3
	GPT122_T6EUDB			Count direction control input of core timer T6
	LETH0_P1_MII_RXD3B			LETH0 PortX MII receive data bit 3 (to be used with LETH0_P1_RXCLKB)
	P22.11	O0		General-purpose output
	GTM_TOUT137	O1		GTM muxed output
	ASCLIN4_ASLSO_F	O2		Slave select signal output
	—	O3		Reserved
	QSPI0_SLSO10	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT137	O9		eGTM muxed output
	—	O10		Reserved
	LETH0_P1_MIIC_TXEN	O11		LETH0 PortX MII transmit enable (to be used with LETH0_P1_TXCLKC)
	LETH0_P1_RMIIC_TXEN	O12		LETH0 PortX RMII transmit enable (to be used with LETH0_P1_REFCLKC)
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_RMIIRC_TXEN	PO		LETH0 PortX RMII transmit enable (to be used with LETH0_P1_REFCLKC - registered*)

3.3.13 BGA292_STD port 23

Table 43 Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
V20	P23.0	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN5_4			Mux input channel 5 of TIM module 0
	GTM_TIM1_IN5_4			Mux input channel 5 of TIM module 1
	GTM_TIM6_IN7_1			Mux input channel 7 of TIM module 6
	CAN10_RXDC			CAN receive input node 0
	QSPI6_SLSID_F			Slave select input
	EGTM_TIM0_IN5_4			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_4			Mux input channel 5 of TIM module 1
	P23.0	O0		General-purpose output
	GTM_TOUT41	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	QSPI6_SCLK	O7		Master SPI clock output
	QSPI6_MTSR	O8		Master SPI data output
	EGTM_TOUT41	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P1_MIIB_TXER	O12		LETH0 PortX MII transmit error (to be used with LETH0_P1_TXCLKB)
	LETH0_P1_MIIC_TXER	O13		LETH0 PortX MII transmit error (to be used with LETH0_P1_TXCLKC)
	—	O14		Reserved
	—	O15		Reserved
U19	P23.1	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN6_4			Mux input channel 6 of TIM module 0
	GTM_TIM1_IN6_4			Mux input channel 6 of TIM module 1
	GTM_TIM6_IN6_1			Mux input channel 6 of TIM module 6
	MSC1_SDIO			Upstream asynchronous input signal
	ASCLIN6_ARXF_F			Receive input

(table continues...)

Table 43 (continued) Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GPT123_CAPINA			Trigger input to capture value of timer T5 into CAPREL register (input A)
	SCU_E_REQ6F			ERU channel 6 input F
	ADC_TRIG61			Triggers from PORTS to ADC
	QSPI0_MRSTD			Master SPI data input
	LETH0_P1_MII_RMII_RXD1B			LETH0 PortX MII and RMII receive data bit 1 (to be used with LETH0_P1_RXCLKB or LETH0_P1_REFCLKB)
	EGTM_TIM0_IN6_4			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN6_4			Mux input channel 6 of TIM module 1
	LETH0_P1_RXDG			LETH PortX TC14 interface receive data input
	P23.1	O0		General-purpose output
	GTM_TOUT42	O1		GTM muxed output
	ASCLIN1_ARTS	O2		Ready to send output
	QSPI4_SLSO6_F	O3		Master slave select output
	GTM_ECLK0	O4		CGM generated clock
	CAN10_TXD	O5		CAN transmit output node 0
	CLOCK_EXTCLK0	O6		External clock output 0
	ASCLIN6_ASCLK_F	O7		Shift clock output
	QSPI6_MTSR_F	O8		Master SPI data output
	EGTM_TOUT42	O9		eGTM muxed output
	EGTM_ECLK0	O10		CGM generated clock
	—	O11		Reserved
	QSPI6_SCLK_F	O12		Master SPI clock output
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	LETH0_P1_RXMDC	O		LETH PortX MDIO interface clock output combined with receive data input (RX) of TC14 interface
U20	P23.2	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN6_5			Mux input channel 6 of TIM module 0
	GTM_TIM1_IN6_5			Mux input channel 6 of TIM module 1
	GTM_TIM6_IN5_1			Mux input channel 5 of TIM module 6
	ASCLIN7_ARXC			Receive input
	QSPI6_MRSTE_F			Master SPI data input

(table continues...)

Table 43 (continued) Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM0_IN6_5			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN6_5			Mux input channel 6 of TIM module 1
	P23.2	O0		General-purpose output
	GTM_TOUT43	O1		GTM muxed output
	—	O2		Reserved
	ASCLIN6_ASCLK_F	O3		Shift clock output
	CAN23_TXD	O4		CAN transmit output node 3
	CAN12_TXD	O5		CAN transmit output node 2
	CAN10_TXD	O6		CAN transmit output node 0
	QSPI6_SCLK_F	O7		Master SPI clock output
	QSPI6_SLSO3_F	O8		Master slave select output
	EGTM_TOUT43	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P1_MIIB_TXD3	O12		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P1_TXCLKB)
	LETH0_P1_MIIC_TXD3	O13		LETH0 PortX MII transmit data bit 3 (to be used with LETH0_P1_TXCLKC)
	—	O14		Reserved
	QSPI6_MTSR_F	O15		Master SPI data output
T19	P23.3	I	SLOW / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN7_4			Mux input channel 7 of TIM module 0
	GTM_TIM1_IN7_4			Mux input channel 7 of TIM module 1
	GTM_TIM6_IN4_2			Mux input channel 4 of TIM module 6
	MSC1_INJ0			Injection signal from port
	ASCLIN6_ARXA_F			Receive input
	CAN12_RXDC			CAN receive input node 2
	CAN23_RXDB			CAN receive input node 3
	GPT122_CAPINB3			Trigger input to capture value of timer T5 into CAPREL register (input B)
	QSPI6_MTSRB_F			Slave SPI data input
	EGTM_TIM0_IN7_4			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_4			Mux input channel 7 of TIM module 1
	P23.3	O0		General-purpose output

(table continues...)

Table 43 (continued) Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TOUT44	O1		GTM muxed output
	ASCLIN7_ATX	O2		Transmit output
	—	O3		Reserved
	CAN23_TXD	O4		CAN transmit output node 3
	CAN12_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	QSPI6_SLSO0	O7		Master slave select output
	QSPI6_SCLK	O8		Master SPI clock output
	EGTM_TOUT44	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P1_MIIB_TXD2	O12		LETH0 PortX MII transmit data bit 2 (to be used with LETH0_P1_TXCLKB)
	LETH0_P1_MIIC_TXD2	O13		LETH0 PortX MII transmit data bit 2 (to be used with LETH0_P1_TXCLKC)
	—	O14		Reserved
	—	O15		Reserved
T20	P23.4	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN7_5			Mux input channel 7 of TIM module 0
	GTM_TIM1_IN7_5			Mux input channel 7 of TIM module 1
	GTM_TIM6_IN3_2			Mux input channel 3 of TIM module 6
	QSPI6_MRSTD_F			Master SPI data input
	EGTM_TIM0_IN7_5			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_5			Mux input channel 7 of TIM module 1
	P23.4	O0		General-purpose output
	GTM_TOUT45	O1		GTM muxed output
	ASCLIN6_ASLSO_F	O2		Slave select signal output
	QSPI4_SLSO5_F	O3		Master slave select output
	—	O4		Reserved
	MSC1_EN0	O5		Chip Select
	—	O6		Reserved
	—	O7		Reserved
	QSPI6_SLSO1_F	O8		Master slave select output

(table continues...)

Table 43 (continued) Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TOUT45	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P1_MIIB_TXD1	O12		LETH0 PortX MII transmit data bit 1 (to be used with LETH0_P1_TXCLKB)
	—	O13		Reserved
	LETH0_P1_RMIIB_TXD1	O14		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P1_REFCLKB)
	QSPI6_MTSR_F	O15		Master SPI data output
	LETH0_P1_RMIIRB_TXD1	PO		LETH0 PortX RMII transmit data bit 1 (to be used with LETH0_P1_REFCLKB - registered*)
T17	P23.5	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM0_IN2_7			Mux input channel 2 of TIM module 0
	GTM_TIM1_IN2_7			Mux input channel 2 of TIM module 1
	GTM_TIM6_IN2_2			Mux input channel 2 of TIM module 6
	LETH0_P1_MII_RXD3C			LETH0 PortX MII receive data bit 3 (to be used with LETH0_P1_RXCLKC)
	EGTM_TIM0_IN2_7			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_7			Mux input channel 2 of TIM module 1
	P23.5	O0		General-purpose output
	GTM_TOUT46	O1		GTM muxed output
	ASCLIN6_ATX_F	O2		Transmit output
	QSPI4_SLSO4_F	O3		Master slave select output
	—	O4		Reserved
	MSC1_EN1	O5		Chip Select
	CAN22_TXD	O6		CAN transmit output node 2
	—	O7		Reserved
	QSPI6_SLSO2_F	O8		Master slave select output
	EGTM_TOUT46	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	LETH0_P1_MIIB_TXD0	O12		LETH0 PortX MII transmit data bit 0 (to be used with LETH0_P1_TXCLKB)
	—	O13		Reserved

(table continues...)

Table 43 (continued) Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_RMIIB_TXD0	O14		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P1_REFCLKB)
	LETH0_P1_TXD	O15		LETH PortX TC14 interface transmit data output
	LETH0_P1_RMIIRB_TXD0	PO		LETH0 PortX RMII transmit data bit 0 (to be used with LETH0_P1_REFCLKB - registered*)
R17	P23.6	I	FAST / PU1 / VDDEXT / ES	General-purpose input
	GTM_TIM1_IN2_10			Mux input channel 2 of TIM module 1
	GTM_TIM4_IN2_7			Mux input channel 2 of TIM module 4
	GTM_TIM6_IN1_2			Mux input channel 1 of TIM module 6
	CAN22_RXDC			CAN receive input node 2
	QSPI6_MRSTA_F			Master SPI data input
	LETH0_P1_MII_RXD2B			LETH0 PortX MII receive data bit 2 (to be used with LETH0_P1_RXCLKB)
	LETH0_P1_MII_RXD2C			LETH0 PortX MII receive data bit 2 (to be used with LETH0_P1_RXCLKC)
	EGTM_TIM1_IN2_10			Mux input channel 2 of TIM module 1
	P23.6	O0		General-purpose output
	GTM_TOUT138	O1		GTM muxed output
	—	O2		Reserved
	ASCLIN6_ASLSO_F	O3		Slave select signal output
	QSPI0_SLSO11	O4		Master slave select output
	CAN11_TXD	O5		CAN transmit output node 1
	—	O6		Reserved
	QSPI6_SLSO14_F	O7		Master slave select output
	QSPI6_MRST_F	O8		Slave SPI data output
	EGTM_TOUT138	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	QSPI6_MTSR_F	O15		Master SPI data output
R16	P23.7	I	SLOW / PU1 /	General-purpose input
	GTM_TIM1_IN3_10			Mux input channel 3 of TIM module 1

(table continues...)

Table 43 (continued) Port 23 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TIM4_IN3_7		VDDEXT / ES	Mux input channel 3 of TIM module 4
	GTM_TIM6_IN0_2			Mux input channel 0 of TIM module 6
	CAN11_RXDC			CAN receive input node 1
	QSPI6_SCLKA_F			Slave SPI clock inputs
	LETH0_P1_MII_RMII_RXD1C			LETH0 PortX MII and RMII receive data bit 1 (to be used with LETH0_P1_RXCLKC or LETH0_P1_REFCLKC)
	EGTM_TIM1_IN3_10			Mux input channel 3 of TIM module 1
	P23.7	O0		General-purpose output
	GTM_TOUT139	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	QSPI6_SCLK	O8		Master SPI clock output
	EGTM_TOUT139	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

3.3.14 BGA292_STD port 32

Table 44 Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
W18	P32.2	I	FAST / PU1 / VDDEVRS B / ES	General-purpose input
	GTM_TIM0_IN3_8			Mux input channel 3 of TIM module 0
	GTM_TIM1_IN3_8			Mux input channel 3 of TIM module 1
	CAN03_RXDB			CAN receive input node 3
	ASCLIN3_ARXD			Receive input

(table continues...)

Table 44 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CAN21_RXDD			CAN receive input node 1
	SMU_FSPIN2			FSP Status Input - Shows the actual state of the FSP ErroPin
	EGTM_TIM0_IN3_8			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_8			Mux input channel 3 of TIM module 1
	UART_RXDH	I#		Receive input H
	WCAN_RXDF			Wake-up input F
	T0D			T0 capture input D
	T21EXG			T21 interrupt input G
	EXINT7			Interrupt 7 input
	P32.2	O0		General-purpose output
	GTM_TOUT38	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	PMS_DCDCSYNCO	O6		DC-DC synchronization output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT38	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P2.0	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_4	O#5		T2 PWM channel 04
	—	O#6		Reserved
	—	O#7		Reserved

(table continues...)

Table 44 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	SMU_FSP2	O		FSP Output Signal - Generated by SMU
W17	P32.4	I	FAST / PU1 / VDDEVRS B / ES	General-purpose input
	GTM_TIM0_IN5_5			Mux input channel 5 of TIM module 0
	GTM_TIM1_IN5_5			Mux input channel 5 of TIM module 1
	ASCLIN1_ACTSB			Clear to send input
	MSC1_SDI2			Upstream asynchronous input signal
	I2C0_SCLD			Serial Clock Input 3
	EGTM_TIM0_IN5_5			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_5			Mux input channel 5 of TIM module 1
	SSC_MRSTD	I#		Master SPI data input D
	T21EXA			T21 interrupt input A
	T2CCU1_0A			T2 capture 1 input 0A
	EXINT8A			Interrupt 8 input A
	EXINT12A			Interrupt 12 input A
	I2CSCLA			Serial clock input A
	P32.4	O0		General-purpose output
	GTM_TOUT40	O1		GTM muxed output
	ASCLIN6_ATX	O2		Transmit output
	CAN03_TXD	O3		CAN transmit output node 3
	GTM_ECLK1	O4		CGM generated clock
	MSC1_EN0	O5		Chip Select
	CLOCK_EXTCLK1	O6		External clock output 1
	CAN21_TXD	O7		CAN transmit output node 1
	I2C0_SCL	O8		Serial Clock Output
	EGTM_TOUT40	O9		eGTM muxed output

(table continues...)

Table 44 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_ECLK1	O10		CGM generated clock
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P2.1	O#0		General-purpose output
	—	O#1		Reserved
	SSC_MRST	O#2		Slave SPI data output
	T20EXF2	O#3		Timer 20 external overflow
	—	O#4		Reserved
	T2CCU0_5	O#5		T2 PWM channel 05
	T2CCU1_0	O#6		T2 PWM channel 10
	I2CSCL	O#7		Serial clock output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
		PMS_DCDCSYNCO		O
T15	P32.5	I	FAST / PU1 / VDDEVRS B / ES	General-purpose input
	GTM_TIM3_IN5_8			Mux input channel 5 of TIM module 3
	GTM_TIM4_IN1_14			Mux input channel 1 of TIM module 4
	GTM_TIM5_IN5_9			Mux input channel 5 of TIM module 5
	SENT0_SENT5C			Receive input channel 5
	SMU_FSPIN3			FSP Status Input - Shows the actual state of the FSP ErroPin
	EGTM_TIM0_IN4_5			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_5			Mux input channel 4 of TIM module 1
	SSC_MTSRD	I#		Slave SPI data input D
	PINRSTC			Reset input C

(table continues...)

Table 44 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	T20EXO			T20 interrupt input O
	T2CCU1_1A			T2 capture 1 input 1A
	EXINT9A			Interrupt 9 input A
	EXINT13A			Interrupt 13 input A
	P32.5	O0		General-purpose output
	GTM_TOUT140	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	SENT0_SPC5	O3		Transmit output
	ASCLIN5_ASLSO_F	O4		Slave select signal output
	—	O5		Reserved
	CAN02_TXD	O6		CAN transmit output node 2
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT140	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P2.2	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	SSC_MTSR	O#2		Master SPI data output
	—	O#3		Reserved
	T21EXF2	O#4		Timer 21 external overflow
	—	O#5		Reserved
	T2CCU1_1	O#6		T2 PWM channel 11
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved

(table continues...)

Table 44 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	SMU_FSP3	O		FSP Output Signal - Generated by SMU
U15	P32.6	I	SLOW / PU1 / VDDEVRS B / ES	General-purpose input
	GTM_TIM3_IN6_8			Mux input channel 6 of TIM module 3
	GTM_TIM4_IN4_15			Mux input channel 4 of TIM module 4
	GTM_TIM5_IN6_9			Mux input channel 6 of TIM module 5
	CAN02_RXDC			CAN receive input node 2
	CBS_TGI4			Trigger input
	ASCLIN2_ARXF			Receive input
	ASCLIN6_ARXC			Receive input
	SENT1_SENT5C			Receive input channel 5
	I2C0_SDAD			Serial Data Input 3
	UART_RXDI	I#		Receive input I
	T1D			T1 capture input D
	T21A			T21 capture input A
	T2CCU1_2A			T2 capture 1 input 2A
	EXINT10A			Interrupt 10 input A
	EXINT14A			Interrupt 14 input A
	I2CSDA			Serial data input A
	P32.6	O0		General-purpose output
	GTM_TOUT141	O1		GTM muxed output
	—	O2		Reserved
	SENT1_SPC5	O3		Transmit output
	—	O4		Reserved
	CAN22_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	—	O7		Reserved
	I2C0_SDA	O8		Serial Data Output
	EGTM_TOUT141	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved

(table continues...)

Table 44 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	LETH0_P1_PPS	O12		LETH PortX Pulse Per Second Signal from Precision Time Protocol
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P2.3	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional receive pin O
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	—	O#5		Reserved
	T2CCU1_2	O#6		T2 PWM channel 12
	I2CSDA	O#7		Serial data output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	CBS_TGO4	O		Trigger output
U16	P32.7	I	SLOW / PU1 / VDDEVRS B / ES	General-purpose input
	GTM_TIM3_IN7_8			Mux input channel 7 of TIM module 3
	GTM_TIM4_IN0_15			Mux input channel 0 of TIM module 4
	GTM_TIM5_IN7_8			Mux input channel 7 of TIM module 5
	CBS_TGI5			Trigger input
	CAN22_RXDB			CAN receive input node 2
	SENT0_SENT6C			Receive input channel 6
	ADC_SIGN0			Sign for Carrier Cancellation
	LETH0_P1_MII_RXERB			LETH0 PortX MII receive error (to be used with LETH0_P1_RXCLKB)
	WCAN_RXDH	I#		Wake-up input H

(table continues...)

Table 44 (continued) Port 32 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	T20EXH			T20 interrupt input H
	T2CCU1_3A			T2 capture 1 input 3A
	EXINT11A			Interrupt 11 input A
	EXINT15A			Interrupt 15 input A
	P32.7	O0		General-purpose output
	GTM_TOUT142	O1		GTM muxed output
	ASCLIN6_ATX	O2		Transmit output
	SENT0_SPC6	O3		Transmit output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT142	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P2.4	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	—	O#5		Reserved
	T2CCU1_3	O#6		T2 PWM channel 13
	PMSRTC32_OUT	O#7		RTC oscillator output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved

(table continues...)

Table 44 (continued) **Port 32 functions**

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	CBS_TGO5	O		Trigger output

3.3.15 BGA292_STD port 33

Table 45 **Port 33 functions**

Ball	Symbol	Ctrl.	Buffer type	Function
W10	P33.0	I	SLOW / PU1 / VDDEVRS B / ES5	General-purpose input
	GTM_TIM0_IN4_6			Mux input channel 4 of TIM module 0
	GTM_TIM1_IN4_6			Mux input channel 4 of TIM module 1
	GTM_TIM3_IN0_14			Mux input channel 0 of TIM module 3
	SENT1_SENT9B			Receive input channel 9
	GPT122_T6INA			Trigger/gate input of core timer T6
	GTM_CDTM1_DTM0_3			Input mux of CDTM1_DTM0_AUXIN0/1
	GTM_CDTM1_DTM1_3			Input mux of CDTM1_DTM1_AUXIN0/1
	EGTM_CDTM1_DTM0_3			Input mux of CDTM1_DTM0_AUXIN0/1
	EGTM_CDTM1_DTM1_3			Input mux of CDTM1_DTM1_AUXIN0/1
	EGTM_CDTM1_DTM2_3			Input mux of CDTM1_DTM2_AUXIN0/1
	EGTM_CDTM1_DTM3_3			Input mux of CDTM1_DTM3_AUXIN0/1
	EGTM_TIM0_IN4_6			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_6			Mux input channel 4 of TIM module 1
	T21EXB	I#		T20 interrupt input B
	T2CCU0_0A			T2 capture 0 input 0A
	EXINT3A			Interrupt 3 input A
	EXINT12B			Interrupt 12 input B
	ADCOMPCH0			Analog input channel 0
	ADC_TMADC4CH10	AI		Analog Input for TMADC4 Channel 10
	P33.0	O0		General-purpose output
	GTM_TOUT22	O1		GTM muxed output
	ASCLIN5_ATX	O2		Transmit output
	SENT1_SPC9	O3		Transmit output

(table continues...)

Table 45 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O4		Reserved
	ADC_EMUXCTRL03	O5		EMUX0 Control from TMADC to PORTS
	ADC_BFL2	O6		Boundary flags from FCC
	PSI5S1_TX	O7		TX data output
	—	O8		Reserved
	EGTM_TOUT22	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.0	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_0	O#5		T2 PWM channel 00
	T2CCU1_4	O#6		T2 PWM channel 14
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
Y10	P33.1	I	SLOW / PU1 / VDDEVRS B / ES5	General-purpose input
	GTM_TIM0_IN5_6			Mux input channel 5 of TIM module 0
	GTM_TIM1_IN5_6			Mux input channel 5 of TIM module 1
	GTM_TIM3_IN1_14			Mux input channel 1 of TIM module 3
	PSI5_RX0C			RXD inputs (receive data) channel 0

(table continues...)

Table 45 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ADC_CLKIN2			Clock input to EXMOD
	SENT0_SENT9B			Receive input channel 9
	GPT122_CAPINA			Trigger input to capture value of timer T5 into CAPREL register (input A)
	EGTM_TIM0_IN5_6			Mux input channel 5 of TIM module 0
	EGTM_TIM1_IN5_6			Mux input channel 5 of TIM module 1
	UART_RXDK	I#		Receive input K
	SSC_SCLKD			Slave SPI clock input D
	T0A			T0 capture input A
	T20EXA			T2 interrupt input A
	T2CCU0_1A			T2 capture 0 input 1A
	EXINT4A			Interrupt 4 input A
	EXINT13B			Interrupt 13 input B
	ADCOMPCH1			Analog input channel 1
	ADC_TMADC4CH9	AI		Analog Input for TMADC4 Channel 9
	P33.1	O0		General-purpose output
	GTM_TOUT23	O1		GTM muxed output
	ASCLIN3_ASLSO	O2		Slave select signal output
	QSPI2_SCLK	O3		Master SPI clock output
	ADC_CLKOUT1	O4		Clock output from EXMOD
	ADC_EMUXCTRL02	O5		EMUX0 Control from TMADC to PORTS
	ADC_BFL4	O6		Boundary flags from FCC
	SENT0_SPC9	O7		Transmit output
	PSI5S1_CLK	O8		PSI5S CLK is a clock that can be used on a pin to drive the external PHY.
	EGTM_TOUT23	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.1	O#0		General-purpose output

(table continues...)

Table 45 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	UART_RXDO	O#1		Bidirectional receive pin O
	SSC_SCLK	O#2		Clock output
	—	O#3		Reserved
	T21EXF2	O#4		Timer 21 external overflow
	T2CCU0_1	O#5		T2 PWM channel 01
	T2CCU1_5	O#6		T2 PWM channel 15
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
W11	P33.2	I	SLOW / PU1 / VDDEVRS B / ES5	General-purpose input
	GTM_TIM0_IN6_6			Mux input channel 6 of TIM module 0
	GTM_TIM1_IN6_6			Mux input channel 6 of TIM module 1
	GTM_TIM3_IN2_13			Mux input channel 2 of TIM module 3
	SENT1_SENT8B			Receive input channel 8
	ADC_DATA2			Modulated data to EXMOD
	GPT120_CAPINB3			Trigger input to capture value of timer T5 into CAPREL register (input B)
	EGTM_TIM0_IN6_6			Mux input channel 6 of TIM module 0
	EGTM_TIM1_IN6_6			Mux input channel 6 of TIM module 1
	WCAN_RXDE	I#		Wake-up input E
	SCRDAP0_1			SCRDAP0 input
	T21B			T21 capture input B
	T2CCU0_2A			T2 capture 0 input 2A
	EXINT5A			Interrupt 5 input A
	EXINT14B			Interrupt 14 input B
	ADCOMPCH2			Analog input channel 2
	ADC_TMADC4CH8	AI		Analog Input for TMADC4 Channel 8

(table continues...)

Table 45 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	P33.2	O0		General-purpose output
	GTM_TOUT24	O1		GTM muxed output
	ASCLIN3_ASCLK	O2		Shift clock output
	QSPI2_SLSO10	O3		Master slave select output
	PSI5_TX0	O4		TXD outputs (send data)
	ADC_EMUXCTRL01	O5		EMUX0 Control from TMADC to PORTS
	ADC_BFL3	O6		Boundary flags from FCC
	—	O7		Reserved
	SENT1_SPC8	O8		Transmit output
	EGTM_TOUT24	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	GPT122_T3OUT	O12		External output for overflow/underflow detection of core timer T3
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.2	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	—	O#2		Reserved
	T20EXF2	O#3		Timer 20 external overflow
	—	O#4		Reserved
	T2CCU0_2	O#5		T2 PWM channel 02
	—	O#6		Reserved
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved

(table continues...)

Table 45 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
Y11	P33.3	I	SLOW / PU1 / VDDEVRS B / ES5	General-purpose input
	GTM_TIM0_IN7_6			Mux input channel 7 of TIM module 0
	GTM_TIM1_IN7_6			Mux input channel 7 of TIM module 1
	GTM_TIM3_IN3_13			Mux input channel 3 of TIM module 3
	PSI5_RX1C			RXD inputs (receive data) channel 1
	SENT0_SENT8B			Receive input channel 8
	ADC_CLKIN1			Clock input to EXMOD
	EGTM_TIM0_IN7_6			Mux input channel 7 of TIM module 0
	EGTM_TIM1_IN7_6			Mux input channel 7 of TIM module 1
	UART_RXDP	I#		Receive input P
	T20A			T20 capture input A
	T2CCU0_3A			T2 capture 0 input 3A
	EXINT6A			Interrupt 6 input A
	EXINT15B			Interrupt 15 input B
	ADCOMPCH3			Analog input channel 3
	ADC_TMADC4CH7	AI		Analog Input for TMADC4 Channel 7
	P33.3	O0		General-purpose output
	GTM_TOUT25	O1		GTM muxed output
	ASCLIN5_ASCLK	O2		Shift clock output
	QSPI4_SLSO2	O3		Master slave select output
	ADC_CLKOUT2	O4		Clock output from EXMOD
	ADC_EMUXCTRL00	O5		EMUX0 Control from TMADC to PORTS
	ADC_BFL5	O6		Boundary flags from FCC
	—	O7		Reserved
	SENT0_SPC8	O8		Transmit output
	EGTM_TOUT25	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	GPT122_T6OUT	O12		External output for overflow/underflow detection of core timer T6
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved

(table continues...)

Table 45 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SCR_P0.3	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional receive pin O
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_3	O#5		T2 PWM channel 03
	—	O#6		Reserved
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	SCRDAP1_1	I/O		SCRDAP1 input
	SPD_1	I/O		Single pin DAP1
W12	P33.4	I	SLOW / PU1 / VDDEVRS B / ES5	General-purpose input
	GTM_TIM0_IN0_10			Mux input channel 0 of TIM module 0
	GTM_TIM1_IN0_10			Mux input channel 0 of TIM module 1
	GTM_TIM4_IN4_10			Mux input channel 4 of TIM module 4
	SENT1_SENT7B			Receive input channel 7
	ADC_DATA1			Modulated data to EXMOD
	ASCLIN5_ARXB_F			Receive input
	GTM_CDTM2_DTM0_1			Input mux of CDTM2_DTM0_AUXIN0/1
	GTM_CDTM2_DTM1_1			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_CDTM2_DTM0_1			Input mux of CDTM2_DTM0_AUXIN0/1
	EGTM_CDTM2_DTM1_1			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_CDTM2_DTM2_1			Input mux of CDTM2_DTM2_AUXIN0/1
	EGTM_CDTM2_DTM3_1			Input mux of CDTM2_DTM3_AUXIN0/1
	EGTM_TIM0_IN0_10			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_10			Mux input channel 0 of TIM module 1

(table continues...)

Table 45 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	UART_RXDC	I#		Receive input C
	WCAN_RXDP			Wake-up input P
	T1B			T1 capture input B
	T2CCU0_3D			T2 capture 0 input 3D
	EXINT0A			Interrupt 0 input A
	EXINT6D			Interrupt 6 input D
	EXINT12C			Interrupt 12 input C
	ADCOMPCH4			Analog input channel 4
	ADC_TMADC4CH6	AI		Analog Input for TMADC4 Channel 6
	P33.4	O0		General-purpose output
	GTM_TOUT26	O1		GTM muxed output
	ASCLIN2_ARTS	O2		Ready to send output
	QSPI2_SLS012	O3		Master slave select output
	PSI5_TX1	O4		TXD outputs (send data)
	ADC_EMUXCTRL12	O5		EMUX1 Control from TMADC to PORTS
	ADC_BFL0	O6		Boundary flags from FCC
	CAN13_TXD	O7		CAN transmit output node 3
	SENT1_SPC7	O8		Transmit output
	EGTM_TOUT26	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.4	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional receive pin O
	—	O#2		Reserved
	—	O#3		Reserved
	T21EXF2	O#4		Timer 21 external overflow
	T2CCU0_4	O#5		T2 PWM channel 04
	—	O#6		Reserved
	—	O#7		Reserved

(table continues...)

Table 45 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
Y12	P33.5	I	SLOW / PU1 / VDDEVRS B / ES5	General-purpose input
	GTM_TIM0_IN1_8			Mux input channel 1 of TIM module 0
	GTM_TIM1_IN1_8			Mux input channel 1 of TIM module 1
	GTM_TIM4_IN5_10			Mux input channel 5 of TIM module 4
	ADC_CLKIN0			Clock input to EXMOD
	GPT120_T4EUDB			Count direction control input of timer T4
	PSI5S0_RXC			RX data input
	ASCLIN2_ACTSB			Clear to send input
	PSI5_RX2C			RXD inputs (receive data) channel 2
	SENT1_SENT2C			Receive input channel 2
	CAN13_RXDB			CAN receive input node 3
	QSPI4_MRSTG			Master SPI data input
	EGTM_TIM0_IN1_8			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_8			Mux input channel 1 of TIM module 1
	WCAN_RXDD	I#		Wake-up input D
	SSC_MRSTA			Master SPI data input A
	T0B			T0 capture input B
	T20EXB			T20 interrupt input B
	EXINT1A			Interrupt 1 input A
	EXINT13C			Interrupt 13 input C
	ADCOMPCH5			Analog input channel 5
	ADC_TMADC4CH5	AI		Analog Input for TMADC4 Channel 5
	P33.5	O0		General-purpose output
	GTM_TOUT27	O1		GTM muxed output
	QSPI0_SLSO7	O2		Master slave select output

(table continues...)

Table 45 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI1_SLS07	O3		Master slave select output
	ADC_CLKOUT3	O4		Clock output from EXMOD
	ADC_EMUXCTRL11	O5		EMUX1 Control from TMADC to PORTS
	ADC_BFL2	O6		Boundary flags from FCC
	ASCLIN5_ASLSO	O7		Slave select signal output
	—	O8		Reserved
	EGTM_TOUT27	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.5	O#0		General-purpose output
	—	O#1		Reserved
	SSC_MRST	O#2		Slave SPI data output
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_5	O#5		T2 PWM channel 05
	—	O#6		Reserved
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
W13	P33.6	I	SLOW / PU1 / VDDEVRS B / ES5	General-purpose input
	GTM_TIM0_IN2_9			Mux input channel 2 of TIM module 0
	GTM_TIM1_IN2_9			Mux input channel 2 of TIM module 1
	GPT120_T2EUDB			Count direction control input of timer T2

(table continues...)

Table 45 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SENT0_SENT12B			Receive input channel 12
	ADC_DATA0			Modulated data to EXMOD
	GPT122_T2INA			Trigger/gate input of timer T2
	GTM_CDTM2_DTM0_2			Input mux of CDTM2_DTM0_AUXIN0/1
	GTM_CDTM2_DTM1_2			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_CDTM2_DTM0_2			Input mux of CDTM2_DTM0_AUXIN0/1
	EGTM_CDTM2_DTM1_2			Input mux of CDTM2_DTM1_AUXIN0/1
	EGTM_CDTM2_DTM2_2			Input mux of CDTM2_DTM2_AUXIN0/1
	EGTM_CDTM2_DTM3_2			Input mux of CDTM2_DTM3_AUXIN0/1
	EGTM_TIM0_IN2_9			Mux input channel 2 of TIM module 0
	EGTM_TIM1_IN2_9			Mux input channel 2 of TIM module 1
	UART_RXDL	I#		Receive input L
	SSC_MTSRA			Slave SPI data input A
	SCRDAPO_0			SCRDAPO input
	T2CCU1_0B			T2 capture 1 input 0B
	EXINT2A			Interrupt 2 input A
	EXINT8B			Interrupt 8 input B
	ADCOMPCH6			Analog input channel 6
	ADC_TMADC4CH4	AI		Analog Input for TMADC4 Channel 4
	P33.6	O0		General-purpose output
	GTM_TOUT28	O1		GTM muxed output
	ASCLIN2_ASLSO	O2		Slave select signal output
	QSPI2_SLSO11	O3		Master slave select output
	PSI5_TX2	O4		TXD outputs (send data)
	ADC_EMUXCTRL10	O5		EMUX1 Control from TMADC to PORTS
	ADC_BFL1	O6		Boundary flags from FCC
	PSI5S0_TX	O7		TX data output
	SENT0_SPC12	O8		Transmit output
	EGTM_TOUT28	O9		eGTM muxed output
	QSPI4_MTSR	O10		Master SPI data output
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved

(table continues...)

Table 45 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.6	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional receive pin O
	SSC_MTSR	O#2		Master SPI data output
	T20EXF2	O#3		Timer 20 external overflow
	—	O#4		Reserved
	—	O#5		Reserved
	T2CCU1_0	O#6		T2 PWM channel 10
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
Y13	P33.7	I	SLOW / PU1 / VDDEVRS B / ES5	General-purpose input
	GTM_TIM0_IN3_9			Mux input channel 3 of TIM module 0
	GTM_TIM1_IN3_9			Mux input channel 3 of TIM module 1
	CAN00_RXDE			CAN receive input node 0
	GPT120_T2INB			Trigger/gate input of timer T2
	PSI5S0_RXD			RX data input
	SCU_E_REQ4A			ERU channel 4 input A
	SENT1_SENT11B			Receive input channel 11
	GPT122_T2EUDA			Count direction control input of timer T2
	ADC_TRIG60			Triggers from PORTS to ADC
	EGTM_TIM0_IN3_9			Mux input channel 3 of TIM module 0
	EGTM_TIM1_IN3_9			Mux input channel 3 of TIM module 1
	WCAN_RXDB	I#		Wake-up input B
	SSC_SCLKA			Slave SPI clock input A
	T20B			T20 capture input B

(table continues...)

Table 45 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	T21EXH			T21 interrupt input H
	T2CCU1_1B			T2 capture 1 input 1B
	EXINT0B			Interrupt 0 input B
	EXINT9B			Interrupt 9 input B
	ADCOMPCH7			Analog input channel 7
	ADC_TMADC4CH3	AI		Analog Input for TMADC4 Channel 3
	P33.7	O0		General-purpose output
	GTM_TOUT29	O1		GTM muxed output
	ASCLIN2_ASCLK	O2		Shift clock output
	QSPI4_SLSO7	O3		Master slave select output
	—	O4		Reserved
	ADC_EMUXCTRL13	O5		EMUX1 Control from TMADC to PORTS
	—	O6		Reserved
	QSPI5_SLSO10	O7		Master slave select output
	SENT1_SPC11	O8		Transmit output
	EGTM_TOUT29	O9		eGTM muxed output
	QSPI4_SCLK	O10		Master SPI clock output
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P0.7	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	SSC_SCLK	O#2		Clock output
	—	O#3		Reserved
	—	O#4		Reserved
	—	O#5		Reserved
	T2CCU1_1	O#6		T2 PWM channel 11
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved

(table continues...)

Table 45 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	SCRDAP1_0	I/O		SCRDAP1 input
	SPD_0	I/O		Single pin DAP0
W14	P33.8	I	FAST / HighZ / VDDEVRS B	General-purpose input
	GTM_TIM0_IN4_7			Mux input channel 4 of TIM module 0
	GTM_TIM1_IN4_7			Mux input channel 4 of TIM module 1
	ASCLIN2_ARXE			Receive input
	SMU_EXT_EMERGENCYCYS TOP_A_REQ			Emergency Stop External Request A
	SMU_FSPIN0			FSP Status Input - Shows the actual state of the FSP ErroPin
	EGTM_TIM0_IN4_7			Mux input channel 4 of TIM module 0
	EGTM_TIM1_IN4_7			Mux input channel 4 of TIM module 1
	UART_RXDF	I#		Receive input F
	WCAN_RXDO			Wake-up input O
	T21EXN			T21 interrupt input N
	T2CCU1_3D			T2 capture 1 input 3D
	EXINT1B			Interrupt 1 input B
	EXINT11D			Interrupt 11 input D
	I2CSDAD			Serial clock input D
	P33.8	O0		General-purpose output
	GTM_TOUT30	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	QSPI4_SLSO2	O3		Master slave select output
	—	O4		Reserved
	CAN00_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	QSPI5_SLSO11_F	O7		Master slave select output
	QSPI6_SLSO13	O8		Master slave select output
	EGTM_TOUT30	O9		eGTM muxed output

(table continues...)

Table 45 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.0	O#0		General-purpose output
	—	O#1		Reserved
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	—	O#5		Reserved
	—	O#6		Reserved
	I2CSDA	O#7		Serial data output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	SMU_FSP0	O		FSP Output Signal - Generated by SMU
Y14	P33.9	I	SLOW / PU1 / VDDEVRS B / ES5	General-purpose input
	GTM_TIM0_IN1_9			Mux input channel 1 of TIM module 0
	GTM_TIM1_IN1_9			Mux input channel 1 of TIM module 1
	XTAL3			XTAL3.RTC Oscillator
	GPT122_T4EUDA			Count direction control input of timer T4
	EGTM_TIM0_IN1_9			Mux input channel 1 of TIM module 0
	EGTM_TIM1_IN1_9			Mux input channel 1 of TIM module 1
	T1A	I#		T1 capture input A
	T20EXC			T2 interrupt input C
	T2CCU0_0B			T2 capture 0 input 0B

(table continues...)

Table 45 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EXINT3B			Interrupt 3 input B
	EXINT14C			Interrupt 14 input C
	I2CSCLD			Serial clock input D
	P33.9	O0		General-purpose output
	GTM_TOUT31	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	QSPI4_SLSO1	O3		Master slave select output
	ASCLIN2_ASCLK	O4		Shift clock output
	CAN01_TXD	O5		CAN transmit output node 1
	ASCLIN0_ATX	O6		Transmit output
	QSPI5_SLSO12	O7		Master slave select output
	QSPI6_SLSO10	O8		Master slave select output
	EGTM_TOUT31	O9		eGTM muxed output
	—	O10		Reserved
	ADC_BFL8	O11		Boundary flags from FCC
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.1	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_0	O#5		T2 PWM channel 00
	—	O#6		Reserved
	I2CSCL	O#7		Serial clock output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved

(table continues...)

Table 45 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#14		Reserved
	—	O#15		Reserved
W15	P33.10	I	SLOW / PU1 / VDDEVRS B / ES5	General-purpose input
	GTM_TIM0_IN0_9			Mux input channel 0 of TIM module 0
	GTM_TIM1_IN0_9			Mux input channel 0 of TIM module 1
	GTM_TIM4_IN4_14			Mux input channel 4 of TIM module 4
	QSPI4_SLSIA			Slave select input
	CAN01_RXDD			CAN receive input node 1
	ASCLIN0_ARXD			Receive input
	EGTM_TIM0_IN0_9			Mux input channel 0 of TIM module 0
	EGTM_TIM1_IN0_9			Mux input channel 0 of TIM module 1
	UART_RXDA	I#		Receive input A
	WCAN_RXDA			Wake-up input A
	RTC32_IN			RTC oscillator input
	T20EXP			T20 interrupt input P
	T21EXK			T21 interrupt input K
	EXINT2B			Interrupt 2 input B
	EXINT15C			Interrupt 15 input C
	P33.10	O0		General-purpose output
	GTM_TOUT32	O1		GTM muxed output
	QSPI1_SLSO6	O2		Master slave select output
	QSPI4_SLSO0	O3		Master slave select output
	ASCLIN1_ASLSO	O4		Slave select signal output
	PSI5S0_CLK	O5		PSI5S CLK is a clock that can be used on a pin to drive the external PHY.
	—	O6		Reserved
	QSPI5_SLSO13	O7		Master slave select output
	—	O8		Reserved
	EGTM_TOUT32	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved

(table continues...)

Table 45 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.2	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional receive pin O
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	—	O#5		Reserved
	—	O#6		Reserved
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	XTAL4	PO		XTAL4. RTC Oscillator
	Y15	P33.11		I
GTM_TIM0_IN2_8			Mux input channel 2 of TIM module 0	
GTM_TIM1_IN2_8			Mux input channel 2 of TIM module 1	
QSPI4_SCLKA			Slave SPI clock inputs	
SMM_ESR2_PORT_IN			ESR2 pad data from PIN Slice	
QSPI5_SCLKF_F			Slave SPI clock inputs	
GPT122_T5INA			Trigger/gate input of timer T5	
EGTM_TIM0_IN2_8			Mux input channel 2 of TIM module 0	
EGTM_TIM1_IN2_8			Mux input channel 2 of TIM module 1	
PMS_ESR2WKP			ESR2 pin input	
SSC_SCLKB			I#	Slave SPI clock input B
PINRSTA		Reset input A		
T20C		T20 capture input C		
T2CCU0_1B		T2 capture 0 input 1B		

(table continues...)

Table 45 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	T2CCU1_2B			T2 capture 1 input 2B
	EXINT4B			Interrupt 4 input B
	EXINT10B			Interrupt 10 input B
	P33.11	O0		General-purpose output
	GTM_TOUT33	O1		GTM muxed output
	ASCLIN1_ASCLK	O2		Shift clock output
	QSPI4_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	ASCLIN5_ASCLK_F	O5		Shift clock output
	ADC_PWM1	O6		Negative PWM
	QSPI5_SCLK_F	O7		Master SPI clock output
	—	O8		Reserved
	EGTM_TOUT33	O9		eGTM muxed output
	—	O10		Reserved
	ADC_BFL9	O11		Boundary flags from FCC
	PMS_RTCOUT	O12		RTC output for P33.11
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.3	O#0		General-purpose output
	—	O#1		Reserved
	SSC_SCLK	O#2		Clock output
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_1	O#5		T2 PWM channel 01
	T2CCU1_2	O#6		T2 PWM channel 12
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved

(table continues...)

Table 45 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#14		Reserved
	—	O#15		Reserved
	PMS_ESR2PORST	PO		ESR2 reset output. For details please refer to the PMS/SMM chapter.
W16	P33.12	I	FAST / PU1 / VDDEVRS B / ES5	General-purpose input
	GTM_TIM2_IN0_6			Mux input channel 0 of TIM module 2
	GTM_TIM3_IN0_6			Mux input channel 0 of TIM module 3
	QSPI4_MTSRA			Slave SPI data input
	CAN00_RXDD			CAN receive input node 0
	GPT122_T5EUDA			Count direction control input of timer T5
	SMU_FSPIN1			FSP Status Input - Shows the actual state of the FSP ErroPin
	EGTM_TIM2_IN0_6			Mux input channel 0 of TIM module 2
	PMS_PINCWKP			PINC (P33.12) pin input
	UART_RXDG	I#		Receive input G
	WCAN_RXDG			Wake-up input G
	SSC_MTSRB			Slave SPI data input B
	T1C			T1 capture input C
	T21C			T21 capture input C
	T2CCU0_2B			T2 capture 0 input 2B
	T2CCU1_3B			T2 capture 1 input 3B
	EXINT5B			Interrupt 5 input B
	EXINT11B			Interrupt 11 input B
	P33.12	O0		General-purpose output
	GTM_TOUT34	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	QSPI4_MTSR	O3		Master SPI data output
	ASCLIN1_ASCLK	O4		Shift clock output
	CAN22_TXD	O5		CAN transmit output node 2
	ADC_PWM0	O6		Positive PWM
	QSPI5_MTSR_F	O7		Master SPI data output
	ASCLIN5_ATX_F	O8		Transmit output
	EGTM_TOUT34	O9		eGTM muxed output
	—	O10		Reserved

(table continues...)

Table 45 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.4	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	SSC_MTSR	O#2		Master SPI data output
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_2	O#5		T2 PWM channel 02
	T2CCU1_3	O#6		T2 PWM channel 13
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	SMU_FSP1	O		FSP Output Signal - Generated by SMU
Y16	P33.13	I	FAST / PU1 / VDDEVRS B / ES5	General-purpose input
	GTM_TIM2_IN1_5			Mux input channel 1 of TIM module 2
	GTM_TIM3_IN1_5			Mux input channel 1 of TIM module 3
	ASCLIN1_ARXF			Receive input
	ADC_SIGN1			Sign for Carrier Cancellation
	QSPI4_MRSTA			Master SPI data input
	MSC1_INJ1			Injection signal from port
	CAN22_RXDA			CAN receive input node 2
	GPT122_T6EUDA			Count direction control input of core timer T6
	QSPI5_MRSTD_F			Master SPI data input
	PSI5S1_RXD			RX data input

(table continues...)

Table 45 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TIM2_IN1_5	I#		Mux input channel 1 of TIM module 2
	PMS_PINBWKP			PINB (P33.13) pin input
	UART_RXDB			Receive input B
	WCAN_RXDC			Wake-up input C
	SSC_MRSTB			Master SPI data input B
	T0C			T0 capture input C
	T20EXD			T20 interrupt input D
	T2CCU0_3B			T2 capture 0 input 3B
	EXINT0C			Interrupt 0 input C
	EXINT6B			Interrupt 6 input B
	ADCOMPCH8			Analog input channel 8
	P33.13	O0		General-purpose output
	GTM_TOUT35	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	QSPI4_MRST	O3		Slave SPI data output
	QSPI2_SLSO6	O4		Master slave select output
	CAN00_TXD	O5		CAN transmit output node 0
	ASCLIN5_ASLSO_F	O6		Slave select signal output
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT35	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.5	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional receive pin O
	SSC_MRST	O#2		Slave SPI data output
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_3	O#5		T2 PWM channel 03

(table continues...)

Table 45 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	T2CCU1_4	O#6		T2 PWM channel 14
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
T14	P33.14	I	FAST / PU1 / VDDEVRS B / ES5	General-purpose input
	GTM_TIM2_IN0_8			Mux input channel 0 of TIM module 2
	GTM_TIM4_IN5_14			Mux input channel 5 of TIM module 4
	GTM_TIM5_IN0_8			Mux input channel 0 of TIM module 5
	QSPI2_SCLKD			Slave SPI clock inputs
	CBS_TGI6			Trigger input
	CAN31_RXDB			CAN receive input node 1
	QSPI5_MRSTF_F			Master SPI data input
	EGTM_TIM2_IN0_8			Mux input channel 0 of TIM module 2
	SSC_SCLKC	I#		Slave SPI clock input C
	EXTNMI			NMI input
	T21EXC			T21 interrupt input C
	EXINT1C			Interrupt 1 input C
	ADCOMPCH9			Analog input channel 9
	P33.14	O0		General-purpose output
	GTM_TOUT143	O1		GTM muxed output
	—	O2		Reserved
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	QSPI5_MRST	O7		Slave SPI data output
	—	O8		Reserved

(table continues...)

Table 45 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	EGTM_TOUT143	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.6	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	SSC_SCLK	O#2		Clock output
	—	O#3		Reserved
	—	O#4		Reserved
	—	O#5		Reserved
	T2CCU1_5	O#6		T2 PWM channel 15
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	CBS_TGO6	O		Trigger output
U14	P33.15	I	FAST / PU1 / VDDEVRS B / ES5	General-purpose input
	GTM_TIM2_IN1_7			Mux input channel 1 of TIM module 2
	GTM_TIM4_IN6_11			Mux input channel 6 of TIM module 4
	GTM_TIM5_IN1_9			Mux input channel 1 of TIM module 5
	CBS_TGI7			Trigger input
	QSPI5_SLSIB_F			Slave select input
	SENT1_SENT14D			Receive input channel 14
	QSPI4_MTSRD			Slave SPI data input
	EGTM_TIM2_IN1_7			Mux input channel 1 of TIM module 2

(table continues...)

Table 45 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	UART_RXDE	I#		Receive input E
	PINRSTB			Reset input B
	T20EXE			T20 interrupt input E
	T2CCU0_0C			T2 capture 0 input 0C
	T2CCU1_0C			T2 capture 1 input 0C
	EXINT2C			Interrupt 2 input C
	EXINT3C			Interrupt 3 input C
	EXINT8C			Interrupt 8 input C
	ADCOMPCH10			Analog input channel 10
	P33.15	O0		General-purpose output
	GTM_TOUT144	O1		GTM muxed output
	CAN31_TXD	O2		CAN transmit output node 1
	QSPI2_SLSO11	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	SENT1_SPC14	O8		Transmit output
	EGTM_TOUT144	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P1.7	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional receive pin O
	—	O#2		Reserved
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_0	O#5		T2 PWM channel 00
	T2CCU1_0	O#6		T2 PWM channel 10
	—	O#7		Reserved

(table continues...)

Table 45 (continued) Port 33 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	CBS_TGO7	O		Trigger output

3.3.16 BGA292_STD port 34

Table 46 Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
U11	P34.1	I	SLOW / PU1 / VDDEVRS B / ES5	General-purpose input
	GTM_TIM2_IN3_9			Mux input channel 3 of TIM module 2
	GTM_TIM3_IN4_13			Mux input channel 4 of TIM module 3
	GTM_TIM5_IN3_9			Mux input channel 3 of TIM module 5
	SENT0_SENT12D			Receive input channel 12
	GPT122_T3INA			Trigger/gate input of core timer T3 (input A, B and C)
	EGTM_TIM2_IN3_9			Mux input channel 3 of TIM module 2
	UART_RXDD	I#		Receive input D
	T21EXD			T21 interrupt input D
	T2CCU0_1C			T2 capture 0 input 1C
	T2CCU1_1C			T2 capture 1 input 1C
	EXINT4C			Interrupt 4 input C
	EXINT9C			Interrupt 9 input C
	ADCOMPCH11			Analog input channel 11
	ADC_TMADC4CH15	AI		Analog Input for TMADC4 Channel 15
	P34.1	O0		General-purpose output
	GTM_TOUT146	O1		GTM muxed output
	ASCLIN4_ATX	O2		Transmit output
	—	O3		Reserved

(table continues...)

Table 46 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	CAN00_TXD	O4		CAN transmit output node 0
	CAN20_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	SENT0_SPC12	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT146	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P3.0	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional receive pin O
	—	O#2		Reserved
	T20EXF2	O#3		Timer 20 external overflow
	—	O#4		Reserved
	T2CCU0_1	O#5		T2 PWM channel 01
	T2CCU1_1	O#6		T2 PWM channel 11
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	PMS_DEBUG0	O		PMS debugging power mode K
T12	P34.2	I	SLOW / PU1 / VDDEVRS B / ES	General-purpose input
	GTM_TIM2_IN4_8			Mux input channel 4 of TIM module 2
	GTM_TIM3_IN5_15			Mux input channel 5 of TIM module 3
	GTM_TIM5_IN4_8			Mux input channel 4 of TIM module 5

(table continues...)

Table 46 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN4_ARXB			Receive input
	CAN00_RXDG			CAN receive input node 0
	CAN20_RXDC			CAN receive input node 0
	SENT0_SENT14B			Receive input channel 14
	GPT122_T3EUDA			Count direction control input of core timer T3
	I2C1_SDAD			Serial Data Input 3
	EGTM_TIM2_IN4_8			Mux input channel 4 of TIM module 2
	WCAN_RXDI	I#		Wake-up input I
	T20EXF			T20 interrupt input F
	T2CCU0_2C			T2 capture 0 input 2C
	EXINT5C			Interrupt 5 input C
	ADCOMPCH12			Analog input channel 12
	I2CSDAB			Serial data input B
	ADC_TMADC4CH14	AI		Analog Input for TMADC4 Channel 14
	P34.2	O0		General-purpose output
	GTM_TOUT147	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	I2C1_SDA	O8		Serial Data Output
	EGTM_TOUT147	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P3.1	O#0		General-purpose output
	—	O#1		Reserved
	—	O#2		Reserved

(table continues...)

Table 46 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	—	O#3		Reserved
	T21EXF2	O#4		Timer 21 external overflow
	T2CCU0_2	O#5		T2 PWM channel 02
	T2CCU1_2	O#6		T2 PWM channel 12
	I2CSDA	O#7		Serial data output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	PMS_DEBUG1	O		PMS debugging power mode K
U12	P34.3	I	SLOW / PU1 / VDDEVRS B / ES	General-purpose input
	GTM_TIM2_IN5_9			Mux input channel 5 of TIM module 2
	GTM_TIM3_IN6_14			Mux input channel 6 of TIM module 3
	GTM_TIM5_IN5_10			Mux input channel 5 of TIM module 5
	ASCLIN4_ARXE			Receive input
	SENT1_SENT14B			Receive input channel 14
	GPT122_T4INA			Trigger/gate input of timer T4
	I2C1_SCLD			Serial Clock Input 3
	EGTM_TIM2_IN5_9			Mux input channel 5 of TIM module 2
	PINRSTD	I#		Reset input D
	T21EXE			T21 interrupt input E
	T2CCU0_3C			T2 capture 0 input 3C
	EXINT0D			Interrupt 0 input D
	EXINT6C			Interrupt 6 input C
	ADCOMPCH13			Analog input channel 13
	I2CSCLB			Serial clock input B
	ADC_TMADC4CH13	AI		Analog Input for TMADC4 Channel 13
	P34.3	O0		General-purpose output
	GTM_TOUT148	O1		GTM muxed output

(table continues...)

Table 46 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ASCLIN4_ASCLK	O2		Shift clock output
	ASCLIN4_ATX	O3		Transmit output
	CAN00_TXD	O4		CAN transmit output node 0
	CAN20_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	—	O7		Reserved
	I2C1_SCL	O8		Serial Clock Output
	EGTM_TOUT148	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P3.2	O#0		General-purpose output
	—	O#1		Reserved
	—	O#2		Reserved
	T20EXF2	O#3		Timer 20 external overflow
	—	O#4		Reserved
	T2CCU0_3	O#5		T2 PWM channel 03
	T2CCU1_3	O#6		T2 PWM channel 13
	I2CSCL	O#7		Serial clock output
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	PMS_DEBUG2	O		PMS debugging power mode K
T13	P34.4	I	SLOW / PU1 /	General-purpose input
	GTM_TIM2_IN6_8			Mux input channel 6 of TIM module 2

(table continues...)

Table 46 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	GTM_TIM3_IN7_13	I#	VDDEVRS B / ES	Mux input channel 7 of TIM module 3
	GTM_TIM5_IN6_10			Mux input channel 6 of TIM module 5
	QSPI2_MRSTD			Master SPI data input
	SENT1_SENT13B			Receive input channel 13
	EGTM_TIM2_IN6_8			Mux input channel 6 of TIM module 2
	UART_RXDJ			Receive input J
	SSC_MRSTC			Master SPI data input C
	T20EXG			T20 interrupt input P
	T2CCU1_2C			T2 capture 1 input 2C
	EXINT1D			Interrupt 1 input D
	EXINT10C	AI		Interrupt 10 input C
	ADCOMPCH14			Analog input channel 14
	ADC_TMADC4CH12			Analog Input for TMADC4 Channel 12
	P34.4	O0		General-purpose output
	GTM_TOUT149	O1		GTM muxed output
	ASCLIN4_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	QSPI2_MRST	O4		Slave SPI data output
	—	O5		Reserved
	ADC_BFL6	O6		Boundary flags from FCC
	—	O7		Reserved
	—	O8		Reserved
	EGTM_TOUT149	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P3.3	O#0		General-purpose output
	UART_RXDO	O#1		Bidirectional receive pin O
	SSC_MRST	O#2		Slave SPI data output
	—	O#3		Reserved

(table continues...)

Table 46 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	T21EXF2	O#4		Timer 21 external overflow
	T2CCU0_4	O#5		T2 PWM channel 04
	T2CCU1_4	O#6		T2 PWM channel 14
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	PMS_DEBUG3	O		PMS debugging power mode K
U13	P34.5	I	FAST / PU1 / VDDEVRS B / ES	General-purpose input
	GTM_TIM2_IN7_9			Mux input channel 7 of TIM module 2
	GTM_TIM4_IN7_11			Mux input channel 7 of TIM module 4
	GTM_TIM5_IN7_9			Mux input channel 7 of TIM module 5
	QSPI2_MTSRD			Slave SPI data input
	QSPI4_MRSTF			Master SPI data input
	SENT0_SENT13C			Receive input channel 13
	EGTM_TIM2_IN7_9			Mux input channel 7 of TIM module 2
	WCAN_RXDJ	I#		Wake-up input J
	SSC_MTSRC			Slave SPI data input C
	T21EXF			T21 interrupt input F
	T2CCU1_3C			T2 capture 1 input 3C
	EXINT2D			Interrupt 2 input D
	EXINT11C			Interrupt 11 input C
	ADCOMPCH15			Analog input channel 15
	ADC_TMADC4CH11	AI		Analog Input for TMADC4 Channel 11
	P34.5	O0		General-purpose output
	GTM_TOUT150	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved

(table continues...)

Table 46 (continued) Port 34 functions

Ball	Symbol	Ctrl.	Buffer type	Function
	QSPI2_MTSR	O4		Master SPI data output
	—	O5		Reserved
	ADC_BFL7	O6		Boundary flags from FCC
	SENT0_SPC13	O7		Transmit output
	—	O8		Reserved
	EGTM_TOUT150	O9		eGTM muxed output
	—	O10		Reserved
	—	O11		Reserved
	—	O12		Reserved
	—	O13		Reserved
	—	O14		Reserved
	—	O15		Reserved
	SCR_P3.4	O#0		General-purpose output
	UART_TXD	O#1		Transmit output
	SSC_MTSR	O#2		Master SPI data output
	—	O#3		Reserved
	—	O#4		Reserved
	T2CCU0_5	O#5		T2 PWM channel 05
	T2CCU1_5	O#6		T2 PWM channel 15
	—	O#7		Reserved
	—	O#8		Reserved
	—	O#9		Reserved
	—	O#10		Reserved
	—	O#11		Reserved
	—	O#12		Reserved
	—	O#13		Reserved
	—	O#14		Reserved
	—	O#15		Reserved
	PMS_DEBUG4	O		PMS debugging power mode K

3.3.17 BGA292_STD analog

Table 47 Analog Inputs functions

Ball	Symbol	Ctrl.	Buffer type	Function
T10	AN0	I	D / HighZ / VDDM	Analog Input 0
	ADC_TMADC0CH0			Analog Input for TMADC0 Channel 0
	ADC_DSADC1PA			Analog Input for DSADC1 Positive Input A
	ADC_FCC1			Analog Input for FCC1
U10	AN1	I	D / HighZ / VDDM	Analog Input 1
	ADC_TMADC0CH1			Analog Input for TMADC0 Channel 1
	ADC_DSADC1NA			Analog Input for DSADC1 Negative Input A
W9	AN2	I	D / HighZ / VDDM	Analog Input 2
	ADC_TMADC0CH2			Analog Input for TMADC0 Channel 2
	ADC_DSADC0PA			Analog Input for DSADC0 Positive Input A
	ADC_FCC0			Analog Input for FCC0
U9	AN3	I	D / HighZ / VDDM	Analog Input 3
	ADC_TMADC0CH3			Analog Input for TMADC0 Channel 3
	ADC_DSADC0NA			Analog Input for DSADC0 Negative Input A
T9	AN4	I	D / HighZ / VDDM	Analog Input 4
	ADC_TMADC0CH4			Analog Input for TMADC0 Channel 4
	ADC_TMADC1CH0			Analog Input for TMADC1 Channel 0
Y9	AN5	I	D / HighZ / VDDM	Analog Input 5
	ADC_TMADC0CH5			Analog Input for TMADC0 Channel 5
	ADC_TMADC1CH1			Analog Input for TMADC1 Channel 1
T8	AN6	I	D / HighZ / VDDM	Analog Input 6
	ADC_TMADC0CH6			Analog Input for TMADC0 Channel 6
	ADC_TMADC1CH2			Analog Input for TMADC1 Channel 2
U8	AN7	I	D / HighZ / VDDM	Analog Input 7
	ADC_TMADC0CH7			Analog Input for TMADC0 Channel 7
	ADC_TMADC1CH3			Analog Input for TMADC1 Channel 3
W8	AN8	I	D / HighZ / VDDM	Analog Input 8
	ADC_TMADC0CH8			Analog Input for TMADC0 Channel 8
	ADC_TMADC5CH0			Analog Input for TMADC5 Channel 0
U7	AN9	I	D / HighZ / VDDM	Analog Input 9
	ADC_TMADC0CH9			Analog Input for TMADC0 Channel 9
	ADC_TMADC5CH1			Analog Input for TMADC5 Channel 1

(table continues...)

Table 47 (continued) Analog Inputs functions

Ball	Symbol	Ctrl.	Buffer type	Function
Y8	AN10	I	D / HighZ / VDDM	Analog Input 10
	ADC_TMADC0CH10			Analog Input for TMADC0 Channel 10
	ADC_TMADC5CH2			Analog Input for TMADC5 Channel 2
W7	AN11	I	D / HighZ / VDDM	Analog Input 11
	ADC_TMADC0CH11			Analog Input for TMADC0 Channel 11
	ADC_TMADC5CH3			Analog Input for TMADC5 Channel 3
T7	AN12	I	D / HighZ / VDDM	Analog Input 12
	ADC_TMADC0CH12			Analog Input for TMADC0 Channel 12
	ADC_DSADC0PB			Analog Input for DSADC0 Positive Input B
	ADC_DSADC3PB			Analog Input for DSADC3 Positive Input B
	ADC_FCC3			Analog Input for FCC3
W6	AN13	I	D / HighZ / VDDM	Analog Input 13
	ADC_TMADC0CH13			Analog Input for TMADC0 Channel 13
	ADC_DSADC0NB			Analog Input for DSADC0 Negative Input B
	ADC_DSADC3NB			Analog Input for DSADC3 Negative Input B
U6	AN14	I	D / HighZ / VDDM	Analog Input 14
	ADC_TMADC0CH14			Analog Input for TMADC0 Channel 14
	ADC_DSADC1PB			Analog Input for DSADC1 Positive Input B
	ADC_DSADC9PB			Analog Input for DSADC9 Positive Input B
	ADC_FCC9			Analog Input for FCC9
T6	AN15	I	D / HighZ / VDDM	Analog Input 15
	ADC_TMADC0CH15			Analog Input for TMADC0 Channel 15
	ADC_DSADC1NB			Analog Input for DSADC1 Negative Input B
	ADC_DSADC9NB			Analog Input for DSADC9 Negative Input B
W5	AN16	I	D / HighZ / VDDM	Analog Input 16
	ADC_TMADC1CH4			Analog Input for TMADC1 Channel 4
	ADC_DSADC6PC			Analog Input for DSADC6 Positive Input C
	ADC_FCC6			Analog Input for FCC6
U5	AN17 / P40.10	I	S / PU1 / VDDM	Analog Input 17
				General-purpose input
	ADC_TMADC1CH5			Analog Input for TMADC1 Channel 5
	ADC_DSADC6NC			Analog Input for DSADC6 Negative Input C
	SENT0_SENT5A			Receive input channel 5

(table continues...)

Table 47 (continued) Analog Inputs functions

Ball	Symbol	Ctrl.	Buffer type	Function
W4	AN18 / P40.11	I	S / PU1 / VDDM	Analog Input 18
				General-purpose input
				Analog Input for TMADC1 Channel 6
				Analog Input for TMADC5 Channel 4
				Analog Input for DSADC7 Positive Input C
				Analog Input for FCC7
				Receive input channel 5
W3	AN19 / P40.12	I	S / PU1 / VDDM	Analog Input 19
				General-purpose input
				Analog Input for TMADC1 Channel 7
				Analog Input for TMADC5 Channel 5
				Analog Input for DSADC7 Negative Input C
				Receive input channel 6
Y3	AN20	I	D / HighZ / VDDM	Analog Input 20
				Analog Input for TMADC1 Channel 8
				Analog Input for DSADC2 Positive Input A
				Analog Input for FCC2
Y2	AN21	I	D / HighZ / VDDM	Analog Input 21
				Analog Input for TMADC1 Channel 9
				Analog Input for DSADC2 Negative Input A
T5	AN22	I	D / HighZ / VDDM	Analog Input 22
				Analog Input for TMADC1 Channel 10
				Analog Input for TMADC5 Channel 6
R5	AN23	I	D / HighZ / VDDM	Analog Input 23
				Analog Input for TMADC1 Channel 11
				Analog Input for TMADC5 Channel 7
W2	AN24 / P40.0	I	S / PU1 / VDDM	Analog Input 24
				General-purpose input
				Analog Input for TMADC1 Channel 12
				Analog Input for DSADC2 Positive Input B
				Receive input channel 0
W1	AN25 / P40.1	I	S / PU1 / VDDM	Analog Input 25
				General-purpose input

(table continues...)

Table 47 (continued) Analog Inputs functions

Ball	Symbol	Ctrl.	Buffer type	Function
	ADC_TMADC1CH13			Analog Input for TMADC1 Channel 13
	ADC_DSADC2NB			Analog Input for DSADC2 Negative Input B
	SENT1_SENT0A			Receive input channel 0
V2	AN26 / P40.2	I	S / PU1 / VDDM	Analog Input 26
				General-purpose input
	ADC_TMADC1CH14			Analog Input for TMADC1 Channel 14
	ADC_TMADC5CH8			Analog Input for TMADC5 Channel 8
	SENT0_SENT1A			Receive input channel 1
V1	AN27 / P40.3	I	S / PU1 / VDDM	Analog Input 27
				General-purpose input
	ADC_TMADC1CH15			Analog Input for TMADC1 Channel 15
	ADC_TMADC5CH9			Analog Input for TMADC5 Channel 9
	SENT1_SENT1A			Receive input channel 1
U2	AN28 / P40.13	I	S / PU1 / VDDM	Analog Input 28
				General-purpose input
	ADC_TMADC3CH0			Analog Input for TMADC3 Channel 0
	ADC_TMADC5CH10			Analog Input for TMADC5 Channel 10
	SENT1_SENT6A			Receive input channel 6
U1	AN29 / P40.14	I	S / PU1 / VDDM	Analog Input 29
				General-purpose input
	ADC_TMADC3CH1			Analog Input for TMADC3 Channel 1
	ADC_TMADC5CH11			Analog Input for TMADC5 Channel 11
	SENT0_SENT7A			Receive input channel 7
T4	AN30	I	D / HighZ / VDDM	Analog Input 30
	ADC_TMADC3CH2			Analog Input for TMADC3 Channel 2
	ADC_TMADC5CH12			Analog Input for TMADC5 Channel 12
R4	AN31	I	D / HighZ / VDDM	Analog Input 31
	ADC_TMADC3CH3			Analog Input for TMADC3 Channel 3
	ADC_TMADC5CH13			Analog Input for TMADC5 Channel 13
P4	AN32 / P40.4	I	S / PU1 / VDDM	Analog Input 32
				General-purpose input
	ADC_TMADC3CH4			Analog Input for TMADC3 Channel 4
	ADC_TMADC5CH14			Analog Input for TMADC5 Channel 14

(table continues...)

Table 47 (continued) Analog Inputs functions

Ball	Symbol	Ctrl.	Buffer type	Function
	SENT0_SENT2A			Receive input channel 2
R1	AN33 / P40.5	I	S / PU1 / VDDM	Analog Input 33
				General-purpose input
	ADC_TMADC3CH5			Analog Input for TMADC3 Channel 5
	ADC_TMADC5CH15			Analog Input for TMADC5 Channel 15
	SENT1_SENT2A			Receive input channel 2
P5	AN34	I	D / HighZ / VDDM	Analog Input 34
	ADC_TMADC3CH6			Analog Input for TMADC3 Channel 6
	ADC_DSADC7PD			Analog Input for DSADC7 Positive Input D
R2	AN35	I	D / HighZ / VDDM	Analog Input 35
	ADC_TMADC3CH7			Analog Input for TMADC3 Channel 7
	ADC_DSADC7ND			Analog Input for DSADC7 Negative Input D
N4	AN36 / P40.6	I	S / PU1 / VDDM	Analog Input 36
				General-purpose input
	ADC_TMADC3CH8			Analog Input for TMADC3 Channel 8
	ADC_DSADC8PA			Analog Input for DSADC8 Positive Input
	ADC_FCC8			Analog Input for FCC8
	SENT0_SENT3A			Receive input channel 3
P2	AN37 / P40.7	I	S / PU1 / VDDM	Analog Input 37
				General-purpose input
	ADC_TMADC3CH9			Analog Input for TMADC3 Channel 9
	ADC_DSADC8NA			Analog Input for DSADC8 Negative Input
	SENT1_SENT3A			Receive input channel 3
N5	AN38 / P40.8	I	S / PU1 / VDDM	Analog Input 38
				General-purpose input
	ADC_TMADC3CH10			Analog Input for TMADC3 Channel 10
	ADC_DSADC8PB			Analog Input for DSADC8 Positive Input B
	SENT0_SENT4A			Receive input channel 4
P1	AN39 / P40.9	I	S / PU1 / VDDM	Analog Input 39
				General-purpose input
	ADC_TMADC3CH11			Analog Input for TMADC3 Channel 11
	ADC_DSADC8NB			Analog Input for DSADC8 Negative Input B
	SENT1_SENT4A			Receive input channel 4

(table continues...)

Table 47 (continued) Analog Inputs functions

Ball	Symbol	Ctrl.	Buffer type	Function
M5	AN40	I	D / HighZ / VDDM	Analog Input 40
	ADC_TMADC3CH12			Analog Input for TMADC3 Channel 12
	ADC_TMADC6CH0			Analog Input for TMADC6 Channel 0
M4	AN41	I	D / HighZ / VDDM	Analog Input 41
	ADC_TMADC3CH13			Analog Input for TMADC3 Channel 13
	ADC_TMADC6CH1			Analog Input for TMADC6 Channel 1
L5	AN42	I	D / HighZ / VDDM	Analog Input 42
	ADC_TMADC3CH14			Analog Input for TMADC3 Channel 14
	ADC_TMADC6CH2			Analog Input for TMADC6 Channel 2
L4	AN43	I	D / HighZ / VDDM	Analog Input 43
	ADC_TMADC3CH15			Analog Input for TMADC3 Channel 15
	ADC_TMADC6CH3			Analog Input for TMADC6 Channel 3
N1	AN44	I	D / HighZ / VDDM	Analog Input 44
	ADC_TMADC6CH4			Analog Input for TMADC6 Channel 4
	ADC_DSADC8PC			Analog Input for DSADC8 Positive Input C
N2	AN45	I	D / HighZ / VDDM	Analog Input 45
	ADC_TMADC6CH5			Analog Input for TMADC6 Channel 5
	ADC_DSADC8NC			Analog Input for DSADC8 Negative Input C
M1	AN46	I	D / HighZ / VDDM	Analog Input 46
	ADC_TMADC6CH6			Analog Input for TMADC6 Channel 6
	ADC_DSADC8PD			Analog Input for DSADC8 Positive Input D
M2	AN47	I	D / HighZ / VDDM	Analog Input 47
	ADC_TMADC6CH7			Analog Input for TMADC6 Channel 7
	ADC_DSADC8ND			Analog Input for DSADC8 Negative Input D

3.3.18 BGA292_STD special

Table 48 Special I/O functions

Ball	Symbol	Ctrl.	Buffer type	Function
K14	PHY1_TXP	O	PHY / VDDPHPH Y1	(Ball name)
	SGBT_TXP0	O		Transmit data (P line)
L14	PHY1_TXN	O	PHY / VDDPHPH Y1	(Ball name)
	SGBT_TXN0	O		Transmit data (N line)

3.3.19 BGA292_STD system

Table 49 System I/O functions

Ball	Symbol	Ctrl.	Buffer type	Function
A1	THD0_A	I	—	Reserved - has to be connected to VSSEXT
M19	XTAL2	O	XTAL / VDDEXTOSC	XTAL2. Main Oscillator/PLL/Clock generator output
M20	XTAL1	I	XTAL / VDDEXTOSC	XTAL1. Main Oscillator/PLL/Clock generator input
L19	TRST	I	FAST / PU2 / VDDEXT	JTAG Module Reset/Enable Input
	DAPE0	I		DAPE: DAPE0 Data I/O DAPE: DAPE0 Data I/O (PD Devices: VSS)
J16	TCK	I	FAST / PD3 / VDDEXT	JTAG Module Clock Input
	DAP0	I		DAP:DAP0 Clock Input
K16	TMS	I	FAST / PD3 / VDDEXT	JTAG Module State Machine Control Input
	DAP1	I/O		DAP:DAP1 Data I/O
G16	ESR1	I/O	FAST / PU1 / VDDEXT	ESR1 pad data
	SMM_ESR1_PORT_IN	I		ESR1 pad data from PIN Slice
	PMS_ESR1WKP	I		ESR1 pin input
F16	ESR0	I/O	FAST / OD / VDDEXT	ESR0 pad data
	SMM_ESR0_PORT_IN	I		ESR0 pad data from PIN Slice
	PMS_ESR0WKP	I		ESR0 pin input
G17	PORST	I/O	PORST / PD / VDDEXT	Power on Reset. Additional strong PD in case of power fail.
	PMS_PORSTOUT	O		Power On Reset Output. Additional strong PD in case of power fail.
	PMS_PORSTIN	I		Power On Reset Input. Additional strong PD in case of power fail.
B2	THD0_K	I	—	Reserved - has to be connected to VSSEXT

3.3.20 BGA292_STD supply

Table 50 Supply functions

Ball	Symbol	Ctrl.	Buffer type	Function
H14	NC1_H14	I	—	Not connected. These pins are not connected on package level and will not be used for future extensions

(table continues...)

Table 50 (continued) Supply functions

Ball	Symbol	Ctrl.	Buffer type	Function
N14	NC1_N14	I	—	Not connected. These pins are not connected on package level and will not be used for future extensions
P11	NC1_P11	I	—	Not connected. These pins are not connected on package level and will not be used for future extensions
U4	NC1_U4	I	—	Not connected. These pins are not connected on package level and will not be used for future extensions
Y1	NC1_Y1	I	—	Not connected. These pins are not connected on package level and will not be used for future extensions
E15	PHYx_RESREF	I	—	PHYx Resistor Reference
Y7	VAGND1	I	—	Negative Analog Reference Voltage 1
T2	VAGND2	I	—	Negative Analog Reference Voltage 2
Y6	VAREF1	I	—	Positive Analog Reference Voltage 1
T1	VAREF2	I	—	Positive Analog Reference Voltage 2
G13, H12, H7, H9, J13, J8, M8, N12, N7, N9, P8	VDD	I	—	Digital Core Power Supply (0.9V / 0.95V / 1V)
T11	VDDEVRSB	I	—	Standby Power Supply (5V / 3.3V) for the Standby SRAM
A2, B3, V19, W20	VDDEXT	I	—	External Power Supply (5V / 3.3V)
Y19	VDDEXTDC	I	—	External DCDC Supply (3.3V / 5.0V / 5.5V / 6.5V)
B18, D16	VDDEXTHS	I	—	External Power Supply (5V / 3.3V)
A19	VDDEXTHS_SENSE	I/O	—	External Power Supply (5V / 3.3V)
N20	VDDEXTOSC	I	—	External Power Supply for Oscillator (shall be supplied with same level as used for VDDEXT)
D5	VDDFLEX	I	—	External Power Supply for FLEX Port Pads (5V / 3.3V)
Y5	VDDM	I	—	External Power Supply (5V / 3.3V)
N19	VDDPHPHY1	I	—	PHY1 External Power Supply (1.8V)
M13	VDDPHY1	I	—	PHY1 Digital Core Power Supply (0.9V / 0.95V / 1V)
G8	VDDSB	I	—	Retention Power Supply (1V) for the Standby SRAM
P13	VDD_SENSE	I/O	—	Digital Core Power Supply (0.9V / 0.95V / 1V)
Y17	VGATE1N	O	—	DCDC N ch MOSFET gate driver output
Y18	VGATE1P	O	—	DCDC P ch MOSFET gate driver output

(table continues...)

Table 50 (continued) Supply functions

Ball	Symbol	Ctrl.	Buffer type	Function
G10, G11, G12, G9, H10, H11, J10, J11, J14, J7, K10, K11, K12, K13, K7, K8, K9, L10, L11, L12, L13, L7, L8, L9, M10, M11, M7, N10, N11, P10, P9	VSS	I	—	Digital Ground
B19, D17, D4, E16, E5, T16, U17	VSSEXT	I	—	External Vss
W19, Y20	VSSEXTDC	I	—	DCDC Ground
A20	VSSEXTHS_SENSE	I/O	—	External Vss
L20	VSSEXTOSC	I	—	Oscillator Ground
Y4	VSSM	I	—	External Vss
M14	VSSPHY	I	—	PHY Digital Ground
P12	VSS_SENSE	I/O	—	Digital Ground

3.4 Pad Sequence

Related information

[Logic symbols for package variants](#) on page 27

[BGA436_STD package variant pin configuration](#) on page 28

[BGA292_STD package variant pin configuration](#) on page 258

[Legend](#) on page 444

3.4.1 Sequence of pads in pad frame

Table 51 Pad Sequence

Number	Pad name	Pad type	Comment
1	COMPARATOR_VGPI O_tr	—	
2	THD0_A	—	Reserved - has to be connected to VSSEXT
3	OTP	VDDEXT	
4	P01.2	SLOW / PU1 / VDDEXT / ES	General-purpose I/O

(table continues...)

Table 51 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
5	P01.1	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
6	VSS_V	—	Supply Voltage
7	VDD_V	—	Supply Voltage
8	P01.8	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
9	VDDEXT_50_TL_HEA T_T1	—	Supply Voltage
10	VSSEXT_TL_HEAT_T 1	—	Supply Voltage
11	PADS_BUF_P02	—	
12	P02.0	FAST / PU1 / VDDEXT / ES	General-purpose I/O
13	P02.8	FAST / PU1 / VDDEXT / ES	General-purpose I/O
14	VSSEXT_TL_HEAT_T 2	—	Supply Voltage
15	VDDEXT_50_TL_HEA T_T2	—	Supply Voltage
16	P02.2	FAST / PU1 / VDDEXT / ES	General-purpose I/O
17	P02.9	FAST / PU1 / VDDEXT / ES	General-purpose I/O
18	VDDEXT_50_TL	—	Supply Voltage
19	VSSEXT_TL	—	Supply Voltage
20	P02.4	FAST / PU1 / VDDEXT / ES	General-purpose I/O
21	P02.5	FAST / PU1 / VDDEXT / ES	General-purpose I/O
22	P02.6	FAST / PU1 / VDDEXT / ES	General-purpose I/O
23	P02.7	FAST / PU1 / VDDEXT / ES	General-purpose I/O
24	VDDEXT_50_TL_HEA T_T3	—	Supply Voltage
25	VSSEXT_TL_HEAT_T 3	—	Supply Voltage
26	P02.11	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
27	P02.10	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
28	TERMINATOR5V	—	
29	BANDGAP_VGPIO	—	
30	TERMINATOR5V	—	
31	PADS_BUF_WKPCLR _3	—	
32	P01.9	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
33	P01.11	SLOW / PU1 / VDDEXT / ES	General-purpose I/O

(table continues...)

Table 51 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
34	P01.10	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
35	PADS_BUF_P01	—	
36	PADS_BUF_P00	—	
37	P01.13	FAST / PU1 / VDDEXT / ES	General-purpose I/O
38	P01.12	FAST / PU1 / VDDEXT / ES	General-purpose I/O
39	P00.0	FAST / PU1 / VDDEXT / ES	General-purpose I/O GPIO w. Analog function overlaid
40	P01.15	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
41	P01.14	FAST / PU1 / VDDEXT / ES	General-purpose I/O
42	VDDEXT_50_TL_HEA T_T4	—	Supply Voltage
43	VSSEXT_TL_HEAT_T 4	—	Supply Voltage
44	P00.13	FAST / PU1 / VDDEXT / ES	General-purpose I/O GPIO w. Analog function overlaid
45	P00.15	FAST / PU1 / VDDEXT / ES	General-purpose I/O GPIO w. Analog function overlaid
46	P01.4	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
47	P00.14	SLOW / PU1 / VDDEXT / ES	General-purpose I/O GPIO w. Analog function overlaid
48	VDDEXT_50_TL_HEA T_T5	—	Supply Voltage
49	VSSEXT_TL_HEAT_T 5	—	Supply Voltage
50	P01.5	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
51	P01.3	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
52	P01.6	FAST / PU1 / VDDEXT / ES	General-purpose I/O
53	P01.7	FAST / PU1 / VDDEXT / ES	General-purpose I/O
54	TERMINATOR5V	—	
55	AN34	D / HighZ / VDDM	Analog Input 34
56	AN35	D / HighZ / VDDM	Analog Input 35
57	VAREF5	Vx	Supply Voltage
58	VAGND0	Vx	Supply Voltage
59	VAGND1	Vx	Supply Voltage
60	VAGND2	Vx	Supply Voltage

(table continues...)

Table 51 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
61	VAGND3	Vx	Supply Voltage
62	VAGND4	Vx	Supply Voltage
63	VAREF0	Vx	Supply Voltage
64	VAGND5	Vx	Supply Voltage
65	VAREF1	Vx	Supply Voltage
66	VAREF2	Vx	Supply Voltage
67	AN9	D / HighZ / VDDM	Analog Input 9
68	VAREF3	Vx	Supply Voltage
69	AN10	D / HighZ / VDDM	Analog Input 10
70	VAREF4	Vx	Supply Voltage
71	AN32/P40.4	S / PU1 / VDDM	Analog Input 32 / General-purpose input
72	AN42	D / HighZ / VDDM	Analog Input 42
73	P00.1	SLOW / PU1 / VDDEXT / ES	General-purpose I/O GPIO w. Analog function overlaid
74	AN64	D / HighZ / VDDM	Analog Input 64
75	AN14	D / HighZ / VDDM	Analog Input 14
76	AN27/P40.3	S / PU1 / VDDM	Analog Input 27 / General-purpose input
77	AN19/P40.12	S / PU1 / VDDM	Analog Input 19 / General-purpose input
78	AN28/P40.13	S / PU1 / VDDM	Analog Input 28 / General-purpose input
79	AN7	D / HighZ / VDDM	Analog Input 7
80	AN21	D / HighZ / VDDM	Analog Input 21
81	AN33/P40.5	S / PU1 / VDDM	Analog Input 33 / General-purpose input
82	P00.12	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
83	P00.11	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
84	P00.10	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
85	P00.9	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
86	P00.8	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
87	P00.7	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid

(table continues...)

Table 51 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
88	P00.6	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
89	AN69/P41.2	S / PU1 / VDDM	Analog Input 69 / General-purpose input
90	P00.5	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
91	P00.4	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
92	P00.3	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
93	P00.2	SLOW / PU1 / VDDEXT / ES1	General-purpose I/O GPIO w. Analog function overlaid
94	AN63/P41.8	S / PU1 / VDDM	Analog Input 63 / General-purpose input
95	AN70/P41.3	S / PU1 / VDDM	Analog Input 70 / General-purpose input
96	AN71/P41.4	S / PU1 / VDDM	Analog Input 71 / General-purpose input
97	AN8	D / HighZ / VDDM	Analog Input 8
98	AN0	D / HighZ / VDDM	Analog Input 0
99	AN1	D / HighZ / VDDM	Analog Input 1
100	AN2	D / HighZ / VDDM	Analog Input 2
101	AN58	D / HighZ / VDDM	Analog Input 58
102	AN51	D / HighZ / VDDM	Analog Input 51
103	AN65	D / HighZ / VDDM	Analog Input 65
104	AN44	D / HighZ / VDDM	Analog Input 44
105	AN30	D / HighZ / VDDM	Analog Input 30
106	AN23	D / HighZ / VDDM	Analog Input 23
107	AN59	D / HighZ / VDDM	Analog Input 59
108	AN37/P40.7	S / PU1 / VDDM	Analog Input 37 / General-purpose input
109	AN52	D / HighZ / VDDM	Analog Input 52
110	AN31	D / HighZ / VDDM	Analog Input 31
111	AN66	D / HighZ / VDDM	Analog Input 66
112	AN60	D / HighZ / VDDM	Analog Input 60
113	AN53	D / HighZ / VDDM	Analog Input 53
114	AN67/P41.0	S / PU1 / VDDM	Analog Input 67 / General-purpose input
115	AN45	D / HighZ / VDDM	Analog Input 45
116	AN38/P40.8	S / PU1 / VDDM	Analog Input 38 / General-purpose input

(table continues...)

Table 51 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
117	AN39/P40.9	S / PU1 / VDDM	Analog Input 39 / General-purpose input
118	AN61	D / HighZ / VDDM	Analog Input 61
119	AN46	D / HighZ / VDDM	Analog Input 46
120	AN47	D / HighZ / VDDM	Analog Input 47
121	AN54/P41.5	S / PU1 / VDDM	Analog Input 54 / General-purpose input
122	AN48	D / HighZ / VDDM	Analog Input 48
123	AN68/P41.1	S / PU1 / VDDM	Analog Input 68 / General-purpose input
124	AN62/P41.7	S / PU1 / VDDM	Analog Input 62 / General-purpose input
125	AN56	D / HighZ / VDDM	Analog Input 56
126	AN55/P41.6	S / PU1 / VDDM	Analog Input 55 / General-purpose input
127	AN49	D / HighZ / VDDM	Analog Input 49
128	AN50	D / HighZ / VDDM	Analog Input 50
129	AN20	D / HighZ / VDDM	Analog Input 20
130	AN41	D / HighZ / VDDM	Analog Input 41
131	AN29/P40.14	S / PU1 / VDDM	Analog Input 29 / General-purpose input
132	AN43	D / HighZ / VDDM	Analog Input 43
133	AN15	D / HighZ / VDDM	Analog Input 15
134	AN6	D / HighZ / VDDM	Analog Input 6
135	AN22	D / HighZ / VDDM	Analog Input 22
136	AN36/P40.6	S / PU1 / VDDM	Analog Input 36 / General-purpose input
137	AN5	D / HighZ / VDDM	Analog Input 5
138	AN13	D / HighZ / VDDM	Analog Input 13
139	AN25/P40.1	S / PU1 / VDDM	Analog Input 25 / General-purpose input
140	AN18/P40.11	S / PU1 / VDDM	Analog Input 18 / General-purpose input
141	AN26/P40.2	S / PU1 / VDDM	Analog Input 26 / General-purpose input
142	AN40	D / HighZ / VDDM	Analog Input 40
143	AN57	D / HighZ / VDDM	Analog Input 57
144	AN24/P40.0	S / PU1 / VDDM	Analog Input 24 / General-purpose input
145	AN12	D / HighZ / VDDM	Analog Input 12
146	AN17/P40.10	S / PU1 / VDDM	Analog Input 17 / General-purpose input
147	AN4	D / HighZ / VDDM	Analog Input 4
148	AN16	D / HighZ / VDDM	Analog Input 16
149	AN3	D / HighZ / VDDM	Analog Input 3

(table continues...)

Table 51 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
150	AN11	D / HighZ / VDDM	Analog Input 11
151	VDDM_50_CONVIF1	—	Supply Voltage
152	VDDM_50_CONVPAD	—	Supply Voltage
153	VDDM_50_CONVDS1	—	Supply Voltage
154	VDDM_50_CONVDS2	—	Supply Voltage
155	VDDM_50_CONVIF2	—	Supply Voltage
156	VDDM_50_CONVDS0	—	Supply Voltage
157	VSSM_CONVDS1	—	Supply Voltage
158	VSSM_CONVIF1	—	Supply Voltage
159	VSSM_CONVDS2	—	Supply Voltage
160	VSSM_CONVIF0	—	Supply Voltage
161	VSSM_CONVPAD	—	Supply Voltage
162	VSSM_CONVDS0	—	Supply Voltage
163	VSSM_CONVIF2	—	Supply Voltage
164	VSSEXT_CONVE	—	Supply Voltage
165	VDDM_50_CONVIF0	—	Supply Voltage
166	VDDEXT_50_CONVE	—	Supply Voltage
167	TERMINATOR5V	—	
168	P31.0	FAST / PU1 / VDDEXT / ES	General-purpose I/O
169	P31.1	FAST / PU1 / VDDEXT / ES	General-purpose I/O
170	VSSEXT_TL_HEAT_L1	—	Supply Voltage
171	VDDEXT_50_TL_HEAT_L1	—	Supply Voltage
172	P31.3	FAST / PU1 / VDDEXT / ES	General-purpose I/O
173	PADS_BUF_WKPCLR_0	—	
174	P31.2	FAST / PU1 / VDDEXT / ES	General-purpose I/O
175	P31.4	FAST / PU1 / VDDEXT / ES	General-purpose I/O
176	VDD_H	—	Supply Voltage
177	VSS_H	—	Supply Voltage
178	P31.6	FAST / PU1 / VDDEXT / ES	General-purpose I/O
179	TERMINATOR5V	—	
180	BANDGAP_HGPIO	—	

(table continues...)

Table 51 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
181	TERMINATOR5V	—	
182	P31.5	FAST / PU1 / VDDEXT / ES	General-purpose I/O
183	P31.7	FAST / PU1 / VDDEXT / ES	General-purpose I/O
184	VSSEXT_TL_HEAT_L 2	—	Supply Voltage
185	VDDEXT_50_TL_HEA T_L2	—	Supply Voltage
186	PADS_BUF_P34	—	
187	TERMINATOR5V	—	
188	DIODE	—	
189	DIODE_TCP	—	
190	TREFE_L	—	
191	TPROTBS	—	
192	TERMINATOR5V	—	
193	ANARES_TGATE_5V	—	
194	TGRPROT2CORE_5V	—	
195	P33.1	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
196	P33.3	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
197	P33.0	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
198	VSSEVRSB_PAD	—	Supply Voltage
199	VDDEVRSB_50_PAD	—	Supply Voltage
200	P34.1	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
201	P33.2	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
202	P33.5	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
203	P33.4	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
204	P34.3	SLOW / PU1 / VDDEVRSB / ES	General-purpose I/O
205	P34.2	SLOW / PU1 / VDDEVRSB / ES	General-purpose I/O
206	P33.7	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
207	P33.6	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
208	VSSEVRSB_PAD	—	Supply Voltage
209	VDDEVRSB_50_PAD	—	Supply Voltage
210	P34.5	FAST / PU1 / VDDEVRSB / ES	General-purpose I/O
211	P34.4	SLOW / PU1 / VDDEVRSB / ES	General-purpose I/O
212	P33.8	FAST / HighZ / VDDEVRSB	General-purpose I/O

(table continues...)

Table 51 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
213	P33.15	FAST / PU1 / VDDEVRSB / ES5	General-purpose I/O
214	P33.10	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
215	P33.9	SLOW / PU1 / VDDEVRSB / ES5	General-purpose I/O
216	PADS_BUF_P33	—	
217	P33.14	FAST / PU1 / VDDEVRSB / ES5	General-purpose I/O
218	VSSEVRSB_PAD	—	Supply Voltage
219	VDDEVRSB_50_PAD	—	Supply Voltage
220	P33.11	FAST / PU1 / VDDEVRSB / ES5	General-purpose I/O
221	P32.6	SLOW / PU1 / VDDEVRSB / ES	General-purpose I/O
222	P32.5	FAST / PU1 / VDDEVRSB / ES	General-purpose I/O
223	P33.12	FAST / PU1 / VDDEVRSB / ES5	General-purpose I/O
224	P33.13	FAST / PU1 / VDDEVRSB / ES5	General-purpose I/O
225	VSSEVRSB_PAD	—	Supply Voltage
226	VDDEVRSB_50_PAD	—	Supply Voltage
227	P32.4	FAST / PU1 / VDDEVRSB / ES	General-purpose I/O
228	P32.2	FAST / PU1 / VDDEVRSB / ES	General-purpose I/O
229	P32.7	SLOW / PU1 / VDDEVRSB / ES	General-purpose I/O
230	PADS_BUF_P32	—	
231	VDDPMS1_H	—	Supply Voltage
232	VSS_H	—	Supply Voltage
233	VSSQ_TL	—	Supply Voltage
234	VDDEVRSB_50_TL	—	Supply Voltage
235	VSSEVRSB_TL	—	Supply Voltage
236	VDDEVRSB_50_TL	—	Supply Voltage
237	TGRPROT2CORE	—	
238	TGRPROTBS	—	
239	TERMINATOR5V	—	
240	DIODE_TCP	—	
241	Tpp7ve	—	
242	VDDEXTDC_70_TL_S ENSE	—	Supply Voltage
243	Tpp7v	—	
244	VDDEXTDC_70_TL	—	Supply Voltage
245	VDDEXTDC_70_TL	—	Supply Voltage

(table continues...)

Table 51 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
246	VDDEXTDC_70_TL	—	Supply Voltage
247	CTRL1V3P0	—	
248	CTRL1V3P2	—	
249	CTRL1V3P1	—	
250	Tpp7v	—	
251	CTRL1V3N2	—	
252	CTRL1V3N1	—	
253	CTRL1V3N0	—	
254	VSSEXTDC_TL	—	Supply Voltage
255	VSSEXTDC_TL	—	Supply Voltage
256	VSSEXTDC_TL	—	Supply Voltage
257	Dgtpp	—	
258	VSS_H	—	Supply Voltage
259	PMS_testmode	—	
260	TERMINATOR5V	—	
261	PADS_BUF_P30	—	
262	P30.0	FAST / PU1 / VDDEXT / ES	General-purpose I/O
263	P30.2	FAST / PU1 / VDDEXT / ES	General-purpose I/O
264	P30.4	FAST / PU1 / VDDEXT / ES	General-purpose I/O
265	VSSEXT_TL_HEAT_L 3	FAST	Supply Voltage
266	VDDEXT_50_TL_HEA T_L3	FAST	Supply Voltage
267	P30.1	FAST / PU1 / VDDEXT / ES	General-purpose I/O
268	P30.3	FAST / PU1 / VDDEXT / ES	General-purpose I/O
269	P30.7	FAST / PU1 / VDDEXT / ES	General-purpose I/O
270	P30.5	FAST / PU1 / VDDEXT / ES	General-purpose I/O
271	P30.6	FAST / PU1 / VDDEXT / ES	General-purpose I/O
272	P30.8	FAST / PU1 / VDDEXT / ES	General-purpose I/O
273	P30.10	FAST / PU1 / VDDEXT / ES	General-purpose I/O
274	P30.9	FAST / PU1 / VDDEXT / ES	General-purpose I/O
275	P30.11	FAST / PU1 / VDDEXT / ES	General-purpose I/O
276	P30.13	FAST / PU1 / VDDEXT / ES	General-purpose I/O
277	VDD_H	—	Supply Voltage

(table continues...)

Table 51 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
278	VSS_H	—	Supply Voltage
279	P30.12	FAST / PU1 / VDDEXT / ES	General-purpose I/O
280	P30.14	FAST / PU1 / VDDEXT / ES	General-purpose I/O
281	VSSEXT_TL_HEAT_L4	—	Supply Voltage
282	VDDEXT_50_TL_HEAT_L4	—	Supply Voltage
283	VSSEXT_TL	—	Supply Voltage
284	PADS_BUF_WKPCLR_1	—	
285	COMPARATOR_HGPI_O_lb	—	
286	CRACK_SENSOR_1	—	
287	COMPARATOR_VGPI_O_bl	—	
288	TOXMON	—	
289	VSSEXT_TL_HEAT_B1	—	Supply Voltage
290	VDDEXT_50_TL_HEAT_B1	—	Supply Voltage
291	P25.3	FAST / PU1 / VDDEXT / ES	General-purpose I/O
292	P26.0	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
293	P30.15	FAST / PU1 / VDDEXT / ES	General-purpose I/O
294	P25.4	FAST / PU1 / VDDEXT / ES	General-purpose I/O
295	PADS_BUF_P25	—	
296	P25.5	FAST / PU1 / VDDEXT / ES	General-purpose I/O
297	P25.9	FAST / PU1 / VDDEXT / ES	General-purpose I/O
298	VDDEXT_50_TL	—	Supply Voltage
299	VSSEXT_TL	—	Supply Voltage
300	P25.2	FAST / PU1 / VDDEXT / ES	General-purpose I/O
301	P25.1	FAST / PU1 / VDDEXT / ES	General-purpose I/O
302	COMPARATOR_VLVD_S_bl	—	
303	P25.0	FAST / PU1 / VDDEXT / ES	General-purpose I/O
304	VDDEXT_50_TL_HEAT_B2	—	Supply Voltage

(table continues...)

Table 51 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
305	VSSEXT_TL_HEAT_B 2	—	Supply Voltage
306	VDDEXT_50_TL	—	Supply Voltage
307	P23.2	FAST / PU1 / VDDEXT / ES	General-purpose I/O
308	P23.1	FAST / PU1 / VDDEXT / ES	General-purpose I/O
309	P23.0	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
310	P23.4	FAST / PU1 / VDDEXT / ES	General-purpose I/O
311	P23.3	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
312	PADS_BUF_P23	—	
313	TERMINATOR5V	—	
314	BANDGAP_VLVDS	—	
315	VDDEXT_50_TL	—	Supply Voltage
316	VSSEXT_TL	—	Supply Voltage
317	TERMINATOR5V	—	
318	P23.6	FAST / PU1 / VDDEXT / ES	General-purpose I/O
319	P22.2	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose I/O
320	P22.3	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose I/O
321	P22.5	FAST / PU1 / VDDEXT / ES	General-purpose I/O
322	P23.7	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
323	P22.4	FAST / PU1 / VDDEXT / ES	General-purpose I/O
324	P22.7	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
325	P25.11	FAST / PU1 / VDDEXT / ES	General-purpose I/O
326	VSSEXT_TL_HEAT_B 3	—	Supply Voltage
327	VDDEXT_50_TL_HEA T_B3	—	Supply Voltage
328	P22.8	FAST / PU1 / VDDEXT / ES	General-purpose I/O
329	P23.5	FAST / PU1 / VDDEXT / ES	General-purpose I/O
330	VSS_V	—	Supply Voltage
331	VDD_V	—	Supply Voltage
332	PADS_BUF_P22	—	
333	P22.6	FAST / PU1 / VDDEXT / ES	General-purpose I/O
334	P22.9	FAST / PU1 / VDDEXT / ES	General-purpose I/O

(table continues...)

Table 51 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
335	P22.11	FAST / PU1 / VDDEXT / ES	General-purpose I/O
336	P22.10	FAST / PU1 / VDDEXT / ES	General-purpose I/O
337	P22.0	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose I/O
338	P22.1	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose I/O
339	P25.7	FAST / PU1 / VDDEXT / ES	General-purpose I/O
340	P25.8	FAST / PU1 / VDDEXT / ES	General-purpose I/O
341	VDDEXT_50_TL_HEAT_B4	—	Supply Voltage
342	VSSEXT_TL_HEAT_B4	—	Supply Voltage
343	P25.10	FAST / PU1 / VDDEXT / ES	General-purpose I/O
344	P25.13	FAST / PU1 / VDDEXT / ES	General-purpose I/O
345	nc	—	
346	XTAL2	XTAL / VDDEXTOSC	XTAL2. Main Oscillator/PLL/Clock generator output XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT
347	XTAL1	XTAL / VDDEXTOSC	XTAL1. Main Oscillator/PLL/Clock generator input XTAL1. Main Oscillator/PLL/Clock Generator Input.
348	VSS_OSC	—	Supply Voltage
349	VDDEXTOSC_50_TL	—	Supply Voltage
350	PHY1_TXP	VDDPHPHY1	Transmit data (P line)
351	PHY1_RXP	VDDPHPHY1	Receive data (P line)
352	PHY1_TXN	VDDPHPHY1	Transmit data (N line)
353	PHY1_RXN	VDDPHPHY1	Receive data (N line)
354	VSSPHY1_TL	—	Supply Voltage
355	VDDPHPHY1_18_TL	—	Supply Voltage
356	VDDPHY1_10_TL	—	Supply Voltage
357	TERMINATOR5V	—	
358	TRST	FAST / PU2 / VDDEXT	
359	P25.6	FAST / PU1 / VDDEXT / ES	General-purpose I/O
360	TCK	FAST / PD3 / VDDEXT	

(table continues...)

Table 51 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
361	P25.14	FAST / PU1 / VDDEXT / ES	General-purpose I/O
362	P25.12	FAST / PU1 / VDDEXT / ES	General-purpose I/O
363	P21.7	FAST / PU1 / VDDEXT / ES	General-purpose I/O
364	TMS	FAST / PD3 / VDDEXT	
365	P25.15	FAST / PU1 / VDDEXT / ES	General-purpose I/O
366	VSSEXT_TL_HEAT_B5	—	Supply Voltage
367	VDDEXT_50_TL_HEAT_B5	—	Supply Voltage
368	P21.2	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose I/O
369	P21.3	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose I/O
370	P20.0	FAST / PU1 / VDDEXT / ES	General-purpose I/O
371	P20.2	S / PU / VDDEXT	General-purpose I/O This pin is latched at power on reset release to enter test mode.
372	P21.0	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose I/O
373	P21.1	LVDS_RX / FAST / PU1 / VDDEXT / ES	General-purpose I/O
374	PADS_BUF_P21	—	
375	VSSEXT_TL_HEAT_B6	—	Supply Voltage
376	VDDEXT_50_TL_HEAT_B6	—	Supply Voltage
377	P24.0	FAST / PU1 / VDDEXT / ES	General-purpose I/O
378	P21.6	FAST / PD3 / VDDEXT / ES	General-purpose I/O PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ.
379	P24.2	FAST / PU1 / VDDEXT / ES	General-purpose I/O

(table continues...)

Table 51 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
380	ESR1	FAST / PU1 / VDDEXT	External System Request Reset 1. Default NMI function (Configuration options see also SMM / SCU chapter for details). EVR Wakeup Source. Behavior after power-on can be different. See also SMM chapter: External service request interface. Behavior for system reset differs to the warm power-on reset behavior and is in that case always pull-up
381	P24.3	FAST / PU1 / VDDEXT / ES	General-purpose I/O
382	P24.1	FAST / PU1 / VDDEXT / ES	General-purpose I/O
383	P24.4	FAST / PU1 / VDDEXT / ES	General-purpose I/O
384	P21.4	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose I/O
385	P21.5	LVDS_TX / FAST / PU1 / VDDEXT / ES6	General-purpose I/O
386	P20.1	FAST / PU1 / VDDEXT / ES	General-purpose I/O
387	VSSEXT_TL_HEAT_B7	—	Supply Voltage
388	VDDEXT_50_TL_HEAT_B7	—	Supply Voltage
389	ESR0	FAST / OD / VDDEXT	External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SMM chapter for details. Behavior after power-on can be different. See also SMM chapter "External service request interface (ESRx)
390	P24.5	FAST / PU1 / VDDEXT / ES	General-purpose I/O
391	PORST	PORST / PD / VDDEXT	Power On Reset Input. Additional strong PD in case of power fail.
392	VDDEXT_50_TL	—	Supply Voltage
393	P20.3	FAST / PU1 / VDDEXT / ES	General-purpose I/O
394	VSS_V	—	Supply Voltage
395	VDD_V	—	Supply Voltage
396	P24.14	FAST / PU1 / VDDEXT / ES	General-purpose I/O
397	COMPARATOR_VLVD S_br	—	
398	VSSEXT_TL	—	Supply Voltage

(table continues...)

Table 51 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
399	PADS_BUF_P24	—	
400	PADS_BUF_WKPCLR_5	—	
401	COMPARATOR_VGPI_O_br	—	
402	COMPARATOR_HGPI_O_rb	—	
403	INST_PADS_EN_LS_HS2EXT_0	—	
404	INST_PADS_EN_LS_HS2EXT_1	—	
405	TERMINATOR5V	—	
406	INST_PADS_AND_LS_HS2EXT_0	—	
407	DIODE	—	
408	TERMINATOR5V	—	
409	P20.6	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
410	VDDEXTHS_50_TL	—	Supply Voltage
411	P20.7	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
412	VDDEXTHS_50_TL_HEAT_R1	—	Supply Voltage
413	VSSEXT_TL_HEAT_R1	—	Supply Voltage
414	P20.8	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
415	P20.9	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
416	P20.10	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
417	VSSEXT_TL_UNLOADED	—	Supply Voltage
418	P20.11	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
419	VDDEXTHS_50_TL_UNLOADED	—	Supply Voltage
420	P20.12	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
421	P20.13	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
422	VDDEXTHS_50_TL	—	Supply Voltage
423	VSSEXT_TL	—	Supply Voltage
424	P20.14	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O

(table continues...)

Table 51 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
425	VSSEXT_TL_HEAT_R 2	—	Supply Voltage
426	VDDEXTHS_50_TL_H EAT_R2	—	Supply Voltage
427	P14.0	FAST / PU1 / VDDEXTHS / ES2	General-purpose I/O
428	P14.1	FAST / PU1 / VDDEXTHS / ES2	General-purpose I/O
429	P14.5	FAST / PU2 / VDDEXTHS / ES	General-purpose I/O
430	VSSEXT_TL	—	Supply Voltage
431	VDDEXTHS_50_TL	—	Supply Voltage
432	P14.6	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
433	ANARES_TGATE_1	—	
434	ANARES_TGATE_2	—	
435	P15.0	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
436	ANARES_TGATE_4	—	
437	P15.3	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
438	P15.1	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
439	PADS_BUF_P20	—	
440	VDDEXTHS_50_TL_H EAT_R3	—	Supply Voltage
441	VSSEXT_TL_HEAT_R 3	—	Supply Voltage
442	P15.5	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
443	PADS_BUF_WKPCLR _2	—	
444	P14.11	SLOW / PU1 / VDDEXTHS / ES	General-purpose I/O
445	P14.13	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
446	P13.9	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
447	INST_PADS_LS_EXT 2HS_1	—	
448	P14.12	SLOW / PU1 / VDDEXTHS / ES	General-purpose I/O
449	P14.14	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
450	P15.2	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
451	ANARES_TGATE_3	—	
452	P14.15	SLOW / PU1 / VDDEXTHS / ES	General-purpose I/O
453	VSSEXT_TL	—	Supply Voltage

(table continues...)

Table 51 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
454	VDDEXTHS_50_TL	—	Supply Voltage
455	P15.4	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
456	P15.6	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
457	INST_PADS_AND_LS_EXT2HS_0	—	
458	P15.7	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
459	P15.11	FAST / PU1 / VDDEXTHS / ES6	General-purpose I/O
460	VDD_H	—	Supply Voltage
461	VSS_H	—	Supply Voltage
462	P15.10	FAST / PU1 / VDDEXTHS / ES6	General-purpose I/O
463	COMPARATOR_HLVD S_rb	—	
464	P15.8	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
465	P15.15	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
466	P15.13	FAST / PU1 / VDDEXTHS / ES6	General-purpose I/O
467	VSSEXT_TL	—	Supply Voltage
468	VDDEXTHS_50_TL	—	Supply Voltage
469	P15.12	FAST / PU1 / VDDEXTHS / ES6	General-purpose I/O
470	P14.2	SLOW / PU2 / VDDEXTHS / ES	General-purpose I/O
471	PADS_BUF_P15	—	
472	INST_PADS_LS_EXT 2HS_0	—	
473	P15.14	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
474	PADS_BUF_P14	—	
475	P13.5	LVDS_TX / FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
476	P13.4	LVDS_TX / FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
477	VDDEXTHS_50_TL_H EAT_R4	—	Supply Voltage
478	VSSEXT_TL_HEAT_R 4	—	Supply Voltage
479	P13.7	LVDS_TX / FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
480	P13.6	LVDS_TX / FAST / PU1 / VDDEXTHS / ES	General-purpose I/O

(table continues...)

Table 51 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
481	P14.4	SLOW / PU2 / VDDEXTHS / ES	General-purpose I/O
482	P14.10	LVDS_RX / FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
483	P14.9	LVDS_RX / FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
484	VSSEXT_TL	—	Supply Voltage
485	VDDEXTHS_50_TL	—	Supply Voltage
486	P14.7	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
487	TERMINATOR5V	—	
488	BANDGAP_HLVDS	—	
489	VSSEXT_TL_HEAT_R5	—	Supply Voltage
490	VDDEXTHS_50_TL_HEAT_R5	—	Supply Voltage
491	PADS_BUF_P13	—	
492	P14.3	SLOW / PU2 / VDDEXTHS / ES	General-purpose I/O
493	P13.1	LVDS_TX / FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
494	P13.0	LVDS_TX / FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
495	P14.8	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
496	P13.3	LVDS_TX / FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
497	P13.2	LVDS_TX / FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
498	P13.11	SLOW / PU1 / VDDEXTHS / ES	General-purpose I/O
499	P13.14	SLOW / PU1 / VDDEXTHS / ES	General-purpose I/O
500	P13.12	SLOW / PU1 / VDDEXTHS / ES	General-purpose I/O
501	P13.10	FAST / PU1 / VDDEXTHS / ES	General-purpose I/O
502	P13.13	SLOW / PU1 / VDDEXTHS / ES	General-purpose I/O
503	COMPARATOR_HLVDS_rt	—	
504	VDDEXTHS_50_TL_HEAT_R7	—	Supply Voltage
505	VSSEXT_TL_HEAT_R7	—	Supply Voltage
506	P13.15	SLOW / PU1 / VDDEXTHS / ES	General-purpose I/O

(table continues...)

Table 51 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
507	TERMINATOR5V	—	
508	DIODE	—	
509	TERMINATOR5V	—	
510	PADS_BUF_WKPCLR_4	—	
511	P12.1	FAST / PU1 / VDDFLEX / ES	General-purpose I/O
512	P11.3	FAST / PU1 / VDDFLEX / ES	General-purpose I/O
513	P11.6	FAST / PU1 / VDDFLEX / ES	General-purpose I/O
514	P11.0	FAST / PU1 / VDDFLEX / ES	General-purpose I/O
515	P11.2	FAST / PU1 / VDDFLEX / ES	General-purpose I/O
516	P11.12	FAST / PU1 / VDDFLEX / ES	General-purpose I/O
517	P12.0	SLOW / PU1 / VDDFLEX / ES	General-purpose I/O
518	VSSFLEX_TL	—	Supply Voltage
519	VDDFLEX_50_TL	—	Supply Voltage
520	P11.4	FAST / PU1 / VDDFLEX / ES	General-purpose I/O
521	P11.10	FAST / PU1 / VDDFLEX / ES	General-purpose I/O
522	P11.8	SLOW / PU1 / VDDFLEX / ES	General-purpose I/O
523	P11.1	FAST / PU1 / VDDFLEX / ES	General-purpose I/O
524	P11.5	FAST / PU1 / VDDFLEX / ES	General-purpose I/O
525	P11.7	SLOW / PU1 / VDDFLEX / ES	General-purpose I/O
526	P11.9	FAST / PU1 / VDDFLEX / ES	General-purpose I/O
527	VDDFLEX_50_TL_HEAT_R1	—	Supply Voltage
528	VSSFLEX_TL_HEAT_R1	—	Supply Voltage
529	P11.11	FAST / PU1 / VDDFLEX / ES	General-purpose I/O
530	P11.14	SLOW / PU1 / VDDFLEX / ES	General-purpose I/O
531	PADS_BUF_P11	—	
532	INST_PADS_LS_EXT2FLEX_0	—	
533	P11.13	SLOW / PU1 / VDDFLEX / ES	General-purpose I/O
534	P11.15	SLOW / PU1 / VDDFLEX / ES	General-purpose I/O
535	TERMINATOR5V	—	
536	DIODE	—	
537	TERMINATOR5V	—	

(table continues...)

Table 51 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
538	P10.0	FAST / PU1 / VDDEXT / ES	General-purpose I/O
539	P10.1	FAST / PU1 / VDDEXT / ES	General-purpose I/O
540	P10.2	FAST / PU1 / VDDEXT / ES	General-purpose I/O
541	VDDEXT_50_TL	—	Supply Voltage
542	VSSEXT_TL	—	Supply Voltage
543	P10.9	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
544	P10.13	FAST / PU1 / VDDEXT / ES	General-purpose I/O
545	PADS_BUF_P10	—	
546	P10.6	FAST / PU2 / VDDEXT / ES	General-purpose I/O
547	P10.3	FAST / PU1 / VDDEXT / ES	General-purpose I/O
548	P10.11	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
549	P10.10	FAST / PU1 / VDDEXT / ES	General-purpose I/O
550	P10.5	FAST / PU2 / VDDEXT / ES	General-purpose I/O
551	P10.15	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
552	P10.8	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
553	VDDEXT_50_TL_HEA T_R6	—	Supply Voltage
554	VSSEXT_TL_HEAT_R 6	—	Supply Voltage
555	P10.4	FAST / PU1 / VDDEXT / ES	General-purpose I/O
556	P10.14	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
557	P02.13	FAST / PU1 / VDDEXT / ES	General-purpose I/O
558	P01.0	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
559	P10.7	FAST / PU1 / VDDEXT / ES	General-purpose I/O
560	P02.1	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
561	ANARES_TGATE_6	—	
562	P02.12	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
563	ANARES_TGATE_5	—	
564	P02.3	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
565	P02.15	FAST / PU1 / VDDEXT / ES	General-purpose I/O
566	VDDEXT_50_TL	—	Supply Voltage
567	VSSEXT_TL	—	Supply Voltage
568	P02.14	SLOW / PU1 / VDDEXT / ES	General-purpose I/O
569	THD0_K	—	Reserved - has to be connected to VSSEXT

(table continues...)



Table 51 (continued) Pad Sequence

Number	Pad name	Pad type	Comment
570	COMPARATOR_HGPI O_rt	—	

3.5 Legend

Column 'Ctrl.'

- I = Input (for GPIO port lines with Pn_DRVCFG bit field Selection MODE = 0XXXX_B)
- O = Output (for GPIO port lines the `O` represents the HWOUT functions which are being controlled directly by the mapped hardware module)
- PO = Priority Output (for GPIO port lines the `PO` represents the priority functions controlled by the Pn_PCSRSEL.PCSR bit-field, where PCSR is set)
- O0 = Output with Pn_DRVCFG bit field selection MODE = 1X0000_B
- O1 = Output with Pn_DRVCFG bit field selection MODE = 1X0001_B (ALT1)
- O2 = Output with Pn_DRVCFG bit field selection MODE = 1X0010_B (ALT2)
- O3 = Output with Pn_DRVCFG bit field selection MODE = 1X0011_B (ALT3)
- O4 = Output with Pn_DRVCFG bit field selection MODE = 1X0100_B (ALT4)
- O5 = Output with Pn_DRVCFG bit field selection MODE = 1X0101_B (ALT5)
- O6 = Output with Pn_DRVCFG bit field selection MODE = 1X0110_B (ALT6)
- O7 = Output with Pn_DRVCFG bit field selection MODE = 1X0111_B (ALT7)
- O8 = Output with Pn_DRVCFG bit field selection MODE = 1X1000_B (ALT8)
- O9 = Output with Pn_DRVCFG bit field selection MODE = 1X1001_B (ALT9)
- O10 = Output with Pn_DRVCFG bit field selection MODE = 1X1010_B (ALT10)
- O11 = Output with Pn_DRVCFG bit field selection MODE = 1X1011_B (ALT11)
- O12 = Output with Pn_DRVCFG bit field selection MODE = 1X1100_B (ALT12)
- O13 = Output with Pn_DRVCFG bit field selection MODE = 1X1101_B (ALT13)
- O14 = Output with Pn_DRVCFG bit field selection MODE = 1X1110_B (ALT14)
- O15 = Output with Pn_DRVCFG bit field selection MODE = 1X1111_B (ALT15)
- I# and O# mark SCR peripheral mappings

Column 'Buffer type'

- FAST = Pad class FAST (5V/3.3V)
- HSFAST = Pad class HSFAST (3.3V/1.8V)
- SLOW = Pad class SLOW (5V/3.3V)
- LVDS_TX = Pad class LVDS Transmit
- LVDS_RX = Pad class LVDS Receive
- S = Pad class S (Analog Input overlayed with General Purpose Input)
- D = Pad class D (Analog Input)
- Porst = Porst input Pad
- XTAL1 = XTAL1 input Pad
- XTAL2 = XTAL2 output Pad
- Startup: Startup behavior in this document describes the behavior from supply rampup until VDDPPA for VDDEXT (for VDDEXT IO behavior) and additionally VDDPPSB for VDDEVR SB (for VDDEVR SB IO behavior) is reached
 For startup behavior until VDDPPA and VDDPPSB level is reached please refer to PMS table "Pad state depending on VDDEVR SB and VDDEXT supply"
- PU = The default state during and after reset ($\overline{\text{PORST}} = 0$) is pull-up. Pull-up in Standby mode
- PU1 = The default state of GPIOs (Px.y) during reset ($\overline{\text{PORST}} = 0$) is controlled through PMS_PADCON.ALLTRIST (HWCFG6 P14.4). The default state of GPIOs (Px.y) after reset ($\overline{\text{PORST}} = 1$) is controlled through PORT reset value determined by PMS_PADCON.ALLTRIST (HWCFG6 P14.4). In Standby Mode the state is controlled through PMS_PADCON.ALLTRIST (HWCFG6 P14.4). See PMS, HWCFG[6]

3 Pin definition and functions

- PU2 = with pull-up device connected during reset ($\overline{\text{PORST}} = 0$). The default state of GPIOs (Px.y) after reset ($\overline{\text{PORST}} = 1$) is controlled through PORT reset value determined by PMS_PADCON.ALLTRIST (HWCFG6 P14.4). In Standby Mode it is controlled through PMS_PADCON.ALLTRIST (HWCFG6 P14.4)
- PD = with pull-down device connected during startup. The default state during and after reset ($\overline{\text{PORST}} = 0$) is pull-down. HighZ in Standby mode
- PD3 = The default state of Pins during reset ($\overline{\text{PORST}} = 0$) is controlled through PMS_PADCON.ALLTRIST (HWCFG6 P14.4) with pull-down behavior if ALLTRIST=0. The default state after PORST release is pull-down with transition of the Pad Level from AL to TTL. In Standby Mode it is controlled through PMS_PADCON.ALLTRIST (HWCFG6 P14.4) with pull-down behavior if ALLTRIST=0
- OD = open drain during reset ($\overline{\text{PORST}} = 0$)
- ES = Supports Emergency Stop
- ES1 = ES. ES is controlled by Pn_PCSRSEL register
- ES2 = ES. ES can be overruled by DXCPL - DAP over CAN physical layer, No overruling for DXCM - Debug over CAN message
- ES3 = ES. ES can be overruled by JTAG mode if this pin is used as TDI
- ES4 = ES. ES can be overruled by JTAG or Three Pin DAP mode
- ES5 = ES. ES can be overruled by the Standby Controller - SCR - if implemented. Overruling can be disabled via the control register P33_PCSR and P34_PCSR
- ES6 = ES. On LVDS TX pads the ES affects the pads only in CMOS mode, not in LVDS mode. Thus, only when LPCRx.TX_EN selects the CMOS Mode, the output is switched off in the ES event

Related information

[Logic symbols for package variants](#) on page 27

[BGA436_STD package variant pin configuration](#) on page 28

[BGA292_STD package variant pin configuration](#) on page 258

[Pad Sequence](#) on page 422

4 Electrical characteristics

4.1 Parameter interpretation

The parameters listed in this section represent both the characteristics of the device and its requirements on the system. To aid the interpretation of the parameters when evaluating them for a design, they are marked with a two-letter abbreviation in the 'Symbol' column.

- **CC**
 - Controller Characteristics which are a distinctive feature of the device and must be taken into account for a system design
- **SR**
 - System Requirements which must be provided by the microcontroller system in which the device is designed in to

4.2 Absolute maximum ratings

Note: Stresses above the values listed under 'absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational conditions of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

4.2.1 Absolute maximum ratings

Table 52 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Storage Temperature	T_{ST} SR	-65	-	150	°C	Up to 65 h at $T_J = 150^{\circ}\text{C}$
Maximum Junction Temperature	T_J SR	-40	-	165	°C	
Voltage at $V_{DDEXTDC}$ EVRC supply pin with respect to $V_{SSEXTDC}$	$V_{DDEXTDC}$ SR	-0.7	-	7.5	V	Up to 2.8 h; EVRC in reset (no switching)
Voltage at V_{DDM} , V_{DDEXT} / $V_{DDEXTHS}$, V_{DDFLEX} and $V_{DDEVRSB}$ power supply pins with respect to V_{SSEXT}	V_{PADIO} SR	-0.7	-	6.5	V	Up to 2.8 h
		-0.7	-	5.7	V	Up to 72 h
Voltage at V_{DD} and V_{DDPHYX} power supply pins with respect to V_{SS} ^{1) 2)}	V_{DD} SR	-0.7	-	1.2	V	Up to 2.8 h
		-0.7	-	1.14	V	Up to 72 h
Voltage at V_{DDPHYX} power supply pins with respect to V_{SS}	V_{DDPHYX} SR	-0.7	-	2.4	V	Up to 2.8 h
		-0.7	-	2.0	V	Up to 72 h
Voltage on all analog and class S input pins with respect to V_{SS} ³⁾	V_{IN} SR	-0.7	-	6.5	V	Up to 2.8 h
Voltage on V_{DDPHYX} (HSPHY) input pins with respect to V_{SSPHY} ³⁾	V_{IN} SR	-0.7	-	1.2	V	Up to 2.8 h
Voltage on all other input pins with respect to V_{SS} ³⁾	V_{IN} SR	-0.7	-	6.5	V	Up to 2.8 h
Input current on any pin during overload condition ⁴⁾	I_{IN} SR	-10	-	10	mA	Up to 2.8 h
Absolute maximum sum of all input circuit currents during overload condition for all ports ⁴⁾	ΣI_{INx} SR	-100	-	100	mA	

1) Valid for cumulated overshoots of up to 2.8 h

2) Due to EVRC output voltage oscillation during switch off phase, V_{DD} can drop down to -0.7 V. For V_{DD} an input level down up to -0.7 V during switch off phase will not cause any damage or reliability issues.

3) Voltages below V_{IN} (Min) have no impact to the device reliability as long as the times and currents defined in section Pin reliability in overload for the affected pad(s) are not violated.

4) This parameter is an Absolute Maximum Rating. Exposure to Absolute Maximum Ratings for extended periods of time may damage the device

4.3 Pin reliability in overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

The following table defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- Allowed time interval (defined in Note column) for overload condition is not exceeded. If no time limit is defined, the allowed time includes example temperature profiles. The number of hours in example temperature profiles are examples only, and the applicable numbers are defined by the customer profiles accepted by Infineon.
- Operating conditions are met for
 - pad supply levels
 - temperature

If a pin current is out of the operating conditions but within the overload parameters, then the parameters functionality of this pin as stated in the operating conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Related information

[Operating conditions](#) on page 451

[Example temperature profiles](#) on page 457

4.3.1 Overload characteristics

Table 53 Overload characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input current on any digital pin during overload condition	I_{IN}	-5	-	5	mA	Except LVDS
		-15 ¹⁾	-	15 ¹⁾	mA	Except LVDS; limited to max. 20 pulses with 1ms pulse length
Input current on LVDS pin during overload condition	I_{INLVDS}	-3	-	3	mA	
Input current on analog input pin during overload condition	I_{INANA}	-5	-	5	mA	Limited to 60 h over lifetime
		-3	-	3	mA	
Absolute sum of all analog input currents for analog inputs during overload condition	I_{INSA}	-20	-	20	mA	
Absolute maximum sum of all input circuit currents during overload condition (digital and analog combined)	ΣI_{INS}	-100	-	100	mA	
Signal voltage over/undershoot at GPIOs	V_{OVS}	$V_{SS} - 2$	-	$V_{DDIO} + 2$ ²⁾	V	Limited to 60 h over lifetime; valid for non LVDS and analog pads

(table continues...)

Table 53 (continued) Overload characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Sum of all inactive device pin currents	I_{IDS}	-100	-	100	mA	
Static pin output current	$I_{OUT\ CC}$	-	-	2.5	mA	100% duty cycle; output driver = medium
		-	-	5	mA	100% duty cycle; output driver = strong
Overload coupling factor for digital inputs, negative	$K_{OVDN\ CC}$	-	-	$3 \cdot 10^{-4}$		Overload injected on GPIO non LVDS pad and affecting neighbour fast pads; $-5\text{ mA} < I_{IN} < 0\text{ mA}$
		-	-	$1 \cdot 10^{-4}$		Overload injected on GPIO non LVDS pad and affecting neighbour slow pads; $-5\text{ mA} < I_{IN} < 0\text{ mA}$
		-	-	0.87		Overload injected on LVDS RX pad and affecting neighbour LVDS pads
		-	-	0.55		Overload injected on LVDS TX pad and affecting neighbour LVDS pads
Overload coupling factor for digital inputs, positive	$K_{OVDP\ CC}$	-	-	$1.5 \cdot 10^{-3}$		Overload injected on GPIO non LVDS pad and affecting neighbour GPIO non LVDS pads
		-	-	1		Overload injected on LVDS RX pad and affecting neighbour LVDS pads
		-	-	$5 \cdot 10^{-3}$		Overload injected on LVDS TX pad and affecting neighbour LVDS pads
Overload coupling factor for analog inputs, negative ³⁾	$K_{OVAN\ CC}$	-	-	$1 \cdot 10^{-4}$		Analog inputs overlaid with slow pads or pull down diagnostics; $-5\text{ mA} < I_{IN} < 0\text{ mA}$
		-	-	$1 \cdot 10^{-5}$		else $-5\text{ mA} < I_{IN} < 0\text{ mA}$
Overload coupling factor for analog inputs, positive ^{3) 4)}	$K_{OVAP\ CC}$	-	-	$2 \cdot 10^{-4}$		Analog inputs overlaid with slow pads or pull down diagnostics; $0\text{ mA} < I_{IN} < 5\text{ mA}$
		-	-	$2 \cdot 10^{-5}$		else $0\text{ mA} < I_{IN} < 5\text{ mA}$

- 1) Reduced TMADC / DSADC (if feature available) result accuracy and / or GPIO input levels (V_{IL} and V_{IH}) can differ from specified parameters.
2) VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB
3) Overload coupling on analog inputs is caused by parasitic effects between pads, input multiplexers and surrounding structures. The given parameters have been verified for all permutations of channels. Also watch multiple connections of a pin to several channels.

4 Electrical characteristics

- 4) In case of overload condition on analog inputs, the V_{DDEXT}/V_{DDM} supply must not float.
-

4.4 Operating conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the TC49xN STD.

Digital supply voltages applied to the TC49xN STD must be static regulated voltages.

All parameters specified in the following tables refer to these operating conditions (see table below), unless otherwise stated in the Note / Test Condition column.

Related information

[Pin reliability in overload](#) on page 448

4.4.1 Clock operating conditions

Table 54 Clock operating conditions

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
System PLL and Peripheral PLL clocks						
PLL0 output frequency from SYS PLL	$f_{\text{PLL0}} SR$	25	-	400	MHz	
PLL1 output frequency from PER PLL	$f_{\text{PLL1}} SR$	25	-	160	MHz	
PLL2 output frequency from PER PLL	$f_{\text{PLL2}} SR$	50	-	200	MHz	
PLL3 output frequency from PER PLL	$f_{\text{PLL3}} SR$	50	-	400 ¹⁾	MHz	
System clocks - CPU						
CPU frequency (All CPUs)	$f_{\text{CPUx}} SR$	25 ²⁾	-	400	MHz	
CPU-CS frequency	$f_{\text{CPU\_CS}} SR$	25 ²⁾	-	200	MHz	
PPU frequency	$f_{\text{PPU}} CC$	25 ²⁾	-	400	MHz	
System clocks						
SRI frequency	$f_{\text{SRI}} SR$	25 ²⁾	-	400	MHz	
SPB frequency	$f_{\text{SPB}} SR$	25 ²⁾	-	100	MHz	
CPB frequency	$f_{\text{CPB}} SR$	25 ³⁾	-	200	MHz	
TPB frequency ⁴⁾	$f_{\text{TPB}} SR$	-	-	200	MHz	
FSI frequency	$f_{\text{FSI}} SR$	25 ⁵⁾	-	100	MHz	
GTM frequency	$f_{\text{GTM}} SR$	-	-	200	MHz	
eGTM frequency	$f_{\text{eGTM}} SR$	-	-	400	MHz	
STM frequency	$f_{\text{STM}} SR$	-	-	200	MHz	
LETH frequency	$f_{\text{LETH}} SR$	125	-	200	MHz	
MCANH frequency	$f_{\text{MCANH}} SR$	f_{MCAN}	-	200	MHz	
CANXL host frequency	$f_{\text{CANXLH}} SR$	f_{CANXL}	-	200	MHz	
Peripheral clocks						
DSADC frequency	$f_{\text{DSADC}} SR$	-	160 ⁶⁾	-	MHz	
(table continues...)						

(table continues...)

Table 54 (continued) **Clock operating conditions**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TMADC frequency ⁷⁾	$f_{\text{ADC}} \text{ SR}$	-	160 ⁶⁾	-	MHz	
ERAY frequency	$f_{\text{ERAY}} \text{ SR}$	-	80	-	MHz	
ASCLIN frequency	$f_{\text{ASCLINx}} \text{ SR}$	-	-	200	MHz	
CAN frequency	$f_{\text{MCAN}} \text{ SR}$	-	-	160	MHz	
CANXL frequency	$f_{\text{CANXL}} \text{ SR}$	-	-	160	MHz	
LETH frequency	$f_{\text{LETH100}} \text{ SR}$	-	200 ⁶⁾	-	MHz	Setting required when TC14 3 pin interface is used.
MSC frequency	$f_{\text{MSC}} \text{ SR}$	-	-	200	MHz	
I2C frequency	$f_{\text{I2C}} \text{ SR}$	-	-	100	MHz	
QSPI frequency	$f_{\text{QSPI}} \text{ SR}$	-	-	200	MHz	
xSPI frequency ⁸⁾	$f_{\text{XSPI}} \text{ SR}$	-	-	200 ⁹⁾	MHz	
SGBT frequency	$f_{\text{SGBT}} \text{ SR}$	-	20	25	MHz	
HRPWM reference clock frequency	$f_{\text{HRPWM}} \text{ SR}$	-	f_{PLL0}	-	MHz	In case of HRPWM operation f_{PLL0} has to be set to 400 MHz

- 1) 400 MHz is the maximum PLL3 operating frequency for test operations only. It is strongly recommended that applications use the PLL3 output frequency of 200 MHz.
- 2) In case of operation with the $f(\text{MIN})$ value the ratio of $f(\text{MIN}) / f_{\text{SR1}}$ and $f(\text{MIN}) / f_{\text{SPB}}$ shall be 1/1
- 3) In case of operation with the $f(\text{MIN})$ value the ratio of $f(\text{MIN}) / f_{\text{SR1}}$, $f(\text{MIN}) / f_{\text{SPB}}$ and $f(\text{MIN}) / f_{\text{CPB}}$ shall be 1/1/1
- 4) f_{TPB} needs to be at least two times higher than f_{SPB}
- 5) For FSI frequency $f_{\text{FSI}} < 100$ MHz the bank sleep feature shall not be used to ensure a proper shutdown operation of the NVM in case of a reset. Operation at $f_{\text{FSI}}(\text{Min})$ prolongs data memory and SOTA program memory write times significantly.
- 6) The proper functionality of the module can only be ensured for the typical clock frequency setting.
- 7) This clock is also used for CDSP modules (if available)
- 8) The appropriate baud rate divider in CCU and XSPI for the maximum supported data rate in each device must be selected for both fast (via HSPHY, if applicable) and slow (via GPIO) XSPI interfaces
- 9) The max. frequency setting is also valid for the clock named $f_{\text{XSPI SL}}$.

Related information

[Supply operating conditions](#) on page 453

[Limitation of supply voltage over time](#) on page 455

[Temperature operating conditions](#) on page 456

[Example temperature profiles](#) on page 457

4.4.2 Supply operating conditions

Table 55 Supply operating conditions

Supply operating conditions at pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
External supply voltage for EVRC DCDC regulator and MOSFET gate driver	$V_{DDEXTDC}$ SR	4.95 ¹⁾	-	7	V	HWCFG [2:1] = [11]. High-voltage $V_{DDEXTDC}$ mode with EVRC active.
		2.97 ¹⁾	-	5.5	V	HWCFG [2:1] = [00, 01 or 10]. Low-voltage $V_{DDEXTDC}$ modes.
External supply voltage for IO supply pins	V_{DDEXT} SR	4.5	5.0	5.5 ²⁾	V	Nominal 5 V Pad / Port Pin supply range. 5 V pad parameters are valid. 5 V NVM programming range
		3.6	-	4.5	V	Allowed only during transients and not a nominal use case. 3.3 V pad parameters are valid; a running NVM command sequence (e.g. program or erase) shall be suspended or aborted
		2.97	3.3	3.63	V	Nominal 3.3 V Pad / Port Pin supply range. 3.3 V pad parameters are valid. 3.3 V NVM programming range
External supply voltage for IO supply pins	$V_{DDEXTHS}$ SR	4.5	5.0	5.5 ²⁾	V	Nominal 5 V Pad / Port Pin supply range. 5 V pad parameters are valid
		3.6	-	4.5	V	Allowed only during transients and not a nominal use case. 3.3 V pad parameters are valid
		2.97	3.3	3.63	V	Nominal 3.3 V Pad / Port Pin supply range. 3.3 V pad parameters are valid
External supply voltage for main XTAL/Oscillator ³⁾	$V_{DDEXTOSC}$ SR	4.5	5.0	5.5 ²⁾	V	Nominal 5V Pad / Port Pin supply range. 5V pad parameters are valid. 5V NVM programming range
		3.6	-	4.5	V	Allowed only during transients and not a nominal use case. 3.3 V pad parameters are valid
		2.97	3.3	3.63	V	Nominal 3.3 V Pad / Port Pin supply range. 3.3 V pad parameters are valid. 3.3 V NVM programming range
External supply voltage for PMS, standby domains, standby pins and SCR	$V_{DDEVRSB}$ SR	4.5 ⁴⁾	5	5.5 ²⁾	V	
		2.97 ⁴⁾	3.3	3.63	V	

(table continues...)

Table 55 (continued) Supply operating conditions

Supply operating conditions at pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
External supply voltage for ADC modules and ANx analog and class S input pins with respect to VSSM	$V_{DDM} SR$	4.5	5.0	5.5 ²⁾	V	Nominal ADC supply voltage range. ADC 5 V parameters are valid
		3.6	-	4.5	V	Allowed only during transients and not a nominal use case. Degraded ADC parameters are valid (see TMADC 5V chapter)
		2.97	3.3	3.63	V	Nominal ADC supply voltage range. Degraded ADC parameters are valid (see TMADC 5V chapter)
External supply voltage for IO supply for Flex port	$V_{DDFLEX} SR$	4.5	5.0	5.5 ²⁾	V	5 V pad parameters are valid
		2.97	3.3	3.63	V	3.3 V pad parameters are valid
External supply voltage for HSPHY module ⁵⁾	$V_{DDPHPHYX} SR$	1.62	1.8	1.98 ⁶⁾	V	
Supply Voltage for core logic (V_{DD}) at unloaded supply pin. ⁷⁾	$V_{DD} SR$	0.943 ⁸⁾	1.025	1.128 ⁹⁾	V	V_{DD} (VID_CON.VDDNOM) setpoint value for slow and typical devices. V_{DD} setpoint value, if no voltage scaling possible (e.g. in case of fixed external supply voltage)
		0.897 ⁸⁾	0.975	1.073 ⁹⁾	V	V_{DD} (VID_CON.VDDNOM) setpoint value for fast devices
Supply Voltage for HSPHY core logic (V_{DDPHYX}) at unloaded supply pin	$V_{DDPHYX} SR$	0.943	1.025	1.107 ⁹⁾	V	V_{DDPHYX} (VID_CON.VDDNOM) setpoint value for slow and typical devices. V_{DDPHYX} setpoint value, if no voltage scaling possible (e.g. in case of fixed external supply voltage)
		0.897	0.975	1.053 ⁹⁾	V	V_{DDPHYX} (VID_CON.VDDNOM) setpoint value for fast devices
Core ground supply	$V_{SS} SR$	0	-	-	V	
Analog ground supply V_{SSM}	$V_{SSM} CC$	-0.1	0	0.1	V	
Minimum external voltage to ensure defined pad states for $V_{DDEVRSB}$ supplied pins	$V_{DDPPSB} CC$	1.3 ¹⁰⁾	-	-	V	Default pad pull-up or tristate is ensured at respective $V_{DDEVRSB}$ supply level
Minimum external voltage to ensure defined pad states for V_{DDEXT} supplied pins	$V_{DDPPA} CC$	1.3 ¹⁰⁾	-	-	V	Default pad pull-up or tristate is ensured at respective V_{DDEXT} supply level

(table continues...)

Table 55 (continued) Supply operating conditions

Supply operating conditions at pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
External supply voltage for Standby SRAM	$V_{\text{DDSB SR}}$	0.943	1.025	1.107	V	VDDSB (VID_CON.VDDNOM) setpoint value for slow and typical devices. VDDSB setpoint value, if no voltage scaling is possible (e.g. in case of fixed external supply voltage)
		0.897	0.975	1.053	V	VDDSB (VID_CON.VDDNOM) setpoint value for fast devices

- 1) V_{DDEXTDC} supply voltage is allowed to drop down to 2.8 V during device start-up cranking phase.
- 2) Voltage overshoot up to 6.5 V is permissible, provided that the duration is less than 2 h cumulated. ADC accuracy is reduced and leakage current is increased. The voltage life time profile limitations need to be considered.
- 3) V_{DDEXTOSC} and V_{DDEXT} shall be supplied from the same regulator source
- 4) V_{DDEVRSB} supply voltage is allowed to drop down to 2.76 V during device start-up and operation mode transitions, and to 2.6 V during standby modes.
- 5) If at least one HSPHYx module is used, all VDDPHPHYx and VDDPHYx supply rails in the device shall be supplied complying to operating range limits.
- 6) Voltage overshoot up to 2.4 V is permissible, provided that the duration is less than 2 h cumulated.
- 7) The V_{DD} voltage on the loaded VDD ball would be higher than that on the internal sense point indicated by the unloaded VDD_SENSE pin with respect to unloaded VSS_SENSE ball. The difference is attributed to the static and dynamic core voltage drop on the power distribution network. The loaded V_{DD} voltage is indicated by VDDPAD monitor and unloaded V_{DD} internal voltage is indicated by the VDD monitor respectively. It is expected that the external regulator static + dynamic voltage undershoot at unloaded VDD_SENSE point is limited to V_{DD} (Typ) - 6% as is documented in the max pattern current consumption use case to have adequate headroom for voltage monitoring and margin towards reset (VDDPRIUV limit).
- 8) For $V_{\text{DD}} \text{ VDDPRIUV (MIN)} \leq V_{\text{DD}} < V_{\text{DD}} \text{ (MIN)}$ core logic operation is validated for patterns without additional load jumps to ensure device start-up. Analog performance of ADCs or HSPHYx are not being guaranteed. Operation at rated frequency is ensured in production test down to VDD VDDPRIUV reset limit at VDD sense point.
- 9) Voltage overshoot up to 1.2 V is permissible, provided that the duration is less than 2 h cumulated. ADC accuracy is reduced and leakage current is increased. The voltage life time profile limitations need to be considered.
- 10) HWCFG[6] pin is latched and pull-up or tristate is activated at Port pins when V_{DDEXT} or V_{DDEVRSB} has reached this level.

Related information

[Clock operating conditions](#) on page 451

[Limitation of supply voltage over time](#) on page 455

[Temperature operating conditions](#) on page 456

[Example temperature profiles](#) on page 457

4.4.3 Limitation of supply voltage over time

The maximum operation voltage for $V_{\text{DDEXT/DDM}}$ supply rails is limited over the complete lifetime.

Note: *The following voltage profile is an example. Application specific voltage profiles need to be aligned and approved by Infineon Technologies for the fulfillment of quality and reliability targets.*

Table 56 **Example voltage profile 1**

$V_{DDEXT/DDM}$	Duration [h]
$5.4\text{ V} < V_{DDEXT/DDM} \leq 5.5\text{ V}$	$\leq 5\%$ of lifetime
$5.15\text{ V} < V_{DDEXT/DDM} \leq 5.4\text{ V}$	$\leq 15\%$ of lifetime
$4.85\text{ V} < V_{DDEXT/DDM} \leq 5.15\text{ V}$	$\leq 60\%$ of lifetime
$4.6\text{ V} < V_{DDEXT/DDM} \leq 4.85\text{ V}$	$\leq 15\%$ of lifetime
$4.5\text{ V} < V_{DDEXT/DDM} \leq 4.6\text{ V}$	$\leq 5\%$ of lifetime

The maximum operation voltage for V_{DD} supply rails is limited over the complete lifetime.

Note: *The following voltage profile is an example. Application specific voltage profiles need to be aligned and approved by Infineon Technologies for the fulfillment of quality and reliability targets.*

Table 57 **Example voltage profile 2**

V_{DD}	Duration [h]
$V_{DD, typ} - 3\% \text{ of } V_{DD, typ} < V_{DD} \leq V_{DD, typ} + 3\% \text{ of } V_{DD, typ}$	$\leq 90\%$ of lifetime
Operating $V_{DD, min} < V_{DD} \leq V_{DD, typ} - 3\% \text{ of } V_{DD, typ}$ AND $V_{DD, typ} + 3\% \text{ of } V_{DD, typ} < V_{DD} \leq \text{Operating } V_{DD, max}$	$\leq 10\%$ of lifetime
Operating $V_{DD, max} < V_{DD} \leq \text{Absolute maximum } V_{DD, max}$	as documented in absolute maximum ratings section.

Related information

[Clock operating conditions](#) on page 451

[Supply operating conditions](#) on page 453

[Temperature operating conditions](#) on page 456

[Example temperature profiles](#) on page 457

4.4.4 Temperature operating conditions

Table 58 **Temperature operating conditions**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Ambient Temperature	T_A SR	-40	-	125	°C	valid for all SAK products
Junction Temperature	T_J SR	-40	-	160	°C	valid for all SAK products

Related information

[Clock operating conditions](#) on page 451

[Supply operating conditions](#) on page 453

[Limitation of supply voltage over time](#) on page 455

[Example temperature profiles](#) on page 457

4.4.5 Example temperature profiles

The maximum operating junction temperature T_J is limited over the complete lifetime.

Note: *The following temperature profiles are provided as a reference distribution across the lifetime of the product. Application specific temperature profiles shall be separately aligned through Infineon customer support team and approved by Infineon Technologies towards fulfillment of the respective quality and reliability targets.*

Table 59 Standard temperature profile reference

Junction temperature T_J (°C)	Duration (hours)	Comments
≤ 160	300	Device in Operation in RUN mode
≤ 150	600	Device in Operation in RUN mode
≤ 145	1000	Device in Operation in RUN mode
≤ 140	1000	Device in Operation in RUN mode
≤ 135	1000	Device in Operation in RUN mode
≤ 130	1200	Device in Operation in RUN mode
≤ 125	3000	Device in Operation in RUN mode
≤ 120	5000	Device in Operation in RUN mode
≤ 115	5000	Device in Operation in RUN mode
≤ 110	5000	Device in Operation in RUN mode
≤ 105	1000	Device in Operation in RUN mode
≤ 100	400	Device in Operation in RUN mode
	24500	Total operational lifetime
≤ 40	151000	Total non-operational lifetime Device in Standby 0 mode or is switched off

Table 60 Extended temperature profile reference

Junction temperature T_J (°C)	Duration (hours)	Comments
≤ 150	300	Device in Operation in RUN mode
≤ 140	600	Device in Operation in RUN mode
≤ 130	1000	Device in Operation in RUN mode
≤ 120	1800	Device in Operation in RUN mode
≤ 110	20000	Device in Operation in RUN mode
≤ 105	12300	Device in Operation in RUN mode
≤ 85	3000	Device in Operation in RUN mode
≤ 40	500	Device in Operation in RUN mode
≤ -40	500	Device in Operation in RUN mode
≤ 90	30000	Device in Operation in RUN mode (reduced performance)

(table continues...)

Table 60 (continued) **Extended temperature profile reference**

Junction temperature T_J (°C)	Duration (<i>hours</i>)	Comments
≤ 85	30000	Device in Operation in RUN mode (reduced performance)
	100000	Total operational lifetime
≤ 40	75500	Total non-operational lifetime Device in Standby 0 mode or is switched off

Related information

[Clock operating conditions](#) on page 451

[Supply operating conditions](#) on page 453

[Limitation of supply voltage over time](#) on page 455

[Temperature operating conditions](#) on page 456

[Pin reliability in overload](#) on page 448

4.5 Switchable pad characteristics

The pad classes Slow GPIO and Fast GPIO support both Automotive Level (AL) or TTL level (TTL) operation. Parameters are defined for AL operation and degraded in TTL operation.

4.5.1 – PORST Pad characteristics

Table 61 – PORST Pad characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
PORST pad output current ¹⁾	$I_{\text{PORST CC}}$	13	-	-	mA	$V_{\text{DDEXT}} = 2.97 \text{ V}$; $V_{\text{PORST}} = 0.9 \text{ V}$
Spike filter always blocked pulse duration	$t_{\text{SF1 CC}}$	-	-	80	ns	
Spike filter pass-through blocked pulse duration	$t_{\text{SF2 CC}}$	276	-	-	ns	Without additional PORST Digital Filter active (PORSTDF = 0)
Input high voltage level	$V_{\text{IH SR}}$	1.4	-	-	V	$V_{\text{DDEXT}} = 2.97 \text{ V}$
		2.0	-	-	V	TTL; $V_{\text{DDEXT}} = 4.5 \text{ V}$
Input low voltage level	$V_{\text{IL SR}}$	-	-	0.5	V	$V_{\text{DDEXT}} = 2.97 \text{ V}$
		-	-	0.8	V	TTL; $V_{\text{DDEXT}} = 4.5 \text{ V}$
Input hysteresis ²⁾	$HYS \text{ CC}$	$0.026 * V_{\text{DDEXT}}$	-	-	V	None of the neighbour pads are used as output
Pull-down current ^{3) 1)}	$I_{\text{PDL CC}}$	15	-	-	μA	V_{IL} ; $V_{\text{DDEXT}} = 2.97 \text{ V}$
		-	-	130	μA	V_{IH} ; TTL
Input leakage current	$I_{\text{OZ CC}}$	-1000	-	1000	nA	$T_J \leq 150^\circ\text{C}$; $(0.1 * V_{\text{DDEXT}}) < V_{\text{IN}} < (0.9 * V_{\text{DDEXT}})$
		-1050	-	1050	nA	$T_J \leq 150^\circ\text{C}$; else
		-1100	-	1100	nA	$T_J \leq T_J (\text{Max})$; $(0.1 * V_{\text{DDEXT}}) < V_{\text{IN}} < (0.9 * V_{\text{DDEXT}})$
		-1150	-	1150	nA	$T_J \leq T_J (\text{Max})$; else
Pin capacitance	$C_{\text{IO CC}}$	-	2	3	pF	In addition 2.5 pF from package to be added

1) It is recommended that PORST pin shall be externally pulled high with a pull-up resistor in the range 1.4 kΩ up to 6.4 kΩ.

2) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.

3) Values for Pull-down resistor is defined via parameter R_{PDL} in table Fast 5 V Pad.

4.5.2 5 V switchable pad characteristics

The pad classes Slow GPIO and Fast GPIO support both Automotive Level (AL) or TTL level (TTL) operation. Parameters are defined for AL operation and degraded in TTL operation.

4.5.2.1 Fast 5V GPIO characteristics

Table 62 Fast 5V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output Parameters						
On-Resistance of pad output	$R_{\text{DS(on) CC}}$	100	225	295	Ohm	Driver = medium; $I_{\text{OH}} / I_{\text{OL}} = 2$ mA
		31	55	80	Ohm	Driver = strong; $I_{\text{OH}} / I_{\text{OL}} = 8$ mA ¹⁾
Rise / Fall time ²⁾	$t_{\text{RF CC}}$	1.6	-	3.2	ns	$C_{\text{L}} = 25$ pF; driver = strong, edge = sharp; measured from 20 % to 80 % of V_{DDIO} ; else
		4+0.55* C_{L}	4+0.75* C_{L}	12+1.0* C_{L}	ns	Driver = medium; $C_{\text{L}} \leq 200$ pF; measured from 10 % to 90 % of V_{DDIO}
		1.0+0.18 * C_{L}	2.5+0.27 * C_{L}	5.0+0.37 * C_{L}	ns	Driver = strong, edge = medium; $C_{\text{L}} \leq 200$ pF; measured from 10 % to 90 % of V_{DDIO}
		0.5+0.08 * C_{L}	0.5+0.11 * C_{L}	1.0+0.17 * C_{L}	ns	Driver = strong, edge = sharp; $C_{\text{L}} \leq 200$ pF; measured from 10 % to 90 % of V_{DDIO}
Asymmetry of sending ³⁾	$t_{\text{TX\_ASYM CC}}$	-1	-	1	ns	$C_{\text{L}} = 15$ pF; valid for all data rates excluding clock tolerance
Input parameters						
Input frequency	$f_{\text{IN CC}}$	-	-	160	MHz	
Input high voltage level	$V_{\text{IH SR}}$	0.7 * V_{DDIO}	-	-	V	AL; else
		2.0	-	-	V	TTL
Input low voltage level	$V_{\text{IL SR}}$	-	-	0.44 * V_{DDIO}	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	$V_{\text{ILD SR}}$	-95	-	95	mV	Max. variation of 1 ms; $V_{\text{DDIO}} =$ constant; AL

(table continues...)

Table 62 (continued) Fast 5V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input hysteresis ⁴⁾	HYS CC	0.09 * V_{DDIO}	-	-	V	None of the neighbour pads are used as output; AL
		0.06 * V_{DDIO}	-	-	V	None of the neighbour pads are used as output; TTL
		75	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; AL
		185 ⁵⁾	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; TTL
Pull-up current ⁶⁾	I_{PUH} CC	30	-	-	µA	V_{IH} ; AL or TTL
		-	-	130	µA	V_{IL} ; AL or TTL
Equivalent resistance to pull-up device	R_{PUH} CC	30	-	42	kOhm	$0.1 * V_{DDIO} \leq V_{IN} \leq V_{DDIO}$; Automotive level
		56	-	78	kOhm	$0.1 * V_{DDIO} \leq V_{IN} \leq V_{DDIO}$; TTL level
Pull-down current ⁷⁾	I_{PDL} CC	30	-	-	µA	V_{IL} ; AL
		28	-	-	µA	V_{IL} ; TTL
		-	-	130	µA	V_{IH} ; AL or TTL
Equivalent resistance to pull-down device	R_{PDL} CC	43	-	58	kOhm	$0.1 * V_{DDIO} \leq V_{IN} \leq V_{DDIO}$; Automotive level
		18	-	25	kOhm	$0.1 * V_{DDIO} \leq V_{IN} \leq V_{DDIO}$; TTL level

(table continues...)

Table 62 (continued) Fast 5V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input leakage current	$I_{OZ\ CC}$	-3900	-	3900	nA	$T_J \leq 150^\circ\text{C}$; $(0.1 * V_{DDIO}) < V_{IN} < (0.9 * V_{DDIO})$
		-4800	-	4800	nA	$T_J \leq 150^\circ\text{C}$; else
		-4100	-	4100	nA	$T_J \leq T_J(\text{Max})$; $(0.1 * V_{DDIO}) < V_{IN} < (0.9 * V_{DDIO})$
		-5100	-	5100	nA	$T_J \leq T_J(\text{Max})$; else
		-3700	-	3700	nA	$T_J \leq 150^\circ\text{C}$; $(0.1 * V_{DDEXT}/V_{DDEXTHS}) < V_{IN} < (0.9 * V_{DDEXT}/V_{DDEXTHS})$; LVDS_RX / Fast pad type
		-13000	-	13000	nA	$T_J \leq 150^\circ\text{C}$; LVDS_RX / Fast pad type ; else
		-3900	-	3900	nA	$T_J \leq T_J(\text{Max})$; $(0.1 * V_{DDEXT}/V_{DDEXTHS}) < V_{IN} < (0.9 * V_{DDEXT}/V_{DDEXTHS})$; LVDS_RX / Fast pad type
		-14500	-	14500	nA	$T_J \leq T_J(\text{Max})$; LVDS_RX / Fast pad type; else
		-4600	-	4600	nA	$T_J \leq 150^\circ\text{C}$; $(0.1 * V_{DDEXT}/V_{DDEXTHS}) < V_{IN} < (0.9 * V_{DDEXT}/V_{DDEXTHS})$; LVDS_TX / Fast pad type
		-5800	-	5800	nA	$T_J \leq 150^\circ\text{C}$; LVDS_TX / Fast pad type ; else
		-4800	-	4800	nA	$T_J \leq T_J(\text{Max})$; $(0.1 * V_{DDEXT}/V_{DDFLEX}) < V_{IN} < (0.9 * V_{DDEXT}/V_{DDFLEX})$; LVDS_TX / Fast pad type
		-6100	-	6100	nA	$T_J \leq T_J(\text{Max})$; LVDS_TX / Fast pad type; else
Pin capacitance	$C_{IO\ CC}$	-	2	3	pF	In addition 2.5 pF from package to be added
Pad set-up time to get an software update of the configuration active	$t_{SET\ CC}$	-	-	100	ns	Time measured from alternating writing of port registers PADCFG.GPIO.SET and PADCFG.GPIO.CLR until toggling of pad

- 1) The 8 mA condition is an Infineon internal test condition and not allowed as DC (or permanent) load on this standard pad.
- 2) In the formulas the value of C_L needs to be entered in pF to obtain results in ns
- 3) This parameter defines the difference of the output signal delay parameter for rising and falling edge
- 4) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
- 5) For Pin P01.14 the Min value is 165 mV.
- 6) Values for Pull-up resistor is defined via parameter R_{PUH} in table Fast 5 V Pad.

4 Electrical characteristics

7) Values for Pull-down resistor is defined via parameter R_{PDL} in table Fast 5 V Pad.

Related information

[Slow 5V GPIO characteristics](#) on page 463

[Class S 5V characteristics](#) on page 465

4.5.2.2 Slow 5V GPIO characteristics

Table 63 Slow 5V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
On-Resistance of pad output	$R_{DS\,ON\,CC}$	100	225	295	Ohm	Driver = medium; $I_{OH}/I_{OL} = 2$ mA
Rise / Fall time ¹⁾	$t_{RF\,CC}$	$4+0.55 \cdot C_L$	$4+0.75 \cdot C_L$	$12+1 \cdot C_L$	ns	Driver = medium, edge = medium; $C_L \leq 200$ pF; measured from 10 % to 90 % of V_{DDIO}
		$1.5+0.25 \cdot C_L$	$2.5+0.40 \cdot C_L$	$7+0.55 \cdot C_L$	ns	Driver = medium, edge = sharp; $C_L \leq 200$ pF; measured from 10 % to 90 % of V_{DDIO}
Asymmetry of sending ²⁾	$t_{TX\_ASYM\,CC}$	-1.3	-	1.3	ns	$C_L = 15$ pF; valid for all data rates excluding clock tolerance
Input frequency	$f_{IN\,CC}$	-	-	160	MHz	
Input high voltage level	$V_{IH\,SR}$	$0.7 \cdot V_{DDIO}$	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	$V_{IL\,SR}$	-	-	$0.44 \cdot V_{DDIO}$	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	$V_{ILD\,SR}$	-100	-	100	mV	Max. variation of 1 ms; $V_{DDIO} =$ constant; AL
Input hysteresis ³⁾	$HYS\,CC$	$0.09 \cdot V_{DDIO}$	-	-	V	None of the neighbour pads are used as output; AL
		$0.058 \cdot V_{DDIO}$	-	-	V	None of the neighbour pads are used as output; TTL
		75	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; AL
		210	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; TTL

(table continues...)

Table 63 (continued) Slow 5V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Pull-up current ⁴⁾	$I_{PUH\ CC}$	30	-	-	μA	V_{IH} ; AL or TTL
		-	-	130	μA	V_{IL} ; AL or TTL
Pull-down current ⁵⁾	$I_{PDL\ CC}$	30	-	-	μA	V_{IL} ; AL
		28	-	-	μA	V_{IL} ; TTL
		-	-	130	μA	V_{IH} ; AL or TTL
Input leakage current	$I_{OZ\ CC}$	-1700	-	1700	nA	$T_J \leq 150^\circ\text{C}$; $(0.1 * V_{DDIO}) < V_{IN} < (0.9 * V_{DDIO})$; no analog input
		-2000	-	2000	nA	$T_J \leq 150^\circ\text{C}$; no analog input; else
		-1900	-	1900	nA	$T_J \leq T_J\ (\text{Max})$; $(0.1 * V_{DDIO}) < V_{IN} < (0.9 * V_{DDIO})$; no analog input
		-2200	-	2200	nA	$T_J \leq T_J\ (\text{Max})$; no analog input; else
		-2800	-	2800	nA	$T_J \leq 150^\circ\text{C}$; $(0.1 * V_{DDEXT/DDFLEX}) < V_{IN} < (0.9 * V_{DDEXT/DDFLEX})$; $V_{SSM} < V_{IN} < V_{DDM}$; analog input mapped
		-3300 ⁶⁾	-	3300 ⁶⁾	nA	$T_J \leq 150^\circ\text{C}$; $V_{SSM} < V_{IN} < V_{DDM}$; analog input mapped; else
		-2900	-	2900	nA	$T_J \leq T_J\ (\text{Max})$; $(0.1 * V_{DDEXT/DDFLEX}) < V_{IN} < (0.9 * V_{DDEXT/DDFLEX})$; $V_{SSM} < V_{IN} < V_{DDM}$; analog input mapped
		-3500	-	3500	nA	$T_J \leq T_J\ (\text{Max})$; $V_{SSM} < V_{IN} < V_{DDM}$; analog input mapped; else
Pin capacitance	$C_{IO\ CC}$	-	2	3	pF	In addition 2.5 pF from package to be added
Pad set-up time to get an software update of the configuration active	$t_{SET\ CC}$	-	-	100	ns	Time measured from alternating writing of port registers PADCFG.GPIO.SET and PADCFG.GPIO.CLR until toggling of pad

1) In the formulas the value of C_L needs to be entered in pF to obtain results in ns

2) This parameter defines the difference of the output signal delay parameter for rising and falling edge

3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.

4) Values for Pull-up resistor is defined via parameter R_{PUH} in table Fast 5 V Pad.

5) Values for Pull-down resistor is defined via parameter R_{PDL} in table Fast 5 V Pad.

6) For $(V_{IN} > V_{DDM})$ or $(V_{IN} < V_{SSM})$ leakage is doubled.

Related information

[Fast 5V GPIO characteristics](#) on page 460

[Class S 5V characteristics](#) on page 465

4.5.2.3 Class S 5V characteristics

Table 64 Class S 5V characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input frequency	f_{IN} CC	-	-	160	MHz	
Input high voltage level	V_{IH} SR	0.7 * V_{DDM}	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} SR	-	-	0.44 * V_{DDM}	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	V_{ILD} SR	-70	-	70	mV	Max. variation of 1 ms; V_{DDM} = constant; AL
Input hysteresis ¹⁾	HYS CC	0.09 * V_{DDM}	-	-	V	None of the neighbour pads are used as output; AL
		0.06 * V_{DDM}	-	-	V	None of the neighbour pads are used as output; TTL
		75	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; AL
		290	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; TTL
Pull-up current ²⁾	I_{PUH} CC	30	-	-	μA	V_{IH} ; AL and TTL
		-	-	130	μA	V_{IL} ; AL and TTL
Pull-down current ³⁾	I_{PDL} CC	30	-	-	μA	V_{IL} ; AL
		28	-	-	μA	V_{IL} ; TTL
		-	-	130	μA	V_{IH} ; AL and TTL
Input leakage current	I_{OZ} CC	-900	-	900	nA	$T_J \leq 150^\circ\text{C}$; PDD option available
		-400	-	400	nA	$T_J \leq 150^\circ\text{C}$; else
		-1100	-	1100	nA	$T_J \leq T_J$ (Max); PDD option available
		-500	-	500	nA	$T_J \leq T_J$ (Max); else
Pin capacitance	C_{IO} CC	-	2	3	pF	In addition 2.5 pF from package to be added

(table continues...)

Table 64 (continued) Class S 5V characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Pad set-up time to get an software update of the configuration active	$t_{SET\ CC}$	-	-	100	ns	

- 1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
2) Values for Pull-up resistor is defined via parameter R_{PUH} in table Fast 5 V Pad.
3) Values for Pull-down resistor is defined via parameter R_{PDL} in table Fast 5 V Pad.

Related information

[Fast 5V GPIO characteristics](#) on page 460

[Slow 5V GPIO characteristics](#) on page 463

4.5.3 3.3 V switchable pad characteristics

Pad classes as Slow GPIO and Fast GPIO support both Automotive Level (AL) or TTL level (TTL) operation. Parameters are defined for AL operation and degraded in TTL operation.

4.5.3.1 Fast 3.3V GPIO characteristics

Table 65 Fast 3.3V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
On-Resistance of pad output	$R_{DS\ ON\ CC}$	125	225	320	Ohm	Driver = medium; $I_{OH} / I_{OL} = 2\text{ mA}$
		31	55	80	Ohm	Driver = strong; $I_{OH} / I_{OL} = 8\text{ mA}$ 1)
Rise / Fall time ²⁾	$t_{RF\ CC}$	1.6	-	4.5	ns	$C_L = 25\text{ pF}$; driver = strong, edge = sharp; measured from 20 % to 80 % of V_{DDIO}
		$2+0.57 \cdot C_L$	$5.5+0.75 \cdot C_L$	$10+1.25 \cdot C_L$	ns	Driver = medium; $C_L \leq 200\text{ pF}$; measured from 10 % to 90 % of V_{DDIO}
		$1.5+0.18 \cdot C_L$	$1.5+0.28 \cdot C_L$	$8+0.43 \cdot C_L$	ns	Driver = strong, edge = medium; $C_L \leq 200\text{ pF}$; measured from 10 % to 90 % of V_{DDIO}
		$0.75+0.08 \cdot C_L$	$0.75+0.11 \cdot C_L$	$2.5+0.21 \cdot C_L$	ns	Driver = strong, edge = sharp; $C_L \leq 200\text{ pF}$; measured from 10 % to 90 % of V_{DDIO}
		-	-	5	ns	$C_L = 25\text{ pF}$; driver = strong, edge = sharp; measured from 0.8 V to 2.0 V (RMII)

(table continues...)

Table 65 (continued) Fast 3.3V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Asymmetry of sending ³⁾	t_{TX_ASYM} CC	-1	-	1	ns	$C_L = 15$ pF; valid for all data rates excluding clock tolerance
Input frequency	f_{IN} CC	-	-	160	MHz	
Input high voltage level	V_{IH} SR	0.7 * V_{DDIO}	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} SR	-	-	0.42 * V_{DDIO}	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	V_{ILD} SR	-70	-	70	mV	Max. variation of 1 ms; $V_{DDIO} =$ constant; AL
Input hysteresis ⁴⁾	HYS CC	0.055 * V_{DDIO}	-	-	V	None of the neighbour pads are used as output; AL
		0.081 * V_{DDIO}	-	-	V	None of the neighbour pads are used as output; TTL
		125	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; AL
		220	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; TTL
Pull-up current ⁵⁾	I_{PUH} CC	17	-	-	μA	V_{IH} ; AL
		11	-	-	μA	V_{IH} ; TTL
		-	-	80	μA	V_{IL} ; AL and TTL
Pull-down current ⁶⁾	I_{PDL} CC	19	-	-	μA	V_{IL} ; AL and TTL
		-	-	105	μA	V_{IH} ; AL
		-	-	115	μA	V_{IH} ; TTL

(table continues...)

Table 65 (continued) Fast 3.3V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input leakage current	$I_{OZ\ CC}$	-2300	-	2300	nA	$T_J \leq 150^\circ\text{C}; (0.1 * V_{DDIO}) < V_{IN} < (0.9 * V_{DDIO})$
		-2700	-	2700	nA	$T_J \leq 150^\circ\text{C}; \text{else}$
		-2500	-	2500	nA	$T_J \leq T_J (\text{Max}); (0.1 * V_{DDIO}) < V_{IN} < (0.9 * V_{DDIO})$
		-2900	-	2900	nA	$T_J \leq T_J (\text{Max}); \text{else}$
		-1800	-	1800	nA	$T_J \leq 150^\circ\text{C}; (0.1 * V_{DDEXT/ DDEXTHS}) < V_{IN} < (0.9 * V_{DDEXT/ DDEXTHS}); \text{LVDS\_RX / Fast pad type}$
		-8000	-	8000	nA	$T_J \leq 150^\circ\text{C}; \text{LVDS\_RX / Fast pad type; else}$
		-2000	-	2000	nA	$T_J \leq T_J (\text{Max}); (0.1 * V_{DDEXT/ DDEXTHS}) < V_{IN} < (0.9 * V_{DDEXT/ DDEXTHS}); \text{LVDS\_RX / Fast pad type}$
		-9000	-	9000	nA	$T_J \leq T_J (\text{Max}); \text{LVDS\_RX / Fast pad type; else}$
		-2800	-	2800	nA	$T_J \leq 150^\circ\text{C}; (0.1 * V_{DDEXT/ DDEXTHS}) < V_{IN} < (0.9 * V_{DDEXT/ DDEXTHS}); \text{LVDS\_TX / Fast pad type}$
		-3200	-	3200	nA	$T_J \leq 150^\circ\text{C}; \text{LVDS\_TX / Fast pad type; else}$
		-3000	-	3000	nA	$T_J \leq T_J (\text{Max}); (0.1 * V_{DDEXT/ DDEXTHS}) < V_{IN} < (0.9 * V_{DDEXT/ DDEXTHS}); \text{LVDS\_TX / Fast pad type}$
		-3500	-	3500	nA	$T_J \leq T_J (\text{Max}); \text{LVDS\_TX / Fast pad type; else}$
Pin capacitance	$C_{IO\ CC}$	-	2	3	pF	In addition 2.5 pF from package to be added
Pad set-up time to get an software update of the configuration active	$t_{SET\ CC}$	-	-	100	ns	Time measured from alternating writing of port registers PADCFG.GPIO.SET and PADCFG.GPIO.CLR until toggling of pad

- 1) The 8 mA condition is an Infineon internal test condition and not allowed as DC (or permanent) load on this standard pad.
- 2) In the formulas the value of C_L needs to be entered in pF to obtain results in ns
- 3) This parameter defines the difference of the output signal delay parameter for rising and falling edge
- 4) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise
- 5) Values for Pull-up resistor is defined via parameter R_{PUH} in table Fast 5 V Pad.
- 6) Values for Pull-down resistor is defined via parameter R_{PDL} in table Fast 5 V Pad.

Related information

[Slow 3.3V GPIO characteristics](#) on page 469

[Class S 3.3V characteristics](#) on page 471

4.5.3.2 Slow 3.3V GPIO characteristics

Table 66 Slow 3.3V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
On-Resistance of pad output	$R_{\text{DS(on) CC}}$	125	225	320	Ohm	Driver = medium; $I_{\text{OH}}/I_{\text{OL}} = 2$ mA
Rise / Fall time ¹⁾	$t_{\text{RF CC}}$	$2+0.57 \cdot C_L$	$5.5+0.75 \cdot C_L$	$10+1.25 \cdot C_L$	ns	Driver = medium, edge = medium; $C_L \leq 200$ pF; measured from 10 % to 90 % of V_{DDIO}
		$2+0.30 \cdot C_L$	$3.5+0.50 \cdot C_L$	$5+0.70 \cdot C_L$	ns	Driver = medium, edge = sharp; $C_L \leq 200$ pF; measured from 10 % to 90 % of V_{DDIO}
Asymmetry of sending ²⁾	$t_{\text{TX\_ASYM CC}}$	-1.3	-	1.3	ns	$C_L = 15$ pF; valid for all data rates excluding clock tolerance
Input frequency	$f_{\text{IN CC}}$	-	-	160	MHz	
Input high voltage level	$V_{\text{IH SR}}$	$0.7 \cdot V_{\text{DDIO}}$	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	$V_{\text{IL SR}}$	-	-	$0.42 \cdot V_{\text{DDIO}}$	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	$V_{\text{ILD SR}}$	-70	-	70	mV	Max. variation of 1 ms; $V_{\text{DDIO}} =$ constant; AL
Input hysteresis ³⁾	$HYS CC$	$0.055 \cdot V_{\text{DDIO}}$	-	-	V	None of the neighbour pads are used as output; AL
		$0.081 \cdot V_{\text{DDIO}}$	-	-	V	None of the neighbour pads are used as output; TTL
		125	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; AL
		220	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; TTL

(table continues...)

Table 66 (continued) Slow 3.3V GPIO characteristics

VDDIO corresponds to the supply voltage of the IO supply domains VDDEXT, VDDEXTHS, VDDFLEX and VDDEVRSB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Pull-up current ⁴⁾	$I_{PUH} CC$	17	-	-	μA	V_{IH} ; AL
		11	-	-	μA	V_{IH} ; TTL
		-	-	80	μA	V_{IL} ; AL and TTL
Pull-down current ⁵⁾	$I_{PDL} CC$	19	-	-	μA	V_{IL} ; AL and TTL
		-	-	105	μA	V_{IH} ; AL
		-	-	115	μA	V_{IH} ; TTL
Input leakage current	$I_{OZ} CC$	-1100	-	1100	nA	$T_J \leq 150^\circ C$; $(0.1 * V_{DDIO}) < V_{IN} < (0.9 * V_{DDIO})$; no analog input
		-1200	-	1200	nA	$T_J \leq 150^\circ C$; no analog input; else
		-1200	-	1200	nA	$T_J \leq T_J (Max)$; $(0.1 * V_{DDIO}) < V_{IN} < (0.9 * V_{DDIO})$; no analog input
		-1300	-	1300	nA	$T_J \leq T_J (Max)$; no analog input; else
		-1700	-	1700	nA	$T_J \leq 150^\circ C$; $(0.1 * V_{DDEXT/DDFLEX}) < V_{IN} < (0.9 * V_{DDEXT/DDFLEX})$; $V_{SSM} < V_{IN} < V_{DDM}$; analog input mapped
		-1800 ⁶⁾	-	1800 ⁶⁾	nA	$T_J \leq 150^\circ C$; $V_{SSM} < V_{IN} < V_{DDM}$; analog input mapped; else
		-1800	-	1800	nA	$T_J \leq T_J (Max)$; $(0.1 * V_{DDEXT/DDFLEX}) < V_{IN} < (0.9 * V_{DDEXT/DDFLEX})$; $V_{SSM} < V_{IN} < V_{DDM}$; analog input mapped
		-2000	-	2000	nA	$T_J \leq T_J (Max)$; $V_{SSM} < V_{IN} < V_{DDM}$; analog input mapped; else
Pin capacitance	$C_{IO} CC$	-	2	3	pF	In addition 2.5 pF from package to be added
Pad set-up time to get an software update of the configuration active	$t_{SET} CC$	-	-	100	ns	Time measured from alternating writing of port registers PADCFG.GPIO.SET and PADCFG.GPIO.CLR until toggling of pad

1) In the formulas the value of C_L needs to be entered in pF to obtain results in ns

2) This parameter defines the difference of the output signal delay parameter for rising and falling edge

3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.

4) Values for Pull-up resistor is defined via parameter R_{PUH} in table Fast 5 V Pad.

5) Values for Pull-down resistor is defined via parameter R_{PDL} in table Fast 5 V Pad.

6) For $(V_{IN} > V_{DDM})$ or $(V_{IN} < V_{SSM})$ leakage is doubled.

Related information

[Fast 3.3V GPIO characteristics](#) on page 466

[Class S 3.3V characteristics](#) on page 471

4.5.3.3 Class S 3.3V characteristics

Table 67 Class S 3.3V characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input frequency	f_{IN} CC	-	-	160	MHz	
Input high voltage level	V_{IH} SR	0.7 * V_{DDM}	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} SR	-	-	0.42 * V_{DDM}	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	V_{ILD} SR	-70	-	70	mV	Max. variation of 1 ms; V_{DDM} = constant; AL
Input hysteresis ¹⁾	HYS CC	0.055 * V_{DDM}	-	-	V	None of the neighbour pads are used as output; AL
		0.085 * V_{DDM}	-	-	V	None of the neighbour pads are used as output; TTL
		125	-	-	mV	Two of the neighbour pads are used as output with driver = strong, edge = sharp; AL
Pull-up current ²⁾	I_{PUH} CC	17	-	-	μA	V_{IH} ; AL
		11	-	-	μA	V_{IH} ; TTL
		-	-	80	μA	V_{IL} ; AL and TTL
Pull-down current ³⁾	I_{PDL} CC	19	-	-	μA	V_{IL} ; AL and TTL
		-	-	105	μA	V_{IH} ; AL
		-	-	115	μA	V_{IH} ; TTL
Input leakage current	I_{OZ} CC	-700	-	700	nA	$T_J \leq 150^\circ\text{C}$; PDD option available
		-400	-	400	nA	$T_J \leq 150^\circ\text{C}$; else
		-800	-	800	nA	$T_J \leq T_J$ (Max); PDD option available
		-500	-	500	nA	$T_J \leq T_J$ (Max); else
Pin capacitance	C_{IO} CC	-	2	3	pF	In addition 2.5 pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

4 Electrical characteristics

- 1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
- 2) Values for Pull-up resistor is defined via parameter R_{PUH} in table Fast 5 V Pad.
- 3) Values for Pull-down resistor is defined via parameter R_{PDL} in table Fast 5 V Pad.

Related information

[Fast 3.3V GPIO characteristics](#) on page 466

[Slow 3.3V GPIO characteristics](#) on page 469

4.5.4 Class D characteristics

Table 68 Class D characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input leakage current	$I_{OZ\ CC}$	-1000	-	1000	nA	$T_J \leq 150^\circ\text{C}$; PDD option available
		-800	-	800	nA	$T_J \leq 150^\circ\text{C}$; valid for AN9, AN10, AN34, AN35, AN57
		-100	-	100	nA	$T_J \leq 150^\circ\text{C}$; else
		-1100	-	1100	nA	$T_J \leq T_J (\text{Max})$; PDD option available
		-900	-	900	nA	$T_J \leq T_J (\text{Max})$; valid for AN9, AN10, AN34, AN35, AN57
		-110	-	110	nA	$T_J \leq T_J (\text{Max})$; else
Pin capacitance	$C_{IO\ CC}$	-	2	3	pF	In addition 2.5 pF from package to be added

4.5.5 ADC reference pads characteristics

Table 69 ADC reference pads characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input leakage current for V_{AREF}	$I_{OZ2\ CC}$	-2 ¹⁾	-	2 ¹⁾	μA	$T_J \leq 150^\circ\text{C}$; $V_{AREF} \leq V_{DDM}$; used for TMADC and FCC; valid for BGA292
		-7 ¹⁾	-	7 ¹⁾	μA	$T_J \leq 150^\circ\text{C}$; $V_{AREF} \leq V_{DDM} + 50\text{ mV}$; used for TMADC and FCC; valid for BGA292
		-4 ¹⁾	-	4 ¹⁾	μA	$T_J \leq T_J (\text{Max})$; $V_{AREF} \leq V_{DDM}$; used for TMADC and FCC (if available); valid for BGA292
		-14 ¹⁾	-	14 ¹⁾	μA	$T_J \leq T_J (\text{Max})$; $V_{AREF} \leq V_{DDM} + 50\text{ mV}$; used for TMADC and FCC (if available); valid for BGA292
		-1 ²⁾	-	1 ²⁾	μA	$T_J \leq 150^\circ\text{C}$; $V_{AREF} \leq V_{DDM}$; used for TMADC and FCC; valid for BGA436
		-3.5 ²⁾	-	3.5 ²⁾	μA	$T_J \leq 150^\circ\text{C}$; $V_{AREF} \leq V_{DDM} + 50\text{ mV}$; used for TMADC and FCC; valid for BGA436
		-2 ²⁾	-	2 ²⁾	μA	$T_J \leq T_J (\text{Max})$; $V_{AREF} \leq V_{DDM}$; used for TMADC and FCC; valid for BGA436
		-7 ²⁾	-	7 ²⁾	μA	$T_J \leq T_J (\text{Max})$; $V_{AREF} \leq V_{DDM} + 50\text{ mV}$; used for TMADC and FCC; valid for BGA436
		-2 ³⁾	-	2 ³⁾	μA	$T_J \leq 150^\circ\text{C}$; $V_{AREF} \leq V_{DDM}$; used for DSADC; valid for BGA436 & BGA292
		-6 ³⁾	-	6 ³⁾	μA	$T_J \leq 150^\circ\text{C}$; $V_{AREF} \leq V_{DDM} + 50\text{ mV}$; used for DSADC; valid for BGA436 & BGA292
		-4 ³⁾	-	4 ³⁾	μA	$T_J \leq T_J (\text{Max})$; $V_{AREF} \leq V_{DDM}$; used for DSADC; valid for BGA436 & BGA292
		-12 ³⁾	-	12 ³⁾	μA	$T_J \leq T_J (\text{Max})$; $V_{AREF} \leq V_{DDM} + 50\text{ mV}$; used for DSADC; valid for BGA436 & BGA292

1) Limit is valid for VAREF2 pin.

2) Limit is valid for VAREF2 and VAREF3 (if ball/pin available) pins each.

3) Limit is valid for VAREF1 pin and used for DSADC.

4.5.6 Driver mode selection for slow and fast pads

Table 70 Driver mode selection for Slow pads

PDx.2	PDx.1	PDx.0	Port functionality	Driver setting
X	X	0	Speed grade 1	medium sharp edge (sm)
X	X	1	Speed grade 2	medium edge (m)

Table 71 Driver mode selection for Fast pads

PDx.2	PDx.1	PDx.0	Port functionality	Driver setting
X	0	0	Speed grade 1	Strong sharp edge (ss)
X	0	1	Speed grade 2	Strong medium edge (sm)
X	1	0	Speed grade 3	medium edge (m)
X	1	1	Speed grade 4	Reserved.
				Note: Do not use this combination!

4.6 High performance LVDS pad characteristic

This LVDS pad type is used for the high speed chip to chip communication interface of the new TC49xN STD. It is composed out of an LVDS pad and a fast pad.

$C_L = 2.5$ pF for all LVDS parameters.

Note: Driver ground potential difference is defined as driver-receiver potential difference, that can result in a voltage shift when comparing the driver output voltage level and the receiver input voltage level of a transmitted signal.

Note: R_T in table 'LVDS - IEEE standard LVDS general purpose Link (GPL)' is as termination resistor of the receiver according to figure 3-5 in IEEE Std 1596.3-1996 and is represented in either by R_{IN} or by $R_T = 100\Omega$ but not both.

Note: Default after start-up = CMOS function

4.6.1 LVDS - IEEE standard LVDS general purpose link (GPL)

Table 72 LVDS - IEEE standard LVDS general purpose link (GPL)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Driver dc characteristics						
Output voltage high	V_{oh} CC	-	-	1475	mV	$R_T = 100\text{ Ohm} \pm 1\%$; LPCRx.VDIFFADJ = 00 and 01
		-	-	1500	mV	$R_T = 100\text{ Ohm} \pm 1\%$; LPCRx.VDIFFADJ = 10 and 11
Output voltage low	V_{ol} CC	925	-	-	mV	$R_T = 100\text{ Ohm} \pm 1\%$; LPCRx.VDIFFADJ = 00 and 01
		900	-	-	mV	$R_T = 100\text{ Ohm} \pm 1\%$; LPCRx.VDIFFADJ = 10 and 11
Output differential voltage	V_{od} CC	380	-	500	mV	$R_T = 100\text{ Ohm} \pm 1\%$; LPCRx.VDIFFADJ = 11; Multi slave operation
		240	-	330	mV	$R_T = 100\text{ Ohm} \pm 1\%$; LPCRx.VDIFFADJ = 00
		280	-	370	mV	$R_T = 100\text{ Ohm} \pm 1\%$; LPCRx.VDIFFADJ = 01
		320	-	410	mV	$R_T = 100\text{ Ohm} \pm 1\%$; LPCRx.VDIFFADJ = 10
Output differential voltage in Sleep Mode ¹⁾	V_{ODSM} CC	-5	-	20	mV	$R_T = 100\text{ Ohm} \pm 20\%$; LPCRx.VDIFFADJ = xx
Output offset (Common mode) voltage	V_{os} CC	1125	-	1275	mV	$R_T = 100\text{ Ohm} \pm 1\%$

(table continues...)

Table 72 (continued) LVDS - IEEE standard LVDS general purpose link (GPL)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output impedance	R_O CC	40	-	140	Ohm	
Delta output impedance	dR_O SR	-	-	10	%	
Change in V_{OD} between 0 and 1	dV_{od} CC	-	-	25	mV	$R_T = 100 \text{ Ohm} \pm 1\%$
Change in V_{OS} between 0 and 1	dV_{os} CC	-	-	25	mV	$R_T = 100 \text{ Ohm} \pm 1\%$

Driver ac characteristics

Duty cycle	t_{duty} CC	45	-	55	%	
Fall time (20% - 80%)	t_{fall20} CC	-	-	0.75 ²⁾	ns	$Z_L = 100 \text{ Ohm} \pm 20\%$ at 2 pF external load
Rise time (20% - 80%)	t_{rise20} CC	-	-	0.75 ³⁾	ns	$Z_L = 100 \text{ Ohm} \pm 20\%$ at 2 pF external load

Receiver dc characteristics

Input voltage range	V_i SR	0	-	1600	mV	Driver ground potential difference < 925 mV; $R_T = 100 \text{ Ohm} \pm 10\%$
		0	-	2000	mV	Driver ground potential difference < 925 mV; $R_T = 100 \text{ Ohm} \pm 20\%$
Input differential threshold	V_{idth} SR	-100	-	100	mV	Driver ground potential difference < 925 mV

Receiver ac characteristics

Pad setup time	t_{SET_LVDS} CC	-	10	13	μs	

- 1) Common Mode voltage of TX is maintained
2) $t_{fall20} = 0.75 \text{ ns} + (C_L - 2)[\text{pF}] * 20 \text{ ps}$. C_L defines the external load.
3) $t_{rise20} = 0.75 \text{ ns} + (C_L - 2)[\text{pF}] * 20 \text{ ps}$. C_L defines the external load.

Related information

[LVDS pad input model](#) on page 477

4.6.2 LVDS pad input model

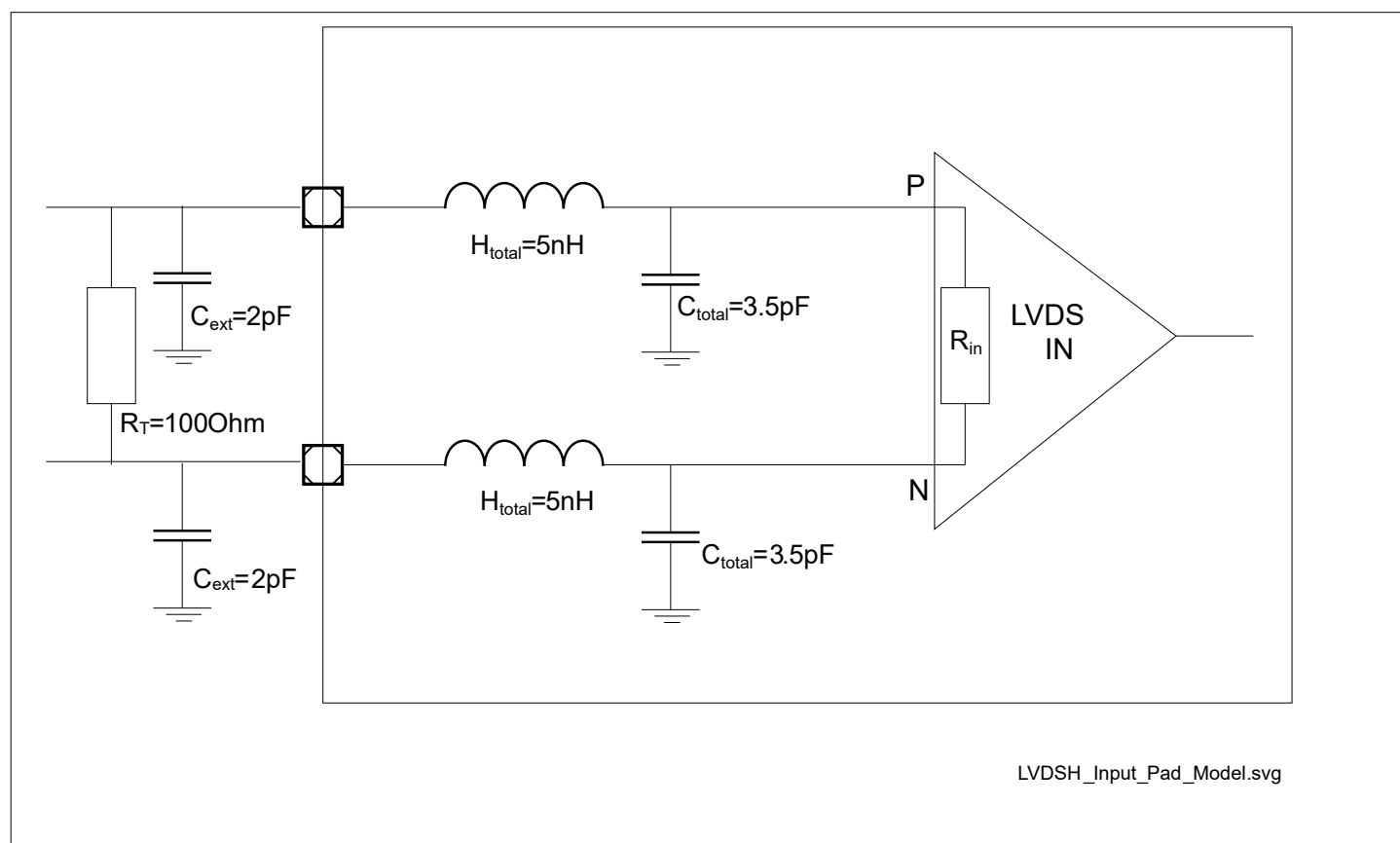


Figure 4 LVDS pad input model

Related information

[LVDS - IEEE standard LVDS general purpose link \(GPL\)](#) on page 475

4.7 TMADC characteristics

The accuracy of the converter results depends on the reference voltage range. The parameters in the table below are valid for a reference voltage range of $(V_{AREF} - V_{AGND}) \geq 4.5 \text{ V}$.

If the reference voltage range is below 4.5 V, for example 3.3 V, the accuracy parameter values increase by a factor of $1.1 / k$, where $k = 3.3 \text{ V} / 4.5 \text{ V}$. If TUE is specified with $\pm 4 \text{ LSB}_{12}$ at 4.5 V the corresponding value at 3.3 V will be: $4 \text{ LSB}_{12} \times (1.1 \times 4.5 \text{ V} / 3.3 \text{ V}) = 6 \text{ LSB}_{12} \rightarrow \pm 6 \text{ LSB}_{12}$.

Note: Noise on supply voltage V_{DDM} influences the conversion. The accuracy (error) parameters are defined for a supply voltage ripple of below 20 mVpp up to 10 MHz (below 5 mVpp above 10 MHz).

Note: Digital functions overlapping analog inputs influence accuracy.

Note: The total unadjusted error (TUE) is defined without noise. The overall deviation depends on TUE and EN_{RMS} (depending on the noise distribution). Example: For a noise distribution of 4 sigma and $EN_{RMS} = 1.0 \text{ LSB}$ the additional peak-peak noise error is $\pm(4 \times 1.0) = 8 \text{ LSB}_{12}$.

4.7.1 TMADC 5V characteristics

Table 73 TMADC 5V characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TMADC internal regulator characteristics						
TMADC IVR output voltage	$V_{DDK \text{ CC}}$	-	2.4	-	V	
Deviation of IVR output voltage V_{DDK}	$dV_{DDK \text{ CC}}$	-2.0	-	2.0	%	Based on device-specific value
TMADC reference voltage characteristics						
Analog reference voltage	$V_{AREF \text{ SR}}$	$V_{DDM} - 0.1$	V_{DDM}	$V_{DDM} + 0.05^{1)}$	V	$2.97 \text{ V} \leq V_{DDM} \leq 5.5 \text{ V}$
Negative reference voltage ²⁾	$V_{AGND \text{ SR}}$	$V_{SSM} - 0.05$	V_{SSM}	$V_{SSM} + 0.05$	V	V_{SSM} and V_{AGND} are connected together
Reference input charge consumption per conversion (from V_{AREF}) ³⁾	$Q_{CONV \text{ CC}}$	-	-	10	pC	
TMADC accuracy						
Total Unadjusted Error ^{4) 5) 6) 7) 8)}	$TUE \text{ CC}$	-4	-	4	LSB	12-bit resolution DC input; $4.5 \text{ V} \leq V_{DDM} \leq 5.5 \text{ V}$
Integral Non-linearity ^{4) 5) 8)}	$EA_{INL \text{ CC}}$	-3	-	3	LSB	$4.5 \text{ V} \leq V_{DDM} \leq 5.5 \text{ V}$
Differential Non-linearity ^{4) 5) 9) 8)}	$EA_{DNL \text{ CC}}$	-1	-	2	LSB	$4.5 \text{ V} \leq V_{DDM} \leq 5.5 \text{ V}$
Gain error ^{4) 5) 8)}	$EA_{GAIN \text{ CC}}$	-4	-	4	LSB	$4.5 \text{ V} \leq V_{DDM} \leq 5.5 \text{ V}$
Offset ^{4) 5) 6) 8)}	$EA_{OFF \text{ CC}}$	-4	-	4	LSB	$4.5 \text{ V} \leq V_{DDM} \leq 5.5 \text{ V}$
RMS Noise ^{4) 5) 6) 10) 11) 7)}	$EN_{RMS \text{ CC}}$	-	0.5	1	LSB	12bit resolution DC input

(table continues...)

Table 73 (continued) **TMADC 5V characteristics**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TMADC input characteristics						
Analog input voltage range	V_{AIN} SR	V_{AGND}	-	V_{AREF}	V	V_{AIN} is limited by the respective pad supply voltage; see pin configuration (buffer type)
Analog input charge consumption ¹²⁾	Q_{AINS} CC	-	-	3.0	pC	
TMADC timing						
Converter reference clock ¹³⁾	f_{ADCI} SR	-	-	80	MHz	$4.5\text{ V} \leq V_{DDM} \leq 5.5\text{ V}$
		-	-	40	MHz	$2.97\text{ V} \leq V_{DDM} < 4.5\text{ V}$
Conversion time (excluding sample and hold time)	t_{CONV} CC	16	-	16	cycles	Measured between two conversion start-points, thus these numbers are valid for pipelined conversions ¹⁴⁾
Sampling time ¹⁵⁾	t_{mstc} SR	50	-	-	ns	Valid for the continous conversion mode; $4.5\text{ V} \leq V_{DDM} \leq 5.5\text{ V}$
		100	-	-	ns	Valid for the continous conversion mode; $2.97\text{ V} \leq V_{DDM} < 4.5\text{ V}$
		100	-	-	ns	Valid for a single conversion; $4.5\text{ V} \leq V_{DDM} \leq 5.5\text{ V}$
		200	-	-	ns	Valid for a single conversion; $2.97\text{ V} \leq V_{DDM} < 4.5\text{ V}$
Sampling time monitor channel	t_{mmstc} SR	1	-	-	μs	
Calibration time	t_{CAL} CC	-	-	3	ms	Valid for power up calibration and recalibration; $4.5\text{ V} \leq V_{DDM} \leq 5.5\text{ V}$
		-	-	6	ms	Valid for power up calibration and recalibration; $2.97\text{ V} \leq V_{DDM} < 4.5\text{ V}$
Hold Time for pending Sample	t_{HOLD} SR	-	-	3	μs	$4.5\text{ V} \leq V_{DDM} \leq 5.5\text{ V}$
		-	-	6	μs	$2.97\text{ V} \leq V_{DDM} < 4.5\text{ V}$
Wakeup time	t_{WUDIS} CC	-	-	8	μs	From module disable state (MODCFG.RUN set from zero to one); $4.5\text{ V} \leq V_{DDM} \leq 5.5\text{ V}$
		-	-	15	μs	From module disable state (MODCFG.RUN set from zero to one); $2.97\text{ V} \leq V_{DDM} < 4.5\text{ V}$

(table continues...)

Table 73 (continued) **TMADC 5V characteristics**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TMADC diagnosis characteristics						
Converter diagnostics voltage accuracy	$dV_{CSD\ CC}$	-1	-	1	%	Referred to V_{DDM}
Resistance of the pull-down test device ¹⁶⁾	$R_{PDD\ CC}$	-	-	0.3	kOhm	Measured at pad input voltage $V_{IN} = V_{DDM} / 2$
Broken wire detection charge current	$I_{BWCHG\ CC}$	5	10	15	μA	
Broken wire detection discharge current	$I_{BWDISCHG\ CC}$	5	10	15	μA	

- 1) For $V_{DDM} = 5.5\text{ V}$ the valid Max. value is 5.5 V
- 2) VAGND shall be directly connected with minimized impedance to the VSSM / PCB GND plane to avoid noise coupling (e.g. with via beside the ball)
- 3) Parameter is valid for the typical value of $V_{AREF}-V_{AGND}$. If a reduced $V_{AREF}-V_{AGND}$ voltage is used this parameter will decrease linearly.
- 4) This parameter is valid for $V_{AREF}-V_{AGND}$ equal or higher than the typical value * 0.9. If a reduced $V_{AREF}-V_{AGND}$ voltage is used this parameter can increase. If $V_{AREF}-V_{AGND}$ is reduced with the factor k (k is the quotient built out of the reduced reference voltage and the 4.5 V), the parameter will increase with 1.1/k. e.g., $k = 3.3\text{ V}/4.5\text{ V} = 0.73 \rightarrow 1.1/k = 1.5 \rightarrow 1.5 * TUE: 6\text{ LSB at } 3.3\text{ V reference}$
- 5) This parameter is only guaranteed with a maximum supply voltage ripple on VDDM / VSSM of 20 mVpp in a frequency band from 1 kHz to 10 MHz. Supply voltage ripples above 10 MHz must be smaller than 5 mV. This must be guaranteed by high quality power supply sources and proper blocking capacitors
- 6) This parameter is valid for analog inputs within Pads not sharing digital functions. Parameter for analog inputs sharing digital functions (pad type Slow and Fast) will increase by 3 LSB
- 7) Resulting worst case combined error is arithmetic combination of TUE and user-defined distribution of EN_{RMS}
- 8) Start-up calibration is a prerequisite to achieve TMADC accuracy specification. It needs to be repeated when channel to SAR-core mapping is changed. Refer to user manual TMADC chapter "Module start-up calibration" for details.
- 9) Monotonic characteristic, no missing codes (after calibration)
- 10) Only valid if VAGND is directly connected with minimized impedance to the VSSM / PCB GND plane to avoid noise coupling (e.g. with via beside the ball)
- 11) The value is derived from a 1 sigma distribution
- 12) The specified value does not include the pin leakage current I_{OZ} . I_{OZ} has to be added to get the total current value.
- 13) This is the operating frequency of TMADC selectable by the bit 'TMADC supply level' (SUPPLEV.TMADCSUP)
- 14) f_{ADCI} clock cycles
- 15) Sampling time is a configurable parameter (see details in the user manual)
- 16) Enabling of the pull down test device is only allowed in PWM operation with a duty cycle of $\leq 50\%$ and a frequency of 1 kHz

Related information

TMADC input structure figure on page 481

4.7.2 TMADC input structure figure

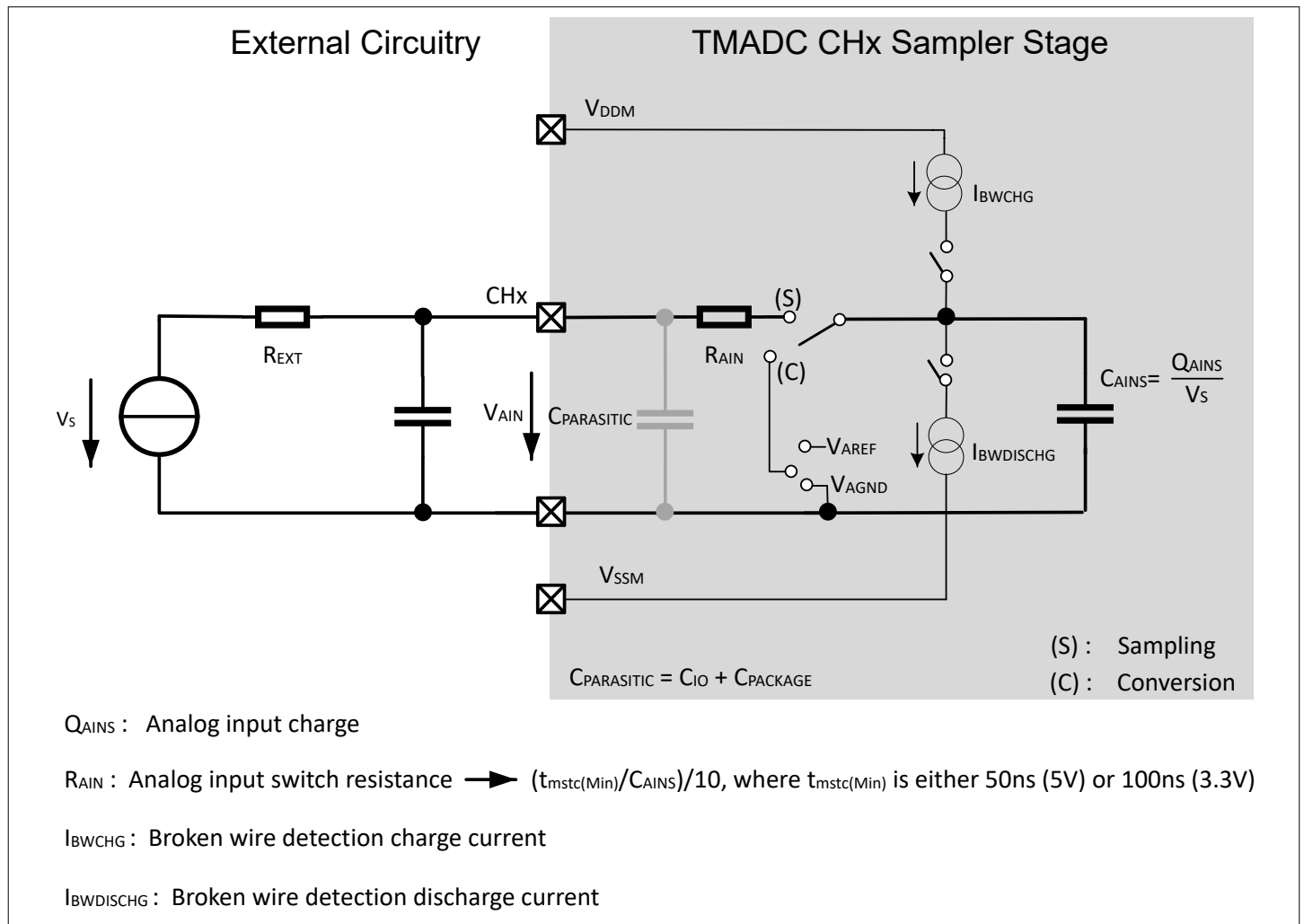


Figure 5 Equivalent Circuitry for Analog Inputs

Related information

[TMADC 5V characteristics](#) on page 478

4.8 DSADC characteristics

The DSADC parameters describe the product properties and do not include external circuitry.

They are only valid for a voltage range $4.5\text{ V} \leq V_{DDM} \leq 5.5\text{ V}$ and junction temperatures $T_J \leq 150\text{ °C}$ if not defined explicitly.

The signal-noise ratio (SNR) is specified for differential inputs. For single ended operation and for quasi-differential mode (i.e. using VCM) the resulting signal-noise ratio is reduced by 6 dB.

4.8.1 DSADC 5V characteristics

Table 74 DSADC 5V characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
DSADC reference voltage requirements						
Positive reference voltage	$V_{AREF\ SR}$	$V_{DDM} - 0.1$	V_{DDM}	$V_{DDM} + 0.05^{1)}$	V	
Reference ground voltage ²⁾	$V_{AGND\ SR}$	$V_{SSM} - 0.05$	V_{SSM}	$V_{SSM} + 0.05$	V	V_{SSM} and V_{AGND} are connected together
DSADC accuracy						
Common mode voltage accuracy ³⁾	$dV_{CM\ CC}$	-2	-	2	%	Common mode voltage is derived from V_{DDM} . Accuracy mismatch between V_{AREF} and V_{DDM} not included.
Gain error degradation ^{4) 5)}	$ED_{GAIN\ CC}$	-0.2 ⁶⁾	$\pm 0.1^{6)}$	0.2 ⁶⁾	%	$T_J \leq 150^{\circ}\text{C}$; Target, calibrated, V_{AREF} constant after calibration; $f_{MOD} = 40\text{ MHz}$
		-	$\pm 0.25^{6)}$	-	%	$150^{\circ}\text{C} < T_J \leq T_J (\text{Max})$; V_{AREF} constant after calibration; $f_{MOD} = 40\text{ MHz}$
		-1	-	1	%	Calibrated once; $f_{MOD} = 40\text{ MHz}$
		-5	-	5	%	Uncalibrated; $f_{MOD} = 40\text{ MHz}$
DC offset error	$ED_{OFF\ CC}$	-5 ⁶⁾	-	5 ⁶⁾	mV	Calibrated; $f_{MOD} = 40\text{ MHz}$
		-25	-	25	mV	Calibrated once; $f_{MOD} = 40\text{ MHz}$
		-50	-	50	mV	Uncalibrated; $f_{MOD} = 40\text{ MHz}$
Signal-Noise Ratio for differential input signals	$SNR\ CC$	86	-	-	dB	$T_J \leq 150^{\circ}\text{C}$; $f_{PB} = 30\text{ kHz}$; $f_{MOD} = 40\text{ MHz}$ ⁷⁾
		83	-	-	dB	$T_J \leq 150^{\circ}\text{C}$; $f_{PB} = 50\text{ kHz}$; $f_{MOD} = 40\text{ MHz}$ ⁷⁾
		79	-	-	dB	$T_J \leq 150^{\circ}\text{C}$; $f_{PB} = 100\text{ kHz}$; $f_{MOD} = 40\text{ MHz}$ ⁷⁾
Signal to Noise Ratio single ended mode	$SNR_{se\ CC}$	-	SNR-6dB	-	dB	
Signal-Noise Ratio degradation	$DSNR\ CC$	-	-	3	dB	$150^{\circ}\text{C} < T_J \leq T_J (\text{Max})$; Resulting Signal-Noise Ratio value is SNR - DSNR
Spurious-free dynamic range	$SFDR\ CC$	60	-	-	dB	$f_{MOD} = 40\text{ MHz}$
DSADC input characteristics						
Analog input voltage range	$V_{DSIN\ SR}$	V_{SSM}	-	V_{AREF}	V	
(table continues...)						

Table 74 (continued) **DSADC 5V characteristics**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Average input current ^{8) 9)}	$I_{AVG\ CC}$	-1	±0.1	1	µA	Valid for $f_{MOD} = 40\text{ MHz}$; $T_J \leq 150^\circ\text{C}$ 7)
Analog input leakage current ⁹⁾	$I_{A\_leak\ CC}$	-200	-	200	nA	$T_J \leq 150^\circ\text{C}$; for one modulator 7)
Common mode voltage bias resistance	$R_{BIAS\ CC}$	100	130	170	kOhm	On-chip variation $\leq \pm 2.5\%$.
Input signal bandwidth	$BW\ SR$	-	-	100	kHz	
Common Mode Rejection in differential mode	$CMR_{DIFF\ CC}$	65	-	-	dB	

DSADC timing

On-chip modulator clock frequency	$f_{MOD\ SR}$	10	-	40	MHz	
DSM start-up time	$t_{START\ CC}$	-	-	8	µs	Time from enable till valid output bitstream; $4.5\text{ V} \leq V_{DDM} \leq 5.5\text{ V}$
Output sampling rate	$f_D\ CC$	9.76	-	1250	kHz	

- 1) For $V_{DDM} = 5.5\text{ V}$ the valid Max. value is 5.5 V
- 2) VAGND shall be directly connected with minimized impedance to the VSSM / PCB GND plane to avoid noise coupling (e.g. with via beside the ball).
- 3) On pins with overlaid GPIO function limits are extended by 1% (25mV) and on pins with overlaid PDD function limits are extended by 1.5% due to leakage current for $T_J > 150^\circ\text{C}$
- 4) This parameter is valid within the defined range of f_{MOD} .
- 5) Gain mismatch error between the different DSADC channels is within $\pm 0.5\%$.
- 6) Recalibration needed in case of a temperature change $\Delta T_J > 20^\circ\text{C}$.
- 7) In case T_J (Max) operating condition value is lower than 150°C , operating condition value is valid instead.
- 8) For detailed information, refer to User Manual Chapter.
- 9) The specified value does not include the pin leakage current I_{OZ} . I_{OZ} has to be added to get the total current value.

4.9 FCC characteristics

The parameters in the table that follow are valid for a reference voltage range of $(V_{AREF} - V_{AGND}) \geq 4.5\text{ V}$.

If the reference voltage range is below 4.5 V, for example 3.3 V, the accuracy parameter values increase by a factor of $1.1 / k$, where $k = 3.3\text{ V} / 4.5\text{ V}$. For example, if EA_{GAIN} and EA_{OFF} is specified with $\pm 3\text{ LSB}_{10}$ at 4.5 V the corresponding value at 3.3 V will be: $3\text{ LSB}_{10} \times (1.1 \times 4.5\text{ V} / 3.3\text{ V}) = 4.5\text{ LSB}_{10} \rightarrow \pm 4.5\text{ LSB}_{10}$.

Note: Noise on supply voltage V_{DDM} influences the conversion. The accuracy (error) parameters are defined for a supply voltage ripple of below 20 mVpp up to 10 MHz (below 5 mVpp above 10 MHz).

Note: Digital functions overlapping analog inputs influence accuracy. In the table below accuracy is given for pins marked as "AN" in the ballout.

4.9.1 FCC characteristics

Table 75 FCC characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
FCC reference voltage requirements						
Positive Reference Voltage	$V_{AREF} SR$	$V_{DDM} - 0.1$	V_{DDM}	$V_{DDM} + 0.05^{1)}$	V	
Negative Reference Voltage	$V_{AGND} SR$	$V_{SSM} - 0.05$	V_{SSM}	$V_{SSM} + 0.05$	V	
FCC accuracy						
Resolution	$RES CC$	-	10 bit	-		Physical implementation
Gain error	$EA_{GAIN} CC$	-3 ^{2) 3)}	-	3 ^{2) 3)}	LSB	
Offset	$EA_{OFF} CC$	-3 ^{2) 3)}	-	3 ^{2) 3)}	LSB	
RMS Noise	$EN_{RMS} CC$	-	-	1 ^{2) 3)}	LSB	
FCC input characteristics						
Analog Input Voltage	$V_A SR$	V_{AGND}	-	V_{AREF}	V	Includes dynamic changes during single monitoring window
Input charge consumption ⁴⁾	$Q_{AIN} CC$	-	-	2.5	pC	Consumed per init phase
FCC timing						
Clock Frequency	$f_{ADC} SR$	-	160	-	MHz	For product only $f_{(Typ)}$ is valid
Comparison Delay	$t_D CC$	-	1	4	cycles	
Monitoring Time	$t_{MON} CC$	-	-	10 ⁵⁾	μs	
Initialization time	$t_{INIT} CC$	-	17	18	cycles	4.5 V ≤ V_{DDM} ≤ 5.5 V
		-	21	24	cycles	2.97 V ≤ V_{DDM} ≤ 4.5 V
Ramp initialization time	$t_{RINIT} CC$	-	5	6	cycles	4.5 V ≤ V_{DDM} ≤ 5.5 V
		-	9	12	cycles	2.97 V ≤ V_{DDM} ≤ 4.5 V
Wakeup time	$t_{WUDIS} CC$	-	85	86	cycles	4.5 V ≤ V_{DDM} ≤ 5.5 V; from module disable state (MODEN.RUN set from zero to one and CLKEN_FCC.FCCEN is one)
		-	93	96	cycles	2.97 V ≤ V_{DDM} ≤ 4.5 V; from module disable state (MODEN.RUN set from zero to one and CLKEN_FCC.FCCEN is one)

1) For $V_{DDM} = 5.5 V$ the Max value is 5.5 V

2) This parameter is valid for $V_{AREF} - V_{AGND}$ equal or higher than the typical value * 0.9. If a reduced $V_{AREF} - V_{AGND}$ voltage is used this parameter can increase. If $V_{AREF} - V_{AGND}$ is reduced with the factor k (k is the quotient build out of the reduced reference voltage and the 4.5 V), the parameter will increase with $1.1/k$; for example $k = 3.3 V / 4.5 V = 0.73 \rightarrow 1.1/0.73 = 1.5 \rightarrow 1.5 * \text{Offset} = 4.5 \text{ LSB at } 3.3 V \text{ Reference}$

3) If max monitoring time is violated, parameter limits have to be multiplied with the factor $C_1 = -2+3t/t_{MON}$

4) The specified value does not include the pin leakage current I_{OZ} . I_{OZ} has to be added to get the total current value

5) Module will loose charge and degrade in performance if max time is violated

4.10 High Resolution PWM characteristics

4.10.1 HRPWM characteristics

Table 76 HRPWM characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output resolution mean ^{1) 2)}	RES_{CC}	152.25	156	160.25	ps	Measurement based on output frequency variation
Peak to Peak Variation of Output Resolution	$RES_{pp\ CC}$	-1000	-	1000	ps	SysPLL FM modulation off; driver = strong, edge = sharp; calculated to 3σ variation ³⁾

- 1) Parameter values are valid for PWM frequencies ≤ 500 kHz
2) Parameter values are valid for $10\% \leq$ PWM Duty Cycle $\leq 90\%$
3) RMS variation of Output Resolution (1σ) can be calculated by $RES_{pp}/6$

4.11 External clock sources

OSC_XTAL is used to provide an accurate clock source for the device. It enables the connection of an external 20 MHz to 50 MHz crystals outside of the device. Ceramic resonators are also supported.

The purpose of the RTC 32 kHz oscillator is to offer a precise and power saving clock option for the device in its lower power modes like Sleep and Standby.

Note: *It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.*

4.11.1 OSC_XTAL characteristics

Table 77 OSC_XTAL characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Oscillator frequency ¹⁾	f_{OSC} SR	20	-	50	MHz	External clock mode selected, if shaper is not bypassed
		20	-	50	MHz	External Crystal Mode selected
Oscillator start-up time	t_{OSCS} CC	-	-	3 ²⁾	ms	Valid for above specified f_{OSC} range and 8 pF load capacitance
Input voltage at XTAL1	V_{IX} SR	-0.45	-	2.6	V	External crystal mode
		-0.5	-	$V_{DDEXTOSC}$	V	External clock mode, if shaper is not bypassed
Input high voltage at XTAL1	V_{IHBX} SR	3.15	-	$V_{DDEXTOSC}$	V	External clock mode, if shaper is not bypassed; $V_{DDEXTOSC} = 5$ V
		2.08	-	$V_{DDEXTOSC}$	V	External clock mode, if shaper is not bypassed; $V_{DDEXTOSC} = 3.3$ V
Input low voltage at XTAL1	V_{ILBX} SR	-0.5	-	0.5	V	
Input amplitude (peak to peak) at XTAL1	V_{PPX} SR	1.0	-	3.0	V	External crystal mode; valid for $20 \text{ MHz} \leq f_{OSC} \leq 50 \text{ MHz}$
		2.5	-	$V_{DDEXTOSC}$	V	External clock mode, if shaper is not bypassed; valid for $20 \text{ MHz} \leq f_{OSC} \leq 50 \text{ MHz}$
Input current at XTAL1	I_{IX1} CC	-70	-	70	μA	DC input voltage sweep from $0V < V_{IN} < V_{DDEXTOSC}$; $T_J = T_J$ (Max)
Duty cycle at XTAL1	DC_{X1} SR	40	-	60	%	External clock mode, if shaper is not bypassed; $V_{XTAL1} = 0.5 * V_{PPX}$
Absolute RMS jitter at XTAL1	J_{ABSX1} SR	-	-	28	ps	External clock mode, if shaper is not bypassed; 10 KHz to $f_{OSC} / 2$

(table continues...)

Table 77 (continued) **OSC_XTAL characteristics**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Slew rate at XTAL1	SR_{XTAL1} <i>SR</i>	0.3	-	-	V/ns	External clock mode, if shaper is not bypassed; Maximum 30% difference between rising and falling slew rate
Internal load capacitor	C_{L0} <i>CC</i>	1.0	1.2	1.4	pF	Enabled via bit OSCCON.CAP0EN
Internal load capacitor	C_{L1} <i>CC</i>	2.1	2.3	2.5	pF	Enabled via bit OSCCON.CAP1EN
Internal load capacitor	C_{L2} <i>CC</i>	5.4	5.9	6.4	pF	Enabled via bit OSCCON.CAP2EN
Internal load capacitor	C_{L3} <i>CC</i>	8.1	8.7	9.3	pF	Enabled via bit OSCCON.CAP3EN
Internal load stray capacitance between XTAL1 and XTAL2	C_{XINTS} <i>CC</i>	1.15	1.20	1.25	pF	
Internal load stray capacitance between XTAL1 and ground	C_{XTAL1} <i>CC</i>	4.7	5.6	6.6	pF	

1) SGMII protocol operation via HSPHY is only possible with 25MHz or 40 MHz

2) This value depends on the frequency of the used external crystal. For faster crystal frequencies this value decreases

Related information

[RTC 32 kHz oscillator characteristics](#) on page 487

4.11.2 RTC 32 kHz oscillator characteristics

Table 78 **RTC 32 kHz oscillator characteristics**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Operating input frequency of external crystal	f_{OSC} <i>CC</i>	-	32.768	-	kHz	The range depends on external crystal accuracy
Start-up time	T_{SU} <i>CC</i>	-	-	5	s	
Input high voltage at XTAL3	V_{IHBX} <i>CC</i>	-	-	$V_{DDEVRSB} + 0.5$	V	
Input low voltage at XTAL3	V_{ILBX} <i>CC</i>	-0.5	-	-	V	
Oscillation amplitude at XTAL PADIN	V_{PP} <i>CC</i>	0.3	0.5	$V_{DDEVRSB}$	V	
Input hysteresis for shaper	V_{HYS} <i>CC</i>	-	50	-	mV	RTC_CON0.HYSEN = 1
Oscillator bias current	I_{bias} <i>CC</i>	0.2	0.6	0.8	μA	Lowest gain setting: RTC_CON0.GAINSEL = 00
		0.75	1.3	1.7	μA	Highest gain setting: RTC_CON0.GAINSEL = 11

(table continues...)

Table 78 (continued) RTC 32 kHz oscillator characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Total current consumption of RTC	$I_{\text{RTC CC}}$	-	3	6	μA	

Related information

[OSC_XTAL characteristics](#) on page 486

4.12 Internal clock sources

The TC49xN STD provides two fully integrated clock options:

- Back-up clock
- Standby clock

The 100 MHz clock source is a precise on-chip clock. After start-up, the 100 MHz clock source has a lower accuracy (see f_{BACKUT}) and the clock source is later trimmed by the start-up software (see f_{BACKT} parameter).

The Standby clock source is used during standby mode. Its accuracy is specified by the f_{SB} and f_{SBT} parameters. This clock source is trimmed after start-up.

4.12.1 Back-up oscillator characteristics

Table 79 Back-up oscillator characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Back-up clock frequency before trimming	$f_{\text{BACKUT CC}}$	70	100	130	MHz	$V_{\text{DDEXT}}, V_{\text{DDEVRSB}} \geq 2.97 \text{ V}$
Back-up clock frequency after trimming	$f_{\text{BACKT CC}}$	98	100	102	MHz	$V_{\text{DDEXT}}, V_{\text{DDEVRSB}} \geq 2.97 \text{ V}$
Back-up clock fine trim LSB	$f_{\text{BACKLSBFT CC}}$	18	-	40	kHz	

Related information

[Standby oscillator characteristics](#) on page 489

4.12.2 Standby oscillator characteristics

Table 80 Standby oscillator characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Standby clock before trimming	$f_{\text{SB CC}}$	30	70	110	kHz	$V_{\text{DDEXT}}, V_{\text{DDEVRSB}} \geq 2.97 \text{ V}$
Standby clock after trimming	$f_{\text{SBT CC}}$	62	70	75	kHz	$V_{\text{DDEXT}}, V_{\text{DDEVRSB}} \geq 2.97 \text{ V}$
Standby clock fine trim LSB	$f_{\text{SBLSBFT CC}}$	1.82	2.03	2.24	kHz	LPOSCGAIN=0

Related information

[Back-up oscillator characteristics](#) on page 489

4.13 System Phase Locked Loop (SYS_PLL) characteristics

The following characteristics are valid for the System Phase Locked Loop (SYS_PLL). In order to achieve the specified performance of the module following constraints need to be considered:

Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed $C_L = 20 \text{ pF}$ with the maximum driver and sharp edge.

Note: The maximum peak-to-peak noise on the power supply voltage, is limited to a peak-to-peak voltage of $V_{PP} = 100 \text{ mV}$ for noise frequencies below 300 KHz and $V_{PP} = 40 \text{ mV}$ for noise frequencies above 300 KHz. These conditions can be achieved by appropriate blocking of the supply voltage as near as possible to the supply pins and using PCB supply and ground planes.

4.13.1 System PLL characteristics

Table 81 System PLL characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
DCO Input frequency range	$f_{REF} CC$	20	-	50	MHz	
Modulation Amplitude	$MA CC$	0	-	2	%	
Peak Period jitter ¹⁾	$DP CC$	-150	-	150	ps	Without modulation (PLL output frequency); valid for $f_{REF} = 20 \text{ MHz}$ and $f_{DCO} = 800 \text{ MHz}$; peak is equal to 5 sigma RMS jitter at DCO output
Peak accumulated jitter	$D_{PP} CC$	-5	-	5	ns	Without modulation (PLL output frequency); valid for $f_{REF} = 20 \text{ MHz}$ and $f_{DCO} = 800 \text{ MHz}$; measured over 100 μs (over at least 6k samples)
Total long term jitter	$J_{TOT} CC$	-	-	10	ns	Including modulation (PLL output frequency); MA 2%; valid for $f_{REF} = 20 \text{ MHz}$ and $f_{DCO} = 800 \text{ MHz}$; measured over at least 1000 output clock observances
DCO frequency range	$f_{DCO} CC$	400	-	1000	MHz	
PLL lock-in time	$t_L CC$	4	-	100	μs	

1) Scaling division on the measurement to be applied: $\sqrt{f_{DCO} / f_{Acquired}}$, at maximum 16

4.14 Peripheral Phase Locked Loop (PER_PLL) characteristics

The following characteristics are valid for the Peripheral Phase Locked Loop (PER_PLL). In order to achieve the specified performance of the module following constraints need to be considered:

Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed $C_L = 20 \text{ pF}$ with the maximum driver and sharp edge.

Note: The maximum peak-to-peak noise on the power supply voltage, is limited to a peak-to-peak voltage of $V_{PP} = 100 \text{ mV}$ for noise frequencies below 300 KHz and $V_{PP} = 40 \text{ mV}$ for noise frequencies above 300 KHz. These conditions can be achieved by appropriate blocking of the supply voltage as near as possible to the supply pins and using PCB supply and ground planes.

4.14.1 Peripheral PLL characteristics

Table 82 Peripheral PLL characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
DCO input frequency range	$f_{REF} CC$	20	-	50	MHz	
Peak Period jitter ¹⁾	$DP CC$	-150	-	150	ps	Valid for $f_{REF} = 20 \text{ MHz}$ and $f_{DCO} = 800 \text{ MHz}$; peak is equal to 5 sigma RMS valid at DCO output
Peak accumulated jitter	$D_{PPI} CC$	-700	-	700	ps	Valid for $f_{REF} = 20 \text{ MHz}$ and $f_{DCO} = 800 \text{ MHz}$; measured over 100 μs (over at least 6k samples)
Peak accumulated jitter at SYSCLK pin	$D_{PP} CC$	-1000	-	1000	ps	Valid for $f_{REF} = 20 \text{ MHz}$ and $f_{DCO} = 800 \text{ MHz}$; measured over 100 μs (over at least 6k samples)
RMS accumulated jitter	$D_{RMS} CC$	-150	-	150	ps	Valid for $f_{REF} = 20 \text{ MHz}$ and $f_{DCO} = 800 \text{ MHz}$; measured over 100 μs (over at least 6k samples)
Absolute RMS jitter (PLL out)	$J_{ABS20} CC$	-92	-	92	ps	Valid for $f_{REF} = 20 \text{ MHz}$; $f_{DCO} = 800 \text{ MHz}$; integration range from 10 kHz to about f_{DCO} divided by 2
DCO frequency range	$f_{DCO} CC$	400	-	800	MHz	
PLL lock-in time	$t_L CC$	4	-	100	μs	

1) Scaling division on the measurement to be applied: $\sqrt{f_{DCO} / f_{Acquired}}$, at maximum 16

4.15 Power supply topology and power supply characteristics

4.15.1 Power supply topology

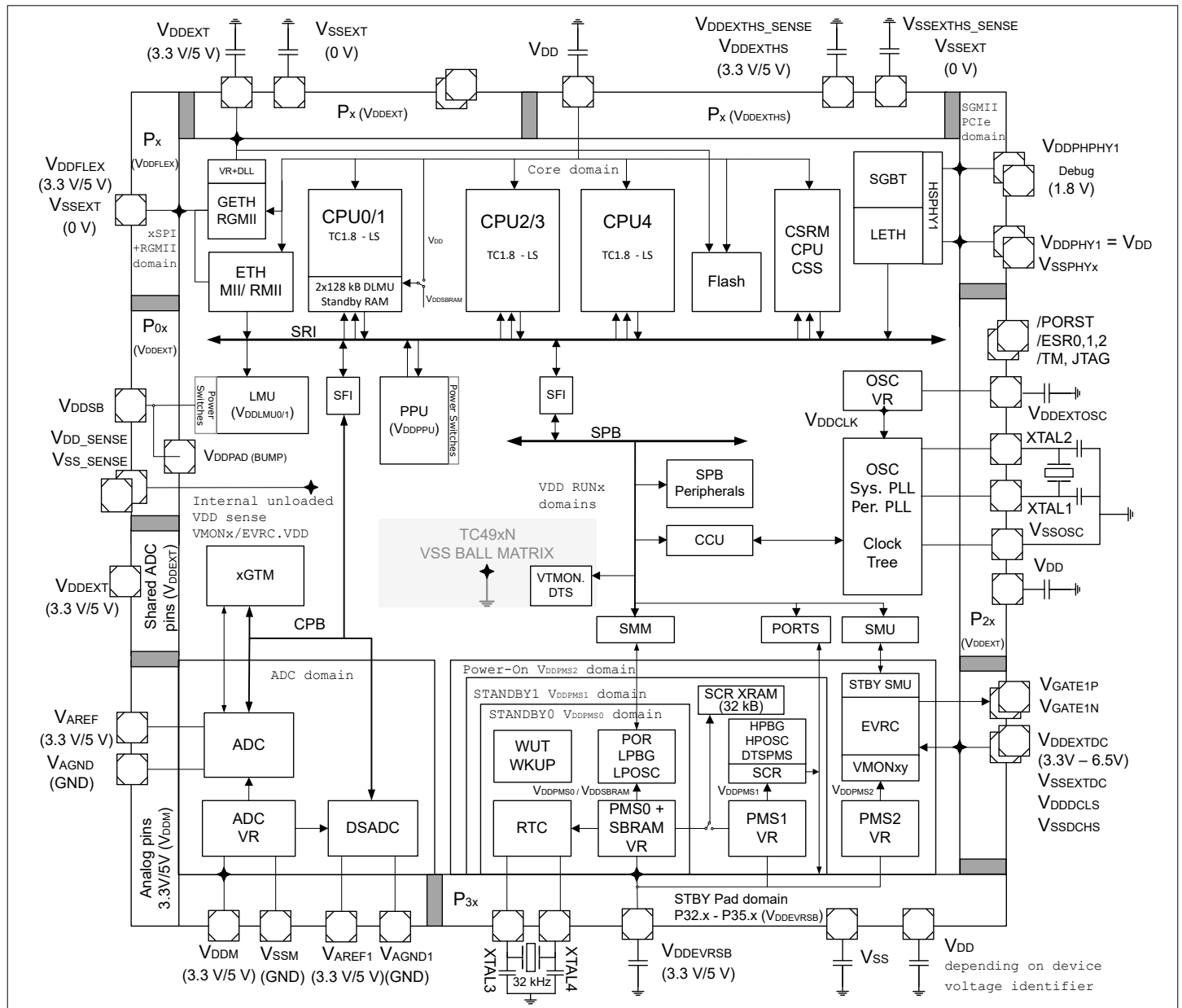


Figure 6 Power Supply Topology

Related information

[Supply ramp-up and ramp-down behavior](#) on page 493

[LVD reset characteristics](#) on page 494

[Line Transients](#) on page 495

4.15.2 Supply ramp-up and ramp-down behavior

This section presents the behavior of the supply rails during ramp-up, ramp-down, and dynamic operational phases.

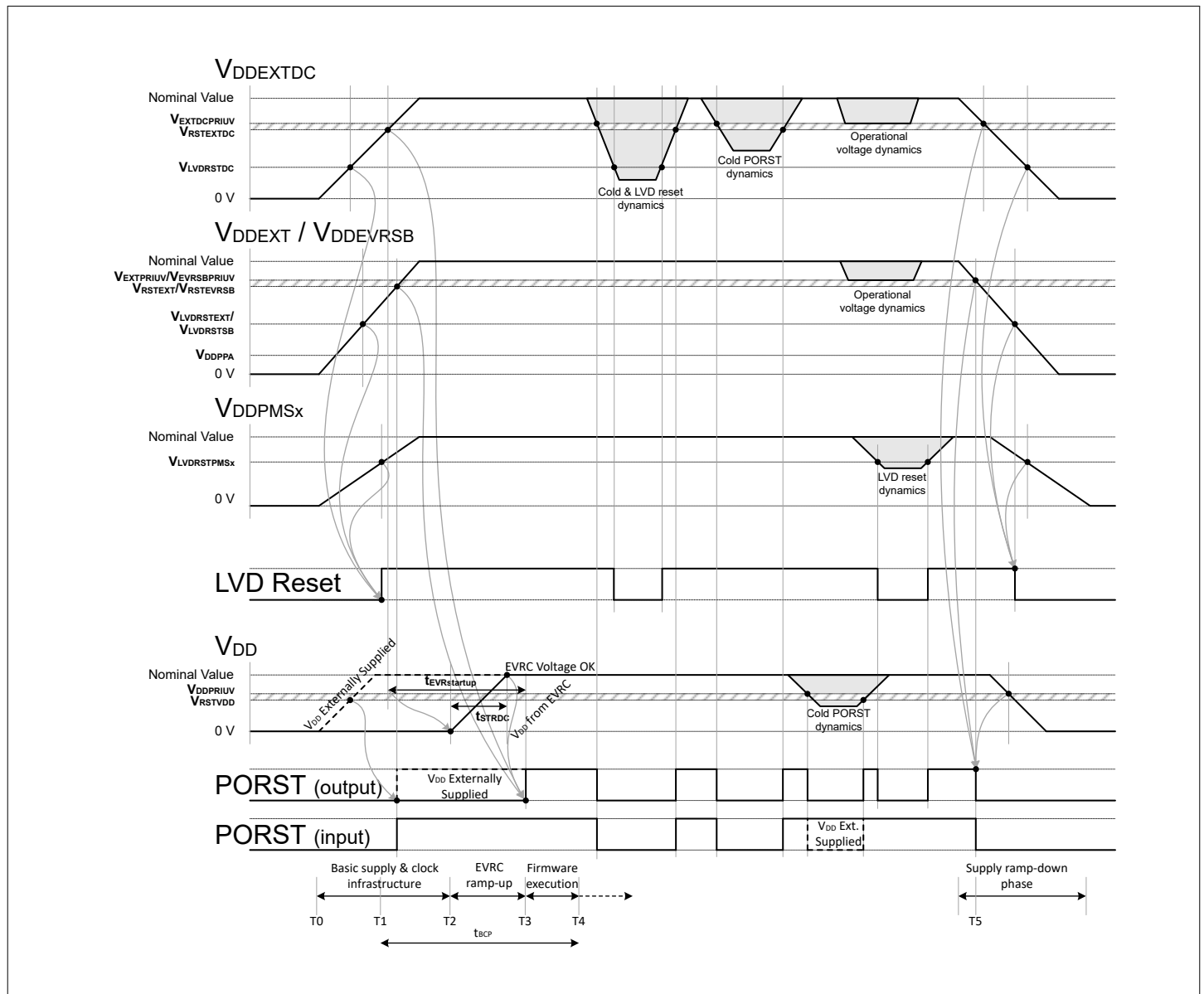


Figure 7 Supply ramp-up and ramp-down behavior

- The start-up slew rates for the supply rails shall comply to the respective data sheet parameters dV_{xx}/dt . The slope is defined as the maximum tangential slope between 0% to 100% voltage level. The actual waveform may not represent the specification
- In case of an external regulator for the V_{DD} supply rail, it is ensured that the load jumps to the external regulator (from the V_{DD} rail) are limited during the start-up phase to the $dI_{DD\text{DYN\_STRT}}$ data sheet parameter
- PORST is active or asserted when either PORST (input) or PORST (output) is active or asserted
- PORST (input) active means that the reset is held active by external agents by pulling the PORST pin low. It is recommended to keep the PORST (input) asserted until the external supply is above the respective primary reset threshold (V_{RSTxx} parameter in the datasheet)
- PORST (output) active means that the microcontroller asserts the reset internally and drives the PORST pin low, propagating the reset to external devices. The PORST (output) is asserted by the MCU when at least one supply domain violates its primary under-voltage reset threshold. The PORST (output) is de-asserted by the microcontroller when all relevant supplies (with $V_{MONP\_VxxRST.RESETOFF} = 0$) are above their primary reset thresholds and the basic supply and clock infrastructure is available

The power sequence as shown in the figure above is enumerated as follows:

- T0 is the begin of the supply ramp-up from the external regulator
- T1 is the point in time when LVD reset is released. The LVD resets are released when $V_{DDEXTDC}$, V_{DDEXT} , $V_{DDEVRSB}$, and V_{DDPMSx} are above their LVD reset levels (denoted as $V_{LVDRSTxx}$)
- T0 up to T2 refers to the period in time when basic supply and clock infrastructure components are made available as the external supply ramps up. The band-gap and internal clock sources are started. The supply mode is evaluated based on the *HWCFG* pins. These events are initiated after LVD reset release at T1
- T2 refers to the point in time where a soft start of the EVRC is initiated. PORST (input) does not have any effect on the EVRC output and the regulator continues to generate the respective voltage though PORST is asserted and the device is in reset state. The generated voltage follows a soft ramp-up over the t_{STRDC} time (data sheet parameter) to avoid overshoots
- T3 refers to the point in time when all supplies are above their primary reset thresholds, denoted as V_{RSTxx} . There are two parameters denoting the primary reset threshold, respectively V_{RSTxx} (which is the untrimmed threshold) and $V_{xxPRIUV}$ (which is the trimmed threshold). Their values are located closely to each other and are indicated therefore as a thin hashed region in the figure above. During the supply ramp-up phase, the untrimmed threshold V_{RSTxx} is used for the first PORST release. After the firmware execution phase, the trimmed threshold $V_{xxPRIUV}$ is used for the PORST assertions. Subsequent reset releases occur at the untrimmed threshold V_{RSTxx} , since the primary voltage monitors reset thresholds *VMONP_VxxRST.RESETTRIM* are being reset to the V_{RSTxx} values also after a cold PORST (see the "Cold PORST" reset values of the *VMONP_VxxRST* registers)
- The supply start-up phase is completed when the regulator outputs are stable and operational and all voltages have ramped up. Consequently cold PORST reset is released when all voltages on the primary monitors are above their minimum operational limits ($V_{RSTxx}/V_{xxPRIUV}$)
- T4 refers to the point in time when the firmware execution is completed and the user code execution starts, with CPU0 running at the f_{BACKT} clock frequency. The time between T1 and T4 is documented as t_{BCP} (cold power on reset boot time, datasheet parameter)
- T5 refers to the point in time during the supply ramp-down phase when at least one of the supplies (either externally provided or internally generated) drops below its respective primary under-voltage reset threshold $V_{xxPRIUV}$

Related information

[Power supply topology](#) on page 492

[LVD reset characteristics](#) on page 494

[Line Transients](#) on page 495

4.15.3 LVD reset characteristics

Table 83 LVD reset characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
V_{DDEXT} LVDANA reset undervoltage detector comparator threshold	$V_{LVDRSTEXT}$ CC	2.5	-	2.77	V	Supply ramp-down and undershoots
		2.53	-	2.8	V	Supply ramp-up
$V_{DDEVRSB}$ LVDANA reset undervoltage detector comparator threshold	$V_{LVDRSTSB}$ CC	2.26	-	2.5	V	Supply ramp-down and undershoots
		2.21	-	2.53	V	Supply ramp-up
$V_{DDEXTDC}$ LVDANA reset undervoltage detector comparator threshold	$V_{LVDRSTDC}$ CC	2.5	-	2.77	V	Supply ramp-down and undershoots
		2.53	-	2.8	V	Supply ramp-up

(table continues...)

Table 83 (continued) LVD reset characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
V_{DDPMS0} LVDPMs _x undervoltage detector comparator threshold	$V_{LVD RSTPMS0 CC}$	0.75	0.785	0.82	V	Supply ramp-down and undershoots
		0.75	0.785	0.82	V	Supply ramp-up
V_{DDPMS1} , V_{DDPMS2} and $V_{DD SBRAM}$ LVDPMs _x undervoltage detector comparator threshold	$V_{LVD RSTPMS1 CC}$	0.75	0.785	0.82	V	Supply ramp-down and undershoots
		0.75	0.785	0.82	V	Supply ramp-up
L_{VDx} reset assertion response time on under voltage for V_{DDEXT} , $V_{DDEVRSB}$, $V_{DDEXTDC}$ and V_{DDPMSx} detectors	$t_{LVD CC}$	-	1	3	μs	LVD assertion
Input high voltage level for HWCFG pins on LVDANA reset release	$V_{IH\_HWCFG SR}$	$0.7 \cdot V_{DDIO}^{1)}$	-	-	V	$V_{DDIO} = V_{LVD RSTEXT}^{1)}$
Input low voltage level for HWCFG pins on LVDANA reset release	$V_{IL\_HWCFG SR}$	-	-	$0.44 \cdot V_{DDIO}^{1)}$	V	$V_{DDIO} = V_{LVD RSTEXT}^{1)}$

1) V_{DDIO} corresponding to the supply voltage of the IO supply domains V_{DDEXT} or $V_{DDEXT HS}$

Related information

[Power supply topology](#) on page 492

[Supply ramp-up and ramp-down behavior](#) on page 493

[Line Transients](#) on page 495

4.15.4 Line Transients

Table 84 Line Transients

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
External V_{DDEXT} / $V_{DDEXT HS}$ and $V_{DDEVRSB}$ supply ramp-up and ramp-down slope ^{1) 2)}	$dV_{DDEXT}/dt SR$	8.3E-06	1	100	V/ms	
External V_{DDM} supply ramp-up and ramp-down slope ^{1) 2)}	$dV_{DDM}/dt SR$	8.3E-06	1	100	V/ms	
External V_{DD} supply ramp-up and ramp-down slope ^{1) 2)}	$dV_{DD}/dt SR$	$8.3E-06^{2)}$	1	50	V/ms	
$V_{DDEXTDC}$ voltage during cranking	$V_{DDEXTDC CRANKING SR}$	2.97	-	7	V	Up to 2.8 h; EVRC in reset (no switching); Cold PORST is not triggered

(table continues...)

Table 84 (continued) Line Transients

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
$V_{DDEXTDC}$ voltage during standby	$V_{DDEXTDC}$ STANDBY <i>SR</i>	0.0	-	7	V	Up to 2.8 h; EVRC in reset (no switching); Higher standby current if $V_{DDEXTDC}$ is kept supplied
V_{DDEXT} voltage during cranking	V_{DDEXT} CRANKING <i>SR</i>	2.97	-	5.5	V	Cold PORST is not triggered
V_{DDEXT} voltage during standby	V_{DDEXT} STANDBY <i>SR</i>	0.0	-	5.5	V	Higher standby current if V_{DDEXT} is kept supplied
$V_{DDEVRSB}$ voltage during cranking	$V_{DDEVRSB}$ CRANKING <i>SR</i>	2.97	-	5.5	V	Cold PORST is not triggered
$V_{DDEVRSB}$ voltage during standby	$V_{DDEVRSB}$ STANDBY <i>SR</i>	2.6	-	5.5	V	

- 1) The device is robust against residual voltage ramp-up starting between [0 up to minimal operational voltage] for V_{DDEXT} , $V_{DDEVRSB}$, $V_{DDEXTDC}$, V_{DDHSIF} (if applicable), V_{DDM} and V_{DD} .
- 2) The slope is defined as the maximal tangential slope between 0% to 100% voltage level. Actual waveform may not represent the specification.

Related information

[Power supply topology](#) on page 492

[Supply ramp-up and ramp-down behavior](#) on page 493

[LVD reset characteristics](#) on page 494

4.16 PMS characteristics

The PMS is comprised of 3 power domain partitions PMS0, PMS1, and PMS2, to support the low power STANDBY0 and STANDBY1 modes. Each of the domains has its own voltage regulator:

- VDDPMS0 is used for the PMS0 domain
- VDDPMS1 is used for the PMS1/PMS2 domains

The EVRC SMPS regulator is also included in the PMS. Its purpose is to provide the main VDD core voltage.

The entire power supply topology can be found in chapter 'Power Supply Topology'.

4.16.1 VDDPMS0 and VDDSBRAM regulator characteristics

Table 85 VDDPMS0 and VDDSBRAM regulator characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input $V_{DDEVRSB}$ voltage range during start-up and operation mode transitions	$V_{DDEVRSBIN SR}$	2.76	-	6.5	V	
VDDPMS0 regulator output voltage Static accuracy without dynamic load/line regulation - untrimmed	$V_{DDPMS0OUT CC}$	0.88	0.95	1	V	
VDDPMS0 regulator output voltage range including load/line regulation and aging	$V_{DDPMS0 CC}$	0.88	0.95	1	V	
VDDPMS0 maximum output load current	$I_{DDPMS0MAX SR}$	-	-	1	mA	
VDDPMS0 and VDDSBRAM regulator line transient response	$dV_{DDPMS0}/dV_{IN CC}$	-20	-	20	mV	$dV/dT = 50 \text{ V/ms}$; $dV < 2.97-5.5 \text{ V} $; $C_L = 1 \text{ nF}$ (C_L is an on-chip load capacitor)
Input $V_{DDEVRSB}$ voltage range during standby operation	$V_{DDEVRSBINST BY SR}$	2.6	-	-	V	

Related information

[VDDPMS1 regulator characteristics](#) on page 498

[EVRC SMPS characteristics](#) on page 499

[EVRC SMPS external components](#) on page 502

[Internal supply voltage operating conditions](#) on page 504

4.16.2 VDDPMS1 regulator characteristics

Table 86 VDDPMS1 regulator characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VDDPMS1 regulator output voltage static accuracy without dynamic load/line regulation - untrimmed	$V_{DDPMS1UT CC}$	0.936	0.98	1.024	V	
VDDPMS1 regulator output voltage static accuracy without dynamic load/line regulation - trimmed	$V_{DDPMS1T CC}$	0.93	0.95	0.97	V	Standby mode at 70 kHz
		0.96	0.98	1	V	Standby mode and operation at 100 MHz
VDDPMS1 regulator output voltage range including load/line regulation and aging	$V_{DDPMS1 CC}$	0.91	0.95	0.97	V	Standby mode at 70 kHz
		0.94	0.98	1.00	V	Standby mode and operation at 100 MHz
VDDPMS1 maximum output load current	$I_{DDPMS1MAX SR}$	-	-	15	mA	
VDDPMS1 regulator load transient response	$dV_{DDPMS1}/dI_{OUT CC}$	-60	-	60	mV	$dI < \pm 3 \text{ mA}$; $t_r = 0.01 \mu\text{s}$; $t_f = 0.01 \mu\text{s}$; $T_{\text{settle}} = 20 \mu\text{s}$; $C_L = 1.5 \text{ nF}$ (C_L is an on-chip load capacitor); VDDPMS1 regulator in high current sink mode
Maximum load step limitation of VDDPMS1 regulator	$dI_{DDPMS1}/dI_{OUT SR}$	-	-	4	mA	SW limits load jumps
VDDPMS1 regulator line transient response	$dV_{DDPMS1}/dV_{IN CC}$	-15	-	15	mV	$dV/dT = 50 \text{ V/ms}$; $dV < 2.97\text{-}5.5 \text{ V} $

Related information

[VDDPMS0 and VDDSB RAM regulator characteristics](#) on page 497

[EVRC SMPS characteristics](#) on page 499

[EVRC SMPS external components](#) on page 502

[Internal supply voltage operating conditions](#) on page 504

4.16.3 EVRC SMPS characteristics

Table 87 EVRC SMPS characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input $V_{DDEXTDC}$ Voltage range during start-up ¹⁾	$V_{INEXTDCSTR}$ SR	2.6 ²⁾	-	6.5	V	$V_{DDEXTDC} = 3.3\text{ V}/5\text{ V}$ nominal voltage, EVRC in reset (no switching). Operation between 5.5 V and 6.5 V is limited to max. 2.8 h
		3.5	-	7.5	V	HWCFG [2:1] = [11]. High-voltage $V_{DDEXTDC}$ mode, EVRC in reset (no switching). Operation between 7.0 V and 7.5 V is limited to max. 2.8 h
Input $V_{DDEXTDC}$ voltage range during operation mode	$V_{INEXTDC}$ SR	2.97	-	5.5	V	$V_{DDEXTDC} = 3.3\text{ V}/5\text{ V}$ nominal voltage
		4.95	-	7.0	V	HWCFG [2:1] = [11]. High-voltage $V_{DDEXTDC}$ mode
Input $V_{DDEXTDC}$ and $V_{DDEVRSB}$ peak to peak Voltage Ripple during start-up and operation, at the external regulator output	$V_{INRIPPLE}$ SR	-	0.1	0.3	V	100 kHz < f_{ripple} < 3 MHz; square/sinusoidal ripple may be assumed
SMPS regulator output voltage range including load/line regulation and aging - trimmed	V_{DDDC} CC	0.983	1.025	1.087	V	$I_{DDEXTDC} \leq I_{DDDC} \leq I_{DDDCMAX}$; $V_{ID} = \text{slow} + \text{typical samples}$; for load transients $ dI < 200\text{ mA}$
		0.936	0.975	1.034	V	$I_{DDEXTDC} \leq I_{DDDC} \leq I_{DDDCMAX}$; $V_{ID} = \text{fast samples}$; for load transients $ dI < 200\text{ mA}$
SMPS regulator static voltage output accuracy without dynamic load/line regulation - trimmed	V_{DDDCCT} CC	1.004	1.025	1.046	V	$I_{DDEXTDC} \leq I_{DDDC} \leq I_{DDDCMAX}$; $V_{ID} = \text{slow} + \text{typical samples}$; Voltage at V_{DD_SENSE} (EVRC feedback)
		0.955	0.975	0.995	V	$I_{DDEXTDC} \leq I_{DDDC} \leq I_{DDDCMAX}$; $V_{ID} = \text{fast samples}$; Voltage at V_{DD_SENSE} (EVRC feedback)
SMPS regulator static voltage output accuracy without dynamic load/line regulation - untrimmed	V_{DDDCUT} CC	0.975	1.025	1.075	V	$I_{DD\_LEAK} \leq I_{DDDC} \leq I_{DDDCSTR}$

(table continues...)

Table 87 (continued) EVRC SMPS characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Programmable switching frequency after trimming	$f_{\text{DCDC}} \text{ SR}$	-	0.8	-	MHz	$I_{\text{DDDC}} \leq I_{\text{DDDCMAX}}$ (HE case); start-up frequency switches from 444 kHz in open loop operation to f_{DCDC} in closed loop operation
		-	0.45	-	MHz	$I_{\text{DDDC}} \leq I_{\text{DDDCMAX}}$ (HE case); start-up frequency switches from 444 kHz in open loop operation to f_{DCDC} in closed loop operation
Start-up time	$t_{\text{STRDC}} \text{ CC}$	0.2	-	1.5	ms	SMPS start-up mode; it is defined as the EVRC ramp-up time from 0V until V_{DD} nominal voltage reached, on condition that all other PORST requirements were released before; $I_{\text{DDDC}} = I_{\text{DDDCSTRT}}$
Switching frequency modulation spread	$\Delta T_{\text{DCSPR}} \text{ SR}$	-	10	-	ns	Modulation spread of the switching frequency, expressed as time period instead of frequency
Maximum ripple at I_{MAX}	$\Delta V_{\text{DDDC}} \text{ CC}$	-	-	14	mV	$I_{\text{DDDCSTRT}} \leq I_{\text{DDDC}} \leq I_{\text{DDDCMAX}}$; $\Delta V_{\text{DDDC}} = (\text{peak-to-peak ripple} / 2)$
Current consumption of SMPS regulator at minimum load	$I_{\text{DCNL}} \text{ CC}$	-	-	30	mA	$f_{\text{DCDC}} = 0.8 \text{ MHz}$; $I_{\text{DDDC}} = 10 \text{ mA}$; $T_J = 25^\circ\text{C}$; current drawn from the V_{DDEXTDC} rail
Standby/Quiescent current consumption of SMPS regulator	$I_{\text{DCSTBY}} \text{ CC}$	-	10	-	μA	EVRC off in standby mode; current drawn from the V_{DDEXTDC} rail; V_{DDEXTDC} LV case (3.3 V/5 V); $V_{\text{DDEXTDC}} = 3.3 \text{ V}/5 \text{ V} \pm 10\%$; $T_J \leq 25^\circ\text{C}$
		-	20	-	μA	EVRC off in standby mode; current drawn from the V_{DDEXTDC} rail; V_{DDEXTDC} LV case (3.3 V/5 V); $V_{\text{DDEXTDC}} = 3.3 \text{ V}/5 \text{ V} \pm 10\%$; $25^\circ\text{C} < T_J \leq T_J(\text{Max})$
		-	2.6	-	mA	EVRC off in standby mode; current drawn from the V_{DDEXTDC} rail; V_{DDEXTDC} HV case (6.5 V); V_{DDEXTDC} remains supplied at 6.5 V

(table continues...)

Table 87 (continued) EVRC SMPS characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SMPS regulator peak efficiency	n_{DC} SR	-	85	-	%	$V_{IN} = 3.3$ V; $f_{DCDC} = 0.45$ MHz
		-	85	-	%	$V_{IN} = 3.3$ V; $f_{DCDC} = 0.8$ MHz
Maximum output current	$I_{DDDCMAX}$ CC	-	-	5.5	A	HE case, RUN Mode 3)
Load current during SMPS regulator start-up	$I_{DDDCSTRT}$ CC	0.1	-	3	A	HE, PORST asserted
SMPS regulator line transient response	dV_{DDDC}/dV_{IN} CC	-6	-	6	%	Expressed as % of V_{DDDC} nominal value; $dV/dt = 120$ V/ms; $ dV < V_{INEXTDCSTRT}(\text{Min}) - V_{INEXTDCSTRT}(\text{Max}) $; does not include EVRC ripple.
		-1	-	1	%	Expressed as % of V_{DDDC} nominal value; $dV/dt = 1$ V/ms; $ dV < V_{INEXTDCSTRT}(\text{Min}) - V_{INEXTDCSTRT}(\text{Max}) $; does not include EVRC ripple.
SMPS regulator load transient response before trimming	dV_{DDDCUT}/dI_{OUT} CC	-4	-	4	%	Expressed as % of V_{DDDC} nominal value; $ dI < dI_{DDDC_STRT}$; $I_{DDDC} = I_{DDDCSTRT}$; $t_r = 0.1$ μ s; $t_f = 0.1$ μ s; V_{DDDC} untrimmed; $T_{settle} = 20$ μ s; HE components; includes EVRC ripple
		-4	-	4	%	Expressed as % of V_{DDDC} nominal value; $ dI < dI_{DDDC_LBIST} $; $I_{DDDC} = I_{DDDCSTRT}$; EVRC bandgap and clock trimmed but operated with default coefficients; HE components; includes EVRC ripple
Input Synchronisation frequency	$f_{DCDCSYNC}$ SR	0.42	0.45	0.49	MHz	$f_{DCDC} = 0.45$ MHz HE case
		0.72	0.8	0.9	MHz	$f_{DCDC} = 0.8$ MHz HE case
Feedback ADC resolution for voltage scaling	dV_{FBADC} SR	-	2.83	-	mV	Used for scaling of VDD target value in EVRC_CON0 register. Feedback ADC nominal range < 1.446 V

1) Voltage range dependent on used MOSFETs (see chapter PMS in User Manual)

2) LCDCDC standalone lower limit. The minimum startup voltage of LCDCDC also depends on LVD reset threshold and Primary undervoltage thresholds of VDDEVRB, VDDEXT, VDDEXTDC

3) HE refers to EVRC configuration and components for $I_{DD} < I_{DDDCMAX}$ for HE case

Related information

[VDDPMS0 and VDDSB RAM regulator characteristics](#) on page 497

[VDDPMS1 regulator characteristics](#) on page 498

[EVRC SMPS external components](#) on page 502

[Internal supply voltage operating conditions](#) on page 504

4.16.4 EVRC SMPS external components

Table 88 EVRC SMPS external components

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
External output capacitor value	$C_{OUT\ SR}$	28.6	44	59.4	μF	$I_{DDDC} \leq I_{DDDCMAX}$; $f_{DCDC} = 0.8$ MHz; 2 * 22 μF connected in parallel
		35.75	55	74.25	μF	$I_{DDDC} \leq I_{DDDCMAX}$; $f_{DCDC} = 0.45$ MHz; 33 μF + 22 μF connected in parallel
External output capacitor ESR	$C_{OUT\_ESR\ SR}$	-	-	100	Ohm	$f = 10$ Hz
		-	-	20	mOhm	$f \geq 0.5$ MHz ; $f \leq 10$ MHz
External input capacitor values (Buffer + Decoupling) ¹⁾	$C_{IN\ SR}$	14.3 + 0.065	22 + 0.1 ²⁾	29.7 + 0.135	μF	$I_{DDDC} \leq I_{DDDCMAX}$; $f_{DCDC} = 0.45$ MHz
		14.3 + 0.065	22 + 0.1 ²⁾	29.7 + 0.135	μF	$I_{DDDC} \leq I_{DDDCMAX}$; $f_{DCDC} = 0.8$ MHz
External input capacitor ESR	$C_{IN\_ESR\ SR}$	-	-	20	mOhm	$f \geq 0.5$ MHz; $f \leq 10$ MHz
		-	-	100	Ohm	$f = 100$ Hz
External inductor value	$L_{DC\ SR}$	1.54	2.2	2.86	μH	$f_{DCDC} = 0.8$ MHz
		1.54	2.2	2.86	μH	$f_{DCDC} = 0.45$ MHz
External inductor DCR	$L_{DC\_DCR\ SR}$	-	-	0.02	Ohm	Max. value depending on output current
External Inductor Saturation Current Margin	$\Delta I_{SAT\ SR}$	400	-	-	mA	The saturation current of the coil must be larger than $I_{DDDC} + \Delta I_{SAT}$
P + N-channel MOSFET Gate threshold voltage	$V_{GSTH\ SR}$	-	1	-	V	NMOS
		-	-1	-	V	PMOS

(table continues...)

Table 88 (continued) EVRC SMPS external components

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SMPS regulator load transient response after trimming	$dV_{DDDC}/dI_{OUT\ CC}$	-2.5	-	9	%	Expressed as % of V_{DDDC} nominal value; $-800\text{ mA} < dI < 0\text{ mA}$; negative value specifies the max. undershoot after the overshoot; $I_{DD}(\text{Freerun}) \leq I_{DDDC} \leq I_{DDDCMAX}$; $t_f = 0.1\text{ }\mu\text{s}$; $T_{\text{settle}} = 40\text{ }\mu\text{s}$; application reset load drop; includes EVRC ripple ³⁾
		-4	-	4	%	Expressed as % of V_{DDDC} nominal value; $-450\text{ mA} < dI < 450\text{ mA}$; $I_{DD}(\text{Freerun}) \leq I_{DDDC} \leq I_{DDDCMAX}$; $t_r = 0.1\text{ }\mu\text{s}$; $t_f = 0.1\text{ }\mu\text{s}$; two consecutive load transients, in the same direction, separated by a time of $20\text{ }\mu\text{s}$; PPU+2xCPU load jump; includes EVRC ripple ³⁾
		-2.75	-	2.0	%	Expressed as % of V_{DDDC} nominal value; $-200\text{ mA} < dI < 200\text{ mA}$; $I_{DD}(\text{Freerun}) \leq I_{DDDC} \leq I_{DDDCMAX}$; $t_r = 0.1\text{ }\mu\text{s}$; $t_f = 0.1\text{ }\mu\text{s}$; $T_{\text{settle}} = 20\text{ }\mu\text{s}$; 2 x CPU load jump; includes EVRC ripple
		-3	-	14	%	Expressed as % of V_{DDDC} nominal value; $-1.2\text{ A} < dI < 0\text{ A}$; negative value specifies the max. undershoot after the overshoot; $I_{DD}(\text{Freerun}) \leq I_{DDDC} \leq I_{DDDCMAX}$; $t_f = 0.1\text{ }\mu\text{s}$; $T_{\text{settle}} = 100\text{ }\mu\text{s}$; cold or warm PORST load drop; includes EVRC ripple ³⁾

- 1) The "+" means that both (Buffer and Decoupling) Capacitors have to be connected in parallel close to the external power stage. The smaller one (Decoupling Capacitor) needs to be placed as close as possible to the source connection of the PMOS.
- 2) Additional external components maybe required depending on EMI/EMC requirements
- 3) T_{settle} is the time after which the V_{DD} output voltage returns to within $\pm 1.5\%$ of the static EVRC output voltage value without any load transient.

Related information

[VDDPMS0 and VDDSB RAM regulator characteristics](#) on page 497

[VDDPMS1 regulator characteristics](#) on page 498

[EVRC SMPS characteristics](#) on page 499

[Internal supply voltage operating conditions](#) on page 504

4.16.5 Internal supply voltage operating conditions

Table 89 Internal supply voltage operating conditions

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Internal core supply voltage for PMS0	V_{DDPMS0} SR	0.80	0.95	1.08	V	
Internal core supply voltage for PMS1 and PMS2	$V_{DDPMS1,2}$ SR	0.81	0.95	1.08	V	Standby mode at 70 kHz
		0.81	0.98	1.13	V	Standby mode and operation at 100 MHz

Related information

[VDDPMS0 and VDDSB RAM regulator characteristics](#) on page 497

[VDDPMS1 regulator characteristics](#) on page 498

[EVRC SMPS characteristics](#) on page 499

[EVRC SMPS external components](#) on page 502

4.17 System mode dependent and reset timing characteristics

4.17.1 System state timings

Table 90 System state timings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
STANDBY0 entry transition time from STANDBY1_70k mode on SCR events	$t_{\text{STBY10}} \text{ CC}$	-	-	50	μs	
STANDBY0 exit transition time to STANDBY1_70k mode on wake-up events	$t_{\text{STBY01}} \text{ CC}$	-	-	150	μs	
Standby RAM supply switch activation time during Run mode on V_{DDEXT} or V_{DD} primary undervoltage event	$t_{\text{STBYRAM}} \text{ CC}$	-	-	1	μs	dLMU Standby RAM supply switched
STANDBY1 entry transition time from RUN mode on V_{DDEXT} or V_{DD} undervoltage event	$t_{\text{RXSTBY1}} \text{ CC}$	-	1	10	μs	Current consumption I_{STANDBY1} reached
STANDBY1 transition time to disable Bandgap and ADCOMP	$t_{\text{ADC100M}} \text{ CC}$	-	-	10	μs	SCR ADCOMP and HPBG disable, with SCU_PMS1IVRCON.SINKCTRLE N=0
STANDBY1 transition time to enable Bandgap and ADCOMP	$t_{\text{100MADC}} \text{ CC}$	-	-	50	μs	SCR ADCOMP_CON.EN_REQ request until ADCOMP_RESHSTAT.EN_STAT set to 1. ADCOMP SUCAL not considered, with SCU_PMS1IVRCON.SINKCTRLE N=0
STANDBY1 transition time to disable back-up clock	$t_{\text{100M70k}} \text{ CC}$	-	-	110	μs	SCR f_{SBT} clock request via SCU_CLK.DIV_REQ to switch off f_{BACKT} clock, with SCU_PMS1IVRCON.SINKCTRLE N=0
STANDBY1 transition time to enable back-up clock	$t_{\text{70k100M}} \text{ SR}$	-	-	170	μs	SCR f_{BACKT} clock request via SCU_CLK.DIV_REQ until SCU_CLK.DIV_STAT is updated

(table continues...)

Table 90 (continued) System state timings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Minimum HWCFG hold time after LVDANA reset release during start-up	$t_{\text{HWCFG}} \text{ SR}$	200	-	400	μs	HWCFG latch after start-up for EVRC configuration. V_{DDEXT} , V_{DDEVRSB} and V_{DDEXTDC} above LVD detector levels. $R_{\text{HWCFG}} = 4.7 \text{ k}\Omega \pm 50\%$, $V_{\text{IL}} = \text{see } V_{\text{IL\_HWCFG}}$, $V_{\text{IH}} = \text{see } V_{\text{IH\_HWCFG}}$.
Power domain supply switch-off transition time after taken request	$t_{\text{PDDIS}} \text{ CC}$	-	-	200	μs	Load jump sequencing of 25 mA / 5 μs as default reset value. $\text{PD\_CON0.CLKPPU} = [000, 001, 010, 011 \text{ or } 100]$
Minimum external supplies hold time after warm reset assertion	$t_{\text{SUPHOLD}} \text{ SR}$	360	-	-	μs	Valid for all primary voltage monitors to ensure proper reset shutdown sequencing.
MBIST execution time extending the boot time	$t_{\text{MBIST}} \text{ CC}$	-	-	6	ms	Key-on MBIST (4N-DT, $f_{\text{SRI}}=100 \text{ MHz}$) and consecutive initialization. Configuration details incl. SRAM-grouping described in UM, VMT-chapter.
		-	25	-	ms	Key-off MBIST (4N-DT, $f_{\text{SRI}} = \text{MAX}$). Configuration details incl. SRAM-grouping described in UM, VMT-chapter.
LBIST execution time	$t_{\text{LBIST}} \text{ CC}$	-	-	50	ms	Key-off LBIST; Time per LBIST-Cluster; Reset time excluded
		-	-	6	ms	Key-on LBIST; Reset time excluded
Timing-Window available for placement of external Tool-Requests via COMDATA/ Cerberus	$t_{\text{WINDOW}} \text{ CC}$	800	-	-	μs	In case of DXCPL used, shortened SPD-0-bitwidth in Activation sequence required.
Transitioning time to permanent reset	$t_{\text{WCST}} \text{ CC}$	-	-	43	ms	Time is a sum of t_{BCP} (incl. EVR ramp-up) + t_{BCP} (w/o EVR ramp-up) + 2 * (FW fault handling time + $t_{\text{CPU0WDT}} + t_{\text{RTC}} + t_{\text{WARMRSTSEQ}}$)

Related information

[Reset timings](#) on page 507

[Power, pad and reset timing figure](#) on page 509

4.17.2 Reset timings

Table 91 Reset timings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Cold Power on Reset Boot Time ¹⁾	$t_{BCP\ CC}$	-	-	3.3	ms	Firmware execution time after PORST release without EVRC ramp-up; RAM initialization, LBIST execution and CSRM boot time is not included ²⁾
		-	3	5.5	ms	$dV_{DDEXT}/dT = 1\text{ V/ms}$; $V_{DDEXT} > V_{LVDRST5}$; boot time after Cold PORST including EVRC ramp-up, PBIST and Firmware execution time; RAM initialization and CSRM boot time are not included
Minimum cold PORST reset hold time in case of power fail event issued by EVR primary VMONP monitors	$t_{EVRPOR\ CC}$	10 ³⁾	-	-	μs	
Minimum PORST active hold time externally after power supplies are stable at operating levels after start-up	$t_{POA\ SR}$	-	1 ⁴⁾	-	ms	
EVRC ramp-up time till cold PORST reset release	$t_{EVRstartup\ CC}$	-	1	2	ms	It is defined from the $V_{EXTDCPRIUV}$ reset threshold crossing until cold PORST reset release. $dV/dT=1\text{ V/ms}$; EVRC active
Application Reset Boot Time	$t_{BAR\ CC}$	-	-	750	μs	operating with max. frequencies, with valid BMHD header; Warm Reset Sequencing Delay Time not included
System Reset Boot Time ²⁾	$t_{BSR\ CC}$	-	-	2	ms	w/o SWAP, with valid BMHD header
Warm PORST reset boot time ²⁾	$t_{BWP\ CC}$	-	-	3	ms	Start from internal NVM with configured BMHD. Time does not include RAM initialization, Foreground CSRM-Boot, ABM and LBIST-Runtime
Warm Reset Sequencing Delay Time	$t_{WARMRSTSEQ\ CC}$	-	-	300	μs	
Configurable PORST digital filter delay in addition to analog pad filter delay	$t_{PORSTDF\ CC}$	600	-	1200	ns	

(table continues...)

Table 91 (continued) Reset timings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Ports inactive after ESR0 reset active	$t_{PI\ CC}$	-	-	$8 / f_{SPB}$	ns	
Ports inactive after PORST reset active	$t_{PIP\ CC}$	-	-	600	ns	
Hold time from PORST rising edge	$t_{POH\ SR}$	360	-	-	ns	
Setup time to PORST rising edge	$t_{POS\ SR}$	0	-	-	ns	
SCR reset boot time ²⁾	$t_{SCRBOOT\ CC}$	-	-	60	μs	On user mode entry at 20 MHz SCR core clock, Standby exit, WDT (System) double bit ECC reset and soft reset
		-	-	230	μs	On user mode entry at 70 kHz SCR core clock, Standby exit, WDT (System) double bit ECC reset and soft reset

- 1) RAM initialization in SSW of PMEM, DMEM, PTAG, DTAG and DLMU RAMs add 1000 μs in addition.
- 2) From release of PORST by PMS
- 3) Cold PORST reset is driven by μC and maintained in an extended voltage range between V_{DDPPA} limit and absolute maximum rating voltage limits.
- 4) The reset release on supply ramp-up or supply restoration is delayed by a voltage hysteresis of 1.5% (default value) above the undervoltage reset limit implemented on V_{DDEXT} , V_{DDHSIF} (if applicable) and V_{DD} rails. This mechanism helps to avoid multiple consecutive cold PORST events during slow supply ramp-ups owing to voltage drop/current jumps when reset is released. The t_{POA} additional time is recommended for a robust start-up and not a mandatory requirement.

Related information

[System state timings](#) on page 505

[Power, pad and reset timing figure](#) on page 509

4.17.3 Power, pad and reset timing figure

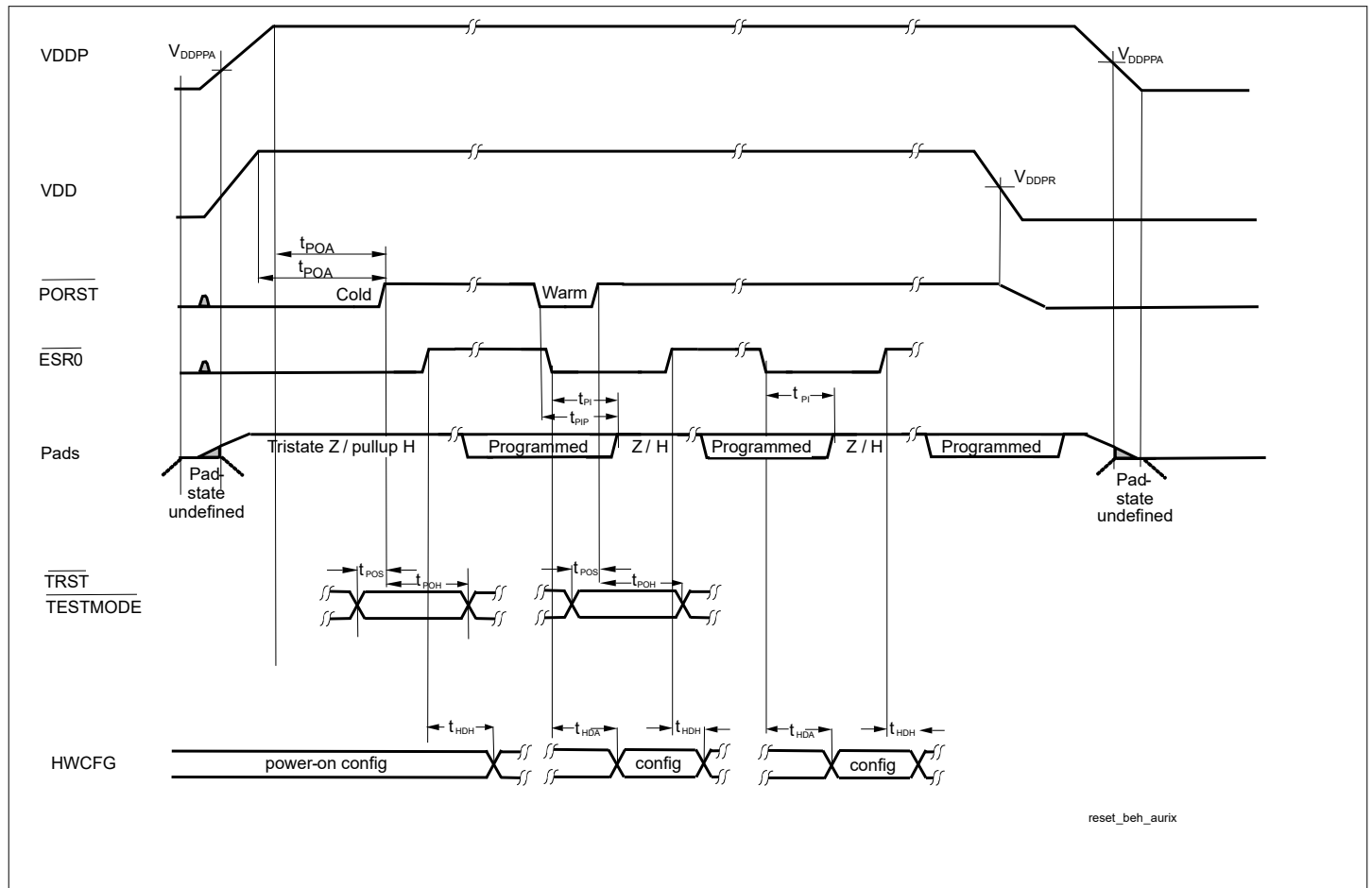


Figure 8 Power, pad and reset timing

Related information

[System state timings](#) on page 505

[Reset timings](#) on page 507

4.18 PMS voltage monitoring characteristics

The supply rails monitored by primary and secondary voltage monitors are measured by primary and secondary monitor ADCs. Four ADC topologies are used for this purpose:

- Tracking High Voltage ADC (TRKHV)
- Tracking Core ADC (TRKCORE)
- SAR High Voltage ADC (SARHV)
- SAR Core ADC (SARCORE)

The characteristics of this ADCs can be found in the following sub-chapter.

4.18.1 Primary and secondary voltage monitor ADC characteristics

Table 92 Primary and secondary voltage monitor ADC characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Core tracking ADC characteristics						
Core tracking ADC least significant bit	$V_{TRKCORELSB\ CC}$	-	2.830	-	mV	LSB value is supposed to be used for theoretical voltage threshold calculation
Core tracking ADC measurement latency	$t_{TRKCORE\ CC}$	-	-	21	ns	Back-up Clock oscillator trimmed; spike FILTER = 0; with one single ADC input used
High-voltage tracking ADC characteristics						
High-voltage tracking ADC least significant bit	$V_{TRKHVLSB\ CC}$	-	11.32	-	mV	LSB value is supposed to be used for theoretical voltage threshold calculation
High-voltage tracking ADC measurement latency	$t_{TRKHV\ CC}$	-	-	41	ns	Back-up Clock oscillator trimmed; spike FILTER = 0; with one single ADC input used
Core SAR ADC characteristics						
Core SAR ADC least significant bit	$V_{SARCORELSB\ CC}$	-	0.586	-	mV	LSB value is supposed to be used for theoretical voltage threshold calculation
Core SAR ADC measurement latency	$t_{SARCORE\ CC}$	-	420	430	ns	Back-up Clock oscillator trimmed; spike FILTER = 0; with one single ADC input used; after firmware boot
High-voltage SAR ADC characteristics						
High-voltage SAR ADC measurement latency	$t_{SARHV\ CC}$	-	-	450	ns	Back-up Clock oscillator trimmed; spike FILTER = 0; with one single ADC input used
High-voltage SAR ADC least significant bit	$V_{SARHVLSB\ CC}$	-	2.830	-	mV	LSB value is supposed to be used for theoretical voltage threshold calculation

4.18.2 Primary voltage monitors

4.18.2.1 Primary voltage monitors parameters overview

Note: This table includes all voltage rails available for the TC4x family. The availability per derivative can be looked up in the [Primary voltage monitors characteristics table](#).

Table 93 **Primary voltage monitors parameters**

Voltage rail	VMONP LSB datasheet parameter	Primary under-voltage reset threshold after trimming - datasheet parameter	Effect of primary under-voltage reset threshold violation ¹⁾
V_{DD}	$V_{TRKCORELSB}$	$V_{DDPRIUV}$	Cold PORST
V_{DDEXT}	$V_{TRKHVLSB}$	$V_{EXTPRIUV}$	Cold PORST
$(V_{DDEXTDC} - V_{SSDCHS})$	$V_{TRKHVLSB}$	$V_{DCHSPRIUV}$	Cold PORST only if $HWCFG[2:1] = 11_B$
$V_{DDEXTDC}$	$V_{TRKHVLSB}$	$V_{EXTDCPRIUV}$	Only when EVRC is enabled, a power state transition corresponding to an EVRC failure is triggered. The primary monitor triggers not only a cold PORST, but a deeper power state where the EVRC regulator is disabled, until the supply raises above the reset release threshold.
V_{DDDCLS}	$V_{TRKHVLSB}$	$V_{DCLSPRIUV}$	Cold PORST only if $HWCFG[2:1] = 11_B$
$V_{DDEVRSB}$	$V_{SARHVLSB}$	$V_{EVRSBPRIUV}$	Cold PORST
$V_{DDP3NVM}$	$V_{SARHVLSB}$	$V_{DDP3NVPRIUV}$	Cold PORST
V_{DDM}	$V_{SARHVLSB}$	$V_{DDMPRIUV}$	Cold PORST
$V_{DDPPHYx}$	$V_{SARHVLSB}$	$V_{PPHYPRIUV}$	Cold PORST
$V_{DDPHRIFx}$	$V_{SARHVLSB}$	$V_{PHRIFPRIUV}$	Cold PORST
V_{DDHSIF}	$V_{SARHVLSB}$	$V_{HSIFPRIUV}$	Cold PORST
V_{DDPAD}	$V_{SARCORELSB}$	$V_{DDPADPRIUV}$	Cold PORST
V_{DDCPUx}	$V_{SARCORELSB}$	$V_{DDCPUPRIUV}$	Cold PORST
V_{DDPPU}	$V_{SARCORELSB}$	$V_{DDPPUPRIUV}$	Cold PORST
V_{DDLmux}	$V_{SARCORELSB}$	$V_{DDLMPRIUV}$	Cold PORST
V_{DDPHYx}	$V_{SARCORELSB}$	$V_{DDPHYPRIUV}$	Cold PORST
V_{DDRIFx}	$V_{SARCORELSB}$	$V_{DDRIFPRIUV}$	Cold PORST

1) Only if the respective VMONP_VxxRST.RESETOFF bit is set to zero.

Related information

[Primary voltage monitors characteristics](#) on page 512

4.18.2.2 Primary voltage monitors characteristics

Table 94 Primary voltage monitors characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Non-configurable cold PORST thresholds						
$V_{DDEXTDC}$ primary undervoltage reset threshold before trimming ¹⁾	$V_{RSTEXTDC}$ CC	2.6	-	3	V	By last cold PORST release on supply ramp-up including voltage hysteresis ²⁾
V_{DDEXT} primary undervoltage reset threshold before trimming ¹⁾	V_{RSTEXT} CC	2.6	-	3.0	V	By last cold PORST release on supply ramp-up including voltage hysteresis ²⁾
$V_{DDEVRSB}$ primary undervoltage reset threshold before trimming ¹⁾	$V_{RSTEVR SB}$ CC	2.6	-	3.0	V	By last cold PORST release on supply ramp-up including voltage hysteresis ²⁾
V_{DDM} primary undervoltage reset threshold before trimming ¹⁾	$V_{RSTD DM}$ CC	2.6	-	3.0	V	By last cold PORST release on supply ramp-up including voltage hysteresis ²⁾
$V_{DDEXTDC} - V_{SSDCHS}$ primary undervoltage reset threshold before trimming; Only for PBIST ¹⁾	$V_{RSTDCHS}$ CC	2.6	-	3.0	V	By last cold PORST release on supply ramp-up including voltage hysteresis only in $V_{DDEXTDC}$ HV Mode ²⁾
V_{DDDCLS} primary undervoltage reset threshold before trimming; Only for PBIST ¹⁾	$V_{RSTDCLS}$ CC	2.6	-	3.0	V	By last cold PORST release on supply ramp-up including voltage hysteresis only in $V_{DDEXTDC}$ HV Mode ²⁾
V_{DD} primary undervoltage reset threshold before trimming	V_{RSTVDD} CC	-	-	0.894	V	By last cold PORST release on supply ramp-up including voltage hysteresis ²⁾
Configurable cold PORST thresholds						
$V_{DDEXTDC}$ primary undervoltage reset threshold after trimming ¹⁾	$V_{EXTDCPRIUV}$ CC	2.817	2.875	2.933	V	Default cold PORST PRIUV threshold = 0xFE; RESETHYS = 0x0; $3.3\text{ V} \leq V_{DDEXTDC} \leq 5\text{ V}$ mode ²⁾
		3.528	3.600	3.672	V	Default cold PORST PRIUV threshold = 0x13E; RESETHYS = 0x0; $V_{DDEXTDC}$ high-voltage mode ²⁾

(table continues...)

Table 94 (continued) Primary voltage monitors characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
$(V_{DDEXTDC} - V_{SSDCHS})$ primary undervoltage reset threshold after trimming. ¹⁾	$V_{DCHSPRIUV}$ CC	2.817	2.875	2.933	V	Default cold PORST PRIUV threshold = 0xx; RESETHYS = 0xFE; $V_{DDEXTDC}$ high-voltage mode ²⁾
V_{DDDCLS} primary undervoltage reset threshold after trimming. ¹⁾	$V_{DCLSPRIUV}$ CC	2.817	2.875	2.933	V	Default cold PORST PRIUV threshold = 0xFE; RESETHYS = 0x0; $V_{DDEXTDC}$ high-voltage mode ²⁾
V_{DDEXT} primary undervoltage reset threshold after trimming. ¹⁾	$V_{EXTPRIUV}$ CC	2.817	2.875	2.933	V	Default cold PORST PRIUV threshold = 0xFE; RESETHYS = 0x0; $V_{DDEXT} = 3.3$ V mode ²⁾
		4.27	4.358	4.446	V	Configurable cold PORST PRIUV threshold = 0x181; RESETHYS = 0x0; $V_{DDEXT} = 5$ V mode ²⁾
$V_{DDEVRSB}$ primary undervoltage reset threshold after trimming. ¹⁾	$V_{EVRSBPRIUV}$ CC	2.82	2.878	2.936	V	Default cold PORST PRIUV threshold = 0x3F9; RESETHYS = 0x0; $V_{DDEXT} = 3.3$ V mode ²⁾
		4.276	4.364	4.452	V	Configurable cold PORST PRIUV threshold = 0x606; RESETHYS = 0x0; $V_{DDEXT} = 5$ V mode ²⁾
V_{DDEXT} , $V_{DDEVRSB}$, and V_{DDM} primary undervoltage monitor threshold during supply ramp-down (dV_{IO}/dt)	$V_{EXTPRIUVMIN}$ CC	2.76	-	-	V	Valid for $dV_{IO} / dt = 50$ V / ms; with one single ADC input used; for $V_{DDEVRSB}$ and V_{DDM} with a maximum spike filter setting of 0
V_{DDEXT} undervoltage monitor threshold for 5V Flash programming and erase operation	$V_{EXTLVFL}$ CC	4.35	4.4	4.5	V	No cold PORST generation. Only alarm signal to Flash

(table continues...)

Table 94 (continued) **Primary voltage monitors characteristics**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
V_{DDM} primary undervoltage reset threshold after trimming ¹⁾	$V_{DDMPRIUV}$ CC	2.820	2.878	2.936	V	Default cold PORST PRIUV threshold = 0x3F9; RESETHYS = 0x0; V_{DDM} = 3.3 V mode ²⁾
		4.276	4.364	4.452	V	Configurable cold PORST PRIUV threshold = 0x606; RESETHYS = 0x0; V_{DDM} = 5 V mode ²⁾
$V_{DDPHPHYX}$ primary undervoltage reset threshold after trimming ¹⁾	$V_{DDPHYPRIUV}$ CC	1.539	1.571	1.603	V	Optional configurable cold PORST PRIUV threshold = 0x22B; RESETHYS = 0x0 ²⁾
V_{DDPHYX} primary undervoltage reset threshold after trimming	$V_{DDPHYPRIUV}$ CC	0.852	0.870	0.888	V	Optional default cold PORST PRIUV threshold = 0x5CD; RESETHYS = 0x0; valid for devices with V_{DD} = 0.975 V ²⁾
		0.896	0.915	0.934	V	Optional configurable cold PORST PRIUV threshold = 0x619; RESETHYS = 0x0; valid for devices with V_{DD} = 1.025 V ²⁾
V_{DD} primary undervoltage reset threshold after trimming	$V_{DDPRIUV}$ CC	0.875 ³⁾	0.886	0.897	V	Default cold PORST PRIUV threshold = 0x139; RESETHYS = 0x0; Valid for devices with V_{DD} = 0.975 V ²⁾
		0.919	0.931	0.943	V	Configurable cold PORST PRIUV threshold = 0x149; RESETHYS = 0x0; valid for devices with V_{DD} = 1.025 V ²⁾
V_{DD} power domain cold reset level accuracy after trimming, for power-switched power domains	$V_{DDPDCLDUV}$ CC	0.754	0.770	0.786	V	Default power domain cold reset threshold = 0x110; RESETHYS = 0x0; valid for devices with V_{DD} = 0.975 V
		0.798	0.815	0.832	V	Configurable power domain cold reset threshold = 0x120; RESETHYS = 0x0; valid for devices with V_{DD} = 1.025 V

(table continues...)

Table 94 (continued) Primary voltage monitors characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
V_{DDPPU} primary undervoltage reset threshold after trimming	$V_{DDPPUPRIUV}$ CC	0.852	0.870	0.888	V	Optional default cold PORST PRIUV threshold = 0x5CD; RESETHYS = 0x0; valid for devices with $V_{DD} = 0.975$ V ²⁾
		0.896	0.915	0.934	V	Optional configurable cold PORST PRIUV threshold = 0x619; RESETHYS = 0x0; valid for devices with $V_{DD} = 1.025$ V ²⁾
V_{DDPAD} primary undervoltage reset threshold after trimming ⁴⁾	$V_{DDPADPRIUV}$ CC	0.852	0.870	0.888	V	Default cold PORST PRIUV threshold = 0x5CD; RESETHYS = 0x0; valid for devices with $V_{DD} = 0.975$ V ²⁾
		0.896	0.915	0.934	V	Configurable cold PORST PRIUV threshold = 0x619; RESETHYS = 0x0; valid for devices with $V_{DD} = 1.025$ V ²⁾
V_{DDEXT} and $V_{DDEVRSB}$ PBIST primary overvoltage monitor threshold	V_{PBIST5} CC	5.498	-	-	V	
V_{DD} PBIST primary overvoltage monitor threshold	V_{PBISTC} CC	1.128	1.200	1.272	V	
$V_{DDEXTHS}$ primary undervoltage reset threshold after trimming ¹⁾	$V_{EXTHSPRIUV}$ CC	2.820	2.878	2.936	V	Default cold PORST PRIUV threshold = 0x3F9; RESETHYS = 0x0; $V_{DDEXTHS} = 3.3$ V mode ²⁾
		4.276	4.364	4.452	V	Configurable cold PORST PRIUV threshold = 0x606; RESETHYS = 0x0; $V_{DDEXTHS} = 5$ V mode ²⁾

- 1) The monitor tolerances constitute the inherent variation of the band gap and ADC over process, voltage and temperature operational ranges. All voltages are measured on pins/dedicated sense pins (V_{DDxx_SENSE}) if available
- 2) Static voltage with supply slope less than or equal to 1 kV/s assumed as measurement condition.
- 3) V_{RSTxx} parameters are relevant only for the first cold PORST release. Later the reset levels are trimmed by the Firmware and reflected as $V_{xxPRIUV}$ parameters before device is used with full performance. The cold PORST is released with a voltage hysteresis on all the primary monitors to avoid consecutive PORST toggling behavior.
- 4) The reset release on supply ramp-up is delayed by a time duration 20-40 μ s after reaching undervoltage reset threshold and by a voltage hysteresis of 1.5% above the undervoltage reset limit. These mechanisms serve as hysteresis to avoid multiple consecutive cold PORST events during slow supply ramp-ups owing to voltage drop/current jumps when reset is released. In case the 3.3 V supply is provided externally, the internal drop will cause a reset at a higher voltage of 3.0 V at the V_{DDHSIF} (if available) pin.

Related information

[Primary voltage monitors parameters overview](#) on page 510

4.18.3 Secondary voltage monitors

4.18.3.1 Secondary voltage monitors parameters overview

Note: This table includes all voltage rails available for the TC4x family. The availability per derivative can be looked up in the [Secondary voltage monitors characteristics](#) table.

Table 95 Secondary voltage monitors parameters

Voltage rail	VMONS LSB datasheet parameter	Secondary voltage monitor accuracy after trimming - datasheet parameter	Effects of secondary voltage monitoring thresholds violation ¹⁾
$V_{DDEVRSB}$	$V_{SARHVLSB}$	$V_{DDEVRSBMON}$	UV, OV alarm
V_{DDEXT}	$V_{SARHVLSB}$	$V_{DDEXTMON}$	UV, OV alarm
$V_{DDP3NVM}$	$V_{SARHVLSB}$	$V_{DDP3NVMMON}$	UV, OV alarm
V_{DDM}	$V_{SARHVLSB}$	V_{DDMMON}	UV, OV alarm
V_{DDFLEX}	$V_{SARHVLSB}$	$V_{DDFLEXMON}$	UV, OV alarm
V_{DD}	$V_{SARCORELSB}$	V_{DDMON}	UV, OV alarm
V_{DDPMS0}	$V_{SARCORELSB}$	$V_{DDPMS0MON}$	UV, OV alarm
$V_{DDPMS1,2}$	$V_{SARCORELSB}$	$V_{DDPMS2MON}$	UV, OV alarm
$V_{DDSB RAM}$	$V_{SARCORELSB}$	$V_{DDPMS0MON}$	UV, OV alarm
V_{DDPAD}	$V_{SARCORELSB}$	$V_{DDPADMON}$	UV, OV alarm
$V_{DDPPHYx}$	$V_{SARHVLSB}$	$V_{DDPPHYxMON}$	UV, OV alarm
$V_{DDPHRIFx}$	$V_{SARHVLSB}$	$V_{DDPHRIFxMON}$	UV, OV alarm
V_{DDHSIF}	$V_{SARHVLSB}$	$V_{DDHSIFMON}$	UV, OV alarm
V_{DDPHYx}	$V_{SARCORELSB}$	$V_{DDPHYxMON}$	UV, OV alarm
V_{DDRIFx}	$V_{SARCORELSB}$	$V_{DDRIFxMON}$	UV, OV alarm
V_{DDCPUx}	$V_{SARCORELSB}$	$V_{DDCPUxMON}$	UV, OV alarm
V_{DDPPU}	$V_{SARCORELSB}$	$V_{DDPPUMON}$	UV, OV alarm
$V_{DDL MUX}$	$V_{SARCORELSB}$	$V_{DDL MUMON}$	UV, OV alarm
$V_{DDEXTDC}$	$V_{TRKHVLSB}$	$V_{DDEXTDCMON}$	UV, OV alarm

1) Only if the corresponding VMONS_VxxCON.UVMOD, respectively VMONS_VxxCON.OVMOD, are not zero.

Related information

[Secondary voltage monitors characteristics](#) on page 517

4.18.3.2 Secondary voltage monitors characteristics

Table 96 Secondary voltage monitors characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
$V_{DDEXTDC}$ secondary supply monitor accuracy after trimming	$V_{DDEXTDCMONCC}$	2.906	2.966	3.026	V	$V_{DDEXTDC} = 3.3$ V mode; xxVAL monitoring threshold = 2.966 V = 0x106 (UV); FILTER = 0 ¹⁾
		5.734	5.852	5.970	V	$V_{DDEXTDC}$ high-voltage mode; xxVAL monitoring threshold = 5.852 V = 0x205 (UV); FILTER = 0 ¹⁾
		5.391	5.502	5.613	V	$V_{DDEXTDC} = 5$ V mode; xxVAL monitoring threshold = 5.502 V = 0x1E6 (OV); FILTER = 0 ¹⁾
		6.856	6.996	7.136	V	$V_{DDEXTDC}$ high-voltage mode; xxVAL monitoring threshold = 6.996 V = 0x26A (OV); FILTER = 0 ¹⁾
		3.561	3.634	3.707	V	$V_{DDEXTDC} = 3.3$ V mode; xxVAL monitoring threshold = 3.634 V = 0x141 (OV); FILTER = 0 ¹⁾
		4.414	4.505	4.596	V	$V_{DDEXTDC} = 5$ V mode; xxVAL monitoring threshold = 4.505 V = 0x18D (UV); FILTER = 0 ¹⁾

(table continues...)

Table 96 (continued) Secondary voltage monitors characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
V_{DDEXT} secondary supply monitor accuracy after trimming	$V_{DDEXTMONCC}$	4.410	4.500	4.590	V	$V_{DDEXT} = 5\text{ V}$ mode; xxVAL monitoring threshold = 4.500 V = 0x636 (UV); FILTER = 0 ¹⁾
		5.389	5.499	5.609	V	$V_{DDEXT} = 5\text{ V}$ mode; xxVAL monitoring threshold = 5.499 V = 0x797 (OV); FILTER = 0 ¹⁾
		2.909	2.969	3.029	V	$V_{DDEXT} = 3.3\text{ V}$ mode; xxVAL monitoring threshold = 2.969 V = 0x419 (UV); FILTER = 0 ¹⁾
		3.558	3.631	3.704	V	$V_{DDEXT} = 3.3\text{ V}$ mode; xxVAL monitoring threshold = 3.631 V = 0x503 (OV); FILTER = 0 ¹⁾
$V_{DDEVRSB}$ secondary supply monitor accuracy after trimming	$V_{DDEVRSBMONCC}$	2.909	2.969	3.029	V	$V_{DDEXT} = 3.3\text{ V}$ mode; xxVAL monitoring threshold = 2.969 V = 0x419 (UV); FILTER = 0 ¹⁾
		4.410	4.500	4.590	V	$V_{DDEXT} = 5\text{ V}$ mode; xxVAL monitoring threshold = 4.500 V = 0x636 (UV); FILTER = 0 ¹⁾
		3.558	3.631	3.704	V	$V_{DDEXT} = 3.3\text{ V}$ mode; xxVAL monitoring threshold = 3.631 V = 0x503 (OV); FILTER = 0 ¹⁾
		5.389	5.499	5.609	V	$V_{DDEXT} = 5\text{ V}$ mode; xxVAL monitoring threshold = 5.499 V = 0x797 (OV); FILTER = 0 ¹⁾

(table continues...)

Table 96 (continued) **Secondary voltage monitors characteristics**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
V_{DDM} secondary supply monitor accuracy after trimming	V_{DDMMON} CC	2.909	2.969	3.029	V	V_{DDM} = 3.3 V mode; xxVAL monitoring threshold = 2.969 V = 0x419 (UV); FILTER = 0 ¹⁾
		3.558	3.631	3.704	V	V_{DDM} = 3.3 V mode; xxVAL monitoring threshold = 3.631 V = 0x503 (OV); FILTER = 0 ¹⁾
		5.389	5.499	5.609	V	V_{DDM} = 5 V mode; xxVAL monitoring threshold = 5.499V = 0x797(OV); FILTER = 0 ¹⁾
		4.410	4.500	4.590	V	V_{DDM} = 5 V mode; xxVAL monitoring threshold = 4.500 V = 0x636 (UV); FILTER = 0 ¹⁾
V_{DDFLEX} secondary supply monitor accuracy after trimming	$V_{DDFLEXMON}$ CC	2.909	2.969	3.029	V	V_{DDFLEX} = 3.3 V mode; xxVAL monitoring threshold = 2.969 V = 0x419(UV); FILTER = 0 ¹⁾
		3.558	3.631	3.704	V	V_{DDFLEX} = 3.3 V mode; xxVAL monitoring threshold = 3.631 V = 0x503(OV); FILTER = 0 ¹⁾
		5.389	5.499	5.609	V	V_{DDFLEX} = 5V mode; xxVAL monitoring threshold=5.499V= 0x797(OV); FILTER=0 ¹⁾
		4.410	4.500	4.590	V	V_{DDFLEX} = 5 V mode; xxVAL monitoring threshold = 4.500 V = 0x636(UV); FILTER = 0 ¹⁾
V_{DDPHYX} secondary supply monitor accuracy after trimming	$V_{DDPHYXMON}$ CC	1.586	1.619	1.652	V	xxVAL monitoring threshold = 1.619 V = 0x23C(UV); FILTER = 0 ¹⁾
		1.941	1.981	2.021	V	xxVAL monitoring threshold = 1.981 V = 0x2BC(OV); FILTER = 0 ¹⁾

(table continues...)

Table 96 (continued) Secondary voltage monitors characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
V_{DDPHYX} secondary supply monitor accuracy after trimming	$V_{DDPHYXMON}$ CC	0.879	0.897	0.915	V	xxVAL monitoring threshold = 0.897 V = 0x5FB(UV); FILTER = 0 ¹⁾
		1.084	1.107	1.130	V	xxVAL monitoring threshold = 1.107 V = 0x761(OV); FILTER = 0 ¹⁾
V_{DD} secondary supply monitor accuracy after trimming ²⁾	V_{DDMON} CC	0.879	0.897	0.915	V	xxVAL monitoring threshold = 0.897 V = 0x5FB(UV); FILTER = 0 ¹⁾
		1.105	1.128	1.151	V	xxVAL monitoring threshold = 1.128 V = 0x785(OV); FILTER = 0 ¹⁾
V_{DDPPU} secondary supply monitor accuracy after trimming	$V_{DDPPUMON}$ CC	0.879	0.897	0.915	V	xxVAL monitoring threshold = 0.897 V = 0x5FB(UV); FILTER = 0 ¹⁾
		1.105	1.128	1.151	V	xxVAL monitoring threshold = 1.128 V = 0x785(OV); FILTER = 0 ¹⁾
V_{DDPMS0} and $V_{DDSB RAM}$ secondary supply monitor accuracy after trimming ³⁾	$V_{DDPMS0MON}$ CC	0.768	0.785	0.801	V	xxVAL monitoring threshold = 0.785 V = 0x53B(UV); FILTER = 0 ¹⁾
		1.079	1.102	1.125	V	xxVAL monitoring threshold = 1.102 V = 0x759(OV); FILTER = 0 ¹⁾
V_{DDPMS1} and V_{DDPMS2} secondary supply monitor accuracy after trimming ³⁾	$V_{DDPMS2MON}$ CC	0.778	0.794	0.810	V	xxVAL monitoring threshold = 0.794 V = 0x54B(UV); FILTER = 0 ¹⁾
		1.129	1.153	1.177	V	xxVAL monitoring threshold = 1.153 V = 0x7B0(OV); FILTER = 0 ¹⁾
V_{DDPAD} secondary supply monitor accuracy after trimming	$V_{DDPADMON}$ CC	0.879	0.897	0.915	V	xxVAL monitoring threshold = 0.897 V = 0x5FB(UV); FILTER = 0 ¹⁾
		1.105	1.128	1.151	V	xxVAL monitoring threshold = 1.128 V = 0x785(OV); FILTER = 0 ¹⁾

(table continues...)

Table 96 (continued) Secondary voltage monitors characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
V_{DDSB} secondary supply monitor accuracy after trimming ³⁾	$V_{DDSBMON}$ CC	0.879	0.897	0.915	V	xxVAL monitoring threshold = 0.897 V = 0x5FB(UV); FILTER = 0 ¹⁾
		1.105	1.128	1.151	V	xxVAL monitoring threshold = 1.128 V = 0x785(OV); FILTER = 0 ¹⁾
$V_{DDEXTHS}$ secondary supply monitor accuracy after trimming	$V_{DDEXTHSMON}$ CC	4.410	4.500	4.590	V	$V_{DDEXTHS}$ = 5 V mode; xxVAL monitoring threshold = 4.500 V = 0x636 (UV); FILTER = 0 ¹⁾
		5.389	5.499	5.609	V	$V_{DDEXTHS}$ = 5 V mode; xxVAL monitoring threshold = 5.499 V = 0x797 (OV); FILTER = 0 ¹⁾
		2.909	2.969	3.029	V	$V_{DDEXTHS}$ = 3.3 V mode; xxVAL monitoring threshold = 2.969 V = 0x419 (UV); FILTER = 0 ¹⁾
		3.558	3.631	3.704	V	$V_{DDEXTHS}$ = 3.3 V mode; xxVAL monitoring threshold = 3.631 V = 0x503 (OV); FILTER = 0 ¹⁾

- 1) Static voltage with supply slope less than or equal to 1 kV/s assumed as measurement condition.
- 2) The monitor tolerances constitute the inherent variation of the band gap and ADC over process, voltage and temperature operational ranges. All voltages are measured on pins
- 3) To monitor voltage level not provided in conditions the values for OV and UV thresholds can be generated by a linear interpolation or extrapolation based on the given points.

Related information

[Secondary voltage monitors parameters overview](#) on page 516

4.19 Stand-by Controller (SCR)

4.19.1 SCR SAR ADC characteristics

Table 97 SCR SAR ADC characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Current consumption on VDDEVRSB supply	$I_{VDDEVRSB\ CC}$	-	0.7	1.25	mA	when ADC is turned on
Nominal SCR ADC Least Significant Bit Voltage	$V_{LSB\ CC}$	-	2.8302	-	mV	11 bit resolution. 5.7962V full range; BACKUP OSC and HPBG trimmed
Wake up Time at Digital Startup	$t_{WUADC\ CC}$	436	436	436	cycles	cycle time = $2 / f_{BACKT}$
Startup Calibration Time	$t_{SCAL\ CC}$	1477	1477	1477	cycles	cycle time = $2 / f_{BACKT}$
Sampling Time	$t_{SMV\ CC}$	80	-	-	ns	
Conversion Time	$t_{convMV\ CC}$	18	18	18	cycles	cycle time = $2 / f_{BACKT}$
Integral Non-Linearity	$E_{INL\ CC}$	-4	-	4	LSB	HPBG, BACKUP OSC trimmed, ADC calibrated, excluding noise
Differential Non - Linearity	$E_{DNL\ CC}$	-1	-	3	LSB	HPBG, BACKUP OSC trimmed, ADC calibrated, excluding noise
Offset Error	$E_{OFFSET\ CC}$	-4	-	4	LSB	HPBG, BACKUP OSC trimmed and ADC calibrated, excluding noise
Gain Error	$E_{GAIN\ CC}$	-11	-	11	LSB	HPBG, BACKUP OSC trimmed and ADC calibrated, excluding noise
Total Unadjusted Error	$E_{TUE\ CC}$	-12	-	12	LSB	$0V \leq V_{IN} \leq 5.5V$; HPBG, BACKUP OSC trimmed and ADC calibrated; excluding noise
		-8	-	8	LSB	$0V \leq V_{IN} \leq 3.63V$; HPBG, BACKUP OSC trimmed and ADC calibrated; excluding noise
RMS Noise	$EN_{RMS\ CC}$	-	2	3	LSB	HPBG, BACKUP OSC trimmed and ADC calibrated
Input charge consumption per conversion ¹⁾	$Q_{AIN\ CC}$	-	-	2.5	pC	$V_{ain} = V_{DDEVRSB} = 5.5\ V$

1) pad leakage current is not considered and has to be added to the ADC input current

4.20 Temperature sensor characteristics

The temperature monitoring of the TC49xN STD consists of:

- VTMON DTS
- PMS DTS

The VTMON DTS modules (VTMON.DTS[0:x]) are multiple on-chip temperature sensors at different locations across the microcontroller.

The PMS DTS is a temperature sensor dedicated for the PMS.

4.20.1 VTMON DTS characteristics

Table 98 VTMON DTS characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
DTS measurement time for each conversion	$t_M CC$	-	-	2	ms	Measured between consecutive conversions
Temperature difference between DTS instances excluding accuracy	$\Delta T CC$	-3	-	3	°C	Based on Real and Max pattern distribution and thermal simulations
Inherent DTS accuracy over temperature range	$T_{NL} CC$	-1	-	1	°C	Total accuracy is defined by T_{ACC} , the sum of T_{CALACC} and T_{NL}
Calibration reference accuracy	$T_{CALACC} CC$	-2	-	2	°C	Calibration points at $T_J = -40^{\circ}C$ and $T_J = 127^{\circ}C$
Total DTS accuracy after calibration and trimming	$T_{ACC} CC$	-3	-	3	°C	$T_{ACC} = T_{CALACC} + T_{NL}$; valid for all VTMON.DTS[0:x] instances
Extended Operating temperature range only for DTS	$T_{SR} SR$	-45	-	ABS T_J (Max)	°C	Junction temperature
Thermal runaway and shutdown monitoring range ^{1) 2)}	$T_{TSD} CC$	-	-	ABS T_J (Max)	°C	Alarm to SMU to trigger reset

- 1) The operating temperature range of the device is defined and limited by the operating temperature range definition within the chapter "Operating conditions". It is not allowed to operate the device in the thermal runaway and thermal shutdown range.
- 2) User has to ensure that the range is adapted according to the specified operating conditions valid for its application.

Related information

[PMS DTS characteristics](#) on page 524

4.20.2 PMS DTS characteristics

Table 99 PMS DTS characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
DTS measurement time for each conversion	$t_M CC$	-	-	2	ms	Measured between consecutive conversions
Inherent DTS accuracy over temperature range	$T_{NL} CC$	-1	-	1	°C	Total accuracy is defined by T_{ACC} , the sum of T_{CALACC} and T_{NL}
Calibration reference accuracy	$T_{CALACC} CC$	-2	-	2	°C	Calibration points at $T_J = -40^{\circ}\text{C}$ and $T_J = 127^{\circ}\text{C}$
Total DTS accuracy after calibration and trimming	$T_{ACC} CC$	-3	-	3	°C	$T_{ACC} = T_{CALACC} + T_{NL}$
Extended Operating temperature range only for DTS	$T_{SR} SR$	-45	-	165	°C	Junction temperature

Related information

[VTMON DTS characteristics](#) on page 523

4.21 Current consumption characteristics

The total power supply current defined here consists of leakage and switching components.

Application relevant values are typically lower than those given in the following tables and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

4.21.1 Definition of TC49xN application use cases

The power pattern definition for all functional blocks is described in this section.

Note: The use case of a functional block may not be applicable to both (STD and COM devices). For availability of a functional block, refer to features chapter.

Table 100 TC49xN application use cases

Functional block	Real0	Real1	Freerun one CPU
Supply Voltage, PMS	$VDDEXT = VDDEXTDC = VDDEXT(TYP)(5\text{ V}) + 2\%$ $VDD = VDD(TYP) + 2\%$ VDD Voltage Scaling active $VDDPHPHYx = VDDPHYx(TYP) + 2\%$ EVRC inactive	$VDDEXT = VDDEXTDC = VDDEXT(TYP)(5\text{ V}) + 2\%$ $VDD = VDD(TYP) + 2\%$ VDD Voltage Scaling active $VDDPHPHYx = VDDPHYx(TYP) + 2\%$ EVRC inactive	$VDDEXT = VDDEXTDC = VDDEXT(TYP)(5\text{ V}) + 2\%$ $VDD = VDD(TYP) + 2\%$ VDD Voltage Scaling active $VDDPHPHYx = VDDPHYx(TYP) + 2\%$ EVRC inactive
Temperature	$T_J = 160^\circ\text{C}$	$T_J = 160^\circ\text{C}$	$T_J = 160^\circ\text{C}$
Production Split	Respective Fast corner for SLOW and FAST splits	Respective Fast corner for SLOW and FAST splits	Respective Fast corner for SLOW and FAST splits
Integration time	20 ms	20 ms	20 ms
PACKAGE	STD	STD	STD
PORTS	minimal pattern activity	minimal pattern activity	minimal pattern activity
SMM	RUN1 mode	RUN1 mode	RUN1 mode
CLOCK	$XTAL = 25\text{ MHz}$ $f_{SYS\_PLL\_DCO} = 800\text{ MHz}$ $f_{PLL} = 400\text{ MHz}$	$XTAL = 25\text{ MHz}$ $f_{SYS\_PLL\_DCO} = 800\text{ MHz}$ $f_{PLL} = 400\text{ MHz}$	$XTAL = 25\text{ MHz}$ $f_{SYS\_PLL\_DCO} = 800\text{ MHz}$ $f_{PLL} = 400\text{ MHz}$
SRI, SPB/FPI, CPB	$f_{SRI}, f_{LLI}, f_{FSI2} = 400\text{ MHz},$ $f_{SPB}, f_{FSI} = 100\text{ MHz},$ $f_{CPB} = 200\text{ MHz}$	$f_{SRI}, f_{LLI}, f_{FSI2} = 400\text{ MHz},$ $f_{SPB}, f_{FSI} = 100\text{ MHz},$ $f_{CPB} = 200\text{ MHz}$	$f_{SRI}, f_{LLI}, f_{FSI2} = 400\text{ MHz},$ $f_{SPB}, f_{FSI} = 100\text{ MHz},$ $f_{CPB} = 200\text{ MHz}$
CPU0	CPU0 active at 400 MHz and executing power pattern	CPU0 active at 400 MHz and executing power pattern	CPU0 active at 400 MHz and executing power pattern
CPU1	CPU active @ 400 MHz executing 0.6 IPC realistic pattern with 80% activity	CPU active @ 400 MHz executing 0.6 IPC realistic pattern with 80% activity	CPU inactive

(table continues...)

Table 100 (continued) TC49xN application use cases

Functional block	Real0	Real1	Freerun one CPU
CPU2	CPU active @ 400 MHz executing 0.6 IPC realistic pattern with 80% activity	CPU active @ 400 MHz executing 0.6 IPC realistic pattern with 80% activity	CPU inactive
CPU3	CPU active @ 400 MHz executing 0.6 IPC realistic pattern with 80% activity	CPU active @ 400 MHz executing 0.6 IPC realistic pattern with 80% activity	CPU inactive
CPU4	CPU active @ 400 MHz executing 0.6 IPC realistic pattern with 80% activity	CPU active @ 400 MHz executing 0.6 IPC realistic pattern with 80% activity	CPU inactive
DMA0	DMA Real pattern	DMA Real pattern	inactive
DMA1	DMA Real pattern	DMA Real pattern	inactive
IR	enabled	enabled	inactive
LMU	LMU inactive	LMU inactive	switched off
NVM/R	Read activity from all Flash modules with 50% dutycycle. Periodic Data Flash write - Assumptions for the 2x data banks: 50% of the time in Read mode - Every 1ms write 128 B of data into each of the data banks - Rest of the time is Read-idle - Assumptions for the 2x program banks: 50% of the time in Read mode - Rest of the time is Read-idle	Read activity from all Flash modules with 50% dutycycle. Periodic Data Flash write - Assumptions for the 2x data banks: 50% of the time in Read mode - Every 1ms write 128 B of data into each of the data banks - Rest of the time is Read-idle - Assumptions for the 2x program banks: 50% of the time in Read mode - Rest of the time is Read-idle	inactive
CSRM	CSRM CPU @ 200 MHz and executing power pattern with 60% activity	CSRM CPU @ 200 MHz and executing power pattern with 60% activity	CPU inactive
CSS	ComSec ShortFrames usecase. CAN data encryption/ decryption $f_{CSS} = f_{SRI} = 400$ MHz	ComSec ShortFrames usecase. CAN data encryption/ decryption $f_{CSS} = f_{SRI} = 400$ MHz	inactive
PPU	PPU switched off	PPU (256b) at 400 MHz. PPU real pattern	switched off

(table continues...)

Table 100 (continued) TC49xN application use cases

Functional block	Real0	Real1	Freerun one CPU
HSPHY	inactive	inactive	inactive
HSSL	inactive	inactive	inactive
xSPI	inactive	inactive	inactive
DRE	inactive	inactive	inactive
SDMMC	inactive	inactive	inactive
CAN	2 modules active fCAN = 160 MHz	2 modules active fCAN = 160 MHz	inactive
CAN XL	inactive	inactive	inactive
ERAY	ERAY0 CH0 active	ERAY0 CH0 active	inactive
LETH	2x LETH channels active 1*100Mbps (MII) on LETH1 1*100Mbps (MII) on LETH0 fLETH = fSRI/4	3x LETH channels active 1*100Mbps (MII) on LETH1 2*100Mbps (MII) on LETH0 fLETH = fSRI/4	inactive
ASCLIN	6 modules active fASCLINF/S = 200/160 MHz	6 modules active fASCLINF/S = 200/160 MHz	inactive
SENT	2 modules with 30 channels active	2 modules with 30 channels active	inactive
PSI5	inactive	inactive	inactive
PSI5S	inactive	inactive	inactive
MSC	3 modules active	3 modules active	inactive
QSPI	6 modules active fQSPI = 200 MHz	6 modules active fQSPI = 200 MHz	inactive
I2C	2 modules active fI2C = 66.6 MHz	2 modules active fI2C = 66.6 MHz	inactive
VTMON	All DTS instances active	All DTS instances active	inactive
Logic TEST	inactive	inactive	inactive
VMT	inactive	inactive	inactive
SCR	inactive	inactive	inactive
PMS, SCU	default reset state	default reset state	default reset state
WTU	Respective CPU units active	Respective CPU units active	Respective CPU units active
SMU	SMU_SAFE0 and SMU_CS - Enabled	SMU_SAFE0 and SMU_CS - Enabled	SMU_SAFE0 and SMU_CS - Enabled
FCE	default reset state	default reset state	default reset state

(table continues...)

Table 100 (continued) TC49xN application use cases

Functional block	Real0	Real1	Freerun one CPU
GTM	3 clusters at 200 MHz. Rest at 100 MHz. 6TIM+6TOM+7ATOM+14DTM +DPLL+2SPE+ 2PSM+ 5MCS active	3 clusters at 200 MHz. Rest at 100 MHz. 6TIM+6TOM+7ATOM+14DTM +DPLL+2SPE+ 2PSM+ 5MCS active	inactive
eGTM	2TIM + 2TOM+3ATOM active at 400 MHz	2TIM + 2TOM+3ATOM active at 400 MHz	inactive
GST	not available	not available	not available
HRPWM	inactive	inactive	inactive
GPT12	All modules active	All modules active	inactive
ADC.TMADC	5 ADCs active fTMADC = 160 MHz	5 ADCs active fTMADC = 160 MHz	inactive
ADC.DSADC	6 ADCs active 4 DSADC are used with 4 CDSP 2 remaining DSADC run w/o CDSP	6 ADCs active 4 DSADC are used with 4 CDSP 2 remaining DSADC run w/o CDSP	inactive
ADC.FCC	6 ADCs active	6 ADCs active	inactive
ADC.CDSP	8 CDSPs active fCDSP = 160 MHz	8 CDSPs active fCDSP = 160 MHz	inactive
DEBUG	inactive	inactive	inactive
SGBT, TRACE	inactive	inactive	inactive

Note: Modules which are inactive are clock-gated by setting respective module clock control register CLC.DISS = 0x1.

Related information

[Current consumption and power dissipation overview in RUN mode](#) on page 529

[Respective supply rail currents in RUN mode](#) on page 530

[Current consumption in SLEEP and STANDBY modes](#) on page 531

[Load Transients](#) on page 533

4.21.2 Current consumption and power dissipation overview in RUN mode

Table 101 Current consumption and power dissipation overview in RUN mode

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Sum of all currents with DC-DC EVRC regulator active	$I_{DDTOTDC\ CC}$	-	-	900 ¹⁾	mA	Real0 power pattern; $T_J = T_J$ (Max); $V_{DDEXTDC} = 5V$; V_{DDEXT} (Typ) + 2%; $V_{DDEXTHS}$ (Typ) + 2%; V_{DDM} (Typ) + 2%; $V_{DDEVRSB}$ (Typ) + 2%; V_{DDFLEX} (Typ) + 2%; V_{DD} (Typ) + 2%
		-	-	1000 ¹⁾	mA	Real1 power pattern; $T_J = T_J$ (Max); $V_{DDEXTDC} = 5V$; V_{DDEXT} (Typ) + 2%; $V_{DDEXTHS}$ (Typ) + 2%; V_{DDM} (Typ) + 2%; $V_{DDEVRSB}$ (Typ) + 2%; V_{DDFLEX} (Typ) + 2%; V_{DD} (Typ) + 2%
Maximum power dissipation	$PD\ SR$	-	-	3700	mW	Real0 power pattern; $T_J = T_J$ (Max); $V_{DDEXTDC} = 5V$; V_{DDEXT} (Typ) + 2%; $V_{DDEXTHS}$ (Typ) + 2%; V_{DDM} (Typ) + 2%; $V_{DDEVRSB}$ (Typ) + 2%; V_{DDFLEX} (Typ) + 2%; V_{DD} (Typ) + 2%
		-	-	4150	mW	Real1 power pattern; $T_J = T_J$ (Max); $V_{DDEXTDC} = 5V$; V_{DDEXT} (Typ) + 2%; $V_{DDEXTHS}$ (Typ) + 2%; V_{DDM} (Typ) + 2%; $V_{DDEVRSB}$ (Typ) + 2%; V_{DDFLEX} (Typ) + 2%; V_{DD} (Typ) + 2%

1) $I_{DDTOTDC} = I_{DCNL} (EVRC) (Max) + I_{DDEXT} (Max) + I_{DDEXTHS} (Max) + I_{DDM} (Max) + I_{DDEVRSB} (Max) + I_{DDFLEX} (Max) + [(I_{DD} (Max) * V_{DD}) / (V_{DDEXTDC} * 72\% \text{ Efficiency})]$

Related information

[Definition of TC49xN application use cases](#) on page 525

[Respective supply rail currents in RUN mode](#) on page 530

[Current consumption in SLEEP and STANDBY modes](#) on page 531

[Load Transients](#) on page 533

4.21.3 Respective supply rail currents in RUN mode

Table 102 Respective supply rail currents in RUN mode

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VDD supply rail currents						
Sum of I_{DD} core supply currents (incl. $I_{DD\_LEAK} + I_{DD\_DYN}$)	$I_{DD} CC$	-	-	3000	mA	Freerun power pattern with CPU0 (@max IPC) active; $T_J = T_J$ (Max); V_{DD} (Typ) + 2%
		-	-	3055	mA	Real0 power pattern; $T_J = T_J$ (Max); V_{DD} (Typ) + 2%
		-	-	3465	mA	Real1 power pattern; $T_J = T_J$ (Max); V_{DD} (Typ) + 2%
VDDEVRSB supply rail currents						
$I_{DDEVRSB}$ supply current (incl. leakage)	$I_{DDEVRSB} CC$	-	-	30	mA	Freerun power pattern; $T_J = T_J$ (Max); $V_{DDEVRSB}$ (Typ) + 2%
		-	-	30	mA	Real0/1 power pattern with SCR; $T_J = T_J$ (Max); $V_{DDEVRSB}$ (Typ) + 2%
		-	-	25	mA	Real0/1 power pattern without SCR; $T_J = T_J$ (Max); $V_{DDEVRSB}$ (Typ) + 2%
VDDEXT/VDDEXTHS supply rail currents						
$I_{DDEXT} / I_{DDEXTHS}$ supply current (incl. leakage and $I_{IEXTLVDS}$) ¹⁾	$I_{DDEXT} CC$	-	-	50	mA	Real0/1 power pattern; $T_J = T_J$ (Max); V_{DDEXT} (Typ) + 2%; $V_{DDEXTHS}$ (Typ) + 2%
VDDFLEX / VDDHSIF (if applicable) supply rail currents						
I_{DDFLEX} supply current (incl. leakage)	$I_{DDFLEX} CC$	-	-	4	mA	Real0/1 power pattern; $T_J = T_J$ (Max); V_{DDFLEX} (Typ) + 2%
VDDM supply rail currents						
I_{DDM} supply current (incl. leakage)	$I_{DDM} CC$	-	-	50	mA	Real0/1 power pattern; $T_J = T_J$ (Max); V_{DDM} (Typ) + 2%
VDDPPHYx supply rail currents						
$I_{DDPPHYx}$ supply current (incl. leakage)	$I_{DDPPHYx} CC$	-	-	3	mA	Freerun power pattern; $T_J = T_J$ (Max); V_{DDPPHY} (Typ) + 2%; HSPHY disabled
VDDPHYx supply rail currents						
I_{DDPHYx} supply current (incl. $I_{DDPHYx\_LEAK} + I_{DDPHYx\_DYN}$)	$I_{DDPHYx} CC$	-	-	60	mA	Freerun power pattern; $T_J = T_J$ (Max); V_{DDPHY} (Typ) + 2%
VDDSB supply rail currents						
I_{DDSB} core current (incl. leakage)	$I_{DDSB} CC$	-	-	2 ²⁾	mA	Freerun power pattern with CPU0 active; $T_J = T_J$ (Max); V_{DDSB} (Typ) + 2%

1) Maximum current drawn by clock functions on VDDEXTOSC rail is less than 15 mA. VDDEXT and VDDEXTOSC supply rails shall be supplied from the same regulator source as there are parasitic injection paths between the supply rails and the voltage difference shall be less than

4 Electrical characteristics

100 mV. Resistances on the VDDEXTOSC path, if required, shall be dimensioned small enough to have sufficient margins to primary and secondary undervoltage monitor limits.

- 2) Once cold PORST is released, and the device is in RUN mode, the LMU standby memory supply is switched from VDDSB rail to VDD rail by an internal switch.

Related information

[Definition of TC49xN application use cases](#) on page 525

[Current consumption and power dissipation overview in RUN mode](#) on page 529

[Current consumption in SLEEP and STANDBY modes](#) on page 531

[Load Transients](#) on page 533

4.21.4 Current consumption in SLEEP and STANDBY modes

Table 103 Current consumption in SLEEP and STANDBY modes

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SLEEP mode current consumption						
Σ Sum of all IDD core supply currents in SLEEP mode	$I_{\text{SLEEP CC}}$	10	-	85	mA	All CPUs in idle; All peripherals in SLEEP mode; $f_{\text{SRI/SPB}} = 1$ MHz via LPDIV divider; SCR inactive; $T_J = 25^{\circ}\text{C}$; $V_{\text{DDEXTDC}} = 5\text{ V}$; V_{DDEXT} (Typ) + 2%; V_{DDEXTHS} (Typ) + 2%; V_{DDM} (Typ) + 2%; V_{DDEVRSB} (Typ) + 2%; $V_{\text{DD}} = 0.9\text{ V}$.
Σ Sum of all currents in STANDBY0 mode drawn at VDDEVRSB, VDDEXT, VDDEXTHS, VDDM, VAREF and VDDEXTDC rail ¹⁾	$I_{\text{STANDBY2 CC}}$	-	80	100	μA	16kB Standby RAM (CPU0 dLMU) supplied; 32kB SCR RAM not supplied; $T_J = 25^{\circ}\text{C}$; $f_{\text{SCR}} = 70\text{ kHz}$; All rails VDDEVRSB, VDDEXT, VDDEXTHS, VDDM, VAREF and VDDEXTDC rails are supplied with V_{DDEVRSB} (Typ) + 2%.
STANDBY0 mode current consumption without memory retention						
VDDPMS0 Standby domain current in STANDBY0 mode at VDDEVRSB rail	$I_{\text{STBYPMS0 CC}}$	-	35	-	uA	Standby RAM (dLMU) not supplied; 32kB SCR XRAM not supplied; $f_{\text{SCR}} = 70\text{ kHz}$; $T_J = 25^{\circ}\text{C}$; V_{DDEVRSB} (Typ) + 2%; $V_{\text{DDPMS0}} + 4\%$;
STANDBY0 current consumption with memory retention (dLMU)						
VDDPMS0 Standby domain current in STANDBY0 mode at VDDEVRSB rail	$I_{\text{STBYPMS0 CC}}$	-	40	-	μA	16kB Standby RAM (CPU0 dLMU) supplied; 32kB SCR XRAM not supplied; $f_{\text{SCR}} = 70\text{ kHz}$; $T_J = 25^{\circ}\text{C}$; V_{DDEVRSB} (Typ) + 2%; $V_{\text{DDPMS0}} + 4\%$

(table continues...)

Table 103 (continued) **Current consumption in SLEEP and STANDBY modes**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
STANDBY1 mode current consumption						
VDDPMS1 Standby domain current in STANDBY1 mode at VDDEVRSB rail	$I_{STBYPMS1\ CC}$	-	215	-	μA	Standby RAM (dLMU) not supplied; SCR active; $f_{SCR} = 70$ kHz; $T_J = 25^{\circ}\text{C}$; $V_{DDEVRSB}$ (Typ) + 2%
		-	3.7	-	mA	Standby RAM (dLMU) not supplied; SCR active; $f_{SCR} = 1.25$ MHz; $T_J = 25^{\circ}\text{C}$; $V_{DDEVRSB}$ (Typ) + 2%; $dl_{SCR}/dt < \pm 500$ uA
		-	7.8	-	mA	Standby RAM (dLMU) not supplied; SCR active; $f_{SCR} = 20$ MHz; $T_J = 85^{\circ}\text{C}$; $V_{DDEVRSB}$ (Typ) + 2%; HPOSC and ADCOMP active; $dl_{SCR}/dt < \pm 1$ mA
		-	12.8	-	mA	Standby RAM (dLMU) not supplied; SCR active; $f_{SCR} = 100$ MHz; $T_J = 150^{\circ}\text{C}$; $V_{DDEVRSB}$ (Typ) + 2%; HPOSC and ADCOMP active; $dl_{SCR}/dt < \pm 3$ mA
STANDBY current consumption with memory retention (LMU) for calibration support						
VDDSB Standby domain current	$I_{STBYLMU\ CC}$	-	-	120 ²⁾	mA	LMU RAM kept supplied during Standby; $T_J = T_J$ (Max); V_{DDBSB} (Typ) + 10%

1) During measurements, the pins available in the voltage domain VDDEVRSB, VDDEXT and VDDM are left open

2) The current consumption value is based on pre-silicon simulation and has not been characterized.

Related information

[Definition of TC49xN application use cases on page 525](#)

[Current consumption and power dissipation overview in RUN mode on page 529](#)

[Respective supply rail currents in RUN mode on page 530](#)

[Load Transients on page 533](#)

4.21.5 Load Transients

Table 104 Load Transients

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
IDD core dynamic current load jump during LBIST	$dI_{DD\text{DYN\_LBIST}} CC$	-300	-	600	mA	Key-on LBIST; $t_r = 20 \mu s$; $t_f = 15 \mu s$; $T_{DWELL} > 20 \mu s$; external regulator untrimmed; EVRC bandgap and clock trimmed but operated with default coefficients; V_{DD} (Typ) - 5%
		-600	-	800	mA	Key-off LBIST; $t_r = 50 \mu s$; $t_f = 20 \mu s$; $T_{DWELL} > 20 \mu s$; external regulator untrimmed; EVRC bandgap and clock trimmed but operated with default coefficients; V_{DD} (Typ) - 3%
IDD core dynamic current load jump by MBIST	$dI_{DD\text{DYN\_VMT}} CC$	-330	-	330	mA	$t_{MBIST} < 6ms$. VMT Ganging procedure for SRAM test and initialization (definition refer to VMT chapter in User Manual); V_{DD} (Typ) - 3%
IDD core dynamic current load jump during start-up (e.g.: Supply ramp-up, Clock ramp-up, Firmware execution, Processor unit activation, PORST deassertion)	$dI_{DD\text{DYN\_STRT}} CC$	-250	-	250	mA	$t_r = 0.02 \mu s$; $t_f = 0.02 \mu s$; $T_{DWELL} = 100 \mu s$; regulator untrimmed; V_{DD} (Typ) - 3%

Related information

[Definition of TC49xN application use cases](#) on page 525

[Current consumption and power dissipation overview in RUN mode](#) on page 529

[Respective supply rail currents in RUN mode](#) on page 530

[Current consumption in SLEEP and STANDBY modes](#) on page 531

4.22 AC characteristics

All AC parameters are specified for the complete operating range defined in [Chapter 4.4](#) unless otherwise noted. Unless otherwise noted, the timings are defined with the following guidelines:

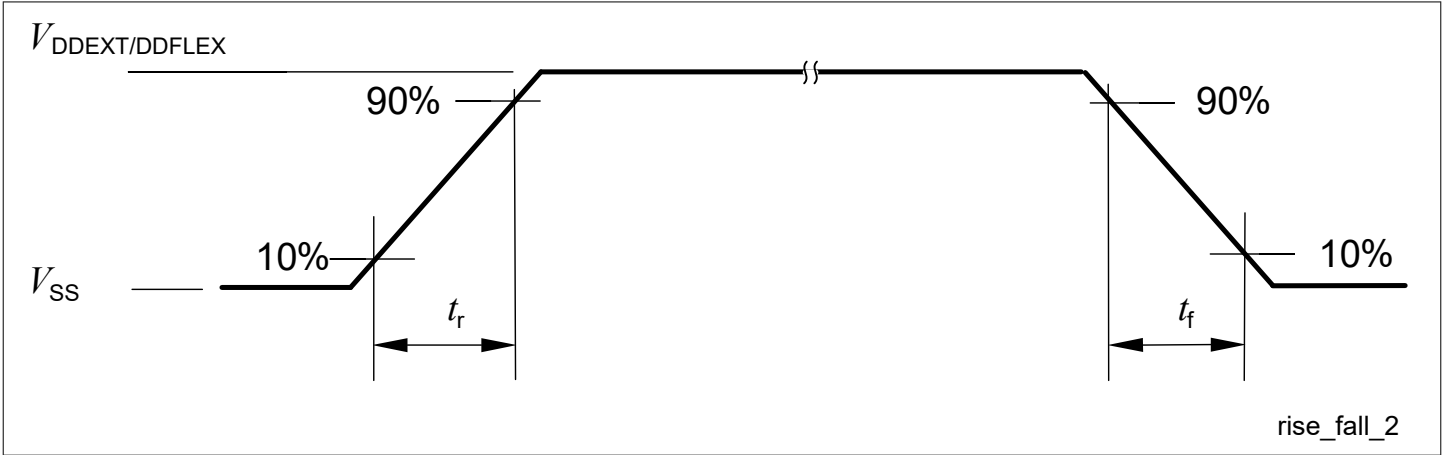


Figure 9 Definition of rise and fall times

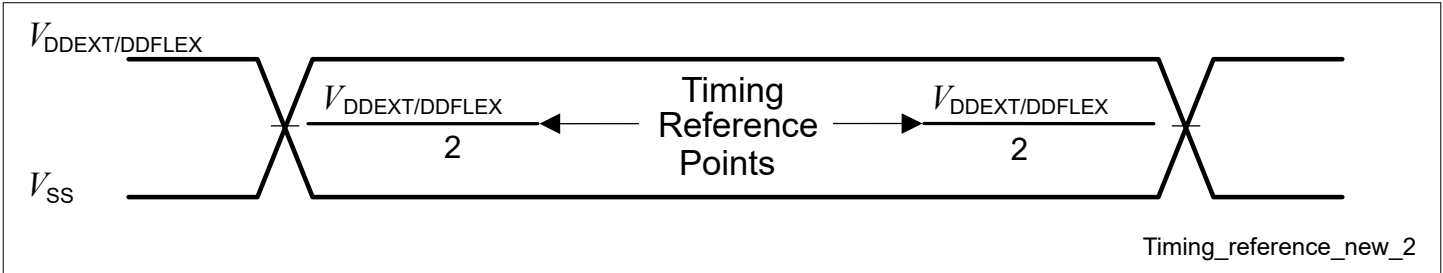


Figure 10 Time Reference Point Definition

4.23 ASCLIN SPI Master timing characteristics

This section defines the timing characteristics for the ASCLIN module in the TC49xN STD. The specified timing values are split in two sets:

- Speed graded signals with extension _F
- Signals belonging to a defined set of ports grouped to a segment:

Table 105 Segment definition

Segment	Ports	Module
0	Port01, Port02, Port10, Port11	ASCLIN2
1	Port12, Port13, Port14	ASCLIN0, ASCLIN7
2	Port30, Port32, Port33, Port34, Port35	ASCLIN5
3	Port21, Port22, Port23	ASCLIN4, ASCLIN6
4	Port15, Port20	ASCLIN1, ASCLIN3

4.23.1 ASCLIN Master Mode timing for strong sharp (ss) output pads

Table 106 ASCLIN Master Mode timing for strong sharp (ss) output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ASCLKO clock period	$t_{50\ SR}$	20	-	-	ns	$C_L = 25\text{ pF}$
Deviation from ideal duty cycle	$t_{500\ CC}$	-2	-	2	ns	$C_L = 25\text{ pF}$; valid for identical pad types of category Fast (signals mapped to those pads are marked with suffix _F) and mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = sharp or signals mapped to port slices within a segment
MTSR delay from ASCLKO shifting edge	$t_{51\ CC}$	-4	-	4	ns	$C_L = 25\text{ pF}$; valid for identical pad types of category Fast with identical configuration driver = strong, edge = sharp. Signals mapped to those pads are marked with suffix _F
		-4.0	-	5.5	ns	$C_L = 25\text{ pF}$; valid for mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = sharp or signals mapped to port slices within a segment
		-8	-	8	ns	$C_L = 25\text{ pF}$; else

(table continues...)

Table 106 (continued) ASCLIN Master Mode timing for strong sharp (ss) output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ASLSON delay from the first ASCLKO edge	$t_{510\ CC}$	-3.5	-	3.5	ns	$C_L = 25\text{ pF}$; valid for identical pad types of category Fast with identical configuration driver = strong, edge = sharp. Signals mapped to those pads are marked with suffix _F
		-4.0	-	3.5	ns	$C_L = 25\text{ pF}$; valid for mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = sharp or signals mapped to port slices within a segment
		-7	-	7	ns	$C_L = 25\text{ pF}$; else
MRST setup to ASCLKO latching edge	$t_{52\ SR}$	25	-	-	ns	$C_L = 25\text{ pF}$; valid for identical pad types of category Fast (signals mapped to those pads are marked with suffix _F) and mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = sharp or signals mapped to port slices within a segment
		29	-	-	ns	$C_L = 25\text{ pF}$; else
MRST hold from ASCLKO latching edge	$t_{53\ SR}$	-2	-	-	ns	$C_L = 25\text{ pF}$; valid for mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = sharp or signals mapped to port slices within a segment
		-2	-	-	ns	$C_L = 25\text{ pF}$; else

4.23.2 ASCLIN Master Mode timing for strong medium (sm) output pads

Table 107 ASCLIN Master Mode timing for strong medium (sm) output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ASCLKO clock period	$t_{50\ SR}$	50	-	-	ns	$C_L = 50\text{ pF}$
Deviation from ideal duty cycle	$t_{500\ CC}$	-5	-	5	ns	$C_L = 50\text{ pF}$

(table continues...)

Table 107 (continued) ASCLIN Master Mode timing for strong medium (sm) output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
MTSR delay from ASCLKO shifting edge	$t_{51\ CC}$	-7	-	7	ns	$C_L = 50\text{ pF}$; valid for identical pad types (signals mapped to those pads are marked with suffix _F) and mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = medium or signals mapped to port slices within a segment
		-10	-	10	ns	$C_L = 50\text{ pF}$; else
ASLSON delay from the first ASCLKO edge	$t_{510\ CC}$	-7	-	7	ns	$C_L = 50\text{ pF}$; valid for identical pad types (signals mapped to those pads are marked with suffix _F) and mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = medium or signals mapped to port slices within a segment
		-10	-	10	ns	$C_L = 50\text{ pF}$; else
MRST setup to ASCLKO latching edge	$t_{52\ SR}$	35	-	-	ns	$C_L = 50\text{ pF}$; valid for identical pad types (signals mapped to those pads are marked with suffix _F) and mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = medium or signals mapped to port slices within a segment
		36	-	-	ns	$C_L = 50\text{ pF}$; else
MRST hold from ASCLKO latching edge	$t_{53\ SR}$	-5	-	-	ns	$C_L = 50\text{ pF}$

4.23.3 ASCLIN Master Mode timing for medium (m) output pads

Table 108 ASCLIN Master Mode timing for medium (m) output pads

Note: The following timing parameters are valid for all mappings of the ASCLIN module.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ASCLKO clock period	$t_{50\ SR}$	160	-	-	ns	$C_L = 50\text{ pF}$
Deviation from ideal duty cycle	$t_{500\ CC}$	-10	-	10	ns	$C_L = 50\text{ pF}$

(table continues...)

Table 108 (continued) **ASCLIN Master Mode timing for medium (m) output pads**

Note: The following timing parameters are valid for all mappings of the ASCLIN module.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
MTSR delay from ASCLKO shifting edge	t_{51} CC	-20	-	20	ns	$C_L = 50$ pF
ASLSON delay from the first ASCLKO edge	t_{510} CC	-20	-	20	ns	$C_L = 50$ pF
MRST setup to ASCLKO latching edge	t_{52} SR	80	-	-	ns	$C_L = 50$ pF
MRST hold from ASCLKO latching edge	t_{53} SR	-12	-	-	ns	$C_L = 50$ pF

4.23.4 ASCLIN SPI Master timing figures

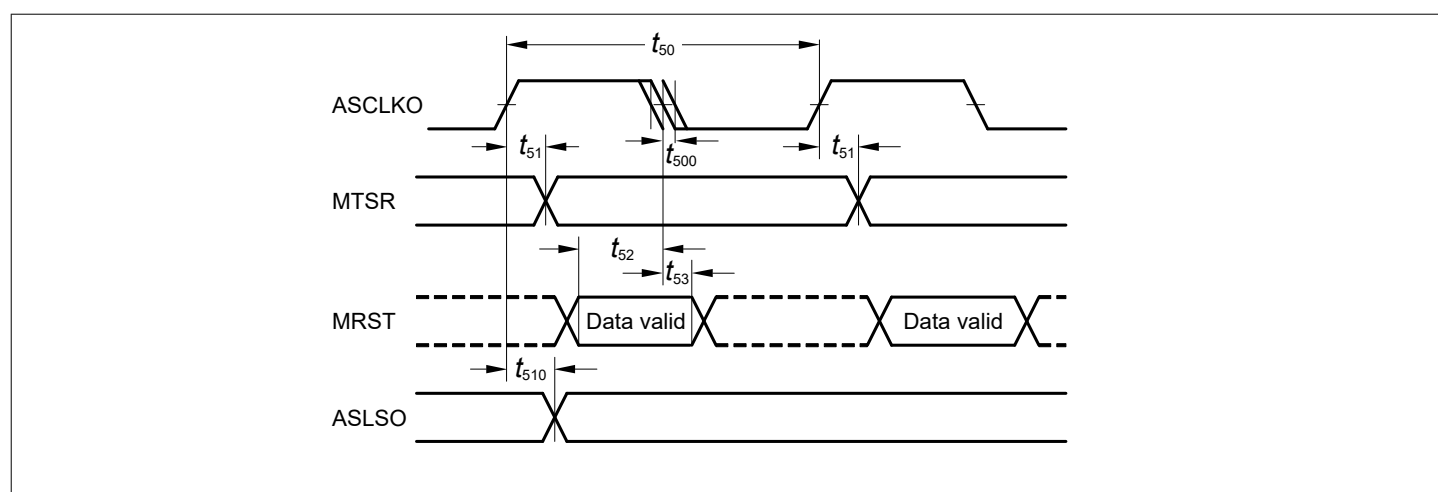


Figure 11 ASCLIN SPI Master Timing

4.24 Inter-IC (I2C) interface timing characteristics

The I2C module of the TC49xN STD supports following operating modes:

- Standard mode for speeds up to 100 kbits/s
- Fast mode for speeds up to 400 kbits/s
- High Speed mode for speeds up to 3.4 Mbits/s

Note: All I2C timing values are SR for Master Mode and CC for Slave Mode.

4.24.1 I2C standard mode timing

Table 109 I2C standard mode timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1	-	-	300	ns	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Capacitive load for each bus line	C_b SR	-	-	400	pF	
Bus free time between a STOP and START condition	t_{10}	4.7	-	-	μs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Rise time of both SDA and SCL	t_2	-	-	1000	ns	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Data hold time	t_3	0	-	-	μs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Data set-up time	t_4	250	-	-	ns	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Low period of SCL clock	t_5	4.7	-	-	μs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
High period of SCL clock	t_6	4	-	-	μs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Hold time for the (repeated) START condition	t_7	4	-	-	μs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Set-up time for (repeated) START condition	t_8	4.7	-	-	μs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line

(table continues...)

Table 109 (continued) I2C standard mode timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Set-up time for STOP condition	t_9	4	-	-	μs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line

Related information

[I2C fast mode timing](#) on page 540

[I2C high speed mode timing](#) on page 541

[I2C standard and fast mode timing figures](#) on page 542

4.24.2 I2C fast mode timing

Table 110 I2C fast mode timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1	20+0.1* C_b	-	300	ns	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Capacitive load for each bus line	C_b SR	-	-	400	pF	
Bus free time between a STOP and START condition	t_{10}	1.3	-	-	μs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Rise time of both SDA and SCL	t_2	20+0.1* C_b	-	300	ns	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Data hold time	t_3	0	-	-	μs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Data set-up time	t_4	100	-	-	ns	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Low period of SCL clock	t_5	1.3	-	-	μs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
High period of SCL clock	t_6	0.6	-	-	μs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Hold time for the (repeated) START condition	t_7	0.6	-	-	μs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line

(table continues...)

Table 110 (continued) I2C fast mode timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Set-up time for (repeated) START condition	t_8	0.6	-	-	μs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line
Set-up time for STOP condition	t_9	0.6	-	-	μs	Measured with a pull-up resistor of 4.7 kOhm at each of the SCL and SDA line

Related information

[I2C standard mode timing](#) on page 539

[I2C high speed mode timing](#) on page 541

[I2C standard and fast mode timing figures](#) on page 542

4.24.3 I2C high speed mode timing

Table 111 I2C high speed mode timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Capacitive load for each bus line	C_b SR	-	-	400	pF	
Fall time of SCL	t_{11}	10 ¹⁾	-	40 ¹⁾	ns	Bus line load C_b = 100 pF
Fall time of SDA	t_{12}	10 ¹⁾	-	80 ¹⁾	ns	Bus line load C_b = 100 pF
Rise time of SCL	t_{13}	10 ¹⁾	-	40 ¹⁾	ns	Bus line load C_b = 100 pF
Rise time of SDA	t_{14}	10 ¹⁾	-	80 ¹⁾	ns	Bus line load C_b = 100 pF
Data hold time	t_3	0 ¹⁾	-	70 ¹⁾	ns	Bus line load C_b = 100 pF
Data set-up time	t_4	10 ¹⁾	-	-	ns	Bus line load C_b = 100 pF
Low period of SCL clock	t_5	160 ¹⁾	-	-	ns	Bus line load C_b = 100 pF
High period of SCL clock	t_6	60 ¹⁾	-	-	ns	Bus line load C_b = 100 pF
Hold time for the (repeated) START condition	t_7	160 ¹⁾	-	-	ns	Bus line load C_b = 100 pF
Set-up time for (repeated) START condition	t_8	160 ¹⁾	-	-	ns	Bus line load C_b = 100 pF
Set-up time for STOP condition	t_9	160 ¹⁾	-	-	ns	Bus line load C_b = 100 pF

1) Values are defined for C_b = 100 pF, for the Timing of C_b = 400 pF see the I2C Standard.

Related information

[I2C standard mode timing](#) on page 539

[I2C fast mode timing](#) on page 540

[I2C standard and fast mode timing figures](#) on page 542

4.24.4 I2C standard and fast mode timing figures

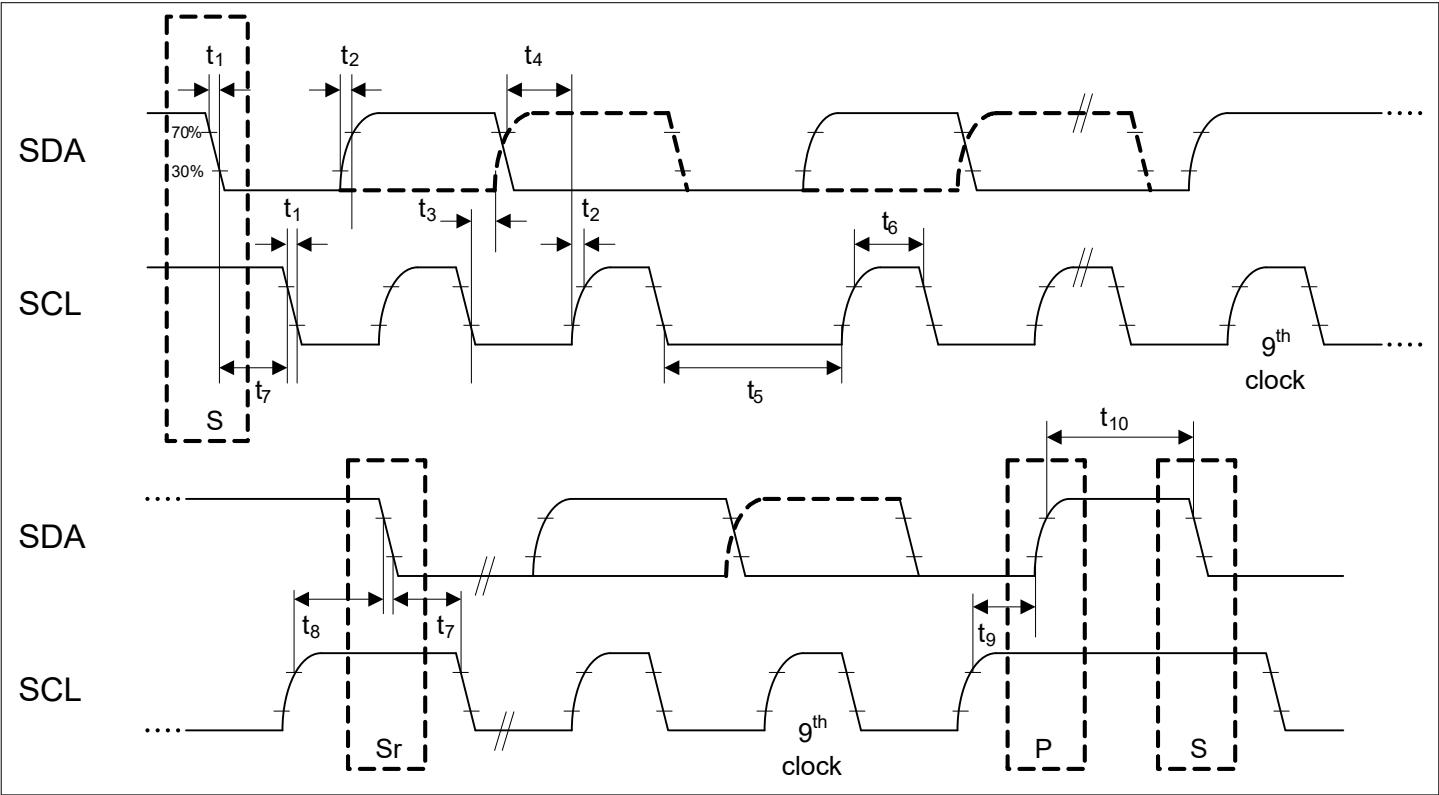


Figure 12 I2C standard and fast mode timing

Related information

[I2C standard mode timing](#) on page 539

[I2C fast mode timing](#) on page 540

[I2C high speed mode timing](#) on page 541

4.25 CAN characteristics

4.25.1 CAN internal receive delay for all pads

Table 112 CAN internal receive delay for all pads

The RX delay is the time measured from pad input to input of the CAN RXD input buffer

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
RX delay	$t_{\text{RXD CC}}$	-	-	$15 + (2 \cdot (1/f_{\text{MCAN}}))$	ns	

4.25.2 CAN internal transmit delay for strong sharp (ss) output pads

Table 113 CAN internal transmit delay for strong sharp (ss) output pads

The TXD delay is the time measured from CAN TXD output buffer to the pad output with the defined load

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TXD delay	$t_{\text{intern\_TXD}}$ CC	-	-	16	ns	Fast 5V GPIO - driver = strong edge = sharp; $C_L \leq 10$ pF
		-	-	17	ns	Fast 5V GPIO - driver = strong edge = sharp; $C_L \leq 20$ pF
		-	-	18	ns	Fast 3.3V GPIO - driver = strong edge = sharp; $C_L \leq 10$ pF
		-	-	19.	ns	Fast 3.3V GPIO - driver = strong edge = sharp; $C_L \leq 20$ pF

4.25.3 CAN internal transmit delay for medium (m) output pads

Table 114 CAN internal transmit delay for medium (m) output pads

The TXD delay is the time measured from CAN TXD output buffer to the pad output with the defined load

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TXD delay	$t_{\text{intern\_TXD}}$ CC	-	-	19.5	ns	Fast / Slow 5V GPIO - driver = medium edge = medium; $C_L \leq 10$ pF
		-	-	24.5	ns	Fast / Slow 5V GPIO - driver = medium edge = medium; $C_L \leq 20$ pF
		-	-	23	ns	Fast / Slow 3.3V GPIO - driver = medium edge = medium; $C_L \leq 10$ pF
		-	-	28	ns	Fast / Slow 3.3V GPIO - driver = medium edge = medium; $C_L \leq 20$ pF

4.25.4 CAN internal transmit delay for strong medium (sm) output pads

Table 115 CAN internal transmit delay for strong medium (sm) output pads

The TXD delay is the time measured from CAN TXD output buffer to the pad output with the defined load

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TXD delay	$t_{\text{intern\_TXD}}^{CC}$	-	-	19.75	ns	Fast / Slow 5V GPIO - driver = strong edge = medium; $C_L \leq 10$ pF
		-	-	21.00	ns	Fast / Slow 5V GPIO - driver = strong edge = medium; $C_L \leq 20$ pF
		-	-	21.5	ns	Fast / Slow 3.3V GPIO - driver = strong edge = medium; $C_L \leq 10$ pF
		-	-	24.00	ns	Fast / Slow 3.3V GPIO - driver = strong edge = medium; $C_L \leq 20$ pF

4.26 CAN XL characteristics

4.26.1 CANXL internal receive delay for all pads

Table 116 CANXL internal receive delay for all pads

The RX delay is the time measured from pad input to input of the CANXL RXD input buffer

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
RX delay	t_{RXD}^{CC}	-	-	$15 + (2 * (1 / f_{\text{CANXL}}))$	ns	

4.26.2 CANXL internal transmit delay for strong sharp (ss) output pads

Table 117 CANXL internal transmit delay for strong sharp (ss) output pads

The TXD delay is the time measured from CANXL TXD output buffer to the pad output with the defined load

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TXD delay	$t_{\text{intern\_TXD}}^{CC}$	-	-	16.10	ns	Fast 5V GPIO - driver = strong edge = sharp; $C_L \leq 10$ pF
		-	-	17	ns	Fast 5V GPIO - driver = strong edge = sharp; $C_L \leq 20$ pF
		-	-	16.5	ns	Fast 3.3V GPIO - driver = strong edge = sharp; $C_L \leq 10$ pF
		-	-	17.5	ns	Fast 3.3V GPIO - driver = strong edge = sharp; $C_L \leq 20$ pF

4.26.3 CANXL internal transmit delay for medium (m) output pads

Table 118 CANXL internal transmit delay for medium (m) output pads

The TXD delay is the time measured from CANXL TXD output buffer to the pad output with the defined load

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TXD delay	$t_{\text{intern\_TXD}}^{CC}$	-	-	19	ns	Fast / Slow 5V GPIO - driver = medium edge = medium; $C_L \leq 10$ pF
		-	-	24	ns	Fast / Slow 5V GPIO - driver = medium edge = medium; $C_L \leq 20$ pF
		-	-	22.5	ns	Fast / Slow 3.3V GPIO - driver = medium edge = medium; $C_L \leq 10$ pF
		-	-	27	ns	Fast / Slow 3.3V GPIO - driver = medium edge = medium; $C_L \leq 20$ pF

4.26.4 CANXL internal transmit delay for strong medium (sm) output pads

Table 119 CANXL internal transmit delay for strong medium (sm) output pads

The TXD delay is the time measured from CANXL TXD output buffer to the pad output with the defined load

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TXD delay	$t_{\text{intern\_TXD}}^{CC}$	-	-	18	ns	Fast / Slow 5V GPIO - driver = strong edge = medium; $C_L \leq 10$ pF
		-	-	20	ns	Fast / Slow 5V GPIO - driver = strong edge = medium; $C_L \leq 20$ pF
		-	-	19	ns	Fast / Slow 3.3V GPIO - driver = strong edge = medium; $C_L \leq 10$ pF
		-	-	22	ns	Fast / Slow 3.3V GPIO - driver = strong edge = medium; $C_L \leq 20$ pF

4.27 MSC 5V timing characteristics

The following sub-chapters include the 5V timing characteristics of the Microsecond Channel (MSC) module. For the specified timing values it is assumed that FCLPx, SOPx, and ENx pads have the same pad settings.

The below listed tables contain the clock period T_A . $T_A = 1/f_A$ where f_A is the input clock frequency of the MSC ABRA block (see also User Manual Chapter MSC).

In case the MSC ABRA block is bypassed T_A is defined as $T_A = 1/f_{\text{MSC}}$ where f_{MSC} is the input clock frequency without ABRA block up to 50 MHz (see User Manual Chapter MSC Baud rate configuration).

Note: Pad asymmetry (defined by parameter t_{TX_ASYM}) is already included in the timing characteristics that follow.

Note: The following timing characteristics are only valid for MSC modules 0, 2 and 3.

4.27.1 MSC clock/data timing for strong sharp (ss) 5V output pads

Table 120 MSC clock/data timing for strong sharp (ss) 5V output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
FCLPx clock period	$t_{40} CC$	$2 * T_A$	-	-	ns	$C_L = 50 \text{ pF}$
Deviation from ideal duty cycle	$t_{400} CC$	-2.5	-	2	ns	$C_L = 50 \text{ pF}$
SOPx output delay	$t_{44} CC$	-5.0	-	4.0	ns	$C_L = 50 \text{ pF}$
ENx output delay	$t_{45} CC$	-6.0	-	5.0	ns	$C_L = 50 \text{ pF}$

Related information

[MSC clock/data timing for strong medium \(sm\) 5V output pads](#) on page 546

[MSC clock/data timing for medium \(m\) 5V output pads](#) on page 547

[MSC clock/data timing for LVDS 5V output pads](#) on page 547

[Upstream interface timing](#) on page 548

[MSC clock/data timing figures](#) on page 548

4.27.2 MSC clock/data timing for strong medium (sm) 5V output pads

Table 121 MSC clock/data timing for strong medium (sm) 5V output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
FCLPx clock period	$t_{40} CC$	$2 * T_A$	-	-	ns	$C_L = 50 \text{ pF}$
Deviation from ideal duty cycle	$t_{400} CC$	-5	-	5	ns	$C_L = 50 \text{ pF}$
SOPx output delay	$t_{44} CC$	-7	-	7	ns	$C_L = 50 \text{ pF}$
ENx output delay	$t_{45} CC$	-7	-	7	ns	$C_L = 50 \text{ pF}$

Related information

[MSC clock/data timing for strong sharp \(ss\) 5V output pads](#) on page 546

[MSC clock/data timing for medium \(m\) 5V output pads](#) on page 547

[MSC clock/data timing for LVDS 5V output pads](#) on page 547

[Upstream interface timing](#) on page 548

[MSC clock/data timing figures](#) on page 548

4.27.3 MSC clock/data timing for medium (m) 5V output pads

Table 122 MSC clock/data timing for medium (m) 5V output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
FCLPx clock period	$t_{40\text{ CC}}$	$2 * T_A$	-	-	ns	$C_L = 50\text{ pF}$
Deviation from ideal duty cycle	$t_{400\text{ CC}}$	-10	-	10	ns	$C_L = 50\text{ pF}$
SOPx output delay	$t_{44\text{ CC}}$	-20	-	20	ns	$C_L = 50\text{ pF}$
ENx output delay	$t_{45\text{ CC}}$	-20	-	20	ns	$C_L = 50\text{ pF}$

Related information

[MSC clock/data timing for strong sharp \(ss\) 5V output pads](#) on page 546

[MSC clock/data timing for strong medium \(sm\) 5V output pads](#) on page 546

[MSC clock/data timing for LVDS 5V output pads](#) on page 547

[Upstream interface timing](#) on page 548

[MSC clock/data timing figures](#) on page 548

4.27.4 MSC clock/data timing for LVDS 5V output pads

Table 123 MSC clock/data timing for LVDS 5V output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
FCLPx clock period	$t_{40\text{ CC}}$	$2 * T_A^{1) 2) 3)}$	-	-	ns	LVDS; $C_L = 50\text{ pF}$
Deviation from ideal duty cycle	$t_{400\text{ CC}}$	$-1.5^{1)}$	-	$1.5^{1)}$	ns	LVDS; $0 < C_L < 50\text{ pF}$
SOPx output delay	$t_{44\text{ CC}}$	$-4.0^{1)}$	-	$3.5^{1)}$	ns	$C_L = 50\text{ pF}$
ENx output delay	$t_{45\text{ CC}}$	$-4^{1)}$	-	$9^{1)}$	ns	ss; $C_L = 50\text{ pF}$; ABRA block bypassed
		$-4^{1)}$	-	$8.5^{1)}$	ns	ss; $C_L = 50\text{ pF}$; ABRA block used
		$-2^{1)}$	-	$17^{1)}$	ns	sm; $C_L = 50\text{ pF}$
		$-30^{1)}$	-	$30^{1)}$	ns	m; $C_L = 50\text{ pF}$

1) The load ($C_L=50\text{pF}$) defined in the condition list is a load definition for the single end signal EN and does not intend to add an additional load inside the differential signal lines. For single end signals the load definition defines the max length of the signal on the PCB layout. For the LVDS pads the IEEE Std 1596.3-1996 load definitions apply.

2) T_A depends on the clock source selected for baud rate generation in the ABRA block of the MSC.

3) The capacitive load on the LVDS pins is differential, the capacitive load on the CMOS pins is single ended.

Related information

[MSC clock/data timing for strong sharp \(ss\) 5V output pads](#) on page 546

[MSC clock/data timing for strong medium \(sm\) 5V output pads](#) on page 546

[MSC clock/data timing for medium \(m\) 5V output pads](#) on page 547

[Upstream interface timing](#) on page 548

[MSC clock/data timing figures](#) on page 548

4.27.5 Upstream interface timing

Table 124 Upstream interface timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SDI bit time	$t_{46} \text{ SR}$	$8 * t_{\text{MSC}}$	-	-	ns	
SDI rise time	$t_{48} \text{ SR}$	-	-	200	ns	
SDI fall time	$t_{49} \text{ SR}$	-	-	200	ns	

Related information

[MSC clock/data timing for strong sharp \(ss\) 5V output pads on page 546](#)

[MSC clock/data timing for strong medium \(sm\) 5V output pads on page 546](#)

[MSC clock/data timing for medium \(m\) 5V output pads on page 547](#)

[MSC clock/data timing for LVDS 5V output pads on page 547](#)

[MSC clock/data timing figures on page 548](#)

4.27.6 MSC clock/data timing figures

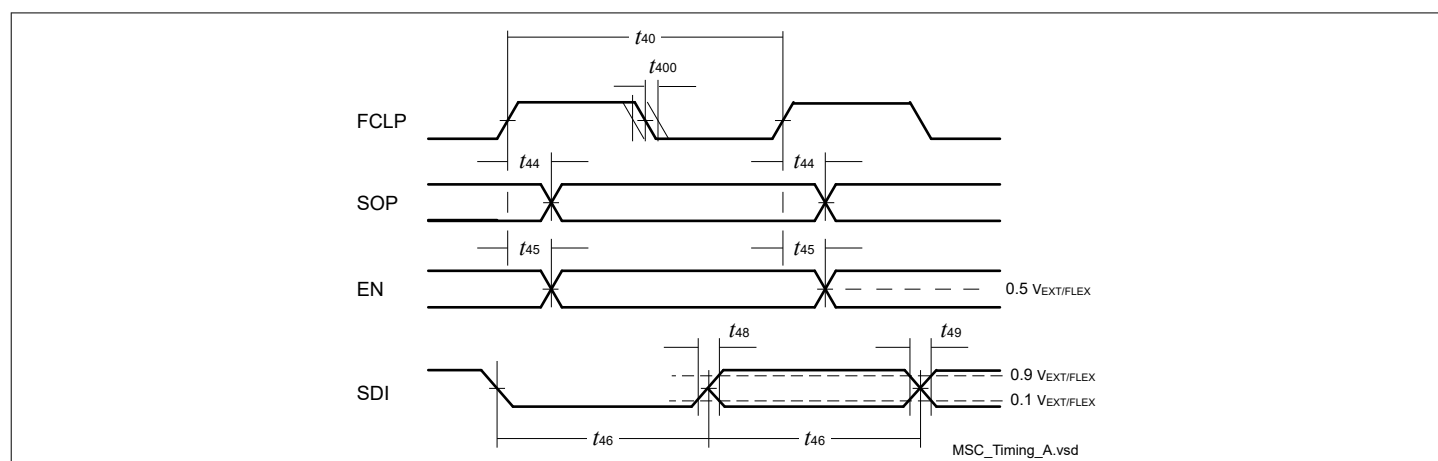


Figure 13 MSC clock/data timing

Related information

[MSC clock/data timing for strong sharp \(ss\) 5V output pads on page 546](#)

[MSC clock/data timing for strong medium \(sm\) 5V output pads on page 546](#)

[MSC clock/data timing for medium \(m\) 5V output pads on page 547](#)

[MSC clock/data timing for LVDS 5V output pads on page 547](#)

[Upstream interface timing on page 548](#)

4.28 E-Ray characteristics

The timing characteristics of following sub-chapter are valid for the driver setting = strong and edge configuration = sharp of the output drivers with a load capacitance of $C_L = 25 \text{ pF}$.

4.28.1 Transmit characteristics

Table 125 Transmit characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Rise time of TxEN	$t_{dCCTxENRise25CC}$	-	-	9	ns	$C_L = 25 \text{ pF}$
Fall time of TxEN	$t_{dCCTxENFall25CC}$	-	-	9	ns	$C_L = 25 \text{ pF}$
Sum of rise and fall time	$t_{dCCTxRise25+dCCTxFall25CC}$	-	-	9	ns	20% - 80%; $C_L = 25 \text{ pF}$
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, rising edge of TxEN	$t_{dCCTxEN01CC}$	-	-	25	ns	
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, falling edge of TxEN	$t_{dCCTxEN10CC}$	-	-	25	ns	
Asymmetry of sending	t_{tx_asymCC}	-2.45	-	2.45	ns	$C_L = 25 \text{ pF}$
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, rising edge of TxD	$t_{dCCTxD01CC}$	-	-	25	ns	
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, falling edge of TxD	$t_{dCCTxD10CC}$	-	-	25	ns	
TxD signal sum of rise and fall time at TP1_BD	t_{txd_sumCC}	-	-	9	ns	

Related information

[Receive characteristics](#) on page 550

4.28.2 Receive characteristics

Table 126 Receive characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Acceptance of asymmetry at receiving part	$t_{dCCTxAsymAcc_{ept25}}$ <i>SR</i>	-30.5	-	43.0	ns	$C_L = 25 \text{ pF}$
Acceptance of asymmetry at receiving part	$t_{dCCTxAsymAcc_{ept15}}$ <i>SR</i>	-31.5	-	44.0	ns	$C_L = 15 \text{ pF}$
Threshold for detecting logical high	$T_{uCCLogic1}$ <i>SR</i>	35	-	70	%	
Threshold for detecting logical low	$T_{uCCLogic0}$ <i>SR</i>	30	-	65	%	
Sum of delay between TP4_CC and TP4_FF and delays derived from TP4_FFi, rising edge of RxD	$t_{dCCRx01}$ <i>CC</i>	-	-	10	ns	
Sum of delay between TP4_CC and TP4_FF and delays derived from TP4_FFi, falling edge of RxD	$t_{dCCRx10}$ <i>CC</i>	-	-	10	ns	

Related information

[Transmit characteristics](#) on page 549

4.29 QSPI timing characteristics, Master and Slave Mode

This section defines the timings for the QSPI in the TC49xN STD. For the specified timing values it is assumed that SCLKO, MTSR, and SLSO pads have the same pad settings. The specified timing values are split in two sets:

- Speed graded signals with extension _F
- Signals belonging to a defined set of ports grouped to a segment:

Table 127 Segment definition

Segment	Ports	Module
0	Port01, Port02, Port10	QSPI1
1	Port11, Port13, Port14	QSPI2
2	Port30, Port33, Port34, Port35	QSPI5
3	Port21, Port22, Port23, Port25	QSPI4, QSPI6
4	Port15, Port20	QSPI0, QSPI7

4.29.1 QSPI Master Mode timing characteristics

Note: Pad asymmetry (defined by parameter t_{TX_ASYM}) is already included in the timing characteristics that follow.

Note: The following timings are only valid when the same pad type with the same speed grade configuration are used for all output signals.

4.29.1.1 QSPI Master Mode timing for strong sharp (ss) output pads

Table 128 QSPI Master Mode timing for strong sharp (ss) output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SCLKO clock period	$t_{50\ CC}$	20	-	-	ns	$C_L = 25\ pF$
Deviation from the ideal duty cycle	$t_{500\ CC}$	-3.5	-	2.5	ns	$C_L = 25\ pF$; timing parameter is valid for all other QSPI signals (apart signals with suffix _F) mapped to port slices within a segment
		-2	-	2	ns	$C_L = 25\ pF$; timing parameter is only valid for the preferred QSPI module mappings (corresponding signals mapped to those pads are marked with suffix _F)

(table continues...)

Table 128 (continued) QSPI Master Mode timing for strong sharp (ss) output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
MTSR delay from SCLKO shifting edge	$t_{51\ CC}$	-4	-	5	ns	$C_L = 25\text{ pF}$; valid for identical pad types of category Fast with identical configuration driver = strong, edge = sharp. Signals mapped to those pads are marked with suffix _F
		-5	-	5.5	ns	$C_L = 25\text{ pF}$; valid for mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = sharp or signals mapped to port slices within a segment
		-8	-	8	ns	$C_L = 25\text{ pF}$; else
SLSOn deviation from the ideal programmed position	$t_{510\ CC}$	-4	-	5	ns	$C_L = 25\text{ pF}$; valid for identical pad types of category Fast with configuration driver = strong and edge = sharp. Signals mapped to those pads are marked with suffix _F
		-5.0	-	5.5	ns	$C_L = 25\text{ pF}$; valid for mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = sharp or signals mapped to port slices within a segment
		-8	-	8	ns	$C_L = 25\text{ pF}$; else
MRST setup to SCLK latching edge	$t_{52\ SR}$	25 ^{1) 2)}	-	-	ns	$C_L = 25\text{ pF}$; valid for identical pad types of category Fast (signals mapped to those pads are marked with suffix _F) and mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = sharp or signals mapped to port slices within a segment
		26.5 ^{1) 2)}	-	-	ns	$C_L = 25\text{ pF}$; else

(table continues...)

Table 128 (continued) QSPI Master Mode timing for strong sharp (ss) output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
MRST hold from SCLK latching edge	$t_{53} SR$	-2 ^{1) 2)}	-	-	ns	$C_L = 25$ pF; valid for identical pad types of category Fast (signals mapped to those pads are marked with suffix _F) and mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = sharp or signals mapped to port slices within a segment
		-2 ^{1) 2)}	-	-	ns	$C_L = 25$ pF; else

1) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.

2) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

Related information

[QSPI Master Mode timing for strong medium \(sm\) output pads](#) on page 553

[QSPI Master Mode timing for medium \(m\) output pads](#) on page 554

[QSPI Master Mode timing for LVDS output pads \(clock/data\)](#) on page 555

[QSPI Master Mode timing figures](#) on page 556

4.29.1.2 QSPI Master Mode timing for strong medium (sm) output pads

Table 129 QSPI Master Mode timing for strong medium (sm) output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SCLKO clock period	$t_{50} CC$	50	-	-	ns	$C_L = 50$ pF
Deviation from the ideal duty cycle	$t_{500} CC$	-5	-	5	ns	$C_L = 50$ pF
MTSR delay from SCLKO shifting edge	$t_{51} CC$	-7	-	7	ns	$C_L = 50$ pF; valid for identical pad types of category Fast with configuration driver = strong and edge = medium. Signals mapped to those pads are marked with suffix _F
		-7	-	7	ns	$C_L = 50$ pF; valid for mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = medium or signals mapped to port slices within a segment
		-10	-	10	ns	$C_L = 50$ pF; else

(table continues...)

Table 129 (continued) QSPI Master Mode timing for strong medium (sm) output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SLSON deviation from the ideal programmed position	$t_{510} CC$	-7	-	7	ns	$C_L = 50$ pF; valid for identical pad types of category Fast with configuration driver = strong and edge = medium. Signals mapped to those pads are marked with suffix _F
		-7	-	7.5	ns	$C_L = 50$ pF; valid for mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = medium or signals mapped to port slices within a segment
		-10	-	10	ns	$C_L = 50$ pF; else
MRST setup to SCLK latching edge	$t_{52} SR$	35 ^{1) 2)}	-	-	ns	$C_L = 50$ pF; valid for mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = medium or signals mapped to port slices within a segment
MRST hold from SCLK latching edge	$t_{53} SR$	-5 ^{1) 2)}	-	-	ns	$C_L = 50$ pF; valid for mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = medium or signals mapped to port slices within a segment

1) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.

2) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

Related information

[QSPI Master Mode timing for strong sharp \(ss\) output pads](#) on page 551

[QSPI Master Mode timing for medium \(m\) output pads](#) on page 554

[QSPI Master Mode timing for LVDS output pads \(clock/data\)](#) on page 555

[QSPI Master Mode timing figures](#) on page 556

4.29.1.3 QSPI Master Mode timing for medium (m) output pads

Table 130 QSPI Master Mode timing for medium (m) output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SCLKO clock period	$t_{50} CC$	160	-	-	ns	$C_L = 50$ pF

(table continues...)

Table 130 (continued) QSPI Master Mode timing for medium (m) output pads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Deviation from the ideal duty cycle	$t_{500\ CC}$	-10	-	10	ns	$C_L = 50\text{ pF}$
MTSR delay from SCLKO shifting edge	$t_{51\ CC}$	-20	-	20	ns	$C_L = 50\text{ pF}$
SLSON deviation from the ideal programmed position	$t_{510\ CC}$	-20	-	20	ns	$C_L = 50\text{ pF}$
MRST setup to SCLK latching edge	$t_{52\ SR}$	80 ^{1) 2)}	-	-	ns	$C_L = 50\text{ pF}$
MRST hold from SCLK latching edge	$t_{53\ SR}$	-12 ^{1) 2)}	-	-	ns	$C_L = 50\text{ pF}$; QSPI; valid for identical pad types of category Fast with configuration driver = medium and edge = medium
		-13 ^{1) 2)}	-	-	ns	$C_L = 50\text{ pF}$; SCR SSC

1) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.

2) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

Related information

[QSPI Master Mode timing for strong sharp \(ss\) output pads](#) on page 551

[QSPI Master Mode timing for strong medium \(sm\) output pads](#) on page 553

[QSPI Master Mode timing for LVDS output pads \(clock/data\)](#) on page 555

[QSPI Master Mode timing figures](#) on page 556

4.29.1.4 QSPI Master Mode timing for LVDS output pads (clock/data)

Table 131 QSPI Master Mode timing for LVDS output pads (clock/data)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SCLKO clock period	$t_{50\ CC}$	20 ¹⁾	-	-	ns	$C_L = 25\text{ pF}$
Deviation from the ideal duty cycle	$t_{500\ CC}$	-1 ¹⁾	-	1 ¹⁾	ns	$C_L = 25\text{ pF}$
MTSR delay from SCLKO shifting edge	$t_{51\ CC}$	-3 ¹⁾	-	4 ¹⁾	ns	$C_L = 25\text{ pF}$; valid for identical pad types of category Fast (signals mapped to those pads are marked with suffix _F) and mixed pad types of category Fast and HSFast with identical configuration driver = strong, edge = sharp or signals mapped to port slices within a segment
		-4.0	-	10	ns	$C_L = 25\text{ pF}$; else

(table continues...)

Table 131 (continued) QSPI Master Mode timing for LVDS output pads (clock/data)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SLSON deviation from the ideal programmed position	$t_{510} CC$	-4 ¹⁾	-	8.0 ¹⁾	ns	$C_L = 25$ pF; driver strength ss
		-10 ¹⁾	-	14 ¹⁾	ns	$C_L = 25$ pF; driver strength sm
		-30 ¹⁾	-	30 ¹⁾	ns	$C_L = 25$ pF; driver strength m
MRST setup to SCLK latching edge	$t_{52} SR$	18 ¹⁾	-	-	ns	$C_L = 25$ pF; valid for LVDS Input pads only
MRST hold from SCLK latching edge	$t_{53} SR$	-1 ¹⁾	-	-	ns	$C_L = 25$ pF; valid for LVDS Input pads only

1) The load ($C_L = 25$ pF) defined in the condition list is a load definition for the single end signal SLSON and does not intend to add an additional load inside the differential signal lines. For single end signals the load definition defines the max length of the signal on the PCB layout. For the LVDS pads the IEEE Std 1596.3-1996 load definitions apply.

Related information

[QSPI Master Mode timing for strong sharp \(ss\) output pads](#) on page 551

[QSPI Master Mode timing for strong medium \(sm\) output pads](#) on page 553

[QSPI Master Mode timing for medium \(m\) output pads](#) on page 554

[QSPI Master Mode timing figures](#) on page 556

4.29.1.5 QSPI Master Mode timing figures

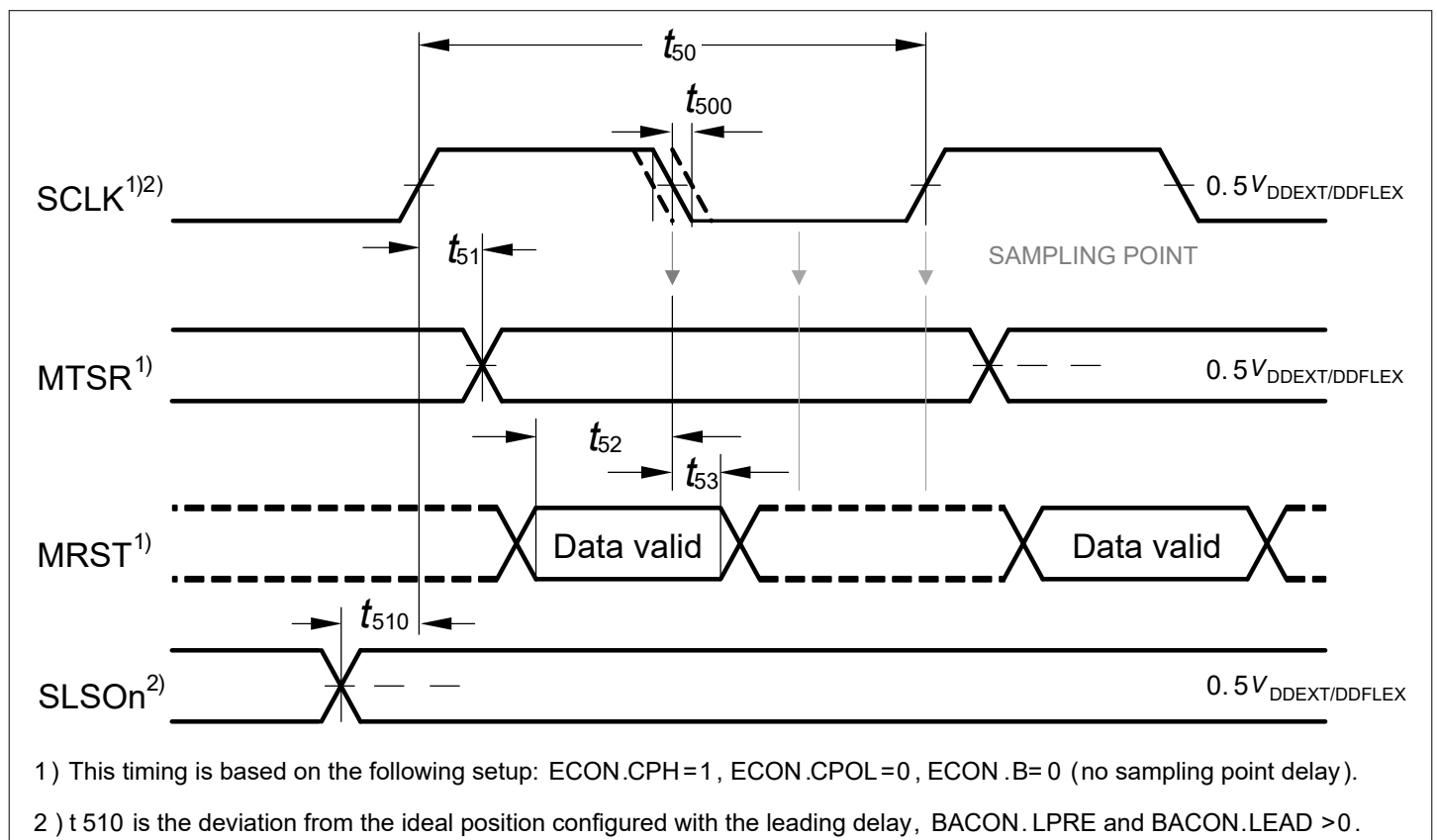


Figure 14 QSPI master mode timing

Related information

[QSPI Master Mode timing for strong sharp \(ss\) output pads on page 551](#)

[QSPI Master Mode timing for strong medium \(sm\) output pads on page 553](#)

[QSPI Master Mode timing for medium \(m\) output pads on page 554](#)

[QSPI Master Mode timing for LVDS output pads \(clock/data\) on page 555](#)

4.29.2 QSPI Slave Mode timing characteristics

4.29.2.1 QSPI Slave Mode timing

Table 132 QSPI Slave Mode timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
SCLK clock period	$t_{54} \text{ SR}$	4 x T_{Max} ¹⁾	-	-	ns	
SCLK duty cycle	$t_{55}/t_{54} \text{ SR}$	40	-	60	%	
MTSR setup to SCLK latching edge	$t_{56} \text{ SR}$	6	-	-	ns	Input Level AL; valid for QSPI input signals marked with suffix _F or QSPI input signals mapped to port slices within a segment
		11.5	-	-	ns	Input Level AL; else
		6	-	-	ns	Input Level TTL; valid for QSPI input signals marked with suffix _F or QSPI input signals mapped to port slices within a segment
		11	-	-	ns	Input Level TTL; else
MTSR hold from SCLK latching edge	$t_{57} \text{ SR}$	4	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
SLSI setup to first SCLK shift edge	$t_{58} \text{ SR}$	4	-	-	ns	Input Level AL; valid for QSPI input signals marked with suffix _F or QSPI input signals mapped to port slices within a segment
		7.5	-	-	ns	Input Level AL; else
		6	-	-	ns	Input Level TTL; valid for QSPI input signals marked with suffix _F or QSPI input signals mapped to port slices within a segment
		7	-	-	ns	Input Level TTL; else
SLSI hold from last SCLK latching edge	$t_{59} \text{ SR}$	3	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL

(table continues...)

Table 132 (continued) **QSPI Slave Mode timing**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
MRST delay from SCLK shift edge	$t_{60\ CC}$	2	-	24	ns	driver = strong, edge = sharp; $C_L = 50\text{ pF}$; valid for identical pad types of category Fast (signals mapped to those pads are marked with suffix _F) and mixed pad types of category Fast and HSFast or signals mapped to port slices within a segment
		-	-	27.5	ns	driver = strong, edge = sharp; $C_L = 50\text{ pF}$; else
		5	-	35	ns	driver = strong, edge = medium; $C_L = 50\text{ pF}$
		12	-	-	ns	medium driver; $C_L = 50\text{ pF}$; QSPI
		14	-	-	ns	medium driver; $C_L = 50\text{ pF}$; SCR SSC
		-	-	80	ns	medium driver; $C_L = 50\text{ pF}$

1) $T_{MAX} = 1/f_{QSPI} (\text{Max})$

Related information

[QSPI Slave Mode timing figures](#) on page 558

4.29.2.2 QSPI Slave Mode timing figures

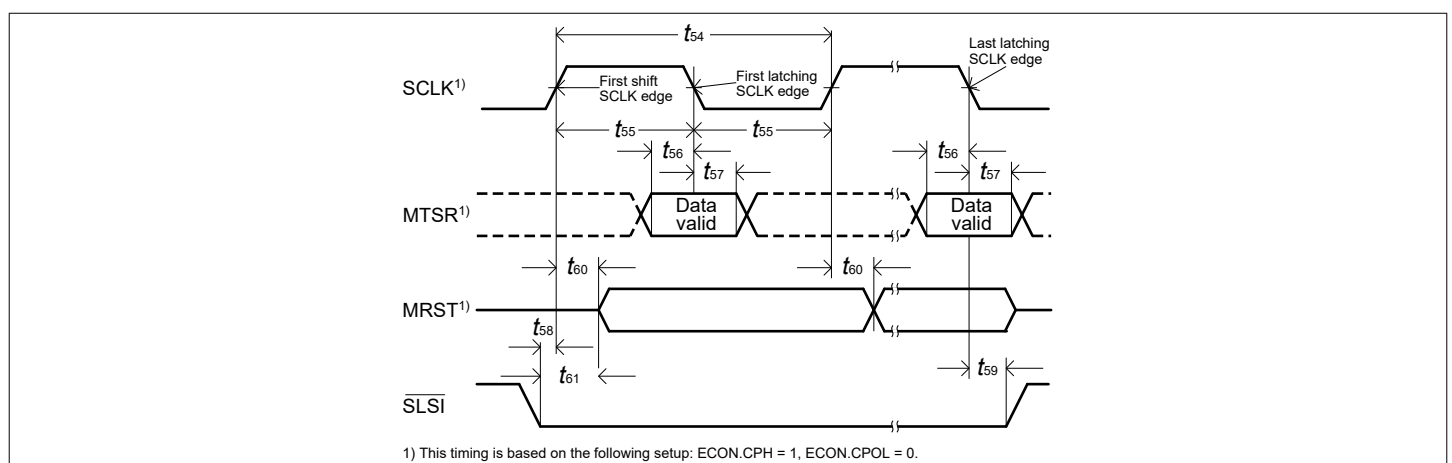


Figure 15 **Slave mode timing**

Related information

[QSPI Slave Mode timing](#) on page 557

4.30 SDMMC Interface timing characteristics

4.30.1 SDMMC timing

Table 133 SDMMC timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Clock period Data Transfer Mode	$t_1 CC$	20	-	-	ns	Push-pull; $C_L \leq 30$ pF; $V_{DDEXT} = 3.3$ V
Clock period Identification Mode	$t_2 CC$	-	-	2500	ns	Open-drain; $C_L \leq 30$ pF; $V_{DDEXT} = 3.3$ V
Clock low time	$t_3 CC$	6.5	-	-	ns	$C_L \leq 30$ pF; $V_{DDEXT} = 3.3$ V
Clock high time	$t_4 CC$	6.5	-	-	ns	$C_L \leq 30$ pF; $V_{DDEXT} = 3.3$ V
Data output valid time before rising clock edge	$t_5 CC$	3	-	-	ns	$C_L \leq 30$ pF; $V_{DDEXT} = 3.3$ V
Data output valid time after rising clock edge	$t_6 CC$	3	-	-	ns	$C_L \leq 30$ pF; $V_{DDEXT} = 3.3$ V
Data input hold time	$t_7 SR$	2.5	-	-	ns	$C_L \leq 30$ pF; $V_{DDEXT} = 3.3$ V; TTL levels
Data Input delay time	$t_8 SR$	-	-	13.7	ns	$C_L \leq 30$ pF; $V_{DDEXT} = 3.3$ V; TTL levels
Data Input setup time	$t_9 SR$	5.2	-	-	ns	$C_L \leq 30$ pF; $V_{DDEXT} = 3.3$ V; TTL levels

Related information

[SDMMC timing figure](#) on page 560

4.30.2 SDMMC timing figure

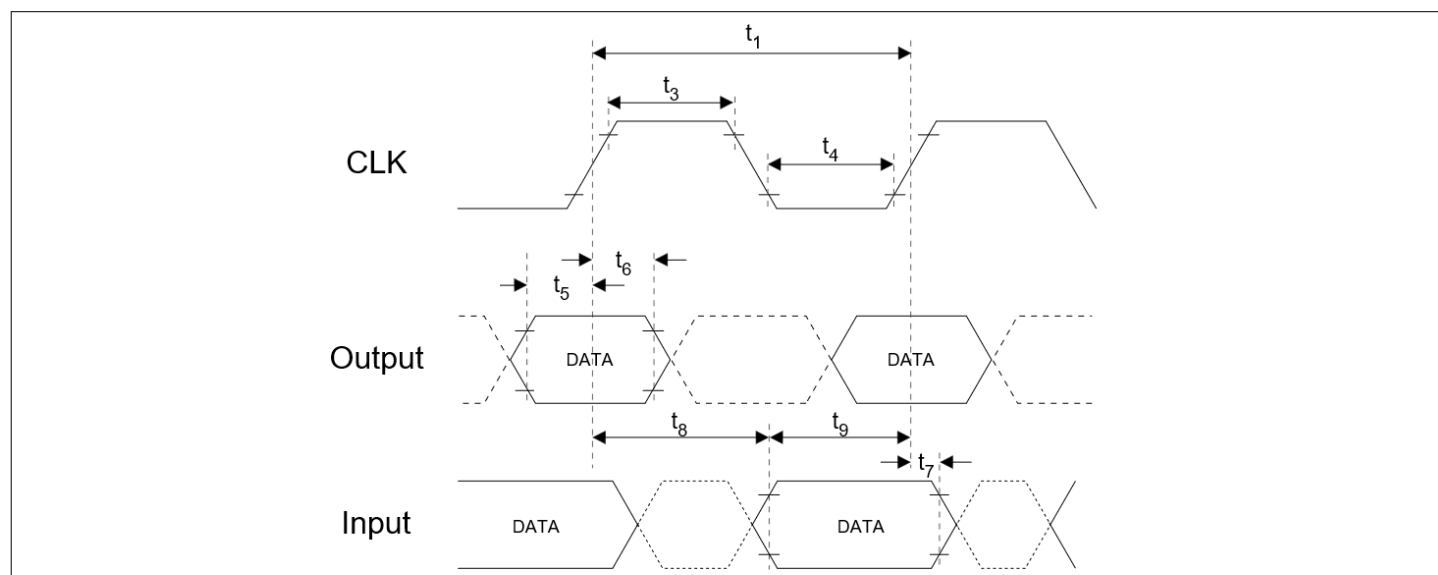


Figure 16 SDMMC Timing

Related information

[SDMMC timing](#) on page 559

4.31 HSCT characteristics

4.31.1 HSCT - Rx parasitics and loads

Table 134 HSCT - Rx parasitics and loads

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Parasitic inductance budget	$H_{\text{total CC}}$	-	-	10	nH	Value is valid for the desired HSCT transmission speed of 320 Mbps. Total Budget for complete receiver, including package, pins and bond wire. The contribution of the silicon is negligible.
Capacitance total budget	$C_{\text{total CC}}$	-	-	7	pF	Total Budget for complete receiver, including silicon, package, pins and bond wire. The maximum contribution of the package to the overall budget is 3.5 pF.

Related information

[HSCT - Rx/Tx setup timing characteristics](#) on page 561

[HSCT characteristics](#) on page 561

[HSCT eye diagram](#) on page 562

4.31.2 HSCT - Rx/Tx setup timing characteristics

Table 135 HSCT - Rx/Tx setup timing characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Disable time of the LVDS pad	$t_{LVDS\text{DIS}} CC$	-	-	20	ns	
RX o/p duty cycle	$DC_{rx} CC$	40	-	60	%	
Wakeup time from Sleep Mode	$t_{SWU} CC$	-	-	250	ns	
RX start-up time	$t_{rx\text{i}} CC$	-	-	600	ns	Wake-up RX from power down.
TX start-up time	$t_{tx} CC$	-	-	280	ns	Wake-up TX from power down.

Related information

[HSCT - Rx parasitics and loads](#) on page 560

[HSCT characteristics](#) on page 561

[HSCT eye diagram](#) on page 562

4.31.3 HSCT characteristics

Table 136 HSCT characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Bit Error Rate based on 20 MHz reference clock at Slave PLL side	$BER_{20} CC$	-	-	10EXP-12		at 320 Mbps with 20 MHz Sysclk
Bit Error Rate based on 25 MHz reference clock at Slave PLL side	$BER_{25} CC$	-	-	10EXP-12		at 320 Mbps with 25 MHz Sysclk
Transition time from RX Disable to RX Low Speed Mode	$t_{DISLS} CC$	-	-	1000	ns	Transition time from RX Disable to RX Low Speed Mode
Transition time from RX High/Low Speed Mode to RX Medium Speed Mode	$t_{HLSMS} CC$	-	-	500	ns	Transition time from RX High/Low Speed Mode to RX Medium Speed Mode
Transition time from RX High/Medium Speed Mode to RX Low Speed Mode	$t_{HMSLS} CC$	-	-	700	ns	Transition time from RX High/Medium Speed Mode to RX Low Speed Mode
Transition time from TX High Speed Mode to TX Low Speed Mode	$t_{HSLS} CC$	-	-	800	ns	Transition time from TX High Speed Mode to TX Low Speed Mode
Transition time from TX Low Speed Mode to TX High Speed Mode	$t_{LSHS} CC$	-	-	500	ns	Transition time from TX Low Speed Mode to TX High Speed Mode
Transition time from RX Medium/Low Speed Mode to RX High Speed Mode	$t_{MLS HS} CC$	-	-	400	ns	Transition time from RX Medium/Low Speed Mode to RX High Speed Mode

(table continues...)

Table 136 (continued) HSCT characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
HSCT physical layer power-on	$t_{PON\ CC}$	-	-	1.5	μs	HSCT physical layer power-on
Eye Opening	$EO\ CC$	55	-	-	%	at 320 Mbps with 25 MHz Sysclk
		55	-	-	%	at 320 Mbps with 20 MHz Sysclk

Related information

[HSCT - Rx parasitics and loads](#) on page 560

[HSCT - Rx/Tx setup timing characteristics](#) on page 561

[HSCT eye diagram](#) on page 562

4.31.4 HSCT eye diagram

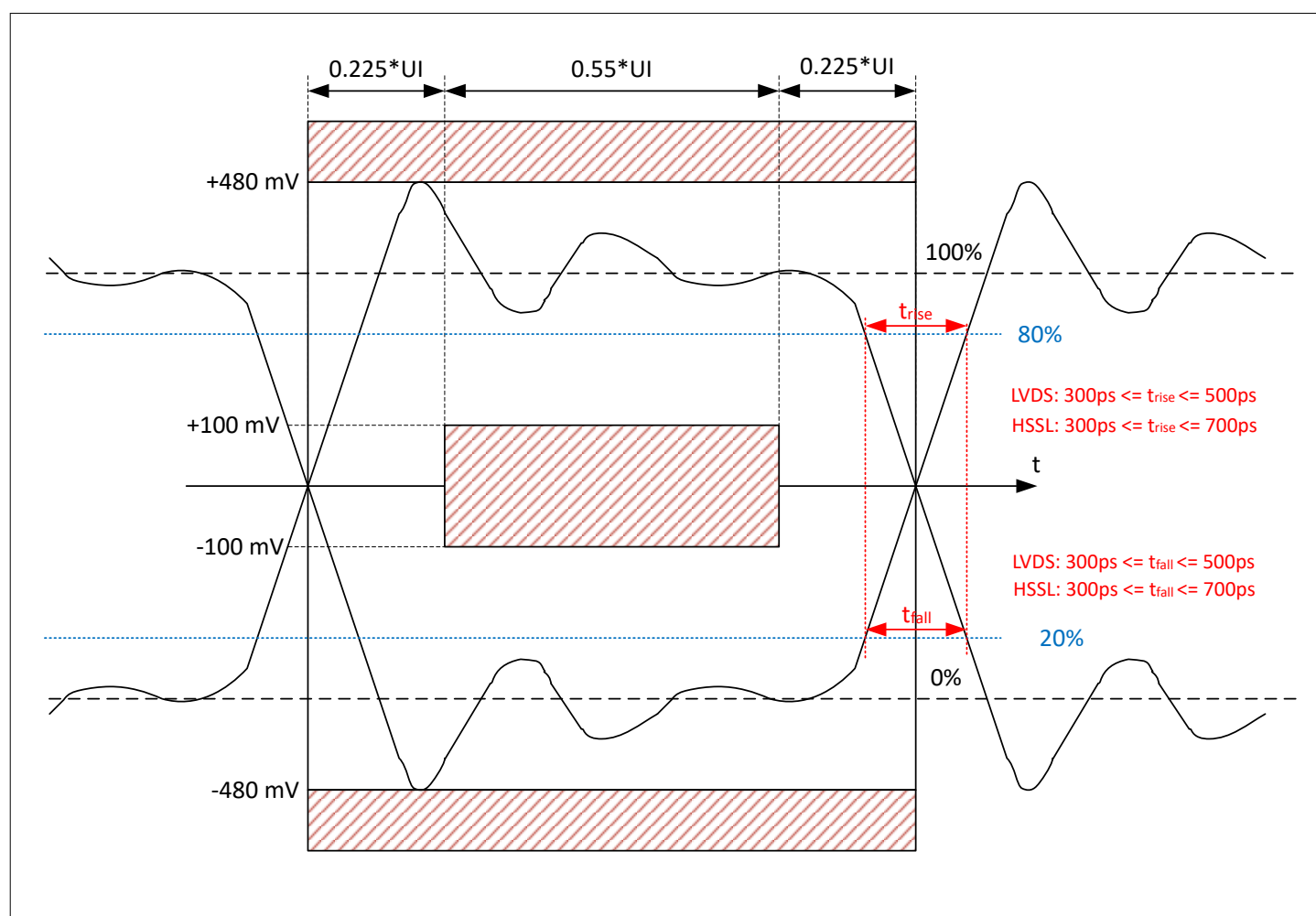


Figure 17 HSCT eye diagram

Related information

[HSCT - Rx parasitics and loads](#) on page 560

[HSCT - Rx/Tx setup timing characteristics](#) on page 561

[HSCT characteristics](#) on page 561

4.32 Ethernet Interface (ETH) timing characteristics

4.32.1 ETH definition of measurement reference points

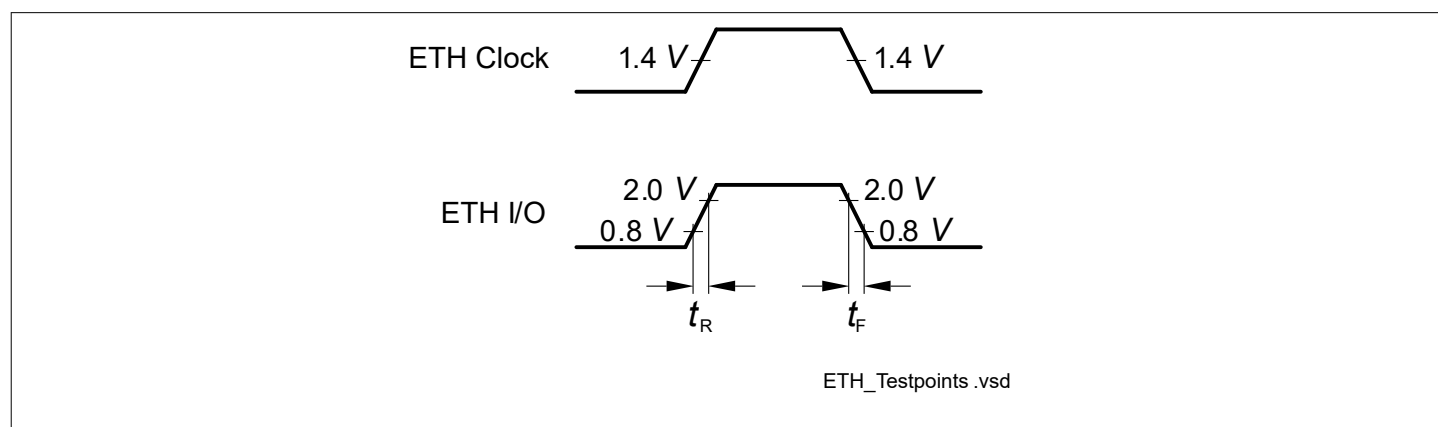


Figure 18 ETH Measurement Reference Points

4.32.2 ETH Management signal timing characteristics (ETH_MDC, ETH_MDIO)

The timing characteristics listed in the following sub-chapter are valid for the Ethernet (ETH) management signals MDC Management Data clock) and MDIO (Management Data Input/output). The following signal timings are valid for 3.3 V.

4.32.2.1 ETH management signal timing

Table 137 ETH management signal timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ETH_MDC period	$t_1 CC$	80	-	-	ns	$C_L = 25 \text{ pF}$
ETH_MDC high time	$t_2 CC$	16	-	-	ns	$C_L = 25 \text{ pF}$
ETH_MDC low time	$t_3 CC$	16	-	-	ns	$C_L = 25 \text{ pF}$
ETH_MDIO setup time (output)	$t_4 CC$	10	-	-	ns	$C_L = 25 \text{ pF}$
ETH_MDIO hold time (output)	$t_5 CC$	10	-	-	ns	$C_L = 25 \text{ pF}$
ETH_MDIO data valid (input)	$t_6 SR$	0	-	20	ns	$C_L = 25 \text{ pF}$

Related information

[ETH management signal timing figures](#) on page 564

4.32.2.2 ETH management signal timing figures

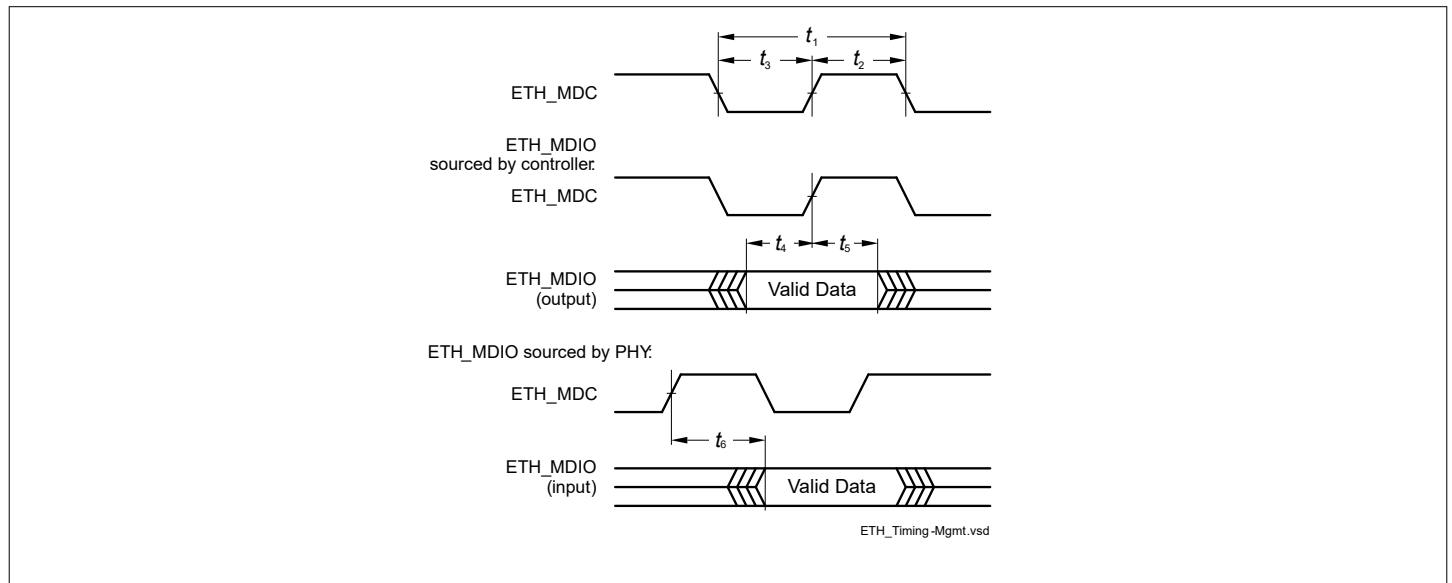


Figure 19 ETH management signal timing

Related information

[ETH management signal timing](#) on page 563

4.32.3 ETH 10BASE-T1S signal timing characteristics

In the following sub-chapter, the timing characteristics of the ETH 10BASE-T1S (Three Pin Interface) are listed.

4.32.3.1 ETH 10BASE-T1S signal timing

Table 138 ETH 10BASE-T1S signal timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Transmit data '0' low duration	$t_{\text{LowTXD0 CC}}$	-	20	-	ns	$C_L = 25 \text{ pF}$
Transmit data '0' high duration	$t_{\text{HighTXD0 CC}}$	-	60	-	ns	$C_L = 25 \text{ pF}$
Transmit data '1' low or high duration	$t_{\text{LowHighTXD1 CC}}$	-	20	-	ns	$C_L = 25 \text{ pF}$
RXD signal low pulse duration	$t_{\text{LowRXD SR}}$	12	-	-	ns	
RXD signal high pulse duration	$t_{\text{HighRXD SR}}$	12	-	-	ns	
ED signal low pulse duration	$t_{\text{LowED SR}}$	21	-	-	ns	

4.32.3.2 ETH 10BASE-T1S signal timing figure

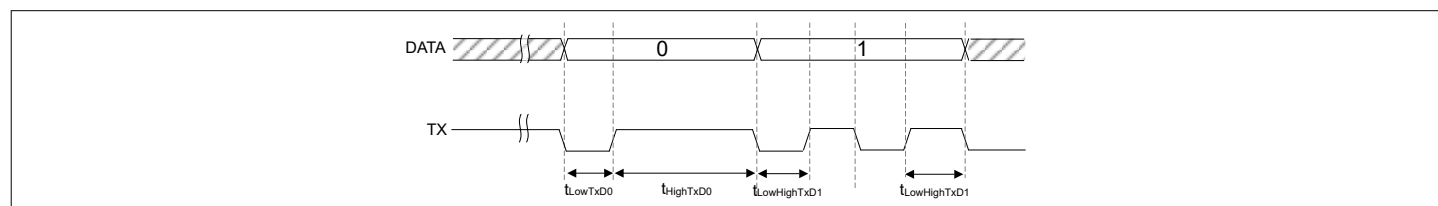


Figure 20 10BASE-T1S Signal Timing

4.32.4 ETH MII timing characteristics

In the following sub-chapter, the timing characteristics of the MII (Media Independent Interface) are listed. The following signal timings are valid for 3.3 V.

4.32.4.1 ETH MII signal timing

Table 139 ETH MII signal timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Clock period	t_7 SR	-	40	-	ns	$C_L = 25$ pF; baudrate = 100 Mbps
		-	400	-	ns	$C_L = 25$ pF; baudrate = 10 Mbps
Clock high time	t_8 SR	14	-	26	ns	$C_L = 25$ pF; baudrate = 100 Mbps
		140 ¹⁾	-	260 ²⁾	ns	$C_L = 25$ pF; baudrate = 10 Mbps
Clock low time	t_9 SR	14	-	26	ns	$C_L = 25$ pF; baudrate = 100 Mbps
		140 ¹⁾	-	260 ²⁾	ns	$C_L = 25$ pF; baudrate = 10 Mbps
Input setup time	t_{10} SR	10	-	-	ns	$C_L = 25$ pF
Input hold time	t_{11} SR	10	-	-	ns	$C_L = 25$ pF
Output valid time	t_{12} CC	0	-	25	ns	$C_L = 25$ pF

1) Defined by 35% of clock period.

2) Defined by 65% of clock period.

Related information

[ETH MII signal timing figures](#) on page 566

4.32.4.2 ETH MII signal timing figures

Ethernet media independent interface (ETH MII) signal timing.

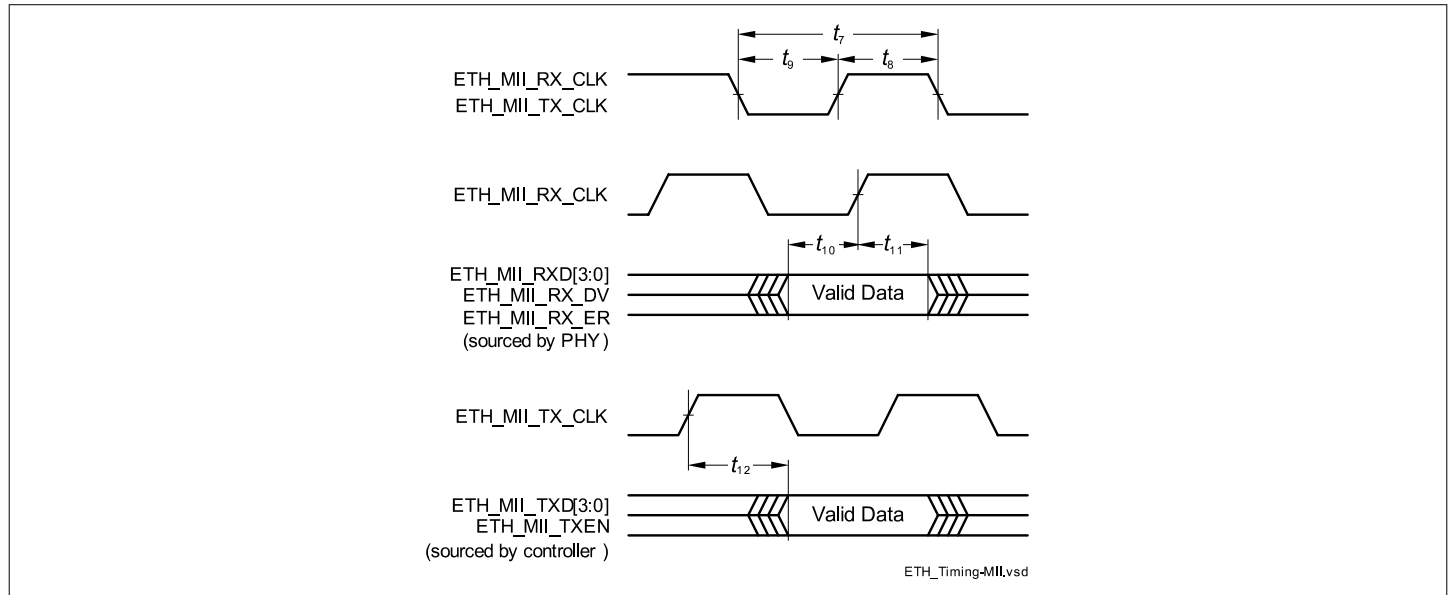


Figure 21 ETH MII signal timing

Related information

[ETH MII signal timing](#) on page 565

4.32.5 ETH RMII timing characteristics

The following sub-chapter contains the timing characteristics of the RMII (Reduced Media Independent Interface).

4.32.5.1 ETH RMII signal timing valid for 3.3V

Table 140 ETH RMII signal timing valid for 3.3V

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ETH_RMII_REF_CL clock period	t_{13} SR	-	20	-	ns	50 ppm; $C_L = 25$ pF ¹⁾
ETH_RMII_REF_CL clock high time	t_{14} SR	7 ²⁾	-	13 ³⁾	ns	$C_L = 25$ pF ¹⁾
ETH_RMII_REF_CL clock low time	t_{15} SR	7 ²⁾	-	13 ³⁾	ns	$C_L = 25$ pF ¹⁾
ETHTXEN, ETHTXD[1:0], ETHRXD[1:0], ETHCRSDV; setup time	t_{16} CC	4	-	-	ns	$C_L = 25$ pF ¹⁾
ETHTXEN, ETHTXD[1:0], ETHRXD[1:0], ETHCRSDV; hold time	t_{17} CC	2	-	-	ns	$C_L = 25$ pF ¹⁾

(table continues...)

Table 140 (continued) **ETH RMII signal timing valid for 3.3V**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ETH_RMII_TXD[1:0], ETH_RMII_TXEN data valid	t_{18} CC	-	-	15.2	ns	$C_L = 25$ pF

- 1) Maximum allowed capacitive load C_L for the RMII function on Port 20 in TC4Dx is 20 pF
2) Defined by 35% of clock period.
3) Defined by 65% of clock period.

Related information

[ETH RMII signal timing figures](#) on page 567

4.32.5.2 ETH RMII signal timing figures

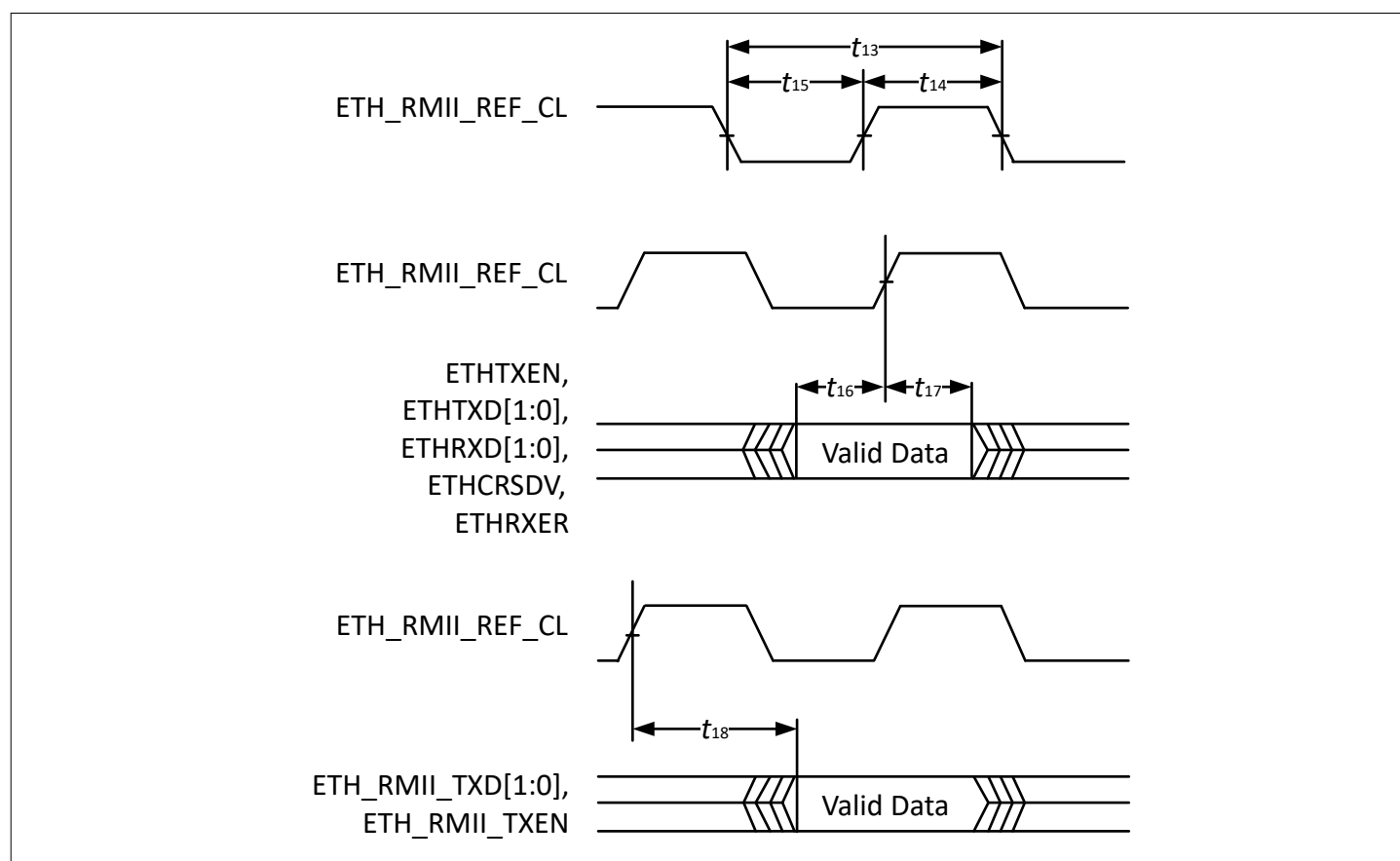


Figure 22 **ETH RMII signal timing**

Related information

[ETH RMII signal timing valid for 3.3V](#) on page 566

4.32.6 ETH SERDES characteristics

The following sub-chapters include the characteristics of the SGMII (Serial Gigabit Media Independent Interface).

Note: SGMII protocol operation via HSPHY is only possible with $f_{OSC} = 25\text{MHz}$ or 40MHz

4.32.6.1 ETH SERDES transmitter characteristics

Table 141 ETH SERDES transmitter characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Single ended signal DC characteristics						
Output DC high value	V_{oh} CC	-	-	1000	mV	
Output DC low value	V_{ol} CC	-350	-	-	mV	
Output current when shorted between P and N	I_{sab} CC	-	-	12	mA	
Differential signal characteristics						
Output Differential Voltage	$ V_{od} $ CC	250	-	630	mV	
Change in Vod between "1" and "0"	$\Delta V_{od} $ CC	-	-	25	mV	
Output common mode voltage	V_{os} CC	250	-	650	mV	
Change in Vos between "1" and "0"	ΔV_{os} CC	-	-	25	mV	
TX Output impedance, differentially	R_o CC	80	-	120	Ohm	
AC characteristics						
TX AC min amplitude	TX_{A1} CC	200	-	-	mV	
TX AC max amplitude	TX_{A2} CC	-	-	700	mV	
AC characteristics - SGMII 1.25 Gbaud						
Unit Interval	UI CC	-	800	-	ps	Allowed variation from Typ value: ± 300 ppm
Max jitter value	TX_{X1} CC	-	-	0.15	UI	valid for an SGMII line rate of 1.25 Gbaud (for 8b/10b encoded protocols with a data rate of 1 Gbps/100 Mbps)
Data eye measure point	TX_{X2} CC	-	-	0.39	UI	valid for an SGMII line rate of 1.25 Gbaud (for 8b/10b encoded protocols with a data rate of 1 Gbps/100 Mbps)
Total jitter	J_T CC	-	-	0.30	UI	valid for an SGMII line rate of 1.25 Gbaud (for 8b/10b encoded protocols with a data rate of 1 Gbps/100 Mbps)

Related information

[ETH SERDES transmitter eye](#) on page 569

[ETH SERDES receiver characteristics](#) on page 569

[ETH SERDES receiver eye](#) on page 570

4.32.6.2 ETH SERDES transmitter eye

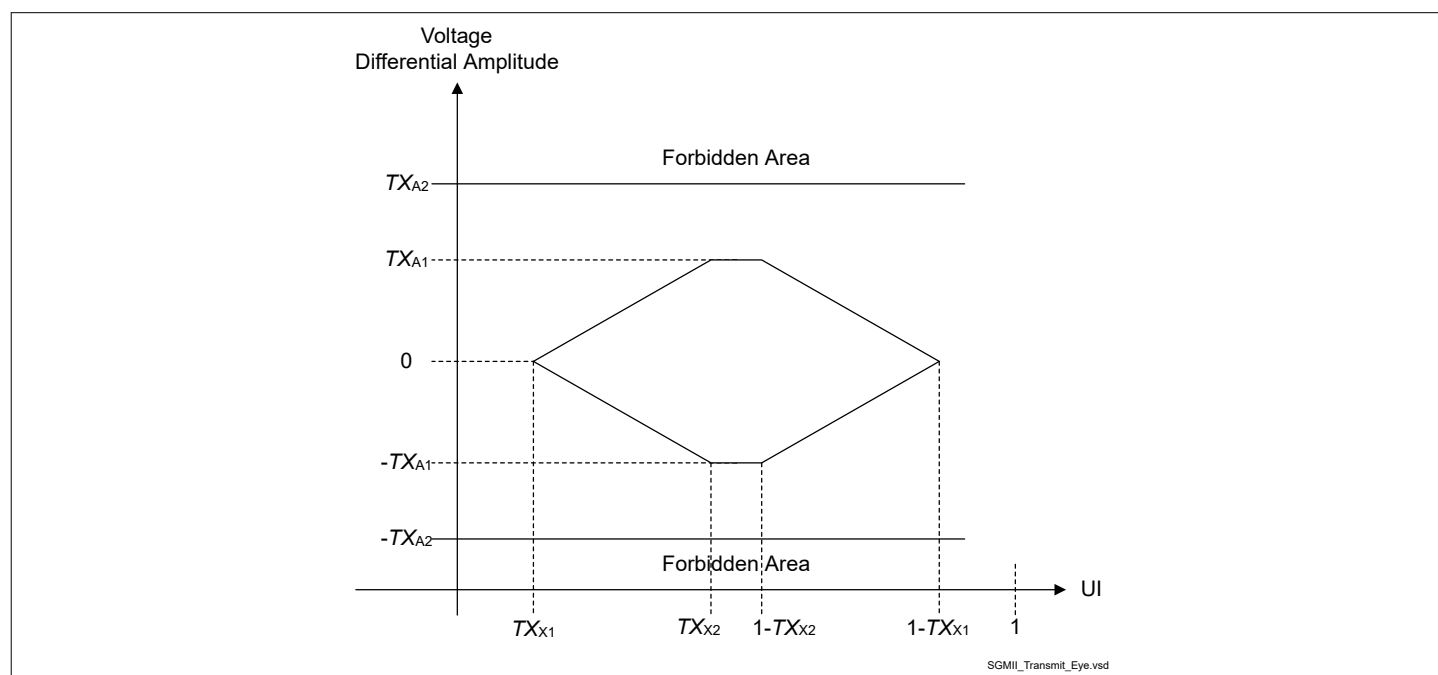


Figure 23 SERDES transmitter eye

Related information

[ETH SERDES transmitter characteristics](#) on page 568

[ETH SERDES receiver characteristics](#) on page 569

[ETH SERDES receiver eye](#) on page 570

4.32.6.3 ETH SERDES receiver characteristics

Table 142 ETH SERDES receiver characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Single ended signal DC characteristics						
Receiver input voltage range	V_i CC	0	-	1000	mV	
Differential signal characteristics						
Input differential impedance	R_{in} CC	80	-	120	Ohm	
AC characteristics						
RX AC min amplitude	RX_{A1} CC	100	-	-	mV	
RX AC max amplitude	RX_{A2} CC	-	-	700	mV	
Max jitter value	RX_{X1} CC	-	-	0.275	UI	Valid for all specified transmit line rates

Related information

[ETH SERDES transmitter characteristics](#) on page 568

[ETH SERDES transmitter eye](#) on page 569

[ETH SERDES receiver eye](#) on page 570

4.32.6.4 ETH SERDES receiver eye

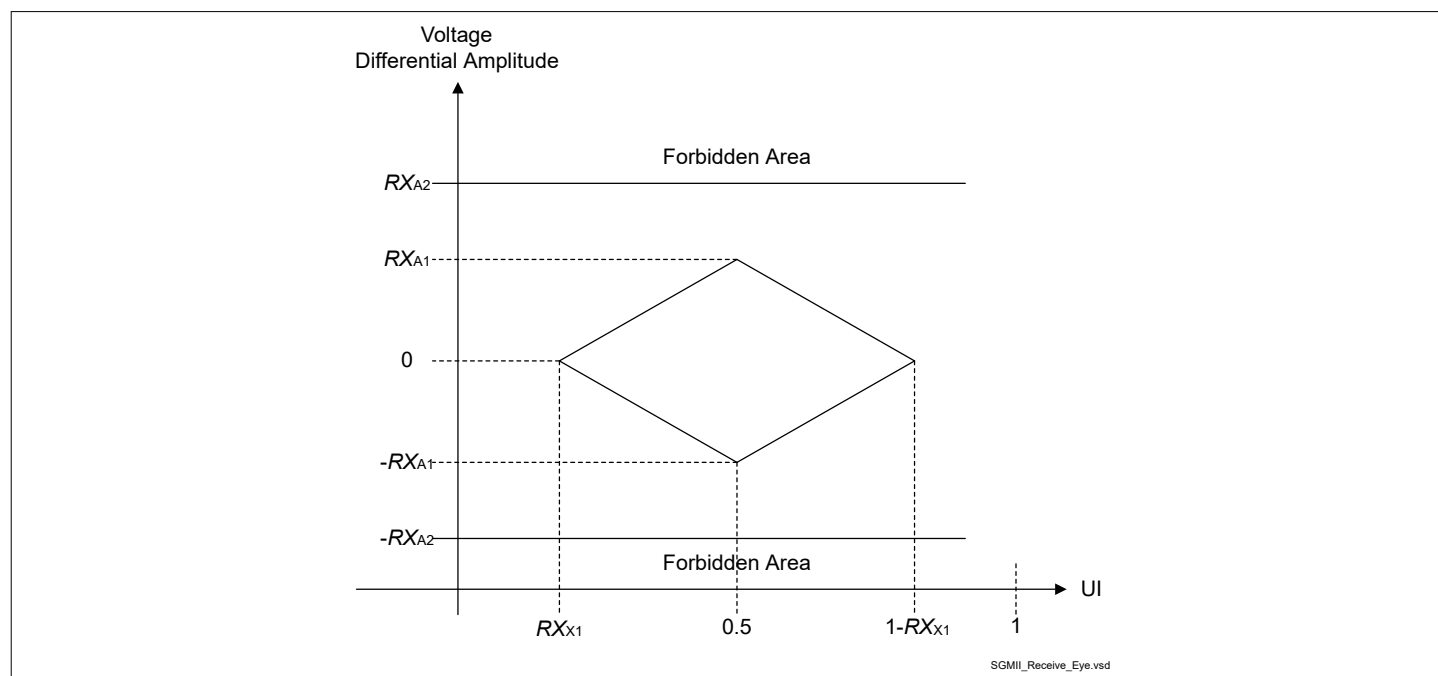


Figure 24 SERDES receiver eye

Related information

[ETH SERDES transmitter characteristics](#) on page 568

[ETH SERDES transmitter eye](#) on page 569

[ETH SERDES receiver characteristics](#) on page 569

4.33 FSP timing characteristics

Table 143 FSP timing characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Skew between FSP0 and FSP1, respectively between FSP2 and FSP3	$t_{\text{FSPSKEW}}^{\text{CC}}$	-6	-	6	ns	$C_L = 50 \text{ pF}$, driver = strong, edge = sharp
		-8	-	8	ns	$C_L = 50 \text{ pF}$, driver = strong, edge = medium
		-12	-	12	ns	$C_L = 50 \text{ pF}$, driver = medium

4.34 Flash characteristics

Table 144 Flash characteristics

Note: A running NVM command sequence (e.g. program or erase) shall be aborted before the supply voltages are ramped down to enter standby mode

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Program Flash Erase Time per logical sector	$t_{\text{SECTOR\_ERP CC}}$	-	-	0.2 ¹⁾	s	cycle count: ≤ 1000
Program Flash Erase Time per logical sector range	$t_{\text{RANGE\_ERP CC}}$	-	-	0.4 ¹⁾	s	cycle count: ≤ 1000; range: ≤ 32 consecutive logical sectors (≤ 512 KB)
Program Flash Program Time with 4x64 bit Program Operation per Page (32 Byte)	$t_{\text{PRG\_P64\_P CC}}$	-	-	90 ¹⁾	μs	32 Byte
Program Flash Program Time with 256 bit Program Operation per Page (32 Byte)	$t_{\text{PRG\_P256\_P CC}}$	-	-	70 ¹⁾	μs	32 Byte
Program Flash Program Time with 4x64 bit Program Operation in Burst Mode (512 Byte)	$t_{\text{PRG\_P64\_B CC}}$	-	-	530 ¹⁾	μs	512 Byte
Program Flash Program Time with 256 bit Program Operation in Burst Mode (512 Byte)	$t_{\text{PRG\_P256\_B CC}}$	-	-	220 ¹⁾	μs	512 Byte
Program Flash Program Time with 256 bit Program Operation in Burst Mode for 2 MB	$t_{\text{PRG\_P256\_B\_2MB CC}}$	-	-	1 ¹⁾	s	Derived value for documentation purpose
Write Page Once adder	$t_{\text{ADD CC}}$	-	-	15 ¹⁾	μs	Adder to Program Time when using Write Page Once
Program Flash abort to read latency	$t_{\text{ABORTP CC}}$	-	-	120 ¹⁾	μs	For Write Burst, Verify Erased and for multi-(logical) sector erase commands
Data Flash Program time per Page (8 Byte)	$t_{\text{PRG\_D\_P CC}}$	-	-	150 ¹⁾	μs	8 Byte
Data Flash Program time in Burst Mode (32 Byte)	$t_{\text{PRG\_D\_B CC}}$	-	-	200 ¹⁾	μs	32 Byte
Data Flash abort to read latency	$t_{\text{ABORTD CC}}$	-	-	120 ¹⁾	μs	
Wait time after margin change	$t_{\text{FL\_MarginDel CC}}$	-	-	5	μs	
Program Flash Endurance per Logical Sector ²⁾	$N_{\text{E\_P CC}}$	-	-	1000	cycles	

(table continues...)

Table 144 (continued) Flash characteristics

Note: A running NVM command sequence (e.g. program or erase) shall be aborted before the supply voltages are ramped down to enter standby mode

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Number of Erase Operations per Program Flash Bank	$N_{\text{ERP CC}}$	-	-	32000	cycles	
Program Flash Retention Time, Sector	$t_{\text{RET CC}}$	20	-	-	years	Max. 1000 erase/program cycles
UCB Retention Time	$t_{\text{RTU CC}}$	20	-	-	years	Max. 200 erase/program cycles per UCB
Data Flash access delay	$t_{\text{DF CC}}$	-	-	50	ns	
Program Flash access delay	$t_{\text{PF CC}}$	-	-	15	ns	
Number of erase operations on DF0 over lifetime	$N_{\text{ERD0S CC}}$	-	-	2000000 ³⁾	cycles	
Number of erase operations on DF1 over lifetime	$N_{\text{ERD1S CC}}$	-	-	2000000 ³⁾	cycles	
Data Flash Endurance per CSRMx sector ⁴⁾	$N_{\text{E\_CSRM CC}}$	-	-	250000 ⁵⁾	cycles	Retention time and T_J as mentioned in "Temperature operating conditions" chapter
DataFlash Endurance per EEPROMx sector ⁶⁾	$N_{\text{E\_EEPROM CC}}$	-	-	250000 ⁵⁾	cycles	Retention time and T_J in "Temperature operating conditions" chapter
Program Flash Maximum Number of Overwrite Operations on the same Page	$N_{\text{P\_PAGE\_OVE RWR CC}}$	-	-	2	cycles	After the initial prog each page of a wordline may be overwritten 2 additional times before next erase; in addition parameter $N_{\text{P\_LOGSEC\_BL\_PROG}}$ must be met
Data Flash Maximum Number of Overwrite Operations on the same Page	$N_{\text{D\_PAGE\_OVE RWR CC}}$	-	-	2	cycles	After the initial prog each page of a wordline may be overwritten 2 additional times before next erase; in addition parameter $N_{\text{D\_LOGSEC\_BL\_PROG}}$ must be met
Program Flash Logical Sector: Number of Program Operations on the same Bitline Address	$N_{\text{P\_LOGSEC\_B L\_PROG CC}}$	0	16	24	cycles	valid within a Logical Sector: 16 = # Wordlines per Log Sec; 24 considers 8 additional overwrites on the same bitline address

(table continues...)

Table 144 (continued) Flash characteristics

Note: A running NVM command sequence (e.g. program or erase) shall be aborted before the supply voltages are ramped down to enter standby mode

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Data Flash Logical Sector: Number of Program Operations on the same Bitline Address	$N_{D\_LOGSEC\_B\_L\_PROG}$ CC	0	4	8	cycles	valid within a Logical Sector: 4 = # Wordlines per Log Sec; 8 considers 4 additional overwrites on the same bitline address
User Content Count execution time per word-line	t_{CVWL} CC	-	-	150 ¹⁾	µs	
Data Flash Erase Time per logical sector	t_{SECTOR_ERDM} CC	-	-	0.15 ^{1) 7)}	s	cycle count: ≤ max allowed cycles defined by parameters NE_EEPROM and NE_CSRM
Data Flash Erase Time per logical sector range	t_{RANGE_ERDM} CC	-	-	0.5 ^{1) 7)}	s	cycle count: ≤ max allowed cycles defined by parameters NE_EEPROM and NE_CSRM; range: ≤ 128 consecutive logical sectors (≤ 256 KB)
DataFlash Erase Time per logical sector of quasi static data and per UCB	$t_{SECTOR\_ERDM\_LC\_UCB}$ CC	-	-	200 ¹⁾	ms	cycle count: ≤ 1.000 (EEPROM quasi static data or UCB)
DataFlash Erase Time per logical sector range of quasi static data	$t_{RANGE\_ERDM\_LC}$ CC	-	-	500 ¹⁾	ms	cycle count: ≤ 1.000 (EEPROM quasi static data or UCB)
Data Flash Erase Verify time per page	$t_{VER\_PAGE\_DS}$ CC	-	-	15 ¹⁾	µs	Time per 8 Byte page for Verify Erased Page command
Program Flash Erase Verify time per page	$t_{VER\_PAGE\_P}$ CC	-	-	15 ¹⁾	µs	Time per 32 Byte page for Verify Erased Page command
Data Flash Erase Verify time per sector	$t_{VER\_SEC\_DS}$ CC	-	-	180 ¹⁾	µs	Time per 2 KB sector for Verify Erased Logical Sector Range command
Program Flash Erase Verify time per sector	$t_{VER\_SEC\_P}$ CC	-	-	360 ¹⁾	µs	Time per 16KB sector for Verify Erased Logical Sector Range command
Data Flash Erase Verify time per wordline	$t_{VER\_WL\_DS}$ CC	-	-	50 ¹⁾	µs	
Program Flash Erase Verify time per wordline	$t_{VER\_WL\_P}$ CC	-	-	30 ¹⁾	µs	
Bank Sleep command execution time ⁸⁾	t_{BANK_SLEEP} CC	-	-	40	µs	

(table continues...)

Table 144 (continued) Flash characteristics

Note: A running NVM command sequence (e.g. program or erase) shall be aborted before the supply voltages are ramped down to enter standby mode

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Bank Wake-Up command execution time ⁹⁾	$t_{\text{BANK\_WAKEUP CC}}$	-	-	100	μs	
Bank Wake-Up command execution time (When NVM is in Deep Sleep) ⁹⁾	$t_{\text{NVM\_WAKEUP CC}}$	-	-	130	μs	
Program Flash Replace Logical Sector command execution time ¹⁰⁾	$t_{\text{RLS\_PF CC}}$	-	-	120	μs	
Data Flash Replace Logical Sector command execution time ¹⁰⁾	$t_{\text{RLS\_DF CC}}$	-	-	120	μs	
Disable Protection command execution time ¹⁰⁾	$T_{\text{DIS\_PROT CC}}$	1.9	-	2.0	μs	Values are measured starting from the point that the DMU acknowledges a bus request until it completes the command sequence execution.

- 1) Only valid for $f_{\text{FSI}} \geq 100$ MHz
- 2) Replace Logical Sector command must be used if a sector fails during an erase or a program operation. FAR will be accepted only when the Replace Logical Sector command also fails, or when the result of the Count Free Redundant Sectors command is 0 for the fail-affected PFlash bank (HOST and CSRM). For more details see "Error handling" chapter in the User Manual.
- 3) Allows segmentation of addressable memory into 8 logical sectors.
- 4) If a sector fails during an erase or a program operation, it is suggested to use the Replace Logical Sector command. If the Replace Logical Sector command is used, FAR will be accepted only when the command also fails, or when the result of the Count Free Redundant Sectors command is 0 for the CSRM DFlash bank. For more details see "Error handling" chapter in the User Manual. If the Replace Logical Sector command is not used to repair the failing sector, then it is the user's responsibility to implement a wordline skipping algorithm that is able to prevent the use of the failing wordlines, otherwise FAR will not be accepted.
- 5) Only valid when a robust EEPROM emulation algorithm is used. For more details see the Users Manual.
- 6) If a sector fails during an erase or a program operation, it is suggested to use the Replace Logical Sector command. If the Replace Logical Sector command is used, FAR will be accepted only when the command also fails, or when the result of the Count Free Redundant Sectors command is 0 for the HOST DFlash bank. For more details see "Error handling" chapter in the User Manual. If the Replace Logical Sector command is not used to repair the failing sector, then it is the user's responsibility to implement a wordline skipping algorithm that is able to prevent the use of the failing wordlines, otherwise FAR will not be accepted.
- 7) Under out-of-spec conditions (e.g. over-cycling) or in case of activation of WL oriented defects, the duration of erase processes may be increased by up to 50%.
- 8) Value is measured from the moment when DMU acknowledges the command request to the moment when the status flags of all selected banks are set in the sleep register (HOST and CSRM)
- 9) Value is measured from the moment when DMU acknowledges the command request to the moment when the status flags of all selected banks are cleared in the sleep register (HOST and CSRM)
- 10) Value is measured from the moment when DMU acknowledges the command request to the moment when command execution is completed.

4.35 xSPI timing characteristics

4.35.1 xSPI SDR timing without data strobe

Table 145 xSPI SDR timing without data strobe

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Transmit frequency in SDR mode	f_{TX_SDR} CC	-	-	25	MHz	Valid for Port 11 (only available in STD package variant) and Port 20; driver = strong, edge = sharp
Receive frequency in SDR mode	f_{RX_SDR} CC	-	-	25	MHz	Valid for Port 11 (only available in STD package variant) and Port 20; $V_{DDEXT} = 3.3$ V
Clock low to input valid timing ¹⁾	t_v SR	1	-	8	ns	Valid for Port 11 (only available in STD package variant) and Port 20; $f_{RX\_SDR} \leq 25$ MHz; $V_{DDEXT} = 3.3$ V; depending on the system load the sample delay shall be adapted by setting the corresponding value inside register RX_SAMPLE_DELAY.RSD; $C_L = 15$ pF
Output hold time ¹⁾	t_{hosdr} CC	2.0	-	-	ns	$C_L = 15$ pF
Output setup time ¹⁾	t_{susdr} CC	2.0	-	-	ns	$C_L = 15$ pF

1) Timing is measured at 50% of the output level

Related information

[xSPI SDR without data strobe timing figure](#) on page 575

4.35.2 xSPI SDR without data strobe timing figure

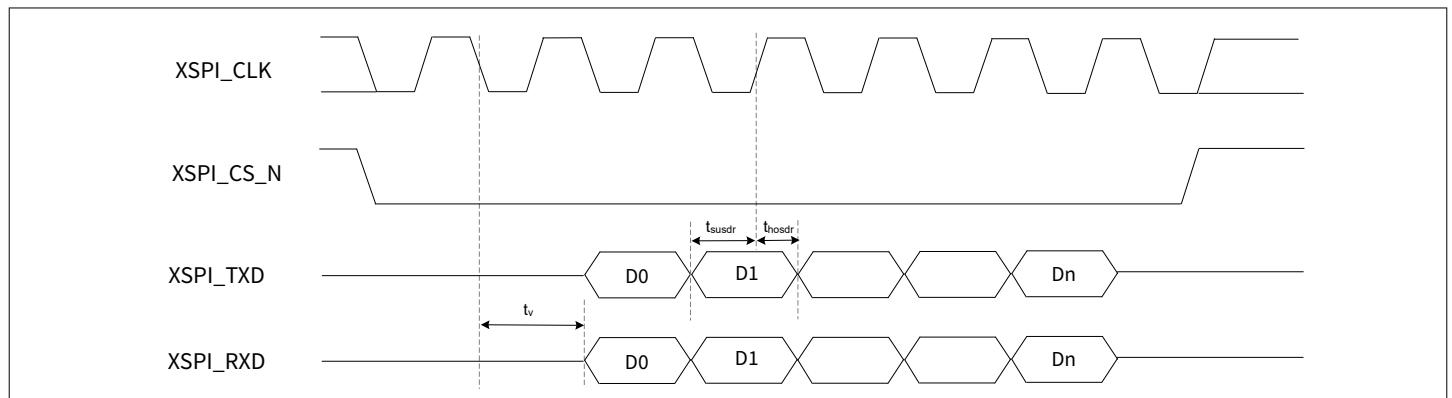


Figure 25 SDR without Data Strobe Timing

Related information

[xSPI SDR timing without data strobe](#) on page 575

4.36 DAP timing characteristics

The following characteristics are applicable for communication through the DAP debug interface.

4.36.1 DAP timing

Table 146 DAP timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
DAP0 clock period	t_{11} SR	6.25	-	-	ns	
DAP0 high time	t_{12} SR	2	-	-	ns	
DAP0 low time	t_{13} SR	2	-	-	ns	
DAP0 clock rise time	t_{14} SR	-	-	1	ns	$f = 160$ MHz
		-	-	4	ns	$f = 40$ MHz
		-	-	2	ns	$f = 80$ MHz
DAP0 clock fall time	t_{15} SR	-	-	1	ns	$f = 160$ MHz
		-	-	4	ns	$f = 40$ MHz
		-	-	2	ns	$f = 80$ MHz
DAP1 setup to DAP0 rising edge ¹⁾	t_{16} SR	4	-	-	ns	$f = 160$ MHz or $f = 80$ MHz
		5	-	-	ns	$f = 40$ MHz
DAP1 hold after DAP0 rising edge	t_{17} SR	2	-	-	ns	
DAP1 valid per DAP0 clock period ¹⁾	t_{19} CC	1	-	-	ns	$C_L = 20$ pF; $f = 160$ MHz; TTL
		7.25	-	-	ns	$C_L = 20$ pF; $f = 80$ MHz; TTL
		10	-	-	ns	$C_L = 50$ pF; $f = 40$ MHz; TTL

1) Timing parameter and parameter value is also valid for the DAP2 and DAP3 lines

Related information

[SCR DAP timing](#) on page 577

[DAP timing figures](#) on page 578

4.36.2 SCR DAP timing

Table 147 SCR DAP timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
DAP0 clock period	t_{11} SR	50	-	-	ns	
DAP0 high time	t_{12} SR	15	-	-	ns	
DAP0 low time	t_{13} SR	15	-	-	ns	

(table continues...)

Table 147 (continued) SCR DAP timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
DAP0 clock rise time	$t_{14} \text{ SR}$	-	-	8	ns	$f = 20 \text{ MHz}$
DAP0 clock fall time	$t_{15} \text{ SR}$	-	-	8	ns	$f = 20 \text{ MHz}$
DAP1 setup to DAP0 rising edge	$t_{16} \text{ SR}$	10	-	-	ns	
DAP1 hold after DAP0 rising edge	$t_{17} \text{ SR}$	10	-	-	ns	
DAP1 valid per DAP0 clock period	$t_{19} \text{ CC}$	30	-	-	ns	$C_L = 20 \text{ pF}; f = 20 \text{ MHz}$

Related information

[DAP timing](#) on page 577

[DAP timing figures](#) on page 578

4.36.3 DAP timing figures

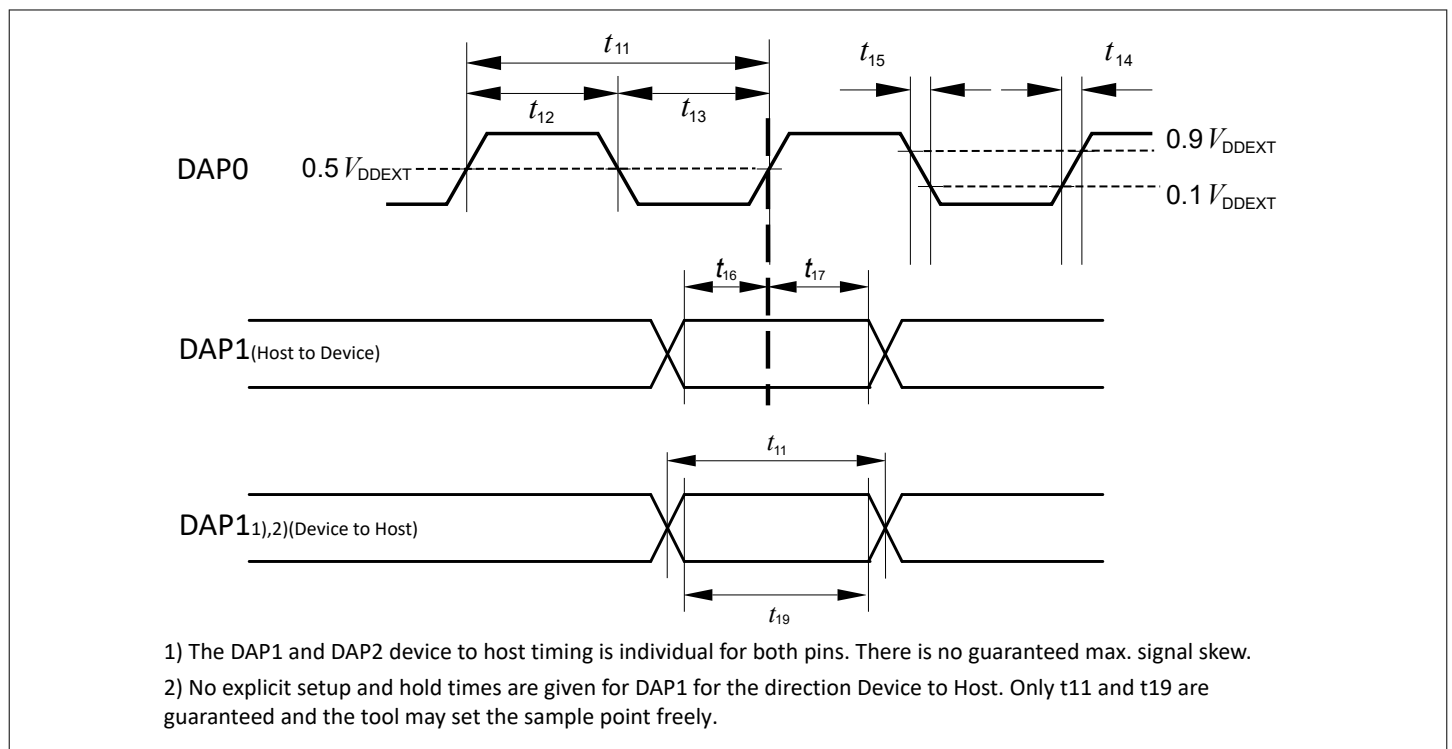


Figure 26 DAP timing

Related information

[DAP timing](#) on page 577

[SCR DAP timing](#) on page 577

4.37 JTAG timing characteristics

The following characteristics are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

The explanation of the timing characteristics can be found in the 'JTAG timing figures' sub-chapter.

4.37.1 JTAG timing

Table 148 JTAG timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	50	-	-	ns	
TCK high time	t_2 SR	10	-	-	ns	
TCK low time	t_3 SR	10	-	-	ns	
TCK clock rise time	t_4 SR	-	-	4	ns	
TCK clock fall time	t_5 SR	-	-	4	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6.0	-	-	ns	
TDI/TMS hold after TCK rising edge	t_7 SR	6.0	-	-	ns	
TDO valid after TCK falling edge (propagation delay)	t_8 CC	3.0	-	-	ns	$C_L \leq 20$ pF
		-	-	26.5	ns	$C_L \leq 50$ pF
TDO hold after TCK falling edge	t_{18} CC	2	-	-	ns	
TDO high impedance to valid from TCK falling edge	t_9 CC	-	-	28	ns	$C_L \leq 50$ pF
TDO valid output to high impedance from TCK falling edge	t_{10} CC	-	-	25	ns	$C_L \leq 50$ pF

Related information

[JTAG timing figures](#) on page 580

4.37.2 JTAG timing figures

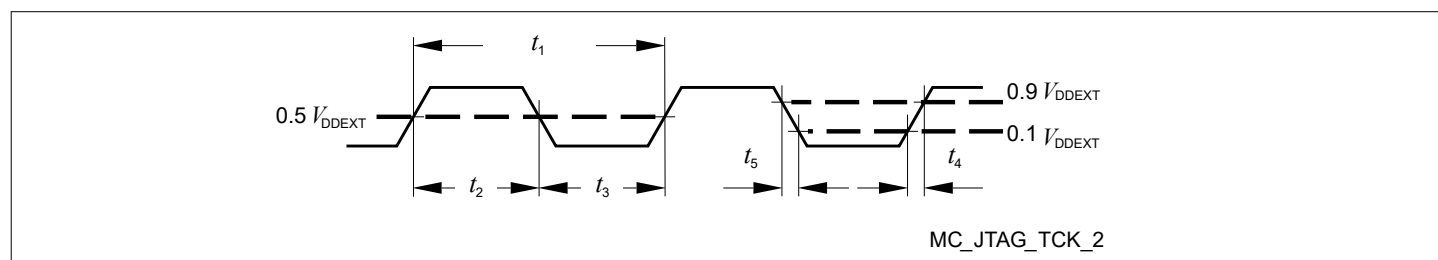


Figure 27 Test clock timing (TCK)

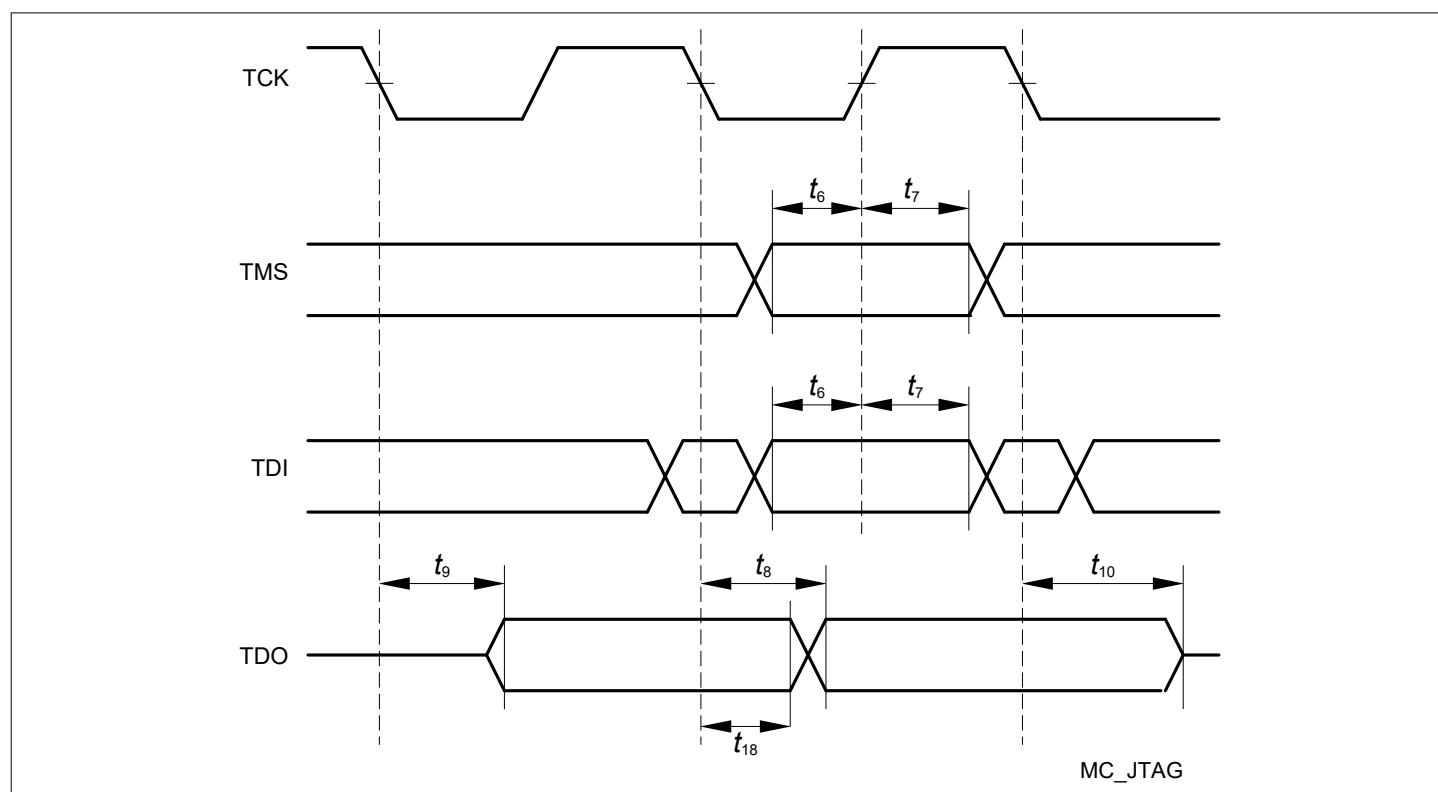


Figure 28 JTAG timing

Related information

[JTAG timing](#) on page 579

4.38 SGBT characteristics

SGBT is a trace interface dedicated for laboratory use only. Defined timing is only valid for laboratory conditions.

4.38.1 SGBT transmitter characteristics

Table 149 SGBT transmitter characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Differential signal characteristics						
Differential p-p voltage	$TX_{V_{diff\_pp}} CC$	600	-	1200	mV	
Differential DC impedance	$TX_{Z_{diff\_dc}} CC$	80	-	120	Ohm	
AC characteristics						
Rise time 20%-80%	$TX_{T_{rise}} CC$	30	-	-	ps	Measured at BGA pins by de-embedding the breakout channel (no additional de-embedding of the package is applied).
Fall time 20%-80%	$TX_{T_{fall}} CC$	30	-	-	ps	Measured at BGA pins by de-embedding the breakout channel (no additional de-embedding of the package is applied).
Differential skew	$TX_{T_{skew}} CC$	-	-	20	ps	Valid for a line rate of 6.25 Gbaud/s (for 8b/10b encoded protocols with a data rate of 5 Gbps)
		-	-	20	ps	Valid for a line rate of 5 Gbaud/s (for 8b/10b encoded protocols with a data rate of 4 Gbps)
		-	-	20	ps	Valid for a line rate of 2.5 Gbaud/s (for 8b/10b encoded protocols with a data rate of 2 Gbps)
Deterministic jitter	$J_D CC$	-	-	0.15	UI	Valid for a line rate of 6.25 Gbaud/s (for 8b/10b encoded protocols with a data rate of 5 Gbps)
		-	-	0.17	UI	Valid for a line rate of 5 Gbaud/s (for 8b/10b encoded protocols with a data rate of 4 Gbps)
		-	-	0.17	UI	Valid for a line rate of 2.5 Gbaud/s (for 8b/10b encoded protocols with a data rate of 2 Gbps)

(table continues...)

Table 149 (continued) SGBT transmitter characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Total jitter	J_T CC	-	-	0.35	UI	Valid for a line rate of 6.25 Gbaud/s (for 8b/10b encoded protocols with a data rate of 5 Gbps)
		-	-	0.35	UI	Valid for a line rate of 5 Gbaud/s (for 8b/10b encoded protocols with a data rate of 4 Gbps)
		-	-	0.35	UI	Valid for a line rate of 2.5 Gbaud/s (for 8b/10b encoded protocols with a data rate of 2 Gbps)
External AC coupling capacitance	$TX\_C_{ac\_ext}$ SR	75	100	200	nF	

Timing characteristics

Data rate	TX_DR CC	4999.5	5000	5000.5	Mbps	Valid for a line rate of 6.25 Gbaud/s (for 8b/10b encoded protocols with a data rate of 5 Gbps)
		3999.6	4000	4000.4	Mbps	Valid for a line rate of 5 Gbaud/s (for 8b/10b encoded protocols with a data rate of 4 Gbps)
		1999.8	2000	2000.2	Mbps	Valid for a line rate of 2.5 Gbaud/s (for 8b/10b encoded protocols with a data rate of 2 Gbps)

4.39 External components

4.39.1 HSPHY external components

Table 150 HSPHY external components

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
High speed PHY (HSPHY) resistor reference ¹⁾	$R_{RESREFX}$ SR	194	196	198	Ohm	Resistor has to be placed between pin PHYx_RESREF and VSSPHY plane on PCB

1) Reference resistor value is valid for SGMII, PCIE and SGBT operation using the HSPHY (if functions are available).

4.39.2 Buffering and decoupling capacitors

Table 151 Buffering and decoupling capacitors

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Capacitances on VDD pins / rail ^{1) 2) 3)}	C_{VDD_EXTBUF} SR	-	10 + 10 + 4.7	-	μF	Core supply provided externally and EVRC is off.
Capacitances on VDD pins / rail ²⁾	C_{VDD_EXTDEC} SR	-	2x1000 +2x100 +2x47	-	nF	Capacitors placed on bottom PCB layer below center ball matrix.
Capacitances on VDDEXT pins / rail ^{2) 4)}	C_{VDDEXT_EXTB} UF SR	-	4.7	-	μF	
Capacitances on VDDEXT pins / rail ²⁾	C_{VDDEXT_EXTD} EC SR	-	4 x 100	-	nF	
Capacitances on VDDEXTHS pins / rail ²⁾	$V_{DDEXTHS\_EXT}$ DEC SR	-	1 x 100	-	nF	
Capacitances on VDDEXTOSC pins / rail ²⁾	$C_{VDDEXTOSC\_E}$ XTDEC SR	-	100	-	nF	XTAL supply. Decoupling to local VSSOSC ground
Capacitances on VDDEXT pins / rail ²⁾	$C_{VDDEFLEX\_EXT}$ DEC SR	-	100	-	nF	
Capacitances on VDDEVRSB pins / rail ²⁾	$C_{VDDEVRSB\_EX}$ TDEC SR	-	100	-	nF	
Capacitances on VDDEXTDC pins / rail ^{2) 5)}	$C_{VDDEXTDC\_EX}$ TDEC SR	-	100	-	nF	Capacitor can be omitted for the use cases VDDEXTDC is tied to VDDEXT and EVRC is not used.
Capacitances on each VDDMx pins / rail ²⁾	C_{VDDM_EXTDE} C SR	-	100	-	nF	
Filter on VAREF pins / rail ²⁾	C_{VAREF_EXTFIL} SR	-	2.2	-	μF	Additional Resistor depending on noise and use case
Capacitances on each VDDPHPHYx pins / rail ²⁾	$C_{VDDPHPHYx\_EXTDEC}$ SR	-	1000 + 100	-	nF	Bigger capacitor may be omitted if regulator capacitors present
Capacitances on each VDDPHYx pins / rail ^{2) 6)}	$C_{VDDPHYx\_EXT}$ DEC SR	-	2200 + 100	-	nF	Capacitors for each HSPHY unit to ensure SGMII LETH/GETH (1Gbps) functionality. Ferrite bead is required to suppress high-frequency noise of power supply.

- 1) The capacitors can be omitted if additional buffer capacitors from the regulator generating the respective supply are placed close to the uC depending on load jumps, current consumption and bandwidth of the regulator.
- 2) The given capacitors serve as a reference example considering typical power pattern use cases and load jumps as documented in the datasheet. This is derived based on an example PCB implementation and regulator schematic scheme as shown in the figure and is verified only by simulation and validation and not characterization. The capacitances may not cover all extremities of use cases, all external regulators and components, therefore the implementation need to be additionally validated by the user together with the chosen regulators to ensure function. The tolerances of the capacitors need to be confirmed by the chosen capacitor vendor and adequate derating margins shall be applied for temperature, dc bias, lifetime and maximum continuous operation duration. Therefore Infineon cannot take liability on capacitor performance or tolerance, PCB implementations and external regulator schemes and this needs to be ensured by the user.

4 Electrical characteristics

- 3) If EVRC is used, the components specified in the EVRC regulator specification shall be considered instead.
- 4) If an equivalent capacitor is available from an external regulator, the capacitance is not needed.
- 5) Component size 0402 can be used in order to realize a capacitor placement as close as possible to the ball/pin. Other capacitance values and component sizes are also possible.
- 6) High-frequency noise of power supply might occur due to a noisy switch mode power supply or by sharing other supply domains with HSPHY

4.40 Quality declarations

4.40.1 Quality parameters

Table 152 Quality parameters

Quality Parameters (Golden Reference)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Moisture Sensitivity Level	MSL_{CC}	-	-	3		Conforming to JEDEC J-STD-020 for 260°C
ESD susceptibility according to Charged Device Model (CDM)	$V_{CDM_{SR}}$	-	-	250	V	for all balls/pins; conforming to JESD22-C101-C
ESD susceptibility according to Human Body Model (HBM)	$V_{HBM_{SR}}$	-	-	1000	V	Conforming to JESD22-A114-B
Operation Lifetime	$t_{OP_{CC}}$	-	-	24500	hour	see "Example temperature profile" as an example
Number of allowed power cycles	$N_{PC_{SR}}$	-	-	$1.5 \cdot 10^6$	cycles	

4.40.2 SRAM related fault tolerance

Table 153 SRAM related fault tolerance

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Maximum number of acceptable hard Single-Bit Errors ¹⁾	$M_{SBE_{CC}}$	-	-	7		Total RAM considered SRAM_TOT = 7806 kB ¹⁾
Maximum number of Bitline-oriented Errors	$M_{BLE_{CC}}$	-	-	2		

- ¹⁾ The parameter considers all RAMs being used by application except the ones specifically marked in the User Manual device specific VMT chapter with "Exclude from test".

5 Package information

Topics:

- PG-F2BGA-436
- PG-F2BGA-292

You can find all of the Infineon packages, types of packing and package related information, on our internet pages:
www.infineon.com/products.

5.1 PG-F2BGA-436

5.1.1 PG-F2BGA-436 outline

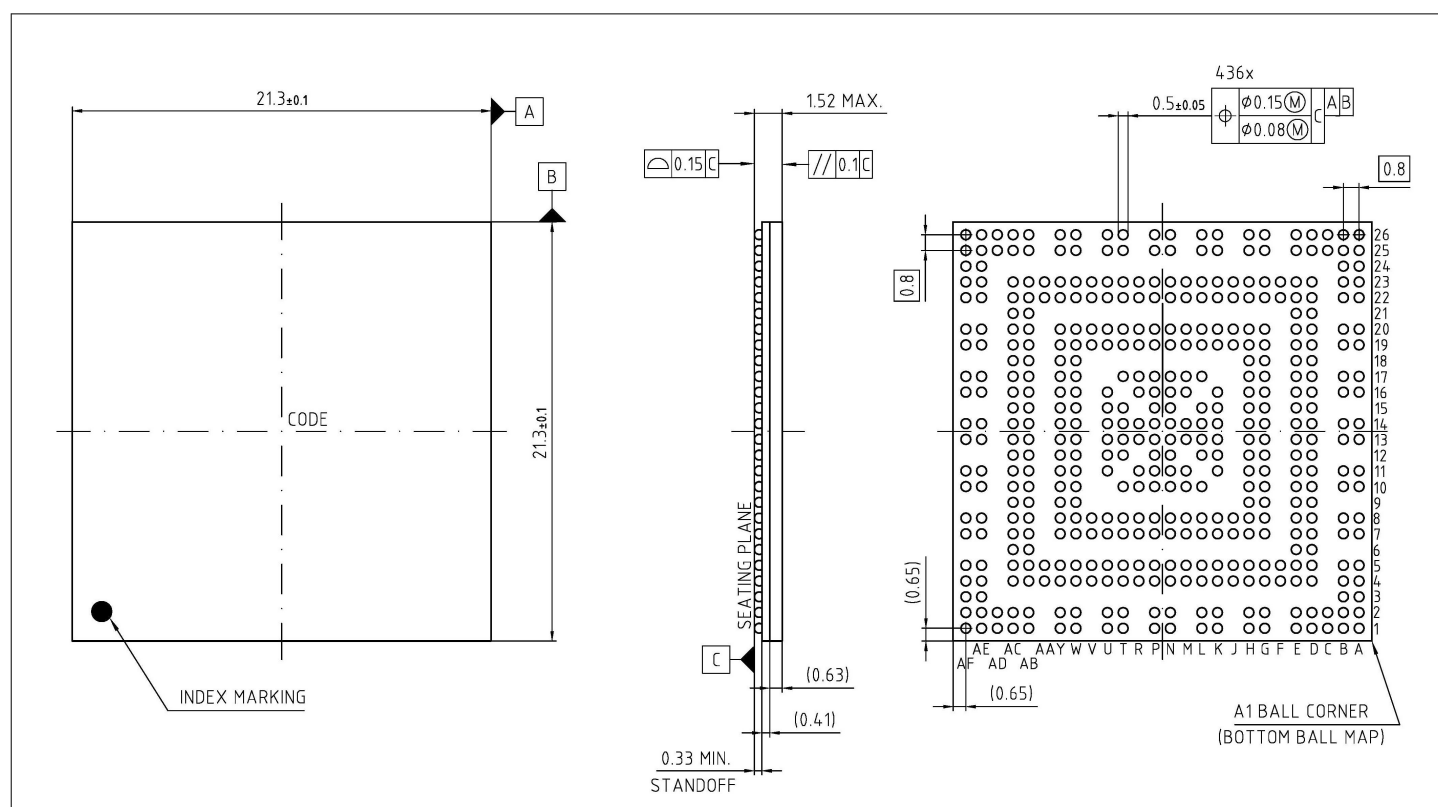


Figure 29 PG-F2BGA-436 Outline

5.1.2 PG-F2BGA-436 characteristics

Table 154 PG-F2BGA-436 characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Maximum Force applicable on package against top cooling TIM interface and mounting	P_{kgTopF} SR	-	100.0	-	N	

(table continues...)

Table 154 (continued) PG-F2BGA-436 characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
JEDEC Top Thermal resistance with heat sink at top of uC (junction to case top)	$R_{th-JCT\ CC}$	-	1.4 ¹⁾	-	K/W	Real1 power pattern used
JEDEC Bottom thermal resistance with heat sink at bottom of uC (junction to case bottom)	$R_{th-JCB\ CC}$	-	2.4 ¹⁾	-	K/W	Real1 power pattern used
Junction to Ambient (ECU) thermal resistance incl. PCB and ECU Housing enclosure (Standard Cooling)	$R_{th-JA\_SC\_ECU\ CC}$	-	14	-	K/W	Standard cooling stack and PCB considered as described in UM. Real0 Power Pattern with reduced ambient temperature $T_A = 95^{\circ}C$.
Junction to Ambient (uC) thermal resistance incl. PCB and excl. ECU Housing enclosure (Standard Cooling)	$R_{th-JA\_SC\_uC\ CC}$	-	6	-	K/W	Real0 Power Pattern with reduced ambient temperature $T_A = 95^{\circ}C$.
Junction to Ambient (ECU) thermal resistance incl. PCB and ECU Housing enclosure (Top Cooling)	$R_{th-JA\_TC\_ECU\ CC}$	-	9.5	-	K/W	Top cooling stack and PCB considered as described in UM. TIM thickness = 1.16mm, TIM Conductivity = 2.6W/mK. Real1 power pattern used. $T_A = 105^{\circ}C$.
Junction to Ambient (uC) thermal resistance incl. PCB and excl. ECU Housing enclosure (Top Cooling)	$R_{th-JA\_TC\_uC\ CC}$	-	3	-	K/W	Real1 power pattern used. $T_A = 105^{\circ}C$.

- 1) All parameters are established using thermal simulations. The top and bottom thermal resistances between the case and the ambient (R_{TH_JCA} , R_{TH_JCB}) are to be combined with the thermal resistances between the junction and the case given above (R_{TH_JCT} , R_{TH_JCB}), in order to calculate the total thermal resistance between the junction and the ambient (R_{TH_JA}). The thermal resistances between the case and the ambient (R_{TH_JCA} , R_{TH_JCB}) depend on the external system (PCB, case) characteristics, and are under user responsibility. The junction temperature can be calculated using the following equation: ($T_J = T_A + R_{TH\_JA} * PD$), where the R_{TH_JA} is the total thermal resistance between the junction and the ambient. R_{TH_JCT} and R_{TH_JCB} case thermal resistances are measured by the 'cold plate method' (MIL SPEC-883 Method 1012.1). R_{TH_JA} is established using reference ECU / PCB stacks and automotive boundary conditions as documented in the User Manual.

5.2 PG-F2BGA-292

5.2.1 PG-F2BGA-292 outline

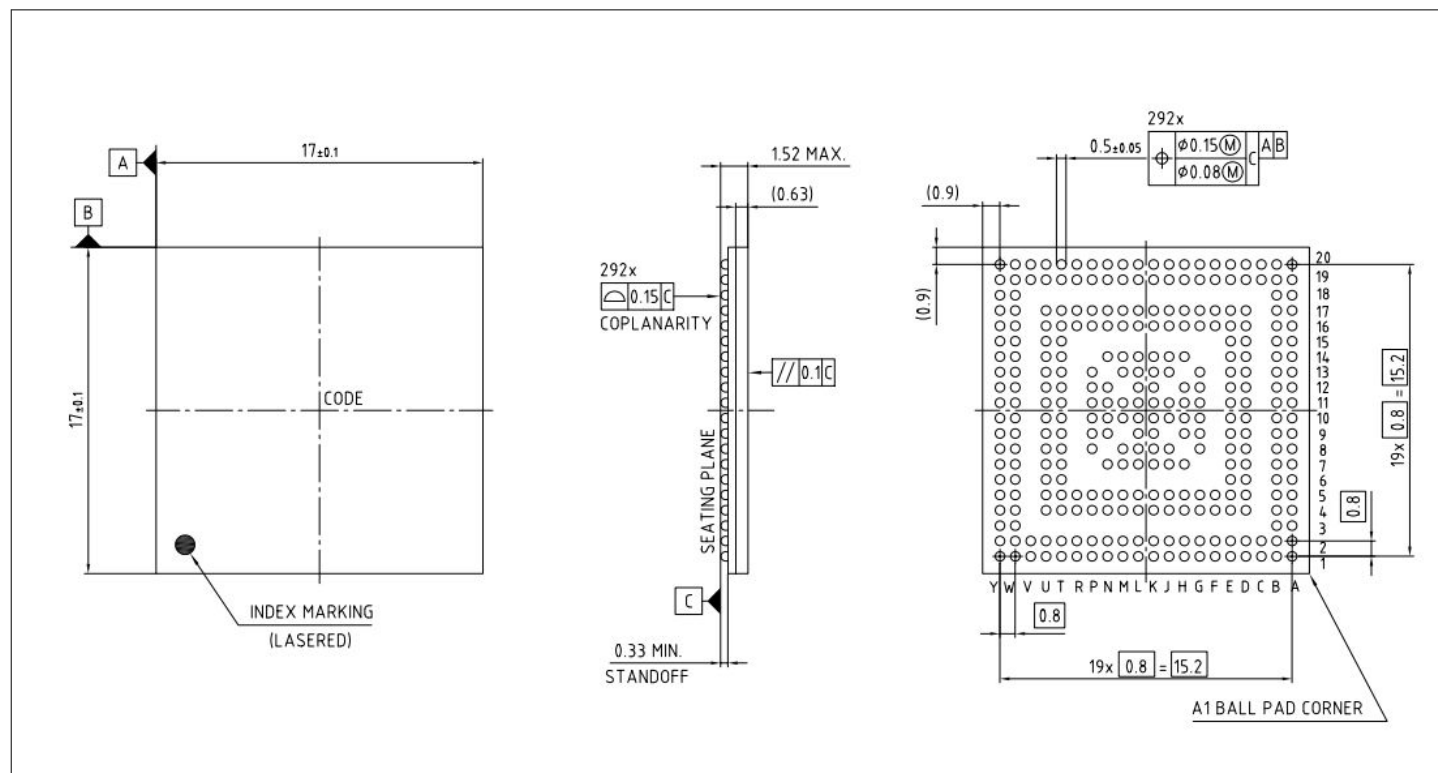


Figure 30 PG-F2BGA-292 Outline

5.2.2 PG-F2BGA-292 characteristics

Table 155 PG-F2BGA-292 characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Maximum Force applicable on package against top cooling TIM interface and mounting	P_{kgTopF} SR	-	65	-	N	
JEDEC Top Thermal resistance with heat sink at top of uC (junction to case top)	R_{th-JCT} CC	-	1.4 ¹⁾	-	K/W	Real1 power pattern used.
JEDEC Bottom thermal resistance with heat sink at bottom of uC (junction to case bottom)	R_{th-JCB} CC	-	2.7 ¹⁾	-	K/W	Real1 power pattern used.

(table continues...)

Table 155 (continued) PG-F2BGA-292 characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Junction to Ambient (ECU) thermal resistance incl. PCB and ECU Housing enclosure (Standard Cooling)	$R_{th-JA\_SC\_ECU}$ CC	-	16	-	K/W	Standard cooling stack and PCB considered as described in UM. Real0 Power Pattern with reduced ambient temperature $T_A = 95^{\circ}\text{C}$.
Junction to Ambient (uC) thermal resistance incl. PCB and excl. ECU Housing enclosure (Standard Cooling)	$R_{th-JA\_SC\_uC}$ CC	-	8	-	K/W	Real0 Power Pattern with reduced ambient temperature $T_A = 95^{\circ}\text{C}$.
Junction to Ambient (ECU) thermal resistance incl. PCB and ECU Housing enclosure (Top Cooling)	$R_{th-JA\_TC\_ECU}$ CC	-	10	-	K/W	Top cooling stack and PCB considered as described in UM. TIM thickness = 1.16mm, TIM Conductivity = 2.6W/mK. Real1 power pattern used. $T_A = 105^{\circ}\text{C}$.
Junction to Ambient (uC) thermal resistance incl. PCB and excl. ECU Housing enclosure (Top Cooling)	$R_{th-JA\_TC\_uC}$ CC	-	3	-	K/W	Real1 power pattern used. $T_A = 105^{\circ}\text{C}$.

- 1) All parameters are established using thermal simulations. The top and bottom thermal resistances between the case and the ambient (R_{th_JCA} , R_{th_JCA}) are to be combined with the thermal resistances between the junction and the case given above (R_{th_JCT} , R_{th_JCB}), in order to calculate the total thermal resistance between the junction and the ambient (R_{th_JA}). The thermal resistances between the case and the ambient (R_{th_JCA} , R_{th_JCA}) depend on the external system (PCB, case) characteristics, and are under user responsibility. The junction temperature can be calculated using the following equation: ($T_J = T_A + R_{th\_JA} * P_D$), where the R_{th_JA} is the total thermal resistance between the junction and the ambient. R_{th_JCT} and R_{th_JCB} case thermal resistances are measured by the 'cold plate method' (MIL SPEC-883 Method 1012.1). R_{th_JA} is established using reference ECU / PCB stacks and automotive boundary conditions as documented in the User Manual.



6 Revision history

Reference	Subjects (major changes since previous revision)
V 1.0, 2026-03	
	Initial version

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2026-03-04

Published by

Infineon Technologies AG
81726 Munich, Germany

© 2026 Infineon Technologies AG
All Rights Reserved.

Do you have a question about any aspect of this document?

Email: erratum@infineon.com

Document reference
IFX-abx1770377445643

Important notice

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Warnings

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.