

英飞凌 32 位

微控制器

TC37x

32 位单片机

AA版

32位单片机

数据手册

V 1.1, 2021-03

微控制器

Edition 2021-03
Published by
Infineon Technologies AG
81726 Munich, Germany
© 2021 Infineon Technologies AG
All Rights Reserved.

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com)

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

本数据手册的原文使用英文撰写。为方便起见，英飞凌提供了译文；由于翻译过程中可能使用了自动化工具，英飞凌不保证译文的准确性。为确认准确性请 务必访问 infineon.com 参考最新的英文版本（控制文档）。

Revision History

Page or Item	Subjects (major changes since previous revision)
V 0.4, 2018-01	
	Version 0.4 is the first version of this document
V 0.6, 2018-10	
	The history is documented in the last chapter
V 0.61, 2019-01	
	The history is documented in the last chapter
V 0.7, 2019-05	
	The history is documented in the last chapter
V 1.0, 2020-01	
	The history is documented in the last chapter
V 1.1, 2021-03	
	The history is documented in the last chapter

Trademarks of Infineon Technologies AG

AURIX™, C166™, CanPAK™, CIPOS™, CIPURSE™, EconoPACK™, CoolMOST™, CoolSET™, CORECONTROL™, CROSSAVE™, DAVE™, DI-POL™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPIM™, EconoPACK™, EiceDRIVER™, eupec™, FCOS™, HITFET™, HybridPACK™, I²RF™, ISOFACE™, IsoPACK™, MIPAQ™, ModSTACK™, my-d™, NovalithIC™, OptiMOST™, ORIGA™, POWERCODE™; PRIMARION™, PrimePACK™, PrimeSTACK™, PRO-SIL™, PROFET™, RASIC™, ReverSave™, SatRIC™, SIEGET™, SINDRION™, SIPMOS™, SmartLEWIS™, SOLID FLASH™, TEMPFET™, thinQ!™, TRENCHSTOP™, TriCore™.

Other Trademarks

Advance Design System™ (ADS) of Agilent Technologies, AMBA™, ARM™, MULTI-ICE™, KEIL™, PRIMECELL™, REALVIEW™, THUMB™, μVision™ of ARM Limited, UK.AUTOSAR™ is licensed by AUTOSAR development partnership. Bluetooth™ of Bluetooth SIG Inc. CAT-iq™ of DECT Forum. COLOSSUS™, FirstGPS™ of Trimble Navigation Ltd. EMV™ of EMVCo, LLC (Visa Holdings Inc.). EPCOS™ of Epcos AG. FLEXGO™ of Microsoft Corporation. FlexRay™ is licensed by FlexRay Consortium. HYPERTERMINAL™ of Hilgraeve Incorporated. IEC™ of Commission Electrotechnique Internationale. IrDA™ of Infrared Data Association Corporation. ISO™ of INTERNATIONAL ORGANIZATION FOR STANDARDIZATION. MATLAB™ of MathWorks, Inc. MAXIM™ of Maxim Integrated Products, Inc. MICROTEC™, NUCLEUS™ of Mentor Graphics Corporation. MIPI™ of MIPI Alliance, Inc. MIPS™ of MIPS Technologies, Inc., USA. muRata™ of MURATA MANUFACTURING CO., MICROWAVE OFFICE™ (MWO) of Applied Wave Research Inc., OmniVision™ of OmniVision Technologies, Inc. Openwave™ Openwave Systems Inc. RED HAT™ Red Hat, Inc. RFMD™ RF Micro Devices, Inc. SIRIUS™ of Sirius Satellite Radio Inc. SOLARIS™ of Sun Microsystems, Inc. SPANSION™ of Spansion LLC Ltd. Symbian™ of Symbian Software Limited. TAIYO YUDEN™ of Taiyo Yuden Co. TEAKLITE™ of CEVA, Inc. TEKTRONIX™ of Tektronix Inc. TOKO™ of TOKO KABUSHIKI KAISHA TA. UNIX™ of X/Open Company Limited. VERILOG™, PALLADIUM™ of Cadence Design Systems, Inc. VLYNQ™ of Texas Instruments Incorporated. VXWORKS™, WIND RIVER™ of WIND RIVER SYSTEMS, INC. ZETEX™ of Diodes Zetex Limited.

商标最新更新日期 2011-11-11

目录

1	特性描述.....	7
2	TC37x 引脚定义及功能.....	12
2.1	TC37x TP 的 LFBGA-292 封装引脚.....	13
2.2	TC37x T 和 TP 的 LQFP-176 封装引脚.....	113
2.3	焊盘框中焊盘排列顺序.....	194
2.4	图例说明.....	210
3	电气规格参数.....	212
3.1	参数解释.....	212
3.2	绝对最大额定值.....	213
3.3	过载下的引脚可靠性.....	214
3.4	工作条件.....	217
3.5	5 V / 3.3 V 可切换焊盘.....	221
3.6	高性能 LVDS 焊盘.....	241
3.7	VADC 参数.....	244
3.8	DSADC 参数.....	248
3.9	MHz 振荡器.....	251
3.10	备用时钟.....	253
3.11	温度传感器.....	254
3.12	电源电流.....	255
3.12.1	计算 1.25 V 消耗电流.....	262
3.13	电源基础结构和供电启动.....	263
3.13.1	供电上升和下降行为.....	263
3.13.1.1	单电源模式 (a).....	263
3.13.1.2	单电源模式 (e).....	266
3.13.1.3	外部供电模式 (d).....	268
3.13.1.4	外部供电模式 (h).....	270
3.14	复位时序.....	272
3.15	PMS.....	275
3.16	系统锁相环 (SYS_PLL).....	285
3.17	外设锁相环 (PER_PLL).....	286
3.18	AC规范.....	287
3.19	JTAG参数.....	288
3.20	DAP 参数.....	290
3.21	ASCLIN SPI 主时序.....	292
3.22	QSPI 时序、主模式和从模式.....	294
3.23	MSC时序 5V 操作.....	298
3.24	以太网接口 (ETH) 特性.....	300
3.24.1	ETH 测量参考点.....	300
3.24.2	ETH管理信号参数 (ETH_MDC、ETH_MDIO).....	301
3.24.3	ETH MII 参数.....	302
3.24.4	ETH RMII 参数.....	303
3.24.5	ETH RGMII 参数.....	304
3.25	E-Ray参数.....	305
3.26	HSCT 参数.....	307
3.27	Inter-IC (I2C) 接口时序.....	308
3.28	Flash 目标参数.....	312
3.29	质量声明.....	317
3.30	封装外形尺寸.....	318

3.30.1	封装参数.....	319
4	修订记录.....	321
4.1	从版本0.4 到版本0.6 的变更	321
4.2	从版本0.6 到版本0.61 的变更	330
4.3	从版本0.61到版本0.7 的变更	333
4.4	从版本0.7到版本0.71 的变更	335
4.5	从版本0.71 到版本1.0 的变更	337
4.6	从版本1.0 到版本1.1 的变更	338

1 特性描述

TC37x产品系列具有以下特点：

- 配备三个 CPU 核心的高性能微控制器
- 三个 32 位超标量 TriCore CPU (TC1.6.2P)，每个都具有以下特点：
 - 卓越的实时性能
 - 强大的位处理能力
 - 完全集成的 DSP 功能
 - 乘法累加单元能够实现每个周期2次MAC运算
 - 全流水线浮点单元(FPU)
 - 全温度范围内运行速度高达 300 MHz
 - 高达 240/96 KB 的数据暂存 RAM (DSPR)
 - 高达 64 KB 的指令暂存 RAM (PSPR)
 - 32 KB 指令高速缓存 (ICACHE)
 - 16 KB 数据缓存 (DCACHE)
- 最多支持两个 TC1.6.2P 的锁步核
- 多个片上存储器
 - 所有嵌入式 NVM 和 SRAM 均受到 ECC 保护
 - 高达 6 MB 的程序闪存式存储器 (PFLASH)
 - 高达 256 KB 数据闪存式存储器 (DFLASH 0) 可用于 EEPROM 仿真
 - 引导只读存储器 (BROM)
- 具有安全数据传输的 128 通道 DMA 控制器
- 先进的中断系统 (ECC保护)
- 高性能片上总线结构
 - 64 位交叉互连总线 (SRI)可提供总线主控器、CPU 和存储器之间高速并行访问
 - 用于片上外设和功能单元的 32 位系统外设总线 (SPB)
 - SRI 至 SPB 总线桥 (SFI 桥)
- 某些型号可选配硬件安全模块 (HSM)
- 处理安全监测警报的安全管理单元 (SMU)
- 具有 ECC、内存初始化和 MBIST 功能 (MTU) 的内存测试单元
- 用于检查数字 I/O 的硬件 I/O 监视器 (IOM)
- 多功能片上外设单元
 - 12 个异步/同步串行通道 (ASCLIN)，支持硬件 LIN (V1.3、V2.0、V2.1 和 J2602)，速率高达 50 MBaud
 - 5 个队列 SPI 接口通道 (QSPI)，具有主从功能，速率高达 50 Mbit/s
 - 1 个高速串行链路 (HSSL)，用于处理器间串行通讯，速度高达 320 Mbit/s
 - 2 个串行微秒总线接口 (MSC)，用于将串行端口扩展到外部电源设备
 - 2 个 MCMCAN 模块，每个模块带有 4 个 CAN 节点，可通过 FIFO 缓冲实现高效数据处理
 - 15 个单边半字节传输 (SENT) 通道，用于连接传感器
 - 1 个 FlexRay™模块，带 2 个通道 (E-Ray)，支持 V2.1
 - 一个通用定时器模块 (GTM)，提供一组强大的数字信号滤波和定时器功能，以实现自主和复杂的输入/输出管理
 - 1 个捕获/比较 6 模块 (两个内核：CCU60 和 CCU61)

- 1个通用12位定时器单元 (GPT120)
- 2个通道外设传感器接口符合V1.3 (PSI5)
- 1个带串行 PHY 的外围传感器接口 (PSI5-S)
- 1个符合 V2.1 的集成电路总线接口 (I2C)
- 1 IEEE802.3以太网 MAC , 带有 RMII 和 MII 接口 (ETH)
- 多功能逐次逼近型 ADC (VADC)
 - 12个独立 ADC 内核集群
 - 输入电压范围为 0 V 至 5.5V (ADC 电源)
- Delta-Sigma ADC (DSADC)
 - 6个通道
- 数字可编程 I/O 端口
- 支持OCDS Level 1 片上调试 (CPU、DMA、片上总线)
- 多核调试、实时跟踪和校准
- 四/五线 JTAG (IEEE 1149.1) 或 DAP (器件访问端口) 接口
- 电源管理系统和片上稳压器
- 带有系统 PLL 和外设 PLL 的时钟生成单元
- 嵌入式电压稳压器
- 符合 AEC-Q100 的汽车应用要求 (仅适用于相应销售代码的交付发布后)
- ISO 26262 安全要素, 不依赖于上下文, 安全要求高达 ASIL D (仅适用于 IFX 发布的“安全包发布说明”中列出的销售代码)

订购信息

英飞凌微控制器的订购代码提供了特定产品的准确参考。此订购代码标识：

- 器件型号本身，即其功能集、温度范围和电源电压
- 封装和交付类型

表 1-1 平台特性概述

Feature		TC37x
CPUs	Type	TC1.6.2
	Cores / Checker Cores	3 / 2
	Max. Freq.	300 MHz
Cache per CPU	Program	32 KB
	Data	16 KB
SRAM per CPU	PSPR	64 KB
	DSPR	240 KB for CPU0,1/ 96 KB else
	DLMU	64 KB
SRAM global	DAM	32 KB
Extension Memory	TCM	-
	XCM	-
	XTM	-
Program Flash	Size	6 MB
	Banks	2 x 3 MB
Data Flash	Size (single-ended)	256 KB (DF0) + 128 KB (DF1)
DMA	Channels	128
CONVCTRL	Modules	1
EVADC	Primary Groups/Channels	4 / 32
	Secondary Groups/Channels	4 / 64
	Fast Compare Channels	4
EDSADC	Channels	6

表 1-1 平台特性概述 (续)

Feature		TC37x
GTM	Clusters	6 (5 @ 200 MHz + 1 @ 100 MHz)
	TIM (8 ch)	6
	TOM (16 ch)	3
	ATOM (8 ch)	6
	MCS (8 ch)	5
	CMU / ICM	1 / 1
	PSM	1
	TBU channels ¹⁾	4 (TBU0-3)
	SPE	2
	CMP / MON	1 / 1
	BRC / DPLL	1 / 1
	CDTM modules	5
	DTM modules	16 (6 on TOM, 10 on ATOM)
Timer	GPT12	1
	CCU6	1
STM	Modules	3
FlexRay	Modules	1
	Channels	2
CAN	Modules	2
	Nodes	2 x 4
	of which support TT-CAN	1
QSPI	Modules	5
	HSCI Channels	0
ASCLIN	Modules	12
I2C	Interfaces	1
SENT	Channels	15
PSI5	Modules	2
PSI5-S	Modules	1
HSSL	Channels	1
MSC	Channels	2
SDMMC	eMMC/SD Interface	-
CIF	Camera Interface	-
Ethernet (10/100Mbit/1Gbit)	Modules	1
FCE	Modules	1
Safety Support	SMU	yes
	IOM	yes
Security	HSM+	1

表 1-1 平台特性概述 (续)

Feature		TC37x
Debug	OCDS	yes
	MCDS	no
	miniMCDS	yes
	miniMCDS TRAM	8 KB
	AGBT	no
Low Power Features	Standby RAM	2
	SCR	yes
Packages	Type	Pad Position Configuration / LFBGA-292 / LQFP-176 /
I/O	Type	5 V CMOS / 3.3 V CMOS / LVDS
T _{ambient}	Range	-40 ... +150°C

TBU3 具有作为角度时钟的特殊用途。

2 TC37x 引脚定义及功能

下图显示了 TC37x 封装版本：

- LFBGA-292 特性封装 TP (图 2-1)
- LQFP-176 用于特性封装 T 和 TP (图 2-2)
- 焊盘框中焊盘排列顺序(章节 2.3)

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

2.1 TC37x TP 的 LFBGA-292 封装引脚

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20				
A	NC1	VEXT	P10.7	P10.6	P10.2	P10.3	P10.0	P11.11	P11.9	P11.2	P13.3	P13.1	P14.8	P14.5	P14.1	P15.6	P15.4	P15.1	VDDP3	VSS	A			
B	P02.0	VSS	VEXT	P10.8	P10.5	P10.4	P10.1	P11.12	P11.10	P11.3	P13.2	P13.0	P14.6	P14.3	P14.4	P14.0	P15.3	VDDP3	VSS	P15.0	B			
C	P02.2	P02.1																	P15.2	P20.14	C			
D	P02.4	P02.3	VSS	VFLEX	P11.15	P11.14	P11.5	P11.6	P11.4	P14.10	P14.9	P14.7	P15.8	P15.7	VDD	VSS			P20.12	P20.13	D			
E	P02.6	P02.5	P02.9	VSS	P11.13	P11.8	P11.7	P11.1	P11.0	P12.1	P12.0	P14.2	P15.5	VDD	VSS	P20.9			P20.10	P20.11	E			
F	P02.8	P02.7	P02.11	P02.10											ESR0	P20.6			P20.7	P20.8	F			
G	P00.0	P00.1	P01.4	P01.3				VDD	VSS	VSS	VSS	VSS	VSS	VDD			ESR1	PURST			P20.1	P20.3	G	
H	P00.2	P00.3	P01.6	P01.5			VDD		VSS	VSS	VSS	VSS		VDD			P21.7 / TDO	P21.6 / TDI			P20.2	P20.0	H	
J	P00.4	P00.5	P00.6	P01.7			VSS	VSS		VSS	VSS		VSS	VSS			TCK	P21.1			P21.3	P21.5	J	
K	P00.7	P00.9	P00.8	P00.10			VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC			TMS	P21.0			P21.2	P21.4	K	
L	P00.11	P00.12	AN43	AN42			VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS			P22.10	P22.11	TRST	VSS			L	
M	AN46	AN47	AN41	AN40			VSS	VSS		VSS	VSS		VSS	VSS			P22.8	P22.9	XTAL2	XTAL1			M	
N	AN44	AN45	AN36 / P40.6	AN38 / P40.8			VDD		VSS	VSS	VSS	VSS		VDD			P22.6	P22.7	VDD	VEXT			N	
P	AN39 / P40.9	AN37 / P40.7	AN32 / P40.4	AN34				VDD	VSS	VSS	VSS	VSS	VDD			P22.4	P22.5			P22.1	P22.0			P
R	AN33 / P40.5	AN35	AN31	AN23											P23.7	P23.6			P22.3	P22.2			R	
T	VAREF 2	VAGND 2	AN30	AN22	AN15	AN12	AN6	AN4	AN0	VEVRS B	P34.2	P34.4	P33.14	P32.5	VSS	P23.5			P23.3	P23.4			T	
U	AN29 / P40.14	AN28 / P40.13	NC1	AN17 / P40.10	AN14	AN9	AN7	AN3	AN1	P34.1	P34.3	P34.5	P33.15	P32.6	P32.7	VSS			P23.1	P23.2			U	
V	AN27 / P40.3	AN26 / P40.2																	VEXT	P23.0			V	
W	AN25 / P40.1	AN24 / P40.0	AN19 / P40.12	AN18 / P40.11	AN16	AN13	AN11	AN8	AN2	P33.0	P33.2	P33.4	P33.6	P33.8	P33.10	P33.12	P32.1 / VGATE 1P	P32.4	VSS	VEXT			W	
Y	NC1	AN21	AN20	VSSM	VDDM	VAREF 1	VAGND 1	AN10	AN5	P33.1	P33.3	P33.5	P33.7	P33.9	P33.11	P33.13	P32.0 / VGATE 1N	P32.2	P32.3	VSS			Y	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20				

TC37xpd - (top view)

图 2-1 TC37x TP 的LFBGA-292封装变体

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-1 端口 P00 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
G1	P00.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN4_10			Mux input channel 4 of TIM module 5
	GTM_TIM3_IN0_1			Mux input channel 0 of TIM module 3
	GTM_TIM2_IN0_1			Mux input channel 0 of TIM module 2
	CCU61_CTRAPA			Trap input capture
	CCU60_T12HRE			External timer start 12
	MSC0_INJ0			Injection signal from port
	GETH_MDIOA			MDIO Input
	P00.0	O0		General-purpose output
	GTM_TOUT9	O1		GTM muxed output
	IOM_REF0_9			Reference input 0
	ASCLIN3_ASCLK	O2		Shift clock output
	ASCLIN3_ATX	O3		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	—	O4		Reserved
	CAN10_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1
	GETH_MDIO	O		MDIO Output

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-1 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
G2	P00.1	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN5_11			Mux input channel 5 of TIM module 5
	GTM_TIM3_IN1_1			Mux input channel 1 of TIM module 3
	GTM_TIM2_IN1_1			Mux input channel 1 of TIM module 2
	CCU60_CC60INB			T12 capture input 60
	ASCLIN3_ARXE			Receive input
	EDSADC_DSCIN5A			Modulator clock input, channel 5
	CAN10_RXDA			CAN receive input node 0
	PSI5_RX0A			RXD inputs (receive data) channel 0
	CCU61_CC60INA			T12 capture input 60
	SENT_SENT0B			Receive input channel 0
	EVADC_G9CH11	AI		Analog input channel 11, group 9
	EDSADC_EDS5NA			Negative analog input channel 5, pin A
	P00.1	O0		General-purpose output
	GTM_TOUT10	O1		GTM muxed output
	IOM_REF0_10			Reference input 0
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	—	O3		Reserved
	EDSADC_DSCOUT5	O4		Modulator clock output
	—	O5		Reserved
	SENT_SPC0	O6		Transmit output
	CCU61_CC60	O7		T12 PWM channel 60
	IOM_MON1_8			Monitor input 1
	IOM_REF1_13			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-1 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
H1	P00.2	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM5_IN6_11			Mux input channel 6 of TIM module 5
	GTM_TIM3_IN1_2			Mux input channel 1 of TIM module 3
	GTM_TIM2_IN1_2			Mux input channel 1 of TIM module 2
	EDSADC_DSDIN5A			Digital datastream input, channel 5
	SENT_SENT1B			Receive input channel 1
	EVADC_G9CH10	AI		Analog input channel 10, group 9
	EDSADC_EDS5PA			Positive analog input channel 5, pin A
	P00.2	O0		General-purpose output
	GTM_TOUT11	O1		GTM muxed output
	IOM_REF0_11			Reference input 0
	ASCLIN3_ASCLK	O2		Shift clock output
	—	O3		Reserved
	PSI5_TX0	O4		TXD outputs (send data)
	IOM_MON1_14			Monitor input 1
	IOM_REF1_14			Reference input 1
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	QSPI3_SLSO4	O6		Master slave select output
	CCU61_COUT60	O7		T12 PWM channel 60
	IOM_MON1_11			Monitor input 1
	IOM_REF1_10			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-1 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
H2	P00.3	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM5_IN7_10			Mux input channel 7 of TIM module 5
	GTM_TIM3_IN2_1			Mux input channel 2 of TIM module 3
	GTM_TIM2_IN2_1			Mux input channel 2 of TIM module 2
	CCU60_CC61INB			T12 capture input 61
	EDSADC_DSCIN3A			Modulator clock input, channel 3
	EDSADC_ITR5F			Trigger/Gate input, channel 5
	PSI5_RX1A			RXD inputs (receive data) channel 1
	CAN03_RXDA			CAN receive input node 3
	PSI5S_RXA			RX data input
	SENT_SENT2B			Receive input channel 2
	CCU61_CC61INA			T12 capture input 61
	EVADC_G9CH9	AI		Analog input channel 9, group 9
	EDSADC_EDS5NB	Negative analog input channel 5, pin B		
	P00.3	O0		General-purpose output
	GTM_TOUT12	O1		GTM muxed output
	IOM_REF0_12			Reference input 0
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	EDSADC_DSCOUT3	O4		Modulator clock output
	—	O5		Reserved
	SENT_SPC2	O6		Transmit output
	CCU61_CC61	O7		T12 PWM channel 61
	IOM_MON1_9			Monitor input 1
	IOM_REF1_12			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-1 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
J1	P00.4	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM3_IN3_1			Mux input channel 3 of TIM module 3
	GTM_TIM2_IN3_1			Mux input channel 3 of TIM module 2
	SCU_E_REQ2_2			ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	SENT_SENT3B			Receive input channel 3
	EDSADC_DSDIN3A			Digital datastream input, channel 3
	EDSADC_SGNA			Carrier sign signal input
	ASCLIN10_ARXA			Receive input
	EVADC_G9CH8	AI		Analog input channel 8, group 9
	EDSADC_EDS5PB	Positive analog input channel 5, pin B		
	P00.4	O0		General-purpose output
	GTM_TOUT13	O1		GTM muxed output
	IOM_REF0_13			Reference input 0
	PSI5S_TX	O2		TX data output
	CAN11_TXD	O3		CAN transmit output node 1
	PSI5_TX1	O4		TXD outputs (send data)
	IOM_MON1_15			Monitor input 1
	—	O5		Reserved
	SENT_SPC3	O6		Transmit output
	CCU61_COUT61	O7		T12 PWM channel 61
	IOM_MON1_12			Monitor input 1
	IOM_REF1_9			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-1 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
J2	P00.5	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM3_IN4_1			Mux input channel 4 of TIM module 3
	GTM_TIM3_IN0_11			Mux input channel 0 of TIM module 3
	GTM_TIM2_IN4_1			Mux input channel 4 of TIM module 2
	CCU60_CC62INB			T12 capture input 62
	EDSADC_DSCIN2A			Modulator clock input, channel 2
	CCU61_CC62INA			T12 capture input 62
	SENT_SENT4B			Receive input channel 4
	CAN11_RXDB			CAN receive input node 1
	GTM_DTMT1_1			CDTM1_DTM0
	EVADC_G9CH7	AI		Analog input channel 7, group 9
	P00.5	O0		General-purpose output
	GTM_TOUT14	O1		GTM muxed output
	IOM_REF0_14			Reference input 0
	EDSADC_CGPWMN	O2		Negative carrier generator output
	QSPI3_SLSO3	O3		Master slave select output
	EDSADC_DSCOUT2	O4		Modulator clock output
	EVADC_FC0BFLOUT	O5		Boundary flag output, FC channel 0
	SENT_SPC4	O6		Transmit output
	CCU61_CC62	O7		T12 PWM channel 62
	IOM_MON1_10			Monitor input 1
	IOM_REF1_11			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-1 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
J4	P00.6	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM3_IN5_1			Mux input channel 5 of TIM module 3
	GTM_TIM3_IN1_14			Mux input channel 1 of TIM module 3
	GTM_TIM2_IN5_1			Mux input channel 5 of TIM module 2
	EDSADC_ITR4F			Trigger/Gate input, channel 4
	EDSADC_DSDIN2A			Digital datastream input, channel 2
	SENT_SENT5B			Receive input channel 5
	ASCLIN5_ARXA			Receive input
	EVADC_G9CH6	AI		Analog input channel 6, group 9
	P00.6	O0		General-purpose output
	GTM_TOUT15	O1		GTM muxed output
	IOM_REF0_15			Reference input 0
	EDSADC_CGPWMP	O2		Positive carrier generator output
	—	O3		Reserved
	—	O4		Reserved
	EVADC_EMUX10	O5		Control of external analog multiplexer interface 1
	SENT_SPC5	O6		Transmit output
	CCU61_COUT62	O7		T12 PWM channel 62
	IOM_MON1_13			Monitor input 1
	IOM_REF1_8			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-1 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
K1	P00.7	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM3_IN6_1			Mux input channel 6 of TIM module 3
	GTM_TIM3_IN2_11			Mux input channel 2 of TIM module 3
	GTM_TIM2_IN6_1			Mux input channel 6 of TIM module 2
	CCU61_CC60INC			T12 capture input 60
	SENT_SENT6B			Receive input channel 6
	EDSADC_DSCIN4A			Modulator clock input, channel 4
	GPT120_T2INA			Trigger/gate input of timer T2
	CCU61_CCPOS0A			Hall capture input 0
	CCU60_T12HRB			External timer start 12
	GTM_DTMT0_2			CDTM0_DTM0
	EVADC_G9CH5	AI		Analog input channel 5, group 9
	EDSADC_EDS4NA			Negative analog input channel 4, pin A
	P00.7	O0		General-purpose output
	GTM_TOUT16	O1		GTM muxed output
	ASCLIN5_ATX	O2		Transmit output
	EVADC_FC2BFLOUT	O3		Boundary flag output, FC channel 2
	EDSADC_DSCOUT4	O4		Modulator clock output
	EVADC_EMUX11	O5		Control of external analog multiplexer interface 1
	SENT_SPC6	O6		Transmit output
	CCU61_CC60	O7		T12 PWM channel 60
	IOM_MON1_8			Monitor input 1
	IOM_REF1_13			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-1 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
K4	P00.8	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM3_IN7_1			Mux input channel 7 of TIM module 3
	GTM_TIM3_IN3_11			Mux input channel 3 of TIM module 3
	GTM_TIM2_IN7_1			Mux input channel 7 of TIM module 2
	CCU61_CC61INC			T12 capture input 61
	SENT_SENT7B			Receive input channel 7
	EDSADC_DSDIN4A			Digital datastream input, channel 4
	GPT120_T2EUDA			Count direction control input of timer T2
	CCU61_CCPOS1A			Hall capture input 1
	CCU60_T13HRB			External timer start 13
	ASCLIN10_ARXB			Receive input
	EVADC_G9CH4	AI		Analog input channel 4, group 9
	EDSADC_EDS4PA			Positive analog input channel 4, pin A
	P00.8	O0		General-purpose output
	GTM_TOUT17	O1		GTM muxed output
	QSPI3_SLSO6	O2		Master slave select output
	ASCLIN10_ATX	O3		Transmit output
	—	O4		Reserved
	EVADC_EMUX12	O5		Control of external analog multiplexer interface 1
	SENT_SPC7	O6		Transmit output
	CCU61_CC61	O7		T12 PWM channel 61
	IOM_MON1_9			Monitor input 1
	IOM_REF1_12			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-1 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
K2	P00.9	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM4_IN0_7			Mux input channel 0 of TIM module 4
	GTM_TIM1_IN0_1			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_1			Mux input channel 0 of TIM module 0
	CCU61_CC62INC			T12 capture input 62
	SENT_SENT8B			Receive input channel 8
	CCU61_CCPOS2A			Hall capture input 2
	EDSADC_DSCIN1A			Modulator clock input, channel 1
	EDSADC_ITR3F			Trigger/Gate input, channel 3
	GPT120_T4EUDA			Count direction control input of timer T4
	CCU60_T13HRC			External timer start 13
	CCU60_T12HRC			External timer start 12
	EVADC_G9CH3	AI		Analog input channel 3, group 9
	EDSADC_EDS4NB			Negative analog input channel 4, pin B
	P00.9	O0		General-purpose output
	GTM_TOUT18	O1		GTM muxed output
	QSPI3_SLSO7	O2		Master slave select output
	ASCLIN3_ARTS	O3		Ready to send output
	EDSADC_DSCOUT1	O4		Modulator clock output
	ASCLIN4_ATX	O5		Transmit output
	SENT_SPC8	O6		Transmit output
	CCU61_CC62	O7		T12 PWM channel 62
	IOM_MON1_10			Monitor input 1
	IOM_REF1_11			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-1 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
K5	P00.10	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM4_IN1_11			Mux input channel 1 of TIM module 4
	GTM_TIM1_IN1_1			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_1			Mux input channel 1 of TIM module 0
	SENT_SENT9B			Receive input channel 9
	EDSADC_DSDIN1A			Digital datastream input, channel 1
	EVADC_G9CH2	AI		Analog input channel 2, group 9
	EDSADC_EDS4PB			Positive analog input channel 4, pin B
	P00.10	O0		General-purpose output
	GTM_TOUT19	O1		GTM muxed output
	ASCLIN4_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	SENT_SPC9	O6		Transmit output
	CCU61_COUT63	O7		T13 PWM channel 63
	IOM_MON1_7			Monitor input 1
	IOM_REF1_7			Reference input 1
L1	P00.11	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM4_IN2_11			Mux input channel 2 of TIM module 4
	GTM_TIM1_IN2_1			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_1			Mux input channel 2 of TIM module 0
	CCU60_CTRAPA			Trap input capture
	EDSADC_DSCIN0A			Modulator clock input, channel 0
	CCU61_T12HRE			External timer start 12
	SENT_SENT10B			Receive input channel 10
	EVADC_G9CH1	AI		Analog input channel 1, group 9
	EVADC_FC3CH0			Analog input FC channel 3
	P00.11	O0		General-purpose output
	GTM_TOUT20	O1		GTM muxed output
	ASCLIN4_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	EDSADC_DSCOUT0	O4		Modulator clock output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-1 端口 P00 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
L2	P00.12	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM4_IN3_11			Mux input channel 3 of TIM module 4
	GTM_TIM1_IN3_1			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_1			Mux input channel 3 of TIM module 0
	ASCLIN3_ACTSA			Clear to send input
	EDSADC_DSDIN0A			Digital datastream input, channel 0
	ASCLIN4_ARXA			Receive input
	SENT_SENT11B			Receive input channel 11
	EVADC_G9CH0	AI		Analog input channel 0, group 9
	EVADC_FC2CH0			Analog input FC channel 2
	P00.12	O0		General-purpose output
	GTM_TOUT21	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU61_COUT63	O7		T13 PWM channel 63
	IOM_MON1_7			Monitor input 1
	IOM_REF1_7			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-2 端口 P01 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
G5	P01.3	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN5_2			Mux input channel 5 of TIM module 4
	GTM_TIM2_IN0_14			Mux input channel 0 of TIM module 2
	GTM_TIM0_IN5_8			Mux input channel 5 of TIM module 0
	QSPI3_SLSIB			Slave select input
	EVADC_G9CH14	AI		Analog input channel 14, group 9
	P01.3	O0		General-purpose output
	GTM_TOUT111	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	QSPI3_SLSO9	O4		Master slave select output
	CAN01_TXD	O5		CAN transmit output node 1
	IOM_MON2_6			Monitor input 2
	IOM_REF2_6			Reference input 2
	—	O6		Reserved
	—	O7		Reserved
G4	P01.4	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN6_2			Mux input channel 6 of TIM module 4
	GTM_TIM2_IN1_14			Mux input channel 1 of TIM module 2
	GTM_TIM0_IN6_8			Mux input channel 6 of TIM module 0
	CAN01_RXDC			CAN receive input node 1
	EVADC_G9CH13	AI		Analog input channel 13, group 9
	P01.4	O0		General-purpose output
	GTM_TOUT112	O1		GTM muxed output
	—	O2		Reserved
	ASCLIN9_ASLSO	O3		Slave select signal output
	QSPI3_SLSO10	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-2 端口 P01 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
H5	P01.5	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN3_2			Mux input channel 3 of TIM module 5
	GTM_TIM2_IN3_7			Mux input channel 3 of TIM module 2
	GTM_TIM2_IN2_7			Mux input channel 2 of TIM module 2
	QSPI3_MRSTC			Master SPI data input
	ASCLIN9_ARXA			Receive input
	EVADC_G9CH12	AI		Analog input channel 12, group 9
	P01.5	O0		General-purpose output
	GTM_TOUT113	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	QSPI3_MRST	O4		Slave SPI data output
	IOM_MON2_3			Monitor input 2
	IOM_REF2_3			Reference input 2
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
H4	P01.6	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN6_2			Mux input channel 6 of TIM module 5
	GTM_TIM5_IN5_3			Mux input channel 5 of TIM module 5
	GTM_TIM2_IN5_7			Mux input channel 5 of TIM module 2
	QSPI3_MTSRC			Slave SPI data input
	P01.6	O0		General-purpose output
	GTM_TOUT114	O1		GTM muxed output
	—	O2		Reserved
	ASCLIN9_ASCLK	O3		Shift clock output
	QSPI3_MTSR	O4		Master SPI data output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-2 端口 P01 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
J5	P01.7	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN7_2			Mux input channel 7 of TIM module 5
	GTM_TIM2_IN7_7			Mux input channel 7 of TIM module 2
	QSPI3_SCLKC			Slave SPI clock inputs
	ASCLIN9_ARXB			Receive input
	P01.7	O0		General-purpose output
	GTM_TOUT115	O1		GTM muxed output
	—	O2		Reserved
	ASCLIN9_ATX	O3		Transmit output
	QSPI3_SCLK	O4		Master SPI clock output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-3 端口 P02 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
B1	P02.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_2			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_2			Mux input channel 0 of TIM module 0
	CCU61_CC60INB			T12 capture input 60
	ASCLIN2_ARXG			Receive input
	CCU60_CC60INA			T12 capture input 60
	SCU_E_REQ3_2			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	GTM_DTMA0_0			CDTM0_DTM4
	P02.0	O0		General-purpose output
	GTM_TOUT0	O1		GTM muxed output
	IOM_REF0_0			Reference input 0
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI3_SLSO1	O3		Master slave select output
	EDSADC_CGPWMN	O4		Negative carrier generator output
	CAN00_TXD	O5		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	ERAY0_TXDA	O6		Transmit Channel A
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
	IOM_REF1_6			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-3 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
C2	P02.1	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_2			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_2			Mux input channel 1 of TIM module 0
	ERAY0_RXDA2			Receive Channel A2
	ASCLIN2_ARXB			Receive input
	CAN00_RXDA			CAN receive input node 0
	SCU_E_REQ2_1			ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P02.1	O0		General-purpose output
	GTM_TOUT1	O1		GTM muxed output
	IOM_REF0_1			Reference input 0
	QSPI4_SLSO7	O2		Master slave select output
	QSPI3_SLSO2	O3		Master slave select output
	EDSADC_CGPWMP	O4		Positive carrier generator output
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT60	O7		T12 PWM channel 60
	IOM_MON1_3			Monitor input 1
	IOM_REF1_3			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-3 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
C1	P02.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_2			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_2			Mux input channel 2 of TIM module 0
	CCU61_CC61INB			T12 capture input 61
	CCU60_CC61INA			T12 capture input 61
	SENT_SENT14B			Receive input channel 14
	P02.2	O0		General-purpose output
	GTM_TOUT2	O1		GTM muxed output
	IOM_REF0_2			Reference input 0
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI3_SLSO3	O3		Master slave select output
	PSI5_TX0	O4		TXD outputs (send data)
	IOM_MON1_14			Monitor input 1
	IOM_REF1_14			Reference input 1
	CAN02_TXD	O5		CAN transmit output node 2
	IOM_MON2_7			Monitor input 2
	IOM_REF2_7			Reference input 2
	ERAY0_TXDB	O6		Transmit Channel B
	CCU60_CC61	O7		T12 PWM channel 61
	IOM_MON1_1			Monitor input 1
	IOM_REF1_5			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-3 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
D2	P02.3	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN3_2			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_2			Mux input channel 3 of TIM module 0
	EDSADC_DSCIN5B			Modulator clock input, channel 5
	ERAY0_RXDB2			Receive Channel B2
	CAN02_RXDB			CAN receive input node 2
	ASCLIN1_ARXG			Receive input
	MSC1_SDI1			Upstream asynchronous input signal
	PSI5_RX0B			RXD inputs (receive data) channel 0
	SENT_SENT13B			Receive input channel 13
	P02.3	O0		General-purpose output
	GTM_TOUT3	O1		GTM muxed output
	IOM_REF0_3			Reference input 0
	ASCLIN2_ASLSO	O2		Slave select signal output
	QSPI3_SLSO4	O3		Master slave select output
	EDSADC_DSCOUT5	O4		Modulator clock output
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT61	O7		T12 PWM channel 61
	IOM_MON1_4			Monitor input 1
	IOM_REF1_2			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-3 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
D1	P02.4	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN4_1			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_1			Mux input channel 4 of TIM module 0
	CCU61_CC62INB			T12 capture input 62
	EDSADC_DSDIN5B			Digital datastream input, channel 5
	QSPI3_SLSIA			Slave select input
	CCU60_CC62INA			T12 capture input 62
	I2C0_SDAA			Serial Data Input 0
	CAN11_RXDA			CAN receive input node 1
	CAN0_ECTT1			External CAN time trigger input
	SENT_SENT12B			Receive input channel 12
	P02.4	O0		General-purpose output
	GTM_TOUT4	O1		GTM muxed output
	IOM_REF0_4			Reference input 0
	ASCLIN2_ASCLK	O2		Shift clock output
	QSPI3_SLSO0	O3		Master slave select output
	PSI5S_CLK	O4		PSI5S CLK is a clock that can be used on a pin to drive the external PHY.
	I2C0_SDA	O5		Serial Data Output
	ERAY0_TXENA	O6		Transmit Enable Channel A
	CCU60_CC62	O7		T12 PWM channel 62
	IOM_MON1_0			Monitor input 1
	IOM_REF1_4			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-3 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
E2	P02.5	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN5_1			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_1			Mux input channel 5 of TIM module 0
	EDSADC_DSCIN4B			Modulator clock input, channel 4
	I2C0_SCLA			Serial Clock Input 0
	PSI5_RX1B			RXD inputs (receive data) channel 1
	PSI5S_RXB			RX data input
	QSPI3_MRSTA			Master SPI data input
	SENT_SENT3C			Receive input channel 3
	CAN0_ECTT2			External CAN time trigger input
	P02.5	O0		General-purpose output
	GTM_TOUT5	O1		GTM muxed output
	IOM_REF0_5			Reference input 0
	CAN11_TXD	O2		CAN transmit output node 1
	QSPI3_MRST	O3		Slave SPI data output
	IOM_MON2_3			Monitor input 2
	IOM_REF2_3			Reference input 2
	EDSADC_DSCOUT4	O4		Modulator clock output
	I2C0_SCL	O5		Serial Clock Output
	ERAY0_TXENB	O6		Transmit Enable Channel B
	CCU60_COUT62	O7		T12 PWM channel 62
	IOM_MON1_5			Monitor input 1
	IOM_REF1_1			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-3 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
E1	P02.6	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN0_10			Mux input channel 0 of TIM module 3
	GTM_TIM1_IN6_1			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_1			Mux input channel 6 of TIM module 0
	CCU60_CC60INC			T12 capture input 60
	SENT_SENT2C			Receive input channel 2
	EDSADC_DSDIN4B			Digital datastream input, channel 4
	EDSADC_ITR5E			Trigger/Gate input, channel 5
	GPT120_T3INA			Trigger/gate input of core timer T3
	CCU60_CCPOS0A			Hall capture input 0
	CCU61_T12HRB			External timer start 12
	QSPI3_MTSRA			Slave SPI data input
	P02.6	O0		General-purpose output
	GTM_TOUT6	O1		GTM muxed output
	IOM_REF0_6			Reference input 0
	PSI5S_TX	O2		TX data output
	QSPI3_MTSR	O3		Master SPI data output
	PSI5_TX1	O4		TXD outputs (send data)
	IOM_MON1_15			Monitor input 1
	EVADC_EMUX00	O5		Control of external analog multiplexer interface 0
	—	O6		Reserved
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
	IOM_REF1_6			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-3 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
F2	P02.7	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN1_10			Mux input channel 1 of TIM module 3
	GTM_TIM1_IN7_1			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_1			Mux input channel 7 of TIM module 0
	CCU60_CC61INC			T12 capture input 61
	SENT_SENT1C			Receive input channel 1
	EDSADC_DSCIN3B			Modulator clock input, channel 3
	EDSADC_ITR4E			Trigger/Gate input, channel 4
	GPT120_T3EUDA			Count direction control input of core timer T3
	CCU60_CCPOS1A			Hall capture input 1
	QSPI3_SCLKA			Slave SPI clock inputs
	CCU61_T13HRB			External timer start 13
	P02.7	O0		General-purpose output
	GTM_TOUT7	O1		GTM muxed output
	IOM_REF0_7			Reference input 0
	—	O2		Reserved
	QSPI3_SCLK	O3		Master SPI clock output
	EDSADC_DSCOUT3	O4		Modulator clock output
	EVADC_EMUX01	O5		Control of external analog multiplexer interface 0
	SENT_SPC1	O6		Transmit output
	CCU60_CC61	O7		T12 PWM channel 61
	IOM_MON1_1			Monitor input 1
	IOM_REF1_5			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-3 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
F1	P02.8	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN2_10			Mux input channel 2 of TIM module 3
	GTM_TIM3_IN0_2			Mux input channel 0 of TIM module 3
	GTM_TIM2_IN0_2			Mux input channel 0 of TIM module 2
	CCU60_CC62INC			T12 capture input 62
	SENT_SENT0C			Receive input channel 0
	CCU60_CCPOS2A			Hall capture input 2
	EDSADC_DSDIN3B			Digital datastream input, channel 3
	EDSADC_ITR3E			Trigger/Gate input, channel 3
	GPT120_T4INA			Trigger/gate input of timer T4
	CCU61_T12HRC			External timer start 12
	CCU61_T13HRC			External timer start 13
	GTM_DTMA0_1			CDTM0_DTM4
	P02.8			O0
	GTM_TOUT8	O1	GTM muxed output	
	IOM_REF0_8		Reference input 0	
	QSPI3_SLSO5	O2	Master slave select output	
	ASCLIN8_ASCLK	O3	Shift clock output	
	—	O4	Reserved	
	EVADC_EMUX02	O5	Control of external analog multiplexer interface 0	
	GETH_MDC	O6	MDIO clock	
	CCU60_CC62	O7	T12 PWM channel 62	
	IOM_MON1_0		Monitor input 1	
	IOM_REF1_4		Reference input 1	

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-3 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
E4	P02.9	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN2_2			Mux input channel 2 of TIM module 4
	GTM_TIM3_IN3_10			Mux input channel 3 of TIM module 3
	GTM_TIM0_IN2_10			Mux input channel 2 of TIM module 0
	ASCLIN8_ARXA			Receive input
	P02.9	O0		General-purpose output
	GTM_TOUT116	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	ASCLIN8_ATX	O3		Transmit output
	—	O4		Reserved
	CAN01_TXD	O5		CAN transmit output node 1
	IOM_MON2_6			Monitor input 2
	IOM_REF2_6			Reference input 2
	—	O6		Reserved
	—	O7		Reserved
F5	P02.10	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN3_2			Mux input channel 3 of TIM module 4
	GTM_TIM3_IN4_11			Mux input channel 4 of TIM module 3
	GTM_TIM0_IN3_10			Mux input channel 3 of TIM module 0
	ASCLIN2_ARXC			Receive input
	CAN01_RXDE			CAN receive input node 1
	ASCLIN8_ARXB			Receive input
	P02.10	O0		General-purpose output
	GTM_TOUT117	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-3 端口 P02 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
F4	P02.11	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN4_3			Mux input channel 4 of TIM module 4
	GTM_TIM3_IN5_12			Mux input channel 5 of TIM module 3
	GTM_TIM0_IN7_7			Mux input channel 7 of TIM module 0
	EVADC_G9CH15	AI		Analog input channel 15, group 9
	P02.11	O0		General-purpose output
	GTM_TOUT118	O1		GTM muxed output
	—	O2		Reserved
	ASCLIN8_ASLSO	O3		Slave select signal output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-4 端口 P10 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
A7	P10.0	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN0_12			Mux input channel 0 of TIM module 4
	GTM_TIM1_IN4_2			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_2			Mux input channel 4 of TIM module 0
	GPT120_T6EUIDB			Count direction control input of core timer T6
	ASCLIN11_ARXA			Receive input
	GETH_RXERC			Receive Error MII
	P10.0	O0		General-purpose output
	GTM_TOUT102	O1		GTM muxed output
	ASCLIN11_ATX	O2		Transmit output
	QSPI1_SLSO10	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-4 端口 P10 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
B7	P10.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN4_12			Mux input channel 4 of TIM module 4
	GTM_TIM1_IN1_3			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_3			Mux input channel 1 of TIM module 0
	GPT120_T5EUDB			Count direction control input of timer T5
	QSPI1_MRSTA			Master SPI data input
	GTM_DTMT0_1			CDTM0_DTM0
	P10.1	O0		General-purpose output
	GTM_TOUT103	O1		GTM muxed output
	QSPI1_MTSR	O2		Master SPI data output
	QSPI1_MRST	O3		Slave SPI data output
	IOM_MON2_1			Monitor input 2
	IOM_REF2_1			Reference input 2
	MSC0_EN1	O4		Chip Select
	EVADC_FC1BFLOUT	O5		Boundary flag output, FC channel 1
	—	O6		Reserved
	—	O7		Reserved
A5	P10.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN5_12			Mux input channel 5 of TIM module 4
	GTM_TIM1_IN2_3			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_3			Mux input channel 2 of TIM module 0
	CAN02_RXDE			CAN receive input node 2
	MSC0_SDI1			Upstream asynchronous input signal
	QSPI1_SCLKA			Slave SPI clock inputs
	GPT120_T6INB			Trigger/gate input of core timer T6
	SCU_E_REQ2_0			ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	GTM_DTMT2_2			CDTM2_DTM0
	P10.2	O0		General-purpose output
	GTM_TOUT104	O1		GTM muxed output
	IOM_MON2_9			Monitor input 2
	—	O2		Reserved
	QSPI1_SCLK	O3		Master SPI clock output
	MSC0_EN0	O4		Chip Select
	EVADC_FC3BFLOUT	O5		Boundary flag output, FC channel 3
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-4 端口 P10 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A6	P10.3	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN6_10			Mux input channel 6 of TIM module 4
	GTM_TIM1_IN3_3			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_3			Mux input channel 3 of TIM module 0
	QSPI1_MTSRA			Slave SPI data input
	SCU_E_REQ3_0			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	GPT120_T5INB			Trigger/gate input of timer T5
	P10.3	O0		General-purpose output
	GTM_TOUT105	O1		GTM muxed output
	IOM_MON2_10			Monitor input 2
	—	O2		Reserved
	QSPI1_MTSR	O3		Master SPI data output
	MSC0_EN0	O4		Chip Select
	—	O5		Reserved
	CAN02_TXD	O6		CAN transmit output node 2
	IOM_MON2_7			Monitor input 2
	IOM_REF2_7			Reference input 2
	—	O7		Reserved
B6	P10.4	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN7_3			Mux input channel 7 of TIM module 4
	GTM_TIM1_IN6_2			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_2			Mux input channel 6 of TIM module 0
	QSPI1_MTSRC			Slave SPI data input
	CCU60_CCPOS0C			Hall capture input 0
	GPT120_T3INB			Trigger/gate input of core timer T3
	ASCLIN11_ARXB			Receive input
	P10.4	O0		General-purpose output
	GTM_TOUT106	O1		GTM muxed output
	IOM_MON2_11			Monitor input 2
	—	O2		Reserved
	QSPI1_SLSO8	O3		Master slave select output
	QSPI1_MTSR	O4		Master SPI data output
	MSC0_EN0	O5		Chip Select
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-4 端口 P10 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
B5	P10.5	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM4_IN3_13			Mux input channel 3 of TIM module 4
	GTM_TIM1_IN2_4			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_4			Mux input channel 2 of TIM module 0
	PMS_HWCFG4IN			HWCFG4 pin input
	MSC0_INJ1			Injection signal from port
	P10.5	O0		General-purpose output
	GTM_TOUT107	O1		GTM muxed output
	IOM_REF2_9			Reference input 2
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI3_SLSO8	O3		Master slave select output
	QSPI1_SLSO9	O4		Master slave select output
	GPT120_T6OUT	O5		External output for overflow/underflow detection of core timer T6
	ASCLIN2_ASLSO	O6		Slave select signal output
	—	O7		Reserved
A4	P10.6	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM4_IN2_13			Mux input channel 2 of TIM module 4
	GTM_TIM1_IN3_4			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_4			Mux input channel 3 of TIM module 0
	ASCLIN2_ARXD			Receive input
	QSPI3_MTSRB			Slave SPI data input
	PMS_HWCFG5IN			HWCFG5 pin input
	P10.6	O0		General-purpose output
	GTM_TOUT108	O1		GTM muxed output
	IOM_REF2_10			Reference input 2
	ASCLIN2_ASCLK	O2		Shift clock output
	QSPI3_MTSR	O3		Master SPI data output
	GPT120_T3OUT	O4		External output for overflow/underflow detection of core timer T3
	—	O5		Reserved
	QSPI1_MRST	O6		Slave SPI data output
	IOM_MON2_1			Monitor input 2
	IOM_REF2_1			Reference input 2
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-4 端口 P10 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A3	P10.7	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_3			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_3			Mux input channel 0 of TIM module 0
	GPT120_T3EUDB			Count direction control input of core timer T3
	ASCLIN2_ACTSA			Clear to send input
	QSPI3_MRSTB			Master SPI data input
	SCU_E_REQ0_2			ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	CCU60_CCPOS1C			Hall capture input 1
	P10.7	O0		General-purpose output
	GTM_TOUT109	O1		GTM muxed output
	IOM_REF2_11			Reference input 2
	—	O2		Reserved
	QSPI3_MRST	O3		Slave SPI data output
	IOM_MON2_3			Monitor input 2
	IOM_REF2_3			Reference input 2
	—	O4		Reserved
	—	O5		Reserved
	CAN12_TXD	O6		CAN transmit output node 2
	—	O7		Reserved
B4	P10.8	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN0_13			Mux input channel 0 of TIM module 4
	GTM_TIM1_IN5_2			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_2			Mux input channel 5 of TIM module 0
	CAN12_RXDB			CAN receive input node 2
	GPT120_T4INB			Trigger/gate input of timer T4
	QSPI3_SCLKB			Slave SPI clock inputs
	SCU_E_REQ1_2			ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	CCU60_CCPOS2C			Hall capture input 2
	P10.8	O0		General-purpose output
	GTM_TOUT110	O1		GTM muxed output
	ASCLIN2_ARTS	O2		Ready to send output
	QSPI3_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-5 端口 P11 的功能

Ball	Symbol	Ctrl.	Buffer Type	Function
E10	P11.0	I	RFAST / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM4_IN0_4			Mux input channel 0 of TIM module 4
	GTM_TIM2_IN0_7			Mux input channel 0 of TIM module 2
	ASCLIN3_ARXB			Receive input
	GTM_DTMA2_1			CDTM2_DTM4
	P11.0	O0		General-purpose output
	GTM_TOUT119	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	—	O3		Reserved
	—	O4		Reserved
	CAN11_TXD	O5		CAN transmit output node 1
	GETH_TXD3	O6		Transmit Data
	—	O7		Reserved
E9	P11.1	I	RFAST / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM4_IN1_5			Mux input channel 1 of TIM module 4
	GTM_TIM2_IN1_6			Mux input channel 1 of TIM module 2
	P11.1	O0		General-purpose output
	GTM_TOUT120	O1		GTM muxed output
	ASCLIN3_ASCLK	O2		Shift clock output
	ASCLIN3_ATX	O3		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	—	O4		Reserved
	CAN12_TXD	O5		CAN transmit output node 2
	GETH_TXD2	O6		Transmit Data
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-5 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A10	P11.2	I	RFAST / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM3_IN1_3			Mux input channel 1 of TIM module 3
	GTM_TIM2_IN1_3			Mux input channel 1 of TIM module 2
	P11.2	O0		General-purpose output
	GTM_TOUT95	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO5	O3		Master slave select output
	QSPI1_SLSO5	O4		Master slave select output
	MSC0_EN1	O5		Chip Select
	GETH_TXD1	O6		Transmit Data
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1
B10	P11.3	I	RFAST / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM3_IN2_2			Mux input channel 2 of TIM module 3
	GTM_TIM2_IN2_2			Mux input channel 2 of TIM module 2
	MSC0_SDI3			Upstream assynchronous input signal
	QSPI1_MRSTB			Master SPI data input
	P11.3	O0		General-purpose output
	GTM_TOUT96	O1		GTM muxed output
	—	O2		Reserved
	QSPI1_MRST	O3		Slave SPI data output
	IOM_MON2_1			Monitor input 2
	IOM_REF2_1			Reference input 2
	ERAY0_TXDA	O4		Transmit Channel A
	—	O5		Reserved
	GETH_TXD0	O6		Transmit Data
	CCU60_COUT62	O7		T12 PWM channel 62
	IOM_MON1_5			Monitor input 1
	IOM_REF1_1			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-5 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
D10	P11.4	I	RFAST / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM4_IN2_5			Mux input channel 2 of TIM module 4
	GTM_TIM2_IN2_6			Mux input channel 2 of TIM module 2
	GETH_RXCLKB			Receive Clock MII
	P11.4	O0		General-purpose output
	GTM_TOUT121	O1		GTM muxed output
	ASCLIN3_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	CAN13_TXD	O5		CAN transmit output node 3
	GETH_TXER	O6		Transmit Error MII
	GETH_TXCLK	O7		Transmit Clock Output for RGMII
D8	P11.5	I	SLOW / RGMII_In put / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM4_IN3_5			Mux input channel 3 of TIM module 4
	GTM_TIM2_IN3_8			Mux input channel 3 of TIM module 2
	GETH_TXCLKA			Transmit Clock Input for MII
	GETH_GREFCLK			Gigabit Reference Clock input for RGMII (125 MHz high precision)
	P11.5	O0		General-purpose output
	GTM_TOUT122	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-5 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
D9	P11.6	I	RFAST / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM3_IN3_2			Mux input channel 3 of TIM module 3
	GTM_TIM2_IN3_2			Mux input channel 3 of TIM module 2
	QSPI1_SCLKB			Slave SPI clock inputs
	P11.6	O0		General-purpose output
	GTM_TOUT97	O1		GTM muxed output
	ERAY0_TXENB	O2		Transmit Enable Channel B
	QSPI1_SCLK	O3		Master SPI clock output
	ERAY0_TXENA	O4		Transmit Enable Channel A
	MSC0_FCLP	O5		Shift-clock direct part of the differential signal
	GETH_TXEN	O6		Transmit Enable MII and RMII
	GETH_TCTL			Transmit Control for RGMII
	CCU60_COUT61			T12 PWM channel 61
	IOM_MON1_4	O7		Monitor input 1
	IOM_REF1_2			Reference input 1
E8	P11.7	I	SLOW / RGMII_In put / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM4_IN4_5			Mux input channel 4 of TIM module 4
	GTM_TIM2_IN4_7			Mux input channel 4 of TIM module 2
	GETH_RXD3A			Receive Data 3 MII and RGMII (RGMII can use RXD3A only)
	CAN11_RXDD			CAN receive input node 1
	P11.7	O0		General-purpose output
	GTM_TOUT123	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-5 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
E7	P11.8	I	SLOW / RGMII_In put / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM4_IN5_5			Mux input channel 5 of TIM module 4
	GTM_TIM2_IN5_8			Mux input channel 5 of TIM module 2
	GETH_RXD2A			Receive Data 2 MII and RGMII (RGMII can use RXD2A only)
	CAN12_RXDD			CAN receive input node 2
	P11.8	O0		General-purpose output
	GTM_TOUT124	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
A9	P11.9	I	FAST / RGMII_In put / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM3_IN4_2			Mux input channel 4 of TIM module 3
	GTM_TIM2_IN4_2			Mux input channel 4 of TIM module 2
	QSPI1_MTSRB			Slave SPI data input
	ERAY0_RXDA1			Receive Channel A1
	GETH_RXD1A			Receive Data 1 MII, RMII and RGMII (RGMII can use RXD1A only)
	P11.9	O0		General-purpose output
	GTM_TOUT98	O1		GTM muxed output
	—	O2		Reserved
	QSPI1_MTSR	O3		Master SPI data output
	—	O4		Reserved
	MSC0_SOP	O5		Data output - direct part of the differential signal
	—	O6		Reserved
	CCU60_COUT60	O7		T12 PWM channel 60
	IOM_MON1_3			Monitor input 1
	IOM_REF1_3			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-5 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
B9	P11.10	I	FAST / RGMII_Input / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM3_IN5_2			Mux input channel 5 of TIM module 3
	GTM_TIM2_IN5_2			Mux input channel 5 of TIM module 2
	GTM_TIM2_IN0_9			Mux input channel 0 of TIM module 2
	CAN03_RXDD			CAN receive input node 3
	ERAY0_RXDB1			Receive Channel B1
	ASCLIN1_ARXE			Receive input
	SCU_E_REQ6_3			ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	MSC0_SDI0			Upstream assynchronous input signal
	GETH_RXD0A			Receive Data 0 MII, RMII and RGMII (RGMII can use RXD0A only)
	QSPI1_SLSIA	Slave select input		
	P11.10	O0		General-purpose output
	GTM_TOUT99	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO3	O3		Master slave select output
	QSPI1_SLSO3	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	CCU60_CC62	O7		T12 PWM channel 62
	IOM_MON1_0			Monitor input 1
IOM_REF1_4	Reference input 1			

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-5 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A8	P11.11	I	FAST / RGMII_In put / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM3_IN6_2			Mux input channel 6 of TIM module 3
	GTM_TIM3_IN0_14			Mux input channel 0 of TIM module 3
	GTM_TIM2_IN6_2			Mux input channel 6 of TIM module 2
	GETH_CRSDVA			Carrier Sense / Data Valid combi-signal for RMII
	GETH_RXDVA			Receive Data Valid MII
	GETH_CRSB			Carrier Sense MII
	GETH_RCTLA			Receive Control for RGMII
	P11.11	O0		General-purpose output
	GTM_TOUT100	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO4	O3		Master slave select output
	QSPI1_SLSO4	O4		Master slave select output
	MSC0_EN0	O5		Chip Select
	ERAY0_TXENB	O6		Transmit Enable Channel B
	CCU60_CC61	O7		T12 PWM channel 61
	IOM_MON1_1			Monitor input 1
	IOM_REF1_5			Reference input 1
B8	P11.12	I	FAST / RGMII_In put / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM3_IN7_2			Mux input channel 7 of TIM module 3
	GTM_TIM2_IN7_2			Mux input channel 7 of TIM module 2
	GETH_REFCLKA			Reference Clock input for RMII (50 MHz)
	GETH_TXCLKB			Transmit Clock Input for MII
	GETH_RXCLKA			Receive Clock MII
	P11.12	O0		General-purpose output
	GTM_TOUT101	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	GTM_CLK2	O3		CGM generated clock
	ERAY0_TXDB	O4		Transmit Channel B
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	CCU_EXTCLK1	O6		External Clock 1
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
	IOM_REF1_6			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-5 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
E6	P11.13	I	SLOW / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM4_IN6_5			Mux input channel 6 of TIM module 4
	GTM_TIM2_IN6_7			Mux input channel 6 of TIM module 2
	GETH_RXERA			Receive Error MII
	CAN13_RXDD			CAN receive input node 3
	P11.13	O0		General-purpose output
	GTM_TOUT125	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O7		Reserved
D7	P11.14	I	SLOW / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM4_IN7_4			Mux input channel 7 of TIM module 4
	GTM_TIM2_IN7_8			Mux input channel 7 of TIM module 2
	GETH_CRSDVB			Carrier Sense / Data Valid combi-signal for RMII
	GETH_RXDVB			Receive Data Valid MII
	GETH_CRSA			Carrier Sense MII
	P11.14	O0		General-purpose output
	GTM_TOUT126	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-5 端口 P11 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
D6	P11.15	I	SLOW / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM4_IN7_5			Mux input channel 7 of TIM module 4
	GTM_TIM0_IN7_8			Mux input channel 7 of TIM module 0
	GETH_COLA			Collision MII
	P11.15	O0		General-purpose output
	GTM_TOUT127	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-6 端口 P12 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
E12	P12.0	I	SLOW / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM4_IN0_5			Mux input channel 0 of TIM module 4
	GTM_TIM3_IN0_7			Mux input channel 0 of TIM module 3
	CAN00_RXDC			CAN receive input node 0
	GETH_RXCLKC			Receive Clock MII
	GTM_DTMA4_0			CDTM4_DTM4
	P12.0	O0		General-purpose output
	GTM_TOUT128	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	GETH_MDC	O6		MDIO clock
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-6 端口 P12 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
E11	P12.1	I	SLOW / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM4_IN1_6			Mux input channel 1 of TIM module 4
	GTM_TIM3_IN1_6			Mux input channel 1 of TIM module 3
	GETH_MDIOC			MDIO Input
	P12.1	O0		General-purpose output
	GTM_TOUT129	O1		GTM muxed output
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	CAN00_TXD	O5		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	—	O6		Reserved
	—	O7		Reserved
	GETH_MDIO	O		MDIO Output

表 2-7 端口 P13 的功能

Ball	Symbol	Ctrl.	Buffer Type	Function
B12	P13.0	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM3_IN5_3			Mux input channel 5 of TIM module 3
	GTM_TIM2_IN5_3			Mux input channel 5 of TIM module 2
	ASCLIN10_ARXC			Receive input
	P13.0	O0		General-purpose output
	GTM_TOUT91	O1		GTM muxed output
	ASCLIN10_ATX	O2		Transmit output
	QSPI2_SCLKN	O3		Master SPI clock output (LVDS N line)
	MSC0_EN1	O4		Chip Select
	MSC0_FCLN	O5		Shift-clock inverted part of the differential signal
	—	O6		Reserved
	CAN10_TXD	O7		CAN transmit output node 0

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-7 端口 P13 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A12	P13.1	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM3_IN6_3			Mux input channel 6 of TIM module 3
	GTM_TIM2_IN6_3			Mux input channel 6 of TIM module 2
	I2C0_SCLB			Serial Clock Input 1
	CAN10_RXDD			CAN receive input node 0
	ASCLIN10_ARXD			Receive input
	P13.1	O0		General-purpose output
	GTM_TOUT92	O1		GTM muxed output
	—	O2		Reserved
	QSPI2_SCLKP	O3		Master SPI clock output (LVDS P line)
	—	O4		Reserved
	MSC0_FCLP	O5		Shift-clock direct part of the differential signal
	I2C0_SCL	O6		Serial Clock Output
	—	O7		Reserved
B11	P13.2	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM3_IN7_3			Mux input channel 7 of TIM module 3
	GTM_TIM2_IN7_3			Mux input channel 7 of TIM module 2
	GPT120_CAPINA			Trigger input to capture value of timer T5 into CAPREL register
	I2C0_SDAB			Serial Data Input 1
	P13.2	O0		General-purpose output
	GTM_TOUT93	O1		GTM muxed output
	ASCLIN10_ASCLK	O2		Shift clock output
	QSPI2_MTSRN	O3		Master SPI data output (LVDS N line)
	MSC0_FCLP	O4		Shift-clock direct part of the differential signal
	MSC0_SON	O5		Data output - inverted part of the differential signal
	I2C0_SDA	O6		Serial Data Output
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-7 端口 P13 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A11	P13.3	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM3_IN0_3			Mux input channel 0 of TIM module 3
	GTM_TIM2_IN0_3			Mux input channel 0 of TIM module 2
	P13.3	O0		General-purpose output
	GTM_TOUT94	O1		GTM muxed output
	ASCLIN10_ASLSO	O2		Slave select signal output
	QSPI2_MTSRP	O3		Master SPI data output (LVDS P line)
	—	O4		Reserved
	MSC0_SOP	O5		Data output - direct part of the differential signal
	—	O6		Reserved
	—	O7		Reserved

表 2-8 端口 P14 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
B16	P14.0	I	FAST / PU1 / VEXT / ES2	General-purpose input
	GTM_TIM1_IN3_5			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_5			Mux input channel 3 of TIM module 0
	P14.0	O0		General-purpose output
	GTM_TOUT80	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	ERAY0_TXDA	O3		Transmit Channel A
	ERAY0_TXDB	O4		Transmit Channel B
	CAN01_TXD	O5		CAN transmit output node 1
	IOM_MON2_6			Monitor input 2
	IOM_REF2_6			Reference input 2
	ASCLIN0_ASCLK	O6		Shift clock output
	CCU60_COUT62	O7		T12 PWM channel 62
	IOM_MON1_5			Monitor input 1
	IOM_REF1_1			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-8 端口 P14 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A15	P14.1	I	FAST / PU1 / VEXT / ES2	General-purpose input
	GTM_TIM1_IN4_3			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_3			Mux input channel 4 of TIM module 0
	ERAY0_RXDA3			Receive Channel A3
	ASCLIN0_ARXA			Receive input
	ERAY0_RXDB3			Receive Channel B3
	CAN01_RXDB			CAN receive input node 1
	SCU_E_REQ3_1			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	PMS_PINAWKP			PINA (P14.1) pin input
	P14.1	O0		General-purpose output
	GTM_TOUT81	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1
E13	P14.2	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN5_3			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_3			Mux input channel 5 of TIM module 0
	PMS_HWCFG2IN			HWCFG2 pin input
	P14.2	O0		General-purpose output
	GTM_TOUT82	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI2_SLSO1	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	ASCLIN2_ASCLK	O6		Shift clock output
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-8 端口 P14 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
B14	P14.3	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_3			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_3			Mux input channel 6 of TIM module 0
	PMS_HWCFG3IN			HWCFG3 pin input
	ASCLIN2_ARXA			Receive input
	MSC0_SDI2			Upstream assynchronous input signal
	SCU_E_REQ1_0			ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P14.3	O0		General-purpose output
	GTM_TOUT83	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI2_SLSO3	O3		Master slave select output
	ASCLIN1_ASLSO	O4		Slave select signal output
	ASCLIN3_ASLSO	O5		Slave select signal output
	—	O6		Reserved
	—	O7		Reserved
B15	P14.4	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN7_2			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_2			Mux input channel 7 of TIM module 0
	PMS_HWCFG6IN			HWCFG6 pin input
	GTM_DTMT0_0			CDTM0_DTM0
	P14.4	O0		General-purpose output
	GTM_TOUT84	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	GETH_PPS	O6		Pulse Per Second
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-8 端口 P14 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A14	P14.5	I	FAST / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_4			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_4			Mux input channel 0 of TIM module 0
	PMS_HWCFG1IN			HWCFG1 pin input
	GTM_DTMA2_0			CDTM2_DTM4
	P14.5	O0		General-purpose output
	GTM_TOUT85	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	ERAY0_TXDB	O6		Transmit Channel B
	—	O7		Reserved
B13	P14.6	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_4			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_4			Mux input channel 1 of TIM module 0
	P14.6	O0		General-purpose output
	GTM_TOUT86	O1		GTM muxed output
	—	O2		Reserved
	QSPI2_SLSO2	O3		Master slave select output
	CAN13_TXD	O4		CAN transmit output node 3
	—	O5		Reserved
	ERAY0_TXENB	O6		Transmit Enable Channel B
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-8 端口 P14 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
D13	P14.7	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN7_10			Mux input channel 7 of TIM module 4
	GTM_TIM1_IN0_5			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_5			Mux input channel 0 of TIM module 0
	ERAY0_RXDB0			Receive Channel B0
	CAN10_RXDB			CAN receive input node 0
	CAN13_RXDA			CAN receive input node 3
	ASCLIN9_ARXC			Receive input
	P14.7	O0		General-purpose output
	GTM_TOUT87	O1		GTM muxed output
	ASCLIN0_ARTS	O2		Ready to send output
	QSPI2_SLSO4	O3		Master slave select output
	ASCLIN9_ATX	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
A13	P14.8	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN2_3			Mux input channel 2 of TIM module 3
	GTM_TIM2_IN2_3			Mux input channel 2 of TIM module 2
	ERAY0_RXDA0			Receive Channel A0
	CAN02_RXDD			CAN receive input node 2
	ASCLIN1_ARXD			Receive input
	P14.8	O0		General-purpose output
	GTM_TOUT88	O1		GTM muxed output
	ASCLIN5_ASLSO	O2		Slave select signal output
	ASCLIN7_ASLSO	O3		Slave select signal output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-8 端口 P14 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
D12	P14.9	I	LVDS_R X / FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN3_3			Mux input channel 3 of TIM module 3
	GTM_TIM2_IN3_3			Mux input channel 3 of TIM module 2
	ASCLIN0_ACTSA			Clear to send input
	QSPI2_MRSTFN			Master SPI data input (LVDS N line)
	ASCLIN9_ARXD			Receive input
	P14.9	O0		General-purpose output
	GTM_TOUT89	O1		GTM muxed output
	—	O2		Reserved
	MSC0_EN1	O3		Chip Select
	CAN10_TXD	O4		CAN transmit output node 0
	ERAY0_TXENB	O5		Transmit Enable Channel B
	ERAY0_TXENA	O6		Transmit Enable Channel A
	—	O7		Reserved
D11	P14.10	I	LVDS_R X / FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN4_3			Mux input channel 4 of TIM module 3
	GTM_TIM2_IN4_3			Mux input channel 4 of TIM module 2
	QSPI2_MRSTFP			Master SPI data input (LVDS P line)
	P14.10	O0		General-purpose output
	GTM_TOUT90	O1		GTM muxed output
	—	O2		Reserved
	MSC0_EN0	O3		Chip Select
	ASCLIN1_ATX	O4		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	CAN02_TXD	O5		CAN transmit output node 2
	IOM_MON2_7			Monitor input 2
	IOM_REF2_7			Reference input 2
	ERAY0_TXDA	O6		Transmit Channel A
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-9 端口 P15 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
B20	P15.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN3_4			Mux input channel 3 of TIM module 3
	GTM_TIM2_IN3_4			Mux input channel 3 of TIM module 2
	P15.0	O0		General-purpose output
	GTM_TOUT71	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI0_SLS013	O3		Master slave select output
	—	O4		Reserved
	CAN02_TXD	O5		CAN transmit output node 2
	IOM_MON2_7			Monitor input 2
	IOM_REF2_7			Reference input 2
	ASCLIN1_ASCLK	O6		Shift clock output
	—	O7		Reserved
A18	P15.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN4_4			Mux input channel 4 of TIM module 3
	GTM_TIM2_IN4_4			Mux input channel 4 of TIM module 2
	CAN02_RXDA			CAN receive input node 2
	ASCLIN1_ARXA			Receive input
	QSPI2_SLSIB			Slave select input
	SCU_E_REQ7_2			ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P15.1	O0		General-purpose output
	GTM_TOUT72	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI2_SLS05	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-9 端口 P15 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
C19	P15.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN5_4			Mux input channel 5 of TIM module 3
	GTM_TIM2_IN5_4			Mux input channel 5 of TIM module 2
	QSPI2_SLSIA			Slave select input
	SENT_SENT10D			Receive input channel 10
	QSPI2_MRSTE			Master SPI data input
	P15.2	O0		General-purpose output
	GTM_TOUT73	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	QSPI2_SLSO0	O3		Master slave select output
	—	O4		Reserved
	CAN01_TXD	O5		CAN transmit output node 1
	IOM_MON2_6			Monitor input 2
	IOM_REF2_6			Reference input 2
	ASCLIN0_ASCLK	O6		Shift clock output
	—	O7		Reserved
B17	P15.3	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN6_4			Mux input channel 6 of TIM module 3
	GTM_TIM2_IN6_4			Mux input channel 6 of TIM module 2
	CAN01_RXDA			CAN receive input node 1
	ASCLIN0_ARXB			Receive input
	QSPI2_SCLKA			Slave SPI clock inputs
	P15.3	O0		General-purpose output
	GTM_TOUT74	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	MSC0_EN1	O5		Chip Select
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-9 端口 P15 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
A17	P15.4	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN7_4			Mux input channel 7 of TIM module 3
	GTM_TIM2_IN7_4			Mux input channel 7 of TIM module 2
	I2C0_SCLC			Serial Clock Input 2
	QSPI2_MRSTA			Master SPI data input
	SCU_E_REQ0_0			ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	SENT_SENT11D			Receive input channel 11
	P15.4	O0		General-purpose output
	GTM_TOUT75	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI2_MRST	O3		Slave SPI data output
	IOM_MON2_2			Monitor input 2
	IOM_REF2_2			Reference input 2
	—	O4		Reserved
	—	O5		Reserved
	I2C0_SCL	O6		Serial Clock Output
	CCU60_CC62	O7		T12 PWM channel 62
	IOM_MON1_0			Monitor input 1
	IOM_REF1_4			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-9 端口 P15 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
E14	P15.5	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN0_4			Mux input channel 0 of TIM module 3
	GTM_TIM2_IN0_4			Mux input channel 0 of TIM module 2
	ASCLIN1_ARXB			Receive input
	I2C0_SDAC			Serial Data Input 2
	QSPI2_MTSRA			Slave SPI data input
	SCU_E_REQ4_3			ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P15.5	O0		General-purpose output
	GTM_TOUT76	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI2_MTSR	O3		Master SPI data output
	—	O4		Reserved
	MSC0_EN0	O5		Chip Select
	I2C0_SDA	O6		Serial Data Output
	CCU60_CC61	O7		T12 PWM channel 61
	IOM_MON1_1			Monitor input 1
	IOM_REF1_5			Reference input 1
A16	P15.6	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN2_14			Mux input channel 2 of TIM module 2
	GTM_TIM1_IN0_6			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_6			Mux input channel 0 of TIM module 0
	QSPI2_MTSRB			Slave SPI data input
	P15.6	O0		General-purpose output
	GTM_TOUT77	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	QSPI2_MTSR	O3		Master SPI data output
	—	O4		Reserved
	QSPI2_SCLK	O5		Master SPI clock output
	ASCLIN3_ASCLK	O6		Shift clock output
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
	IOM_REF1_6			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-9 端口 P15 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
D15	P15.7	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_5			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_5			Mux input channel 1 of TIM module 0
	ASCLIN3_ARXA			Receive input
	QSPI2_MRSTB			Master SPI data input
	P15.7	O0		General-purpose output
	GTM_TOUT78	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	QSPI2_MRST	O3		Slave SPI data output
	IOM_MON2_2			Monitor input 2
	IOM_REF2_2			Reference input 2
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT60	O7		T12 PWM channel 60
	IOM_MON1_3			Monitor input 1
	IOM_REF1_3			Reference input 1
D14	P15.8	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_5			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_5			Mux input channel 2 of TIM module 0
	QSPI2_SCLKB			Slave SPI clock inputs
	SCU_E_REQ5_0			ERU Channel 5 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P15.8	O0		General-purpose output
	GTM_TOUT79	O1		GTM muxed output
	—	O2		Reserved
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	ASCLIN3_ASCLK	O6		Shift clock output
	CCU60_COUT61	O7		T12 PWM channel 61
	IOM_MON1_4			Monitor input 1
	IOM_REF1_2			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-10 端口 P20 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
H20	P20.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_7			Mux input channel 6 of TIM module 1
	GTM_TIM1_IN4_9			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN6_7			Mux input channel 6 of TIM module 0
	CAN03_RXDC			CAN receive input node 3
	CCU_PAD_SYSCLK			Sysclk input
	CBS_TGI0			Trigger input
	SCU_E_REQ6_0			ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	GPT120_T6EUDA			Count direction control input of core timer T6
	P20.0	O0		General-purpose output
	GTM_TOUT59	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	ASCLIN3_ASCLK	O3		Shift clock output
	—	O4		Reserved
	HSCT0_SYSCLK_OUT	O5		sys clock output
	—	O6		Reserved
	—	O7		Reserved
	CBS_TGO0	O		Trigger output
G19	P20.1	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN4_11			Mux input channel 4 of TIM module 4
	GTM_TIM3_IN3_5			Mux input channel 3 of TIM module 3
	GTM_TIM2_IN3_5			Mux input channel 3 of TIM module 2
	CBS_TGI1			Trigger input
	GTM_DTMA1_1			CDTM1_DTM4
	P20.1	O0		General-purpose output
	GTM_TOUT60	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	CBS_TGO1	O		Trigger output

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-10 端口 P20 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
H19	P20.2	I	S / PU / VEXT	General-purpose input This pin is latched at power on reset release to enter test mode.
				Testmode Enable Input
	TESTMODE			
G20	P20.3	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN5_11			Mux input channel 5 of TIM module 4
	GTM_TIM3_IN4_5			Mux input channel 4 of TIM module 3
	GTM_TIM2_IN4_5			Mux input channel 4 of TIM module 2
	ASCLIN3_ARXC			Receive input
	GPT120_T6INA			Trigger/gate input of core timer T6
	P20.3	O0		General-purpose output
	GTM_TOUT61	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	QSPI0_SLSO9	O3		Master slave select output
	QSPI2_SLSO9	O4		Master slave select output
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	—	O6		Reserved
	—	O7		Reserved
F17	P20.6	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN6_5			Mux input channel 6 of TIM module 3
	GTM_TIM2_IN6_5			Mux input channel 6 of TIM module 2
	CAN12_RXDA			CAN receive input node 2
	ASCLIN9_ARXE			Receive input
	P20.6	O0		General-purpose output
	GTM_TOUT62	O1		GTM muxed output
	ASCLIN1_ARTS	O2		Ready to send output
	QSPI0_SLSO8	O3		Master slave select output
	QSPI2_SLSO8	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-10 端口 P20 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
F19	P20.7	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN7_5			Mux input channel 7 of TIM module 3
	GTM_TIM2_IN7_5			Mux input channel 7 of TIM module 2
	GTM_TIM1_IN5_8			Mux input channel 5 of TIM module 1
	CAN00_RXDB			CAN receive input node 0
	ASCLIN1_ACTSA			Clear to send input
	ASCLIN9_ARXF			Receive input
	P20.7	O0		General-purpose output
	GTM_TOUT63	O1		GTM muxed output
	ASCLIN9_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	CAN12_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	CCU61_COUT63	O7		T13 PWM channel 63
	IOM_MON1_7			Monitor input 1
	IOM_REF1_7			Reference input 1
F20	P20.8	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN7_3			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_3			Mux input channel 7 of TIM module 0
	P20.8	O0		General-purpose output
	GTM_TOUT64	O1		GTM muxed output
	ASCLIN1_ASLSO	O2		Slave select signal output
	QSPI0_SLSO0	O3		Master slave select output
	QSPI1_SLSO0	O4		Master slave select output
	CAN00_TXD	O5		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	—	O6		Reserved
	CCU61_CC60	O7		T12 PWM channel 60
	IOM_MON1_8			Monitor input 1
	IOM_REF1_13			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-10 端口 P20 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
E17	P20.9	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN5_5			Mux input channel 5 of TIM module 3
	GTM_TIM2_IN5_5			Mux input channel 5 of TIM module 2
	CAN03_RXDE			CAN receive input node 3
	ASCLIN1_ARXC			Receive input
	QSPI0_SLSIB			Slave select input
	SCU_E_REQ7_0			ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P20.9	O0		General-purpose output
	GTM_TOUT65	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO1	O3		Master slave select output
	QSPI1_SLSO1	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	CCU61_CC61	O7		T12 PWM channel 61
	IOM_MON1_9			Monitor input 1
	IOM_REF1_12			Reference input 1
E19	P20.10	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN6_6			Mux input channel 6 of TIM module 3
	GTM_TIM2_IN6_6			Mux input channel 6 of TIM module 2
	P20.10	O0		General-purpose output
	GTM_TOUT66	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI0_SLSO6	O3		Master slave select output
	QSPI2_SLSO7	O4		Master slave select output
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	ASCLIN1_ASCLK	O6		Shift clock output
	CCU61_CC62	O7		T12 PWM channel 62
	IOM_MON1_10			Monitor input 1
	IOM_REF1_11			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-10 端口 P20 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
E20	P20.11	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN7_6			Mux input channel 7 of TIM module 3
	GTM_TIM2_IN7_6			Mux input channel 7 of TIM module 2
	QSPI0_SCLKA			Slave SPI clock inputs
	P20.11	O0		General-purpose output
	GTM_TOUT67	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU61_COUT60	O7		T12 PWM channel 60
	IOM_MON1_11			Monitor input 1
	IOM_REF1_10			Reference input 1
D19	P20.12	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN0_5			Mux input channel 0 of TIM module 3
	GTM_TIM2_IN0_5			Mux input channel 0 of TIM module 2
	QSPI0_MRSTA			Master SPI data input
	IOM_PIN_13			GPIO pad input to FPC
	P20.12	O0		General-purpose output
	GTM_TOUT68	O1		GTM muxed output
	IOM_MON0_13			Monitor input 0
	—	O2		Reserved
	QSPI0_MRST	O3		Slave SPI data output
	IOM_MON2_0			Monitor input 2
	IOM_REF2_0			Reference input 2
	QSPI0_MTSR	O4		Master SPI data output
	—	O5		Reserved
	—	O6		Reserved
	CCU61_COUT61	O7		T12 PWM channel 61
	IOM_MON1_12			Monitor input 1
	IOM_REF1_9			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-10 端口 P20 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
D20	P20.13	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN1_4			Mux input channel 1 of TIM module 3
	GTM_TIM2_IN1_4			Mux input channel 1 of TIM module 2
	QSPI0_SLSIA			Slave select input
	IOM_PIN_14			GPIO pad input to FPC
	P20.13	O0		General-purpose output
	GTM_TOUT69	O1		GTM muxed output
	IOM_MON0_14			Monitor input 0
	—	O2		Reserved
	QSPI0_SLSO2	O3		Master slave select output
	QSPI1_SLSO2	O4		Master slave select output
	QSPI0_SCLK	O5		Master SPI clock output
	—	O6		Reserved
	CCU61_COUT62	O7		T12 PWM channel 62
	IOM_MON1_13			Monitor input 1
	IOM_REF1_8			Reference input 1
C20	P20.14	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN2_4			Mux input channel 2 of TIM module 3
	GTM_TIM2_IN2_4			Mux input channel 2 of TIM module 2
	QSPI0_MTSRA			Slave SPI data input
	IOM_PIN_15			GPIO pad input to FPC
	P20.14	O0		General-purpose output
	GTM_TOUT70	O1		GTM muxed output
	IOM_MON0_15			Monitor input 0
	—	O2		Reserved
	QSPI0_MTSR	O3		Master SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-11 端口 P21 的功能

Ball	Symbol	Ctrl.	Buffer Type	Function
K17	P21.0	I	LVDS_RX / FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN0_11			Mux input channel 0 of TIM module 4
	GTM_TIM3_IN4_6			Mux input channel 4 of TIM module 3
	GTM_TIM2_IN4_6			Mux input channel 4 of TIM module 2
	QSPI4_MRSTDN			Master SPI data input (LVDS N line)
	DMU_FDEST			Enter destructive debug mode
	ASCLIN11_ARXC			Receive input
	P21.0	O0		General-purpose output
	GTM_TOUT51	O1		GTM muxed output
	ASCLIN11_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	HSM_HSM1	O		Pin Output Value
J17	P21.1	I	LVDS_RX / FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN1_13			Mux input channel 1 of TIM module 4
	GTM_TIM3_IN5_6			Mux input channel 5 of TIM module 3
	GTM_TIM2_IN5_6			Mux input channel 5 of TIM module 2
	QSPI4_MRSTDP			Master SPI data input (LVDS P line)
	ASCLIN11_ARXD			Receive input
	GTM_DTMA4_1			CDTM4_DTM4
	P21.1	O0		General-purpose output
	GTM_TOUT52	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	HSM_HSM2	O		Pin Output Value

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-11 端口 P21 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
K19	P21.2	I	LVDS_RX / FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN4_11			Mux input channel 4 of TIM module 5
	GTM_TIM1_IN0_7			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_7			Mux input channel 0 of TIM module 0
	QSPI2_MRSTCN			Master SPI data input (LVDS N line)
	SCU_EMGSTOP_PORT_B			Emergency stop Port Pin B input request
	ASCLIN3_ARXGN			Differential Receive input (low active)
	HSCT0_RXDN			Rx data
	QSPI4_MRSTCN			Master SPI data input (LVDS N line)
	ASCLIN11_ARXE			Receive input
	GTM_DTMA1_0			CDTM1_DTM4
	P21.2	O0		General-purpose output
	GTM_TOUT53	O1		GTM muxed output
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	GETH_MDC	O5		MDIO clock
	—	O6		Reserved
	—	O7		Reserved
J19	P21.3	I	LVDS_RX / FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN5_12			Mux input channel 5 of TIM module 5
	GTM_TIM1_IN1_6			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_6			Mux input channel 1 of TIM module 0
	QSPI2_MRSTCP			Master SPI data input (LVDS P line)
	ASCLIN3_ARXGP			Differential Receive input (high active)
	GETH_MDIOD			MDIO Input
	HSCT0_RXDP			Rx data
	QSPI4_MRSTCP			Master SPI data input (LVDS P line)
	P21.3	O0		General-purpose output
	GTM_TOUT54	O1		GTM muxed output
	ASCLIN11_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	GETH_MDIO	O		MDIO Output

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-11 端口 P21 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
K20	P21.4	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM5_IN6_12			Mux input channel 6 of TIM module 5
	GTM_TIM1_IN2_6			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_6			Mux input channel 2 of TIM module 0
	P21.4	O0		General-purpose output
	GTM_TOUT55	O1		GTM muxed output
	ASCLIN11_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	HSCT0_TXDN	O		Tx data
J20	P21.5	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM5_IN7_11			Mux input channel 7 of TIM module 5
	GTM_TIM1_IN3_6			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_6			Mux input channel 3 of TIM module 0
	ASCLIN11_ARXF			Receive input
	P21.5	O0		General-purpose output
	GTM_TOUT56	O1		GTM muxed output
	ASCLIN3_ASCLK	O2		Shift clock output
	ASCLIN11_ATX	O3		Transmit output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	HSCT0_TXDP	O		Tx data

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-11 端口 P21 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
H17	P21.6/TDI	I	FAST / PD / PU2 / VEXT / ES3	General-purpose input PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ. DAPE: DAPE1 Data I/O.
	GTM_TIM4_IN2_12			Mux input channel 2 of TIM module 4
	GTM_TIM1_IN4_8			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_8			Mux input channel 4 of TIM module 0
	GPT120_T5EUDA			Count direction control input of timer T5
	ASCLIN3_ARXF			Receive input
	CBS_TGI2			Trigger input
	TDI			JTAG Module Data Input
	P21.6	O0		General-purpose output
	GTM_TOUT57	O1		GTM muxed output
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	GPT120_T3OUT	O7		External output for overflow/underflow detection of core timer T3
	CBS_TGO2	O		Trigger output
	DAP3	I/O		DAP: DAP3 Data I/O

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-11 端口 P21 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
H16	P21.7/TDO	I	FAST / PU2 / VEXT / ES4	General-purpose input DAP: DAP2 Data I/O; DAPE: DAPE2 Data I/O.
	GTM_TIM4_IN3_12			Mux input channel 3 of TIM module 4
	GTM_TIM1_IN5_7			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_7			Mux input channel 5 of TIM module 0
	GPT120_T5INA			Trigger/gate input of timer T5
	CBS_TGI3			Trigger input
	GETH_RXERB			Receive Error MII
	P21.7	O0		General-purpose output
	GTM_TOUT58	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	ASCLIN3_ASCLK	O3		Shift clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	GPT120_T6OUT	O7		External output for overflow/underflow detection of core timer T6
	CBS_TGO3	O		Trigger output
	DAP2	I/O		DAP: DAP2 Data I/O
	TDO	O		JTAG Module Data Output

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-12 端口 P22 的功能

Ball	Symbol	Ctrl.	Buffer Type	Function
P20	P22.0	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN1_7			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_7			Mux input channel 1 of TIM module 0
	QSPI4_MTSRB			Slave SPI data input
	ASCLIN6_ARXE			Receive input
	P22.0	O0		General-purpose output
	GTM_TOUT47	O1		GTM muxed output
	ASCLIN3_ATXN	O2		Differential Transmit output (low active)
	QSPI4_MTSR	O3		Master SPI data output
	QSPI4_SCLKN	O4		Master SPI clock output (LVDS N line)
	MSC1_FCLN	O5		Shift-clock inverted part of the differential signal
	—	O6		Reserved
	ASCLIN6_ATX	O7		Transmit output
P19	P22.1	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN0_8			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_8			Mux input channel 0 of TIM module 0
	QSPI4_MRSTB			Master SPI data input
	ASCLIN7_ARXE			Receive input
	P22.1	O0		General-purpose output
	GTM_TOUT48	O1		GTM muxed output
	ASCLIN3_ATXP	O2		Differential Transmit output (high active)
	QSPI4_MRST	O3		Slave SPI data output
	IOM_MON2_4			Monitor input 2
	IOM_REF2_4			Reference input 2
	QSPI4_SCLKP	O4		Master SPI clock output (LVDS P line)
	MSC1_FCLP	O5		Shift-clock direct part of the differential signal
	—	O6		Reserved
	ASCLIN7_ATX	O7		Transmit output

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-12 端口 P22 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
R20	P22.2	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN3_7			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_7			Mux input channel 3 of TIM module 0
	QSPI4_SLSIB			Slave select input
	P22.2	O0		General-purpose output
	GTM_TOUT49	O1		GTM muxed output
	ASCLIN5_ATX	O2		Transmit output
	QSPI4_SLSO3	O3		Master slave select output
	QSPI4_MTSRN	O4		Master SPI data output (LVDS N line)
	MSC1_SON	O5		Data output - inverted part of the differential signal
	—	O6		Reserved
	—	O7		Reserved
R19	P22.3	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN4_4			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_4			Mux input channel 4 of TIM module 0
	QSPI4_SCLKB			Slave SPI clock inputs
	ASCLIN5_ARXC			Receive input
	P22.3	O0		General-purpose output
	GTM_TOUT50	O1		GTM muxed output
	—	O2		Reserved
	QSPI4_SCLK	O3		Master SPI clock output
	QSPI4_MTSRP	O4		Master SPI data output (LVDS P line)
	MSC1_SOP	O5		Data output - direct part of the differential signal
	—	O6		Reserved
	—	O7		Reserved
P16	P22.4	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN0_8			Mux input channel 0 of TIM module 3
	ASCLIN7_ARXF			Receive input
	GTM_DTMA3_0			CDTM3_DTM4
	P22.4	O0		General-purpose output
	GTM_TOUT130	O1		GTM muxed output
	ASCLIN4_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	QSPI0_SLSO12	O4		Master slave select output
	—	O5		Reserved
	CAN13_TXD	O6		CAN transmit output node 3
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-12 端口 P22 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
P17	P22.5	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN1_7			Mux input channel 1 of TIM module 3
	QSPI0_MTSRC			Slave SPI data input
	CAN13_RXDC			CAN receive input node 3
	P22.5	O0		General-purpose output
	GTM_TOUT131	O1		GTM muxed output
	ASCLIN4_ATX	O2		Transmit output
	—	O3		Reserved
	QSPI0_MTSR	O4		Master SPI data output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
N16	P22.6	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN2_6			Mux input channel 2 of TIM module 3
	GTM_TIM2_IN6_14			Mux input channel 6 of TIM module 2
	QSPI0_MRSTC			Master SPI data input
	ASCLIN4_ARXC			Receive input
	P22.6	O0		General-purpose output
	GTM_TOUT132	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	QSPI0_MRST	O4		Slave SPI data output
	IOM_MON2_0			Monitor input 2
	IOM_REF2_0			Reference input 2
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
N17	P22.7	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN3_7			Mux input channel 3 of TIM module 3
	QSPI0_SCLKC			Slave SPI clock inputs
	P22.7	O0		General-purpose output
	GTM_TOUT133	O1		GTM muxed output
	ASCLIN4_ASCLK	O2		Shift clock output
	—	O3		Reserved
	QSPI0_SCLK	O4		Master SPI clock output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-12 端口 P22 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
M16	P22.8	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN0_4			Mux input channel 0 of TIM module 5
	GTM_TIM3_IN4_7			Mux input channel 4 of TIM module 3
	QSPI0_SCLKB			Slave SPI clock inputs
	P22.8	O0		General-purpose output
	GTM_TOUT134	O1		GTM muxed output
	ASCLIN5_ASCLK	O2		Shift clock output
	—	O3		Reserved
	QSPI0_SCLK	O4		Master SPI clock output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
M17	P22.9	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN1_10			Mux input channel 1 of TIM module 5
	GTM_TIM3_IN5_7			Mux input channel 5 of TIM module 3
	QSPI0_MRSTB			Master SPI data input
	ASCLIN4_ARXD			Receive input
	GTM_DTMA3_1			CDTM3_DTM4
	P22.9	O0		General-purpose output
	GTM_TOUT135	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	QSPI0_MRST	O4		Slave SPI data output
	IOM_MON2_0			Monitor input 2
	IOM_REF2_0			Reference input 2
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-12 端口 P22 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
L16	P22.10	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN2_8			Mux input channel 2 of TIM module 5
	GTM_TIM3_IN6_7			Mux input channel 6 of TIM module 3
	QSPI0_MTSRB			Slave SPI data input
	P22.10	O0		General-purpose output
	GTM_TOUT136	O1		GTM muxed output
	ASCLIN4_ATX	O2		Transmit output
	—	O3		Reserved
	QSPI0_MTSR	O4		Master SPI data output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
L17	P22.11	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN3_10			Mux input channel 3 of TIM module 5
	GTM_TIM3_IN7_7			Mux input channel 7 of TIM module 3
	P22.11	O0		General-purpose output
	GTM_TOUT137	O1		GTM muxed output
	ASCLIN4_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	QSPI0_SLSO10	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-13 端口 P23 的功能

Ball	Symbol	Ctrl.	Buffer Type	Function
V20	P23.0	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN5_4			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_4			Mux input channel 5 of TIM module 0
	CAN10_RXDC			CAN receive input node 0
	P23.0	O0		General-purpose output
	GTM_TOUT41	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
U19	P23.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_4			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_4			Mux input channel 6 of TIM module 0
	MSC1_SDIO			Upstream asynchronous input signal
	ASCLIN6_ARXF			Receive input
	P23.1	O0		General-purpose output
	GTM_TOUT42	O1		GTM muxed output
	ASCLIN1_ARTS	O2		Ready to send output
	QSPI4_SLSO6	O3		Master slave select output
	GTM_CLK0	O4		CGM generated clock
	CAN10_TXD	O5		CAN transmit output node 0
	CCU_EXTCLK0	O6		External Clock 0
	ASCLIN6_ASCLK	O7		Shift clock output
U20	P23.2	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_5			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_5			Mux input channel 6 of TIM module 0
	ASCLIN7_ARXC			Receive input
	P23.2	O0		General-purpose output
	GTM_TOUT43	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	CAN12_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-13 端口 P23 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
T19	P23.3	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN7_4			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_4			Mux input channel 7 of TIM module 0
	MSC1_INJ0			Injection signal from port
	ASCLIN6_ARXA			Receive input
	CAN12_RXDC			CAN receive input node 2
	P23.3	O0		General-purpose output
	GTM_TOUT44	O1		GTM muxed output
	ASCLIN7_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
T20	P23.4	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN7_5			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_5			Mux input channel 7 of TIM module 0
	P23.4	O0		General-purpose output
	GTM_TOUT45	O1		GTM muxed output
	ASCLIN6_ASLSO	O2		Slave select signal output
	QSPI4_SLSO5	O3		Master slave select output
	—	O4		Reserved
	MSC1_EN0	O5		Chip Select
	—	O6		Reserved
	—	O7		Reserved
T17	P23.5	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_7			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_7			Mux input channel 2 of TIM module 0
	P23.5	O0		General-purpose output
	GTM_TOUT46	O1		GTM muxed output
	ASCLIN6_ATX	O2		Transmit output
	QSPI4_SLSO4	O3		Master slave select output
	—	O4		Reserved
	MSC1_EN1	O5		Chip Select
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-13 端口 P23 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
R17	P23.6	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN2_7			Mux input channel 2 of TIM module 4
	GTM_TIM1_IN2_10			Mux input channel 2 of TIM module 1
	P23.6	O0		General-purpose output
	GTM_TOUT138	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	QSPI0_SLSO11	O4		Master slave select output
	CAN11_TXD	O5		CAN transmit output node 1
	—	O6		Reserved
	—	O7		Reserved
R16	P23.7	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN3_7			Mux input channel 3 of TIM module 4
	GTM_TIM1_IN3_10			Mux input channel 3 of TIM module 1
	CAN11_RXDC			CAN receive input node 1
	P23.7	O0		General-purpose output
	GTM_TOUT139	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-14 端口 P32 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
Y17	P32.0	I	SLOW / PU1 / VEXT / ES	General-purpose input P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
	GTM_TIM3_IN2_5			Mux input channel 2 of TIM module 3
	GTM_TIM2_IN2_5			Mux input channel 2 of TIM module 2
	P32.0	O0		General-purpose output
	GTM_TOUT36	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
W17	P32.1	I	SLOW / PU1 / VEXT / ES	General-purpose input P32.1 / External Pass Device gate control for EVRC
	GTM_TIM3_IN3_15			Mux input channel 3 of TIM module 3
	P32.1	O0		General-purpose output
	GTM_TOUT37	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-14 端口 P32 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y18	P32.2	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN3_8			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_8			Mux input channel 3 of TIM module 0
	CAN03_RXDB			CAN receive input node 3
	ASCLIN3_ARXD			Receive input
	P32.2	O0		General-purpose output
	GTM_TOUT38	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	PMS_DCDCSYNCO	O6		DC-DC synchronization output
	—	O7		Reserved
Y19	P32.3	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN4_5			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_5			Mux input channel 4 of TIM module 0
	P32.3	O0		General-purpose output
	GTM_TOUT39	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	—	O3		Reserved
	ASCLIN3_ASCLK	O4		Shift clock output
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 LFBGA-292 封装 TC37x TP 的引脚

表 2-14 端口 P32 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
W18	P32.4	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN5_5			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_5			Mux input channel 5 of TIM module 0
	ASCLIN1_ACTSB			Clear to send input
	MSC1_SDI2			Upstream assynchronous input signal
	P32.4	O0		General-purpose output
	GTM_TOUT40	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	GTM_CLK1	O4		CGM generated clock
	MSC1_EN0	O5		Chip Select
	CCU_EXTCLK1	O6		External Clock 1
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1
	PMS_DCDCSYNCO	O		DC-DC synchronization output
T15	P32.5	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN5_9			Mux input channel 5 of TIM module 5
	GTM_TIM4_IN1_14			Mux input channel 1 of TIM module 4
	GTM_TIM3_IN5_8			Mux input channel 5 of TIM module 3
	SENT_SENT10C			Receive input channel 10
	P32.5	O0		General-purpose output
	GTM_TOUT140	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	—			Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	CAN02_TXD	O6		CAN transmit output node 2
	IOM_MON2_7	O7		Monitor input 2
	IOM_REF2_7			Reference input 2
	—			Reserved

TC37x 引脚定义和功能 LFBGA-292 封装 TC37x TP 的引脚

表 2-14 端口 P32 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
U15	P32.6	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN6_9			Mux input channel 6 of TIM module 5
	GTM_TIM4_IN4_15			Mux input channel 4 of TIM module 4
	GTM_TIM3_IN6_8			Mux input channel 6 of TIM module 3
	CAN02_RXDC			CAN receive input node 2
	CBS_TGI4			Trigger input
	ASCLIN2_ARXF			Receive input
	ASCLIN6_ARXC			Receive input
	SENT_SENT11C			Receive input channel 11
	P32.6	O0		General-purpose output
	GTM_TOUT141	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	QSPI2_SLSO12	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	CBS_TGO4	O		Trigger output
U16	P32.7	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN7_8			Mux input channel 7 of TIM module 5
	GTM_TIM4_IN0_15			Mux input channel 0 of TIM module 4
	GTM_TIM3_IN7_8			Mux input channel 7 of TIM module 3
	CBS_TGI5			Trigger input
	SENT_SENT12C			Receive input channel 12
	P32.7	O0		General-purpose output
	GTM_TOUT142	O1		GTM muxed output
	ASCLIN6_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	CBS_TGO5	O		Trigger output

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-15 端口 P33 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
W10	P33.0	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM3_IN0_13			Mux input channel 0 of TIM module 3
	GTM_TIM1_IN4_6			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_6			Mux input channel 4 of TIM module 0
	EDSADC_ITR0E			Trigger/Gate input, channel 0
	SENT_SENT13C			Receive input channel 13
	IOM_PIN_0			GPIO pad input to FPC
	GTM_DTMT1_2			CDTM1_DTM0
	EVADC_G10CH7	AI		Analog input channel 7, group 10
	P33.0	O0		General-purpose output
	GTM_TOUT22	O1		GTM muxed output
	IOM_MON0_0			Monitor input 0
	IOM_GTM_0			GTM-provided inputs to EXOR combiner
	ASCLIN5_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	EVADC_FC2BFLOUT	O6		Boundary flag output, FC channel 2
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-15 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y10	P33.1	I	SLOW / PU1 / VEVR SB / ES5	General-purpose input
	GTM_TIM3_IN1_15			Mux input channel 1 of TIM module 3
	GTM_TIM1_IN5_6			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_6			Mux input channel 5 of TIM module 0
	EDSADC_ITR1E			Trigger/Gate input, channel 1
	PSI5_RX0C			RXD inputs (receive data) channel 0
	EDSADC_DSCIN2B			Modulator clock input, channel 2
	SENT_SENT9C			Receive input channel 9
	ASCLIN8_ARXC			Receive input
	IOM_PIN_1			GPIO pad input to FPC
	EVADC_G10CH6	AI		Analog input channel 6, group 10
	P33.1	O0		General-purpose output
	GTM_TOUT23	O1		GTM muxed output
	IOM_MON0_1			Monitor input 0
	IOM_GTM_1			GTM-provided inputs to EXOR combiner
	ASCLIN3_ASLSO	O2		Slave select signal output
	QSPI2_SCLK	O3		Master SPI clock output
	EDSADC_DSCOUT2	O4		Modulator clock output
	EVADC_EMUX02	O5		Control of external analog multiplexer interface 0
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-15 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
W11	P33.2	I	SLOW / PU1 / VEVRB / ES5	General-purpose input
	GTM_TIM3_IN2_14			Mux input channel 2 of TIM module 3
	GTM_TIM1_IN6_6			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_6			Mux input channel 6 of TIM module 0
	EDSADC_ITR2E			Trigger/Gate input, channel 2
	SENT_SENT8C			Receive input channel 8
	EDSADC_DSDIN2B			Digital datastream input, channel 2
	IOM_PIN_2			GPIO pad input to FPC
	EVADC_G10CH5	AI		Analog input channel 5, group 10
	P33.2	O0		General-purpose output
	GTM_TOUT24	O1		GTM muxed output
	IOM_MON0_2			Monitor input 0
	IOM_GTM_2			GTM-provided inputs to EXOR combiner
	ASCLIN3_ASCLK	O2		Shift clock output
	QSPI2_SLSO10	O3		Master slave select output
	PSI5_TX0	O4		TXD outputs (send data)
	IOM_MON1_14			Monitor input 1
	IOM_REF1_14			Reference input 1
	EVADC_EMUX01	O5		Control of external analog multiplexer interface 0
	EVADC_FC3BFLOUT	O6		Boundary flag output, FC channel 3
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-15 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y11	P33.3	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM3_IN3_12			Mux input channel 3 of TIM module 3
	GTM_TIM1_IN7_6			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_6			Mux input channel 7 of TIM module 0
	PSI5_RX1C			RXD inputs (receive data) channel 1
	SENT_SENT7C			Receive input channel 7
	EDSADC_DSCIN1B			Modulator clock input, channel 1
	IOM_PIN_3			GPIO pad input to FPC
	EVADC_G10CH4	AI		Analog input channel 4, group 10
	P33.3	O0		General-purpose output
	GTM_TOUT25	O1		GTM muxed output
	IOM_MON0_3			Monitor input 0
	IOM_GTM_3			GTM-provided inputs to EXOR combiner
	ASCLIN5_ASCLK	O2		Shift clock output
	QSPI4_SLSO2	O3		Master slave select output
	EDSADC_DSCOUT1	O4		Modulator clock output
	EVADC_EMUX00	O5		Control of external analog multiplexer interface 0
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-15 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
W12	P33.4	I	SLOW / PU1 / VEVR SB / ES5	General-purpose input
	GTM_TIM4_IN4_10			Mux input channel 4 of TIM module 4
	GTM_TIM1_IN0_10			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_10			Mux input channel 0 of TIM module 0
	EDSADC_ITR0F			Trigger/Gate input, channel 0
	SENT_SENT6C			Receive input channel 6
	EDSADC_DSDIN1B			Digital datastream input, channel 1
	CCU61_CTRAPC			Trap input capture
	ASCLIN5_ARXB			Receive input
	IOM_PIN_4			GPIO pad input to FPC
	GTM_DTMT2_0			CDTM2_DTM0
	EVADC_G10CH3	AI		Analog input channel 3, group 10
	P33.4	O0	General-purpose output	
	GTM_TOUT26	O1	GTM muxed output	
	IOM_MON0_4		Monitor input 0	
	IOM_GTM_4		GTM-provided inputs to EXOR combiner	
	ASCLIN2_ARTS	O2	Ready to send output	
	QSPI2_SLSO12	O3	Master slave select output	
	PSI5_TX1	O4	TXD outputs (send data)	
	IOM_MON1_15		Monitor input 1	
	EVADC_EMUX12	O5	Control of external analog multiplexer interface 1	
	EVADC_FC0BFLOUT	O6	Boundary flag output, FC channel 0	
	CAN13_TXD	O7	CAN transmit output node 3	

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-15 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y12	P33.5	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM4_IN5_10			Mux input channel 5 of TIM module 4
	GTM_TIM1_IN1_8			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_8			Mux input channel 1 of TIM module 0
	EDSADC_DSCIN0B			Modulator clock input, channel 0
	EDSADC_ITR1F			Trigger/Gate input, channel 1
	GPT120_T4EUIDB			Count direction control input of timer T4
	PSI5S_RXC			RX data input
	ASCLIN2_ACTSB			Clear to send input
	CCU61_CCPOS2C			Hall capture input 2
	SENT_SENT5C			Receive input channel 5
	CAN13_RXDB			CAN receive input node 3
	IOM_PIN_5			GPIO pad input to FPC
	EVADC_G10CH2	AI		Analog input channel 2, group 10
	P33.5	O0		General-purpose output
	GTM_TOUT27	O1		GTM muxed output
	IOM_MON0_5			Monitor input 0
	IOM_GTM_5			GTM-provided inputs to EXOR combiner
	QSPI0_SLSO7	O2		Master slave select output
	QSPI1_SLSO7	O3		Master slave select output
	EDSADC_DSCOUT0	O4		Modulator clock output
	EVADC_EMUX11	O5		Control of external analog multiplexer interface 1
	EVADC_FC2BFLOUT	O6		Boundary flag output, FC channel 2
	ASCLIN5_ASLSO	O7		Slave select signal output

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-15 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
W13	P33.6	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN2_9			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_9			Mux input channel 2 of TIM module 0
	EDSADC_ITR2F			Trigger/Gate input, channel 2
	GPT120_T2EUDB			Count direction control input of timer T2
	SENT_SENT4C			Receive input channel 4
	CCU61_CCPOS1C			Hall capture input 1
	EDSADC_DSDIN0B			Digital datastream input, channel 0
	ASCLIN8_ARXD			Receive input
	IOM_PIN_6			GPIO pad input to FPC
	GTM_DTMT2_1			CDTM2_DTM0
	EVADC_G10CH1	AI		Analog input channel 1, group 10
	P33.6	O0		General-purpose output
	GTM_TOUT28	O1		GTM muxed output
	IOM_MON0_6			Monitor input 0
	IOM_GTM_6			GTM-provided inputs to EXOR combiner
	ASCLIN2_ASLSO	O2		Slave select signal output
	QSPI2_SLSO11	O3		Master slave select output
	—	O4		Reserved
	EVADC_EMUX10	O5		Control of external analog multiplexer interface 1
	EVADC_FC1BFLOUT	O6		Boundary flag output, FC channel 1
	PSI5S_TX	O7		TX data output

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-15 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y13	P33.7	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN3_9			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_9			Mux input channel 3 of TIM module 0
	CAN00_RXDE			CAN receive input node 0
	GPT120_T2INB			Trigger/gate input of timer T2
	CCU61_CCPOS0C			Hall capture input 0
	SCU_E_REQ4_0			ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	SENT_SENT14C			Receive input channel 14
	IOM_PIN_7			GPIO pad input to FPC
	EVADC_G10CH0	AI		Analog input channel 0, group 10
	P33.7	O0		General-purpose output
	GTM_TOUT29	O1		GTM muxed output
	IOM_MON0_7			Monitor input 0
	IOM_GTM_7			GTM-provided inputs to EXOR combiner
	ASCLIN2_ASCLK	O2		Shift clock output
	QSPI4_SLSO7	O3		Master slave select output
	ASCLIN8_ATX	O4		Transmit output
	—	O5		Reserved
	EVADC_FC3BFLOUT	O6		Boundary flag output, FC channel 3
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-15 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
W14	P33.8	I	FAST / HighZ / VEVRSB	General-purpose input
	GTM_TIM1_IN4_7			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_7			Mux input channel 4 of TIM module 0
	ASCLIN2_ARXE			Receive input
	SCU_EMGSTOP_POR T_A			Emergency stop Port Pin A input request
	IOM_PIN_8			GPIO pad input to FPC
	P33.8	O0		General-purpose output
	GTM_TOUT30	O1		GTM muxed output
	IOM_MON0_8			Monitor input 0
	ASCLIN2_ATX			Transmit output
	IOM_MON2_14	O2		Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI4_SLSO2			Master slave select output
	—	O4		Reserved
	CAN00_TXD	O5		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	—	O6		Reserved
	CCU61_COUT62	O7		T12 PWM channel 62
	IOM_MON1_13			Monitor input 1
	IOM_REF1_8			Reference input 1
	SMU_FSP0	O		FSP[1..0] Output Signals - Generated by SMU_core

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-15 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y14	P33.9	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN1_9			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_9			Mux input channel 1 of TIM module 0
	IOM_PIN_9			GPIO pad input to FPC
	P33.9	O0		General-purpose output
	GTM_TOUT31	O1		GTM muxed output
	IOM_MON0_9			Monitor input 0
	ASCLIN2_ATX			Transmit output
	IOM_MON2_14	O2		Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI4_SLSO1			Master slave select output
	ASCLIN2_ASCLK	O4		Shift clock output
	CAN01_TXD	O5		CAN transmit output node 1
	IOM_MON2_6			Monitor input 2
	IOM_REF2_6			Reference input 2
	ASCLIN0_ATX	O6		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	CCU61_CC62	O7		T12 PWM channel 62
	IOM_MON1_10			Monitor input 1
	IOM_REF1_11			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-15 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
W15	P33.10	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM4_IN4_14			Mux input channel 4 of TIM module 4
	GTM_TIM1_IN0_9			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_9			Mux input channel 0 of TIM module 0
	QSPI4_SLSIA			Slave select input
	CAN01_RXDD			CAN receive input node 1
	ASCLIN0_ARXD			Receive input
	IOM_PIN_10			GPIO pad input to FPC
	P33.10	O0		General-purpose output
	GTM_TOUT32	O1		GTM muxed output
	IOM_MON0_10			Monitor input 0
	QSPI1_SLSO6	O2		Master slave select output
	QSPI4_SLSO0	O3		Master slave select output
	ASCLIN1_ASLSO	O4		Slave select signal output
	PSI5S_CLK	O5		PSI5S CLK is a clock that can be used on a pin to drive the external PHY.
	—	O6		Reserved
	CCU61_COUT61	O7		T12 PWM channel 61
	IOM_MON1_12			Monitor input 1
	IOM_REF1_9			Reference input 1
	SMU_FSP1	O		FSP[1..0] Output Signals - Generated by SMU_core
Y15	P33.11	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN2_8			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_8			Mux input channel 2 of TIM module 0
	QSPI4_SCLKA			Slave SPI clock inputs
	IOM_PIN_11			GPIO pad input to FPC
	P33.11	O0		General-purpose output
	GTM_TOUT33	O1		GTM muxed output
	IOM_MON0_11			Monitor input 0
	ASCLIN1_ASCLK	O2		Shift clock output
	QSPI4_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	EDSADC_CGPWMN	O6		Negative carrier generator output
	CCU61_CC61	O7		T12 PWM channel 61
	IOM_MON1_9			Monitor input 1
	IOM_REF1_12			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-15 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
W16	P33.12	I	FAST / PU1 / VEVR SB / ES5	General-purpose input
	GTM_TIM3_IN0_6			Mux input channel 0 of TIM module 3
	GTM_TIM2_IN0_6			Mux input channel 0 of TIM module 2
	QSPI4_MTSRA			Slave SPI data input
	CAN00_RXDD			CAN receive input node 0
	PMS_PINBWKP			PINB (P33.12) pin input
	IOM_PIN_12			GPIO pad input to FPC
	P33.12	O0		General-purpose output
	GTM_TOUT34	O1		GTM muxed output
	IOM_MON0_12			Monitor input 0
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI4_MTSR	O3		Master SPI data output
	ASCLIN1_ASCLK	O4		Shift clock output
	—	O5		Reserved
	EDSADC_CGPWMP	O6		Positive carrier generator output
	CCU61_COUT60	O7		T12 PWM channel 60
	IOM_MON1_11			Monitor input 1
	IOM_REF1_10			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-15 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y16	P33.13	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM3_IN1_5			Mux input channel 1 of TIM module 3
	GTM_TIM2_IN1_5			Mux input channel 1 of TIM module 2
	ASCLIN1_ARXF			Receive input
	EDSADC_SGNB			Carrier sign signal input
	QSPI4_MRSTA			Master SPI data input
	MSC1_INJ1			Injection signal from port
	P33.13	O0		General-purpose output
	GTM_TOUT35	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI4_MRST	O3		Slave SPI data output
	IOM_MON2_4			Monitor input 2
	IOM_REF2_4			Reference input 2
	QSPI2_SLSO6	O4		Master slave select output
	CAN00_TXD	O5		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	—	O6		Reserved
	CCU61_CC60	O7		T12 PWM channel 60
	IOM_MON1_8			Monitor input 1
	IOM_REF1_13			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-15 端口 P33 的功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
T14	P33.14	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM5_IN0_8			Mux input channel 0 of TIM module 5
	GTM_TIM4_IN5_14			Mux input channel 5 of TIM module 4
	GTM_TIM2_IN0_8			Mux input channel 0 of TIM module 2
	QSPI2_SCLKD			Slave SPI clock inputs
	CBS_TGI6			Trigger input
	P33.14	O0		General-purpose output
	GTM_TOUT143	O1		GTM muxed output
	—	O2		Reserved
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU60_CC62	O7		T12 PWM channel 62
	IOM_MON1_0			Monitor input 1
	IOM_REF1_4			Reference input 1
	CBS_TGO6	O		Trigger output
U14	P33.15	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM5_IN1_9			Mux input channel 1 of TIM module 5
	GTM_TIM4_IN6_12			Mux input channel 6 of TIM module 4
	GTM_TIM2_IN1_7			Mux input channel 1 of TIM module 2
	CBS_TGI7			Trigger input
	P33.15	O0		General-purpose output
	GTM_TOUT144	O1		GTM muxed output
	—	O2		Reserved
	QSPI2_SLSO11	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT62	O7		T12 PWM channel 62
	IOM_MON1_5			Monitor input 1
	IOM_REF1_1			Reference input 1
	CBS_TGO7	O		Trigger output

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-16 端口 P34 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
U11	P34.1	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM5_IN3_9			Mux input channel 3 of TIM module 5
	GTM_TIM3_IN4_12			Mux input channel 4 of TIM module 3
	GTM_TIM2_IN3_9			Mux input channel 3 of TIM module 2
	EVADC_G10CH11	AI		Analog input channel 11, group 10
	P34.1	O0		General-purpose output
	GTM_TOUT146	O1		GTM muxed output
	ASCLIN4_ATX	O2		Transmit output
	—	O3		Reserved
	CAN00_TXD	O4		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1
T12	P34.2	I	SLOW / PU1 / VEVRSB / ES	General-purpose input
	GTM_TIM5_IN4_9			Mux input channel 4 of TIM module 5
	GTM_TIM3_IN5_13			Mux input channel 5 of TIM module 3
	GTM_TIM2_IN4_8			Mux input channel 4 of TIM module 2
	ASCLIN4_ARXB			Receive input
	CAN00_RXDG			CAN receive input node 0
	EVADC_G10CH10	AI		Analog input channel 10, group 10
	P34.2	O0		General-purpose output
	GTM_TOUT147	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
	IOM_REF1_6			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-16 端口 P34 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
U12	P34.3	I	SLOW / PU1 / VEVRSB / ES	General-purpose input
	GTM_TIM5_IN5_10			Mux input channel 5 of TIM module 5
	GTM_TIM3_IN6_13			Mux input channel 6 of TIM module 3
	GTM_TIM2_IN5_9			Mux input channel 5 of TIM module 2
	EVADC_G10CH9	AI		Analog input channel 9, group 10
	P34.3	O0		General-purpose output
	GTM_TOUT148	O1		GTM muxed output
	ASCLIN4_ASCLK	O2		Shift clock output
	—	O3		Reserved
	QSPI2_SLSO10	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT60	O7		T12 PWM channel 60
	IOM_MON1_3			Monitor input 1
	IOM_REF1_3			Reference input 1
T13	P34.4	I	SLOW / PU1 / VEVRSB / ES	General-purpose input
	GTM_TIM5_IN6_10			Mux input channel 6 of TIM module 5
	GTM_TIM3_IN7_12			Mux input channel 7 of TIM module 3
	GTM_TIM2_IN6_8			Mux input channel 6 of TIM module 2
	QSPI2_MRSTD			Master SPI data input
	EVADC_G10CH8	AI		Analog input channel 8, group 10
	P34.4	O0		General-purpose output
	GTM_TOUT149	O1		GTM muxed output
	ASCLIN4_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	QSPI2_MRST	O4		Slave SPI data output
	IOM_MON2_2			Monitor input 2
	IOM_REF2_2			Reference input 2
	—	O5		Reserved
	—	O6		Reserved
	CCU60_CC61	O7		T12 PWM channel 61
	IOM_MON1_1			Monitor input 1
	IOM_REF1_5			Reference input 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-16 端口 P34 功能 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
U13	P34.5	I	FAST / PU1 / VEVRSB / ES	General-purpose input
	GTM_TIM5_IN7_9			Mux input channel 7 of TIM module 5
	GTM_TIM4_IN7_12			Mux input channel 7 of TIM module 4
	GTM_TIM2_IN7_9			Mux input channel 7 of TIM module 2
	QSPI2_MTSRD			Slave SPI data input
	ASCLIN8_ARXE			Receive input
	P34.5	O0		General-purpose output
	GTM_TOUT150	O1		GTM muxed output
	ASCLIN8_ATX	O2		Transmit output
	—	O3		Reserved
	QSPI2_MTSR	O4		Master SPI data output
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT61	O7		T12 PWM channel 61
	IOM_MON1_4			Monitor input 1
	IOM_REF1_2			Reference input 1

表 2-17 模拟输入

Ball	Symbol	Ctrl.	Buffer Type	Function
T10	AN0	I	D / HighZ / VDDM	Analog Input 0
	EVADC_G0CH0			Analog input channel 0, group 0
	EDSADC_EDS3PA			Positive analog input channel 3, pin A
U10	AN1	I	D / HighZ / VDDM	Analog Input 1
	EVADC_G0CH1			Analog input channel 1, group 0
	EDSADC_EDS3NA			Negative analog input channel 3, pin A
W9	AN2	I	D / HighZ / VDDM	Analog Input 2
	EVADC_G0CH2			Analog input channel 2, group 0
	EDSADC_EDS0PA			Positive analog input channel 0, pin A
U9	AN3	I	D / HighZ / VDDM	Analog Input 3
	EVADC_G0CH3			Analog input channel 3, group 0
	EDSADC_EDS0NA			Negative analog input channel 0, pin A
T9	AN4	I	D / HighZ / VDDM	Analog Input 4
	EVADC_G11CH0			Analog input channel 0, group 11
	EVADC_G0CH4			Analog input channel 4, group 0
Y9	AN5	I	D / HighZ / VDDM	Analog Input 5
	EVADC_G11CH1			Analog input channel 1, group 11
	EVADC_G0CH5			Analog input channel 5, group 0

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-17 模拟输入 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
T8	AN6	I	D / HighZ / VDDM	Analog Input 6
	EVADC_G11CH2			Analog input channel 2, group 11
	EVADC_G0CH6			Analog input channel 6, group 0
U8	AN7	I	D / HighZ / VDDM	Analog Input 7
	EVADC_G11CH3			Analog input channel 3, group 11
	EVADC_G0CH7			Analog input channel 7, group 0
W8	AN8	I	D / HighZ / VDDM	Analog Input 8
	EVADC_G11CH4			Analog input channel 4, group 11
	EVADC_G1CH0			Analog input channel 0, group 1
U7	AN9	I	D / HighZ / VDDM	Analog Input 9
	EVADC_G11CH5			Analog input channel 5, group 11
	EVADC_G1CH1			Analog input channel 1, group 1
Y8	AN10	I	D / HighZ / VDDM	Analog Input 10
	EVADC_G11CH6			Analog input channel 6, group 11
	EVADC_G1CH2			Analog input channel 2, group 1
W7	AN11	I	D / HighZ / VDDM	Analog Input 11
	EVADC_G11CH7			Analog input channel 7, group 11
	EVADC_G1CH3			Analog input channel 3, group 1
T7	AN12	I	D / HighZ / VDDM	Analog Input 12
	EVADC_G1CH4			Analog input channel 4, group 1
	EDSADC_EDS0PB			Positive analog input channel 0, pin B
W6	AN13	I	D / HighZ / VDDM	Analog Input 13
	EVADC_G1CH5			Analog input channel 5, group 1
	EDSADC_EDS0NB			Negative analog input channel 0, pin B
U6	AN14	I	D / HighZ / VDDM	Analog Input 14
	EVADC_G1CH6			Analog input channel 6, group 1
	EDSADC_EDS3PB			Positive analog input channel 3, pin B
T6	AN15	I	D / HighZ / VDDM	Analog Input 15
	EVADC_G1CH7			Analog input channel 7, group 1
	EDSADC_EDS3NB			Negative analog input channel 3, pin N
W5	AN16	I	D / HighZ / VDDM	Analog Input 16
	EVADC_G2CH0			Analog input channel 0, group 2
	EVADC_FC0CH0			Analog input FC channel 0
U5	AN17/P40.10	I	S / HighZ / VDDM	Analog Input 17
	SENT_SENT10A			Receive input channel 10
	EVADC_G2CH1			Analog input channel 1, group 2
	EVADC_FC1CH0			Analog input FC channel 1

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-17 模拟输入 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
W4	AN18/P40.11	I	S / HighZ / VDDM	Analog Input 18
	SENT_SENT11A			Receive input channel 11
	EVADC_G11CH8			Analog input channel 8, group 11
	EVADC_G2CH2			Analog input channel 2, group 2
W3	AN19/P40.12	I	S / HighZ / VDDM	Analog Input 19
	SENT_SENT12A			Receive input channel 12
	EVADC_G11CH9			Analog input channel 9, group 11
	EVADC_G2CH3			Analog input channel 3, group 2
Y3	AN20	I	D / HighZ / VDDM	Analog Input 20
	EVADC_G2CH4			Analog input channel 4, group 2
	EDSADC_EDS2PA			Positive analog input channel 2, pin A
Y2	AN21	I	D / HighZ / VDDM	Analog Input 21
	EVADC_G2CH5			Analog input channel 5, group 2
	EDSADC_EDS2NA			Negative analog input channel 2, pin A
T5	AN22	I	D / HighZ / VDDM	Analog Input 22
	EVADC_G2CH6			Analog input channel 6, group 2
R5	AN23	I	D / HighZ / VDDM	Analog Input 23
	EVADC_G2CH7			Analog input channel 7, group 2
W2	AN24/P40.0	I	S / HighZ / VDDM	Analog Input 24
	SENT_SENT0A			Receive input channel 0
	EVADC_G3CH0			Analog input channel 0, group 3
	CCU60_CCPOS0D			Hall capture input 0
	EDSADC_EDS2PB			Positive analog input channel 2, pin B
W1	AN25/P40.1	I	S / HighZ / VDDM	Analog Input 25
	SENT_SENT1A			Receive input channel 1
	EVADC_G3CH1			Analog input channel 1, group 3
	CCU60_CCPOS1B			Hall capture input 1
	EDSADC_EDS2NB			Negative analog input channel 2, pin B
V2	AN26/P40.2	I	S / HighZ / VDDM	Analog Input 26
	SENT_SENT2A			Receive input channel 2
	EVADC_G3CH2			Analog input channel 2, group 3
	CCU60_CCPOS1D			Hall capture input 1
	EVADC_G11CH10			Analog input channel 10, group 11
V1	AN27/P40.3	I	S / HighZ / VDDM	Analog Input 27
	SENT_SENT3A			Receive input channel 3
	EVADC_G3CH3			Analog input channel 3, group 3
	CCU60_CCPOS2B			Hall capture input 2
	EVADC_G11CH11			Analog input channel 11, group 11

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-17 模拟输入 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
U2	AN28/P40.13	I	S / HighZ / VDDM	Analog Input 28
	SENT_SENT13A			Receive input channel 13
	EVADC_G3CH4			Analog input channel 4, group 3
U1	AN29/P40.14	I	S / HighZ / VDDM	Analog Input 29
	SENT_SENT14A			Receive input channel 14
	EVADC_G3CH5			Analog input channel 5, group 3
T4	AN30	I	D / HighZ / VDDM	Analog Input 30
	EVADC_G3CH6			Analog input channel 6, group 3
R4	AN31	I	D / HighZ / VDDM	Analog Input 31
	EVADC_G3CH7			Analog input channel 7, group 3
P4	AN32/P40.4	I	S / HighZ / VDDM	Analog Input 32
	SENT_SENT4A			Receive input channel 4
	EVADC_G8CH0			Analog input channel 0, group 8
	CCU60_CCPOS2D			Hall capture input 2
	EVADC_G11CH12			Analog input channel 12, group 11
R1	AN33/P40.5	I	S / HighZ / VDDM	Analog Input 33
	SENT_SENT5A			Receive input channel 5
	EVADC_G8CH1			Analog input channel 1, group 8
	CCU61_CCPOS0D			Hall capture input 0
	EVADC_G11CH13			Analog input channel 13, group 11
P5	AN34	I	D / HighZ / VDDM	Analog Input 34
	EVADC_G8CH2			Analog input channel 2, group 8
	EVADC_G11CH14			Analog input channel 14, group 11
R2	AN35	I	D / HighZ / VDDM	Analog Input 35
	EVADC_G8CH3			Analog input channel 3, group 8
	EVADC_G11CH15			Analog input channel 15, group 11
N4	AN36/P40.6	I	S / HighZ / VDDM	Analog Input 36
	SENT_SENT6A			Receive input channel 6
	EVADC_G8CH4			Analog input channel 4, group 8
	CCU61_CCPOS1B			Hall capture input 1
	EDSADC_EDS1PA			Positive analog input channel 1, pin A
P2	AN37/P40.7	I	S / HighZ / VDDM	Analog Input 37
	SENT_SENT7A			Receive input channel 7
	EVADC_G8CH5			Analog input channel 5, group 8
	CCU61_CCPOS1D			Hall capture input 1
	EDSADC_EDS1NA			Negative analog input channel 1, pin A

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-17 模拟输入 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
N5	AN38/P40.8	I	S / HighZ / VDDM	Analog Input 38
	SENT_SENT8A			Receive input channel 8
	EVADC_G8CH6			Analog input channel 6, group 8
	CCU61_CCPOS2B			Hall capture input 2
	EDSADC_EDS1PB			Positive analog input channel 1, pin B
P1	AN39/P40.9	I	S / HighZ / VDDM	Analog Input 39
	SENT_SENT9A			Receive input channel 9
	EVADC_G8CH7			Analog input channel 7, group 8
	CCU61_CCPOS2D			Hall capture input 2
	EDSADC_EDS1NB			Negative analog input channel 1, pin B
M5	AN40	I	D / HighZ / VDDM	Analog Input 40
	EVADC_G8CH8			Analog input channel 8, group 8
M4	AN41	I	D / HighZ / VDDM	Analog Input 41
	EVADC_G8CH9			Analog input channel 9, group 8
L5	AN42	I	D / HighZ / VDDM	Analog Input 42
	EVADC_G8CH10			Analog input channel 10, group 8
L4	AN43	I	D / HighZ / VDDM	Analog Input 43
	EVADC_G8CH11			Analog input channel 11, group 8
N1	AN44	I	D / HighZ / VDDM	Analog Input 44
	EVADC_G8CH12			Analog input channel 12, group 8
	EDSADC_EDS1PC			Positive analog input channel 1, pin C
N2	AN45	I	D / HighZ / VDDM	Analog Input 45
	EVADC_G8CH13			Analog input channel 13, group 8
	EDSADC_EDS1NC			Negative analog input channel 1, pin C
M1	AN46	I	D / HighZ / VDDM	Analog Input 46
	EVADC_G8CH14			Analog input channel 14, group 8
	EDSADC_EDS1PD			Positive analog input channel 1, pin D
M2	AN47	I	D / HighZ / VDDM	Analog Input 47
	EVADC_G8CH15			Analog input channel 15, group 8
	EDSADC_EDS1ND			Negative analog input channel 1, pin D

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

注释：端口引脚P32.0 和P32.1 是双向引脚，具有以下两个功能：

1. 如果将这些引脚用作标准GPIO，则可以使用P32.0 和P32.1 引脚配置表中定义的功能。
2. 如果引脚用作外部MOSFET 的预驱动器（内部DCDC 情况），P32.0 和P32.1 将充当名为VGATE1N 和VGATE1P 的模拟IO。

表 2-18 系统 I/O

Ball	Symbol	Ctrl.	Buffer Type	Function
Y17	VGATE1N	O	—	DCDC N ch. MOSFET gate driver output P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
W17	VGATE1P	O	—	DCDC P ch. MOSFET gate driver output P32.1 / External Pass Device gate control for EVRC
M20	XTAL1	I	XTAL / VEXT	XTAL pad1 XTAL1. Main Oscillator/PLL/Clock Generator Input.
M19	XTAL2	O	XTAL / VEXT	XTAL pad2 XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT
K16	TMS	I	FAST / PD2 / VEXT	JTAG Module State Machine Control Input TMS: JTAG Module State Machine Control Input. DAP: DAP1 Data I/O.
	DAP1	I/O		DAP: DAP1 Data I/O
L19	TRST	I	FAST / PU2 / VEXT	JTAG Module Reset/Enable Input TRST_N: JTAG Module Reset/Enable Input. DAPE: DAPE0 Clock Input
J16	TCK	I	FAST / PD2 / VEXT	JTAG Module Clock Input TCK: JTAG Module Clock Input. DAP: DAP0 Clock Input.
	DAP0	I		DAP: DAP0 Clock Input
G16	ESR1	I	FAST / PU1 / VEXT	ESR1 Port Pin input - can be used to trigger a reset or an NMI ESR1: External System Request Reset 1. Default NMI function. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter 'Reset Control Unit' and SCU_IOCRR register description. PMS_EVRWUP: EVR Wakeup Pin
	PMS_ESR1WKP	I		ESR1 pin input
G17	PORST	I/O	PORST / PD / VEXT	PORST pin Power On Reset Input. Additional strong PD in case of power fail.

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-18 系统 I/O (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
F16	ESR0	I	FAST / OD / VEXT	ESR0 Port Pin input - can be used to trigger a reset or an NMI ESR0: External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter 'Reset Control Unit' and SCU_IOC register description. PMS_EVRWUP: EVR Wakeup Pin
	PMS_ESR0WKP	I		ESR0 pin input

表 2-19 电源

Ball	Symbol	Ctrl.	Buffer Type	Function
D5	VFLEX	I	—	Digital Power Supply for Flex Port Pads (5V / 3.3V)
P8, P13, N7, N14, E15, H14, D16, G13, G8, H7	VDD	I	—	Digital Core Power Supply (1.25V)
A2, B3, V19, W20	VEXT	I	—	External Power Supply (5V / 3.3V)
Y5	VDDM	I	—	ADC Analog Power Supply (5V / 3.3V)
B18, A19	VDDP3	I	—	Flash Power Supply (3.3V)
B2, D4, E5, T16, U17, W19, Y20, E16, D17, B19, A20	VSS	I	—	Digital Ground
Y4	VSSM	I	—	Analog Ground for VDDM

TC37x 引脚定义和功能 TC37x TP 的 LFBGA-292 封装引脚

表 2-19 电源 (续)

Ball	Symbol	Ctrl.	Buffer Type	Function
P9, P12, N9, N10, N11, N12, M7, M8, M10, M11, M13, M14, L8, L9, L10, L11, L12, L13, K8, K9, K10, K11, K12, K13, J7, J8, J10, J11, J13, J14, H9, H10, H11, H12, G9, G10, G11, G12, L14, P10, P11, K7, L7	VSS	I	—	Digital Ground
L20	VSS	I	—	Oscillator Ground, VSS(OSC)
Y6	VAREF1	I	—	Positive Analog Reference Voltage 1
Y7	VAGND1	I	—	Negative Analog Reference Voltage 1
T1	VAREF2	I	—	Positive Analog Reference Voltage 2
T2	VAGND2	I	—	Negative Analog Reference Voltage 2
K14	NC	I	—	Not connected. These pins are reserved for future extensions and shall not be connected externally
A1, Y1, U4	NC1	I	—	Not connected. These pins are not connected on package level and will not be used for future extensions
T11	VEVRSB	I	—	Standby Power Supply (5V / 3.3V) for the Standby SRAM
N19	VDD	I	—	Digital Power Supply for Oscillator (1.25V), VDD(OSC)
N20	VEXT	I	—	Digital Power Supply for Oscillator (shall be supplied with same level as used for VEXT), VEXT(OSC)

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

2.2 TC37x T 和 TP 的 LQFP-176 封装引脚

注释：在以下QFP封装中，VFLEX电源内部连接到VEXT电源，因此不会在相应的封装图及电源表中显示为专用引脚。

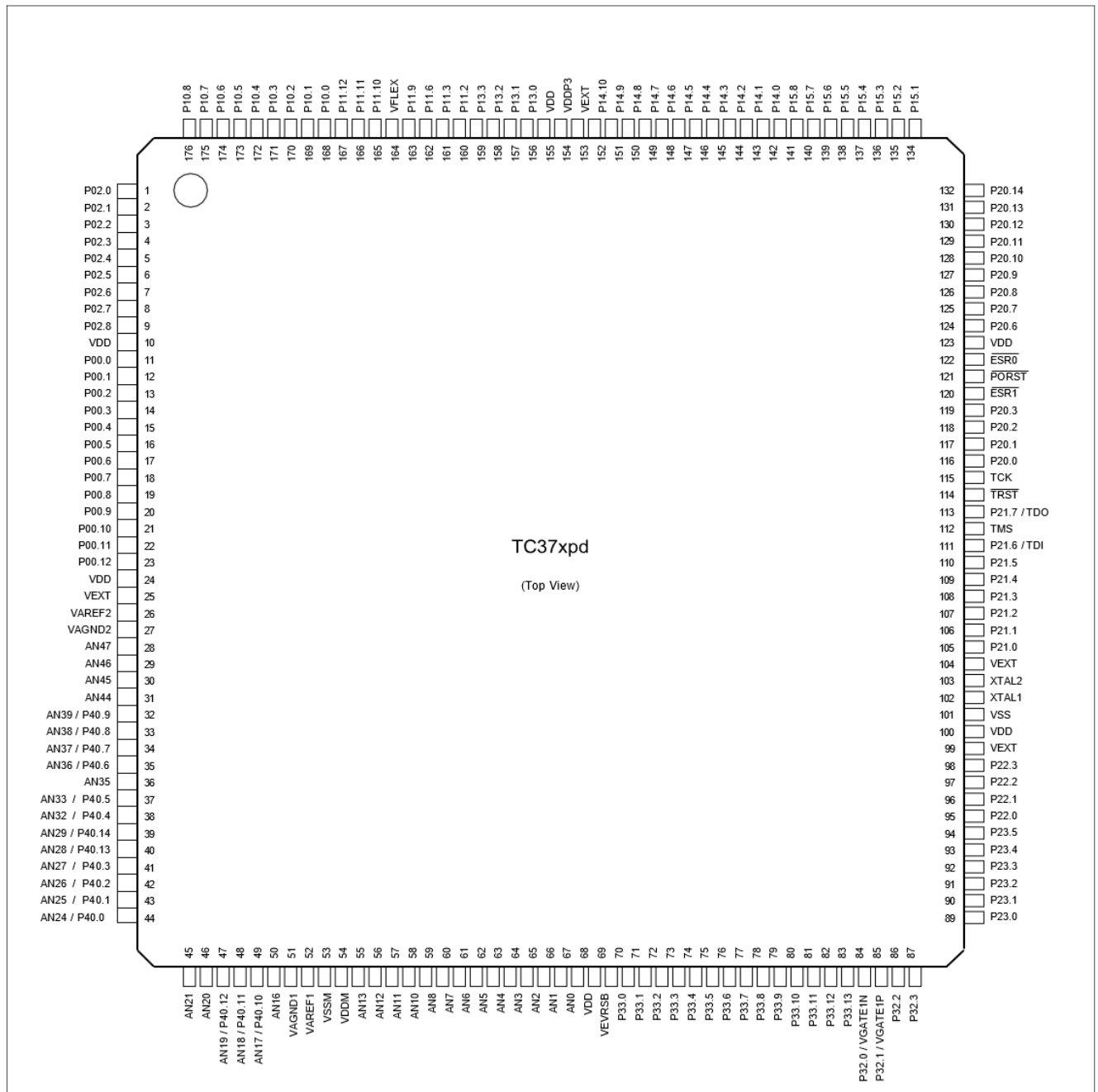


图 2-2 TC37x T 和 TP 的 LQFP-176 封装变体

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-20 端口 P00 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
11	P00.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN4_10			Mux input channel 4 of TIM module 5
	GTM_TIM3_IN0_1			Mux input channel 0 of TIM module 3
	GTM_TIM2_IN0_1			Mux input channel 0 of TIM module 2
	CCU61_CTRAPA			Trap input capture
	CCU60_T12HRE			External timer start 12
	MSC0_INJ0			Injection signal from port
	GETH_MDIOA			MDIO Input
	P00.0	O0		General-purpose output
	GTM_TOUT9	O1		GTM muxed output
	IOM_REF0_9			Reference input 0
	ASCLIN3_ASCLK	O2		Shift clock output
	ASCLIN3_ATX	O3		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	—	O4		Reserved
	CAN10_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1
	GETH_MDIO	O		MDIO Output

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-20 端口 P00 功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
12	P00.1	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN5_11			Mux input channel 5 of TIM module 5
	GTM_TIM3_IN1_1			Mux input channel 1 of TIM module 3
	GTM_TIM2_IN1_1			Mux input channel 1 of TIM module 2
	CCU60_CC60INB			T12 capture input 60
	ASCLIN3_ARXE			Receive input
	EDSADC_DSCIN5A			Modulator clock input, channel 5
	CAN10_RXDA			CAN receive input node 0
	PSI5_RX0A			RXD inputs (receive data) channel 0
	CCU61_CC60INA			T12 capture input 60
	SENT_SENT0B			Receive input channel 0
	EVADC_G9CH11	AI		Analog input channel 11, group 9
	EDSADC_EDS5NA			Negative analog input channel 5, pin A
	P00.1	O0		General-purpose output
	GTM_TOUT10	O1		GTM muxed output
	IOM_REF0_10			Reference input 0
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	—	O3		Reserved
	EDSADC_DSCOUT5	O4		Modulator clock output
	—	O5		Reserved
	SENT_SPC0	O6		Transmit output
	CCU61_CC60	O7		T12 PWM channel 60
	IOM_MON1_8			Monitor input 1
	IOM_REF1_13			Reference input 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-20 端口 P00 功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
13	P00.2	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM5_IN6_11			Mux input channel 6 of TIM module 5
	GTM_TIM3_IN1_2			Mux input channel 1 of TIM module 3
	GTM_TIM2_IN1_2			Mux input channel 1 of TIM module 2
	EDSADC_DSDIN5A			Digital datastream input, channel 5
	SENT_SENT1B			Receive input channel 1
	EVADC_G9CH10	AI		Analog input channel 10, group 9
	EDSADC_EDS5PA			Positive analog input channel 5, pin A
	P00.2	O0		General-purpose output
	GTM_TOUT11	O1		GTM muxed output
	IOM_REF0_11			Reference input 0
	ASCLIN3_ASCLK	O2		Shift clock output
	—	O3		Reserved
	PSI5_TX0	O4		TXD outputs (send data)
	IOM_MON1_14			Monitor input 1
	IOM_REF1_14			Reference input 1
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	QSPI3_SLSO4	O6		Master slave select output
	CCU61_COUT60	O7		T12 PWM channel 60
	IOM_MON1_11			Monitor input 1
	IOM_REF1_10			Reference input 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-20 端口 P00 功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
14	P00.3	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM5_IN7_10			Mux input channel 7 of TIM module 5
	GTM_TIM3_IN2_1			Mux input channel 2 of TIM module 3
	GTM_TIM2_IN2_1			Mux input channel 2 of TIM module 2
	CCU60_CC61INB			T12 capture input 61
	EDSADC_DSCIN3A			Modulator clock input, channel 3
	EDSADC_ITR5F			Trigger/Gate input, channel 5
	PSI5_RX1A			RXD inputs (receive data) channel 1
	CAN03_RXDA			CAN receive input node 3
	PSI5S_RXA			RX data input
	SENT_SENT2B			Receive input channel 2
	CCU61_CC61INA			T12 capture input 61
	EVADC_G9CH9	AI		Analog input channel 9, group 9
	EDSADC_EDS5NB	Negative analog input channel 5, pin B		
	P00.3	O0		General-purpose output
	GTM_TOUT12	O1		GTM muxed output
	IOM_REF0_12			Reference input 0
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	EDSADC_DSCOUT3	O4		Modulator clock output
	—	O5		Reserved
	SENT_SPC2	O6		Transmit output
	CCU61_CC61	O7		T12 PWM channel 61
	IOM_MON1_9			Monitor input 1
	IOM_REF1_12			Reference input 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-20 端口 P00 功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
15	P00.4	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM3_IN3_1			Mux input channel 3 of TIM module 3
	GTM_TIM2_IN3_1			Mux input channel 3 of TIM module 2
	SCU_E_REQ2_2			ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	SENT_SENT3B			Receive input channel 3
	EDSADC_DSDIN3A			Digital datastream input, channel 3
	EDSADC_SGNA			Carrier sign signal input
	ASCLIN10_ARXA			Receive input
	EVADC_G9CH8	AI		Analog input channel 8, group 9
	EDSADC_EDS5PB			Positive analog input channel 5, pin B
	P00.4	O0		General-purpose output
	GTM_TOUT13	O1		GTM muxed output
	IOM_REF0_13			Reference input 0
	PSI5S_TX	O2		TX data output
	CAN11_TXD	O3		CAN transmit output node 1
	PSI5_TX1	O4		TXD outputs (send data)
	IOM_MON1_15			Monitor input 1
	—	O5		Reserved
	SENT_SPC3	O6		Transmit output
	CCU61_COUT61	O7		T12 PWM channel 61
	IOM_MON1_12			Monitor input 1
	IOM_REF1_9			Reference input 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-20 端口 P00 功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
16	P00.5	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM3_IN4_1			Mux input channel 4 of TIM module 3
	GTM_TIM3_IN0_11			Mux input channel 0 of TIM module 3
	GTM_TIM2_IN4_1			Mux input channel 4 of TIM module 2
	CCU60_CC62INB			T12 capture input 62
	EDSADC_DSCIN2A			Modulator clock input, channel 2
	CCU61_CC62INA			T12 capture input 62
	SENT_SENT4B			Receive input channel 4
	CAN11_RXDB			CAN receive input node 1
	GTM_DTMT1_1			CDTM1_DTM0
	EVADC_G9CH7	AI		Analog input channel 7, group 9
	P00.5	O0		General-purpose output
	GTM_TOUT14	O1		GTM muxed output
	IOM_REF0_14			Reference input 0
	EDSADC_CGPWMN	O2		Negative carrier generator output
	QSPI3_SLSO3	O3		Master slave select output
	EDSADC_DSCOUT2	O4		Modulator clock output
	EVADC_FC0BFLOUT	O5		Boundary flag output, FC channel 0
	SENT_SPC4	O6		Transmit output
	CCU61_CC62	O7		T12 PWM channel 62
	IOM_MON1_10			Monitor input 1
	IOM_REF1_11			Reference input 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-20 端口 P00 功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
17	P00.6	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM3_IN5_1			Mux input channel 5 of TIM module 3
	GTM_TIM3_IN1_14			Mux input channel 1 of TIM module 3
	GTM_TIM2_IN5_1			Mux input channel 5 of TIM module 2
	EDSADC_ITR4F			Trigger/Gate input, channel 4
	EDSADC_DSDIN2A			Digital datastream input, channel 2
	SENT_SENT5B			Receive input channel 5
	ASCLIN5_ARXA			Receive input
	EVADC_G9CH6	AI		Analog input channel 6, group 9
	P00.6	O0		General-purpose output
	GTM_TOUT15	O1		GTM muxed output
	IOM_REF0_15			Reference input 0
	EDSADC_CGPWMP	O2		Positive carrier generator output
	—	O3		Reserved
	—	O4		Reserved
	EVADC_EMUX10	O5		Control of external analog multiplexer interface 1
	SENT_SPC5	O6		Transmit output
	CCU61_COUT62	O7		T12 PWM channel 62
	IOM_MON1_13			Monitor input 1
	IOM_REF1_8			Reference input 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-20 端口 P00 功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
18	P00.7	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM3_IN6_1			Mux input channel 6 of TIM module 3
	GTM_TIM3_IN2_11			Mux input channel 2 of TIM module 3
	GTM_TIM2_IN6_1			Mux input channel 6 of TIM module 2
	CCU61_CC60INC			T12 capture input 60
	SENT_SENT6B			Receive input channel 6
	EDSADC_DSCIN4A			Modulator clock input, channel 4
	GPT120_T2INA			Trigger/gate input of timer T2
	CCU61_CCPOS0A			Hall capture input 0
	CCU60_T12HRB			External timer start 12
	GTM_DTMT0_2			CDTM0_DTM0
	EVADC_G9CH5	AI		Analog input channel 5, group 9
	EDSADC_EDS4NA			Negative analog input channel 4, pin A
	P00.7	O0	General-purpose output	
	GTM_TOUT16	O1	GTM muxed output	
	ASCLIN5_ATX	O2	Transmit output	
	EVADC_FC2BFLOUT	O3	Boundary flag output, FC channel 2	
	EDSADC_DSCOUT4	O4	Modulator clock output	
	EVADC_EMUX11	O5	Control of external analog multiplexer interface 1	
	SENT_SPC6	O6	Transmit output	
	CCU61_CC60	O7	T12 PWM channel 60	
	IOM_MON1_8		Monitor input 1	
	IOM_REF1_13		Reference input 1	

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-20 端口 P00 功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
19	P00.8	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM3_IN7_1			Mux input channel 7 of TIM module 3
	GTM_TIM3_IN3_11			Mux input channel 3 of TIM module 3
	GTM_TIM2_IN7_1			Mux input channel 7 of TIM module 2
	CCU61_CC61INC			T12 capture input 61
	SENT_SENT7B			Receive input channel 7
	EDSADC_DSDIN4A			Digital datastream input, channel 4
	GPT120_T2EUDA			Count direction control input of timer T2
	CCU61_CCPOS1A			Hall capture input 1
	CCU60_T13HRB			External timer start 13
	ASCLIN10_ARXB			Receive input
	EVADC_G9CH4	AI		Analog input channel 4, group 9
	EDSADC_EDS4PA			Positive analog input channel 4, pin A
	P00.8	O0		General-purpose output
	GTM_TOUT17	O1		GTM muxed output
	QSPI3_SLSO6	O2		Master slave select output
	ASCLIN10_ATX	O3		Transmit output
	—	O4		Reserved
	EVADC_EMUX12	O5		Control of external analog multiplexer interface 1
	SENT_SPC7	O6		Transmit output
	CCU61_CC61	O7		T12 PWM channel 61
	IOM_MON1_9			Monitor input 1
	IOM_REF1_12			Reference input 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-20 端口 P00 功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
20	P00.9	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM4_IN0_7			Mux input channel 0 of TIM module 4
	GTM_TIM1_IN0_1			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_1			Mux input channel 0 of TIM module 0
	CCU61_CC62INC			T12 capture input 62
	SENT_SENT8B			Receive input channel 8
	CCU61_CCPOS2A			Hall capture input 2
	EDSADC_DSCIN1A			Modulator clock input, channel 1
	EDSADC_ITR3F			Trigger/Gate input, channel 3
	GPT120_T4EUDA			Count direction control input of timer T4
	CCU60_T13HRC			External timer start 13
	CCU60_T12HRC			External timer start 12
	EVADC_G9CH3	AI		Analog input channel 3, group 9
	EDSADC_EDS4NB			Negative analog input channel 4, pin B
	P00.9	O0		General-purpose output
	GTM_TOUT18	O1		GTM muxed output
	QSPI3_SLSO7	O2		Master slave select output
	ASCLIN3_ARTS	O3		Ready to send output
	EDSADC_DSCOUT1	O4		Modulator clock output
	ASCLIN4_ATX	O5		Transmit output
	SENT_SPC8	O6		Transmit output
	CCU61_CC62	O7		T12 PWM channel 62
	IOM_MON1_10			Monitor input 1
	IOM_REF1_11			Reference input 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-20 端口 P00 功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
21	P00.10	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM4_IN1_11			Mux input channel 1 of TIM module 4
	GTM_TIM1_IN1_1			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_1			Mux input channel 1 of TIM module 0
	SENT_SENT9B			Receive input channel 9
	EDSADC_DSDIN1A			Digital datastream input, channel 1
	EVADC_G9CH2	AI		Analog input channel 2, group 9
	EDSADC_EDS4PB	Positive analog input channel 4, pin B		
	P00.10	O0		General-purpose output
	GTM_TOUT19	O1		GTM muxed output
	ASCLIN4_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	SENT_SPC9	O6		Transmit output
	CCU61_COUT63	O7		T13 PWM channel 63
	IOM_MON1_7			Monitor input 1
	IOM_REF1_7			Reference input 1
22	P00.11	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM4_IN2_11			Mux input channel 2 of TIM module 4
	GTM_TIM1_IN2_1			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_1			Mux input channel 2 of TIM module 0
	CCU60_CTRAPA			Trap input capture
	EDSADC_DSCIN0A			Modulator clock input, channel 0
	CCU61_T12HRE			External timer start 12
	SENT_SENT10B			Receive input channel 10
	EVADC_G9CH1	AI		Analog input channel 1, group 9
	EVADC_FC3CH0	Analog input FC channel 3		
	P00.11	O0		General-purpose output
	GTM_TOUT20	O1		GTM muxed output
	ASCLIN4_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	EDSADC_DSCOUT0	O4		Modulator clock output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-20 端口 P00 功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
23	P00.12	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM4_IN3_11			Mux input channel 3 of TIM module 4
	GTM_TIM1_IN3_1			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_1			Mux input channel 3 of TIM module 0
	ASCLIN3_ACTSA			Clear to send input
	EDSADC_DSDIN0A			Digital datastream input, channel 0
	ASCLIN4_ARXA			Receive input
	SENT_SENT11B			Receive input channel 11
	EVADC_G9CH0	AI		Analog input channel 0, group 9
	EVADC_FC2CH0			Analog input FC channel 2
	P00.12	O0		General-purpose output
	GTM_TOUT21	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU61_COUT63	O7		T13 PWM channel 63
	IOM_MON1_7			Monitor input 1
	IOM_REF1_7			Reference input 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-21 端口 P02 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
1	P02.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_2			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_2			Mux input channel 0 of TIM module 0
	CCU61_CC60INB			T12 capture input 60
	ASCLIN2_ARXG			Receive input
	CCU60_CC60INA			T12 capture input 60
	SCU_E_REQ3_2			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	GTM_DTMA0_0			CDTM0_DTM4
	P02.0	O0		General-purpose output
	GTM_TOUT0	O1		GTM muxed output
	IOM_REF0_0			Reference input 0
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI3_SLSO1	O3		Master slave select output
	EDSADC_CGPWMN	O4		Negative carrier generator output
	CAN00_TXD	O5		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	ERAY0_TXDA	O6		Transmit Channel A
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
	IOM_REF1_6			Reference input 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-21 端口 P02 功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
2	P02.1	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_2			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_2			Mux input channel 1 of TIM module 0
	ERAY0_RXDA2			Receive Channel A2
	ASCLIN2_ARXB			Receive input
	CAN00_RXDA			CAN receive input node 0
	SCU_E_REQ2_1			ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P02.1	O0		General-purpose output
	GTM_TOUT1	O1		GTM muxed output
	IOM_REF0_1			Reference input 0
	QSPI4_SLSO7	O2		Master slave select output
	QSPI3_SLSO2	O3		Master slave select output
	EDSADC_CGPWMP	O4		Positive carrier generator output
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT60	O7		T12 PWM channel 60
	IOM_MON1_3			Monitor input 1
	IOM_REF1_3			Reference input 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-21 端口 P02 功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
3	P02.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_2			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_2			Mux input channel 2 of TIM module 0
	CCU61_CC61INB			T12 capture input 61
	CCU60_CC61INA			T12 capture input 61
	SENT_SENT14B			Receive input channel 14
	P02.2	O0		General-purpose output
	GTM_TOUT2	O1		GTM muxed output
	IOM_REF0_2			Reference input 0
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI3_SLSO3	O3		Master slave select output
	PSI5_TX0	O4		TXD outputs (send data)
	IOM_MON1_14			Monitor input 1
	IOM_REF1_14			Reference input 1
	CAN02_TXD	O5		CAN transmit output node 2
	IOM_MON2_7			Monitor input 2
	IOM_REF2_7			Reference input 2
	ERAY0_TXDB	O6		Transmit Channel B
	CCU60_CC61	O7		T12 PWM channel 61
	IOM_MON1_1			Monitor input 1
	IOM_REF1_5			Reference input 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-21 端口 P02 功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
4	P02.3	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN3_2			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_2			Mux input channel 3 of TIM module 0
	EDSADC_DSCIN5B			Modulator clock input, channel 5
	ERAY0_RXDB2			Receive Channel B2
	CAN02_RXDB			CAN receive input node 2
	ASCLIN1_ARXG			Receive input
	MSC1_SDI1			Upstream asynchronous input signal
	PSI5_RX0B			RXD inputs (receive data) channel 0
	SENT_SENT13B			Receive input channel 13
	P02.3	O0		General-purpose output
	GTM_TOUT3	O1		GTM muxed output
	IOM_REF0_3			Reference input 0
	ASCLIN2_ASLSO	O2		Slave select signal output
	QSPI3_SLSO4	O3		Master slave select output
	EDSADC_DSCOUT5	O4		Modulator clock output
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT61	O7		T12 PWM channel 61
	IOM_MON1_4			Monitor input 1
	IOM_REF1_2			Reference input 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-21 端口 P02 功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
5	P02.4	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN4_1			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_1			Mux input channel 4 of TIM module 0
	CCU61_CC62INB			T12 capture input 62
	EDSADC_DSDIN5B			Digital datastream input, channel 5
	QSPI3_SLSIA			Slave select input
	CCU60_CC62INA			T12 capture input 62
	I2C0_SDAA			Serial Data Input 0
	CAN11_RXDA			CAN receive input node 1
	CAN0_ECTT1			External CAN time trigger input
	SENT_SENT12B			Receive input channel 12
	P02.4	O0		General-purpose output
	GTM_TOUT4	O1		GTM muxed output
	IOM_REF0_4			Reference input 0
	ASCLIN2_ASCLK	O2		Shift clock output
	QSPI3_SLSO0	O3		Master slave select output
	PSI5S_CLK	O4		PSI5S CLK is a clock that can be used on a pin to drive the external PHY.
	I2C0_SDA	O5		Serial Data Output
	ERAY0_TXENA	O6		Transmit Enable Channel A
	CCU60_CC62	O7		T12 PWM channel 62
	IOM_MON1_0			Monitor input 1
	IOM_REF1_4			Reference input 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-21 端口 P02 功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
6	P02.5	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN5_1			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_1			Mux input channel 5 of TIM module 0
	EDSADC_DSCIN4B			Modulator clock input, channel 4
	I2C0_SCLA			Serial Clock Input 0
	PSI5_RX1B			RXD inputs (receive data) channel 1
	PSI5S_RXB			RX data input
	QSPI3_MRSTA			Master SPI data input
	SENT_SENT3C			Receive input channel 3
	CAN0_ECTT2			External CAN time trigger input
	P02.5	O0		General-purpose output
	GTM_TOUT5	O1		GTM muxed output
	IOM_REF0_5			Reference input 0
	CAN11_TXD	O2		CAN transmit output node 1
	QSPI3_MRST	O3		Slave SPI data output
	IOM_MON2_3			Monitor input 2
	IOM_REF2_3			Reference input 2
	EDSADC_DSCOUT4	O4		Modulator clock output
	I2C0_SCL	O5		Serial Clock Output
	ERAY0_TXENB	O6		Transmit Enable Channel B
	CCU60_COUT62	O7		T12 PWM channel 62
	IOM_MON1_5			Monitor input 1
	IOM_REF1_1			Reference input 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-21 端口 P02 功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
7	P02.6	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN0_10			Mux input channel 0 of TIM module 3
	GTM_TIM1_IN6_1			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_1			Mux input channel 6 of TIM module 0
	CCU60_CC60INC			T12 capture input 60
	SENT_SENT2C			Receive input channel 2
	EDSADC_DSDIN4B			Digital datastream input, channel 4
	EDSADC_ITR5E			Trigger/Gate input, channel 5
	GPT120_T3INA			Trigger/gate input of core timer T3
	CCU60_CCPOS0A			Hall capture input 0
	CCU61_T12HRB			External timer start 12
	QSPI3_MTSRA			Slave SPI data input
	P02.6	O0		General-purpose output
	GTM_TOUT6	O1		GTM muxed output
	IOM_REF0_6			Reference input 0
	PSI5S_TX	O2		TX data output
	QSPI3_MTSR	O3		Master SPI data output
	PSI5_TX1	O4		TXD outputs (send data)
	IOM_MON1_15			Monitor input 1
	EVADC_EMUX00	O5		Control of external analog multiplexer interface 0
	—	O6		Reserved
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
	IOM_REF1_6			Reference input 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-21 端口 P02 功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
8	P02.7	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN1_10			Mux input channel 1 of TIM module 3
	GTM_TIM1_IN7_1			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_1			Mux input channel 7 of TIM module 0
	CCU60_CC61INC			T12 capture input 61
	SENT_SENT1C			Receive input channel 1
	EDSADC_DSCIN3B			Modulator clock input, channel 3
	EDSADC_ITR4E			Trigger/Gate input, channel 4
	GPT120_T3EUDA			Count direction control input of core timer T3
	CCU60_CCPOS1A			Hall capture input 1
	QSPI3_SCLKA			Slave SPI clock inputs
	CCU61_T13HRB			External timer start 13
	P02.7	O0		General-purpose output
	GTM_TOUT7	O1		GTM muxed output
	IOM_REF0_7			Reference input 0
	—	O2		Reserved
	QSPI3_SCLK	O3		Master SPI clock output
	EDSADC_DSCOUT3	O4		Modulator clock output
	EVADC_EMUX01	O5		Control of external analog multiplexer interface 0
	SENT_SPC1	O6		Transmit output
	CCU60_CC61	O7		T12 PWM channel 61
	IOM_MON1_1			Monitor input 1
	IOM_REF1_5			Reference input 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-21 端口 P02 功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
9	P02.8	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN2_10			Mux input channel 2 of TIM module 3
	GTM_TIM3_IN0_2			Mux input channel 0 of TIM module 3
	GTM_TIM2_IN0_2			Mux input channel 0 of TIM module 2
	CCU60_CC62INC			T12 capture input 62
	SENT_SENT0C			Receive input channel 0
	CCU60_CCPOS2A			Hall capture input 2
	EDSADC_DSDIN3B			Digital datastream input, channel 3
	EDSADC_ITR3E			Trigger/Gate input, channel 3
	GPT120_T4INA			Trigger/gate input of timer T4
	CCU61_T12HRC			External timer start 12
	CCU61_T13HRC			External timer start 13
	GTM_DTMA0_1			CDTM0_DTM4
	P02.8	O0		General-purpose output
	GTM_TOUT8	O1		GTM muxed output
	IOM_REF0_8			Reference input 0
	QSPI3_SLSO5	O2		Master slave select output
	ASCLIN8_ASCLK	O3		Shift clock output
	—	O4		Reserved
	EVADC_EMUX02	O5		Control of external analog multiplexer interface 0
	GETH_MDC	O6		MDIO clock
	CCU60_CC62	O7		T12 PWM channel 62
	IOM_MON1_0			Monitor input 1
	IOM_REF1_4			Reference input 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-22 端口 P10 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
168	P10.0	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN0_12			Mux input channel 0 of TIM module 4
	GTM_TIM1_IN4_2			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_2			Mux input channel 4 of TIM module 0
	GPT120_T6EUIDB			Count direction control input of core timer T6
	ASCLIN11_ARXA			Receive input
	GETH_RXERC			Receive Error MII
	P10.0	O0		General-purpose output
	GTM_TOUT102	O1		GTM muxed output
	ASCLIN11_ATX	O2		Transmit output
	QSPI1_SLSO10	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
169	P10.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN4_12			Mux input channel 4 of TIM module 4
	GTM_TIM1_IN1_3			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_3			Mux input channel 1 of TIM module 0
	GPT120_T5EUIDB			Count direction control input of timer T5
	QSPI1_MRSTA			Master SPI data input
	GTM_DTMT0_1			CDTM0_DTM0
	P10.1	O0		General-purpose output
	GTM_TOUT103	O1		GTM muxed output
	QSPI1_MTSR	O2		Master SPI data output
	QSPI1_MRST	O3		Slave SPI data output
	IOM_MON2_1			Monitor input 2
	IOM_REF2_1			Reference input 2
	MSC0_EN1	O4		Chip Select
	EVADC_FC1BFLOUT	O5		Boundary flag output, FC channel 1
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-22 端口 P10 功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
170	P10.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN5_12			Mux input channel 5 of TIM module 4
	GTM_TIM1_IN2_3			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_3			Mux input channel 2 of TIM module 0
	CAN02_RXDE			CAN receive input node 2
	MSC0_SDI1			Upstream assynchronous input signal
	QSPI1_SCLKA			Slave SPI clock inputs
	GPT120_T6INB			Trigger/gate input of core timer T6
	SCU_E_REQ2_0			ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	GTM_DTMT2_2			CDTM2_DTM0
	P10.2	O0		General-purpose output
	GTM_TOUT104	O1		GTM muxed output
	IOM_MON2_9			Monitor input 2
	—	O2		Reserved
	QSPI1_SCLK	O3		Master SPI clock output
	MSC0_EN0	O4		Chip Select
	EVADC_FC3BFLOUT	O5		Boundary flag output, FC channel 3
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-22 端口 P10 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
171	P10.3	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN6_10			Mux input channel 6 of TIM module 4
	GTM_TIM1_IN3_3			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_3			Mux input channel 3 of TIM module 0
	QSPI1_MTSRA			Slave SPI data input
	SCU_E_REQ3_0			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	GPT120_T5INB			Trigger/gate input of timer T5
	P10.3	O0		General-purpose output
	GTM_TOUT105	O1		GTM muxed output
	IOM_MON2_10			Monitor input 2
	—	O2		Reserved
	QSPI1_MTSR	O3		Master SPI data output
	MSC0_EN0	O4		Chip Select
	—	O5		Reserved
	CAN02_TXD	O6		CAN transmit output node 2
	IOM_MON2_7			Monitor input 2
	IOM_REF2_7			Reference input 2
	—	O7		Reserved
172	P10.4	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN7_3			Mux input channel 7 of TIM module 4
	GTM_TIM1_IN6_2			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_2			Mux input channel 6 of TIM module 0
	QSPI1_MTSRC			Slave SPI data input
	CCU60_CCPOS0C			Hall capture input 0
	GPT120_T3INB			Trigger/gate input of core timer T3
	ASCLIN11_ARXB			Receive input
	P10.4	O0		General-purpose output
	GTM_TOUT106	O1		GTM muxed output
	IOM_MON2_11			Monitor input 2
	—	O2		Reserved
	QSPI1_SLSO8	O3		Master slave select output
	QSPI1_MTSR	O4		Master SPI data output
	MSC0_EN0	O5		Chip Select
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-22 端口 P10 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
173	P10.5	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM4_IN3_13			Mux input channel 3 of TIM module 4
	GTM_TIM1_IN2_4			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_4			Mux input channel 2 of TIM module 0
	PMS_HWCFG4IN			HWCFG4 pin input
	MSC0_INJ1			Injection signal from port
	P10.5	O0		General-purpose output
	GTM_TOUT107	O1		GTM muxed output
	IOM_REF2_9			Reference input 2
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI3_SLSO8	O3		Master slave select output
	QSPI1_SLSO9	O4		Master slave select output
	GPT120_T6OUT	O5		External output for overflow/underflow detection of core timer T6
	ASCLIN2_ASLSO	O6		Slave select signal output
	—	O7		Reserved
174	P10.6	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM4_IN2_13			Mux input channel 2 of TIM module 4
	GTM_TIM1_IN3_4			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_4			Mux input channel 3 of TIM module 0
	ASCLIN2_ARXD			Receive input
	QSPI3_MTSRB			Slave SPI data input
	PMS_HWCFG5IN			HWCFG5 pin input
	P10.6	O0		General-purpose output
	GTM_TOUT108	O1		GTM muxed output
	IOM_REF2_10			Reference input 2
	ASCLIN2_ASCLK	O2		Shift clock output
	QSPI3_MTSR	O3		Master SPI data output
	GPT120_T3OUT	O4		External output for overflow/underflow detection of core timer T3
	—	O5		Reserved
	QSPI1_MRST	O6		Slave SPI data output
	IOM_MON2_1			Monitor input 2
	IOM_REF2_1			Reference input 2
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-22 端口 P10 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
175	P10.7	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_3			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_3			Mux input channel 0 of TIM module 0
	GPT120_T3EUDB			Count direction control input of core timer T3
	ASCLIN2_ACTSA			Clear to send input
	QSPI3_MRSTB			Master SPI data input
	SCU_E_REQ0_2			ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	CCU60_CCPOS1C			Hall capture input 1
	P10.7	O0		General-purpose output
	GTM_TOUT109	O1		GTM muxed output
	IOM_REF2_11			Reference input 2
	—	O2		Reserved
	QSPI3_MRST	O3		Slave SPI data output
	IOM_MON2_3			Monitor input 2
	IOM_REF2_3			Reference input 2
	—	O4		Reserved
	—	O5		Reserved
	CAN12_TXD	O6		CAN transmit output node 2
	—	O7		Reserved
176	P10.8	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN0_13			Mux input channel 0 of TIM module 4
	GTM_TIM1_IN5_2			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_2			Mux input channel 5 of TIM module 0
	CAN12_RXDB			CAN receive input node 2
	GPT120_T4INB			Trigger/gate input of timer T4
	QSPI3_SCLKB			Slave SPI clock inputs
	SCU_E_REQ1_2			ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	CCU60_CCPOS2C			Hall capture input 2
	P10.8	O0		General-purpose output
	GTM_TOUT110	O1		GTM muxed output
	ASCLIN2_ARTS	O2		Ready to send output
	QSPI3_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-23 端口 P11 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
160	P11.2	I	RFAST / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM3_IN1_3			Mux input channel 1 of TIM module 3
	GTM_TIM2_IN1_3			Mux input channel 1 of TIM module 2
	P11.2	O0		General-purpose output
	GTM_TOUT95	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO5	O3		Master slave select output
	QSPI1_SLSO5	O4		Master slave select output
	MSC0_EN1	O5		Chip Select
	GETH_TXD1	O6		Transmit Data
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1
	161	P11.3		I
GTM_TIM3_IN2_2		Mux input channel 2 of TIM module 3		
GTM_TIM2_IN2_2		Mux input channel 2 of TIM module 2		
MSC0_SDI3		Upstream asynchronous input signal		
QSPI1_MRSTB		Master SPI data input		
P11.3		O0	General-purpose output	
GTM_TOUT96		O1	GTM muxed output	
—		O2	Reserved	
QSPI1_MRST		O3	Slave SPI data output	
IOM_MON2_1			Monitor input 2	
IOM_REF2_1			Reference input 2	
ERAY0_TXDA		O4	Transmit Channel A	
—		O5	Reserved	
GETH_TXD0		O6	Transmit Data	
CCU60_COUT62		O7	T12 PWM channel 62	
IOM_MON1_5			Monitor input 1	
IOM_REF1_1			Reference input 1	

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-23 端口 P11 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
162	P11.6	I	RFAST / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM3_IN3_2			Mux input channel 3 of TIM module 3
	GTM_TIM2_IN3_2			Mux input channel 3 of TIM module 2
	QSPI1_SCLKB			Slave SPI clock inputs
	P11.6	O0		General-purpose output
	GTM_TOUT97	O1		GTM muxed output
	ERAY0_TXENB	O2		Transmit Enable Channel B
	QSPI1_SCLK	O3		Master SPI clock output
	ERAY0_TXENA	O4		Transmit Enable Channel A
	MSC0_FCLP	O5		Shift-clock direct part of the differential signal
	GETH_TXEN	O6		Transmit Enable MII and RMII
	GETH_TCTL			Transmit Control for RGMII
	CCU60_COUT61	O7		T12 PWM channel 61
	IOM_MON1_4			Monitor input 1
	IOM_REF1_2			Reference input 1
163	P11.9	I	FAST / RGMII_In put / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM3_IN4_2			Mux input channel 4 of TIM module 3
	GTM_TIM2_IN4_2			Mux input channel 4 of TIM module 2
	QSPI1_MTSRB			Slave SPI data input
	ERAY0_RXDA1			Receive Channel A1
	GETH_RXD1A			Receive Data 1 MII, RMII and RGMII (RGMII can use RXD1A only)
	P11.9	O0		General-purpose output
	GTM_TOUT98	O1		GTM muxed output
	—	O2		Reserved
	QSPI1_MTSR	O3		Master SPI data output
	—	O4		Reserved
	MSC0_SOP	O5		Data output - direct part of the differential signal
	—	O6		Reserved
	CCU60_COUT60	O7		T12 PWM channel 60
	IOM_MON1_3			Monitor input 1
	IOM_REF1_3			Reference input 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-23 端口 P11 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
165	P11.10	I	FAST / RGMII_Input / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM3_IN5_2			Mux input channel 5 of TIM module 3
	GTM_TIM2_IN5_2			Mux input channel 5 of TIM module 2
	GTM_TIM2_IN0_9			Mux input channel 0 of TIM module 2
	CAN03_RXDD			CAN receive input node 3
	ERAY0_RXDB1			Receive Channel B1
	ASCLIN1_ARXE			Receive input
	SCU_E_REQ6_3			ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	MSC0_SDI0			Upstream assynchronous input signal
	GETH_RXD0A			Receive Data 0 MII, RMII and RGMII (RGMII can use RXD0A only)
	QSPI1_SLSIA	Slave select input		
	P11.10	O0		General-purpose output
	GTM_TOUT99	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO3	O3		Master slave select output
	QSPI1_SLSO3	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	CCU60_CC62	O7		T12 PWM channel 62
	IOM_MON1_0			Monitor input 1
IOM_REF1_4	Reference input 1			

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-23 端口 P11 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
166	P11.11	I	FAST / RGMII_In put / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM3_IN6_2			Mux input channel 6 of TIM module 3
	GTM_TIM3_IN0_14			Mux input channel 0 of TIM module 3
	GTM_TIM2_IN6_2			Mux input channel 6 of TIM module 2
	GETH_CRSDVA			Carrier Sense / Data Valid combi-signal for RMII
	GETH_RXDVA			Receive Data Valid MII
	GETH_CRSB			Carrier Sense MII
	GETH_RCTLA			Receive Control for RGMII
	P11.11			O0
	GTM_TOUT100	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO4	O3		Master slave select output
	QSPI1_SLSO4	O4		Master slave select output
	MSC0_EN0	O5		Chip Select
	ERAY0_TXENB	O6		Transmit Enable Channel B
	CCU60_CC61	O7		T12 PWM channel 61
	IOM_MON1_1			Monitor input 1
	IOM_REF1_5			Reference input 1
167	P11.12	I	FAST / RGMII_In put / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM3_IN7_2			Mux input channel 7 of TIM module 3
	GTM_TIM2_IN7_2			Mux input channel 7 of TIM module 2
	GETH_REFCLKA			Reference Clock input for RMII (50 MHz)
	GETH_TXCLKB			Transmit Clock Input for MII
	GETH_RXCLKA			Receive Clock MII
	P11.12	O0		General-purpose output
	GTM_TOUT101	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	GTM_CLK2			CGM generated clock
	ERAY0_TXDB	O4		Transmit Channel B
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	CCU_EXTCLK1			External Clock 1
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
	IOM_REF1_6			Reference input 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-24 端口 P13 的功能

Pin	Symbol	Ctrl.	Buffer Type	Function
156	P13.0	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM3_IN5_3			Mux input channel 5 of TIM module 3
	GTM_TIM2_IN5_3			Mux input channel 5 of TIM module 2
	ASCLIN10_ARXC			Receive input
	P13.0	O0		General-purpose output
	GTM_TOUT91	O1		GTM muxed output
	ASCLIN10_ATX	O2		Transmit output
	QSPI2_SCLKN	O3		Master SPI clock output (LVDS N line)
	MSC0_EN1	O4		Chip Select
	MSC0_FCLN	O5		Shift-clock inverted part of the differential signal
	—	O6		Reserved
	CAN10_TXD	O7		CAN transmit output node 0
157	P13.1	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM3_IN6_3			Mux input channel 6 of TIM module 3
	GTM_TIM2_IN6_3			Mux input channel 6 of TIM module 2
	I2C0_SCLB			Serial Clock Input 1
	CAN10_RXDD			CAN receive input node 0
	ASCLIN10_ARXD			Receive input
	P13.1	O0		General-purpose output
	GTM_TOUT92	O1		GTM muxed output
	—	O2		Reserved
	QSPI2_SCLKP	O3		Master SPI clock output (LVDS P line)
	—	O4		Reserved
	MSC0_FCLP	O5		Shift-clock direct part of the differential signal
	I2C0_SCL	O6		Serial Clock Output
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-24 端口 P13 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
158	P13.2	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM3_IN7_3			Mux input channel 7 of TIM module 3
	GTM_TIM2_IN7_3			Mux input channel 7 of TIM module 2
	GPT120_CAPINA			Trigger input to capture value of timer T5 into CAPREL register
	I2C0_SDAB			Serial Data Input 1
	P13.2	O0		General-purpose output
	GTM_TOUT93	O1		GTM muxed output
	ASCLIN10_ASCLK	O2		Shift clock output
	QSPI2_MTSRN	O3		Master SPI data output (LVDS N line)
	MSC0_FCLP	O4		Shift-clock direct part of the differential signal
	MSC0_SON	O5		Data output - inverted part of the differential signal
	I2C0_SDA	O6		Serial Data Output
	—	O7		Reserved
159	P13.3	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM3_IN0_3			Mux input channel 0 of TIM module 3
	GTM_TIM2_IN0_3			Mux input channel 0 of TIM module 2
	P13.3			General-purpose output
	GTM_TOUT94	O1		GTM muxed output
	ASCLIN10_ASLSO	O2		Slave select signal output
	QSPI2_MTSRP	O3		Master SPI data output (LVDS P line)
	—	O4		Reserved
	MSC0_SOP	O5		Data output - direct part of the differential signal
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-25 端口 P14 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
142	P14.0	I	FAST / PU1 / VEXT / ES2	General-purpose input
	GTM_TIM1_IN3_5			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_5			Mux input channel 3 of TIM module 0
	P14.0	O0		General-purpose output
	GTM_TOUT80	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	ERAY0_TXDA	O3		Transmit Channel A
	ERAY0_TXDB	O4		Transmit Channel B
	CAN01_TXD	O5		CAN transmit output node 1
	IOM_MON2_6			Monitor input 2
	IOM_REF2_6			Reference input 2
	ASCLIN0_ASCLK	O6		Shift clock output
	CCU60_COUT62	O7		T12 PWM channel 62
	IOM_MON1_5			Monitor input 1
	IOM_REF1_1			Reference input 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-25 端口 P14 功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
143	P14.1	I	FAST / PU1 / VEXT / ES2	General-purpose input
	GTM_TIM1_IN4_3			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_3			Mux input channel 4 of TIM module 0
	ERAY0_RXDA3			Receive Channel A3
	ASCLIN0_ARXA			Receive input
	ERAY0_RXDB3			Receive Channel B3
	CAN01_RXDB			CAN receive input node 1
	SCU_E_REQ3_1			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	PMS_PINAWKP			PINA (P14.1) pin input
	P14.1			O0
	GTM_TOUT81	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1
144	P14.2	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN5_3			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_3			Mux input channel 5 of TIM module 0
	PMS_HWCFG2IN			HWCFG2 pin input
	P14.2	O0		General-purpose output
	GTM_TOUT82	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI2_SLSO1	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	ASCLIN2_ASCLK	O6		Shift clock output
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-25 端口 P14 功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
145	P14.3	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_3			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_3			Mux input channel 6 of TIM module 0
	PMS_HWCFG3IN			HWCFG3 pin input
	ASCLIN2_ARXA			Receive input
	MSC0_SDI2			Upstream assynchronous input signal
	SCU_E_REQ1_0			ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P14.3	O0		General-purpose output
	GTM_TOUT83	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI2_SLSO3	O3		Master slave select output
	ASCLIN1_ASLSO	O4		Slave select signal output
	ASCLIN3_ASLSO	O5		Slave select signal output
	—	O6		Reserved
	—	O7		Reserved
146	P14.4	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN7_2			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_2			Mux input channel 7 of TIM module 0
	PMS_HWCFG6IN			HWCFG6 pin input
	GTM_DTMT0_0			CDTM0_DTM0
	P14.4	O0		General-purpose output
	GTM_TOUT84	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	GETH_PPS	O6		Pulse Per Second
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-25 端口 P14 功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
147	P14.5	I	FAST / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_4			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_4			Mux input channel 0 of TIM module 0
	PMS_HWCFG1IN			HWCFG1 pin input
	GTM_DTMA2_0			CDTM2_DTM4
	P14.5	O0		General-purpose output
	GTM_TOUT85	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	ERAY0_TXDB	O6		Transmit Channel B
	—	O7		Reserved
148	P14.6	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_4			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_4			Mux input channel 1 of TIM module 0
	P14.6	O0		General-purpose output
	GTM_TOUT86	O1		GTM muxed output
	—	O2		Reserved
	QSPI2_SLSO2	O3		Master slave select output
	CAN13_TXD	O4		CAN transmit output node 3
	—	O5		Reserved
	ERAY0_TXENB	O6		Transmit Enable Channel B
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-25 端口 P14 功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
149	P14.7	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN7_10			Mux input channel 7 of TIM module 4
	GTM_TIM1_IN0_5			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_5			Mux input channel 0 of TIM module 0
	ERAY0_RXDB0			Receive Channel B0
	CAN10_RXDB			CAN receive input node 0
	CAN13_RXDA			CAN receive input node 3
	ASCLIN9_ARXC			Receive input
	P14.7	O0		General-purpose output
	GTM_TOUT87	O1		GTM muxed output
	ASCLIN0_ARTS	O2		Ready to send output
	QSPI2_SLSO4	O3		Master slave select output
	ASCLIN9_ATX	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
150	P14.8	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN2_3			Mux input channel 2 of TIM module 3
	GTM_TIM2_IN2_3			Mux input channel 2 of TIM module 2
	ERAY0_RXDA0			Receive Channel A0
	CAN02_RXDD			CAN receive input node 2
	ASCLIN1_ARXD			Receive input
	P14.8	O0		General-purpose output
	GTM_TOUT88	O1		GTM muxed output
	ASCLIN5_ASLSO	O2		Slave select signal output
	ASCLIN7_ASLSO	O3		Slave select signal output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-25 端口 P14 功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
151	P14.9	I	LVDS_R X / FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN3_3			Mux input channel 3 of TIM module 3
	GTM_TIM2_IN3_3			Mux input channel 3 of TIM module 2
	ASCLIN0_ACTSA			Clear to send input
	QSPI2_MRSTFN			Master SPI data input (LVDS N line)
	ASCLIN9_ARXD			Receive input
	P14.9	O0		General-purpose output
	GTM_TOUT89	O1		GTM muxed output
	—	O2		Reserved
	MSC0_EN1	O3		Chip Select
	CAN10_TXD	O4		CAN transmit output node 0
	ERAY0_TXENB	O5		Transmit Enable Channel B
	ERAY0_TXENA	O6		Transmit Enable Channel A
	—	O7		Reserved
152	P14.10	I	LVDS_R X / FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN4_3			Mux input channel 4 of TIM module 3
	GTM_TIM2_IN4_3			Mux input channel 4 of TIM module 2
	QSPI2_MRSTFP			Master SPI data input (LVDS P line)
	P14.10	O0		General-purpose output
	GTM_TOUT90	O1		GTM muxed output
	—	O2		Reserved
	MSC0_EN0	O3		Chip Select
	ASCLIN1_ATX	O4		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	CAN02_TXD	O5		CAN transmit output node 2
	IOM_MON2_7			Monitor input 2
	IOM_REF2_7			Reference input 2
	ERAY0_TXDA	O6		Transmit Channel A
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-26 端口 P15 的功能

Pin	Symbol	Ctrl.	Buffer Type	Function
133	P15.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN3_4			Mux input channel 3 of TIM module 3
	GTM_TIM2_IN3_4			Mux input channel 3 of TIM module 2
	P15.0	O0		General-purpose output
	GTM_TOUT71	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI0_SLSO13	O3		Master slave select output
	—	O4		Reserved
	CAN02_TXD	O5		CAN transmit output node 2
	IOM_MON2_7			Monitor input 2
	IOM_REF2_7			Reference input 2
	ASCLIN1_ASCLK	O6		Shift clock output
	—	O7		Reserved
134	P15.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN4_4			Mux input channel 4 of TIM module 3
	GTM_TIM2_IN4_4			Mux input channel 4 of TIM module 2
	CAN02_RXDA			CAN receive input node 2
	ASCLIN1_ARXA			Receive input
	QSPI2_SLSIB			Slave select input
	SCU_E_REQ7_2			ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P15.1	O0		General-purpose output
	GTM_TOUT72	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI2_SLSO5	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-26 端口 P15 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
135	P15.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN5_4			Mux input channel 5 of TIM module 3
	GTM_TIM2_IN5_4			Mux input channel 5 of TIM module 2
	QSPI2_SLSIA			Slave select input
	SENT_SENT10D			Receive input channel 10
	QSPI2_MRSTE			Master SPI data input
	P15.2	O0		General-purpose output
	GTM_TOUT73	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	QSPI2_SLSO0	O3		Master slave select output
	—	O4		Reserved
	CAN01_TXD	O5		CAN transmit output node 1
	IOM_MON2_6			Monitor input 2
	IOM_REF2_6			Reference input 2
	ASCLIN0_ASCLK	O6		Shift clock output
	—	O7		Reserved
136	P15.3	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN6_4			Mux input channel 6 of TIM module 3
	GTM_TIM2_IN6_4			Mux input channel 6 of TIM module 2
	CAN01_RXDA			CAN receive input node 1
	ASCLIN0_ARXB			Receive input
	QSPI2_SCLKA			Slave SPI clock inputs
	P15.3	O0		General-purpose output
	GTM_TOUT74	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	MSC0_EN1	O5		Chip Select
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-26 端口 P15 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
137	P15.4	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN7_4			Mux input channel 7 of TIM module 3
	GTM_TIM2_IN7_4			Mux input channel 7 of TIM module 2
	I2C0_SCLC			Serial Clock Input 2
	QSPI2_MRSTA			Master SPI data input
	SCU_E_REQ0_0			ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	SENT_SENT11D			Receive input channel 11
	P15.4	O0		General-purpose output
	GTM_TOUT75	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI2_MRST	O3		Slave SPI data output
	IOM_MON2_2			Monitor input 2
	IOM_REF2_2			Reference input 2
	—	O4		Reserved
	—	O5		Reserved
	I2C0_SCL	O6		Serial Clock Output
	CCU60_CC62	O7		T12 PWM channel 62
	IOM_MON1_0			Monitor input 1
	IOM_REF1_4			Reference input 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-26 端口 P15 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
138	P15.5	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN0_4			Mux input channel 0 of TIM module 3
	GTM_TIM2_IN0_4			Mux input channel 0 of TIM module 2
	ASCLIN1_ARXB			Receive input
	I2C0_SDAC			Serial Data Input 2
	QSPI2_MTSRA			Slave SPI data input
	SCU_E_REQ4_3			ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P15.5	O0		General-purpose output
	GTM_TOUT76	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI2_MTSR	O3		Master SPI data output
	—	O4		Reserved
	MSC0_EN0	O5		Chip Select
	I2C0_SDA	O6		Serial Data Output
	CCU60_CC61	O7		T12 PWM channel 61
	IOM_MON1_1			Monitor input 1
	IOM_REF1_5			Reference input 1
139	P15.6	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN2_14			Mux input channel 2 of TIM module 2
	GTM_TIM1_IN0_6			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_6			Mux input channel 0 of TIM module 0
	QSPI2_MTSRB			Slave SPI data input
	P15.6	O0		General-purpose output
	GTM_TOUT77	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	QSPI2_MTSR	O3		Master SPI data output
	—	O4		Reserved
	QSPI2_SCLK	O5		Master SPI clock output
	ASCLIN3_ASCLK	O6		Shift clock output
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
	IOM_REF1_6			Reference input 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-26 端口 P15 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
140	P15.7	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_5			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_5			Mux input channel 1 of TIM module 0
	ASCLIN3_ARXA			Receive input
	QSPI2_MRSTB			Master SPI data input
	P15.7	O0		General-purpose output
	GTM_TOUT78	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	QSPI2_MRST	O3		Slave SPI data output
	IOM_MON2_2			Monitor input 2
	IOM_REF2_2			Reference input 2
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT60	O7		T12 PWM channel 60
	IOM_MON1_3			Monitor input 1
	IOM_REF1_3			Reference input 1
141	P15.8	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_5			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_5			Mux input channel 2 of TIM module 0
	QSPI2_SCLKB			Slave SPI clock inputs
	SCU_E_REQ5_0			ERU Channel 5 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P15.8	O0		General-purpose output
	GTM_TOUT79	O1		GTM muxed output
	—	O2		Reserved
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	ASCLIN3_ASCLK	O6		Shift clock output
	CCU60_COUT61	O7		T12 PWM channel 61
	IOM_MON1_4			Monitor input 1
	IOM_REF1_2			Reference input 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-27 端口 P20 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
116	P20.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_7			Mux input channel 6 of TIM module 1
	GTM_TIM1_IN4_9			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN6_7			Mux input channel 6 of TIM module 0
	CAN03_RXDC			CAN receive input node 3
	CCU_PAD_SYSCLK			Sysclk input
	CBS_TGI0			Trigger input
	SCU_E_REQ6_0			ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	GPT120_T6EUDA			Count direction control input of core timer T6
	P20.0	O0		General-purpose output
	GTM_TOUT59	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	ASCLIN3_ASCLK	O3		Shift clock output
	—	O4		Reserved
	HSCT0_SYSCLK_OUT	O5		sys clock output
	—	O6		Reserved
	—	O7		Reserved
	CBS_TGO0	O		Trigger output
117	P20.1	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN4_11			Mux input channel 4 of TIM module 4
	GTM_TIM3_IN3_5			Mux input channel 3 of TIM module 3
	GTM_TIM2_IN3_5			Mux input channel 3 of TIM module 2
	CBS_TGI1			Trigger input
	GTM_DTMA1_1			CDTM1_DTM4
	P20.1	O0		General-purpose output
	GTM_TOUT60	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	CBS_TGO1	O		Trigger output

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-27 端口 P20 功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function	
118	P20.2	I	S / PU / VEXT	General-purpose input This pin is latched at power on reset release to enter test mode.	
	TESTMODE			Testmode Enable Input	
119	P20.3	I	SLOW / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM4_IN5_11			Mux input channel 5 of TIM module 4	
	GTM_TIM3_IN4_5			Mux input channel 4 of TIM module 3	
	GTM_TIM2_IN4_5			Mux input channel 4 of TIM module 2	
	ASCLIN3_ARXC			Receive input	
	GPT120_T6INA			Trigger/gate input of core timer T6	
	P20.3			O0	General-purpose output
	GTM_TOUT61			O1	GTM muxed output
	ASCLIN3_ATX			O2	Transmit output
	IOM_MON2_15				Monitor input 2
	IOM_REF2_15				Reference input 2
	QSPI0_SLSO9				O3
	QSPI2_SLSO9			O4	Master slave select output
	CAN03_TXD			O5	CAN transmit output node 3
	IOM_MON2_8				Monitor input 2
	IOM_REF2_8				Reference input 2
	—			O6	Reserved
	—			O7	Reserved
124	P20.6	I	SLOW / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM3_IN6_5			Mux input channel 6 of TIM module 3	
	GTM_TIM2_IN6_5			Mux input channel 6 of TIM module 2	
	CAN12_RXDA			CAN receive input node 2	
	ASCLIN9_ARXE			Receive input	
	P20.6			O0	General-purpose output
	GTM_TOUT62			O1	GTM muxed output
	ASCLIN1_ARTS			O2	Ready to send output
	QSPI0_SLSO8			O3	Master slave select output
	QSPI2_SLSO8			O4	Master slave select output
	—			O5	Reserved
	—			O6	Reserved
	—			O7	Reserved

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-27 端口 P20 功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
125	P20.7	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN7_5			Mux input channel 7 of TIM module 3
	GTM_TIM2_IN7_5			Mux input channel 7 of TIM module 2
	GTM_TIM1_IN5_8			Mux input channel 5 of TIM module 1
	CAN00_RXDB			CAN receive input node 0
	ASCLIN1_ACTSA			Clear to send input
	ASCLIN9_ARXF			Receive input
	P20.7	O0		General-purpose output
	GTM_TOUT63	O1		GTM muxed output
	ASCLIN9_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	CAN12_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	CCU61_COUT63	O7		T13 PWM channel 63
	IOM_MON1_7			Monitor input 1
	IOM_REF1_7			Reference input 1
126	P20.8	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN7_3			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_3			Mux input channel 7 of TIM module 0
	P20.8	O0		General-purpose output
	GTM_TOUT64	O1		GTM muxed output
	ASCLIN1_ASLSO	O2		Slave select signal output
	QSPI0_SLSO0	O3		Master slave select output
	QSPI1_SLSO0	O4		Master slave select output
	CAN00_TXD	O5		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	—	O6		Reserved
	CCU61_CC60	O7		T12 PWM channel 60
	IOM_MON1_8			Monitor input 1
	IOM_REF1_13			Reference input 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-27 端口 P20 功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
127	P20.9	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN5_5			Mux input channel 5 of TIM module 3
	GTM_TIM2_IN5_5			Mux input channel 5 of TIM module 2
	CAN03_RXDE			CAN receive input node 3
	ASCLIN1_ARXC			Receive input
	QSPI0_SLSIB			Slave select input
	SCU_E_REQ7_0			ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P20.9	O0		General-purpose output
	GTM_TOUT65	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO1	O3		Master slave select output
	QSPI1_SLSO1	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	CCU61_CC61	O7		T12 PWM channel 61
	IOM_MON1_9			Monitor input 1
	IOM_REF1_12			Reference input 1
128	P20.10	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN6_6			Mux input channel 6 of TIM module 3
	GTM_TIM2_IN6_6			Mux input channel 6 of TIM module 2
	P20.10	O0		General-purpose output
	GTM_TOUT66	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI0_SLSO6	O3		Master slave select output
	QSPI2_SLSO7	O4		Master slave select output
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	ASCLIN1_ASCLK	O6		Shift clock output
	CCU61_CC62	O7		T12 PWM channel 62
	IOM_MON1_10			Monitor input 1
	IOM_REF1_11			Reference input 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-27 端口 P20 功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
129	P20.11	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN7_6			Mux input channel 7 of TIM module 3
	GTM_TIM2_IN7_6			Mux input channel 7 of TIM module 2
	QSPI0_SCLKA			Slave SPI clock inputs
	P20.11	O0		General-purpose output
	GTM_TOUT67	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU61_COUT60	O7		T12 PWM channel 60
	IOM_MON1_11			Monitor input 1
	IOM_REF1_10			Reference input 1
130	P20.12	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN0_5			Mux input channel 0 of TIM module 3
	GTM_TIM2_IN0_5			Mux input channel 0 of TIM module 2
	QSPI0_MRSTA			Master SPI data input
	IOM_PIN_13			GPIO pad input to FPC
	P20.12	O0		General-purpose output
	GTM_TOUT68	O1		GTM muxed output
	IOM_MON0_13			Monitor input 0
	—	O2		Reserved
	QSPI0_MRST	O3		Slave SPI data output
	IOM_MON2_0			Monitor input 2
	IOM_REF2_0			Reference input 2
	QSPI0_MTSR	O4		Master SPI data output
	—	O5		Reserved
	—	O6		Reserved
	CCU61_COUT61	O7		T12 PWM channel 61
	IOM_MON1_12			Monitor input 1
	IOM_REF1_9			Reference input 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-27 端口 P20 功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
131	P20.13	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN1_4			Mux input channel 1 of TIM module 3
	GTM_TIM2_IN1_4			Mux input channel 1 of TIM module 2
	QSPI0_SLSIA			Slave select input
	IOM_PIN_14			GPIO pad input to FPC
	P20.13	O0		General-purpose output
	GTM_TOUT69	O1		GTM muxed output
	IOM_MON0_14			Monitor input 0
	—	O2		Reserved
	QSPI0_SLSO2	O3		Master slave select output
	QSPI1_SLSO2	O4		Master slave select output
	QSPI0_SCLK	O5		Master SPI clock output
	—	O6		Reserved
	CCU61_COUT62	O7		T12 PWM channel 62
	IOM_MON1_13			Monitor input 1
	IOM_REF1_8			Reference input 1
132	P20.14	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM3_IN2_4			Mux input channel 2 of TIM module 3
	GTM_TIM2_IN2_4			Mux input channel 2 of TIM module 2
	QSPI0_MTSRA			Slave SPI data input
	IOM_PIN_15			GPIO pad input to FPC
	P20.14	O0		General-purpose output
	GTM_TOUT70	O1		GTM muxed output
	IOM_MON0_15			Monitor input 0
	—	O2		Reserved
	QSPI0_MTSR	O3		Master SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-28 端口 P21 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
105	P21.0	I	LVDS_RX / FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN0_11			Mux input channel 0 of TIM module 4
	GTM_TIM3_IN4_6			Mux input channel 4 of TIM module 3
	GTM_TIM2_IN4_6			Mux input channel 4 of TIM module 2
	QSPI4_MRSTDN			Master SPI data input (LVDS N line)
	DMU_FDEST			Enter destructive debug mode
	ASCLIN11_ARXC			Receive input
	P21.0	O0		General-purpose output
	GTM_TOUT51	O1		GTM muxed output
	ASCLIN11_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	HSM_HSM1	O		Pin Output Value
106	P21.1	I	LVDS_RX / FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM4_IN1_13			Mux input channel 1 of TIM module 4
	GTM_TIM3_IN5_6			Mux input channel 5 of TIM module 3
	GTM_TIM2_IN5_6			Mux input channel 5 of TIM module 2
	QSPI4_MRSTDP			Master SPI data input (LVDS P line)
	ASCLIN11_ARXD			Receive input
	GTM_DTMA4_1			CDTM4_DTM4
	P21.1	O0		General-purpose output
	GTM_TOUT52	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	HSM_HSM2	O		Pin Output Value

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-28 端口 P21 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
107	P21.2	I	LVDS_RX / FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN4_11			Mux input channel 4 of TIM module 5
	GTM_TIM1_IN0_7			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_7			Mux input channel 0 of TIM module 0
	QSPI2_MRSTCN			Master SPI data input (LVDS N line)
	SCU_EMGSTOP_POR T_B			Emergency stop Port Pin B input request
	ASCLIN3_ARXGN			Differential Receive input (low active)
	HSCT0_RXDN			Rx data
	QSPI4_MRSTCN			Master SPI data input (LVDS N line)
	ASCLIN11_ARXE			Receive input
	GTM_DTMA1_0			CDTM1_DTM4
	P21.2	O0		General-purpose output
	GTM_TOUT53	O1		GTM muxed output
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	GETH_MDC	O5		MDIO clock
	—	O6		Reserved
	—	O7		Reserved
108	P21.3	I	LVDS_RX / FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM5_IN5_12			Mux input channel 5 of TIM module 5
	GTM_TIM1_IN1_6			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_6			Mux input channel 1 of TIM module 0
	QSPI2_MRSTCP			Master SPI data input (LVDS P line)
	ASCLIN3_ARXGP			Differential Receive input (high active)
	GETH_MDIOD			MDIO Input
	HSCT0_RXDP			Rx data
	QSPI4_MRSTCP			Master SPI data input (LVDS P line)
	P21.3	O0		General-purpose output
	GTM_TOUT54	O1		GTM muxed output
	ASCLIN11_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	GETH_MDIO	O		MDIO Output

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-28 端口 P21 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
109	P21.4	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM5_IN6_12			Mux input channel 6 of TIM module 5
	GTM_TIM1_IN2_6			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_6			Mux input channel 2 of TIM module 0
	P21.4	O0		General-purpose output
	GTM_TOUT55	O1		GTM muxed output
	ASCLIN11_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	HSCT0_TXDN	O		Tx data
110	P21.5	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM5_IN7_11			Mux input channel 7 of TIM module 5
	GTM_TIM1_IN3_6			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_6			Mux input channel 3 of TIM module 0
	ASCLIN11_ARXF			Receive input
	P21.5	O0		General-purpose output
	GTM_TOUT56	O1		GTM muxed output
	ASCLIN3_ASCLK	O2		Shift clock output
	ASCLIN11_ATX	O3		Transmit output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	HSCT0_TXDP	O		Tx data

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-28 端口 P21 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
111	P21.6/TDI	I	FAST / PD / PU2 / VEXT / ES3	General-purpose input PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ. DAPE: DAPE1 Data I/O.
	GTM_TIM4_IN2_12			Mux input channel 2 of TIM module 4
	GTM_TIM1_IN4_8			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_8			Mux input channel 4 of TIM module 0
	GPT120_T5EUDA			Count direction control input of timer T5
	ASCLIN3_ARXF			Receive input
	CBS_TGI2			Trigger input
	TDI			JTAG Module Data Input
	P21.6	O0		General-purpose output
	GTM_TOUT57	O1		GTM muxed output
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	GPT120_T3OUT	O7		External output for overflow/underflow detection of core timer T3
	CBS_TGO2	O		Trigger output
	DAP3	I/O		DAP: DAP3 Data I/O

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-28 端口 P21 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
113	P21.7/TDO	I	FAST / PU2 / VEXT / ES4	General-purpose input DAP: DAP2 Data I/O; DAPE: DAPE2 Data I/O.
	GTM_TIM4_IN3_12			Mux input channel 3 of TIM module 4
	GTM_TIM1_IN5_7			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_7			Mux input channel 5 of TIM module 0
	GPT120_T5INA			Trigger/gate input of timer T5
	CBS_TGI3			Trigger input
	GETH_RXERB			Receive Error MII
	P21.7	O0		General-purpose output
	GTM_TOUT58	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	ASCLIN3_ASCLK	O3		Shift clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	GPT120_T6OUT	O7		External output for overflow/underflow detection of core timer T6
	CBS_TGO3	O		Trigger output
	DAP2	I/O		DAP: DAP2 Data I/O
	TDO	O		JTAG Module Data Output

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-29 端口 P22 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
95	P22.0	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN1_7			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_7			Mux input channel 1 of TIM module 0
	QSPI4_MTSRB			Slave SPI data input
	ASCLIN6_ARXE			Receive input
	P22.0	O0		General-purpose output
	GTM_TOUT47	O1		GTM muxed output
	ASCLIN3_ATXN	O2		Differential Transmit output (low active)
	QSPI4_MTSR	O3		Master SPI data output
	QSPI4_SCLKN	O4		Master SPI clock output (LVDS N line)
	MSC1_FCLN	O5		Shift-clock inverted part of the differential signal
	—	O6		Reserved
	ASCLIN6_ATX	O7		Transmit output
96	P22.1	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN0_8			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_8			Mux input channel 0 of TIM module 0
	QSPI4_MRSTB			Master SPI data input
	ASCLIN7_ARXE			Receive input
	P22.1	O0		General-purpose output
	GTM_TOUT48	O1		GTM muxed output
	ASCLIN3_ATXP	O2		Differential Transmit output (high active)
	QSPI4_MRST	O3		Slave SPI data output
	IOM_MON2_4			Monitor input 2
	IOM_REF2_4			Reference input 2
	QSPI4_SCLKP	O4		Master SPI clock output (LVDS P line)
	MSC1_FCLP	O5		Shift-clock direct part of the differential signal
	—	O6		Reserved
	ASCLIN7_ATX	O7		Transmit output

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-29 端口 P22 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
97	P22.2	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN3_7			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_7			Mux input channel 3 of TIM module 0
	QSPI4_SLSIB			Slave select input
	P22.2	O0		General-purpose output
	GTM_TOUT49	O1		GTM muxed output
	ASCLIN5_ATX	O2		Transmit output
	QSPI4_SLSO3	O3		Master slave select output
	QSPI4_MTSRN	O4		Master SPI data output (LVDS N line)
	MSC1_SON	O5		Data output - inverted part of the differential signal
	—	O6		Reserved
	—	O7		Reserved
98	P22.3	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN4_4			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_4			Mux input channel 4 of TIM module 0
	QSPI4_SCLKB			Slave SPI clock inputs
	ASCLIN5_ARXC			Receive input
	P22.3	O0		General-purpose output
	GTM_TOUT50	O1		GTM muxed output
	—	O2		Reserved
	QSPI4_SCLK	O3		Master SPI clock output
	QSPI4_MTSRP	O4		Master SPI data output (LVDS P line)
	MSC1_SOP	O5		Data output - direct part of the differential signal
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-30 端口 P23 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
89	P23.0	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN5_4			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_4			Mux input channel 5 of TIM module 0
	CAN10_RXDC			CAN receive input node 0
	P23.0	O0		General-purpose output
	GTM_TOUT41	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
90	P23.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_4			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_4			Mux input channel 6 of TIM module 0
	MSC1_SDIO			Upstream asynchronous input signal
	ASCLIN6_ARXF			Receive input
	P23.1	O0		General-purpose output
	GTM_TOUT42	O1		GTM muxed output
	ASCLIN1_ARTS	O2		Ready to send output
	QSPI4_SLSO6	O3		Master slave select output
	GTM_CLK0	O4		CGM generated clock
	CAN10_TXD	O5		CAN transmit output node 0
	CCU_EXTCLK0	O6		External Clock 0
	ASCLIN6_ASCLK	O7		Shift clock output
91	P23.2	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_5			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_5			Mux input channel 6 of TIM module 0
	ASCLIN7_ARXC			Receive input
	P23.2	O0		General-purpose output
	GTM_TOUT43	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	CAN12_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-30 端口 P23 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
92	P23.3	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN7_4			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_4			Mux input channel 7 of TIM module 0
	MSC1_INJ0			Injection signal from port
	ASCLIN6_ARXA			Receive input
	CAN12_RXDC			CAN receive input node 2
	P23.3	O0		General-purpose output
	GTM_TOUT44	O1		GTM muxed output
	ASCLIN7_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
93	P23.4	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN7_5			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_5			Mux input channel 7 of TIM module 0
	P23.4	O0		General-purpose output
	GTM_TOUT45	O1		GTM muxed output
	ASCLIN6_ASLSO	O2		Slave select signal output
	QSPI4_SLSO5	O3		Master slave select output
	—	O4		Reserved
	MSC1_EN0	O5		Chip Select
	—	O6		Reserved
	—	O7		Reserved
94	P23.5	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_7			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_7			Mux input channel 2 of TIM module 0
	P23.5	O0		General-purpose output
	GTM_TOUT46	O1		GTM muxed output
	ASCLIN6_ATX	O2		Transmit output
	QSPI4_SLSO4	O3		Master slave select output
	—	O4		Reserved
	MSC1_EN1	O5		Chip Select
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-31 端口 P32 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
84	P32.0	I	SLOW / PU1 / VEXT / ES	General-purpose input P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
	GTM_TIM3_IN2_5			Mux input channel 2 of TIM module 3
	GTM_TIM2_IN2_5			Mux input channel 2 of TIM module 2
	P32.0	O0		General-purpose output
	GTM_TOUT36	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
85	P32.1	I	SLOW / PU1 / VEXT / ES	General-purpose input P32.1 / External Pass Device gate control for EVRC
	GTM_TIM3_IN3_15			Mux input channel 3 of TIM module 3
	P32.1	O0		General-purpose output
	GTM_TOUT37	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-31 端口 P32 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
86	P32.2	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN3_8			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_8			Mux input channel 3 of TIM module 0
	CAN03_RXDB			CAN receive input node 3
	ASCLIN3_ARXD			Receive input
	P32.2	O0		General-purpose output
	GTM_TOUT38	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	PMS_DCDCSYNCO	O6		DC-DC synchronization output
	—	O7		Reserved
87	P32.3	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN4_5			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_5			Mux input channel 4 of TIM module 0
	P32.3	O0		General-purpose output
	GTM_TOUT39	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	—	O3		Reserved
	ASCLIN3_ASCLK	O4		Shift clock output
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-31 端口 P32 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
88	P32.4	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN5_5			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_5			Mux input channel 5 of TIM module 0
	ASCLIN1_ACTSB			Clear to send input
	MSC1_SDI2			Upstream assynchronous input signal
	P32.4	O0		General-purpose output
	GTM_TOUT40	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	GTM_CLK1	O4		CGM generated clock
	MSC1_EN0	O5		Chip Select
	CCU_EXTCLK1	O6		External Clock 1
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1
	PMS_DCDCSYNCO	O		DC-DC synchronization output

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-32 端口 P33 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
70	P33.0	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM3_IN0_13			Mux input channel 0 of TIM module 3
	GTM_TIM1_IN4_6			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_6			Mux input channel 4 of TIM module 0
	EDSADC_ITR0E			Trigger/Gate input, channel 0
	SENT_SENT13C			Receive input channel 13
	IOM_PIN_0			GPIO pad input to FPC
	GTM_DTMT1_2			CDTM1_DTM0
	EVADC_G10CH7	AI		Analog input channel 7, group 10
	P33.0	O0		General-purpose output
	GTM_TOUT22	O1		GTM muxed output
	IOM_MON0_0			Monitor input 0
	IOM_GTM_0			GTM-provided inputs to EXOR combiner
	ASCLIN5_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	EVADC_FC2BFLOUT	O6		Boundary flag output, FC channel 2
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-32 端口 P33 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
71	P33.1	I	SLOW / PU1 / VEVRB / ES5	General-purpose input
	GTM_TIM3_IN1_15			Mux input channel 1 of TIM module 3
	GTM_TIM1_IN5_6			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_6			Mux input channel 5 of TIM module 0
	EDSADC_ITR1E			Trigger/Gate input, channel 1
	PSI5_RX0C			RXD inputs (receive data) channel 0
	EDSADC_DSCIN2B			Modulator clock input, channel 2
	SENT_SENT9C			Receive input channel 9
	ASCLIN8_ARXC			Receive input
	IOM_PIN_1			GPIO pad input to FPC
	EVADC_G10CH6	AI		Analog input channel 6, group 10
	P33.1	O0		General-purpose output
	GTM_TOUT23	O1		GTM muxed output
	IOM_MON0_1			Monitor input 0
	IOM_GTM_1			GTM-provided inputs to EXOR combiner
	ASCLIN3_ASLSO	O2		Slave select signal output
	QSPI2_SCLK	O3		Master SPI clock output
	EDSADC_DSCOUT2	O4		Modulator clock output
	EVADC_EMUX02	O5		Control of external analog multiplexer interface 0
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-32 端口 P33 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
72	P33.2	I	SLOW / PU1 / VEVR SB / ES5	General-purpose input
	GTM_TIM3_IN2_14			Mux input channel 2 of TIM module 3
	GTM_TIM1_IN6_6			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_6			Mux input channel 6 of TIM module 0
	EDSADC_ITR2E			Trigger/Gate input, channel 2
	SENT_SENT8C			Receive input channel 8
	EDSADC_DSDIN2B			Digital datastream input, channel 2
	IOM_PIN_2			GPIO pad input to FPC
	EVADC_G10CH5	AI		Analog input channel 5, group 10
	P33.2	O0		General-purpose output
	GTM_TOUT24	O1		GTM muxed output
	IOM_MON0_2			Monitor input 0
	IOM_GTM_2			GTM-provided inputs to EXOR combiner
	ASCLIN3_ASCLK			O2
	QSPI2_SLSO10	O3		Master slave select output
	PSI5_TX0	O4		TXD outputs (send data)
	IOM_MON1_14			Monitor input 1
	IOM_REF1_14			Reference input 1
	EVADC_EMUX01	O5		Control of external analog multiplexer interface 0
	EVADC_FC3BFLOUT	O6		Boundary flag output, FC channel 3
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-32 端口 P33 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
73	P33.3	I	SLOW / PU1 / VEVRB / ES5	General-purpose input
	GTM_TIM3_IN3_12			Mux input channel 3 of TIM module 3
	GTM_TIM1_IN7_6			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_6			Mux input channel 7 of TIM module 0
	PSI5_RX1C			RXD inputs (receive data) channel 1
	SENT_SENT7C			Receive input channel 7
	EDSADC_DSCIN1B			Modulator clock input, channel 1
	IOM_PIN_3			GPIO pad input to FPC
	EVADC_G10CH4	AI		Analog input channel 4, group 10
	P33.3	O0		General-purpose output
	GTM_TOUT25	O1		GTM muxed output
	IOM_MON0_3			Monitor input 0
	IOM_GTM_3			GTM-provided inputs to EXOR combiner
	ASCLIN5_ASCLK	O2		Shift clock output
	QSPI4_SLSO2	O3		Master slave select output
	EDSADC_DSCOUT1	O4		Modulator clock output
	EVADC_EMUX00	O5		Control of external analog multiplexer interface 0
	—	O6		Reserved
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-32 端口 P33 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
74	P33.4	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM4_IN4_10			Mux input channel 4 of TIM module 4
	GTM_TIM1_IN0_10			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_10			Mux input channel 0 of TIM module 0
	EDSADC_ITR0F			Trigger/Gate input, channel 0
	SENT_SENT6C			Receive input channel 6
	EDSADC_DSDIN1B			Digital datastream input, channel 1
	CCU61_CTRAPC			Trap input capture
	ASCLIN5_ARXB			Receive input
	IOM_PIN_4			GPIO pad input to FPC
	GTM_DTMT2_0			CDTM2_DTM0
	EVADC_G10CH3	AI		Analog input channel 3, group 10
	P33.4	O0	General-purpose output	
	GTM_TOUT26	O1	GTM muxed output	
	IOM_MON0_4		Monitor input 0	
	IOM_GTM_4		GTM-provided inputs to EXOR combiner	
	ASCLIN2_ARTS	O2	Ready to send output	
	QSPI2_SLSO12	O3	Master slave select output	
	PSI5_TX1	O4	TXD outputs (send data)	
	IOM_MON1_15		Monitor input 1	
	EVADC_EMUX12	O5	Control of external analog multiplexer interface 1	
	EVADC_FC0BFLOUT	O6	Boundary flag output, FC channel 0	
	CAN13_TXD	O7	CAN transmit output node 3	

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-32 端口 P33 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
75	P33.5	I	SLOW / PU1 / VEVR SB / ES5	General-purpose input
	GTM_TIM4_IN5_10			Mux input channel 5 of TIM module 4
	GTM_TIM1_IN1_8			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_8			Mux input channel 1 of TIM module 0
	EDSADC_DSCIN0B			Modulator clock input, channel 0
	EDSADC_ITR1F			Trigger/Gate input, channel 1
	GPT120_T4EUDB			Count direction control input of timer T4
	PSI5S_RXC			RX data input
	ASCLIN2_ACTSB			Clear to send input
	CCU61_CCPOS2C			Hall capture input 2
	SENT_SENT5C			Receive input channel 5
	CAN13_RXDB			CAN receive input node 3
	IOM_PIN_5			GPIO pad input to FPC
	EVADC_G10CH2	AI		Analog input channel 2, group 10
	P33.5	O0		General-purpose output
	GTM_TOUT27	O1		GTM muxed output
	IOM_MON0_5			Monitor input 0
	IOM_GTM_5			GTM-provided inputs to EXOR combiner
	QSPI0_SLSO7	O2		Master slave select output
	QSPI1_SLSO7	O3		Master slave select output
	EDSADC_DSCOUT0	O4		Modulator clock output
	EVADC_EMUX11	O5		Control of external analog multiplexer interface 1
	EVADC_FC2BFLOUT	O6		Boundary flag output, FC channel 2
	ASCLIN5_ASLSO	O7		Slave select signal output

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-32 端口 P33 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
76	P33.6	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN2_9			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_9			Mux input channel 2 of TIM module 0
	EDSADC_ITR2F			Trigger/Gate input, channel 2
	GPT120_T2EADB			Count direction control input of timer T2
	SENT_SENT4C			Receive input channel 4
	CCU61_CCPOS1C			Hall capture input 1
	EDSADC_DSDIN0B			Digital datastream input, channel 0
	ASCLIN8_ARXD			Receive input
	IOM_PIN_6			GPIO pad input to FPC
	GTM_DTMT2_1			CDTM2_DTM0
	EVADC_G10CH1	AI		Analog input channel 1, group 10
	P33.6	O0		General-purpose output
	GTM_TOUT28	O1		GTM muxed output
	IOM_MON0_6			Monitor input 0
	IOM_GTM_6			GTM-provided inputs to EXOR combiner
	ASCLIN2_ASLSO	O2		Slave select signal output
	QSPI2_SLSO11	O3		Master slave select output
	—	O4		Reserved
	EVADC_EMUX10	O5		Control of external analog multiplexer interface 1
	EVADC_FC1BFLOUT	O6		Boundary flag output, FC channel 1
	PSI5S_TX	O7		TX data output

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-32 端口 P33 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
77	P33.7	I	SLOW / PU1 / VEVR SB / ES5	General-purpose input
	GTM_TIM1_IN3_9			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_9			Mux input channel 3 of TIM module 0
	CAN00_RXDE			CAN receive input node 0
	GPT120_T2INB			Trigger/gate input of timer T2
	CCU61_CCPOS0C			Hall capture input 0
	SCU_E_REQ4_0			ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	SENT_SENT14C			Receive input channel 14
	IOM_PIN_7			GPIO pad input to FPC
	EVADC_G10CH0	AI		Analog input channel 0, group 10
	P33.7	O0		General-purpose output
	GTM_TOUT29	O1		GTM muxed output
	IOM_MON0_7			Monitor input 0
	IOM_GTM_7			GTM-provided inputs to EXOR combiner
	ASCLIN2_ASCLK	O2		Shift clock output
	QSPI4_SLSO7	O3		Master slave select output
	ASCLIN8_ATX	O4		Transmit output
	—	O5		Reserved
	EVADC_FC3BFLOUT	O6		Boundary flag output, FC channel 3
	—	O7		Reserved

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-32 端口 P33 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
78	P33.8	I	FAST / HighZ / VEVRSB	General-purpose input
	GTM_TIM1_IN4_7			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_7			Mux input channel 4 of TIM module 0
	ASCLIN2_ARXE			Receive input
	SCU_EMGSTOP_POR T_A			Emergency stop Port Pin A input request
	IOM_PIN_8			GPIO pad input to FPC
	P33.8	O0		General-purpose output
	GTM_TOUT30	O1		GTM muxed output
	IOM_MON0_8			Monitor input 0
	ASCLIN2_ATX			Transmit output
	IOM_MON2_14	O2		Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI4_SLSO2			Master slave select output
	—	O4		Reserved
	CAN00_TXD	O5		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	—	O6		Reserved
	CCU61_COUT62	O7		T12 PWM channel 62
	IOM_MON1_13			Monitor input 1
	IOM_REF1_8			Reference input 1
	SMU_FSP0	O		FSP[1..0] Output Signals - Generated by SMU_core

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-32 端口 P33 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
79	P33.9	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN1_9			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_9			Mux input channel 1 of TIM module 0
	IOM_PIN_9			GPIO pad input to FPC
	P33.9	O0		General-purpose output
	GTM_TOUT31	O1		GTM muxed output
	IOM_MON0_9			Monitor input 0
	ASCLIN2_ATX			Transmit output
	IOM_MON2_14	O2		Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI4_SLSO1			Master slave select output
	ASCLIN2_ASCLK	O3		Shift clock output
	CAN01_TXD	O5		CAN transmit output node 1
	IOM_MON2_6			Monitor input 2
	IOM_REF2_6			Reference input 2
	ASCLIN0_ATX	O6		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	CCU61_CC62	O7		T12 PWM channel 62
	IOM_MON1_10			Monitor input 1
	IOM_REF1_11			Reference input 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-32 端口 P33 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
80	P33.10	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM4_IN4_14			Mux input channel 4 of TIM module 4
	GTM_TIM1_IN0_9			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_9			Mux input channel 0 of TIM module 0
	QSPI4_SLSIA			Slave select input
	CAN01_RXDD			CAN receive input node 1
	ASCLIN0_ARXD			Receive input
	IOM_PIN_10			GPIO pad input to FPC
	P33.10			O0
	GTM_TOUT32	O1		GTM muxed output
	IOM_MON0_10			Monitor input 0
	QSPI1_SLSO6	O2		Master slave select output
	QSPI4_SLSO0	O3		Master slave select output
	ASCLIN1_ASLSO	O4		Slave select signal output
	PSI5S_CLK	O5		PSI5S CLK is a clock that can be used on a pin to drive the external PHY.
	—	O6		Reserved
	CCU61_COUT61	O7		T12 PWM channel 61
	IOM_MON1_12			Monitor input 1
	IOM_REF1_9			Reference input 1
	SMU_FSP1	O		FSP[1..0] Output Signals - Generated by SMU_core
81	P33.11	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN2_8			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_8			Mux input channel 2 of TIM module 0
	QSPI4_SCLKA			Slave SPI clock inputs
	IOM_PIN_11			GPIO pad input to FPC
	P33.11	O0		General-purpose output
	GTM_TOUT33	O1		GTM muxed output
	IOM_MON0_11			Monitor input 0
	ASCLIN1_ASCLK	O2		Shift clock output
	QSPI4_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	EDSADC_CGPWMN	O6		Negative carrier generator output
	CCU61_CC61	O7		T12 PWM channel 61
	IOM_MON1_9			Monitor input 1
	IOM_REF1_12			Reference input 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-32 端口 P33 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
82	P33.12	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM3_IN0_6			Mux input channel 0 of TIM module 3
	GTM_TIM2_IN0_6			Mux input channel 0 of TIM module 2
	QSPI4_MTSRA			Slave SPI data input
	CAN00_RXDD			CAN receive input node 0
	PMS_PINBWKP			PINB (P33.12) pin input
	IOM_PIN_12			GPIO pad input to FPC
	P33.12	O0		General-purpose output
	GTM_TOUT34	O1		GTM muxed output
	IOM_MON0_12			Monitor input 0
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI4_MTSR	O3		Master SPI data output
	ASCLIN1_ASCLK	O4		Shift clock output
	—	O5		Reserved
	EDSADC_CGPWMP	O6		Positive carrier generator output
	CCU61_COUT60	O7		T12 PWM channel 60
	IOM_MON1_11			Monitor input 1
	IOM_REF1_10			Reference input 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-32 端口 P33 的功能 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
83	P33.13	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM3_IN1_5			Mux input channel 1 of TIM module 3
	GTM_TIM2_IN1_5			Mux input channel 1 of TIM module 2
	ASCLIN1_ARXF			Receive input
	EDSADC_SGNB			Carrier sign signal input
	QSPI4_MRSTA			Master SPI data input
	MSC1_INJ1			Injection signal from port
	P33.13	O0		General-purpose output
	GTM_TOUT35	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI4_MRST	O3		Slave SPI data output
	IOM_MON2_4			Monitor input 2
	IOM_REF2_4			Reference input 2
	QSPI2_SLSO6	O4		Master slave select output
	CAN00_TXD	O5		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	—	O6		Reserved
	CCU61_CC60	O7		T12 PWM channel 60
	IOM_MON1_8			Monitor input 1
	IOM_REF1_13			Reference input 1

表 2-33 模拟输入

Pin	Symbol	Ctrl.	Buffer Type	Function
67	AN0	I	D / HighZ / VDDM	Analog Input 0
	EVADC_G0CH0			Analog input channel 0, group 0
	EDSADC_EDS3PA			Positive analog input channel 3, pin A
66	AN1	I	D / HighZ / VDDM	Analog Input 1
	EVADC_G0CH1			Analog input channel 1, group 0
	EDSADC_EDS3NA			Negative analog input channel 3, pin A
65	AN2	I	D / HighZ / VDDM	Analog Input 2
	EVADC_G0CH2			Analog input channel 2, group 0
	EDSADC_EDS0PA			Positive analog input channel 0, pin A

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-33 模拟输入 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
64	AN3	I	D / HighZ / VDDM	Analog Input 3
	EVADC_G0CH3			Analog input channel 3, group 0
	EDSADC_EDS0NA			Negative analog input channel 0, pin A
63	AN4	I	D / HighZ / VDDM	Analog Input 4
	EVADC_G11CH0			Analog input channel 0, group 11
	EVADC_G0CH4			Analog input channel 4, group 0
62	AN5	I	D / HighZ / VDDM	Analog Input 5
	EVADC_G11CH1			Analog input channel 1, group 11
	EVADC_G0CH5			Analog input channel 5, group 0
61	AN6	I	D / HighZ / VDDM	Analog Input 6
	EVADC_G11CH2			Analog input channel 2, group 11
	EVADC_G0CH6			Analog input channel 6, group 0
60	AN7	I	D / HighZ / VDDM	Analog Input 7
	EVADC_G11CH3			Analog input channel 3, group 11
	EVADC_G0CH7			Analog input channel 7, group 0
59	AN8	I	D / HighZ / VDDM	Analog Input 8
	EVADC_G11CH4			Analog input channel 4, group 11
	EVADC_G1CH0			Analog input channel 0, group 1
58	AN10	I	D / HighZ / VDDM	Analog Input 10
	EVADC_G11CH6			Analog input channel 6, group 11
	EVADC_G1CH2			Analog input channel 2, group 1
57	AN11	I	D / HighZ / VDDM	Analog Input 11
	EVADC_G11CH7			Analog input channel 7, group 11
	EVADC_G1CH3			Analog input channel 3, group 1
56	AN12	I	D / HighZ / VDDM	Analog Input 12
	EVADC_G1CH4			Analog input channel 4, group 1
	EDSADC_EDS0PB			Positive analog input channel 0, pin B
55	AN13	I	D / HighZ / VDDM	Analog Input 13
	EVADC_G1CH5			Analog input channel 5, group 1
	EDSADC_EDS0NB			Negative analog input channel 0, pin B
50	AN16	I	D / HighZ / VDDM	Analog Input 16
	EVADC_G2CH0			Analog input channel 0, group 2
	EVADC_FC0CH0			Analog input FC channel 0
49	AN17/P40.10	I	S / HighZ / VDDM	Analog Input 17
	SENT_SENT10A			Receive input channel 10
	EVADC_G2CH1			Analog input channel 1, group 2
	EVADC_FC1CH0			Analog input FC channel 1

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-33 模拟输入 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
48	AN18/P40.11	I	S / HighZ / VDDM	Analog Input 18
	SENT_SENT11A			Receive input channel 11
	EVADC_G11CH8			Analog input channel 8, group 11
	EVADC_G2CH2			Analog input channel 2, group 2
47	AN19/P40.12	I	S / HighZ / VDDM	Analog Input 19
	SENT_SENT12A			Receive input channel 12
	EVADC_G11CH9			Analog input channel 9, group 11
	EVADC_G2CH3			Analog input channel 3, group 2
46	AN20	I	D / HighZ / VDDM	Analog Input 20
	EVADC_G2CH4			Analog input channel 4, group 2
	EDSADC_EDS2PA			Positive analog input channel 2, pin A
45	AN21	I	D / HighZ / VDDM	Analog Input 21
	EVADC_G2CH5			Analog input channel 5, group 2
	EDSADC_EDS2NA			Negative analog input channel 2, pin A
44	AN24/P40.0	I	S / HighZ / VDDM	Analog Input 24
	SENT_SENT0A			Receive input channel 0
	EVADC_G3CH0			Analog input channel 0, group 3
	CCU60_CCPOS0D			Hall capture input 0
	EDSADC_EDS2PB			Positive analog input channel 2, pin B
43	AN25/P40.1	I	S / HighZ / VDDM	Analog Input 25
	SENT_SENT1A			Receive input channel 1
	EVADC_G3CH1			Analog input channel 1, group 3
	CCU60_CCPOS1B			Hall capture input 1
	EDSADC_EDS2NB			Negative analog input channel 2, pin B
42	AN26/P40.2	I	S / HighZ / VDDM	Analog Input 26
	SENT_SENT2A			Receive input channel 2
	EVADC_G3CH2			Analog input channel 2, group 3
	CCU60_CCPOS1D			Hall capture input 1
	EVADC_G11CH10			Analog input channel 10, group 11
41	AN27/P40.3	I	S / HighZ / VDDM	Analog Input 27
	SENT_SENT3A			Receive input channel 3
	EVADC_G3CH3			Analog input channel 3, group 3
	CCU60_CCPOS2B			Hall capture input 2
	EVADC_G11CH11			Analog input channel 11, group 11
40	AN28/P40.13	I	S / HighZ / VDDM	Analog Input 28
	SENT_SENT13A			Receive input channel 13
	EVADC_G3CH4			Analog input channel 4, group 3

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-33 模拟输入 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
39	AN29/P40.14	I	S / HighZ / VDDM	Analog Input 29
	SENT_SENT14A			Receive input channel 14
	EVADC_G3CH5			Analog input channel 5, group 3
38	AN32/P40.4	I	S / HighZ / VDDM	Analog Input 32
	SENT_SENT4A			Receive input channel 4
	EVADC_G8CH0			Analog input channel 0, group 8
	CCU60_CCPOS2D			Hall capture input 2
	EVADC_G11CH12			Analog input channel 12, group 11
37	AN33/P40.5	I	S / HighZ / VDDM	Analog Input 33
	SENT_SENT5A			Receive input channel 5
	EVADC_G8CH1			Analog input channel 1, group 8
	CCU61_CCPOS0D			Hall capture input 0
	EVADC_G11CH13			Analog input channel 13, group 11
36	AN35	I	D / HighZ / VDDM	Analog Input 35
	EVADC_G8CH3			Analog input channel 3, group 8
	EVADC_G11CH15			Analog input channel 15, group 11
35	AN36/P40.6	I	S / HighZ / VDDM	Analog Input 36
	SENT_SENT6A			Receive input channel 6
	EVADC_G8CH4			Analog input channel 4, group 8
	CCU61_CCPOS1B			Hall capture input 1
	EDSADC_EDS1PA			Positive analog input channel 1, pin A
34	AN37/P40.7	I	S / HighZ / VDDM	Analog Input 37
	SENT_SENT7A			Receive input channel 7
	EVADC_G8CH5			Analog input channel 5, group 8
	CCU61_CCPOS1D			Hall capture input 1
	EDSADC_EDS1NA			Negative analog input channel 1, pin A
33	AN38/P40.8	I	S / HighZ / VDDM	Analog Input 38
	SENT_SENT8A			Receive input channel 8
	EVADC_G8CH6			Analog input channel 6, group 8
	CCU61_CCPOS2B			Hall capture input 2
	EDSADC_EDS1PB			Positive analog input channel 1, pin B
32	AN39/P40.9	I	S / HighZ / VDDM	Analog Input 39
	SENT_SENT9A			Receive input channel 9
	EVADC_G8CH7			Analog input channel 7, group 8
	CCU61_CCPOS2D			Hall capture input 2
	EDSADC_EDS1NB			Negative analog input channel 1, pin B

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-33 模拟输入 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
31	AN44	I	D / HighZ / VDDM	Analog Input 44
	EVADC_G8CH12			Analog input channel 12, group 8
	EDSADC_EDS1PC			Positive analog input channel 1, pin C
30	AN45	I	D / HighZ / VDDM	Analog Input 45
	EVADC_G8CH13			Analog input channel 13, group 8
	EDSADC_EDS1NC			Negative analog input channel 1, pin C
29	AN46	I	D / HighZ / VDDM	Analog Input 46
	EVADC_G8CH14			Analog input channel 14, group 8
	EDSADC_EDS1PD			Positive analog input channel 1, pin D
28	AN47	I	D / HighZ / VDDM	Analog Input 47
	EVADC_G8CH15			Analog input channel 15, group 8
	EDSADC_EDS1ND			Negative analog input channel 1, pin D

注释：端口引脚P32.0 和P32.1 是双向引脚，具有以下两个功能：

- 如果将这些引脚用作标准GPIO，则可以使用P32.0 和P32.1 引脚配置表中定义的功能。
- 如果引脚用作外部MOSFET 的预驱动器（内部DCDC 情况），P32.0 和P32.1 将充当名为VGATE1N 和VGATE1P 的模拟IO。

表 2-34 系统 I/O

Pin	Symbol	Ctrl.	Buffer Type	Function
84	VGATE1N	O	—	DCDC N ch. MOSFET gate driver output P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
85	VGATE1P	O	—	DCDC P ch. MOSFET gate driver output P32.1 / External Pass Device gate control for EVRC
102	XTAL1	I	XTAL / VEXT	XTAL pad1 XTAL1. Main Oscillator/PLL/Clock Generator Input.
103	XTAL2	O	XTAL / VEXT	XTAL pad2 XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT
112	TMS	I	FAST / PD2 / VEXT	JTAG Module State Machine Control Input TMS: JTAG Module State Machine Control Input. DAP: DAP1 Data I/O.
	DAP1	I/O		DAP: DAP1 Data I/O
114	TRST	I	FAST / PU2 / VEXT	JTAG Module Reset/Enable Input TRST_N: JTAG Module Reset/Enable Input. DAPE: DAPE0 Clock Input

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-34 系统 I/O (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
115	TCK	I	FAST / PD2 / VEXT	JTAG Module Clock Input TCK: JTAG Module Clock Input. DAP: DAP0 Clock Input.
	DAP0	I		DAP: DAP0 Clock Input
120	ESR1	I	FAST / PU1 / VEXT	ESR1 Port Pin input - can be used to trigger a reset or an NMI ESR1: External System Request Reset 1. Default NMI function. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter 'Reset Control Unit' and SCU_IOCRR register description. PMS_EVRWUP: EVR Wakeup Pin
	PMS_ESR1WKP	I		ESR1 pin input
121	PORST	I/O	PORST / PD / VEXT	PORST pin Power On Reset Input. Additional strong PD in case of power fail.
122	ESR0	I	FAST / OD / VEXT	ESR0 Port Pin input - can be used to trigger a reset or an NMI ESR0: External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter 'Reset Control Unit' and SCU_IOCRR register description. PMS_EVRWUP: EVR Wakeup Pin
	PMS_ESR0WKP	I		ESR0 pin input

表 2-35 电源

Pin	Symbol	Ctrl.	Buffer Type	Function
164	VFLEX	I	—	Digital Power Supply for Flex Port Pads (5V / 3.3V)
54	VDDM	I	—	ADC Analog Power Supply (5V / 3.3V)
154	VDDP3	I	—	Flash Power Supply (3.3V)
52	VAREF1	I	—	Positive Analog Reference Voltage 1
26	VAREF2	I	—	Positive Analog Reference Voltage 2
69	VEVRSB	I	—	Standby Power Supply (5V / 3.3V) for the Standby SRAM
155	VDD	I	—	Digital Core Power Supply (1.25V)
10	VDD	I	—	Digital Core Power Supply (1.25V)
24	VDD	I	—	Digital Core Power Supply (1.25V)
68	VDD	I	—	Digital Core Power Supply (1.25V)
100	VDD	I	—	Digital Core Power Supply (1.25V)
123	VDD	I	—	Digital Core Power Supply (1.25V)

TC37x 引脚定义和功能 TC37x T的LQFP-176 封装引脚

表 2-35 电源 (续)

Pin	Symbol	Ctrl.	Buffer Type	Function
153	VEXT	I	—	External Power Supply (5V / 3.3V)
25	VEXT	I	—	External Power Supply (5V / 3.3V)
99	VEXT	I	—	External Power Supply (5V / 3.3V)
E-PAD	VSS	I	—	Digital Ground (Exposed PAD), VSS
53	VSSM	I	—	Analog Ground for VDDM
51	VAGND1	I	—	Negative Analog Reference Voltage 1
27	VAGND2	I	—	Negative Analog Reference Voltage 2
104	VEXT	I	—	Digital Power Supply for Oscillator (shall be supplied with same level as used for VEXT), VEXT(OSC)
101	VSS	I	—	Oscillator Ground, VSS(OSC)

TC 37x 引脚定义及功能：焊盘框中焊盘排列顺序

2.3 焊盘框中焊盘排列顺序

表2-36 焊盘清单

Number	Pad Name	Pad Type	X	Y	Comment
1	P15.0	FAST / PU1 / VEXT / ES	277299	185148	General-purpose I/O
2	P15.1	FAST / PU1 / VEXT / ES	378099	185148	General-purpose I/O
3	P15.2	FAST / PU1 / VEXT / ES	478899	185148	General-purpose I/O
4	P15.3	FAST / PU1 / VEXT / ES	529299	362646	General-purpose I/O
5	P15.4	FAST / PU1 / VEXT / ES	579699	185148	General-purpose I/O
6	P15.5	FAST / PU1 / VEXT / ES	630099	362646	General-purpose I/O
7	P15.6	FAST / PU1 / VEXT / ES	680499	185148	General-purpose I/O
8	P15.7	FAST / PU1 / VEXT / ES	729999	362646	General-purpose I/O
9	P15.8	FAST / PU1 / VEXT / ES	779499	185148	General-purpose I/O
10	P14.0	FAST / PU1 / VEXT / ES2	828999	362646	General-purpose I/O
11	VDD	Vx	899199	185148	Supply Voltage
12	P14.1	FAST / PU1 / VEXT / ES2	961497	362646	General-purpose I/O
13	VSS	Vx	1027197	185148	Supply Voltage
14	P14.2	SLOW / PU2 / VEXT / ES	1096695	362646	General-purpose I/O
15	VSS	Vx	1150893	185148	Supply Voltage
16	P14.3	SLOW / PU2 / VEXT / ES	1199691	362646	General-purpose I/O
17	VEXT	Vx	1254069	179145	Supply Voltage
18	P14.4	SLOW / PU2 / VEXT / ES	1306467	362646	General-purpose I/O
19	P14.5	FAST / PU2 / VEXT / ES	1355967	185148	General-purpose I/O
20	P14.6	FAST / PU1 / VEXT / ES	1405467	362646	General-purpose I/O
21	P14.7	SLOW / PU1 / VEXT / ES	1454967	185148	General-purpose I/O
22	P14.8	SLOW / PU1 / VEXT / ES	1504467	362646	General-purpose I/O

TC 37x 引脚定义及功能：焊盘框中焊盘排列顺序

表2-36 焊盘清单 (续)

Number	Pad Name	Pad Type	X	Y	Comment
23	VSS	—	1558467	185148	Supply Voltage
24	P14.9	LVDS_RX / FAST / PU1 / VEXT / ES	1633518	362646	General-purpose I/O
25	P14.10	LVDS_RX / FAST / PU1 / VEXT / ES	1736514	362646	General-purpose I/O
26	VSS	Vx	1807065	185148	Supply Voltage
27	VDD	Vx	1861065	362646	Supply Voltage
28	RESERVED	Vx	1918863	185148	OTPMust be bonded to VSS
29	VEXT	Vx	1968363	362646	Supply Voltage
30	VEXT	Vx	2017863	185148	Supply Voltage
31	VDD_EXT_IO	Vx	2067363	362646	Supply Voltage
32	VDDP3	Vx	2251863	362646	Supply Voltage
33	VDDP3	Vx	2331063	185148	Supply Voltage
34	VDDP3	Vx	2409561	362646	Supply Voltage
35	VSS	—	2472561	185148	Supply Voltage
36	VDD	Vx	2535867	362646	Supply Voltage
37	VDD	Vx	2599065	185148	Supply Voltage
38	VDD	Vx	2662263	362646	Supply Voltage
39	P13.0	LVDS_TX / FAST / PU1 / VEXT / ES6	2769066	185148	General-purpose I/O
40	P13.1	LVDS_TX / FAST / PU1 / VEXT / ES6	2872062	185148	General-purpose I/O
41	VSS	Vx	2979063	185148	Supply Voltage
42	P13.2	LVDS_TX / FAST / PU1 / VEXT / ES6	3086964	185148	General-purpose I/O
43	P13.3	LVDS_TX / FAST / PU1 / VEXT / ES6	3189960	185148	General-purpose I/O
44	VDDP3	Vx	3296961	362646	Supply Voltage
45	VEXT	Vx	3346461	179145	Supply Voltage
46	VDD	Vx	3401559	362646	Supply Voltage
47	VSS	Vx	3451059	185148	Supply Voltage
48	P12.0	SLOW / PU1 / VFLEX / ES	3525975	356643	General-purpose I/O
49	P12.1	SLOW / PU1 / VFLEX / ES	3575475	179145	General-purpose I/O

TC 37x 引脚定义及功能：焊盘框中焊盘排列顺序

表2-36 焊盘清单 (续)

Number	Pad Name	Pad Type	X	Y	Comment
50	P11.0	RFAST / PU1 / VFLEX / ES	3681981	356643	General-purpose I/O
51	VFLEX	Vx	3728979	179145	Supply Voltage
52	P11.1	RFAST / PU1 / VFLEX / ES	3802491	356643	General-purpose I/O
53	VSS	Vx	3851181	185148	Supply Voltage
54	P11.2	RFAST / PU1 / VFLEX / ES	3926385	362646	General-purpose I/O
55	VDD	Vx	3973383	179145	Supply Voltage
56	P11.4	RFAST / PU1 / VFLEX / ES	4089087	362646	General-purpose I/O
57	VSS	Vx	4176585	185148	Supply Voltage
58	P11.3	RFAST / PU1 / VFLEX / ES	4251789	362646	General-purpose I/O
59	VFLEX	Vx	4298787	179145	Supply Voltage
60	P11.6	RFAST / PU1 / VFLEX / ES	4372299	362646	General-purpose I/O
61	VSS	Vx	4420989	185148	Supply Voltage
62	P11.5	SLOW / RGMII_Input / PU1 / VFLEX / ES	4469679	356643	General-purpose I/O
63	P11.7	SLOW / RGMII_Input / PU1 / VFLEX / ES	4520475	179145	General-purpose I/O
64	P11.9	FAST / RGMII_Input / PU1 / VFLEX / ES	4571271	362646	General-purpose I/O
65	VFLEX	Vx	4621671	185148	Supply Voltage
66	P11.8	SLOW / RGMII_Input / PU1 / VFLEX / ES	4670541	356643	General-purpose I/O
67	P11.10	FAST / RGMII_Input / PU1 / VFLEX / ES	4720959	185148	General-purpose I/O
68	P11.11	FAST / RGMII_Input / PU1 / VFLEX / ES	4771557	362646	General-purpose I/O

TC 37x 引脚定义及功能：焊盘框中焊盘排列顺序

表2-36 焊盘清单 (续)

Number	Pad Name	Pad Type	X	Y	Comment
69	VSS	Vx	4822155	185148	Supply Voltage
70	P11.12	FAST / RGMII_Input / PU1 / VFLEX / ES	4870845	362646	General-purpose I/O
71	VSS	Vx	4944051	185148	Supply Voltage
72	VDD	Vx	5028849	356643	Supply Voltage
73	P11.14	SLOW / PU1 / VFLEX / ES	5098347	179145	General-purpose I/O
74	P11.13	SLOW / PU1 / VFLEX / ES	5149827	356643	General-purpose I/O
75	P11.15	SLOW / PU1 / VFLEX / ES	5196825	179145	General-purpose I/O
76	P10.0	SLOW / PU1 / VEXT / ES	5271723	362646	General-purpose I/O
77	P10.1	FAST / PU1 / VEXT / ES	5321223	185148	General-purpose I/O
78	P10.2	FAST / PU1 / VEXT / ES	5370723	362646	General-purpose I/O
79	P10.3	FAST / PU1 / VEXT / ES	5420223	185148	General-purpose I/O
80	P10.4	FAST / PU1 / VEXT / ES	5470218	362646	General-purpose I/O
81	P10.5	SLOW / PU2 / VEXT / ES	5521588	185148	General-purpose I/O
82	P10.6	SLOW / PU2 / VEXT / ES	5571583	362646	General-purpose I/O
83	P10.7	SLOW / PU1 / VEXT / ES	5658813	185148	General-purpose I/O
84	P10.8	SLOW / PU1 / VEXT / ES	5763663	185148	General-purpose I/O
85	VSS	Vx	5837292	286299	Supply Voltage
86	VEXT	Vx	5837292	387099	Supply Voltage
87	VDD	Vx	5659794	487899	Supply Voltage
88	P02.0	FAST / PU1 / VEXT / ES	5837292	540999	General-purpose I/O
89	P02.1	SLOW / PU1 / VEXT / ES	5659794	591399	General-purpose I/O
90	P02.2	FAST / PU1 / VEXT / ES	5837292	641799	General-purpose I/O
91	P02.3	SLOW / PU1 / VEXT / ES	5659794	696699	General-purpose I/O

TC 37x引脚定义及功能：焊盘框中焊盘排列顺序

表2-36 焊盘清单 (续)

Number	Pad Name	Pad Type	X	Y	Comment
92	P02.4	FAST / PU1 / VEXT / ES	5837292	746199	General-purpose I/O
93	P02.5	FAST / PU1 / VEXT / ES	5659794	805599	General-purpose I/O
94	P02.6	FAST / PU1 / VEXT / ES	5837292	855999	General-purpose I/O
95	P02.7	FAST / PU1 / VEXT / ES	5659794	906399	General-purpose I/O
96	P02.8	SLOW / PU1 / VEXT / ES	5837292	956799	General-purpose I/O
97	VDD	Vx	5659794	1025199	Supply Voltage
98	VDD	Vx	5837292	1116999	Supply Voltage
99	VDD	Vx	5659794	1206999	Supply Voltage
100	VSS	—	5837292	1296999	Supply Voltage
101	VSS	Vx	5837292	1404999	Supply Voltage
102	P02.9	SLOW / PU1 / VEXT / ES	5665797	1481499	General-purpose I/O
103	P02.10	SLOW / PU1 / VEXT / ES	5843295	1529199	General-purpose I/O
104	P02.11	SLOW / PU1 / VEXT / ES	5665797	1576197	General-purpose I/O
105	VSS	—	5837292	1650195	Supply Voltage
106	P01.3	SLOW / PU1 / VEXT / ES	5665797	1717695	General-purpose I/O
107	VEXT	Vx	5837292	1776195	Supply Voltage
108	VDD	Vx	5659794	1849095	Supply Voltage
109	VSS	Vx	5837292	1912095	Supply Voltage
110	P01.4	SLOW / PU1 / VEXT / ES	5665797	1961595	General-purpose I/O
111	VSS	Vx	5837292	2038095	Supply Voltage
112	P01.5	SLOW / PU1 / VEXT / ES	5837292	2137095	General-purpose I/O
113	P01.6	FAST / PU1 / VEXT / ES	5665797	2185893	General-purpose I/O
114	P01.7	FAST / PU1 / VEXT / ES	5843295	2238291	General-purpose I/O
115	P00.0	FAST / PU1 / VEXT / ES	5659794	2285289	General-purpose I/O
116	VSS_EXT_IO	—	5837292	2335095	Supply Voltage
117	VDD_EXT_IO	—	5659794	2425095	Supply Voltage
118	VSS	Vx	5837292	2520495	Supply Voltage

TC 37x 引脚定义及功能：焊盘框中焊盘排列顺序

表2-36 焊盘清单 (续)

Number	Pad Name	Pad Type	X	Y	Comment
119	VSS	Vx	5837292	2619495	Supply Voltage
120	VDD	Vx	5659794	2718495	Supply Voltage
121	VDD	Vx	5837292	2814093	Supply Voltage
122	VDD	Vx	5659794	2911491	Supply Voltage
123	P00.1	SLOW / PU1 / VEXT / ES	5837292	3030430	General-purpose I/O
124	P00.2	SLOW / PU1 / VEXT / ES1	5659794	3085430	General-purpose I/O
125	P00.3	SLOW / PU1 / VEXT / ES1	5837292	3140428	General-purpose I/O
126	P00.4	SLOW / PU1 / VEXT / ES1	5659794	3195428	General-purpose I/O
127	P00.5	SLOW / PU1 / VEXT / ES1	5837292	3250426	General-purpose I/O
128	P00.6	SLOW / PU1 / VEXT / ES1	5659794	3305426	General-purpose I/O
129	P00.7	SLOW / PU1 / VEXT / ES1	5837292	3360424	General-purpose I/O
130	P00.8	SLOW / PU1 / VEXT / ES1	5659794	3415424	General-purpose I/O
131	P00.9	SLOW / PU1 / VEXT / ES1	5837292	3470422	General-purpose I/O
132	P00.10	SLOW / PU1 / VEXT / ES1	5659794	3525422	General-purpose I/O
133	P00.11	SLOW / PU1 / VEXT / ES1	5837292	3580420	General-purpose I/O
134	P00.12	SLOW / PU1 / VEXT / ES1	5659794	3635420	General-purpose I/O
135	VSS	Vx	5837292	3690418	Supply Voltage
136	VSS	Vx	5837292	3789518	Supply Voltage
137	VDD	Vx	5837292	3888616	Supply Voltage
138	VDD	Vx	5837292	3987716	Supply Voltage
139	VEXT	Vx	5837292	4086814	Supply Voltage
140	VAREF3	Vx	5837292	4225730	Supply Voltage
141	VAGND3	Vx	5837292	4324828	Supply Voltage
142	VAREF2	Vx	5659794	4379828	Supply Voltage
143	VAGND2	Vx	5837292	4434826	Supply Voltage
144	AN47	D / HighZ / VDDM	5837292	4533926	Analog Input 47
145	AN46	D / HighZ / VDDM	5659794	4588924	Analog Input 46

TC 37x引脚定义及功能：焊盘框中焊盘排列顺序

表2-36 焊盘清单 (续)

Number	Pad Name	Pad Type	X	Y	Comment
146	AN45	D / HighZ / VDDM	5837292	4643924	Analog Input 45
147	AN44	D / HighZ / VDDM	5659794	4698922	Analog Input 44
148	AN43	D / HighZ / VDDM	5837292	4753922	Analog Input 43
149	AN42	D / HighZ / VDDM	5659794	4808920	Analog Input 42
150	AN41	D / HighZ / VDDM	5837292	4863920	Analog Input 41
151	AN40	D / HighZ / VDDM	5659794	4918918	Analog Input 40
152	AN39/P40.9	S / HighZ / VDDM	5837292	5083916	Analog Input 39
153	AN38/P40.8	S / HighZ / VDDM	5659794	5138914	Analog Input 38
154	AN37/P40.7	S / HighZ / VDDM	5837292	5193914	Analog Input 37
155	AN36/P40.6	S / HighZ / VDDM	5659794	5248912	Analog Input 36
156	AN35	D / HighZ / VDDM	5837292	5303912	Analog Input 35
157	AN34	D / HighZ / VDDM	5659794	5358910	Analog Input 34
158	AN33/P40.5	S / HighZ / VDDM	5837292	5413910	Analog Input 33
159	AN32/P40.4	S / HighZ / VDDM	5659794	5468908	Analog Input 32
160	AN31	D / HighZ / VDDM	5837292	5523908	Analog Input 31
161	AN30	D / HighZ / VDDM	5659794	5578906	Analog Input 30
162	AN29/P40.14	S / HighZ / VDDM	5837292	5633906	Analog Input 29
163	AN28/P40.13	S / HighZ / VDDM	5659794	5688904	Analog Input 28
164	AN27/P40.3	S / HighZ / VDDM	5837292	5743904	Analog Input 27
165	AN26/P40.2	S / HighZ / VDDM	5659794	5798902	Analog Input 26
166	AN25/P40.1	S / HighZ / VDDM	5837292	5853902	Analog Input 25

TC 37x 引脚定义及功能：焊盘框中焊盘排列顺序

表2-36 焊盘清单 (续)

Number	Pad Name	Pad Type	X	Y	Comment
167	AN24/P40.0	S / HighZ / VDDM	5837292	5977300	Analog Input 24
168	AN23	D / HighZ / VDDM	5752440	6062292	Analog Input 23
169	AN22	D / HighZ / VDDM	5629140	6062292	Analog Input 22
170	AN21	D / HighZ / VDDM	5574141	5884794	Analog Input 21
171	AN20	D / HighZ / VDDM	5519142	6062292	Analog Input 20
172	AN19/P40.12	S / HighZ / VDDM	5464143	5884794	Analog Input 19
173	AN18/P40.11	S / HighZ / VDDM	5409144	6062292	Analog Input 18
174	AN17/P40.10	S / HighZ / VDDM	5354145	5884794	Analog Input 17
175	AN16	D / HighZ / VDDM	5299146	6062292	Analog Input 16
176	AN15	D / HighZ / VDDM	5244147	5884794	Analog Input 15
177	VAGND1	Vx	5189148	6062292	Supply Voltage
178	VAREF1	Vx	5134149	5884794	Supply Voltage
179	VAGND0	Vx	5079150	6062292	Supply Voltage
180	VAREF0	Vx	5024151	5884794	Supply Voltage
181	VSSM	Vx	4969152	6062292	Supply Voltage
182	VDDM	Vx	4914153	5884794	Supply Voltage
183	VSSM	Vx	4859154	6062292	Supply Voltage
184	VDDM	Vx	4804155	5884794	Supply Voltage
185	VSSM	Vx	4749156	6062292	Supply Voltage
186	VDDM	Vx	4694157	5884794	Supply Voltage
187	AN14	D / HighZ / VDDM	4639158	6062292	Analog Input 14
188	AN13	D / HighZ / VDDM	4584159	5884794	Analog Input 13
189	AN12	D / HighZ / VDDM	4529160	6062292	Analog Input 12
190	AN11	D / HighZ / VDDM	4474161	5884794	Analog Input 11
191	AN10	D / HighZ / VDDM	4419162	6062292	Analog Input 10
192	AN9	D / HighZ / VDDM	4364163	5884794	Analog Input 9

TC 37x 引脚定义及功能：焊盘框中焊盘排列顺序

表2-36 焊盘清单 (续)

Number	Pad Name	Pad Type	X	Y	Comment
193	AN8	D / HighZ / VDDM	4309164	6062292	Analog Input 8
194	AN7	D / HighZ / VDDM	4254165	5884794	Analog Input 7
195	AN6	D / HighZ / VDDM	4199166	6062292	Analog Input 6
196	AN5	D / HighZ / VDDM	4144167	5884794	Analog Input 5
197	AN4	D / HighZ / VDDM	4089168	6062292	Analog Input 4
198	AN3	D / HighZ / VDDM	4034169	5884794	Analog Input 3
199	AN2	D / HighZ / VDDM	3979170	6062292	Analog Input 2
200	AN1	D / HighZ / VDDM	3924171	5884794	Analog Input 1
201	AN0	D / HighZ / VDDM	3869172	6062292	Analog Input 0
202	VSS	Vx	3617253	6062292	Supply Voltage
203	VDD	Vx	3509055	5884794	Supply Voltage
204	VDD	Vx	3429657	6062292	Supply Voltage
205	VDD	Vx	3339459	5884794	Supply Voltage
206	VSS	Vx	3289860	6062292	Supply Voltage
207	VEVRSB	Vx	3206574	5884794	Supply Voltage
208	VEVRSB	Vx	3157074	6062292	Supply Voltage
209	P33.0	SLOW / PU1 / VEVRSB / ES5	3098574	5884794	General-purpose I/O
210	VSS	Vx	3049074	6062292	Supply Voltage
211	VDD	Vx	2986974	5884794	Supply Voltage
212	VSS	Vx	2937375	6062292	Supply Voltage
213	P33.1	SLOW / PU1 / VEVRSB / ES5	2852874	5884794	General-purpose I/O
214	P33.2	SLOW / PU1 / VEVRSB / ES5	2803374	6062292	General-purpose I/O
215	P33.3	SLOW / PU1 / VEVRSB / ES5	2753874	5884794	General-purpose I/O

TC 37x 引脚定义及功能：焊盘框中焊盘排列顺序

表2-36 焊盘清单 (续)

Number	Pad Name	Pad Type	X	Y	Comment
216	P34.1	SLOW / PU1 / VEVR SB / ES5	2704176	6068295	General-purpose I/O
217	P33.4	SLOW / PU1 / VEVR SB / ES5	2654478	5884794	General-purpose I/O
218	P34.2	SLOW / PU1 / VEVR SB / ES	2604978	6068295	General-purpose I/O
219	P33.5	SLOW / PU1 / VEVR SB / ES5	2552976	5884794	General-purpose I/O
220	P34.3	SLOW / PU1 / VEVR SB / ES	2503476	6068295	General-purpose I/O
221	P33.6	SLOW / PU1 / VEVR SB / ES5	2451474	5884794	General-purpose I/O
222	P34.4	SLOW / PU1 / VEVR SB / ES	2399076	6068295	General-purpose I/O
223	VDD	Vx	2352078	5884794	Supply Voltage
224	VSS	Vx	2302479	6062292	Supply Voltage
225	P34.5	FAST / PU1 / VEVR SB / ES	2178378	5890797	General-purpose I/O
226	P33.7	SLOW / PU1 / VEVR SB / ES5	2129580	6062292	General-purpose I/O
227	P33.8	FAST / HighZ / VEVR SB	2080080	5884794	General-purpose I/O
228	P33.9	SLOW / PU1 / VEVR SB / ES5	2030580	6062292	General-purpose I/O
229	VDD	Vx	1981080	5884794	Supply Voltage
230	VSS	Vx	1931481	6062292	Supply Voltage
231	P33.10	FAST / PU1 / VEVR SB / ES5	1796184	6062292	General-purpose I/O
232	P33.14	FAST / PU1 / VEVR SB / ES5	1692684	6068295	General-purpose I/O
233	P33.11	FAST / PU1 / VEVR SB / ES5	1593684	6062292	General-purpose I/O
234	P33.15	SLOW / PU1 / VEVR SB / ES5	1494684	6068295	General-purpose I/O

TC 37x 引脚定义及功能：焊盘框中焊盘排列顺序

表2-36 焊盘清单 (续)

Number	Pad Name	Pad Type	X	Y	Comment
235	P33.12	FAST / PU1 / VEVRSB / ES5	1445184	5884794	General-purpose I/O
236	VSS	Vx	1395684	6062292	Supply Voltage
237	VEVRSB	Vx	1346184	5890797	Supply Voltage
238	P33.13	FAST / PU1 / VEVRSB / ES5	1296684	6062292	General-purpose I/O
239	VSS	Vx	1193670	6062292	Supply Voltage
240	VDD	Vx	1137672	5884794	Supply Voltage
241	VSS	Vx	1085472	6062292	Supply Voltage
242	VEXT	Vx	1025172	5890797	Supply Voltage
243	P32.0	SLOW / PU1 / VEXT / ES	964872	6062292	General-purpose I/O
244	VGATE1N	Vx	915372	5884794	DCDC N ch. MOSFET gate driver output
245	P32.1	SLOW / PU1 / VEXT / ES	861174	6062292	General-purpose I/O
246	VGATE1P	Vx	811674	5884794	DCDC P ch. MOSFET gate driver output
247	P32.2	SLOW / PU1 / VEXT / ES	762174	6062292	General-purpose I/O
248	P32.3	SLOW / PU1 / VEXT / ES	712674	5884794	General-purpose I/O
249	P32.4	FAST / PU1 / VEXT / ES	663174	6062292	General-purpose I/O
250	P32.5	SLOW / PU1 / VEXT / ES	613674	5890797	General-purpose I/O
251	P32.6	SLOW / PU1 / VEXT / ES	562374	6068295	General-purpose I/O
252	P32.7	SLOW / PU1 / VEXT / ES	462375	6068295	General-purpose I/O
253	VSS	Vx	362376	6062292	Supply Voltage
254	VDD	Vx	261576	6062292	Supply Voltage
255	VEXT	Vx	185148	5961141	Supply Voltage
256	VSS	Vx	185148	5854743	Supply Voltage
257	P23.0	SLOW / PU1 / VEXT / ES	185148	5744943	General-purpose I/O
258	P23.1	FAST / PU1 / VEXT / ES	362646	5653143	General-purpose I/O
259	P23.2	SLOW / PU1 / VEXT / ES	185148	5603643	General-purpose I/O

TC 37x引脚定义及功能：焊盘框中焊盘排列顺序

表2-36 焊盘清单 (续)

Number	Pad Name	Pad Type	X	Y	Comment
260	P23.3	SLOW / PU1 / VEXT / ES	362646	5554143	General-purpose I/O
261	P23.4	FAST / PU1 / VEXT / ES	185148	5504643	General-purpose I/O
262	VDD	Vx	356643	5455143	Supply Voltage
263	VSS	Vx	185148	5386743	Supply Voltage
264	P23.5	FAST / PU1 / VEXT / ES	362646	5303043	General-purpose I/O
265	P23.7	SLOW / PU1 / VEXT / ES	179145	5252643	General-purpose I/O
266	P23.6	SLOW / PU1 / VEXT / ES	356643	5205645	General-purpose I/O
267	P22.4	SLOW / PU1 / VEXT / ES	179145	5158647	General-purpose I/O
268	P22.6	SLOW / PU1 / VEXT / ES	356643	5111649	General-purpose I/O
269	P22.7	SLOW / PU1 / VEXT / ES	179145	5064651	General-purpose I/O
270	P22.5	SLOW / PU1 / VEXT / ES	356643	5017653	General-purpose I/O
271	P22.8	SLOW / PU1 / VEXT / ES	179145	4970655	General-purpose I/O
272	P22.9	SLOW / PU1 / VEXT / ES	356643	4923657	General-purpose I/O
273	P22.10	SLOW / PU1 / VEXT / ES	179145	4876659	General-purpose I/O
274	P22.11	SLOW / PU1 / VEXT / ES	356643	4829661	General-purpose I/O
275	VDD	Vx	179145	4782663	Supply Voltage
276	P22.0	LVDS_TX / FAST / PU1 / VEXT / ES6	185148	4675662	General-purpose I/O
277	P22.1	LVDS_TX / FAST / PU1 / VEXT / ES6	185148	4572666	General-purpose I/O
278	VSS	Vx	185148	4461165	Supply Voltage
279	P22.2	LVDS_TX / FAST / PU1 / VEXT / ES6	185148	4351914	General-purpose I/O
280	P22.3	LVDS_TX / FAST / PU1 / VEXT / ES6	185148	4244418	General-purpose I/O
281	VSS	Vx	185148	4139667	Supply Voltage

TC 37x引脚定义及功能：焊盘框中焊盘排列顺序

表2-36 焊盘清单 (续)

Number	Pad Name	Pad Type	X	Y	Comment
282	VEXT	Vx	362646	4081563	Supply Voltage
283	VEXT	Vx	185148	4014063	Supply Voltage
284	VEXT	Vx	362646	3946563	Supply Voltage
285	VDD	Vx	185148	3856563	Supply Voltage
286	VDD	Vx	362646	3770163	Supply Voltage
287	VDD	Vx	362646	3666159	Supply Voltage
288	VSS	—	185148	3616749	Supply Voltage
289	XTAL1	XTAL / VEXT	185148	3459600	XTAL pad1 XTAL1. Main Oscillator/PLL/Clock Generator Input.
290	XTAL2	XTAL / VEXT	185148	3360600	XTAL pad2 XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT
291	VSS	—	185148	3203451	Supply Voltage
292	VEXT	Vx	362646	3154041	Supply Voltage
293	VEXT	Vx	362646	3009663	Supply Voltage
294	VSS	Vx	185148	2960163	Supply Voltage
295	VSS	Vx	185148	2861163	Supply Voltage
296	P21.0	LVDS_RX / FAST / PU1 / VEXT / ES	362646	2788110	General-purpose I/O
297	P21.1	LVDS_RX / FAST / PU1 / VEXT / ES	362646	2685114	General-purpose I/O
298	VDD	Vx	185148	2611863	Supply Voltage
299	P21.2	LVDS_RX / FAST / PU1 / VEXT / ES	362646	2529810	General-purpose I/O
300	P21.3	LVDS_RX / FAST / PU1 / VEXT / ES	362646	2426814	General-purpose I/O
301	VDD	Vx	185148	2347263	Supply Voltage
302	P21.4	LVDS_TX / FAST / PU1 / VEXT / ES6	185148	2237760	General-purpose I/O
303	P21.5	LVDS_TX / FAST / PU1 / VEXT / ES6	185148	2134764	General-purpose I/O

TC 37x 引脚定义及功能：焊盘框中焊盘排列顺序

表2-36 焊盘清单 (续)

Number	Pad Name	Pad Type	X	Y	Comment
304	P21.6/TDI	FAST / PD / PU2 / VEXT / ES3	362646	2027763	General-purpose I/O PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ. DAPE: DAPE1 Data I/O.
305	TMS	FAST / PD2 / VEXT	185148	1977363	JTAG Module State Machine Control Input TMS: JTAG Module State Machine Control Input. DAP: DAP1 Data I/O.
306	P21.7/TDO	FAST / PU2 / VEXT / ES4	362646	1927863	General-purpose I/O DAP: DAP2 Data I/O; DAPE: DAPE2 Data I/O.
307	 TRST	FAST / PU2 / VEXT	185148	1877643	JTAG Module Reset/Enable Input TRST_N: JTAG Module Reset/Enable Input. DAPE: DAPE0 Clock Input
308	TCK	FAST / PD2 / VEXT	362646	1827891	JTAG Module Clock Input TCK: JTAG Module Clock Input. DAP: DAP0 Clock Input.
309	P20.0	FAST / PU1 / VEXT / ES	185148	1777743	General-purpose I/O
310	VEXT	Vx	356643	1723743	Supply Voltage
311	VSS	Vx	185148	1665243	Supply Voltage
312	P20.1	SLOW / PU1 / VEXT / ES	362646	1615743	General-purpose I/O
313	P20.2	S / PU / VEXT	185148	1566243	General-purpose I/O This pin is latched at power on reset release to enter test mode.
314	P20.3	SLOW / PU1 / VEXT / ES	362646	1516743	General-purpose I/O

TC 37x 引脚定义及功能：焊盘框中焊盘排列顺序

表2-36 焊盘清单 (续)

Number	Pad Name	Pad Type	X	Y	Comment
315	ESR1	FAST / PU1 / VEXT	185148	1467243	ESR1 Port Pin input - can be used to trigger a reset or an NMI ESR1: External System Request Reset 1. Default NMI function. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter 'Reset Control Unit' and SCU_IOCRR register description. PMS_EVRWUP: EVR Wakeup Pin
316	PORST	PORST / PD / VEXT	362646	1417743	PORST pin Power On Reset Input. Additional strong PD in case of power fail.
317	ESR0	FAST / OD / VEXT	185148	1368243	ESR0 Port Pin input - can be used to trigger a reset or an NMI ESR0: External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter 'Reset Control Unit' and SCU_IOCRR register description. PMS_EVRWUP: EVR Wakeup Pin
318	VDD	Vx	362646	1280745	Supply Voltage
319	VDD	Vx	185148	1195245	Supply Voltage
320	VDD	Vx	362646	1109745	Supply Voltage
321	VSS	Vx	185148	1060146	Supply Voltage
322	P20.6	SLOW / PU1 / VEXT / ES	362646	966105	General-purpose I/O
323	P20.7	FAST / PU1 / VEXT / ES	185148	916605	General-purpose I/O

TC 37x 引脚定义及功能：焊盘框中焊盘排列顺序

表2-36 焊盘清单（续）

Number	Pad Name	Pad Type	X	Y	Comment
324	P20.8	FAST / PU1 / VEXT / ES	362646	867105	General-purpose I/O
325	P20.9	FAST / PU1 / VEXT / ES	185148	817605	General-purpose I/O
326	P20.10	FAST / PU1 / VEXT / ES	362646	768105	General-purpose I/O
327	P20.11	FAST / PU1 / VEXT / ES	185148	718605	General-purpose I/O
328	P20.12	FAST / PU1 / VEXT / ES	362646	669105	General-purpose I/O
329	P20.13	FAST / PU1 / VEXT / ES	185148	619605	General-purpose I/O
330	P20.14	FAST / PU1 / VEXT / ES	362646	570105	General-purpose I/O
331	VSS	Vx	185148	520110	Supply Voltage
332	VDD	Vx	362646	455805	Supply Voltage
333	VEXT	Vx	179145	382005	Supply Voltage
334	VSS	Vx	185148	281205	Supply Voltage

在第3节“电气规范”的表格中，每当使用术语“相邻焊盘”时，详细定义如图2-36所示。此表述也适用于次邻/最近邻焊盘。

为了找出谁在影响目标焊盘上的操作（干扰），必须定义大量活动的近邻焊盘（ACNP）。

寻找近邻焊盘。

焊盘环有四个边：底部、左侧、顶部、右侧。每条边都是有限的，即有两个端点。

每个焊盘都有两个直接（第一个）邻居，除非它位于边缘的末端。在这种情况下，它只有一个相邻焊盘。类似地，每个焊盘都有两个间接（第二）邻居，除非它或它的第一个邻居位于边缘的末端。我们将这些第一和第二个邻居统称为近邻焊盘。因此每个焊盘都有2到4个近邻焊盘。

可以按照以下顺序寻找近邻：

- 1.) 选择目标焊盘并在表格图2-36中查找其“X”和“Y”坐标。
- 2.) 通过计算与选定焊盘的“X”和“Y”距离来找到第一和第二个邻居。图2-36按“Y”坐标排序，这可能有助于定位4个近邻候选者（如果焊盘靠近边缘，则最终可能有少于4个近邻）。

定义活跃焊盘：

如果焊盘当前正在使用并且名称中没有“Vxx”，则表示焊盘活跃。

确定活跃的邻近焊盘的数量遵循以下规则：

- 如果第一个邻居是活跃的，那么我们对其进行计数，并检查第二个邻居（在选定焊盘的同一侧）是否活跃。
- 如果第一个邻居不活跃，那么我们就不会检查同一侧的第二个邻居。

2.4 图例说明

本第 2 章中 TP 数据与文件 TC37xpd_IO_Spirit_v1.0.0.1.18.xml 匹配。

Ctrl 列:

I = 输入 (对于具有 IOCR 位字段选择 $PCx = 0XXX_B$ 的 GPIO 端口)
O = 输出 (对于 GPIO 端口, “O”在大多数情况下代表端口 HWOUT 功能)
O0 = 带有 IOCR 位字段选择的输出 $PCx = 1X000_B$
O1 = 带有 IOCR 位字段选择的输出 $PCx = 1X001_B$ (ALT1)
O2 = 带 IOCR 位字段选择的输出 $PCx = 1X010_B$ (ALT2)
O3 = 带 IOCR 位字段选择的输出 $PCx = 1X011_B$ (ALT3)
O4 = 带 IOCR 位字段选择的输出 $PCx = 1X100_B$ (ALT4)
O5 = 带 IOCR 位字段选择的输出 $PCx = 1X101_B$ (ALT5)
O6 = 带 IOCR 位字段选择的输出 $PCx = 1X110_B$ (ALT6)
O7 = 带 IOCR 位字段选择的输出 $PCx = 1X111_B$ (ALT7)

“缓冲区类型”列:

RFAST = 焊盘类 RFAST (5V/3.3V)
FAST = 焊盘类 FAST (5V/3.3V)
SLOW = 焊盘类 SLOW (5V/3.3V)
LVDS_TX = 焊盘类 LVDS 发送
LVDS_RX = 焊盘类 LVDS 接收
S = 焊盘类 S (模拟输入与通用输入叠加)
D = 焊盘类 D (模拟输入)
Porst = Porst 输入焊盘
XTAL1 = XTAL1 输入焊盘
XTAL2 = XTAL2 输入焊盘
PU = 复位期间连接上拉器件 ($\overline{PORST} = 0$)
PU1 = 复位期间连接上拉器件 ($\overline{PORST} = 0$)¹⁾
PU2 = 启动和复位期间连接上拉器件, 待机模式下为 HighZ
PD = 复位期间连接下拉器件 ($\overline{PORST} = 0$)
PD1 = 在复位期间连接下拉器件 ($\overline{PORST} = 0$)¹⁾
PD2 = 在启动和复位期间连接下拉电阻, 待机模式下为高阻态
OD = 复位期间开漏 ($\overline{PORST} = 0$)
ES = 支持紧急停止
ES1=ES。ES 可被 VADC 覆盖, 通过 P00_PCSR 控制
ES2=ES。ES 可被 DXCPL (DAP 通过 CAN 物理层) 覆盖, 不可被 DXCM (通过 CAN 消息调试) 覆盖
ES3=ES。如果此引脚用作 TDI 则 ES 可被 JTAG 模式覆盖。
ES4 = ES。ES 可被 JTAG 或三引脚 DAP 模式覆盖。

1) 在PORST 期间和之后, GPIO (Px.y) 的默认状态通过 HWCFG6 (P14.4) 控制。另请参阅 PMS、HWCFG[6] 章节。

TC37x 引脚定义及功能图例

ES5=ES。如果实施的话，ES 可被待机控制器 (SCR) 覆盖。可以通过控制寄存器 P33_PCSR 和 P34_PCSR 禁用重用

ES6=ES。在 LVDS TX 焊盘上，ES 仅在 CMOS 模式下影响焊盘，而不在 LVDS 模式下影响焊盘。因此，仅当 LPCRx.TX_EN 选择 CMOS 模式时，ES 事件中输出才会关闭

3 电气规格参数

3.1 参数解释

本节列出的参数部分代表TC37x 的特性，部分代表其对系统的要求。 为了帮助在评估设计时轻松解释参数，它们在“符号”列中用两个字母的缩写标记：

- **CC**

这些参数表明了**控制器参数**特性，这是TC37x 的一个显著特点，在系统设计中必须加以考虑

- **SR**

这些参数表明了**系统要求**，必须由采用TC37x设计的微控制器系统提供。

电气规格绝对最大额定值

3.2 绝对最大额定值

超过“绝对最大额定值”所列值的载荷可能会对器件造成永久性损坏。这仅仅是一个载荷额定值，并不意味着设备在这些条件下或任何其他高于本规范操作部分所示条件的情况下能够正常运行。暴露于绝对最大额定条件可能会影响器件的可靠性。

表 3-1 最大绝对额定值

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Storage Temperature	T_{ST} SR	-65	-	150	°C	upto 65h @ $T_J = 150^{\circ}\text{C}$
Voltage at V_{DD} power supply pins with respect to V_{SS1} 2)	V_{DD} SR	-	-	1.65	V	upto 2.8h
		-	-	1.45	V	upto 72h
Voltage at V_{DDP3} power supply pins with respect to V_{SS}	V_{DDP3} SR	-	-	4.43	V	
Voltage at V_{DDM} , V_{EXT} , V_{FLEX} and V_{EVRSB} power supply pins with respect to V_{SS}	V_{DDM} SR	-	-	6.75	V	upto 2.8h
		-	-	5.6	V	upto 72h
Voltage on all analog and class S input pins with respect to V_{SS3}	V_{IN} SR	-0.7	-	6.75	V	
Voltage on all other input pins with respect to V_{SS3}	V_{IN} SR	-0.7	-	6.75	V	
Input current on any pin during overload condition 4) 5)	I_{IN} SR	-10	-	10	mA	
Absolute maximum sum of all input circuit currents during overload condition. 4)	ΣI_{IN} SR	-100	-	100	mA	

- 1) 有效期累计长达2.8小时，脉冲形式跟随电源接通阶段，其中上升和下降时间与系统电容和电感有关。
- 2) 由于关断期间 EVRC 输出电压振荡， V_{DD} 可以降至-0.72V。对于 V_{DD} ，关断相期间输入电平低至 -0.72V 不会造成任何损坏或可靠性问题。
- 3) 只要不违反受影响焊盘的过载引脚可靠性章节中定义的时间和电流，低于 V_{INmin} 的电压就不会对器件可靠性产生影响。
- 4) 此参数是绝对最大额定值，长时间暴露于绝对最大额定值可能会损坏器件。
- 5) 指定的最小和最大值表示在运行期间未使用的任何快速、RFast、慢速和 S 级焊盘的输出端出现短路条件时必须维持的电流限值。
这也涵盖了 $C_L = 200\text{pF}$ 时由于操作切换而产生的输出电流。

电气规格 过载时的引脚可靠性

3.3 过载下的引脚可靠性

当接收来自高压设备的信号时，低压设备会出现超出其自身 IO 电源规格的过载电流和电压。

下表定义了满足以下所有条件的情况下不会对可靠性造成任何负面影响的过载条件：

- 不超过过载条件允许的时间间隔（在注释栏中定义）。如果没有定义时间限制，则允许的时间包括“运行寿命小时数”和“非活动寿命小时数”。表 3-67 中的小时数和 表3-68 仅作为示例，适用的数字由英飞凌接受的客户资料定义。
- 工作条件满足
 - 焊盘供电电平
 - 温度

如果引脚电流超出工作条件但在过载参数范围内，则无法再保证此引脚的参数功能符合工作条件中的规定。但在大多数情况下，操作仍可进行，但参数会有所放宽。

表 3-2 过载参数

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current on any digital pin during overload condition	I_{IN}	-5	-	5	mA	except LVDS pins
		-15 ¹⁾	-	15 ¹⁾	mA	except LVDS pins; limited to max. 20 pulses with 1ms pulse length
Input current on LVDS pin during overload condition	I_{INLVDS}	-3	-	3	mA	
Input current on analog input pin during overload condition	I_{INANA}	-3	-	3	mA	
		-5	-	5	mA	limited to 60h over lifetime
Absolute sum of all analog input currents for analog inputs during overload condition	I_{INSA}	-20	-	20	mA	
Absolute maximum sum of all input circuit currents during overload condition (digital and analog combined)	ΣI_{INS}	-100	-	100	mA	
Signal voltage over/undershoot at GPIOs	V_{OUS}	$V_{SS} - 2$	-	$V_{EXT/FLEX/FLEX2} + 2$	V	limited to 60h over lifetime; Valid for non LVDS and analog pads
Sum of all inactive device pin currents	I_{IDS}	-100	-	100	mA	
Static pin output current	I_{OUTCC}	-	-	2.5	mA	100% duty cycle; output driver = medium
		-	-	5	mA	100% duty cycle; output driver = strong

电气规格 过载时的引脚可靠性

表 3-2 过载参数 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overload coupling factor for digital inputs, negative	$K_{\text{OVDN CC}}$	-	-	$3 \cdot 10^{-4}$		Overload injected on GPIO non LVDS pad and affecting neighbor fast pads; $-5\text{mA} < I_{\text{IN}} < 0\text{mA}$
		-	-	$2 \cdot 10^{-3}$		Overload injected on GPIO non LVDS pad and affecting neighbor slow pads VGATE1N and VGATE1P; $-5\text{mA} < I_{\text{IN}} < 0\text{mA}$
		-	-	$1 \cdot 10^{-4}$		Overload injected on GPIO non LVDS pad and affecting neighbor slow pads; $-5\text{mA} < I_{\text{IN}} < 0\text{mA}$
		-	-	0.8		Overload injected on LVDS RX pad and affecting neighbor LVDS pads
		-	-	0.5		Overload injected on LVDS TX pad and affecting neighbor LVDS pads
Overload coupling factor for digital inputs, positive	$K_{\text{OVDP CC}}$	-	-	$1.5 \cdot 10^{-3}$		Overload injected on GPIO non LVDS pad and affecting neighbor GPIO non LVDS pads
		-	-	1		Overload injected on LVDS RX pad and affecting neighbor LVDS pads
		-	-	$5 \cdot 10^{-3}$		Overload injected on LVDS TX pad and affecting neighbor LVDS pads
Overload coupling factor for analog inputs, negative ²⁾	$K_{\text{OVAN CC}}$	-	-	$1 \cdot 10^{-4}$		Analog inputs overlaid with slow pads or pull down diagnostics; $-5\text{mA} < I_{\text{IN}} < 0\text{mA}$
		-	-	$1 \cdot 10^{-5}$		else; $-5\text{mA} < I_{\text{IN}} < 0\text{mA}$

电气规格 过载时的引脚可靠性

表 3-2 过载参数 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overload coupling factor for analog inputs, positive ²⁾	$K_{OVAP\ CC}$	-	-	$2 \cdot 10^{-4}$		Analog inputs overlaid with slow pads or pull down diagnostics; $0\text{mA} < I_{IN} < 5\text{mA}$
		-	-	$2 \cdot 10^{-5}$		else; $0\text{mA} < I_{IN} < 5\text{mA}$

1) 降低的 VADC / DSADC 结果精度和 / 或 GPIO 输入电平 (V_{IL} 和 V_{IH}) 可能与指定参数不同。

2) 模拟输入上的过载耦合是由焊盘、输入多路复用器和周围结构之间的寄生效应引起的。

已针对所有通道排列验证了给定的参数。还观察一个引脚与多个通道的多个连接。

电气规格工作条件

3.4 工作条件

为了确保 TC37x 的正确操作和可靠性，不得超过以下工作条件。除非另有说明，以下部分中指定的所有参数均指这些工作条件。

施加到 TC37x 的数字电源电压必须是静态调节电压。

下表中指定的所有参数均指这些操作条件（见下表），除非在注释/测试条件栏中另有说明。

表 3-3 工作条件

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SRI frequency	f_{SRI} SR	-	-	300	MHz	
CPU Frequency (All CPUs)	f_{CPUx} SR	-	-	300	MHz	
PLL0 output frequency	f_{PLL0} SR	20	-	300	MHz	
SPB frequency	f_{SPB} SR	-	-	100	MHz	
FSI2 frequency	f_{FSI2} SR	-	-	300	MHz	
FSI frequency	f_{FSI} SR	20	-	100	MHz	
GTM frequency	f_{GTM} SR	-	-	200	MHz	
STM frequency	f_{STM} SR	-	-	100	MHz	
ERAY frequency	f_{ERAY} SR	-	80	-	MHz	
BBB frequency	f_{BBB} SR	-	-	150	MHz	
VADC frequency	f_{ADC} SR	-	-	160	MHz	
ASCLIN Operating Frequency	f_{ASCLINx} SR	-	-	200	MHz	
CAN frequency	f_{CAN} SR	-	-	80	MHz	
I2C frequency	f_{I2C} SR	-	-	100	MHz	
Operating MSC Frequency	f_{MSC} SR	-	-	200	MHz	
PLL1 output frequency from PER PLL	f_{PLL1} SR	20	-	320	MHz	
PLL2 output frequency from PER PLL	f_{PLL2} SR	20	-	200	MHz	
QSPI Frequency	f_{QSPI} SR	-	-	200	MHz	
ADAS clock frequency	f_{ADAS} CC	200	-	300	MHz	
MCANH frequency	f_{MCANH} CC	-	-	100	MHz	
GETH frequency	f_{GETH} CC	100	-	150	MHz	
Ambient Temperature	T_{A} SR	-40	-	125	°C	valid for all SAK products
		-40	-	150	°C	valid for all SAL products with package
		-40	-	170	°C	valid for all SAL products without package

电气规格工作条件

表 3-3 工作条件 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Junction Temperature	T_J SR	-40	-	150	°C	valid for all SAK products
		-40	-	170	°C	valid for all SAL products
Core Supply Voltage	V_{DD} SR	1.125 ¹⁾	1.25	1.375 ²⁾	V	
ADC analog supply voltage	V_{DDM} SR	2.97	5.0	5.5 ³⁾	V	
Digital external supply voltage for pads and EVR	V_{EXT} SR	4.5	5.0	5.5 ³⁾	V	Nominal 5V Pad / Port Pin supply range. 5V pad parameters are valid.
		2.97	3.3	3.63	V	Nominal 3.3V Pad / Port Pin supply range with VDDP3 supplied externally and EVR33 inactive. 3.3V pad parameters are valid.
		3.6	-	4.5	V	Flash configured in cranking mode; Flash read operation with reduced performance. EVR33 active in low voltage mode. 3.3V pad parameters are valid.
		2.97	-	3.6	V	Incase EVR33 is active, Flash configured in sleep mode and execution switched to RAM. 3.3V pad parameters are valid.
Digital supply voltage for Flex port	V_{FLEX} SR	2.97	-	4.0	V	3.3V pad parameters are valid; also valid for V_{FLEX2}
		4.5	5.0	5.5 ³⁾	V	5V pad parameters are valid; also valid for V_{FLEX2}
Digital supply voltage for Flash	V_{DDP3} SR	2.97	3.3	3.63 ⁴⁾	V	
		2.6	-	3.63	V	Flash configured in cranking mode; Flash read operation with reduced performance.
Digital ground voltage	V_{SS} SR	0	-	-	V	
Analog ground voltage for V_{DDM}	V_{SSM} CC	-0.1	0	0.1	V	

电气规格工作条件

表 3-3 工作条件 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital external supply voltage for EVR and during Standby mode	$V_{\text{EVRSB}}^{\text{SR}}$	2.97 ⁵⁾	-	5.5	V	
Voltage to ensure defined pad states	$V_{\text{DDPPA}}^{\text{CC}}$	1.3 ⁶⁾	-	-	V	
Digital supply voltage for Flex2 port	$V_{\text{FLEX2}}^{\text{SR}}$	2.97	3.3	3.63	V	3.3V pad parameters are valid
		3.63	5	5.5	V	5V pad parameters are valid

- 1) 当 $V_{\text{DD}} 1.08\text{V} \leq V_{\text{DD}} < 1.125\text{V}$ 时, 仍可进行操作, 但参数会有所放宽。
- 2) 允许过冲电压至 1.69V, 但累计持续时间不得超过 2 小时, ADC 精度降低且漏电增加。
- 3) 允许过冲电压至 6.5V, 但累计持续时间不得超过 2 小时, ADC 精度降低且漏电增加。
- 4) 允许过冲电压至 4.29V, 但累计持续时间不得超过 2 小时, ADC 精度降低且漏电增加。
- 5) V_{EVRSB} 供电电压在待机模式下可降至 2.6V。 V_{EVRSB} 供电引脚上需接一个 100nF 电容。
- 6) 当 VEXT 达到此电平时, HWCFG[6] 引脚被锁存, 并且在端口引脚处激活上拉或三态。

供电电压随时间的限制

$V_{\text{EXT/FLEX/DDM}}$ 电源轨的最大工作电压在整个使用寿命期间受到限制。

下面的电压曲线就是一个例子。为了满足质量和可靠性目标, 特定应用的电压分布需要经过英飞凌科技公司的验证。

表 3-4 电压曲线示例

$V_{\text{EXT/FLEX/DDM}} =$	Duration [h]
$5.4\text{ V} < V_{\text{EXT/FLEX/DDM}} \leq 5.5\text{ V}$	$\leq 5\%$ of lifetime
$5.15\text{ V} < V_{\text{EXT/FLEX/DDM}} \leq 5.4\text{ V}$	$\leq 15\%$ of lifetime
$4.85\text{ V} < V_{\text{EXT/FLEX/DDM}} \leq 5.15\text{ V}$	$\leq 60\%$ of lifetime
$4.6\text{ V} < V_{\text{EXT/FLEX/DDM}} \leq 4.85\text{ V}$	$\leq 15\%$ of lifetime
$4.5\text{ V} < V_{\text{EXT/FLEX/DDM}} \leq 4.6\text{ V}$	$\leq 5\%$ of lifetime

在整个使用寿命期间, V_{DD} 电源轨的最大工作电压是有限的。

下面的电压曲线就是一个例子。为了满足质量和可靠性目标, 特定应用的电压分布需要经过英飞凌科技公司的调整和批准。

表 3-5 电压曲线示例

$V_{\text{DD}} =$	Duration [h]
$1.325\text{ V} < V_{\text{DD}} \leq 1.375\text{ V}$	$\leq 5\%$ of lifetime
$1.275\text{ V} < V_{\text{DD}} \leq 1.325\text{ V}$	$\leq 15\%$ of lifetime
$1.225\text{ V} < V_{\text{DD}} \leq 1.275\text{ V}$	$\leq 60\%$ of lifetime

电气规格工作条件

表 3-5 电压曲线示例

V_{DD}	Duration [h]
$1.175\text{ V} < V_{DD} \leq 1.225\text{ V}$	$\leq 15\%$ of lifetime
$1.125\text{ V} < V_{DD} \leq 1.175\text{ V}$	$\leq 5\%$ of lifetime

电气规格 5 V / 3.3 V 可切换焊盘

3.5 5 V / 3.3 V 可切换焊盘

焊盘类别慢速 GPIO 和快速 GPIO 支持汽车级 (AL) 或 TTL 级 (TTL) 操作。参数是为 AL 操作定义的，并在 TTL 操作中降低。

表 3-6 **PORST** 焊盘

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
PORST pad Output current	$I_{\text{PORST CC}}$	13	-	-	mA	$V_{\text{EXT}} = 2.97\text{V}$; $V_{\text{PORST}} = 0.9\text{V}$
Spike filter always blocked pulse duration	$t_{\text{SF1 CC}}$	-	-	80	ns	
Spike filter pass-through blocked pulse duration	$t_{\text{SF2 CC}}$	260	-	-	ns	without additional PORST Digital Filter active (PORSTDF = 0).
Input hysteresis ¹⁾	$HYS \text{ CC}$	$0.055 * V_{\text{EXT}}$	-	-	V	non of the neighbor pads are used as output; TTL (degraded, used for CIF)
Pull-down current ²⁾	$I_{\text{PDL CC}}$	-	-	130	μA	V_{IH} ; TTL (degraded, used for CIF)
		15	-	-	μA	V_{IL} ; TTL (degraded, used for CIF)
Input leakage current	$I_{\text{OZ CC}}$	-450	-	450	nA	$T_J \leq 150^\circ\text{C}$; $(0.1 * V_{\text{EXT}}) < V_{\text{IN}} < (0.9 * V_{\text{EXT}})$
		-500	-	500	nA	$T_J \leq 150^\circ\text{C}$; else
		-900	-	900	nA	$T_J \leq 170^\circ\text{C}$; $(0.1 * V_{\text{EXT}}) < V_{\text{IN}} < (0.9 * V_{\text{EXT}})$
		-950	-	950	nA	$T_J \leq 170^\circ\text{C}$; else
Input high voltage level	$V_{\text{IH SR}}$	1.4	-	-	V	TTL (degraded, used for CIF); $V_{\text{EXT}} = 2.97\text{V}$
		2.0	-	-	V	TTL; $V_{\text{EXT}} = 4.5\text{V}$
Input low voltage level	$V_{\text{IL SR}}$	-	-	0.5	V	TTL (degraded, used for CIF); $V_{\text{EXT}} = 2.97\text{V}$
		-	-	0.8	V	TTL; $V_{\text{EXT}} = 4.5\text{V}$
Pin capacitance	$C_{\text{IO CC}}$	-	2	3	pF	in addition 2.5pF from package to be added

1) 实施滞回是为了避免亚稳态和由于内部地弹而引起的切换。不能保证它能抑制由于外部系统噪声而引起的切换。

2) 下拉电阻的值通过表 VADC 5V 中的参数 R_{MDD} 定义。

电气规格 5 V / 3.3 V 可切换焊盘

表 3-7 快速 5V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	$R_{\text{DS(on)}}^{\text{CC}}$	125	225	320	Ohm	medium driver; $I_{\text{OH}} / I_{\text{OL}} = 2\text{mA}$
		31	55	80	Ohm	strong driver; $I_{\text{OH}} / I_{\text{OL}} = 8\text{mA}$
Rise / Fall time ^{1) 2)}	$t_{\text{RF}}^{\text{CC}}$	1.6	-	3.2	ns	$C_{\text{L}} = 25\text{pF}$; driver = strong sharp edge; from $0.2 * V_{\text{EXT/FLEX/FLEX2/EVRSB}}$ to $0.8 * V_{\text{EXT/FLEX/FLEX2/EVRSB}}$
		$4+0.55 * C_{\text{L}}$	$4+0.75 * C_{\text{L}}$	$12+1.0 * C_{\text{L}}$	ns	driver = medium; $C_{\text{L}} \leq 200\text{pF}$
		$1.0+0.18 * C_{\text{L}}$	$2.5+0.27 * C_{\text{L}}$	$5.0+0.35 * C_{\text{L}}$	ns	driver = strong edge = medium; $C_{\text{L}} \leq 200\text{pF}$
		$0.5+0.08 * C_{\text{L}}$	$0.5+0.11 * C_{\text{L}}$	$1.0+0.17 * C_{\text{L}}$	ns	driver = strong edge = sharp; $C_{\text{L}} \leq 200\text{pF}$
Asymmetry of sending	$t_{\text{TX_ASYM}}^{\text{CC}}$	-1	-	1	ns	valid for all data rates excluding clock tolerance
Input frequency	$f_{\text{IN}}^{\text{CC}}$	-	-	160	MHz	
Input hysteresis ³⁾	HYS^{CC}	$0.09 * V_{\text{EXT/FLEX/FLEX2/EVRSB}}$	-	-	V	non of the neighbor pads are used as output; AL
		$0.075 * V_{\text{EXT/FLEX/FLEX2/EVRSB}}$	-	-	V	non of the neighbor pads are used as output; TTL
		75	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current ⁴⁾	$I_{\text{PUH}}^{\text{CC}}$	30	-	-	μA	V_{IH} ; AL or TTL
		-	-	130	μA	V_{IL} ; AL or TTL
Pull-down current ⁵⁾	$I_{\text{PDL}}^{\text{CC}}$	-	-	130	μA	V_{IH} ; AL or TTL
		30	-	-	μA	V_{IL} ; AL
		28	-	-	μA	V_{IL} ; TTL

电气规格 5 V / 3.3 V 可切换焊盘

表 3-7 快速 5V GPIO (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current	$I_{OZ\ CC}$	-1100	-	1100	nA	$T_J \leq 150^\circ\text{C}$; $(0.1 \cdot V_{EXT/FLEX/FLEX2/EVRSB}) < V_{IN} < (0.9 \cdot V_{EXT/FLEX/FLEX2/EVRSB})$
		-2500	-	2500	nA	$T_J \leq 150^\circ\text{C}$; $(0.1 \cdot V_{EXT/FLEX/FLEX2}) < V_{IN} < (0.9 \cdot V_{EXT/FLEX/FLEX2})$; LVDS_TX / Fast pad type
		-6000	-	6000	nA	$T_J \leq 150^\circ\text{C}$; LVDS_RX / Fast pad type; else
		-3200	-	3200	nA	$T_J \leq 150^\circ\text{C}$; LVDS_TX / Fast pad type; else
		-1500	-	1500	nA	$T_J \leq 150^\circ\text{C}$; else
		-2000	-	2000	nA	$T_J \leq 170^\circ\text{C}$; $(0.1 \cdot V_{EXT/FLEX/FLEX2/EVRSB}) < V_{IN} < (0.9 \cdot V_{EXT/FLEX/FLEX2/EVRSB})$
		-4000	-	4000	nA	$T_J \leq 170^\circ\text{C}$; $(0.1 \cdot V_{EXT/FLEX/FLEX2}) < V_{IN} < (0.9 \cdot V_{EXT/FLEX/FLEX2})$; LVDS_TX / Fast pad type
		-13500	-	13500	nA	$T_J \leq 170^\circ\text{C}$; LVDS_RX / Fast pad type; else
		-5100	-	5100	nA	$T_J \leq 170^\circ\text{C}$; LVDS_TX / Fast pad type; else
Input high voltage level	$V_{IH\ SR}$	$0.7 \cdot V_{EXT/FLEX/FLEX2/EVRSB}$	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	$V_{IL\ SR}$	-	-	$0.44 \cdot V_{EXT/FLEX/FLEX2/EVRSB}$	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	$V_{ILD\ SR}$	-50	-	50	mV	max. variation of 1ms; $V_{EXT/FLEX/FLEX2/EVRSB} = \text{constant}$; AL

电气规格 5 V / 3.3 V 可切换焊盘

表 3-7 快速 5V GPIO (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pin capacitance	$C_{IO\ CC}$	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	$t_{SET\ CC}$	-	-	100	ns	

1) 在公式中，需要以 pF 为单位输入 C_L 的值才能获得 ns 为单位的结果。

2) 上升/下降时间定义为焊盘供电电压的 10% - 90%。

3) 实施滞回是为了避免亚稳态和由于内部地弹而引起的切换。不能保证它能抑制由于外部系统噪声而引起的切换。

4) 上拉电阻的值通过表 VADC 5V 中的参数 R_{MDU} 定义。

5) 下拉电阻的值通过表 VADC 5V 中的参数 R_{MDD} 定义。

表 3-8 快速 3.3V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	$R_{DS(on)\ CC}$	125	225	320	Ohm	medium driver; $I_{OH/OL} = 2mA$
		31	55	80	Ohm	strong driver; $I_{OH/OL} = 8mA$
Rise / Fall time ^{1) 2)}	$t_{RF\ CC}$	1.6	-	4.5	ns	$C_L = 25pF$; driver = strong sharp edge; from $0.2 * V_{EXT/FLEX/FLEX2/EVRSB}$ to $0.8 * V_{EXT/FLEX/FLEX2/EVRSB}$
		-	-	5	ns	$C_L = 25pF$; driver = strong sharp edge; from 0.8V to 2.0V (RMII)
		$2+0.57*C_L$	$5.5+0.75*C_L$	$10+1.25*C_L$	ns	driver = medium; $C_L \leq 200pF$
		$1.5+0.18*C_L$	$1.5+0.28*C_L$	$8+0.4*C_L$	ns	driver = strong edge = medium; $C_L \leq 200pF$
		$0.75+0.08*C_L$	$0.75+0.11*C_L$	$2.5+0.21*C_L$	ns	driver = strong edge = sharp; $C_L \leq 200pF$
Asymmetry of sending	$t_{TX_ASYM\ CC}$	-1	-	1	ns	valid for all data rates excluding clock tolerance
Input frequency	$f_{IN\ CC}$	-	-	160	MHz	

电气规格 5 V / 3.3 V 可切换焊盘

表 3-8 快速 3.3V GPIO (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input hysteresis ³⁾	HYS_{CC}	0.055 * $V_{EXT/FLEX/F}$ LEX2/EVRSB	-	-	V	non of the neighbor pads are used as output; AL
		0.09 * $V_{EXT/FLEX/F}$ LEX2/EVRSB	-	-	V	non of the neighbor pads are used as output; TTL
		0.055 * $V_{EXT/FLEX/F}$ LEX2/EVRSB	-	-	V	non of the neighbor pads are used as output;TTL (degraded, used for CIF)
		125	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current ⁴⁾	$I_{PUH_{CC}}$	17	-	-	μA	V_{IH} ; AL and TTL (degraded, used for CIF)
		11	-	-	μA	V_{IH} ; TTL
		-	-	80	μA	V_{IL} ; AL and TTL and TTL (degraded, used for CIF)
Pull-down current ⁵⁾	$I_{PDL_{CC}}$	-	-	105	μA	V_{IH} ; AL and TTL (degraded, used for CIF)
		-	-	115	μA	V_{IH} ; TTL
		19	-	-	μA	V_{IL} ; AL and TTL
		15	-	-	μA	V_{IL} ; TTL (degraded, used for CIF)

电气规格 5 V / 3.3 V 可切换焊盘

表 3-8 快速 3.3V GPIO (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current	$I_{OZ\ CC}$	-1100	-	1100	nA	$T_J \leq 150^\circ\text{C}$; $(0.1 \cdot V_{EXT/FLEX/FLEX2/EVRSB}) < V_{IN} < (0.9 \cdot V_{EXT/FLEX/FLEX2/EVRSB})$
		-2500	-	2500	nA	$T_J \leq 150^\circ\text{C}$; $(0.1 \cdot V_{EXT/FLEX/FLEX2}) < V_{IN} < (0.9 \cdot V_{EXT/FLEX/FLEX2})$; LVDS_TX / Fast pad type
		-6000	-	6000	nA	$T_J \leq 150^\circ\text{C}$; LVDS_RX / Fast pad type; else
		-3200	-	3200	nA	$T_J \leq 150^\circ\text{C}$; LVDS_TX / Fast pad type; else
		-1500	-	1500	nA	$T_J \leq 150^\circ\text{C}$; else
		-2000	-	2000	nA	$T_J \leq 170^\circ\text{C}$; $(0.1 \cdot V_{EXT/FLEX/FLEX2/EVRSB}) < V_{IN} < (0.9 \cdot V_{EXT/FLEX/FLEX2/EVRSB})$
		-4000	-	4000	nA	$T_J \leq 170^\circ\text{C}$; $(0.1 \cdot V_{EXT/FLEX/FLEX2}) < V_{IN} < (0.9 \cdot V_{EXT/FLEX/FLEX2})$; LVDS_TX / Fast pad type
		-13500	-	13500	nA	$T_J \leq 170^\circ\text{C}$; LVDS_RX / Fast pad type; else
		-5100	-	5100	nA	$T_J \leq 170^\circ\text{C}$; LVDS_TX / Fast pad type; else
Input high voltage level	$V_{IH\ SR}$	$0.7 \cdot V_{EXT/FLEX/FLEX2/EVRSB}$	-	-	V	AL
		2.0	-	-	V	TTL
		1.4	-	-	V	TTL (degraded, used for CIF)
Input low voltage level	$V_{IL\ SR}$	-	-	$0.42 \cdot V_{EXT/FLEX/FLEX2/EVRSB}$	V	AL
		-	-	0.8	V	TTL
		-	-	0.5	V	TTL (degraded, used for CIF)
Input low/high voltage level	$V_{ILH\ SR}$	1.0	-	1.9	V	RGMII; no hysteresis available

电气规格 5 V / 3.3 V 可切换焊盘

表 3-8 快速 3.3V GPIO (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low threshold variation	$V_{ILD\ SR}$	-33	-	33	mV	max. variation of 1ms; $V_{EXT/FLEX/FLEX2/EVRSB} =$ constant; AL
Pin capacitance	$C_{IO\ CC}$	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	$t_{SET\ CC}$	-	-	100	ns	

- 1) 在公式中，需要以 pF 为单位输入 C_L 的值才能获得 ns 为单位的结果。
- 2) 上升/下降时间定义为焊盘供电电压的 10% - 90%。
- 3) 实施滞回是为了避免亚稳态和由于内部地弹而引起的切换。不能保证它能抑制由于外部系统噪声而引起的切换。
- 4) 上拉电阻的值通过表 VADC 5V 中的参数 R_{MDU} 定义。
- 5) 下拉电阻的值通过表 VADC 5V 中的参数 R_{MDD} 定义。

表 3-9 慢速 5V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	$R_{DS(on)\ CC}$	125	225	320	Ohm	medium driver; $I_{OH/OL}$ = 2mA
Rise / Fall time ^{1) 2)}	$t_{RF\ CC}$	$4+0.55 \cdot C_L$	$4+0.75 \cdot C_L$	$12+1 \cdot C_L$	ns	driver = medium edge = medium ; $C_L \leq 200pF$
		$1.5+0.25 \cdot C_L$	$2.5+0.40 \cdot C_L$	$7+0.55 \cdot C_L$	ns	driver = medium edge = sharp ; $C_L \leq 200pF$
Asymmetry of sending	$t_{TX_ASYM\ CC}$	-1	-	1	ns	valid for all data rates excluding clock tolerance
Input frequency	$f_{IN\ CC}$	-	-	160	MHz	
Input hysteresis ³⁾	$HYS\ CC$	$0.09 \cdot V_{EXT/FLEX/FLEX2/EVRSB}$	-	-	V	non of the neighbor pads are used as output; AL
		$0.075 \cdot V_{EXT/FLEX/FLEX2/EVRSB}$	-	-	V	non of the neighbor pads are used as output; TTL
		75	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL

电气规格 5 V / 3.3 V 可切换焊盘

表 3-9 慢速 5V GPIO (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pull-up current ⁴⁾	I_{PUH} CC	30	-	-	μA	V_{IH} ; AL or TTL; except VGATE1P; except VGATE1N and $T_J > 150^{\circ}\text{C}$
		-	-	130	μA	V_{IL} ; AL or TTL; except VGATE1P; except VGATE1N and $T_J > 150^{\circ}\text{C}$
Pull-down current ⁵⁾	I_{PDL} CC	-	-	130	μA	V_{IH} ; AL or TTL
		30	-	-	μA	V_{IL} ; AL
		28	-	-	μA	V_{IL} ; TTL
Input leakage current	I_{OZ} CC	-300	-	300	nA	$T_J \leq 150^{\circ}\text{C}$; $(0.1 \cdot V_{EXT/FLEX/FLEX2/EVRSB}) < V_{IN} < (0.9 \cdot V_{EXT/FLEX/FLEX2/EVRSB})$
		-400	-	400	nA	$T_J \leq 150^{\circ}\text{C}$; else
		-600	-	600	nA	$T_J \leq 170^{\circ}\text{C}$; $(0.1 \cdot V_{EXT/FLEX/FLEX2/EVRSB}) < V_{IN} < (0.9 \cdot V_{EXT/FLEX/FLEX2/EVRSB})$
		-750	-	750	nA	$T_J \leq 170^{\circ}\text{C}$; else
		-18000	-	18000	nA	P32.0 and P32.1; $T_J \leq 150^{\circ}\text{C}$
		-38000	-	38000	nA	P32.0 and P32.1; $T_J \leq 170^{\circ}\text{C}$
Input high voltage level	V_{IH} SR	$0.7 \cdot V_{EXT/FLEX/FLEX2/EVRSB}$	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} SR	-	-	$0.44 \cdot V_{EXT/FLEX/FLEX2/EVRSB}$	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	V_{ILD} SR	-50	-	50	mV	max. variation of 1ms; $V_{EXT/FLEX/FLEX2/EVRSB} = \text{constant}$; AL
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) 在公式中，需要以 pF 为单位输入 C_L 的值才能获得 ns 为单位的結果。

电气规格 5 V / 3.3 V 可切换焊盘

- 2) 上升/下降时间定义为焊盘供电电压的 10% - 90%。
- 3) 实施滞回是为了避免亚稳态和由于内部地弹而引起的切换。不能保证它能抑制由于外部系统噪声而引起的切换。
- 4) 上拉电阻的值通过表 VADC 5V 中的参数 R_{MDU} 定义。
- 5) 下拉电阻的值通过表 VADC 5V 中的参数 R_{MDD} 定义。

表 3-10 慢速 3.3V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	$R_{DS(on)}^{CC}$	125	225	320	Ohm	medium driver; $I_{OH/OL} = 2mA$
Rise / Fall time ^{1) 2)}	t_{RF}^{CC}	$2+0.57 \cdot C_L$	$5.5+0.75 \cdot C_L$	$10+1.25 \cdot C_L$	ns	driver = medium edge = medium ; $C_L \leq 200pF$
		$2+0.30 \cdot C_L$	$3.5+0.50 \cdot C_L$	$5+0.70 \cdot C_L$	ns	driver = medium edge = sharp ; $C_L \leq 200pF$
Asymmetry of sending	$t_{TX_ASYM}^{CC}$	-1	-	1	ns	valid for all data rates excluding clock tolerance
Input frequency	f_{IN}^{CC}	-	-	160	MHz	
Input hysteresis ³⁾	HYS^{CC}	$0.055 \cdot V_{EXT/FLEX/FLEX2/EVRSB}$	-	-	V	non of the neighbor pads are used as output; AL
		$0.09 \cdot V_{EXT/FLEX/FLEX2/EVRSB}$	-	-	V	non of the neighbor pads are used as output; TTL
		$0.055 \cdot V_{EXT/FLEX/FLEX2/EVRSB}$	-	-	V	non of the neighbor pads are used as output;TTL (degraded, used for CIF)
		125	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL

电气规格 5 V / 3.3 V 可切换焊盘

表 3-10 慢速 3.3V GPIO (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pull-up current ⁴⁾	$I_{PUH\ CC}$	17	-	-	μA	V_{IH} ; AL and TTL (degraded, used for CIF); except VGATE1P; except VGATE1N and $T_J > 150^{\circ}\text{C}$
		11	-	-	μA	V_{IH} ; TTL; except VGATE1P; except VGATE1N and $T_J > 150^{\circ}\text{C}$
		-	-	80	μA	V_{IL} ; AL and TTL and TTL (degraded, used for CIF); except VGATE1P; except VGATE1N and $T_J > 150^{\circ}\text{C}$
Pull-down current ⁵⁾	$I_{PDL\ CC}$	-	-	105	μA	V_{IH} ; AL and TTL (degraded, used for CIF)
		-	-	115	μA	V_{IH} ; TTL
		19	-	-	μA	V_{IL} ; AL and TTL
		15	-	-	μA	V_{IL} ; TTL (degraded, used for CIF)
Input leakage current	$I_{OZ\ CC}$	-300	-	300	nA	$T_J \leq 150^{\circ}\text{C}$; $(0.1 \cdot V_{EXT/FLEX/FLEX2/EVRSB}) < V_{IN} < (0.9 \cdot V_{EXT/FLEX/FLEX2/EVRSB})$
		-400	-	400	nA	$T_J \leq 150^{\circ}\text{C}$; else
		-600	-	600	nA	$T_J \leq 170^{\circ}\text{C}$; $(0.1 \cdot V_{EXT/FLEX/FLEX2/EVRSB}) < V_{IN} < (0.9 \cdot V_{EXT/FLEX/FLEX2/EVRSB})$
		-750	-	750	nA	$T_J \leq 170^{\circ}\text{C}$; else
		-18000	-	18000	nA	P32.0 and P32.1; $T_J \leq 150^{\circ}\text{C}$
		-38000	-	38000	nA	P32.0 and P32.1; $T_J \leq 170^{\circ}\text{C}$
Input high voltage level	$V_{IH\ SR}$	$0.7 \cdot V_{EXT/FLEX/FLEX2/EVRSB}$	-	-	V	AL
		2.0	-	-	V	TTL
		1.4	-	-	V	TTL (degraded, used for CIF)

电气规格 5 V / 3.3 V 可切换焊盘

表 3-10 慢速 3.3V GPIO (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage level	V_{IL} SR	-	-	0.42 * $V_{EXT/FLEX/FLEX2/EVRSB}$	V	AL
		-	-	0.8	V	TTL
		-	-	0.5	V	TTL (degraded, used for CIF)
Input low/high voltage level	V_{ILH} SR	1.0	-	1.9	V	RGMII; no hysteresis available
Input low threshold variation	V_{ILD} SR	-33	-	33	mV	max. variation of 1ms; $V_{EXT/FLEX/FLEX2/EVRSB} =$ constant; AL
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

- 1) 在公式中，需要以 pF 为单位输入 C_L 的值才能获得 ns 为单位的结果。
- 2) 上升/下降时间定义为焊盘供电电压的 10% - 90%。
- 3) 实施滞回是为了避免亚稳态和由于内部地弹而引起的切换。不能保证它能抑制由于外部系统噪声而引起的切换。
- 4) 上拉电阻的值通过表 VADC 5V 中的参数 R_{MDU} 定义。
- 5) 下拉电阻的值通过表 VADC 5V 中的参数 R_{MDD} 定义。

表 3-11 RFast 5V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	$R_{DS(on)}$ CC	125	225	320	Ohm	medium driver; $I_{OH/OL} = 2mA$
		31	55	80	Ohm	strong driver; $I_{OH/OL} = 8mA$
Rise / Fall time ^{1) 2)}	t_{RF} CC	1.6	-	3.2	ns	$C_L = 25pF$; driver = strong sharp edge; from $0.2 * V_{FLEX/FLEX2}$ to $0.8 * V_{FLEX/FLEX2}$
		$4+0.55 * C_L$	$4+0.75 * C_L$	$12+1.0 * C_L$	ns	driver = medium; $C_L \leq 200pF$
		$1.0+0.18 * C_L$	$2.5+0.27 * C_L$	$5.0+0.35 * C_L$	ns	driver = strong edge = medium; $C_L \leq 200pF$
		$0.5+0.08 * C_L$	$0.5+0.11 * C_L$	$1.0+0.17 * C_L$	ns	driver = strong edge = sharp; $C_L \leq 200pF$
Asymmetry of sending	t_{TX_ASYM} CC	-0.5	-	0.5	ns	valid for all data rates excluding clock tolerance

电气规格 5 V / 3.3 V 可切换焊盘

表 3-11 RFast 5V GPIO (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	$f_{IN\ CC}$	-	-	160	MHz	
Input hysteresis ³⁾	$HYS\ CC$	$0.09 \cdot \frac{V_{FLEX/FLEX2}}{2}$	-	-	V	non of the neighbor pads are used as output; AL
		$0.075 \cdot \frac{V_{FLEX/FLEX2}}{2}$	-	-	V	non of the neighbor pads are used as output; TTL
		75	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current ⁴⁾	$I_{PUH\ CC}$	30	-	-	μA	V_{IH} ; AL or TTL
		-	-	130	μA	V_{IL} ; AL or TTL
Pull-down current ⁵⁾	$I_{PDL\ CC}$	-	-	130	μA	V_{IH} ; AL or TTL
		30	-	-	μA	V_{IL} ; AL
		28	-	-	μA	V_{IL} ; TTL
Input leakage current	$I_{OZ\ CC}$	-1700	-	1700	nA	$T_J \leq 150^\circ C$; $(0.1 \cdot \frac{V_{FLEX/FLEX2}}{V_{FLEX/FLEX2}}) < V_{IN} < (0.9 \cdot \frac{V_{FLEX/FLEX2}}{V_{FLEX/FLEX2}})$
		-2100	-	2100	nA	$T_J \leq 150^\circ C$; else
		-3000	-	3000	nA	$T_J \leq 170^\circ C$; $(0.1 \cdot \frac{V_{FLEX/FLEX2}}{V_{FLEX/FLEX2}}) < V_{IN} < (0.9 \cdot \frac{V_{FLEX/FLEX2}}{V_{FLEX/FLEX2}})$
		-4000	-	4000	nA	$T_J \leq 170^\circ C$; else
Input high voltage level	$V_{IH\ SR}$	$0.7 \cdot \frac{V_{FLEX/FLEX2}}{2}$	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	$V_{IL\ SR}$	-	-	$0.44 \cdot \frac{V_{FLEX/FLEX2}}{2}$	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	$V_{ILD\ SR}$	-50	-	50	mV	max. variation of 1ms; $V_{FLEX/FLEX2} = \text{constant}$; AL
Pin capacitance	$C_{IO\ CC}$	-	2	3.5	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	$t_{SET\ CC}$	-	-	100	ns	

1) 在公式中，需要以 pF 为单位输入 C_L 的值才能获得 ns 为单位的结果。

电气规格 5 V / 3.3 V 可切换焊盘

- 2) 上升/下降时间定义为焊盘供电电压的 10% - 90%。
- 3) 实施滞回是为了避免亚稳态和由于内部地弹而引起的切换。不能保证它能抑制由于外部系统噪声而引起的切换。
- 4) 上拉电阻的值通过表 VADC 5V 中的参数 R_{MDU} 定义。
- 5) 下拉电阻的值通过表 VADC 5V 中的参数 R_{MDD} 定义。

表 3-12 RFast 3.3V 焊盘

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	$R_{DS(on)}^{CC}$	8	20	30	Ohm	Driver = RGMII; $I_{OH/OL} = 8mA$
		125	225	320	Ohm	medium driver; $I_{OH/OL} = 2mA$
		31	55	80	Ohm	strong driver; $I_{OH/OL} = 8mA$
Input Duty Cycle	f_D^{SR}	47.5	50	52.5		
Rise / Fall time ^{1) 2)}	t_{RF}^{CC}	1.6	-	4.5	ns	$C_L = 25pF$; driver = strong sharp edge; from $0.2 * V_{FLEX/FLEX2}$ to $0.8 * V_{FLEX/FLEX2}$
		-	-	5	ns	$C_L = 25pF$; driver = strong sharp edge; from 0.8V to 2.0V (RMII)
		-	-	1	ns	Driver = RGMII; from 20%V to 80%V; $C_L = 15pF$
		$2+0.57 * C_L$	$5.5+0.75 * C_L$	$10+1.25 * C_L$	ns	driver = medium; $C_L \leq 200pF$
		$1.5+0.18 * C_L$	$1.5+0.28 * C_L$	$8+0.4 * C_L$	ns	driver = strong edge = medium; $C_L \leq 200pF$
		$0.75+0.08 * C_L$	$0.75+0.11 * C_L$	$2.5+0.21 * C_L$	ns	driver = strong edge = sharp; $C_L \leq 200pF$
Asymmetry of sending	$t_{TX_ASYM}^{CC}$	-0.4	-	0.4	ns	valid for all data rates excluding clock tolerance
Input frequency	f_{IN}^{CC}	-	-	160	MHz	

电气规格 5 V / 3.3 V 可切换焊盘

表 3-12 RFast 3.3V 焊盘 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input hysteresis ³⁾	HYS CC	0.055 * $V_{FLEX/FLEX2}$ 2	-	-	V	non of the neighbor pads are used as output; AL
		0.09 * $V_{FLEX/FLEX2}$ 2	-	-	V	non of the neighbor pads are used as output; TTL
		0.055 * $V_{FLEX/FLEX2}$ 2	-	-	V	non of the neighbor pads are used as output;TTL (degraded, used for CIF)
		125	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current ⁴⁾	I_{PUH} CC	17	-	-	μA	V_{IH} ; AL and TTL (degraded, used for CIF)
		11	-	-	μA	V_{IH} ; TTL
		-	-	80	μA	V_{IL} ; AL and TTL and TTL (degraded, used for CIF)
Pull-down current ⁵⁾	I_{PDL} CC	-	-	105	μA	V_{IH} ; AL and TTL (degraded, used for CIF)
		-	-	115	μA	V_{IH} ; TTL
		19	-	-	μA	V_{IL} ; AL and TTL
		15	-	-	μA	V_{IL} ; TTL (degraded, used for CIF)
Input leakage current	I_{OZ} CC	-1700	-	1700	nA	$T_J \leq 150^\circ\text{C}$; $(0.1 * V_{FLEX/FLEX2}) < V_{IN} < (0.9 * V_{FLEX/FLEX2})$
		-2100	-	2100	nA	$T_J \leq 150^\circ\text{C}$; else
		-3000	-	3000	nA	$T_J \leq 170^\circ\text{C}$; $(0.1 * V_{FLEX/FLEX2}) < V_{IN} < (0.9 * V_{FLEX/FLEX2})$
		-4000	-	4000	nA	$T_J \leq 170^\circ\text{C}$; else
Input high voltage level	V_{IH} SR	0.7 * $V_{FLEX/FLEX2}$ 2	-	-	V	AL
		2.0	-	-	V	TTL
		1.4	-	-	V	TTL (degraded, used for CIF)

电气规格 5 V / 3.3 V 可切换焊盘

表 3-12 RFast 3.3V 焊盘 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage level	V_{IL} SR	-	-	0.42 * $V_{FLEX/FLEX}$ 2	V	AL
		-	-	0.8	V	TTL
		-	-	0.5	V	TTL (degraded, used for CIF)
Input low threshold variation	V_{ILD} SR	-33	-	33	mV	max. variation of 1ms; V_{FLEX} = constant; AL
Pin capacitance	C_{IO} CC	-	2	3.5	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

- 1) 在公式中，需要以 pF 为单位输入 C_L 的值才能获得 ns 为单位的结果。
- 2) 上升/下降时间定义为焊盘供电电压的 10% - 90%。
- 3) 实施滞回是为了避免亚稳态和由于内部地弹而引起的切换。不能保证它能抑制由于外部系统噪声而引起的切换。
- 4) 上拉电阻的值通过表 VADC 5V 中的参数 R_{MDU} 定义。
- 5) 下拉电阻的值通过表 VADC 5V 中的参数 R_{MDD} 定义。

表 3-13 S 类 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{IN} CC	-	-	160	MHz	
Input hysteresis ¹⁾	HYS CC	0.09 * V_{DDM}	-	-	V	non of the neighbor pads are used as output; AL
		0.075 * V_{DDM}	-	-	V	non of the neighbor pads are used as output; TTL
		75	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current ²⁾	I_{PUH} CC	30	-	-	μA	V_{IH} ; AL or TTL
		-	-	130	μA	V_{IL} ; AL or TTL
Pull-down current ³⁾	I_{PDL} CC	-	-	130	μA	V_{IH} ; AL or TTL
		30	-	-	μA	V_{IL} ; AL
		28	-	-	μA	V_{IL} ; TTL

电气规格 5 V / 3.3 V 可切换焊盘

表 3-13 S 类 5V (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current	$I_{OZ\ CC}$	-150	-	150	nA	$T_J \leq 150^\circ\text{C}$; else
		-300	-	300	nA	$T_J \leq 150^\circ\text{C}$; PDD option available, or AltRef option available and EDSADC channel connected
		-300	-	300	nA	$T_J \leq 170^\circ\text{C}$; else
		-600	-	600	nA	$T_J \leq 170^\circ\text{C}$; PDD option available, or AltRef option available and EDSADC channel connected
Input high voltage level	$V_{IH\ SR}$	$0.7 * V_{DDM}$	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	$V_{IL\ SR}$	-	-	$0.44 * V_{DDM}$	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	$V_{ILD\ SR}$	-50	-	50	mV	max. variation of 1ms; $V_{DDM} = \text{constant}$; AL
Pin capacitance	$C_{IO\ CC}$	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	$t_{SET\ CC}$	-	-	100	ns	

1) 实施滞回是为了避免亚稳态和由于内部地弹而引起的切换。不能保证它能抑制由于外部系统噪声而引起的切换。

2) 上拉电阻的值通过表 VADC 5V 中的参数 R_{MDU} 定义。

3) 下拉电阻的值通过表 VADC 5V 中的参数 R_{MDD} 定义。

表 3-14 S 类 3.3V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	$f_{IN\ CC}$	-	-	160	MHz	

电气规格 5 V / 3.3 V 可切换焊盘

表 3-14 S 类 3.3V (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input hysteresis ¹⁾	HYS_{CC}	$0.055 * V_{DDM}$	-	-	V	non of the neighbor pads are used as output; AL
		$0.09 * V_{DDM}$	-	-	V	non of the neighbor pads are used as output; TTL
		$0.065 * V_{DDM}$	-	-	V	non of the neighbor pads are used as output; TTL (degraded used for CIF)
		125	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current ²⁾	$I_{PUH_{CC}}$	17	-	-	μA	V_{IH} ; AL and TTL (degraded, used for CIF)
		11	-	-	μA	V_{IH} ; TTL
		-	-	80	μA	V_{IL}
Pull-down current ³⁾	$I_{PDL_{CC}}$	-	-	105	μA	V_{IH} ; AL and TTL (degraded, used for CIF)
		-	-	115	μA	V_{IH} ; TTL
		19	-	-	μA	V_{IL} ; AL and TTL
		15	-	-	μA	V_{IL} ; TTL (degraded, used for CIF)
Input leakage current	$I_{OZ_{CC}}$	-150	-	150	nA	$T_J \leq 150^\circ C$; else
		-300	-	300	nA	$T_J \leq 150^\circ C$; PDD option available, or AltRef option available and EDSADC channel connected
		-300	-	300	nA	$T_J \leq 170^\circ C$; else
		-600	-	600	nA	$T_J \leq 170^\circ C$; PDD option available
Input high voltage level	$V_{IH_{SR}}$	$0.7 * V_{DDM}$	-	-	V	AL
		2.0	-	-	V	TTL
		1.4	-	-	V	TTL (degraded, used for CIF)

电气规格 5 V / 3.3 V 可切换焊盘

表 3-14 S 类 3.3V (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage level	V_{IL} SR	-	-	0.42 * V_{DDM}	V	AL
		-	-	0.8	V	TTL
		-	-	0.5	V	TTL (degraded, used for CIF)
Input low threshold variation	V_{ILD} SR	-33	-	33	mV	max. variation of 1ms; V_{DDM} = constant; AL
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) 实施滞回是为了避免亚稳态和由于内部地弹而引起的切换。不能保证它能抑制由于外部系统噪声而引起的切换。

2) 上拉电阻的值通过表 VADC 5V 中的参数 R_{MDU} 定义。

3) 下拉电阻的值通过表 VADC 5V 中的参数 R_{MDD} 定义。

表 3-15 D 类

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current	I_{OZ} CC	-150	-	150	nA	$T_J \leq 150^\circ\text{C}$; else
		-300 ¹⁾	-	300 ¹⁾	nA	$T_J \leq 150^\circ\text{C}$; PDD option available, or AltRef option available and EDSADC channel connected
		-300	-	300	nA	$T_J \leq 170^\circ\text{C}$; else
		-600 ²⁾	-	600 ²⁾	nA	$T_J \leq 170^\circ\text{C}$; PDD option available, or AltRef option available and EDSADC channel connected
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added

1) 对于 AN11, 需要添加 100 nA。

2) 对于 AN11, 需要添加 200 nA。

电气规格 5 V / 3.3 V 可切换焊盘

表 3-16 ADC 基准焊盘

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current for V_{AREF}	$I_{OZZ\ CC}$	-1	-	1	μA	$T_J \leq 150^\circ C$; $V_{AREF} < V_{DDM}$; used for EVADC
		-2	-	2	μA	$T_J \leq 170^\circ C$; $V_{AREF} < V_{DDM}$; used for EVADC
		-3.5	-	3.5	μA	$T_J \leq 150^\circ C$; $V_{AREF} \leq V_{DDM} + 50mV$; used for EVADC
		-7	-	7	μA	$T_J \leq 170^\circ C$; $V_{AREF} \leq V_{DDM} + 50mV$; used for EVADC
		-2 ¹⁾	-	2 ¹⁾	μA	$T_J \leq 150^\circ C$; $V_{AREF} < V_{DDM}$; for EDSADC
		-4 ¹⁾	-	4 ¹⁾	μA	$T_J \leq 170^\circ C$; $V_{AREF} < V_{DDM}$; for EDSADC
		-6 ¹⁾	-	6 ¹⁾	μA	$T_J \leq 150^\circ C$; $V_{AREF} \leq V_{DDM} + 50mV$; for EDSADC
		-12 ¹⁾	-	12 ¹⁾	μA	$T_J \leq 170^\circ C$; $V_{AREF} \leq V_{DDM} + 50mV$; for EDSADC

1) 限制对 VAREF1 引脚有效。

表 3-17 慢速 Pad 的驱动器模式选择

PDx.2	PDx.1	PDx.0	Port Functionality	Driver Setting
X	X	0	Speed grade 1	medium sharp edge (sm)
X	X	1	Speed grade 2	medium medium edge (m)

表 3-18 Fast Pad 驱动器模式选择

PDx.2	PDx.1	PDx.0	Port Functionality	Driver Setting
X	0	0	Speed grade 1	Strong sharp edge (ss)
X	0	1	Speed grade 2	Strong medium edge (sm)
X	1	0	Speed grade 3	medium (m)
X	1	1	Speed grade 4	Reserved, do not use this combination

表 3-19 RFast Pad 驱动器模式选择

PDx.2	PDx.1	PDx.0	Port Functionality	Driver Setting
X	0	0	Speed grade 1	Strong sharp edge (ss)
X	0	1	Speed grade 2	Strong medium edge (sm)

电气规格 5 V / 3.3 V 可切换焊盘

表 3-19 RFast Pad 的驱动器模式选择 (续)

PDx.2	PDx.1	PDx.0	Port Functionality	Driver Setting
X	1	0	Speed grade 3	medium (m)
X	1	1	Speed grade 4	RGMII function active

电气规格 高性能 LVDS 焊盘

3.6 高性能 LVDS 焊盘

该 LVDS 焊盘类型用于新型 TC37x 的高速芯片到芯片通信接口。它由一个 LVDSH 焊盘和一个快速焊盘组成。

对于所有 LVDSH 参数， $C_L = 2.5 \text{ pF}$ 。

表 3-20 LVDS - IEEE 标准 LVDS 通用链路 (GPL)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output impedance	$R_{0 \text{ CC}}$	40	-	140	Ohm	$V_{cm} = 1.0 \text{ V}$ and 1.4 V
Rise time (20% - 80%)	$t_{rise20 \text{ CC}}$	-	-	$0.75^{1)}$	ns	$Z_L = 100 \text{ Ohm} \pm 20\%$ @2pF external load
Fall time (20% - 80%)	$t_{fall20 \text{ CC}}$	-	-	$0.75^{2)}$	ns	$Z_L = 100 \text{ Ohm} \pm 20\%$ @2pF external load
Output differential voltage ³⁾	$V_{OD \text{ CC}}$	240	-	330	mV	$R_T = 100 \text{ Ohm} \pm 1\%$; LPCRx.VDIFFADJ=00
		280	-	370	mV	$R_T = 100 \text{ Ohm} \pm 1\%$; LPCRx.VDIFFADJ=01
		320	-	410	mV	$R_T = 100 \text{ Ohm} \pm 1\%$; LPCRx.VDIFFADJ=10
		380	-	500	mV	$R_T = 100 \text{ Ohm} \pm 1\%$; LPCRx.VDIFFADJ=11 ; Multi slave operation
Output voltage high	$V_{OH \text{ CC}}$	-	-	1475	mV	$R_T = 100 \text{ Ohm} \pm 1\%$ VDIFFADJ=00 and 01
		-	-	1500	mV	$R_T = 100 \text{ Ohm} \pm 1\%$ VDIFFADJ=10 and 11
Output voltage low	$V_{OL \text{ CC}}$	925	-	-	mV	$R_T = 100 \text{ Ohm} \pm 1\%$ VDIFFADJ=00 and 01
		900	-	-	mV	$R_T = 100 \text{ Ohm} \pm 1\%$ VDIFFADJ=10 and 11
Output offset (Common mode) voltage	$V_{OS \text{ CC}}$	1125	-	1275	mV	$R_T = 100 \text{ Ohm} \pm 1\%$
Input voltage range	$V_{I \text{ SR}}$	0	-	1600	mV	Driver ground potential difference < 925 mV; $R_T = 100 \text{ Ohm} \pm 10\%$
		0	-	2400	mV	Driver ground potential difference < 925 mV; $R_T = 100 \text{ Ohm} \pm 20\%$
Input differential threshold	$V_{idth \text{ SR}}$	-100	-	100	mV	Driver ground potential difference < 900 mV; VDIFFADJ=10 and 11
		-100	-	100	mV	Driver ground potential difference < 925 mV; VDIFFADJ=00 and 01

电气规格 高性能 LVDS 焊盘

表 3-20 LVDS - IEEE 标准 LVDS 通用链路 (GPL) (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Receiver differential input impedance	R_{in} CC	80	-	120	Ohm	$V_I \leq 2400$ mV
Output differential voltage Sleep Mode ⁴⁾	V_{ODSM} CC	-5	-	20	mV	$R_T = 100$ Ohm $\pm 20\%$; LPCRx.VDIFFADJ=xx
Delta output impedance	$dR0$ SR	-	-	10	%	$V_{cm} = 1.0$ V and 1.4 V
Change in VOS between 0 and 1	$dVOS$ CC	-	-	25	mV	$R_T = 100$ Ohm $\pm 1\%$
Change in Vod between 0 and 1	$dVod$ CC	-	-	25	mV	$R_T = 100$ Ohm $\pm 1\%$
Pad set-up time	t_{SET_LVDS} CC	-	10	13	μ s	
Duty cycle	t_{duty} CC	45	-	55	%	

1) $t_{rise20} = 0.75ns + (C_L - 2)[pF] * 20ps$, C_L 定义外部负载。

2) $t_{fall20} = 0.75ns + (C_L - 2)[pF] * 20ps$, C_L 定义外部负载。

3) 潜在的对IEEE Std 1596.3 的违反是为了新的多从站支持的特点，为符合 IEEE Std 1596.3，LPCRx.VDIFFADJ 必须配置为 01。

4) Tx的共模电压得以维持。

注释：驱动器接地电位的差异定义为驱动器-接收器电位差，在比较驱动器输出电压电平和接收器输入传输信号的电压电平时，可能会导致电压偏移。

注释：表“LVDS-IEEE 标准LVDS通用链路 (GPL)”中， R_T 表示接收端的终端电阻，其定义参考IEEE Std 1596.3-1996 图3-5并在图3-1中表示为 R_{IN} 或 $R_T=100$ Ohm 值，但不能同时按两者计算。

启动后默认=CMOS功能

电气规格 高性能 LVDS 焊盘

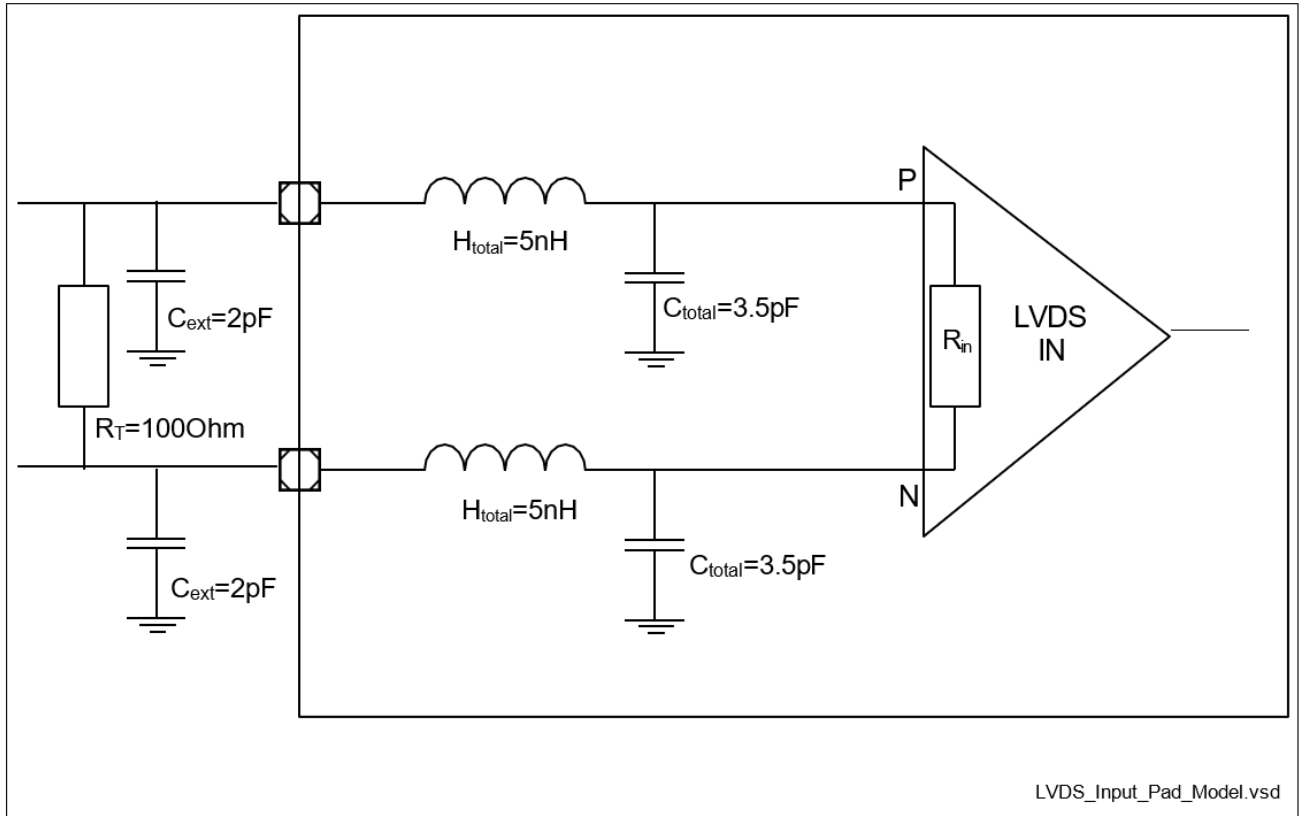


图 3-1 LVDS焊盘输入模型

电气规格 VADC 参数

3.7 VADC 参数

转换器结果的准确性取决于基准电压范围。下表中的参数适用于 ($V_{AREF} - V_{AGND}$) ≥ 4.5 V 的基准电压范围。如果基准电压范围低于 4.5 V k 倍 (例如 3.3 V)，则精度参数将增加 1.1/k 倍 (例如 $1.1 \times 4.5 / 3.3 = 1.5$)。

电压供应上的噪声会影响转换。精度参数定义为供电电压纹波在 10 MHz 以内低于 20 mVpp (在 10 MHz 以上低于 5 mVpp)。

数字功能与模拟输入重叠会影响准确性。

总计不可调整误差/总不可调整误差 (TUE) 的定义是无噪音的。总体偏差取决于 TUE 和 EN_{RMS} (取决于噪声分布)。示例：对于 4 sigma 的噪声分布且 $EN_{RMS} = 1.0$ ，附加峰峰值噪声误差为 8 最低有效位。

快速比较操作以 10 位值执行。

降噪功能通过增加额外的转换步骤来改善结果。因此，转换时间也相应增加 (对于 1、3 或 7 个步骤，每个步骤的转换时间分别为 $4 \times t_{ADCI} + 3 \times t_{ADC}$)。

表 3-21 VADC 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
EVADC IVR output voltage	$V_{DDK\ CC}$	1.15	-	1.35	V	Measured at low temperature.
Deviation of IVR output voltage V_{DDK}	$dV_{DDK\ CC}$	-2	-	2	%	Based on device-specific value
Analog reference voltage ¹⁾	$V_{AREF\ SR}$	4.5	5.0	$V_{DDM} + 0.05$	V	$4.5\ V \leq V_{DDM} \leq 5.5\ V$
		2.97	3.3	$V_{DDM} + 0.05$	V	$2.97\ V \leq V_{DDM} < 4.5\ V$
Analog reference ground	$V_{AGND\ SR}$	V_{SSM}	V_{SSM}	V_{SSM}	V	V_{SSM} and V_{AGND} are connected together
Analog input voltage range	$V_{AIN\ SR}$	V_{AGND}	-	V_{AREF}	V	V_{AIN} is limited by the respective pad supply voltage; see pin configuration (buffer type)
Converter reference clock	$f_{ADCI\ SR}$	16	40	53.33	MHz	$4.5\ V \leq V_{DDM} \leq 5.5\ V$
		16	20	26.67	MHz	$2.97\ V \leq V_{DDM} < 4.5\ V$
Total Unadjusted Error ^{2) 3)}	$TUE\ CC$	-4	-	4	LSB	12-bit resolution for primary/secondary groups, 10-bit resolution for fast compare channels
INL Error ²⁾	$EA_{INL\ CC}$	-3	-	3	LSB	
DNL error ^{2) 4)}	$EA_{DNL\ CC}$	-1	-	3	LSB	
Gain Error ²⁾	$EA_{GAIN\ CC}$	-3.5	-	3.5	LSB	
Offset Error ^{2) 3)}	$EA_{OFF\ CC}$	-4	-	4	LSB	
RMS Noise ^{2) 5) 6)}	$EN_{RMS\ CC}$	-	0.5	0.8	LSB	Noise reduction level 3
		-	0.5	1.0	LSB	Standard conversion

电气规格 VADC 参数

表 3-21 VADC 5V (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reference input charge consumption per conversion (from V_{AREF}) ^{7) 8) 9)}	$Q_{CONV\ CC}$	-	-	20	pC	$V_{AIN} = 0\text{ V}$ (worst case), precharging disabled
		-	-	10	pC	$V_{AIN} = 0\text{ V}$ (worst case), precharging enabled, $V_{DDM} - 5\% < V_{AREF} < V_{DDM} + 50\text{ mV}$
Switched capacitance of an analog input	$C_{AINS\ CC}$	-	2.5	3.4	pF	Input buffer disabled
Analog input charge consumption ¹⁰⁾	$Q_{AINS\ CC}$	-	-	3.5	pC	Primary groups and fast compare channels; $V_{AIN} = V_{AREF}$; $V_{DDM} = 5.0\text{ V}$; input buffer enabled; $T_J \leq 150^\circ\text{C}$
		-	-	3.8	pC	Primary groups and fast compare channels; $V_{AIN} = V_{AREF}$; $V_{DDM} = 5.0\text{ V}$; input buffer enabled; $T_J > 150^\circ\text{C}$
		-	-	4.4	pC	Secondary groups; $V_{AIN} = V_{AREF}$; $V_{DDM} = 5.0\text{ V}$; input buffer enabled; $T_J \leq 150^\circ\text{C}$
		-	-	4.8	pC	Secondary groups; $V_{AIN} = V_{AREF}$; $V_{DDM} = 5.0\text{ V}$; input buffer enabled; $T_J > 150^\circ\text{C}$

电气规格 VADC 参数

表 3-21 VADC 5V (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Sampling time	$t_{\text{S SR}}$	100	-	-	ns	Primary group or fast compare channel, $4.5 \text{ V} \leq V_{\text{DDM}} \leq 5.5 \text{ V}$; input buffer disabled
		300	-	-	ns	Primary group or fast compare channel, $4.5 \text{ V} \leq V_{\text{DDM}} \leq 5.5 \text{ V}$; input buffer enabled
		500	-	-	ns	Secondary group, $4.5 \text{ V} \leq V_{\text{DDM}} \leq 5.5 \text{ V}$; input buffer disabled
		700	-	-	ns	Secondary group, $4.5 \text{ V} \leq V_{\text{DDM}} \leq 5.5 \text{ V}$; input buffer enabled
		200	-	-	ns	Primary Group or fast compare channel, $2.97 \text{ V} \leq V_{\text{DDM}} < 4.5 \text{ V}$; input buffer disabled
		400	-	-	ns	Primary group or fast compare channel, $2.97 \text{ V} \leq V_{\text{DDM}} < 4.5 \text{ V}$; input buffer enabled
		1000	-	-	ns	Secondary group, $2.97 \text{ V} \leq V_{\text{DDM}} < 4.5 \text{ V}$; input buffer disabled
		1200	-	-	ns	Secondary group, $2.97 \text{ V} \leq V_{\text{DDM}} < 4.5 \text{ V}$; input buffer enabled
Sampling time for calibration	$t_{\text{SCAL SR}}$	50	-	-	ns	$4.5 \text{ V} \leq V_{\text{DDM}} \leq 5.5 \text{ V}$
		100	-	-	ns	$2.97 \text{ V} \leq V_{\text{DDM}} < 4.5 \text{ V}$
Input buffer switch-on time	$t_{\text{BUF CC}}$	-	0.4	1	μs	
Wakeup time	$t_{\text{WU CC}}$	-	0.1	0.2	μs	Fast standby mode
		-	1.6	3	μs	Slow standby mode
Broken wire detection delay against V_{AREF}	$t_{\text{BWR CC}}$	-	100	-	cycles	Result above 80% of full scale range, analog input buffer disabled
Broken wire detection delay against V_{AGND}	$t_{\text{BWG CC}}$	-	100	-	cycles	Result below 10% of full scale range, analog input buffer disabled
Converter diagnostics unit resistance ¹¹⁾	$R_{\text{CSD CC}}$	45	-	75	kOhm	
Converter diagnostics voltage accuracy	$dV_{\text{CSD CC}}$	-10	-	10	%	Percentage refers to V_{DDM}

电气规格 VADC 参数

表 3-21 VADC 5V (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Resistance of the multiplexer diagnostics pull-up device	$R_{MDU\ CC}$	30	-	42	kOhm	$0\text{ V} \leq V_{IN} \leq 0.9 \cdot V_{DDM}$, Automotive Levels
		56	-	78	kOhm	$0\text{ V} \leq V_{IN} \leq 0.9 \cdot V_{DDM}$, TTL Levels
Resistance of the multiplexer diagnostics pull-down device	$R_{MDD\ CC}$	43	-	58	kOhm	$0.1 \cdot V_{DDM} \leq V_{IN} \leq V_{DDM}$, Automotive level
		18	-	25	kOhm	$0.1 \cdot V_{DDM} \leq V_{IN} \leq V_{DDM}$, TTL level
Resistance of the pull-down test device	$R_{PDD\ CC}$	-	-	0.3	kOhm	Measured at pad input voltage $V_{IN} = V_{DDM} / 2$.

- 1) 这些限制适用于标准基准输入以及备用基准输入。
- 2) 该参数取决于基准电压范围和电源纹波，请参阅简介。
最坏情况下的组合误差是 TUE 和 EN_{RMS} 的算术组合。
测试是在完成启动校准后禁用后校准的情况下进行的。
- 3) 映射到 SLOW 类型焊盘的模拟输入会影响精度。此参数的值以 3 LSB₁₂ 为单位递增。
- 4) 单调性特性，校准时不会漏码。
- 5) 参数 EN_{RMS} 指的是 1 sigma 分布。
- 6) 映射到 SLOW 类型焊盘的模拟输入 RMS 噪声 (EN_{RMS}) 最高可达 2 LSB₁₂ (启用 DC/DC 软开关)。
- 7) 对于降低的参考电压 $V_{AREF} < 3.375\text{ V}$ ，消耗的电荷 QCONV 会减少 $k2 = V_{AREF} [\text{V}] / 3.375$ 。对于降低的参考电压 $4.5\text{ V} < V_{AREF} \leq 3.375\text{ V}$ ，QCONV 不会降低。
- 8) 当 BWD (断线检测) 处于活动状态时，最大电荷增加 15 pC。
- 9) 快速比较通道仅消耗主/次组电荷的 1/3。
- 10) 对于具有叠加数字 GPIO 或 PDD 功能的模拟输入，该值增加 1 pC。
- 11) 使用至少 1.1 μs 的采样时间以确保测试电压正确稳定。

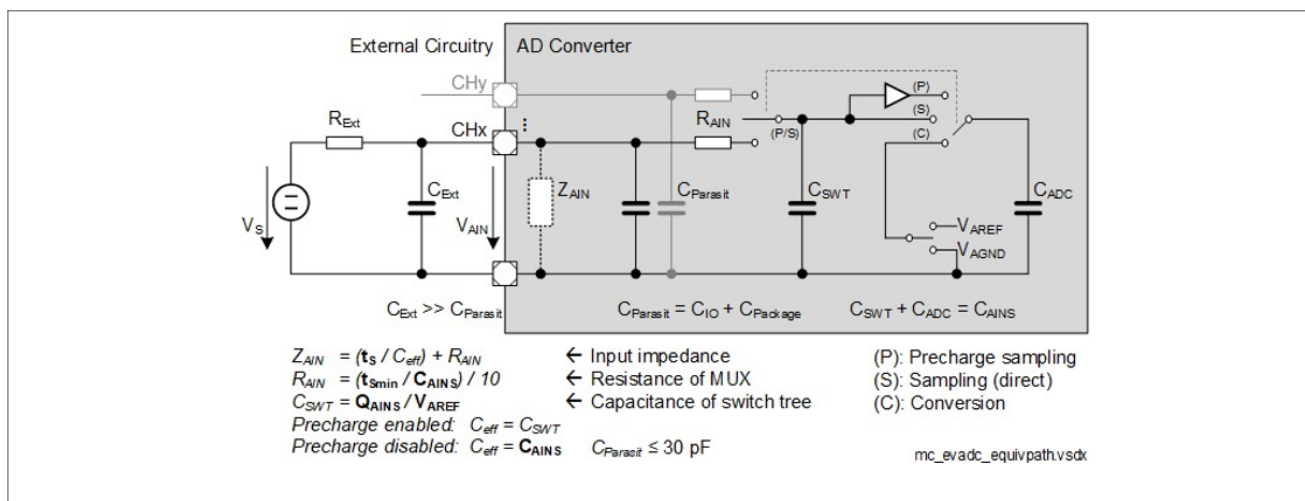


图 3-2 模拟输入等效电路

电气规格 DSADC 参数

3.8 DSADC 参数

DSADC 参数仅对电压范围 $4.5\text{ V} \leq V_{\text{DDM}} \leq 5.5\text{ V}$ 有效。

这些参数描述产品特性，不包括外部电路。如无明确定义，这些值适用于结温 $T_J \leq 150^\circ\text{C}$ 的情况。

校准针对增益因子 1 和 2 指定，校准值参考这些设置。

信噪比 (SNR) 针对差分输入进行指定。对于单端工作模式，信噪比会降低 6 dB。对于准差分模式（即使用 V_{CM} ），当增益 = 2 时，信噪比会降低 3dB（当增益 = 1 时，信噪比会降低 6dB）。

表 3-22 DSADC 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Common mode voltage bias resistance	$R_{\text{BIAS CC}}$	105	130	155	kOhm	On-chip variation $\leq \pm 2.5\%$.
Positive reference voltage	$V_{\text{AREF SR}}$	4.5	-	$V_{\text{DDM}} + 0.05$	V	
Reference ground voltage	$V_{\text{AGND SR}}$	V_{SSM}	-	V_{SSM}	V	V_{SSM} and V_{AGND} are connected together
Reference load current	$I_{\text{REF CC}}$	-	10	12	μA	Per modulator
		-	-	14	μA	Per modulator, $T_J > 150^\circ\text{C}$
Common mode voltage accuracy ¹⁾	$dV_{\text{CM CC}}$	-100	-	100	mV	Deviation from selected voltage
Analog input voltage range	$V_{\text{DSIN SR}}$	V_{SSM}	-	$2 * V_{\text{DDM}}$	V	Differential; $V_{\text{DSXP}} - V_{\text{DSXN}}$
		V_{SSM}	-	V_{DDM}	V	Single ended
Input current ²⁾	$I_{\text{RMS CC}}$	7	10	13	μA	Exact value ($\pm 1\%$) available in UCB; valid for gain = 1 and $f_{\text{MOD}} = 26.7\text{ MHz}$
On-chip modulator clock frequency	$f_{\text{MOD SR}}$	16	-	40	MHz	
Gain error ^{3) 4)}	$ED_{\text{GAIN CC}}$	-0.2 ⁵⁾	$\pm 0.1^{5)}$	0.2 ⁵⁾	%	$T_J \leq 150^\circ\text{C}$; Target, calibrated, V_{AREF} constant after calibration; $f_{\text{MOD}} = 26.67\text{ MHz}$
		-	± 0.25	-	%	$T_J > 150^\circ\text{C}$; V_{AREF} constant after calibration; $f_{\text{MOD}} = 26.67\text{ MHz}$
		-1	-	1	%	Calibrated once; $f_{\text{MOD}} = 26.67\text{ MHz}$
		-2.5	-	2.5	%	Uncalibrated; $f_{\text{MOD}} = 26.67\text{ MHz}$

电气规格 DSADC 参数

表 3-22 DSADC 5V (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DC offset error ³⁾	$ED_{OFF\ CC}$	-5 ⁵⁾	-	5 ⁵⁾	mV	Calibrated; $f_{MOD} = 26.67\text{ MHz}$
		-10	-	10	mV	Calibrated once; $f_{MOD} = 26.67\text{ MHz}$
		-30	-	30	mV	Uncalibrated; $f_{MOD} = 26.67\text{ MHz}$
Signal-Noise Ratio for differential input signals ^{2) 6) 7)}	$SNR\ CC$	80	-	-	dB	$T_J \leq 150^\circ\text{C}$; $f_{PB} = 30\text{ kHz}$; $f_{MOD} = 26.67\text{ MHz}$
		78	-	-	dB	$T_J \leq 150^\circ\text{C}$; $f_{PB} = 50\text{ kHz}$; $f_{MOD} = 26.67\text{ MHz}$
		74	-	-	dB	$T_J \leq 150^\circ\text{C}$; $f_{PB} = 100\text{ kHz}$; $f_{MOD} = 26.67\text{ MHz}$
Signal-Noise Ratio degradation	$DSNR\ CC$	-	-	3	dB	$T_J > 150^\circ\text{C}$; Resulting Signal-Noise Ratio value is SNR - DSNR
Spurious-free dynamic range ³⁾	$SFDR\ CC$	60	-	-	dB	$f_{MOD} = 26.67\text{ MHz}$
Output sampling rate	$f_D\ CC$	3.906	-	300	kHz	16 MHz / 4096, without integrator
Pass band	$f_{PB}\ CC$	1.302	-	100	kHz	Output data rate: $f_D = f_{PB} \cdot 3$; without integrator
		1.302	-	10	kHz	Output data rate: $f_D = f_{PB} \cdot 6$; without integrator
Pass band ripple	$df_{PB}\ CC$	-0.08	-	0.08	dB	FIR filters enabled
Stop band attenuation	$SBA\ CC$	40	-	-	dB	$0.5f_D \dots 1.0f_D$
		45	-	-	dB	$1.0f_D \dots 1.5f_D$
		50	-	-	dB	$1.5f_D \dots 2.0f_D$
		55	-	-	dB	$2.0f_D \dots 2.5f_D$
		60	-	-	dB	$2.5f_D \dots OSR/2f_D$
DC compensation factor	$DCF\ CC$	-3	-	-	dB	$10^{-5}f_D$, offset compensation filter enabled (FCFGMx.OCEN = 001 _B)
Modulator settling time	$t_{MSET}\ CC$	-	-	20	μs	After switching on, voltage regulator already running

1) 在具有叠加 GPIO 功能的引脚上, 由于 $T_J > 150^\circ\text{C}$ 时的漏电流, 最大限值最多增加 25 mV。

2) 有关详细信息, 请参阅用户手册章节。

3) 此参数在 f_{MOD} 定义的范围内有效。

4) 如果采用相同的校准策略, 不同 EDSADC 通道之间的增益不匹配误差在 $\pm 0.5\%$ 以内

电气规格 DSADC 参数

- 5) 如果温度变化 $>20^{\circ}\text{C}$ ，则需要重新校准
- 6) 这些值对于模拟增益因子 1 有效，每增加一个增益因子，减去 3 dB。
- 7) 对于单端输入信号和增益1，SNR降低6 dB。

电气规格 MHz 振荡器

3.9 MHz 振荡器

OSC_XTAL 用作精确的时钟源。OSC_XTAL 支持 16 MHz 至 40 MHz 外部晶振。还支持陶瓷谐振器。

表 3-23 OSC_XTAL

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current at XTAL1	I_{IX1} CC	-70	-	70	μA	$V_{IN} > 0V$; $V_{IN} < V_{EXT}$
Oscillator frequency	f_{OSC} SR	4	-	40	MHz	Direct Input Mode selected, if shaper is not bypassed
		16	-	40	MHz	External Crystal Mode selected
Oscillator start-up time	t_{OSCS} CC	-	-	3 ¹⁾	ms	20MHz $\leq f_{OSC}$ and 8pF load capacitance
Input voltage at XTAL1 ²⁾	V_{IX} SR	-0.7	-	$V_{EXT} + 0.5$	V	If shaper is not bypassed
Input amplitude (peak to peak) at XTAL1	V_{PPX} SR	$0.3 * V_{EXT}$	-	$V_{EXT} + 1.0$	V	If shaper is not bypassed; $f_{OSC} > 25\text{MHz}$
		$0.35 * V_{EXT}$	-	$V_{EXT} + 1.0$	V	If shaper is not bypassed; $f_{OSC} \leq 25\text{MHz}$
Internal load capacitor	C_{L0} CC	1.30	1.40	1.55	pF	enabled via bit OSCCON.CAP0EN
Internal load capacitor	C_{L1} CC	3.05	3.35	3.70	pF	enabled via bit OSCCON.CAP1EN
Internal load capacitor	C_{L2} CC	7.85	8.70	9.55	pF	enabled via bit OSCCON.CAP2EN
Internal load capacitor	C_{L3} CC	12.05	13.35	14.65	pF	enabled via bit OSCCON.CAP3EN
Internal load stray capacitor between XTAL1 and XTAL2	C_{XINTS} CC	1.15	1.20	1.25	pF	
Internal load stray capacitor between XTAL1 and ground	C_{XTAL1} CC	-	2.5	4	pF	
Duty cycle at XTAL1 ³⁾	DC_{X1} SR	35	-	65	%	$V_{XTAL1} = 0.5 * V_{PPX}$
Absolute RMS jitter at XTAL1 ³⁾	J_{ABSX1} SR	-	-	28	ps	10 KHz to $f_{OSC}/2$
Slew rate at XTAL1 ³⁾	SR_{XTAL1} SR	0.3	-	-	V/ns	Maximum 30% difference between rising and falling slew rate

1) t_{OSCS} 定义为从振荡器模式设置为外部晶体模式的时刻开始，直到振荡在 XTAL1 处达到 $0.3 * V_{EXT}$ 的幅度。

该值取决于所用外部晶体的频率。对于更快的晶振频率，该值会减小。

2) 对于电源 ($V_{EXT} < 5.3V$ V_{IX})，最低可低至 -0.9V。对于 XTAL1，低至 -0.9V 的输入电平不会对使用外部晶振的器件造成损坏或可靠性问题。

电气规格 MHz 振荡器

3) XTAL1 的方波输入信号。

注释：强烈建议测量最终目标系统（布局）中的振荡裕度（负阻），以确定振荡器运行的最佳参数。请参考晶体或陶瓷谐振器供应商指定的限制。

电气规格备用时钟

3.10 备用时钟

备用时钟提供了替代时钟源。

表 3-24 备用时钟

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Back-up clock accuracy before trimming	$f_{\text{BACKUT}}^{\text{CC}}$	70	100	130	MHz	$V_{\text{EXT}} \geq 2.97V$
Back-up clock accuracy after trimming ¹⁾	$f_{\text{BACKT}}^{\text{CC}}$	98	100	102	MHz	$V_{\text{EXT}} \geq 2.97V$
Standby clock	$f_{\text{SB}}^{\text{CC}}$	25	70	110	kHz	$V_{\text{EXT}} \geq 2.97V$

1) 通过每 2 毫秒定期调整温度和电压漂移，可以实现短期调整，从而满足 LIN 通信所需的精度，最高温度可达 125 摄氏度

电气规格温度传感器

3.11 温度传感器

表3-25 DTS PMS

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time for each conversion ¹⁾	t_M CC	-	-	2.7	ms	Measured from cold power-on reset release
Calibration reference accuracy	T_{CALACC} CC	-1	-	1	°C	calibration points @ $T_J = -40^{\circ}\text{C}$ and $T_J = 127^{\circ}\text{C}$
Accuracy over temperature range	T_{NL} CC	-2	-	2	°C	T_{CALACC} has to be added in addition
DTS temperature range	T_{SR} SR	-40	-	170	°C	

1) 热复位后, t_M 不会重新启动, 而是从上次转换开始测量。

表 3-26 DTS 核心

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time for each conversion ¹⁾	t_M CC	-	-	2.7	ms	Measured from cold power-on reset release
Temperature difference between on chip temperature sensors	ΔT CC	-3	-	3	°C	
Calibration reference accuracy	T_{CALACC} CC	-2	-	2	°C	calibration points @ $T_J = -40^{\circ}\text{C}$ and $T_J = 127^{\circ}\text{C}$
Accuracy over temperature range	T_{NL} CC	-2	-	2	°C	T_{CALACC} has to be added in addition
DTS temperature range	T_{SR} SR	-40	-	170	°C	

1) 热复位后, t_M 不会重新启动, 而是从上次转换开始测量。

3.12 电源电流

下面定义的总电源电流由漏电流和开关分量组成。

应用相关值通常低于下表给出的值，并且取决于客户的系统运行条件（例如热连接或使用的应用配置）。

下表中参数的运行条件为：

实际（现实）功率模式定义了以下条件：

- $T_J = 150\text{ }^{\circ}\text{C}$
- $f_{SRI} = f_{CPUX} = 300\text{ MHz}$
- $f_{GTM} = 200\text{ MHz}$
- $f_{SPB} = f_{STM} = f_{BAUD1} = f_{BAUD2} = f_{ASCLINX} = 100\text{ MHz}$
- $V_{DD} = 1.275\text{ V}$
- $V_{DDP3} / \text{FLEX} = 3.366\text{ V}$
- $V_{EXT} / \text{EVRSB} = V_{DDM} = 5.1\text{ V}$
- 所有核心都激活，包括两个锁步核（IPC=0.6）
- 以下外设处于非活动状态：HSM、HSCT、GETH、以太网、PSI5、I2C、FCE 和 MTU

最大功率模式定义了以下条件：

- $T_J = 150\text{ }^{\circ}\text{C}$
- $f_{SRI} = f_{CPUX} = 300\text{ MHz}$
- $f_{GTM} = 200\text{ MHz}$
- $f_{SPB} = f_{STM} = f_{BAUD1} = f_{BAUD2} = f_{ASCLINX} = 100\text{ MHz}$
- $V_{DD} = 1.375\text{ V}$
- $V_{DDP3} / \text{FLEX} = 3.63\text{ V}$
- $V_{EXT} / \text{EVRSB} = V_{DDM} = 5.5\text{ V}$
- 所有核心都激活，包括三个锁步核心（IPC=1.2）
- 以下模块处于非活动状态：GETH、FCE和 MTU

电气规格电源电流

表 3-27 消耗电流

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Σ Sum of I_{DD} core and peripheral supply currents (incl. $I_{DDPORST} + \Sigma I_{DDCX0} + \Sigma I_{DDCXx} + I_{DDGTM} + I_{DDSB}$)	$I_{DDRAIL\ CC}$	-	-	775	mA	max power pattern; valid for Feature Package T, and TP products
		-	-	960 ¹⁾	mA	max power pattern; valid for Feature Package TE, and TX products
		-	-	630	mA	real power pattern; valid for Feature Package T, and TP products
		-	-	775	mA	real power pattern; valid for Feature Package TE, and TX products
I_{DD} core current during active power-on reset (PORST pin held low). Leakage current of core domain. ²⁾	$I_{DDPORST\ CC}$	-	-	190	mA	$V_{DD} = 1.275V$; $T_J = 125^\circ C$; valid for Feature Package TE, and TX products
		-	-	132	mA	$V_{DD} = 1.275V$; $T_J = 125^\circ C$; valid for Feature Package T, and TP products
		-	-	220	mA	$V_{DD} = 1.275V$; $T_J = 150^\circ C$; valid for Feature Package T, and TP products
		-	-	315	mA	$V_{DD} = 1.275V$; $T_J = 165^\circ C$; valid for Feature Package T, and TP products
		-	-	315	mA	$V_{DD} = 1.275V$; $T_J = 150^\circ C$; valid for Feature Package TE, and TX products
		-	-	425	mA	$V_{DD} = 1.275V$; $T_J = 165^\circ C$; valid for Feature Package TE, and TX products

电气规格电源电流

表 3-27 消耗电流 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Σ Sum of I_{DDP3} 3.3 V supply currents	$I_{DDP3RAIL}$ CC	-	-	45 ²⁾	mA	max power pattern incl. Flash read current and Dflash programming current.
		-	-	36 ³⁾	mA	real power pattern incl. Flash read current and Dflash programming current.
Σ Sum of external I_{EXT} supply currents (incl. $I_{EXTFLEX} + I_{EVRSB} + I_{EXTLVDS}$)	$I_{EXTRAIL}$ CC	-	-	50	mA	max power pattern
		-	-	35 ⁴⁾	mA	real power pattern
I_{EXT} and I_{FLEX} supply current	$I_{EXTFLEX}$ CC	-	-	11 ^{5) 6)}	mA	real power pattern with port activity absent; PORST output inactive.
I_{EVRSB} supply current ²⁾	I_{EVRSB} CC	-	-	8.5	mA	real power pattern; PMS/EVR module current considered without SCR and Standby RAM during RUN mode.
Σ Sum of external I_{DDM} supply currents (incl. $I_{DDMEVADC} + I_{DDMEDSADC}$)	I_{DDM} CC	-	-	27	mA	real power pattern; sum of currents of EDSADC and EVADC modules
Σ Sum of all currents (incl. $I_{EXTRAIL} + I_{DDMRail} + I_{DDx3RAIL} + I_{DD}$)	I_{DDTOT} CC	-	-	728	mA	real power pattern; $T_J = 150^\circ\text{C}$; valid for Feature Package T, and TP products
		-	-	873	mA	real power pattern; $T_J = 150^\circ\text{C}$; valid for Feature Package TE, and TX products
		-	-	796	mA	real power pattern; $T_J = 160^\circ\text{C}$; valid for Feature Package T, and TP products
		-	-	1015	mA	real power pattern; $T_J = 160^\circ\text{C}$; valid for Feature Package TE, and TX products
Σ Sum of all currents with DC-DC EVRC regulator active ⁷⁾	$I_{DDTOTDC3}$ CC	-	-	430	mA	real power pattern; EVRC reset settings with 72% efficiency; $V_{EXT} = 3.3\text{V}$; $T_J = 150^\circ\text{C}$

电气规格电源电流

表 3-27 电流消耗 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Σ Sum of all currents with DC-DC EVRC regulator active ¹⁾	$I_{DDTOTDC5CC}$	-	-	320	mA	real power pattern; EVRC reset settings with 72% efficiency; $V_{EXT} = 5V$; $T_J = 150^\circ C$
Σ Sum of all currents (SLEEP mode) ²⁾	I_{SLEEP}^{CC}	-	-	25	mA	All CPUs in idle, All peripherals in sleep, $f_{SRI/SPB} = 1 MHz$ via LPDIV divider; $T_J = 25^\circ C$
Σ Sum of all currents (STANDBY mode) drawn at V_{EVRSB} supply pin ⁸⁾	$I_{STANDBY}^{CC}$	-	-	130 ⁹⁾	μA	32 kB Standby RAM block active. SCR inactive. Power to remaining domains switched off. $T_J = 25^\circ C$; $V_{EVRSB} = 5V$
Maximum power dissipation ¹⁰⁾	PD_{SR}	-	-	1600	mW	max power pattern; valid for Feature Package T, and TP products
		-	-	1855	mW	max power pattern; valid for Feature Package TE, and TX products
		-	-	1240	mW	real power pattern; valid for Feature Package T, and TP products
		-	-	1425	mW	real power pattern; valid for Feature Package TE, and TX products

- 1) 对于 QFP 封装的 TC37xED 仿真设备, 总 (IDDED + IDD) 电流需要限制为 700 mA。TC37xED 的最大 (IDDED + IDD) 电流仅在 BGA 封装中受支持。
- 2) 限值是根据实际功率模式 ($V_{DD} = 1.275V$) 定义的。对于最大功率模式, 限值必须乘以系数 1.22。
- 3) 实际的 Pflash 读取模式, Pflash 带宽利用率为 50%, 代码混合为 50% 的 0 和 50% 的 1。使用至少 100nF 的公共去耦电容 (V_{DDP3})。在 3.3V 电源下以突发模式连续进行 Dflash 编程, 并并行进行实际的 Pflash 读取访问。相应闪存模块的擦除电流小于 V_{DDP3} 引脚上的相应编程电流。编程和擦除闪存可能会产生高达 45 mA / 20 ns 的瞬态电流尖峰。由去耦电容器和缓冲电容器处理。此参数与外部电源尺寸有关, 与热无关。
- 4) 针对实际功率模式定义了限制。对于 ADAS 电源模式限制总和为 42mA。
- 5) 消耗电流仅包括最小的端口活动。
- 6) 针对实际功率模式定义了限制。对于 ADAS 功率模式限制必须乘以系数 0.7。
- 7) 从外部稳压器汲取的总电流是根据 72% EVRC SMPS 稳压器效率估算的。IDDTOTDCx 是使用缩放的核心电流 $[(IDD \times VDD)/(V_{in} \times Efficiency)]$ 根据 IDDTOT 计算得出的, 并构成所有其他轨电流和 IDDM。

电气规格电源电流

- 8) 同样的电流限制也适用于其他功率模式
- 9) Σ 运行模式下 VEVRSB 电源引脚上所有电流的总和小于 ($I_{EVRSB} + 4 \text{ mA}$ 待机 RAM 电流 + I_{SCRSB} (如果 SCR 处于活动状态))。
 Σ 建议在此引脚上至少使用 100 nF 去耦电容。32kB 待机 SRAM 对 $I_{STANDBY}$ 电流的使用不到 10uA。
- 10) 仅当所有电源均由外部供电且不包含 EVR33 和 EVRC 的功率损耗时, 这些值才有效。

表3-28 模块电流消耗

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
I_{DDP3} supply current for programming of a Pflash or Dflash bank ¹⁾	$I_{DDP3PROG}$ CC	-	-	25	mA	Pflash 3.3V programming current adder when using external 3.3V supply.
		-	-	9 ²⁾	mA	Pflash 3.3V programming current adder when using external 5V supply.
I_{EXT} supply current added by LVDS pads in LVDS mode ¹⁾	$I_{EXTLVDS}$ CC	-	-	16	mA	real power pattern; 4 pairs of LVDS pins active with transmit function
		-	-	9 ³⁾	mA	real power pattern; 6 pairs of LVDS pins active with receive function

电气规格电源电流

表 3-28 模块电流消耗 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Σ Sum of external I_{DDM} supply currents (incl. $I_{DDMEVADC} + I_{DDMEDSADC}$)	$I_{DDM\ CC}$	-	-	14	mA	real power pattern; current for EDSADC modules only and EVADC modules are inactive; 4 EDSADC channels active continuously.
		-	-	22 ⁴⁾	mA	max power pattern; current for EDSADC modules only and EVADC modules are inactive; all EDSADC channels active continuously.
		-	-	13 ⁵⁾	mA	real power pattern; current for EVADC modules only and EDSADC modules are inactive; 8 EVADC modules active.
		-	-	15 ⁶⁾	mA	max power pattern; current for EVADC modules only and EDSADC modules are inactive; all EVADC modules active.
I_{DDP3} supply current for erasing of a Pflash or Dflash bank	$I_{DDP3ERASE\ CC}$	-	-	25	mA	Pflash 3.3V erasing current adder when using external 3.3V supply
SCR 8-bit Standby Controller current incl. PMS in STANDBY Mode drawn at V_{EVRSB} supply pin	$I_{SCRSB\ CC}$	-	-	7 ⁷⁾	mA	SCR power pattern incl. PMS current consumption with fback clock active; $f_{SYS_SCR} = 20\text{MHz}$; $T_j = 150^\circ\text{C}$
		-	0.150	-	mA	SCR power pattern incl. PMS current consumption with fback inactive; $f_{SYS_SCR} = 70\text{kHz}$; $T_j = 25^\circ\text{C}$
SCR 8-bit Standby Controller CPU in IDLE mode ⁸⁾	$I_{SCRIDLE\ CC}$	-	-	3.5	mA	real power pattern. CPU set into idle mode.

电气规格电源电流

- 1) 同样的电流限制也适用于其他功率模式。
- 2) 在 5V 电压下对 Pflash 进行编程期间, VEXT 电源轨上会额外消耗 2 mA 电流。
- 3) 单个 LVDS 对的接收功能限制为 1.5mA ($t_{EXTLVDS}$)。
- 4) 单个 DS 通道实例消耗 4 mA。
- 5) 在具有 2 个 EVADC 的“ADAS 功率模式”下, EVADC 电流被限制为 3mA (I_{DDM})。
- 6) 单个 VADC 单元消耗 1.3 mA 的电流。
- 7) 如果激活了 SCR ADCOMP, 则需要考虑额外的 0.6 mA 加法器。
- 8) 限值是根据实际功率模式 ($V_{DD} = 1.275V$) 定义的。对于最大功率模式, 限值必须乘以系数 1.22。

表 3-29 模块核心电流消耗

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
I_{DD} core current of CPUx main core with CPUx lockstep core inactive	I_{DDCX0}^{CC}	-	-	72	mA	max power pattern; IPC=1.2
		-	-	48	mA	real power pattern; IPC=0.6
I_{DD} core current of CPUx main core with CPUx lockstep core active	I_{DDCXX}^{CC}	-	-	$I_{DDCX0} + 48$	mA	max power pattern; IPC=1.2
		-	-	$I_{DDCX0} + 37$	mA	real power pattern; IPC=0.6
I_{DD} core current added by GTM	I_{DDGTM}^{CC}	-	-	110	mA	max power pattern
		-	-	90	mA	real power pattern; TIMx, TOMx, ATOMx, MCSx active. 2 clusters at 20 MHz.
		-	-	50	mA	TIMx, TOMx active at 100MHz. ATOMx, MCSx, DPLL inactive. 2 clusters at 100 MHz.
I_{DD} core current added by HSM	I_{DDHSM}^{CC}	-	-	20 ¹⁾	mA	max power pattern; HSM running at 100MHz.
I_{DD} core current added by CIF	I_{DDCIF}^{CC}	-	-	48	mA	conditions t.b.d.
I_{DD} core dynamic current added by LBIST	I_{DDLBI}^{CC}	-	-	200 ²⁾	mA	LBIST Configuration A; $1.2V \leq V_{DD}$
I_{DD} core dynamic current added by MBIST	I_{DDMBI}^{CC}	-	-	225	mA	fMBIST = 300MHz; tMBIST < 6ms. MTU Ganging procedure for SRAM test and initialization; $V_{DD} = 1.375V$.

- 1) 电流消耗包括 AES 模块在内的基本 HSM 激活。
- 2) LBIST 可在启动阶段执行, 也可由应用软件触发。在 LBIST 执行时间 (t_{LBIST}) 内, 二次电压监控器处于非活动状态。在启动阶段, 外部提供的 V_{DD} 电压必须等于或大于 1.2V (V_{DD} 标称值 - 4%), 以确保静态准确性。如果 V_{DD} 由 EVRC 内部供电, 则 EVRC 会注意不要违反 V_{DD} 1.2V 静态欠压限制。

电气规格电源电流

3.12.1 计算 1.25 V 消耗电流

1.25 V 电源轨的电流消耗由两部分组成：

- 静态电流消耗
- 动态电流消耗

静态电流消耗与器件温度 T_J 相关，动态电流消耗取决于配置的时钟频率和执行的软件应用程序。需要将这两部分相加才能得到轨电流消耗。

(3.1)

$$I_0 = 3,974 \left[\frac{\text{mA}}{\text{C}} \right] \times e^{0,024 \times T_J[\text{C}]}$$

(3.2)

$$I_0 = 6,01 \left[\frac{\text{mA}}{\text{C}} \right] \times e^{0,024 \times T_J[\text{C}]}$$

公式 (3.1) 定义典型的静态电流消耗和**公式 (3.2)** 定义最大静态电流消耗。这两个函数均在 $V_{DD} = 1.275 \text{ V}$ 时有效。

3.13 电源基础结构和供电启动

3.13.1 供电上升和下降行为

电源轨的启动斜率应符合 SR（见表 3-33 供电斜坡）。

3.13.1.1 单电源模式 (a)

电气规格电源基础结构和电源启动

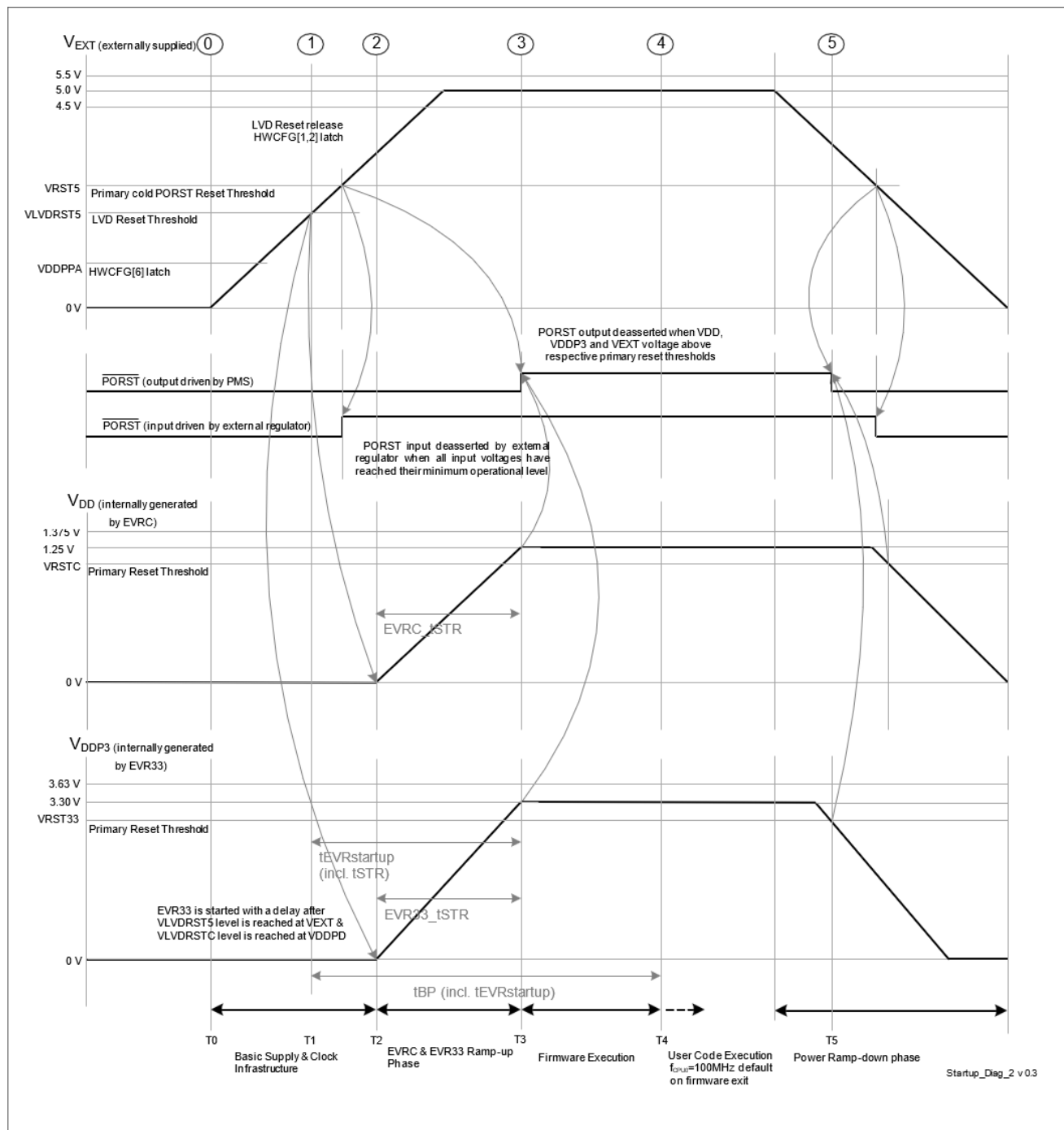


图 3-3 单电源模式 (a) - V_{EXT} (5V) 单电源

$V_{EXT} = 5V$ 单电源模式。 V_{DD} 和 V_{DDP3} 由内置的 EVRC 和 EVR33 稳压器从内部产生。

- 在基本基础设施和 EVRx 稳压器启动阶段 (T_0 至 T_2)，从外部稳压器 (dI_{EXT}/dt) 吸取电流的速率受到限制，最大为 100 mA，稳定时间为 100 μs 。电源轨的启动斜率应符合数据手册参数 SR。斜率定义为 0% 至 100% 电压电平之间的最大切向斜率。实际波形可能不同于规格书。

电气规格电源基础结构和电源启动

- 此外，还确保在固件启动阶段（T3 至 T4）从稳压器吸取的电流（ dI_{DD}/dt ）限制为最大 100 mA，稳定时间为 100 μ s。
- 当 PORST（输入）或 PORST（输出）激活/置位时，PORST 激活/置位。
- PORST（输入）有效意味着外部设备可通过将 PORST 引脚拉低，使复位保持有效。建议保持 PORST（输入）有效，直到外部电源电压高于相应的主复位阈值。
- PORST（输出）有效意味着 μ C 在内部发出复位信号并将 PORST 引脚驱动至低电平，从而将复位信号传播至外部设备。当三个电源域（VDD、VDDP3 或 VEXT）中至少有一个违反其主要欠压复位阈值时， μ C 会发出 PORST 置位（输出）信号。当所有电源均高于其主要复位阈值，且基本电源和时钟基础设施可用时， μ C 会发出 PORST 不置位（输出）信号。在 T3 复位释放期间，预计负载跳变高达 150 mA（ dI_{DD} ）。
- 电源序列如图 3-3 列举如下
 - T1 至 T2 是指外部电源上升时基本电源和时钟基础设施组件可用的时间段。带隙和内部时钟源启动，根据 HWCFG[2:1,4,5,6] 和 TESTMODE 引脚决定供电模式。T1 至 T2 是指外部电源上升时基本电源和时钟基础设施组件可用的时间段。带隙和内部时钟源启动，根据 HWCFG[2:1,6] 引脚决定供电模式。这些事件在 T1 时 LVD 复位释放后启动。当两个输入电压 VEXT 和 VEVR33 分别高于 VLVD RST5 和 VLVD RST33 电平时，LVD 复位被释放。内部预稳压器 VDDP3 输出电压高于 VLVD RST33 电平。
 - T2 指的是 EVRC 和 EVR33 稳压器软启动的时间点。PORST（输入）对 EVR33 或 EVRC 输出没有任何影响，尽管 PORST 已置位且器件处于复位状态，稳压器仍会继续产生相应的电压。产生的电压在 t_{STR} （数据手册参数）时间内呈软上升趋势，以避免过冲。
 - T3 指的是所有电源都高于其主要复位阈值（由 VRST5、VRST33 和 VRSTC 供电电压水平表示）的时间点。EVRC 和 EVR33 稳压器已经启动。
PORST（输出）不置位，并且 HWCFG[3:5] 引脚被 SCU 锁存在 PORST 上升沿。
固件执行已启动。T1 和 T3 之间的时间记录为 $t_{EVRstart}$ （数据手册参数）。
 - T4 指的是固件执行完成并且用户代码以 CPU0 的默认频率 100 MHz 开始执行的时间点。T0 和 T4 之间的时间记录为 t_{BP} （数据手册参数）。
 - T5 指的是斜坡下降阶段期间至少一个外部提供或生成的电源（VDD、VDDP3 或 VEXT）降至其各自的初级欠压复位阈值以下的时间点。

电气规格电源基础结构和电源启动

3.13.1.2 单电源模式 (e)

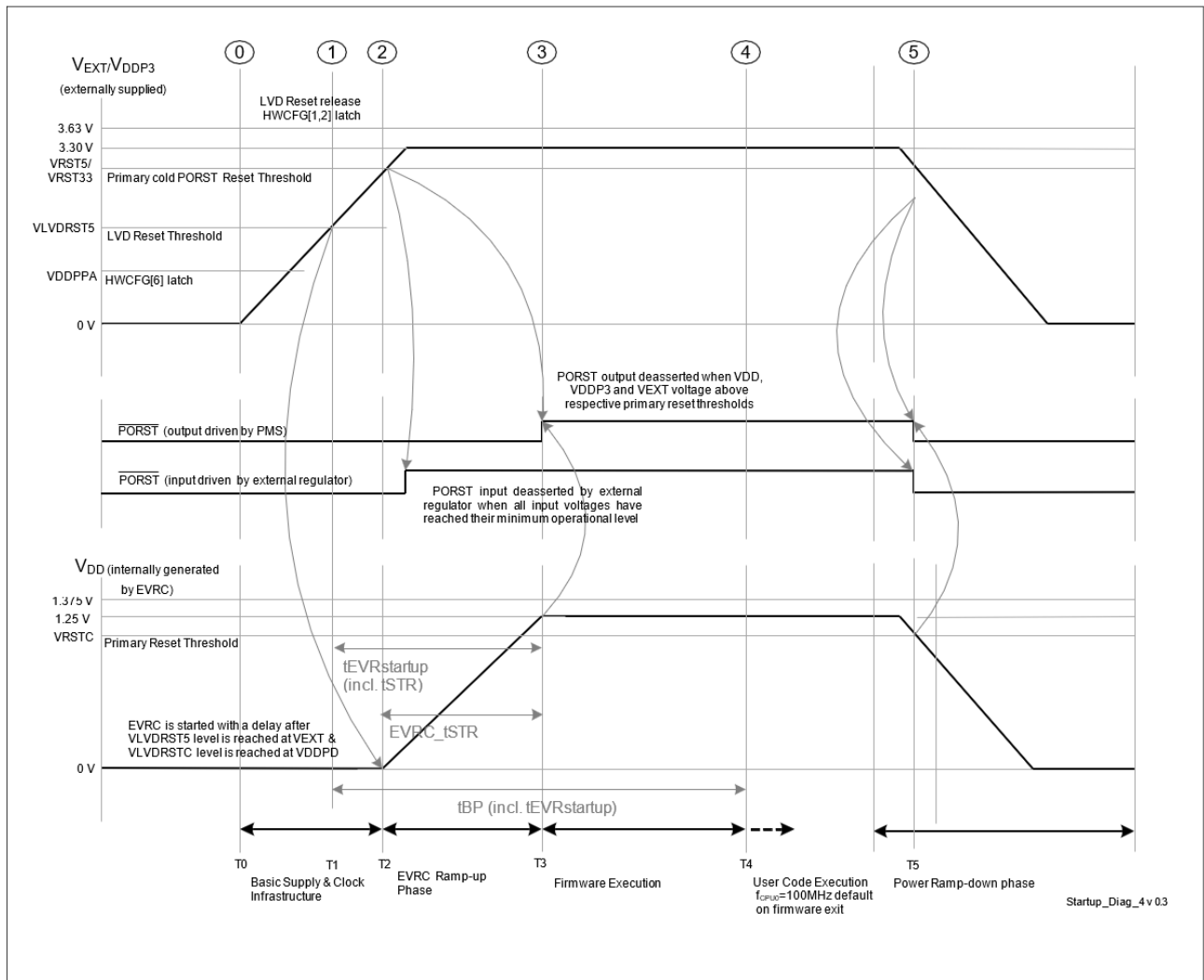


图 3-4 单电源模式 (e) - (V_{EXT} 和 V_{DDP3}) 3.3 V 单电源

$V_{EXT} = V_{DDP3} = 3.3$ V 单电源模式。VDD 由 EVRC 稳压器内部产生。

- 从外部稳压器汲取电流的速率 (di_{EXT}/dt) 在启动阶段被限制为最大 100 mA，建立时间为 100 μ s。电源轨的启动斜率应符合数据手册参数 SR。斜率定义为 0% 至 100% 电压电平之间的最大切向斜率。实际波形可能不同于规格书。
- 当 $PORST$ (输入) 或 $PORST$ (输出) 激活/置位时， $PORST$ 激活/置位。
- $PORST$ (输入) 有效意味着外部设备可通过将 $PORST$ 引脚拉低，使复位保持有效。建议保持 $PORST$ (输入) 有效，直到外部电源电压高于相应的主复位阈值。
- $PORST$ (输出) 有效意味着 μ C 在内部发出复位信号并将 $PORST$ 引脚驱动至低电平，从而将复位信号传播至外部设备。当三个电源域 (V_{DD} 、 V_{DDP3} 或 V_{EXT}) 中至少有一个违反其主要欠压复位阈值时， μ C 会发出 $PORST$ 置位 (输出) 信号。当所有电源均高于其主要复位阈值，且基本电源和时钟基础设施可用时， μ C 会发出 $PORST$ 不置位 (输出) 信号。在 T_3 复位释放期间，预计负载跳变高达 150 mA (dI_{DD})。

电气规格电源基础结构和电源启动

- 电源序列如图 3-4 列举如下
 - T1 至 T2 是指外部电源上升时基本电源和时钟基础设施组件可用的时间段。带隙和内部时钟源启动，根据 HWCFG[2:1,4,5,6] 和 TESTMODE 引脚决定供电模式。T1 至 T2 是指外部电源上升时基本电源和时钟基础设施组件可用的时间段。带隙和内部时钟源启动。根据 HWCFG[2:1,6] 引脚决定供电模式。这些事件在 T1 时 LVD 复位释放后启动。当两个输入电压 VEXT 和 VEVRSB 分别高于 VLVD RST5 和 VLVD RSTSB 电平时，LVD 复位被释放。内部预稳压器 VDDPD 输出电压高于 VLVD RSTC 电平。
 - T2 指的是 EVRC 稳压器软启动开始的时间点。PORST（输入）对 EVRC 输出没有任何影响，尽管 PORST 已断言且设备处于复位状态，稳压器仍会继续产生相应的电压。产生的电压在 tSTR（数据手册参数）时间内呈软上升趋势，以避免过冲。
 - T3 指的是所有电源都高于其主要复位阈值（由 VRST5、VRST33 和 VRSTC 供电电压水平表示）的时间点。EVRC 稳压器已启动。PORST（输出）不置位，并且 HWCFG[3:5] 引脚被 SCU 锁存在 PORST 上升沿。固件执行已启动。T1 和 T3 之间的时间记录为 tEVRstartup（数据手册参数）。
 - T4 指的是固件执行完成并且用户代码以 CPU0 的默认频率 100 MHz 开始执行的时间点。T0 和 T4 之间的时间记录为 tBP（数据手册参数）。
 - T5 指的是斜坡下降阶段期间至少一个外部提供或生成的电源（VDD、VDDP3 或 VEXT）降至其各自的初级欠压复位阈值以下的时间点。

电气规格电源基础结构和电源启动

3.13.1.3 外部供电模式 (d)

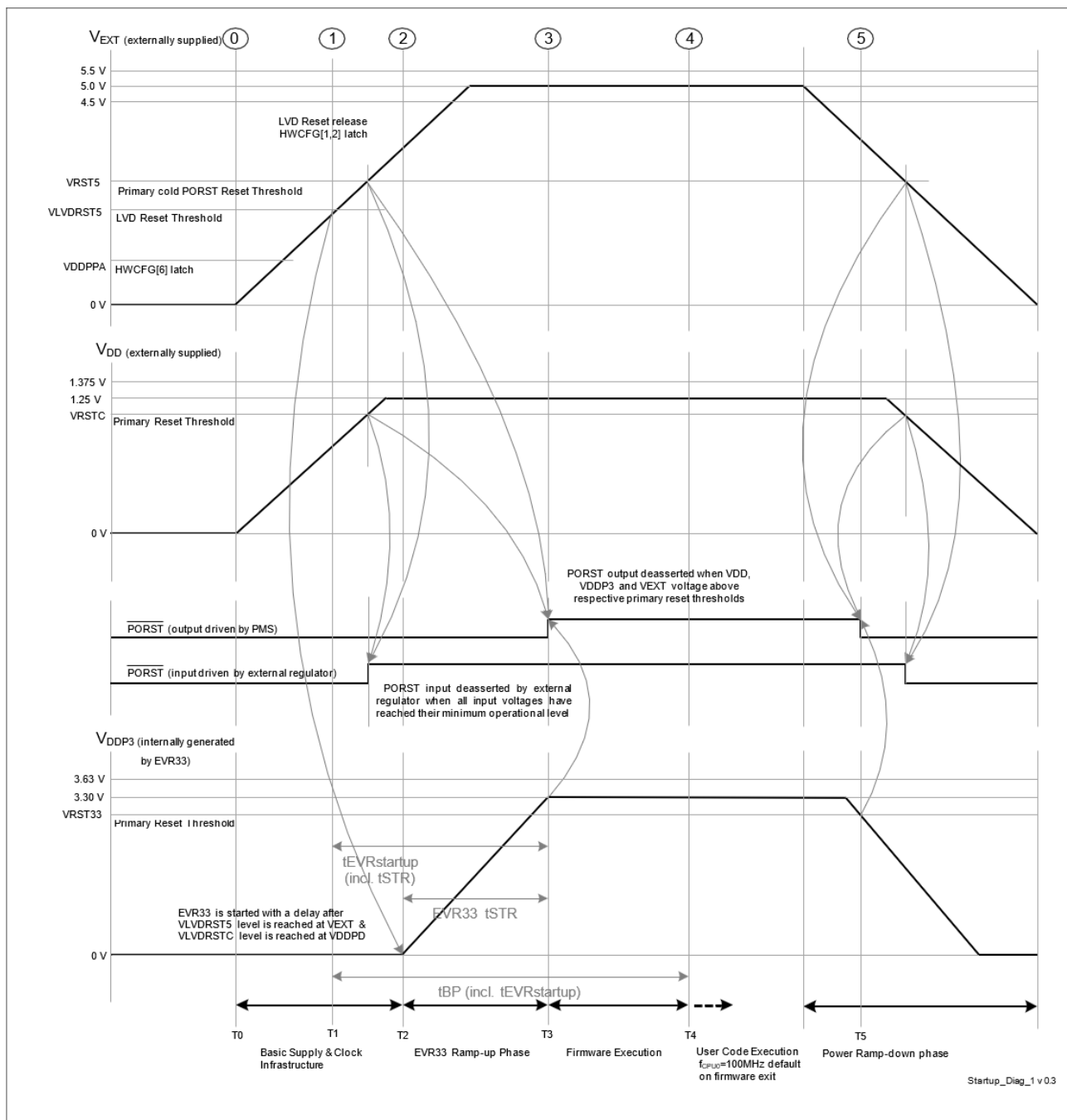


图 3-5 外部供电模式 (d) - V_{EXT} 和 V_{DD} 外部供电

$V_{EXT} = 5V$ 且 V_{DD} 电源由外部供电。3.3V 由 EVR33 稳压器内部产生。

- 外部电源 V_{EXT} 和 V_{DD} 可以在启动、上升和下降时间方面相互独立地上升或下降。电源轨的启动斜率应符合数据手册参数 SR。斜率定义为 0% 至 100% 电压电平之间的最大切向斜率。实际波形可能不同于规格书。预计在启动期间， V_{EXT} 会在 V_{DD} 轨之前上升。如果 V_{DD} 电源轨在 V_{EXT} 之前上升；启动期间的 V_{DD} 电源过冲应限制在工作电压范围内。

电气规格电源基础结构和电源启动

- 从外部稳压器汲取电流的速率 (dI_{EXT}/dt 或 dI_{DD}/dt) 在启动阶段被限制为最大 100 mA，建立时间为 100 μ s。
- 当 PORST (输入) 或 PORST (输出) 激活/置位时，PORST 激活/置位。
- PORST (输入) 有效意味着外部设备可通过将 PORST 引脚拉低，使复位保持有效。建议保持 PORST (输入) 有效，直到外部电源电压高于相应的主复位阈值。
- PORST (输出) 有效意味着 μ C 在内部发出复位信号并将 PORST 引脚驱动至低电平，从而将复位信号传播至外部设备。当三个电源域 (VDD、VDDP3 或 VEXT) 中至少有一个违反其主要欠压复位阈值时， μ C 会发出 PORST 置位 (输出) 信号。当所有电源均高于其主要复位阈值，且基本电源和时钟基础设施可用时， μ C 会发出 PORST 不置位 (输出) 信号。在 T3 复位释放期间，预计负载跳变高达 150 mA (dI_{DD})。
- 电源序列如图 3-5 列举如下
 - T1 至 T2 是指外部电源上升时基本电源和时钟基础设施组件可用的时间段。带隙和内部时钟源启动。根据 HWCFG[2:1,4,5,6] 和 TESTMODE 引脚来决定供电模式。T1 至 T2 是指外部电源上升时基本电源和时钟基础设施组件可用的时间段。带隙和内部时钟源启动。根据 HWCFG[2:1,6] 引脚决定供电模式。这些事件在 T1 时 LVD 复位释放后启动。当两个输入电压 VEXT 和 VEVRSB 分别高于 VLVD RST5 和 VLVD RSTSB 电平时，LVD 复位被释放。内部预稳压器 VDDPD 输出电压高于 VLVD RSTC 电平。
 - T2 指的是 EVR33 稳压器软启动开始的时间点。PORST (输入) 对 EVR33 输出没有任何影响，尽管 PORST 已置位且设备处于复位状态，稳压器仍会继续产生相应的电压。产生的电压在 tSTR (数据手册参数) 时间内呈软上升趋势，以避免过冲。
 - T3 指的是所有电源都高于其主要复位阈值 (由 VRST5、VRST33 和 VRSTC 供电电压水平表示) 的时间点。EVR33 稳压器已启动。PORST (输出) 不置位，并且 HWCFG[3:5] 引脚被 SCU 锁存在 PORST 上升沿。固件执行已启动。T1 和 T3 之间的时间记录为 tEVRstartup (数据手册参数)。
 - T4 指的是固件执行完成并且用户代码以 CPU0 的默认频率 100 MHz 开始执行的时间点。T0 和 T4 之间的时间记录为 tBP (数据手册参数)。
 - T5 指的是斜坡下降阶段期间至少一个外部提供或生成的电源 (VDD、VDDP3 或 VEXT) 降至其各自的初级欠压复位阈值以下的时间点。

电气规格电源基础结构和电源启动

3.13.1.4 外部供电模式 (h)

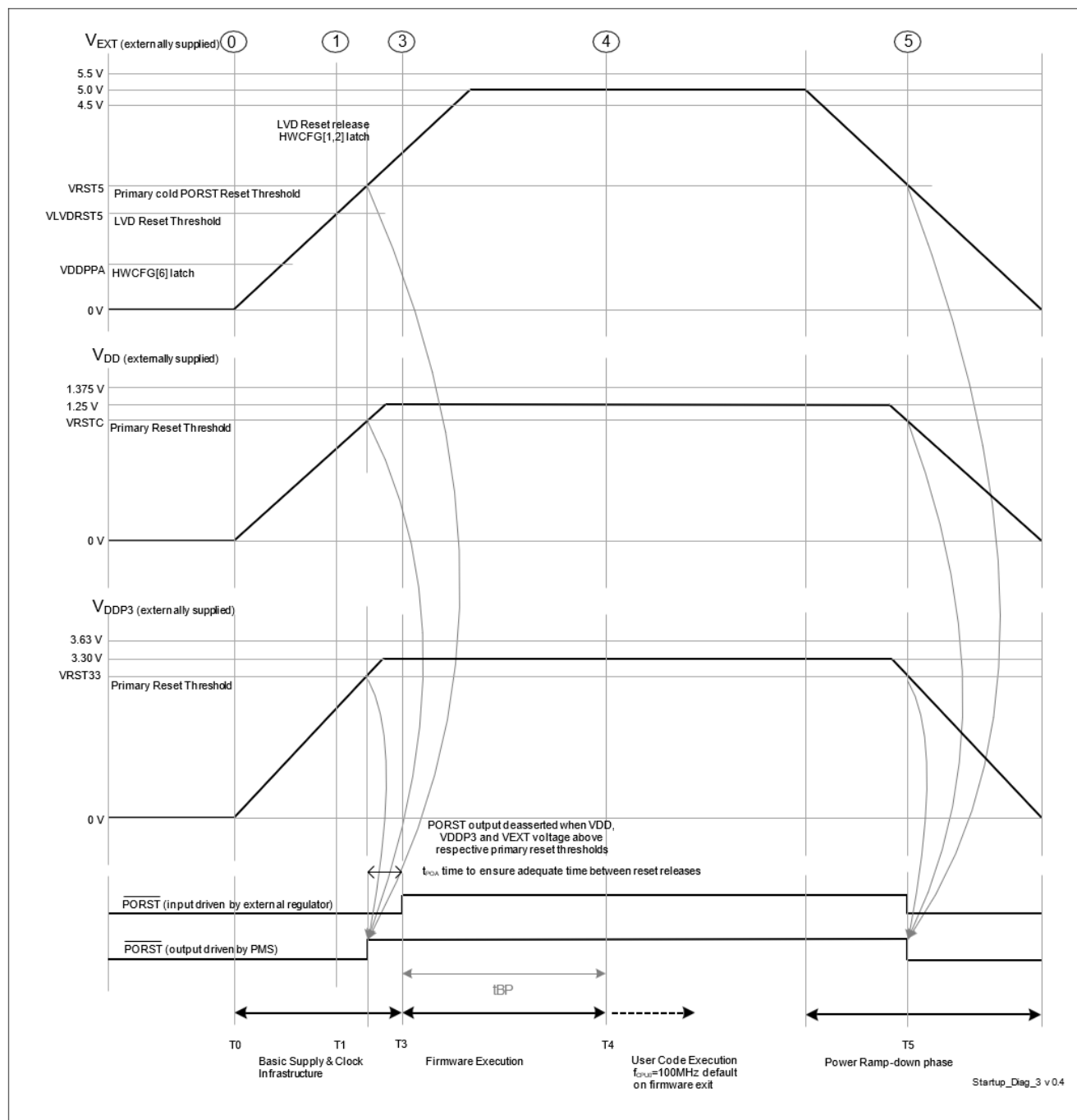


图 3-6 外部供电模式 (h) - V_{EXT} 、 V_{DDP3} 和 V_{DD} 外部供电

所有电源，即 V_{EXT} 、 V_{DDP3} 和 V_{DD} 均由外部供电。

- 外部电源 V_{EXT} 、 V_{DDP3} 和 V_{DD} 可能会根据启动、上升和下降时间而彼此独立地上升或下降。电源轨的启动斜率应符合数据手册参数 SR。斜率定义为 0% 至 100% 电压电平之间的最大切向斜率。实际波形可能不同于规格书。预计在启动期间， V_{EXT} 会在 V_{DDP3} 和 V_{DD} 轨之前上升。如果较小的电压轨在 V_{EXT} 之前上升，则启动期间的 V_{DD} 和 V_{DDP3} 电源过冲应限制在各自电压轨的工作电压范围内。

电气规格 电源基础结构和电源启动

- 从外部稳压器汲取电流的速率 (dI_{EXT}/dt , dI_{DD}/dt 或 dI_{DDP3}/dt) 在启动阶段被限制为最大 100 mA, 建立时间为 100 μ s。
- 当 PORST (输入) 或 PORST (输出) 激活/置位时, PORST 激活/置位。
- PORST (输入) 有效意味着外部设备可通过将 PORST 引脚拉低, 使复位保持有效。建议保持 PORST (输入) 有效, 直到外部电源电压高于相应的主复位阈值。
- PORST (输出) 有效意味着 μ C 在内部发出复位信号并将 PORST 引脚驱动至低电平, 从而将复位信号传播至外部设备。当三个电源域 (VDD、VDDP3 或 VEXT) 中至少有一个违反其主要欠压复位阈值时, μ C 会发出 PORST 置位 (输出) 信号。当所有电源均高于其主要复位阈值, 且基本电源和时钟基础设施可用时, μ C 会发出 PORST 不置位 (输出) 信号。在 T3 复位释放期间, 预计负载跳变高达 150 mA (dI_{DD})。
- 电源序列如图 3-6 列举如下
 - T1 至 T3 是指外部电源上升时基本电源和时钟基础设施组件可用的时间段。带隙和内部时钟源启动。根据 HWCFG[2:1,4,5,6] 和 TESTMODE 引脚来决定供电模式。T1 至 T2 是指外部电源上升时基本电源和时钟基础设施组件可用的时间段。带隙和内部时钟源启动。根据 HWCFG[2:1,6] 引脚决定供电模式。这些事件在 T1 时 LVD 复位释放后启动。当两个输入电压 VEXT 和 VEVRSB 分别高于 VLVD RST5 和 VLVD RSTSB 电平时, LVD 复位被释放。内部预稳压器 VDDPD 输出电压高于 VLVD RSTC 电平。
 - T3 指的是所有电源都高于其主要复位阈值 (由 VRST5、VRST33 和 VRSTC 供电电压水平表示) 的时间点。PORST (输出) 不置位, 并且 HWCFG[3:5] 引脚被 SCU 锁存在 PORST 上升沿。固件执行已启动。
 - T4 指的是固件执行完成并且用户代码以 CPU0 的默认频率 100 MHz 开始执行的时间点。T0 和 T4 之间的时间记录为 tBP (数据手册参数)。
 - T5 指的是斜坡下降阶段期间至少一个外部提供或生成的电源 (VDD、VDDP3 或 VEXT) 降至其各自的初级欠压复位阈值以下的时间点。

电气规格复位时序

3.14 复位时序

表 3-30 复位

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Application Reset Boot Time	t_{BCC}	-	-	400	μs	operating with max. frequencies, with valid BMI header
System Reset Boot Time	t_{BSCC}	-	-	1.1	ms	RAM initialization and HSM boot time are not included, with valid BMI header
Cold Power on Reset Boot Time ¹⁾	t_{BPC}	-	-	3.1	ms	$dV_{EXT}/dT=1V/ms$. $V_{EXT}>V_{LVDRST5}$. Boot time after Cold PORST including EVR ramp-up and Firmware execution time; RAM initialization and HSM boot time are not included.
		-	-	1.6	ms	Firmware execution time after PORST release without EVR ramp-up; RAM initialization and HSM boot time is not included
Minimum cold PORST reset hold time in case of power fail event issued by EVR primary monitors	$t_{EVRPORCC}$	10 ²⁾	-	-	μs	
PMS Infrastructure, EVRC and EVR33 overall start-up time till cold PORST reset release	$t_{EVRstartupCC}$	-	-	1	ms	$dV/dT=1V/ms$. EVRC and EVR33 active
Minimum PORST active hold time externally after power supplies are stable at operating levels after start-up	t_{POASR}	1 ³⁾	-	-	ms	
Configurable PORST digital filter delay in addition to analog pad filter delay	$t_{PORSTDFCC}$	600	-	1200	ns	
Warm Reset Sequencing Delay	$t_{WARMRSTSEQCC}$	-	-	180	μs	
HWCFG pins hold time from ESR0 rising edge	t_{HDHCC}	$16/f_{SPB}$	-	-	ns	

电气规格复位时序

表 3-30 复位 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
HWCFG pins setup time to ESR0 rising edge	t_{HDS} CC	0	-	-	ns	
Ports inactive after ESR0 reset active	t_{PI} CC	$8000/f_{BAC}$ KT	-	$18000/f_{BA}$ CKT	s	
Ports inactive after PORST reset active	t_{PIP} CC	-	-	160	ns	
Hold time from PORST rising edge	t_{POH} SR	150	-	-	ns	
Setup time to PORST rising edge	t_{POS} SR	0	-	-	ns	
Warm PORST reset boot time	t_{BWP} CC	-	-	1.5	ms	without RAM initialization
LBIST execution time extending the boot time	t_{LBIST} CC	-	-	6	ms	LBIST Configuration A; $1.2V \leq V_{DD}$
SCR reset boot time	t_{SCR} CC	-	-	5	μs	User Mode 0
		-	-	16	μs	User Mode 1
		-	13.3	-	μs	WDT double bit ECC, soft reset
Minimum external supplies hold time after warm reset assertion	$t_{SUPHOLD}$ CC	-	-	250	μs	external supplies are V_{EVRSB} , V_{EXT} , $V_{FLEX/FLEX2}$, V_{DDM} , V_{DDP3} and V_{DD}

- 1) RAM 初始化另外增加 500 μs 。
- 2) 冷 PORST 复位由 uC 驱动，并维持在 VDDPPA 限制和绝对最大额定电压限制之间的扩展电压范围内。
- 3) 电源上升或电源恢复时的复位释放被延迟了 1.5%（默认值）的电压滞回，该电压滞回高于 VEXT、VDDP3 和 VDD 轨上实施的欠压复位限值。这种机制有助于避免在电源缓慢上升期间，由于复位释放时压降/电流跳跃而导致的多个连续的冷 PORST 事件。

电气规格复位时序

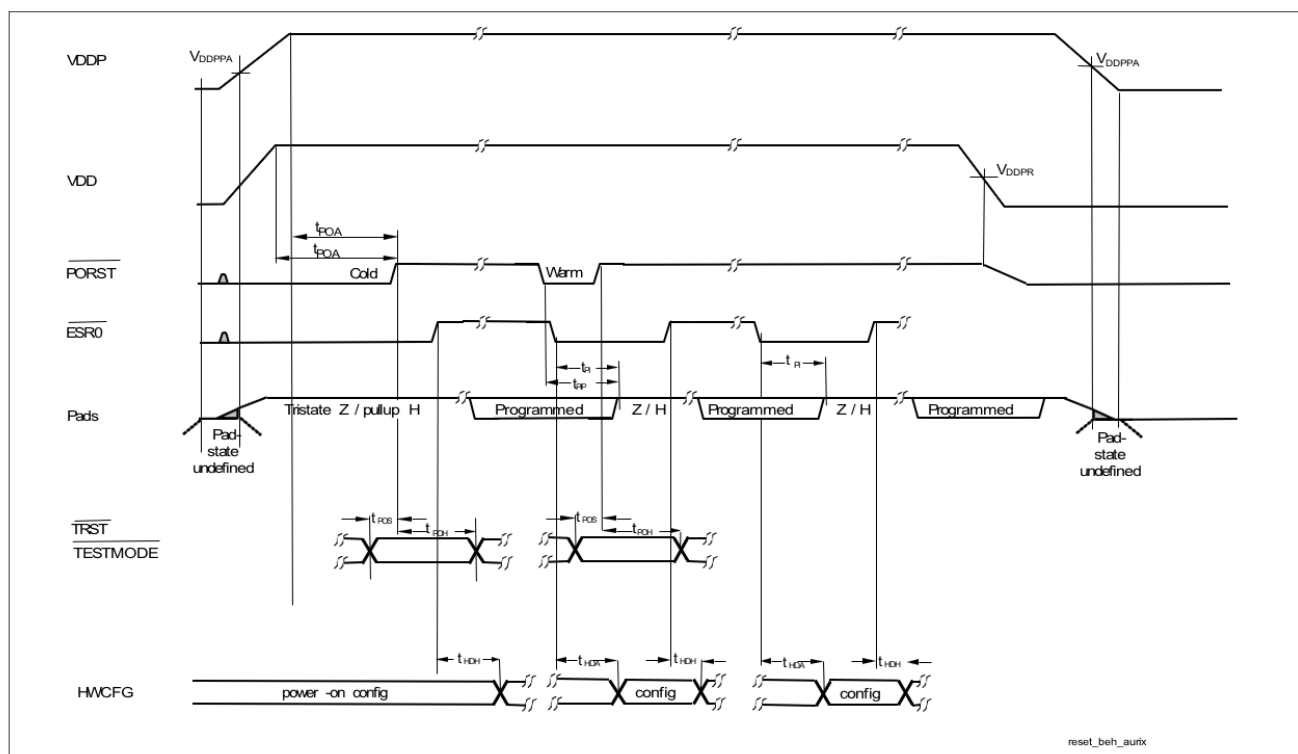


图 3-7 电源、焊盘和复位时序

3.15 PMS

表 3-31 EVR33 LDO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input voltage range	$V_{IN\ SR}$	3.60 ¹⁾	-	5.50	V	Normal RUN mode
		2.97 ²⁾	-	5.50	V	Low voltage cranking mode
Output voltage operational range including load/line regulation and aging ³⁾	$V_{OUT\ CC}$	2.97	3.3	3.63	V	Normal RUN mode
		2.60	3.3	3.63	V	Low voltage cranking mode; $I_{DDP3}=50mA$
Output V_{DDX3} static voltage accuracy after trimming and aging without dynamic load/line regulation.	$V_{OUTT\ CC}$	3.225	3.3	3.375	V	Normal RUN mode
		2.78	3.3	3.375	V	Low voltage cranking mode; $I_{DDP3}=50mA$
Output buffer capacitance on V_{OUT}	$C_{OUT\ SR}$	1.45	2.2	3	μF	
Output buffer capacitor ESR	$C_{OUTESR\ SR}$	-	-	100 ⁴⁾	mOhm	$f > 0.5MHz$; $f < 10MHz$
Maximum output current of the regulator	$I_{MAX\ CC}$	60 ⁵⁾	-	-	mA	Normal RUN mode
Startup time	$t_{STR\ CC}$	-	500	1000	μs	Normal RUN mode
External V_{IN} supply ramp ⁶⁾	$dV_{in}/dt\ SR$	-	1	-	V/ms	
Ripple on Output Voltage	$\Delta V_{OUTTC\ CC}$	-	-	33	mV	$V_{EXT} \geq 2.97V$; $V_{EXT} \leq 5.5V$; $I_{OUTTC} \geq 10mA$; $I_{OUTTC} \leq 60mA$; ΔV_{OUTTC} = (peak to peak ripple / 2)
Load step response ⁷⁾	$dV_{out}/dI_{out\ CC}$	-165	-	-	mV	Normal RUN mode; $dI=10$ to $60mA$; $dt=20ns$; $T_{settle}=20\mu s$
		-	-	165	mV	Normal RUN mode; $dI=60$ to $10mA$; $dt=20ns$; $T_{settle}=20\mu s$
		-180	-	-	mV	Low voltage cranking mode; $dI=10$ to $50mA$; $dt=20ns$; $T_{settle}=20\mu s$
		-	-	180	mV	Low voltage cranking mode; $dI=50$ to $10mA$; $dt=20ns$; $T_{settle}=20\mu s$

表 3-31 EVR33 LDO (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line step response	dV_{out}/dV_{in} CC	-	-	40	mV	$dV_{in}/dT=1V/ms$; $dV=3.6$ to $5V$; $I_{MAX}=60mA$; ΔV_{OUTTC} is included
		-40	-	-	mV	$dV_{in}/dT=1V/ms$; $dV=5$ to $3.6V$; $I_{MAX}=60mA$; ΔV_{OUTTC} is included
		-	-	280	mV	$dV_{in}/dT=50V/ms$; $dV=3.6$ to $5V$; $I_{MAX}=60mA$
		-165	-	-	mV	$dV_{in}/dT=50V/ms$; $dV=5$ to $3.6V$; $I_{MAX}=60mA$

- 1) 最小输入电压中包含 300mV 的最大传输器件压差，以确保正常运行期间传输器件的最佳性能。
- 2) VEXT 输入电压降到 2.97V，将导致 VDDP3 输出电压降到 2.6V，如果在此之前已经将Flash切换到低性能模式，那么是可以正常工作的。
- 3) 如果使用 EVR33，则不允许使用外部感应负载。
- 4) 还建议从引脚到 EVR 输出电容器的电源走线电阻小于 100 mOhm。应在 Cout 之前靠近引脚的位置放置一个 100nF 的附加去耦电容。
- 5) 在低压模式（启动情况）下，使用片上传输装置时，IMAX 限制为 40 mA。若未使用 EVR33，当外部稳压器在上电时序期间 3.3 V 先于 5V 上电时，且 5V VEXT 供电轨存在有源下拉时，注入 3.3V VDDP3 电源轨的电流应限制在 500 mA 以内。
- 6) EVR 能够有效抵御 0 - 2.97 V 之间残余电压的上升。稳健性验证涵盖 0.5V/min 至 120V/ms 之间的 VEXT 电压斜坡范围。产生的电压本身在 tSTR 时间内遵循软上升趋势，以避免过冲。
- 7) 建立时间被定义为直到输出电压在单个器件平均值(VOUTT) 的+1% 范围内。

表 3-32 电源监视器

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Primary Undervoltage Reset threshold for V_{DDP3} before trimming ¹⁾	V_{RST33} CC	-	-	3.00	V	by reset release before EVR trimming on supply ramp-up
Primary undervoltage reset threshold for V_{DD} before trimming	V_{RSTC} CC	-	-	1.138	V	by reset release before trimming on supply ramp-up including 2 LSB voltage Hysteresis
V_{EXT} primary undervoltage monitor accuracy after trimming ²⁾	$V_{EXTPRIUV}$ CC	2.86	2.92	2.97	V	V_{EXT} = Undervoltage cold PORST Primary Monitor Threshold
V_{DDP3} primary undervoltage monitor accuracy after trimming ²⁾	$V_{DDP3PRIUV}$ CC	2.86 ³⁾	2.90	2.97	V	VDDP3 = Undervoltage cold PORST Primary Monitor Threshold

表 3-32 电源监视器 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{DD} primary undervoltage monitor accuracy after trimming ²⁾	$V_{DDPRIUV}$ CC	1.08 ³⁾	1.105	1.125	V	VDD = Undervoltage cold PORST Primary Monitor Threshold
EVR primary monitor measurement latency for a new supply value	t_{PRIUV} CC	-	-	300	ns	The supply ramp / line jump slope is limited to 50V/ms for V_{EXT} , V_{DDP3} and V_{DD} rails.
V_{EXT} , V_{DDM} & V_{EVRSB} secondary supply monitor accuracy after trimming ^{4) 5)}	V_{EXTMON} CC	5.3	5.4	5.5	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=5.4V=EBh(UV)/ ECh(OV). For BGA packages: EVRMONFILT.SWDFI L=1
		5.3	5.4	5.5	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=5.4V=EBh(UV)/ ECh(OV). For QFP packages: EVRMONFILT.SWDFI L=2
		3.2	3.3	3.4	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=3.3V=90h(OV,U V). For BGA packages: EVRMONFILT.SWDFI L=1.
		3.2	3.3	3.4	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=3.3V=90h(OV,U V). For QFP packages: EVRMONFILT.SWDFI L=2

表 3-32 电源监视器 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{EXT} , V_{DDM} & V_{EVRSB} secondary supply monitor accuracy after trimming (cont'd)	V_{EXTMON} CC	4.5	4.6	4.7	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=4.6V=C8h(UV) /C9h(OV). For BGA packages: EVRMONFILT.SWDFI L=1
		4.5	4.6	4.7	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=4.6V=C8h(UV) /C9h(OV). For QFP packages: EVRMONFILT.SWDFI L=2
		4.9	5.0	5.1	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=5V=D9h(UV) /DAh(OV). For BGA packages: EVRMONFILT.SWDFI L=1
		4.9	5.0	5.1	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=5V=D9h(UV) /DAh(OV). For QFP packages: EVRMONFILT.SWDFI L=2

表 3-32 电源监视器 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{DDP3} secondary supply monitor accuracy after trimming ⁵⁾	$V_{DDP3MON}$ CC	2.97	3.035	3.1	V	EVR33xxVAL monitoring threshold=3.035V=CBh(UV)/CCh(OV). EVRMONFILT.EVR33 FIL = 3.
		3.235	3.30	3.365	V	EVR33xxVAL monitoring threshold=3.3V=DDh(OV, UV). EVRMONFILT.EVR33 FIL = 3.
		3.5	3.565	3.63	V	EVR33xxVAL monitoring threshold=3.565V=EEh(UV)/EFh(OV). EVRMONFILT.EVR33 FIL = 3.
V_{DD} & V_{DDPD} secondary supply monitor accuracy after trimming ⁵⁾	V_{DDMON} CC	1.125	1.15	1.175	V	EVRCxxVAL & PRExxVAL monitoring threshold=1.15V=C7h(U V)/C8h(OV). EVRMONFILT.EVRC FIL = 1.
		1.225	1.25	1.275	V	EVRCxxVAL & PRExxVAL monitoring threshold=1.25V=D9h(O V,UV). EVRMONFILT.EVRC FIL = 1.
		1.325	1.35	1.375	V	EVRCxxVAL & PRExxVAL monitoring threshold=1.35V=EAh (UV)/EBh(OV). EVRMONFILT.EVRC FIL = 1.
V_{EXT} LVD Primary undervoltage reset Monitor threshold	$V_{LVDRST5}$ CC	2.3	-	2.72	V	Power-down
		2.4	-	2.75	V	Power-up
V_{EVRSB} LVD Primary undervoltage reset Monitor threshold	$V_{LVDRSTB}$ CC	2.18	-	2.47	V	Power-down
		2.21	-	2.5	V	Power-up
V_{EXT} and V_{EVRSB} PBIST primary overvoltage Monitor threshold	V_{PBIST5} CC	5.63	-	-	V	

表 3-32 电源监视器 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Primary undervoltage reset threshold for V_{EXT} before trimming	V_{RST5}^{CC}	-	-	3.0	V	by last cold PORST release on supply ramp-up including voltage hysteresis.
EVR secondary monitor measurement latency for all 6 supply rails	t_{MON}^{CC}	-	-	3.2	μs	HPOSC and SHPBG bandgap trimmed. Filter inactive.

- 1) 电源上升时的复位释放在达到欠压复位阈值后会延迟 20-40 微秒的时间，并且电压滞回会高于欠压复位限值 1.5%。这种机制有助于避免在电源缓慢上升期间，由于复位释放时压降/电流跳跃而导致的多个连续的冷 PORST 事件。引脚的复位限制为 2.97V，适用于 EVR33 内部产生 3.3V 的情况。如果外部提供 3.3V 电源，则键合线压降将导致 VDDP3 引脚上电压达到 3.0V 就复位。
- 2) 监视器公差构成了带隙和 ADC 在工艺、电压和温度操作范围内的固有变化。 $V_{xxPRIUV}$ 参数在生产过程中经过单独测试，与 $V_{xxPRIUV}$ 限值有 $\pm 1\%$ 的公差。所有电压均在引脚上测量。
- 3) $VRST_{xx}$ 参数仅与第一次冷 PORST 释放相关。随后，在器件以完整性能使用之前，复位电平由固件调整并反映为 $V_{xxPRIUV}$ 参数。冷 PORST 通过所有主监视器上的电压滞回释放，以避免连续的 PORST 切换行为。
- 4) 如果应用程序使用 3.3V 单电源（单电源模式 (e)，即当 V_{EXT} 与 VDDP3 短接时，建议在通道 VDDP3 上使用二次电源监控，因为 VDDP3MON 参数的精度更高。
- 5) 对于未提供监视器电压电平的条件，OV 和 UV 阈值可以根据给定的点通过线性插值或外推生成。

表 3-33 供电斜坡

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
External V_{EXT} & V_{EVR5B} supply ramp-up and ramp-down slope 1) 2) 3)	dV_{EXT}/dt SR	8.3E-6	1	100	V/ms	
External V_{DDP3} supply ramp-up and ramp-down slope ¹⁾³⁾	dV_{DDP3}/dt SR	8.3E-6	1	100	V/ms	
External V_{DD} supply ramp-up and ramp-down slope ¹⁾³⁾	dV_{DD}/dt SR	8.3E-6	1	100	V/ms	
External V_{DDM} supply ramp-up and ramp-down slope ¹⁾³⁾	dV_{DDM}/dt SR	8.3E-6	1	100	V/ms	

- 1) 该器件具有很强的抗残余电压上升能力，对于 V_{EXT} 、 V_{EVR5B} 、VDDP3 和 VDDM，电压上升范围为 0 - 2.97 V，对于 VDD，电压上升范围为 0-1 V。稳健性验证涵盖 0.5V/min 至 120V/ms 之间的 V_{EXT} 电压斜坡范围。
- 2) 在使用 EVR33 或 EVRC 的情况下也有效。产生的电压本身在 t_{STR} 时间内遵循软上升趋势，以避免过冲。
- 3) 斜率定义为 0% 至 100% 电压电平之间的最大切向斜率。实际波形可能不同于规格书。

- TC37x 允许最多 1000000 次电源循环，符合“电源斜坡”表中定义的限制，且对可靠性没有任何限制。

表 3-34 EVRC SMPS

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input V_{EXT} Voltage range	V_{IN} SR	2.97	-	5.5	V	Start-up VEXT voltage > 2.6 V
SMPS regulator output voltage range including load/line regulation and aging	V_{DDDC} CC	1.125	-	1.375	V	$V_{EXT} \geq 2.97V$; $V_{EXT} \leq 5.5V$; $I_{DDDC} \geq 1mA$; $I_{DDDC} \leq 1.5A$; untrimmed
SMPS regulator static voltage output accuracy after trimming without dynamic load/line regulation.	V_{DDDC} CT	1.225	1.25	1.275	V	$V_{EXT} \geq 2.97V$; $V_{EXT} \leq 5.5V$; $I_{DDDC} \geq 1mA$; $I_{DDDC} \leq 1.5A$
Programmable switching frequency	f_{DCDC} SR	1.6	1.82	2.0	MHz	Start-up frequency switches from 500 KHz in open loop operation to 1.82 MHz in closed loop Operation.
		-	0.8	-	MHz	Start-up frequency switches from 500 KHz in open loop operation to 1.82 MHz in closed loop Operation. 0.8 MHz to be set in SW.
Startup time	t_{STRDC} CC	-	-	900	μs	SMPS Start-up Mode. It is defined between $V_{EXTPRIUV}$ reset threshold till PORST release, on condition that all other PORST requirements were released before. $I_{START} < 700mA$.
Switching frequency modulation spread	Δf_{DCSPR} CC	-	1.8%	-	MHz	
Maximum ripple at I_{MAX}	ΔV_{DDDC} CC	-	-	16	mV	$V_{EXT} \geq 2.97V$; $V_{EXT} \leq 5.5V$; $I_{DDDC} \geq 300mA$; $I_{DDDC} \leq 1.5A$; $\Delta V_{DDDC} = (\text{Peak to Peak ripple} / 2)$
No load current consumption of SMPS regulator	I_{DCNL} CC	-	15	19	mA	$f_{DCDC}=1.82MHz$; $I_{DDDC}=I_{SLEEP}$; $V_{EXT} > 2.97V$; $T_j=25^\circ C$
		-	5	-	mA	LPM mode; $I_{DDDC}=I_{SLEEP}$; $V_{EXT} > 2.97V$; $T_j=25^\circ C$

表 3-34 EVRC SMPS (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SMPS regulator load transient response	$\frac{dV_{DDCT}}{dI_{OUT\ CC}}$	-50	-	75	mV	$dI < -250mA$; $I_{DDDC}=280-1500mA$; $t_r=0.1\mu s$; $t_f=0.1\mu s$; $V_{DDDC}=1.25V$; $T_{settle}=100\ \mu s$
		-50	-	87	mV	$dI < -450mA$; $I_{DDDC}=500-1500mA$; $t_r=0.1\mu s$; $t_f=0.1\mu s$; $V_{DDDC}=1.25V$; $T_{settle}=100\ \mu s$
		-100	-	145	mV	$dI < -700mA$; $I_{DDDC}=750-1500mA$; $t_r=0.1\mu s$; $t_f=0.1\mu s$; $V_{DDDC}=1.25V$; $T_{settle}=100\ \mu s$
		-26	-	26	mV	$dI < 100mA$; $I_{DDDC}=50-1500mA$; $t_r=0.1\mu s$; $t_f=0.1\mu s$; $V_{DDDC}=1.25V$; $T_{settle}=20\mu s$;
Maximum output current	$I_{MAX\ CC}$	100	-	-	mA	LPM mode. Typical current in LPM Mode = I_{SLEEP}
		1.5	-	-	A	limited by thermal constraints and component choice
SMPS regulator line transient response	$\frac{dV_{DDCT}}{dV_{IN\ CC}}$	-75	-	75	mV	$dV/dT=120V/ms$; $dV < 2.97 - 5.5V$; $I_{DDDC}=50-1500mA$;
		-12.5	-	12.5	mV	$dV/dT=1V/ms$; $dV < 2.97 - 5.5V$; $I_{DDDC}=50-1500mA$;
SMPS regulator efficiency	$\eta_{DC\ CC}$	-	80	-	%	$V_{IN}=3.3V$; $I_{DDDC}=1500mA$; $f_{DCDC}=1.82MHz$
		-	75	-	%	$V_{IN}=5V$; $I_{DDDC}=1500mA$; $f_{DCDC}=1.82MHz$
Input Synchronisation frequency	$f_{DCDCSYNC\ SR}$	1.6	1.82	2.0	MHz	

表 3-35 EVRC SMPS 外部组件

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
External output capacitor value ¹⁾	C_{OUT_SR}	20.8	32	43.2	μF	$I_{DDDC}=1.5A; f_{DDDC}=0.8MHz$
		15.4	22	29.7	μF	$I_{DDDC}=1.5A; f_{DDDC}=1.82MHz$
External output capacitor ESR	$C_{OUT_ESR_SR}$	-	-	50	mOhm	$f \geq 0.5MHz; f \leq 10MHz$
		-	-	100	Ohm	$f=10Hz$
External input capacitor value ¹⁾	C_{IN_SR}	6.5	10	13.5	μF	$I_{DDDC}=1.5A$
		4.42	6.8	9.18	μF	$I_{DDDC}=500mA$
External input capacitor ESR	$C_{IN_ESR_SR}$	-	-	50	mOhm	$f \geq 0.5MHz; f \leq 10MHz$
		-	-	100	Ohm	$f=100Hz$
External inductor value	L_{DC_SR}	3.29	4.7	6.11		$f_{DCDC}=0.8MHz$
		2.31	3.3	4.29	μH	$f_{DCDC}=1.82MHz$
External inductor DCR	$L_{DC_DCR_SR}$	-	-	0.2	Ohm	
P + N-channel MOSFET logic level	V_{LL_SR}	-	-	2.5	V	
P + N-channel MOSFET drain source breakdown voltage	$ V_{BR_DS} _SR$	+7	-	-	V	NMOS - $V_{GS}=0$.
		-	-	-7	V	PMOS - $V_{GS}=0$.
P + N-channel MOSFET drain source ON-state resistance	R_{ON_SR}	-	150	-	mOhm	$I_{DDDC}=1.5A; V_{GS} =2.5V; T_A=25^\circ C$
		-	200	-	mOhm	$I_{DDDC}=500mA; V_{GS} =2.5V; T_A=25^\circ C$
P + N-channel MOSFET Gate Charge	Q_G_SR	-	-	8	nC	$I_{DDDC}=1.5A$; NMOS- $ V_{GS} =5V$; 1.5A pulsed drain current
		-8	-	-	nC	$I_{DDDC}=1.5A$; PMOS- $ V_{GS} =5V$; 1.5A pulsed drain current
		-	-	4	nC	$I_{DDDC}=500mA$; NMOS- $ V_{GS} =5V$; 0.5A pulsed drain current
		-4	-	-	nC	$I_{DDDC}=500mA$; PMOS- $ V_{GS} =5V$; 0.5A pulsed drain current
External Inductor Saturation Current Margin	ΔI_{SAT_SR}	400	-	-	mA	The saturation current of the coil must be larger than $I_{DDDC} + \Delta I_{SAT}$

表 3-35 EVRC SMPS 外部组件 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
P + N-channel MOSFET Gate threshold voltage	V_{GTH} SR	-	1	-	V	NMOS
		-	-1	-	V	PMOS
N-channel MOSFET reverse diode forward voltage	V_{RDN} SR	-	0.8	-	V	

1) 电容器最小-最大范围代表典型的 +35% 公差，包括DC偏置效应。从电容器到电源或接地轨的走线电阻应限制为 25 mOhm。

电气规格系统锁相环 (SYS_PLL)

3.16 系统锁相环 (SYS_PLL)

表 3-36 PLL 系统

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DCO Input frequency range	f_{REF} CC	10	-	40	MHz	
Modulation Amplitude	MA CC	0	-	2	%	
Peak Period jitter	DP CC	-200	-	200	ps	without modulation (PLL output frequency)
Peak Accumulated Jitter	D_{PP} CC	-5	-	5	ns	without modulation
Total long term jitter	J_{TOT} CC	-	-	11.5	ns	including modulation; MA 1.25%; f_{REF} 20MHz
System frequency deviation	f_{SYSD} CC	-	-	0.01	%	with active modulation
DCO frequency range	f_{DCO} CC	400	-	800	MHz	
PLL lock-in time	t_L CC	4	-	100	μs	

注释：如果每个引脚的电容负载在最大驱动器和锐边的情况下不超过 $C_L = 20$ pF，则指定的PLL 抖动值有效。

注释：电源电压上的最大峰峰值噪声限制为：

噪声频率低于300 KHz时， $V_{PP} = 100$ mV；噪声频率高于300 KHz时， $V_{PP} = 40$ mV。这些条件可以通过在尽可能靠近电源引脚的位置适当阻断电源电压，并使用PCB 电源层和接地层来实现。

电气规格外设锁相环 (PER_PLL)

3.17 外设锁相环 (PER_PLL)

表 3-37 PLL 外设

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Peak Accumulated jitter at SYSClk pin	$D_{PP} CC$	-1000	-	1000	ps	Peak only
Peak accumulated jitter	$D_{PPI} CC$	-700	-	700	ps	Peak only
RMS Accumulated jitter	$D_{RMS} CC$	-100	-	100	ps	measured over 1 μs ; $f_{REF} = 20 \text{ MHz}$ and $f_{DCO} = 640 \text{ MHz}$ or $f_{REF} = 25 \text{ MHz}$ and $f_{DCO} = 800 \text{ MHz}$
Peak Period jitter	$DP CC$	-200	-	200	ps	$f_{DCO} = 640 \text{ MHz}$ or $f_{DCO} = 800 \text{ MHz}$
Absolute RMS jitter (PLL out)	$J_{ABS10} CC$	-125	-	125	ps	$f_{REF} = 10 \text{ MHz}$; $f_{DCO} = 640 \text{ MHz}$
Absolute RMS jitter (PLL out)	$J_{ABS20} CC$	-85	-	85	ps	$f_{REF} = 20 \text{ MHz}$; $f_{DCO} = 640 \text{ MHz}$
Absolute RMS jitter (PLL out)	$J_{ABS25} CC$	-85	-	85	ps	$f_{REF} = 25 \text{ MHz}$; $f_{DCO} = 800 \text{ MHz}$
DCO frequency range	$f_{DCO} CC$	400	-	800	MHz	
DCO input frequency range	$f_{REF} CC$	10	-	40	MHz	
PLL lock-in time	$t_L CC$	4	-	100	μs	

注释：如果每个引脚的电容负载在最大驱动器和锐边的情况下不超过 $C_L = 20 \text{ pF}$ ，则指定的PLL 抖动值有效。

注释：电源电压上的最大峰峰值噪声限制为

噪声频率低于300 KHz时， $V_{PP} = 100 \text{ mV}$ ；噪声频率高于300 KHz时， $V_{PP} = 40 \text{ mV}$ 。这些条件可以通过在尽可能靠近电源引脚的位置适当阻断电源电压，并使用PCB 电源层和接地层来实现。

电气规格 AC电规格

3.18 AC规范

所有AC参数均由[章节3.4](#)中定义的完整操作范围指定，除非在“注释/测试条件”栏中另有说明。

除非图中另有说明，否则时间定义遵循以下准则：

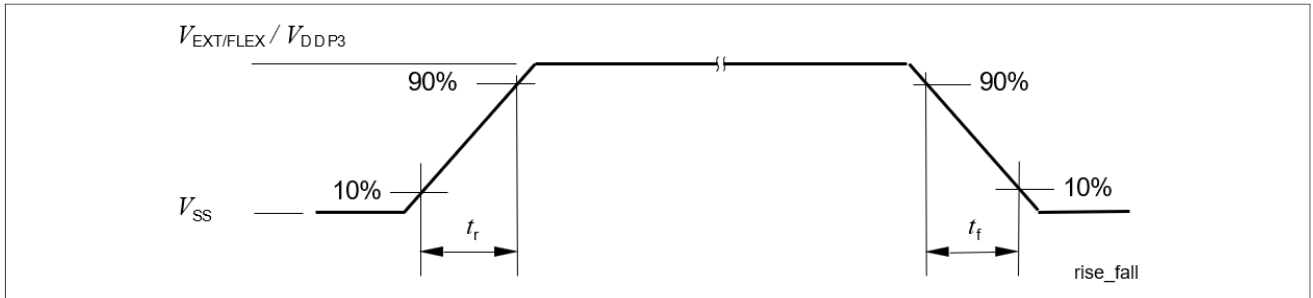


图 3-8 上升/下降时间的定义

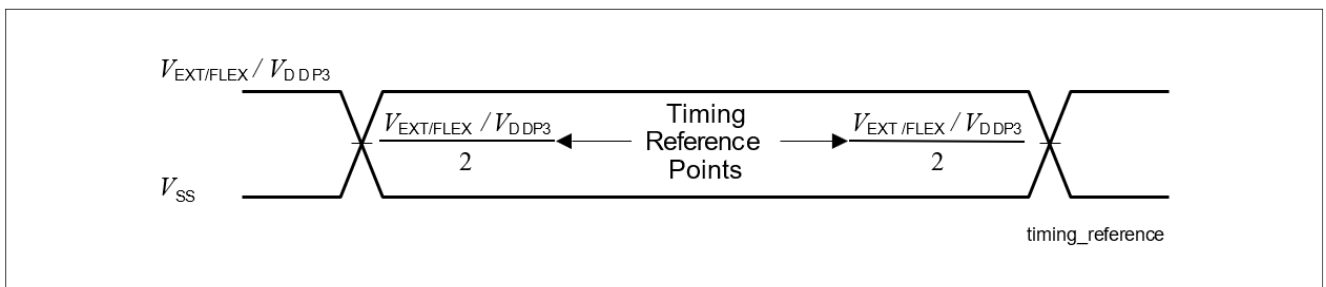


图 3-9 时间基准点定义

电气规格 JTAG 参数

3.19 JTAG参数

以下参数适用于通过 JTAG 调试接口进行通信。JTAG模块完全符合IEEE1149.1-2000。

表 3-38 JTAG

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	50	-	-	ns	
TCK high time	t_2 SR	10	-	-	ns	
TCK low time	t_3 SR	10	-	-	ns	
TCK clock rise time	t_4 SR	-	-	4	ns	
TCK clock fall time	t_5 SR	-	-	4	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6.0	-	-	ns	
TDI/TMS hold after TCK rising edge	t_7 SR	6.0	-	-	ns	
TDO valid after TCK falling edge (propagation delay)	t_8 CC	3.0	-	-	ns	$C_L \leq 20\text{pF}$
		-	-	25	ns	$C_L \leq 50\text{pF}$
TDO hold after TCK falling edge	t_{18} CC	2	-	-	ns	
TDO high impedance to valid from TCK falling edge	t_9 CC	-	-	25	ns	$C_L \leq 50\text{pF}$
TDO valid output to high impedance from TCK falling edge	t_{10} CC	-	-	25	ns	$C_L \leq 50\text{pF}$

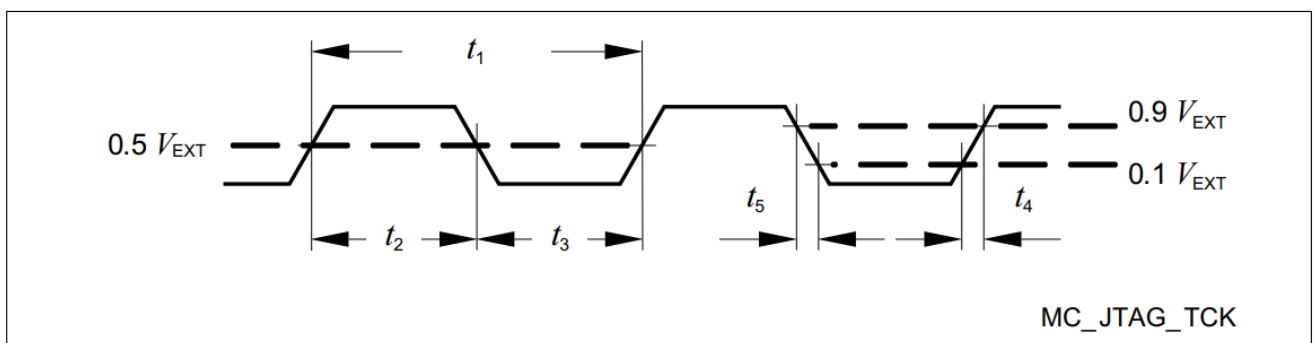


图3-10 测试时钟时序 (TCK)

电气规格 JTAG 参数

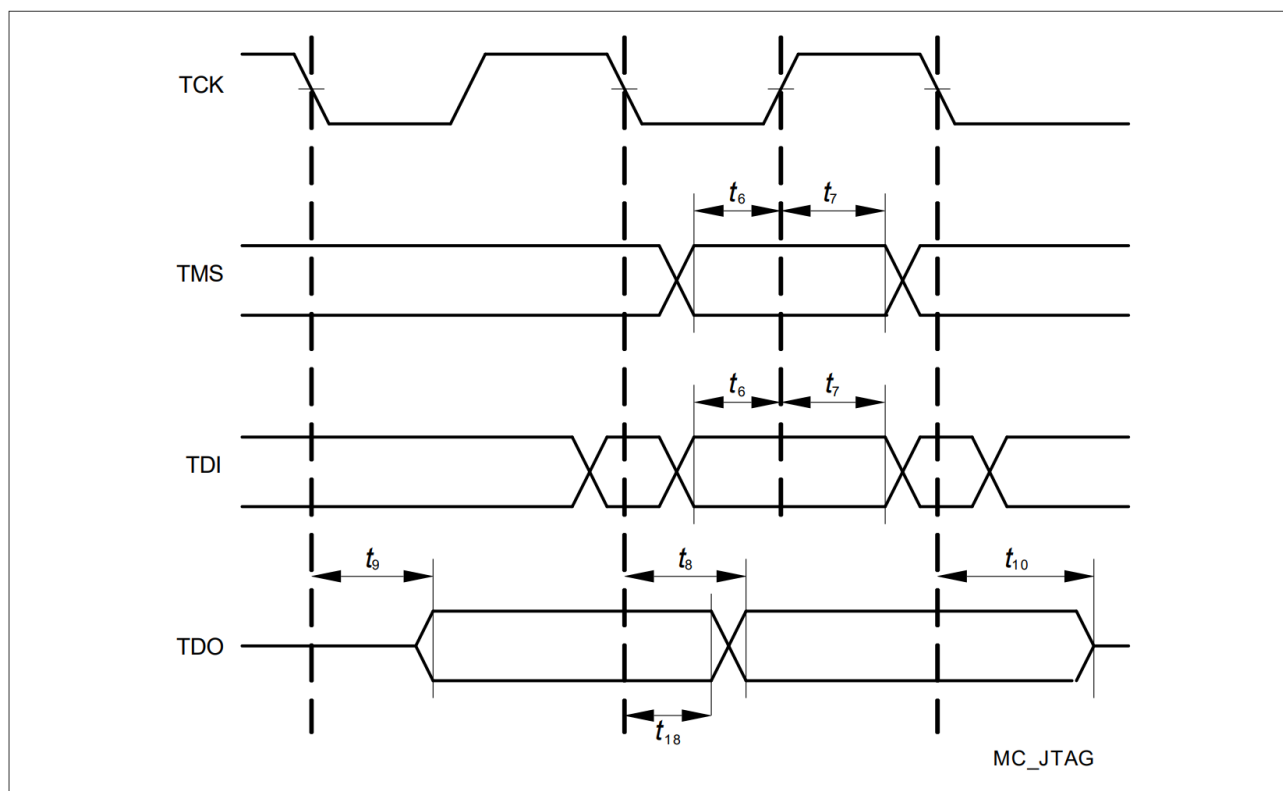


图 3-11 JTAG 时序

电气规格 DAP 参数

3.20 DAP 参数

以下参数适用于通过 DAP 调试接口进行通信。

表 3-39 DAP

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock rise time	t_{14} SR	-	-	1	ns	f=160MHz
		-	-	4	ns	f=40MHz
		-	-	2	ns	f=80MHz
DAP0 clock fall time	t_{15} SR	-	-	1	ns	f=160MHz
		-	-	4	ns	f=40MHz
		-	-	2	ns	f=80MHz
DAP1 setup to DAP0 rising edge	t_{16} SR	4	-	-	ns	
		5	-	-	ns	f=40MHz
DAP1 hold after DAP0 rising edge	t_{17} SR	2	-	-	ns	
DAP1 valid per DAP0 clock period	t_{19} CC	4	-	-	ns	$C_L=20\text{pF}$; f=160MHz
		8	-	-	ns	$C_L=20\text{pF}$; f=80MHz
		10	-	-	ns	$C_L=50\text{pF}$; f=40MHz
DAP0 high time	t_{12} SR	2	-	-	ns	
DAP0 low time	t_{13} SR	2	-	-	ns	
DAP0 clock period	t_{11} SR	6.25	-	-	ns	

表 3-40 SCR DAP

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock rise time	t_{14} SR	-	-	8	ns	f=20MHz
DAP0 clock fall time	t_{15} SR	-	-	8	ns	f=20MHz
DAP1 setup to DAP0 rising edge	t_{16} SR	10	-	-	ns	
DAP1 hold after DAP0 rising edge	t_{17} SR	10	-	-	ns	
DAP1 valid per DAP0 clock period	t_{19} CC	30	-	-	ns	$C_L=20\text{pF}$; f=20MHz
DAP0 high time	t_{12} SR	15	-	-	ns	
DAP0 low time	t_{13} SR	15	-	-	ns	
DAP0 clock period	t_{11} SR	50	-	-	ns	

电气规格 DAP 参数

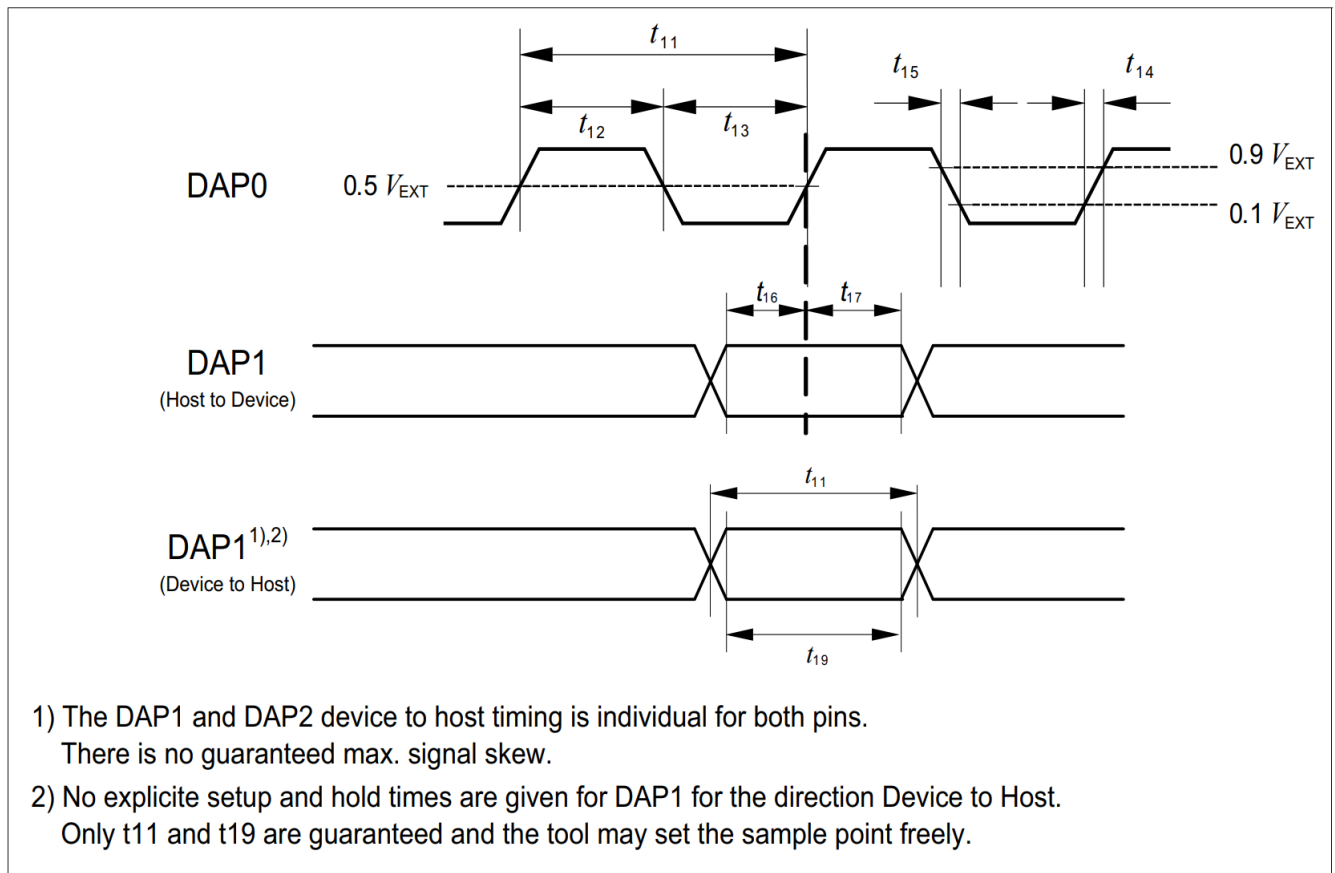


图 3-12 DAP 时序

注释: DAP1 和 DAP2 器件对主控制器器件的两个引脚都是单独的。没有确定的信号最大偏差。

电气规格 ASCLIN SPI 主时序

3.21 ASCLIN SPI 主时序

本节定义了 TC37x 中 ASCLIN 的时序。

注释：焊盘不对称已包含在以下计时中。

表 3-41 主模式强尖锐 (ss) 输出焊盘

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ASCLKO clock period	$t_{50} \text{ CC}$	20	-	-	ns	$C_L=25\text{pF}$
Deviation from ideal duty cycle	$t_{500} \text{ CC}$	-2	-	2	ns	$C_L=25\text{pF}$
MTSR delay from ASCLKO shifting edge	$t_{51} \text{ CC}$	-3.5	-	3.5	ns	$C_L=25\text{pF}$
ASLSON delay from the first ASCLKO edge	$t_{510} \text{ CC}$	-3	-	3.5	ns	$C_L=25\text{pF}$
MRST setup to ASCLKO latching edge	$t_{52} \text{ SR}$	25	-	-	ns	$C_L=25\text{pF}$
MRST hold from ASCLKO latching edge	$t_{53} \text{ SR}$	-2	-	-	ns	$C_L=25\text{pF}$

表 3-42 主模式强中型 (sm) 输出焊盘

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ASCLKO clock period	$t_{50} \text{ CC}$	50	-	-	ns	$C_L=50\text{pF}$
Deviation from ideal duty cycle	$t_{500} \text{ CC}$	-5	-	5	ns	$C_L=50\text{pF}$
MTSR delay from ASCLKO shifting edge	$t_{51} \text{ CC}$	-7	-	7	ns	$C_L=50\text{pF}$
ASLSON delay from the first ASCLKO edge	$t_{510} \text{ CC}$	-7	-	7	ns	$C_L=50\text{pF}$
MRST setup to ASCLKO latching edge	$t_{52} \text{ SR}$	35	-	-	ns	$C_L=50\text{pF}$
MRST hold from ASCLKO latching edge	$t_{53} \text{ SR}$	-5	-	-	ns	$C_L=50\text{pF}$

表 3-43 主模式中型 (m) 输出焊盘

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ASCLKO clock period	$t_{50} \text{ CC}$	160	-	-	ns	$C_L=50\text{pF}$
Deviation from ideal duty cycle	$t_{500} \text{ CC}$	-10	-	10	ns	$C_L=50\text{pF}$
MTSR delay from ASCLKO shifting edge	$t_{51} \text{ CC}$	-20	-	20	ns	$C_L=50\text{pF}$
ASLSON delay from the first ASCLKO edge	$t_{510} \text{ CC}$	-20	-	20	ns	$C_L=50\text{pF}$

电气规格 ASCLIN SPI 主时序

表 3-43 主模式中型 (m) 输出焊盘 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MRST setup to ASCLKO latching edge	t_{52} SR	80	-	-	ns	$C_L=50\text{pF}$
MRST hold from ASCLKO latching edge	t_{53} SR	-15	-	-	ns	$C_L=50\text{pF}$

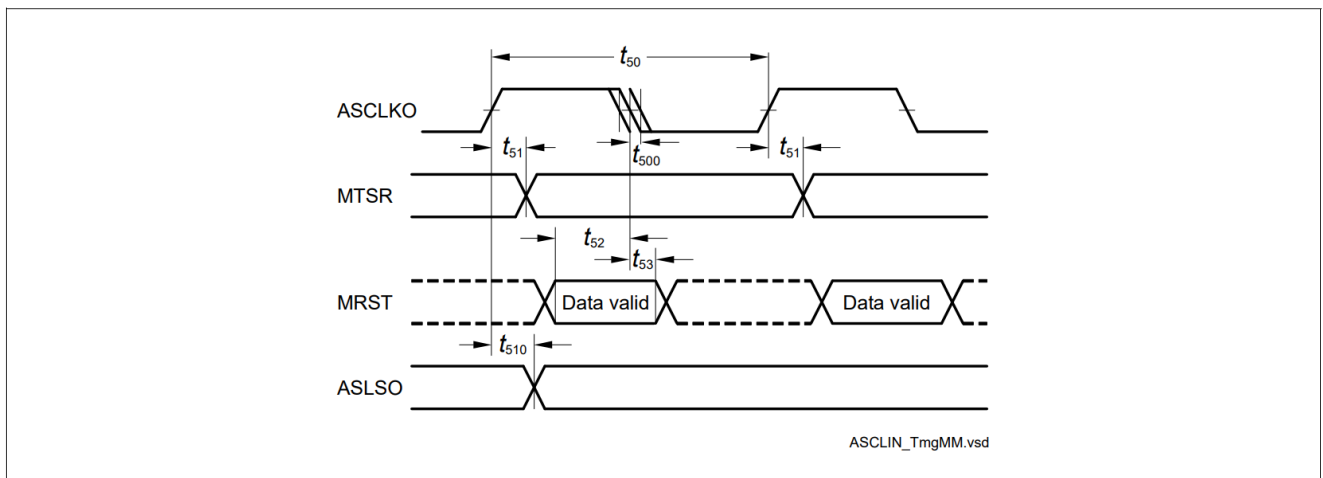


图 3-13 ASCLIN SPI 主机时序

电气规格 QSPI 时序、主从模式

3.22 QSPI 时序、主模式和从模式

本节定义了 TC37x 中 QSPI 的时序。

假设 SCLKO、MTSR 和 SLISO 焊盘具有相同的焊盘设置：

注释：焊盘不对称已包含在以下时序中。

表 3-44 主模式时序，LVDS 数据和时钟输出焊盘

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period	$t_{50\text{ CC}}$	20 ¹⁾	-	-	ns	CL=25pF
Deviation from the ideal duty cycle	$t_{500\text{ CC}}$	-1 ¹⁾	-	1 ¹⁾	ns	CL=25pF
MTSR delay from SCLKO shifting edge	$t_{51\text{ CC}}$	-3 ¹⁾	-	4 ¹⁾	ns	CL=25pF
SLSON deviation from the ideal programmed position	$t_{510\text{ CC}}$	-4 ¹⁾	-	5.5 ¹⁾	ns	$C_L=25\text{pF}$, driver strength ss
		-10 ¹⁾	-	10 ¹⁾	ns	$C_L=25\text{pF}$, driver strength sm
		-30 ¹⁾	-	30 ¹⁾	ns	$C_L=25\text{pF}$, driver strength m
MRST setup to SCLK latching edge	$t_{52\text{ SR}}$	18 ¹⁾	-	-	ns	CL=25pF; valid for LVDS Input pads of QSPI2 only
		19.5 ¹⁾	-	-	ns	CL=25pF; valid for LVDS Input pads of QSPI4 only
MRST hold from SCLK latching edge	$t_{53\text{ SR}}$	-1 ¹⁾	-	-	ns	CL=25pF; valid for LVDS Input pads only

1) 条件列表中定义的负载（ $C_L=25\text{pF}$ ）是针对单端信号 SLISO 的负载定义，并不旨在在差分信号线内添加额外负载。对于单端信号，负载定义定义了 PCB 布局上信号的最大长度。对于 LVDS 焊盘，适用 IEEE Std 1596.3-1996 负载定义。

表 3-45 主模式强尖锐（ss）输出焊盘

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period	$t_{50\text{ CC}}$	50	-	-	ns	CL=25pF
Deviation from the ideal duty cycle	$t_{500\text{ CC}}$	-2	-	2	ns	CL=25pF
MTSR delay from SCLKO shifting edge	$t_{51\text{ CC}}$	-4	-	5	ns	CL=25pF
SLSON deviation from the ideal programmed position	$t_{510\text{ CC}}$	-4	-	5	ns	CL=25pF
MRST setup to SCLK latching edge	$t_{52\text{ SR}}$	25 ^{1) 2)}	-	-	ns	CL=25pF
MRST hold from SCLK latching edge	$t_{53\text{ SR}}$	-2 ^{1) 2)}	-	-	ns	CL=25pF

电气规格 QSPI 时序、主从模式

- 1) 为了补偿平均片上延迟, QSPI 模块提供了位域 ECONZ.A、B 和 C。
- 2) 建立和保持时间对于输入垫阈值的两种设置均有效: TTL 和 AL。

表 3-46 主模式强中型 (sm) 输出焊盘

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period	$t_{50} \text{ CC}$	50	-	-	ns	CL=50pF
Deviation from the ideal duty cycle	$t_{500} \text{ CC}$	-5	-	5	ns	CL=50pF
MTSR delay from SCLKO shifting edge	$t_{51} \text{ CC}$	-7	-	7	ns	CL=50pF
SLSON deviation from the ideal programmed position	$t_{510} \text{ CC}$	-7	-	7	ns	CL=50pF
MRST setup to SCLK latching edge	$t_{52} \text{ SR}$	35 ^{1) 2)}	-	-	ns	CL=50pF
MRST hold from SCLK latching edge	$t_{53} \text{ SR}$	-5 ^{1) 2)}	-	-	ns	CL=50pF

- 1) 为了补偿平均片上延迟, QSPI 模块提供了位域 ECONZ.A、B 和 C。
- 2) 建立和保持时间对于输入焊盘阈值的两种设置均有效: TTL 和 AL。

表 3-47 主模式中等 (m) 输出焊盘

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period	$t_{50} \text{ CC}$	160	-	-	ns	CL=50pF
Deviation from the ideal duty cycle	$t_{500} \text{ CC}$	-10	-	10	ns	CL=50pF
MTSR delay from SCLKO shifting edge	$t_{51} \text{ CC}$	-20	-	20	ns	CL=50pF
SLSON deviation from the ideal programmed position	$t_{510} \text{ CC}$	-20	-	20	ns	CL=50pF
MRST setup to SCLK latching edge	$t_{52} \text{ SR}$	80 ^{1) 2)}	-	-	ns	CL=50pF
MRST hold from SCLK latching edge	$t_{53} \text{ SR}$	-15 ^{1) 2)}	-	-	ns	CL=50pF
		-13 ^{1) 2)}	-	-	ns	CL=50pF; SCR SSC

- 1) 为了补偿平均片上延迟, QSPI 模块提供了位域 ECONZ.A、B 和 C。
- 2) 建立和保持时间对于输入焊盘阈值的两种设置均有效: TTL 和 AL。

表 3-48 从模式时序

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLK clock period	$t_{54} \text{ SR}$	4 x T_{MAX}	-	-	ns	
SCLK duty cycle	$t_{55/t54} \text{ SR}$	40	-	60	%	

电气规格 QSPI 时序、主从模式

表 3-48 从模式时序 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MTSR setup to SCLK latching edge	t_{56} SR	6	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
MTSR hold from SCLK latching edge	t_{57} SR	4	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
SLSI setup to first SCLK shift edge	t_{58} SR	4	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
SLSI hold from last SCLK latching edge	t_{59} SR	3	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
MRST delay from SCLK shift edge	t_{60} CC	5	-	35	ns	driver = strong edge = medium ; $C_L=50\text{pF}$
		2	-	24	ns	driver = strong edge = sharp ; $C_L=50\text{pF}$
		15	-	80	ns	medium driver ; $C_L=50\text{pF}$
		14	-	-	ns	medium driver ; $C_L=50\text{pF}$; SCR SSC

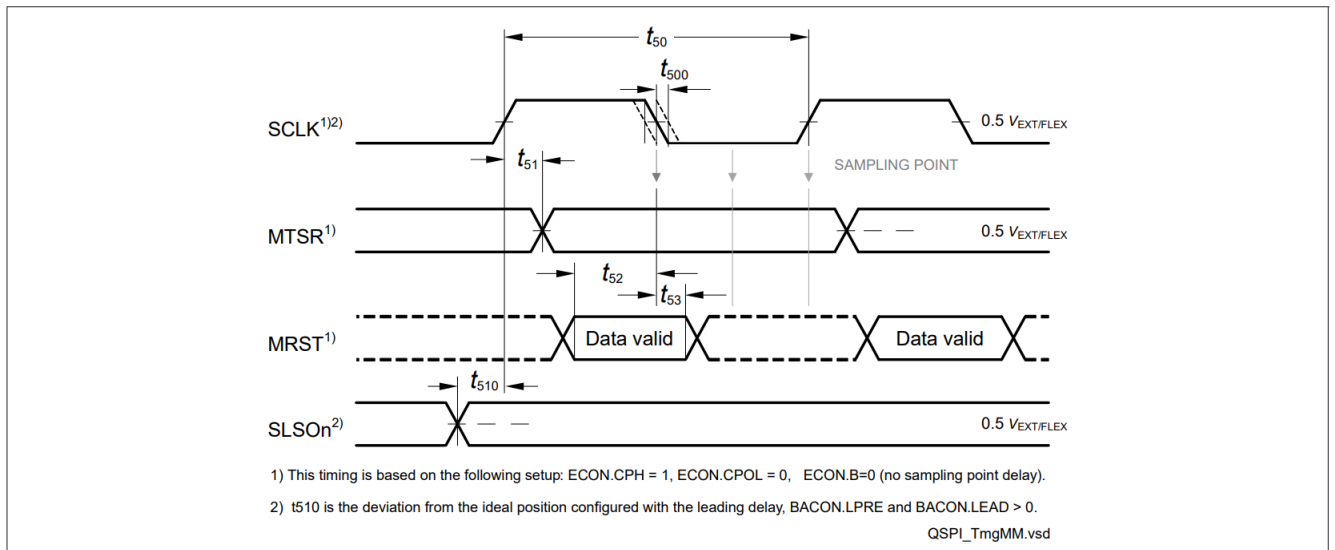


图 3-14 主模式时序

电气规格 QSPI 时序、主从模式

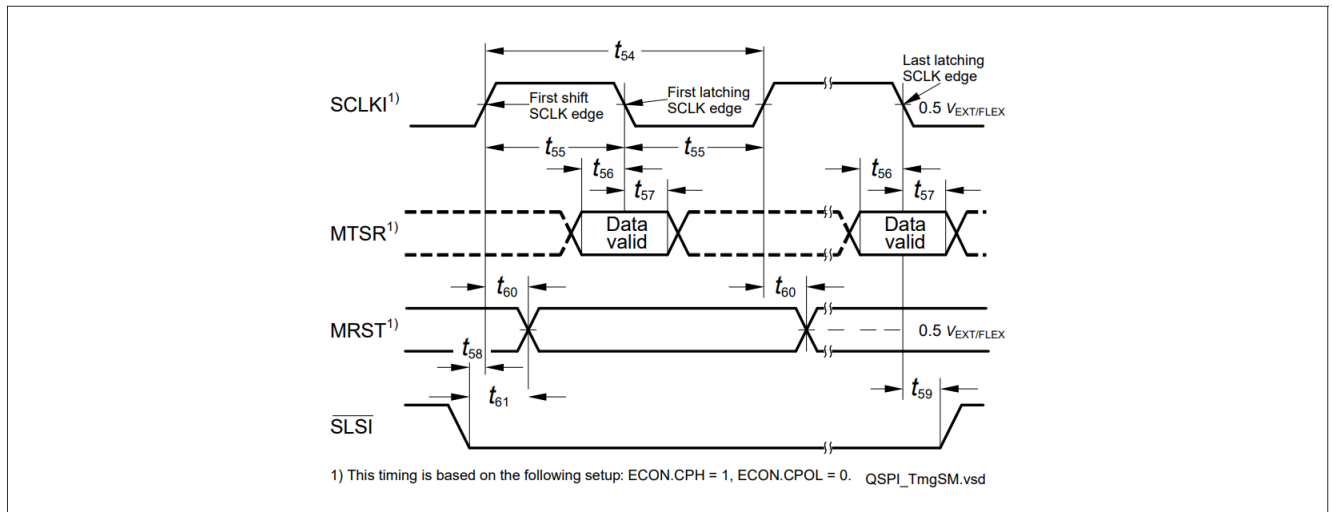


图3-15 从模式时序

电气规格 MSC 时序 5 V 操作

3.23 MSC时序 5 V 操作

以下部分定义了时间。

注释：焊盘不对称已包含在以下时序中。

注释：LVDS焊盘的负载在下列时序中定义为差分负载。

表 3-49 5V下的LVDS 时钟/数据（LVDS 模式下的 LVDS 焊盘）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FCLPx clock period	$t_{40\text{ CC}}$	$2 * T_{A1) 2) 3)}$	-	-	ns	LVDS; $C_L=50\text{pF}$
Deviation from ideal duty cycle	$t_{400\text{ CC}}$	-1 ³⁾	-	1 ³⁾	ns	LVDS; $0 < C_L < 50\text{pF}$
SOPx output delay	$t_{44\text{ CC}}$	-3 ³⁾	-	3 ³⁾	ns	$C_L=50\text{pF}$
ENx output delay	$t_{45\text{ CC}}$	-4 ³⁾	-	5 ³⁾	ns	ss; $C_L=50\text{pF}$; ABRA block bypassed
		-4 ³⁾	-	4 ³⁾	ns	ss; $C_L=50\text{pF}$; ABRA block used
		-2 ³⁾	-	10 ³⁾	ns	sm; $C_L=50\text{pF}$
		-30 ³⁾	-	30 ³⁾	ns	m; $C_L=50\text{pF}$

1) T_A 取决于为MSC的 ABRA 功能块中的波特率生成选择的时钟源。

2) LVDS引脚上的容性负载是差分的，CMOS 引脚上的容性负载是单端的。

3) 条件列表中定义的负载（ $C_L=50\text{pF}$ ）是针对单端信号 EN 的负载定义，并不旨在在差分信号线内添加额外负载。对于单端信号，负载定义定义了 PCB 布局上信号的最大长度。对于 LVDS 焊盘，适用 IEEE Std 1596.3-1996 负载定义。

表 3-50 5V下的强尖锐（ss）时钟/数据驱动器

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FCLPx clock period	$t_{40\text{ CC}}$	$2 * T_A$	-	-	ns	$C_L=50\text{pF}$
Deviation from ideal duty cycle	$t_{400\text{ CC}}$	-2	-	2	ns	$C_L=50\text{pF}$
SOPx output delay	$t_{44\text{ CC}}$	-4	-	3.5	ns	$C_L=50\text{pF}$
ENx output delay	$t_{45\text{ CC}}$	-4	-	3.5	ns	$C_L=50\text{pF}$

表 3-51 5V下的强中型（sm）时钟/数据驱动器

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FCLPx clock period	$t_{40\text{ CC}}$	$2 * T_A$	-	-	ns	$C_L=50\text{pF}$
Deviation from ideal duty cycle	$t_{400\text{ CC}}$	-5	-	5	ns	$C_L=50\text{pF}$
SOPx output delay	$t_{44\text{ CC}}$	-7	-	7	ns	$C_L=50\text{pF}$
ENx output delay	$t_{45\text{ CC}}$	-7	-	7	ns	$C_L=50\text{pF}$

电气规格 MSC 时序 5 V 操作

表 3-52 5V下的中等（m）时钟/数据驱动器

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FCLPx clock period	t_{40} CC	$2 * T_A$	-	-	ns	CL=50pF
Deviation from ideal duty cycle	t_{400} CC	-10	-	10	ns	CL=50pF
SOPx output delay	t_{44} CC	-20	-	20	ns	CL=50pF
ENx output delay	t_{45} CC	-20	-	20	ns	CL=50pF

表 3-53 上行接口

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SDI bit time	t_{46} SR	$8 * t_{MSC}$	-	-	ns	
SDI rise time	t_{48} SR	-	-	200	ns	
SDI fall time	t_{49} SR	-	-	200	ns	

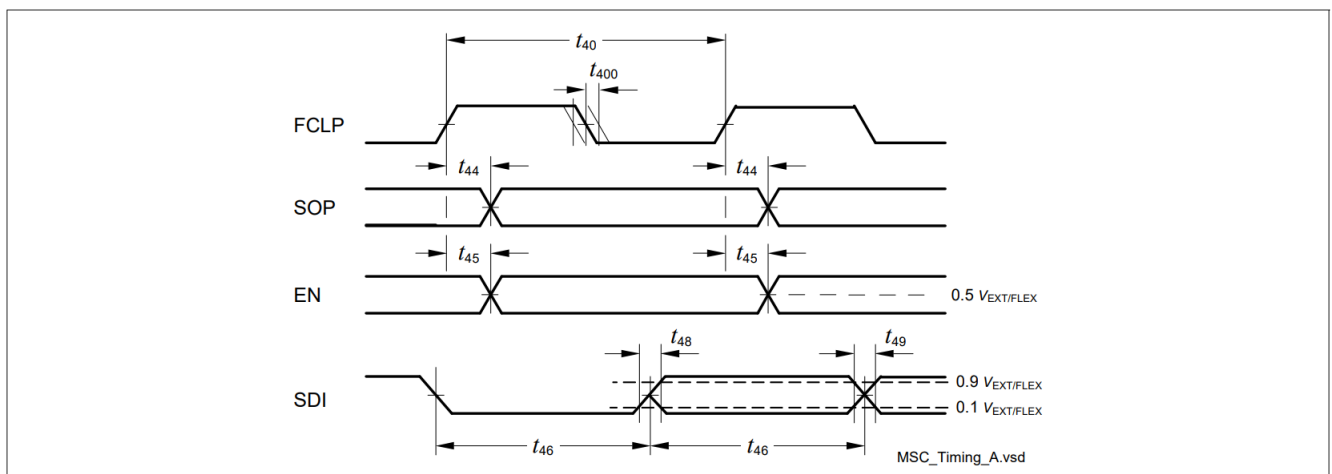


图 3-16 MSC 接口时序

注释：SOP数据信号是在目标器件中的FCLP的下降沿进行采样的。

电气规格 以太网接口 (ETH) 特性

3.24 以太网接口 (ETH) 特性

3.24.1 ETH 测量参考点

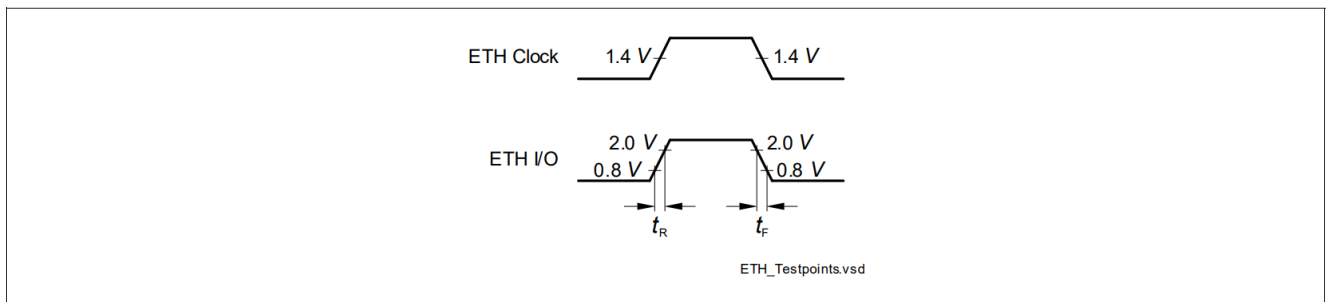


图 3-17 ETH 测量参考点

电气规格 以太网接口 (ETH) 特性

3.24.2 ETH管理信号参数 (ETH_MDC、ETH_MDIO)

表 3-54 适用于3.3V 的 ETH 管理信号参数

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ETH_MDC period	t_1 CC	400	-	-	ns	CL=25pF
ETH_MDC high time	t_2 CC	160	-	-	ns	CL=25pF
ETH_MDC low time	t_3 CC	160	-	-	ns	CL=25pF
ETH_MDIO setup time (output)	t_4 CC	10	-	-	ns	CL=25pF
ETH_MDIO hold time (output)	t_5 CC	10	-	-	ns	CL=25pF
ETH_MDIO data valid (input)	t_6 SR	0	-	300	ns	CL=25pF

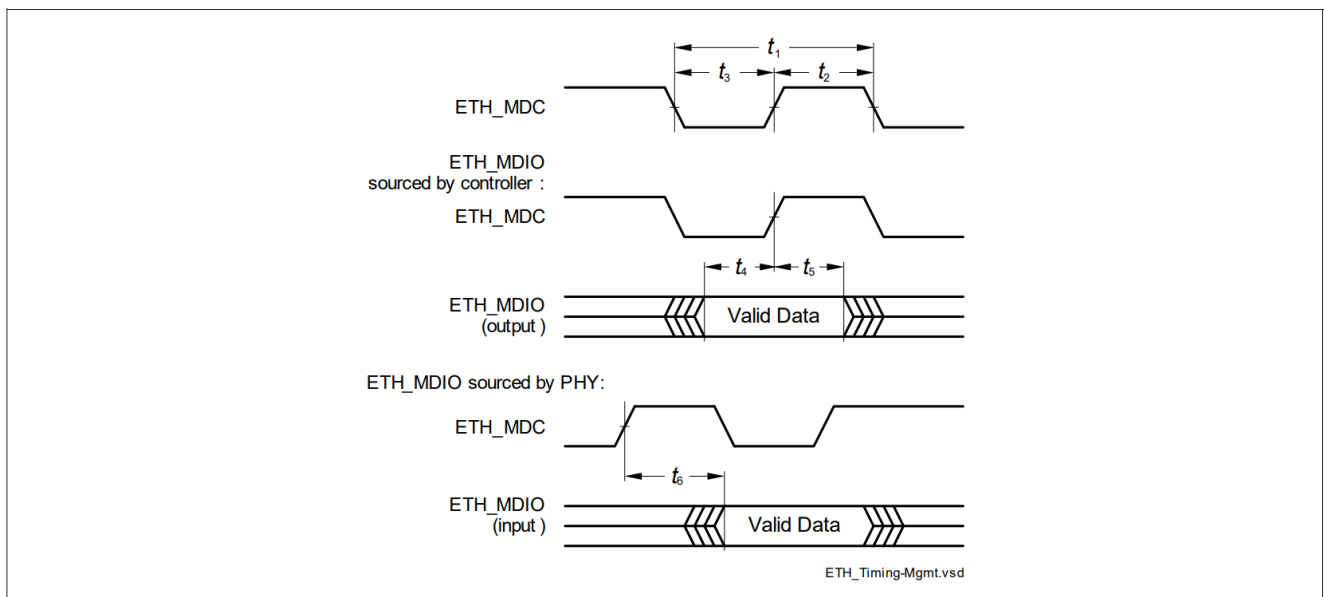


图 3-18 ETH 管理信号时序

电气规格 以太网接口 (ETH) 特性

3.24.3 ETH MII 参数

下面介绍MII（媒体独立接口）的参数。

表 3-55 ETH MII 信号时序参数

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_7 SR	-	40	-	ns	CL=25pF ; baudrate=100Mbps
		-	400	-	ns	CL=25pF ; baudrate=10Mbps
Clock high time	t_8 SR	14	-	26	ns	CL=25pF ; baudrate=100Mbps
		140 ¹⁾	-	260 ²⁾	ns	CL=25pF ; baudrate=10Mbps
Clock low time	t_9 SR	14	-	26	ns	CL=25pF ; baudrate=100Mbps
		140 ¹⁾	-	260 ²⁾	ns	CL=25pF ; baudrate=10Mbps
Input setup time	t_{10} SR	10	-	-	ns	CL=25pF
Input hold time	t_{11} SR	10	-	-	ns	CL=25pF
Output valid time	t_{12} CC	0	-	25	ns	CL=25pF

1) 按时钟周期的 35% 定义。

2) 按时钟周期的 65% 定义。

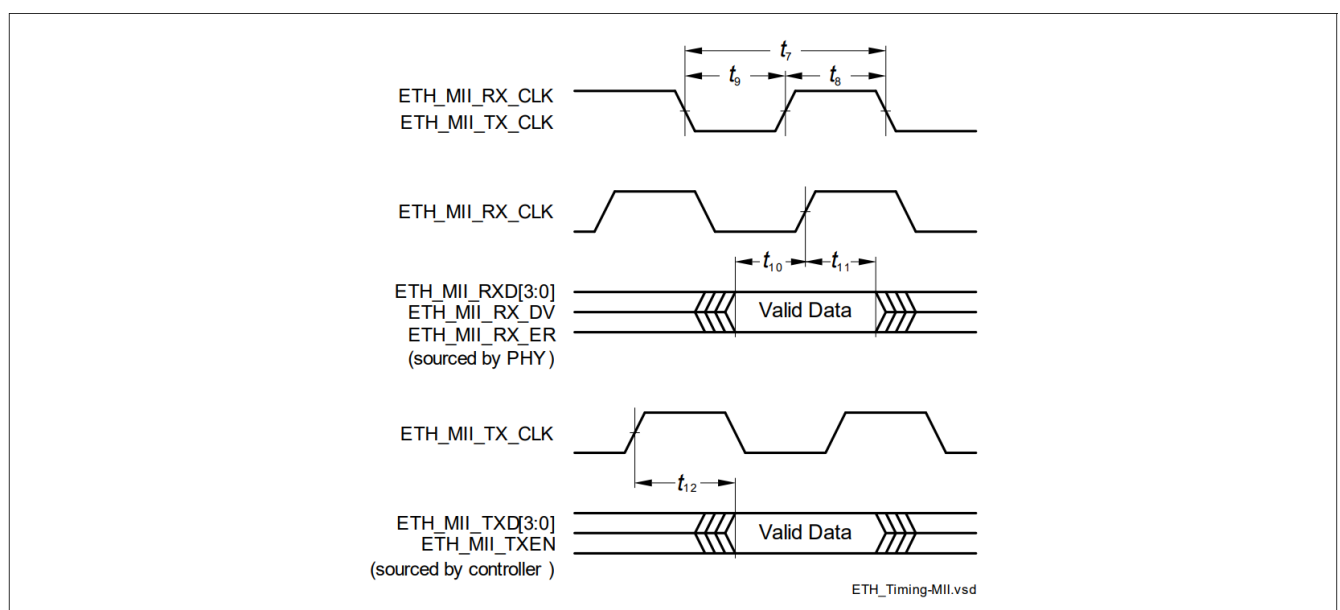


图 3-19 ETH MII 信号时序

电气规格 以太网接口 (ETH) 特性

3.24.4 ETH RMII 参数

下面介绍RMII（精简媒体独立接口）的参数。

表 3-56 适用于3.3V的ETH RMII 信号时序参数

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ETH_RMII_REF_CL clock period	t_{13} SR	-	20	-	ns	50ppm ; CL=25pF
ETH_RMII_REF_CL clock high time	t_{14} SR	7 ¹⁾	-	13 ²⁾	ns	CL=25pF
ETH_RMII_REF_CL clock low time	t_{15} SR	7 ¹⁾	-	13 ²⁾	ns	CL=25pF
ETHTXEN, ETHTXD[1:0], ETHRXD[1:0], ETHCRSDV; setup time ³⁾	t_{16} CC	4	-	-	ns	CL=25pF
ETHTXEN, ETHTXD[1:0], ETHRXD[1:0], ETHCRSDV; hold time ³⁾	t_{17} CC	2	-	-	ns	CL=25pF

- 1) 按时钟周期的 35% 定义。
- 2) 按时钟周期的 65% 定义。
- 3) 对于 ETHRXD 和 ETHCRSDV 信号，此参数是 SR。

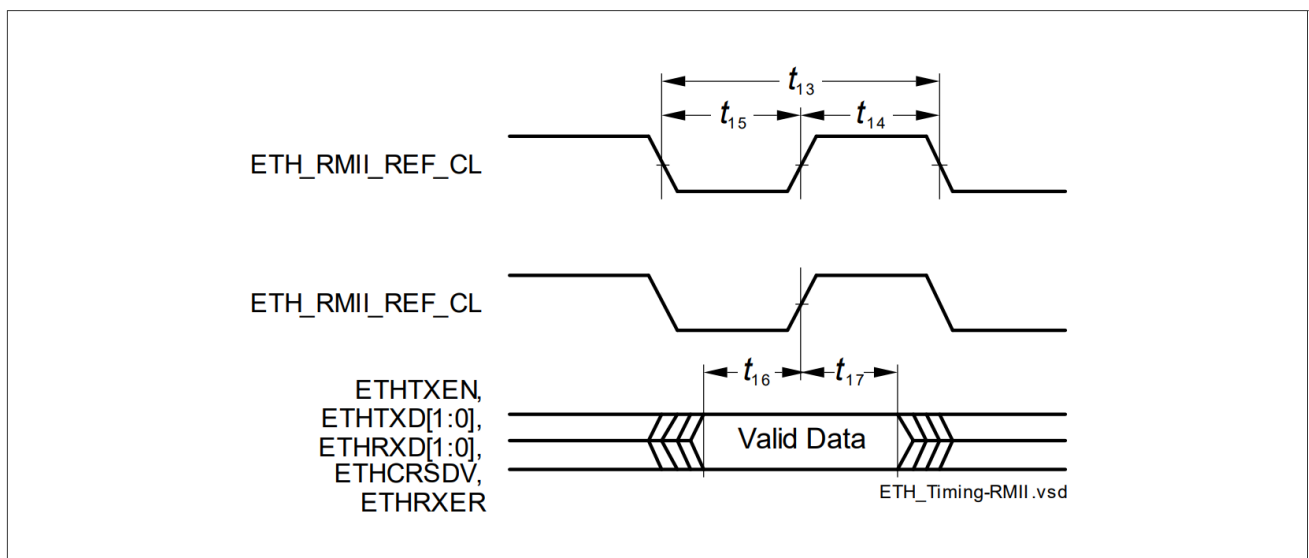


图 3-20 ETH RMII 信号时序

电气规格 以太网接口 (ETH) 特性

3.24.5 ETH RGMII 参数

下面介绍RGMII的参数。

表 3-57 适用于3.3V的ETH RGMII 信号时序参数

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TX Clock period	$t_{19\text{CC}}$	36	40	44	ns	100Mbps
		360	400	440	ns	10Mbps
		7.2	8	8.8	ns	Gigabit
Data to Clock Output skew	$t_{20\text{CC}}$	-500	0	500	ps	
Data to Clock input skew (at receiver)	$t_{21\text{SR}}$	1	1.8	2.6	ns	
Clock duty cycle	t_{dutyCC}	40	50	60	%	10/100Mbps
		45	50	55	%	Gigabit
GREFCLK duty cycle	$t_{\text{duty_inSR}}$	45	-	55	%	
GREFCLK Input accuracy	$ACC\text{SR}$	-0.005	-	0.005	%	

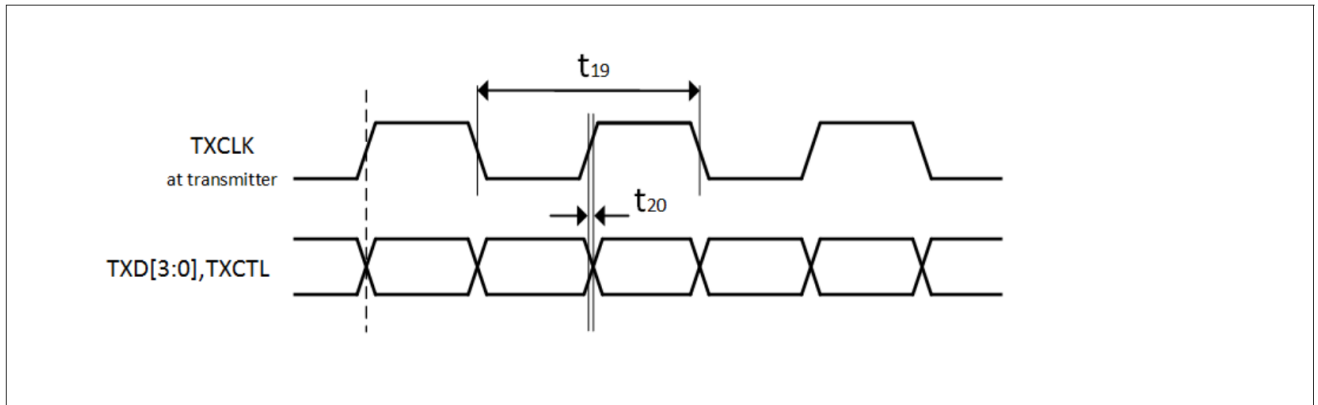


图 3-21 ETH RGMII TX 信号时序（目的地延迟 (DoD)）

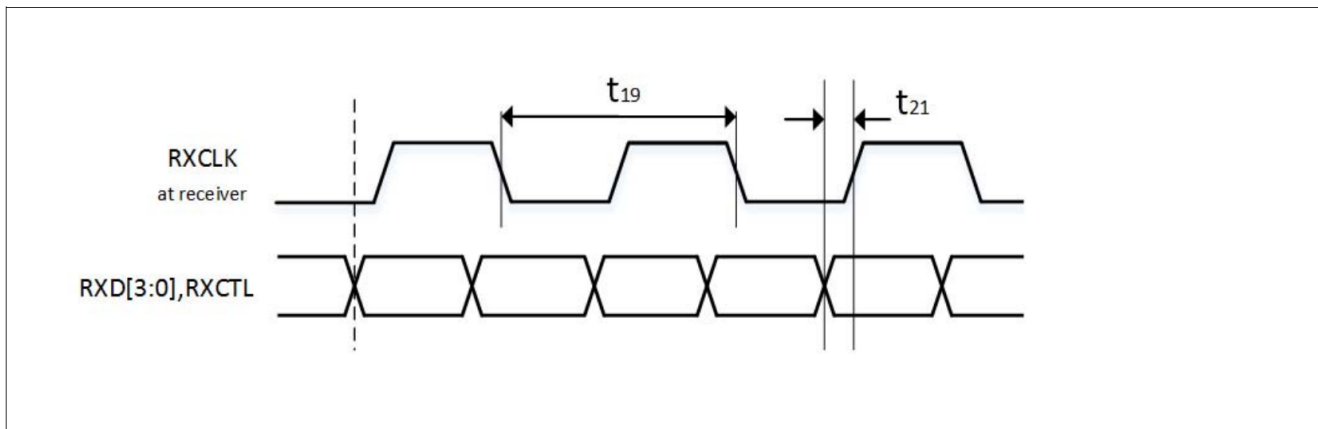


图 3-22 ETH RGMII RX 信号时序（源延迟 (DoS)）

电气规格 E-Ray 参数

3.25 E-Ray 参数

本节的时间安排适用于 $C_L = 25 \text{ pF}$ 的输出驱动器的强驱动器和锐边设置。

表 3-58 发送参数

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise time of TxEN	$t_{\text{dCCTxENRise25 CC}}$	-	-	9	ns	$C_L=25\text{pF}$
Fall time of TxEN	$t_{\text{dCCTxENFall25 CC}}$	-	-	9	ns	$C_L=25\text{pF}$
Sum of rise and fall time	$t_{\text{dCCTxRise25+ dCCTxFall25 CC}}$	-	-	9	ns	20% - 80% ; $C_L=25\text{pF}$
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, rising edge of TxEN	$t_{\text{dCCTxEN01 CC}}$	-	-	25	ns	
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, falling edge of TxEN	$t_{\text{dCCTxEN10 CC}}$	-	-	25	ns	
Asymmetry of sending	$t_{\text{tx_asym CC}}$	-2.45	-	2.45	ns	$C_L=25\text{pF}$
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, rising edge of TxD	$t_{\text{dCCTxD01 CC}}$	-	-	25	ns	
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, falling edge of TxD	$t_{\text{dCCTxD10 CC}}$	-	-	25	ns	
TxD signal sum of rise and fall time at TP1_BD	$t_{\text{txd_sum CC}}$	-	-	9	ns	

表 3-59 接收参数

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Acceptance of asymmetry at receiving part	$t_{\text{dCCTxAsymAcc ept25 SR}}$	-30.5	-	43.0	ns	$C_L=25\text{pF}$
Acceptance of asymmetry at receiving part	$t_{\text{dCCTxAsymAcc ept15 SR}}$	-31.5	-	44.0	ns	$C_L=15\text{pF}$
Threshold for detecting logical high	$T_{\text{uCCLogic1 SR}}$	35	-	70	%	
Threshold for detecting logical low	$T_{\text{uCCLogic0 SR}}$	30	-	65	%	

电气规格 E-Ray 参数

表 3-59 接收参数 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Sum of delay between TP4_CC and TP4_FF and delays derived from TP4_FFi, rising edge of RxD	$t_{dCCRxD01}$ CC	-	-	10	ns	
Sum of delay between TP4_CC and TP4_FF and delays derived from TP4_FFi, falling edge of RxD	$t_{dCCRxD10}$ CC	-	-	10	ns	

电气规格 HSCT 参数

3.26 HSCT 参数

表 3-60 HSCT - Rx 寄生参数和负载

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Capacitance total budget	C_{total} CC	-	3.5	5	pF	Total Budget for complete receiver including silicon, package, pins and bond wire
Parasitic inductance budget	H_{total} CC	-	5	-	nH	

表 3-61 HSCT - Rx/Tx 设置时序

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RX o/p duty cycle	DC_{rx} CC	40	-	60	%	
Disable time of the LVDS pad	$t_{LVDS\text{DIS}}$ CC	-	-	20	ns	
Enable time of the LVDS pad	$t_{LVDS\text{SEN}}$ CC	-	-	400	ns	
Wakeup time from Sleep Mode	t_{SWU} CC	-	-	250	ns	
Maximum length of a wake-up glitch that does not wake-up the receiver	t_{WUP} CC	-	-	0.2	ns	
Bias startup time	t_{bias} CC	-	5	10	μs	Bias distributor waking up from power down and provide stable Bias.
RX startup time	t_{rxl} CC	-	-	600	ns	Wake-up RX from power down.
TX startup time	t_{tx} CC	-	-	280	ns	Wake-up TX from power down.

电气规范 IC 间 (I2C) 接口时序

3.27 Inter-IC (I2C) 接口时序

本节定义了 TC37x 中 I2C 的时序。

所有 I2C 时序参数均为主模式的 SR 和从模式的 CC。

表 3-62 I2C 标准模式时序

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1	-	-	300	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Capacitive load for each bus line	C_b SR	-	-	400	pF	
Bus free time between a STOP and ATART condition	t_{10}	4.7	-	-	μs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Rise time of both SDA and SCL	t_2	-	-	1000	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Data hold time	t_3	0	-	-	μs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Data set-up time	t_4	250	-	-	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Low period of SCL clock	t_5	4.7	-	-	μs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
High period of SCL clock	t_6	4	-	-	μs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Hold time for the (repeated) START condition	t_7	4	-	-	μs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line

电气规范 IC 间 (I2C) 接口时序

表 3-62 I2C 标准模式时序 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Set-up time for (repeated) START condition	t_8	4.7	-	-	μs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Set-up time for STOP condition	t_9	4	-	-	μs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line

表 3-63 I2C 快速模式时序

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1	$20+0.1 \cdot C_b$	-	300	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Capacitive load for each bus line	C_b SR	-	-	400	pF	
Bus free time between a STOP and ATART condition	t_{10}	1.3	-	-	μs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Rise time of both SDA and SCL	t_2	$20+0.1 \cdot C_b$	-	300	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Data hold time	t_3	0	-	-	μs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Data set-up time	t_4	100	-	-	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Low period of SCL clock	t_5	1.3	-	-	μs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
High period of SCL clock	t_6	0.6	-	-	μs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line

电气规范 IC 间 (I2C) 接口时序

表 3-63 I2C 快速模式时序 (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Hold time for the (repeated) START condition	t_7	0.6	-	-	μs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Set-up time for (repeated) START condition	t_8	0.6	-	-	μs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Set-up time for STOP condition	t_9	0.6	-	-	μs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line

表 3-64 I2C 高速模式时序

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Capacitive load for each bus line	C_b SR	-	-	400	pF	
Fall time of SCL	t_{11}	10 ¹⁾	-	40 ¹⁾	ns	bus line load of 100pF
Fall time of SDA	t_{12}	10 ¹⁾	-	80 ¹⁾	ns	bus line load of 100pF
Rise time of SCL	t_{13}	10 ¹⁾	-	40 ¹⁾	ns	bus line load of 100pF
Rise time of SDA	t_{14}	10 ¹⁾	-	80 ¹⁾	ns	bus line load of 100pF
Data hold time	t_3	0 ¹⁾	-	70 ¹⁾	ns	bus line load of 100pF
Data set-up time	t_4	10 ¹⁾	-	-	ns	bus line load of 100pF
Low period of SCL clock	t_5	160 ¹⁾	-	-	ns	bus line load of 100pF
High period of SCL clock	t_6	60 ¹⁾	-	-	ns	bus line load of 100pF
Hold time for the (repeated) START condition	t_7	160 ¹⁾	-	-	ns	bus line load of 100pF
Set-up time for (repeated) START condition	t_8	160 ¹⁾	-	-	ns	bus line load of 100pF
Set-up time for STOP condition	t_9	160 ¹⁾	-	-	ns	bus line load of 100pF

1) 值定义为 $C_b = 100\text{pF}$, 有关 $C_b = 400\text{pF}$ 的时序, 请参阅 I2C 标准。

电气规范 IC 间 (I2C) 接口时序

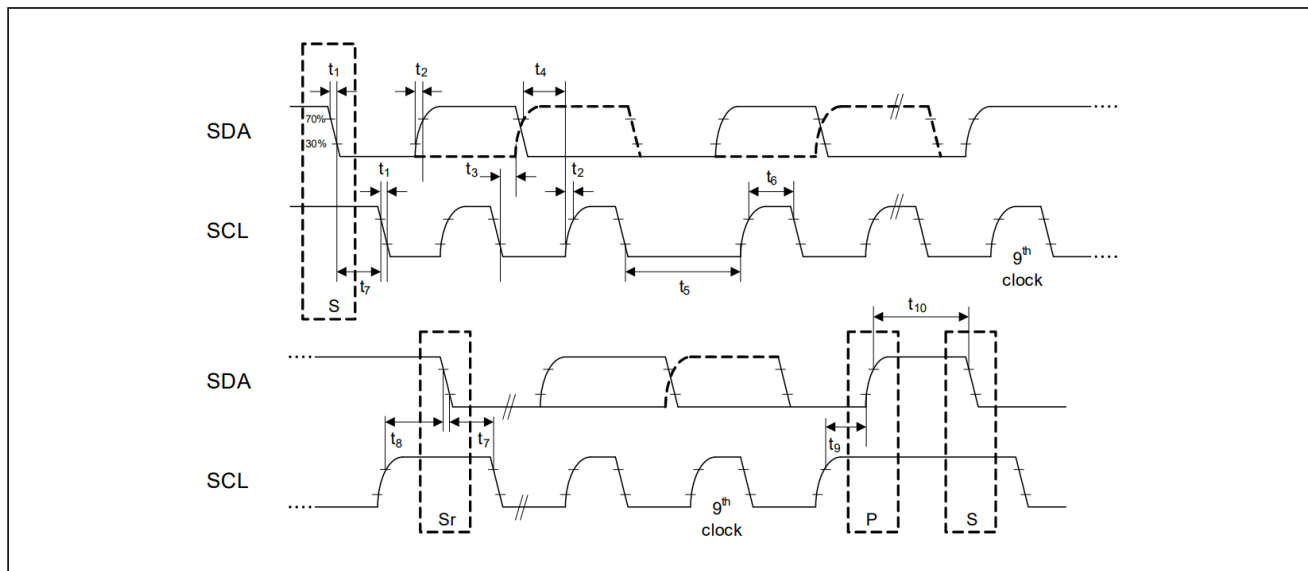


图 3-23 I2C 标准模式和快速模式时序

电气规格 Flash 目标参数

3.28 Flash 目标参数

表 3-65 Flash

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Program Flash Erase Time per logical sector ¹⁾	t_{ERP}^{CC}	-	-	0.5	s	cycle count < 1000
Program Flash Erase Time per Multi-Sector Command ¹⁾	t_{MERP}^{CC}	-	-	0.5	s	For consecutive logical sectors in a physical sector with total range ≤ 512 kByte; cycle count < 1000
Program Flash program time per page in 5 V mode ¹⁾	t_{PRP5}^{CC}	-	-	80	μs	32 Byte
Program Flash program time per page in 3.3 V mode ¹⁾	t_{PRP3}^{CC}	-	-	115	μs	32 Byte
Program Flash program time per burst in 5 V mode ¹⁾	t_{PRPB5}^{CC}	-	-	220	μs	256 Byte
Program Flash program time per burst in 3.3 V mode ¹⁾	t_{PRPB3}^{CC}	-	-	530	μs	256 Byte
Program Flash program time for 1 MByte with burst programming in 3.3 V mode excluding communication ¹⁾	$t_{PRPB3_1MB}^{CC}$	-	-	2.2	s	Derived value for documentation purpose
Program Flash program time for 1 MByte with burst programming in 5 V mode excluding communication ¹⁾	$t_{PRPB5_1MB}^{CC}$	-	-	1	s	Derived value for documentation purpose
Program Flash program time for complete PFlash with burst programming in 5 V mode excluding communication ¹⁾	$t_{PRPB5_PF}^{CC}$	-	-	6	s	Derived value for documentation purpose
Write Page Once adder ¹⁾	t_{ADD}^{CC}	-	-	20	μs	Adder to Program Time when using Write Page Once
Program Flash suspend to read latency ¹⁾	t_{SPNDP}^{CC}	-	-	120	μs	For Write Burst, Verify Erased and for multi-(logical) sector erase commands
Data Flash Erase Disturb Limit (single ended sensing mode)	N_{DFD}^{CC}	-	-	50	cycles	
Data Flash Erase Disturb Limit (complement sensing mode)	N_{DFDC}^{CC}	-	-	500	cycles	
UCB Erase Disturb Limit	N_{UCBD}^{CC}	-	-	500	cycles	

电气规格 Flash 目标参数

表 3-65 Flash (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Program time data flash per page ¹⁾²⁾	t_{PRD}^{CC}	-	-	75	μs	8 Byte
Complete Device Flash Erase Time PFlash and DFlash ^{1)3) 4) 5)}	$t_{ER_Dev}^{CC}$	-	4.3	7	s	Valid for less than 1000 cycles, w/o UCB. Derived value for documentation purpose.
Data Flash program time per burst ¹⁾²⁾	t_{PRDB}^{CC}	-	-	140	μs	32 Byte
Data Flash suspend to read latency ¹⁾	t_{SPNDD}^{CC}	-	-	120	μs	
Wait time after margin change	$t_{FL_MarginDel}^{CC}$	-	-	2	μs	
Program Flash Endurance per Logical Sector	$N_{E_P}^{CC}$	-	-	1000	cycles	Replace logical sector command shall be used if a sector fails during erase or program
Number of erase operations per physical sector in program flash	N_{ERP}^{CC}	-	-	16000	cycles	
Program Flash Retention Time, Sector	t_{RET}^{CC}	20	-	-	years	Max. 1000 erase/program cycles
UCB Retention Time	t_{RTU}^{CC}	20	-	-	years	Max. 100 erase/program cycles per UCB, max 500 erase/program cycles for all UCBs together
Data Flash access delay	t_{DF}^{CC}	-	-	100	ns	see RFLASH of DMU register HF_DWAIT
Data Flash ECC Delay	t_{DFECC}^{CC}	-	-	20	ns	see RECC of DMU register HF_DWAIT
Program Flash access delay	t_{PF}^{CC}	-	-	30	ns	see RFLASH of DMU register HF_PWAIT
Program Flash ECC delay	t_{PFECC}^{CC}	-	-	10	ns	see RECC and CECC of DMU register HF_PWAIT
Number of erase operations on DF0 over lifetime (complement sensing mode) ⁶⁾	N_{ERD0C}^{CC}	-	-	4000000	cycles	
Number of erase operations on DF0 over lifetime (single ended sensing mode) ⁷⁾	N_{ERD0S}^{CC}	-	-	750000	cycles	

电气规格 Flash 目标参数

表 3-65 Flash (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Number of erase operations on DF1 over lifetime (complement sensing mode) ⁶⁾	N_{ERD1C} CC	-	-	2000000	cycles	
Number of erase operations on DF1 over lifetime (single ended sensing mode) ⁷⁾	N_{ERD1S} CC	-	-	500000	cycles	
Data Flash Endurance per EEPROMx sector (complement sensing mode) ⁸⁾	$N_{\text{E_EEP10C}}$ CC	-	-	500000	cycles	Max. data retention time 10 years
DataFlash Endurance per EEPROMx sector (single ended sensing mode) ⁸⁾	$N_{\text{E_EEP10S}}$ CC	-	-	125000	cycles	Retention time and Tj according below example temperature profile
		-	-	125000	cycles	max data retention time 20y, Tj=110°C
		-	-	125000	cycles	max data retention time 8.2y, Tj=125°C
Data Flash Endurance per HSMx sector (complement sensing mode) ⁸⁾	$N_{\text{E_HSMC}}$ CC	-	-	250000	cycles	Max. data retention time 10 years
Data Flash Endurance per HSMx sector (single ended sensing mode) ⁸⁾	$N_{\text{E_HSMs}}$ CC	-	-	125000	cycles	Retention time and Tj according below example temperature profile
		-	-	125000	cycles	max data retention time 20y, Tj=110°C
		-	-	125000	cycles	max data retention time 8.2y, Tj=125°C
Junction temperature limit for PFlash program/erase operations	T_{JPFlash} SR	-	-	150	°C	
Data Flash Erase Time per Sector ¹⁾³⁾⁵⁾	t_{ERD1} CC	-	-	0.5	s	Max. 1000 erase/program cycles
Data Flash Erase Time per Sector ¹⁾³⁾⁵⁾	t_{ERDM} CC	-	-	1.5	s	Max allowed cycles, see NE_EEP10 and NE_HSM parameters
DataFlash Adder on Erase Time per 32kByte erase size when using complement sensing mode ¹⁾	$t_{\text{ER_ADDC32C}}$ CC	-	-	50	ms	Adder per 32 kByte on erase time; applicable only when using complement mode

电气规格 Flash 目标参数

表 3-65 Flash (续)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data Flash Erase Time per Multi-Sector Command ¹⁾³⁾⁵⁾	$t_{\text{MERD1}}^{\text{CC}}$	-	-	0.5	s	Max 1000 erase/program cycles; For consecutive logical sectors $\leq 256\text{KBytes}$
Data Flash Erase Time per Multi-Sector Command ¹⁾³⁾⁵⁾	$t_{\text{MERDM}}^{\text{CC}}$	-	-	1.5	s	Max allowed cycles, see NE_EEP10x and NE_HSMx Parameters; For consecutive logical sectors $\leq 256\text{ kByte}$
Program Flash Access Delay at reduced VDDP3 voltage supply during cranking	$t_{\text{PF_low_VDDP3}}^{\text{CC}}$	-	-	60	ns	see register DMU_HF_PWAIT.CFL ASH
Data Flash Erase Verify time per page (Complement Sensing) ²⁾	$t_{\text{VER_PAGE_D}}^{\text{CC}}$	-	-	10	μs	Time per 8 Byte page for Verify Erased Page command
Data Flash Erase Verify time per page (Single Ended Sensing) ¹⁾	$t_{\text{VER_PAGE_DS}}^{\text{CC}}$	-	-	10	μs	Time per 8 Byte page for Verify Erased Page command
Program Flash Erase Verify time per page ¹⁾	$t_{\text{VER_PAGE_P}}^{\text{CC}}$	-	-	10	μs	Time per 32 Byte page for Verify Erased Page command
Data Flash Erase Verify time per sector (Complement Sensing) ¹⁾	$t_{\text{VER_SEC_DC}}^{\text{CC}}$	-	-	200	μs	Time per 2 KB sector for Verify Erased Logical Sector Range command
Data Flash Erase Verify time per sector (Single Ended Sensing) ¹⁾	$t_{\text{VER_SEC_DS}}^{\text{CC}}$	-	-	360	μs	Time per 4 KB sector for Verify Erased Logical Sector Range command
Program Flash Erase Verify time per sector ¹⁾	$t_{\text{VER_SEC_P}}^{\text{CC}}$	-	-	360	μs	Time per 16KB sector for Verify Erased Logical Sector Range command
Data Flash Erase Verify time per wordline (Complement Sensing) ¹⁾	$t_{\text{VER_WL_DC}}^{\text{CC}}$	-	-	30	μs	
Data Flash Erase Verify time per wordline (Single Ended Sensing) ¹⁾	$t_{\text{VER_WL_DS}}^{\text{CC}}$	-	-	50	μs	
Program Flash Erase Verify time per wordline ¹⁾	$t_{\text{VER_WL_P}}^{\text{CC}}$	-	-	30	μs	

1) 仅对 $f_{\text{FSI}} = 100\text{MHz}$ 有效。

2) 时间不依赖于编程模式 (5V 或 3.3V)。

电气规格 Flash 目标参数

- 3) 在超出规格的条件下 (例如,由于过度循环)或激活WL定向缺陷,擦除过程的持续时间可能会增加高达50%。
- 4) 使用 512 kByte / 256 kByte 擦除指令 (PFlash / DFlash)。
- 5) 如果 DataFlash 在互补感应模式下运行,则擦除时间将增加 $\text{erase_size} / 32\text{kByte} \times \text{tER_ADDC32C}$
- 6) 允许将可寻址内存划分为 8 个逻辑扇区;仍必须进行循环以考虑擦除干扰限制 N_{DFD} 。
- 7) 允许将可寻址内存划分为 6 个逻辑扇区;仍必须进行循环以考虑擦除干扰限制 N_{DFD} 。
- 8) 仅在使用强大的 EEPROM 仿真算法时有效。欲了解更多详细信息,请参阅用户手册。

电气规格质量声明

3.29 质量声明

表 3-66 质量参数

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Moisture Sensitivity Level	MSL CC	-	-	3		Conforming to Jedec J-STD--020C for 240C
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM} SR	-	-	500 ¹⁾	V	for all other balls/pins; conforming to JESD22-C101-C
		-	-	750	V	for corner balls/pins; conforming to JESD22-C101-C
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	-	-	2000 ²⁾	V	Conforming to JESD22-A114-B
ESD susceptibility of the LVDS pins according to Human Body Model (HBM)	V_{HBM1} SR	-	-	2000	V	
Operation Lifetime	t_{OP} CC	-	-	24500	hour	see below temperature profile as an example

1) AGBT 接口的焊盘最大电压限制为 250V。

2) AGBT 接口的焊盘最大电压限制为 1000V。

温度曲线示例

以下温度曲线就是一个例子。为了满足质量和可靠性目标，特定应用的温度曲线需要经过英飞凌科技公司的验证。

表 3-67 温度曲线示例

$T_J =$	Duration [h]	Comment
$\leq 170^{\circ}\text{C}$	≤ 30	
$\leq 160^{\circ}\text{C}$	≤ 120	
$\leq 150^{\circ}\text{C}$	≤ 220	
$\leq 140^{\circ}\text{C}$	≤ 350	
$\leq 130^{\circ}\text{C}$	≤ 780	
$\leq 120^{\circ}\text{C}$	≤ 1600	
$\leq 110^{\circ}\text{C}$	≤ 3000	
$\leq 100^{\circ}\text{C}$	≤ 7000	
$\leq 90^{\circ}\text{C}$	≤ 8000	
$\leq 80^{\circ}\text{C}$	≤ 2400	
$\leq 70^{\circ}\text{C}$	≤ 1000	
	≤ 24500	total time

电气规格 封装外形

表 3-68 非活动寿命温度曲线示例

$T_J =$	Duration [h]	Comment
$\leq 55^{\circ}\text{C}$	≤ 150700	

3.30 封装外形尺寸

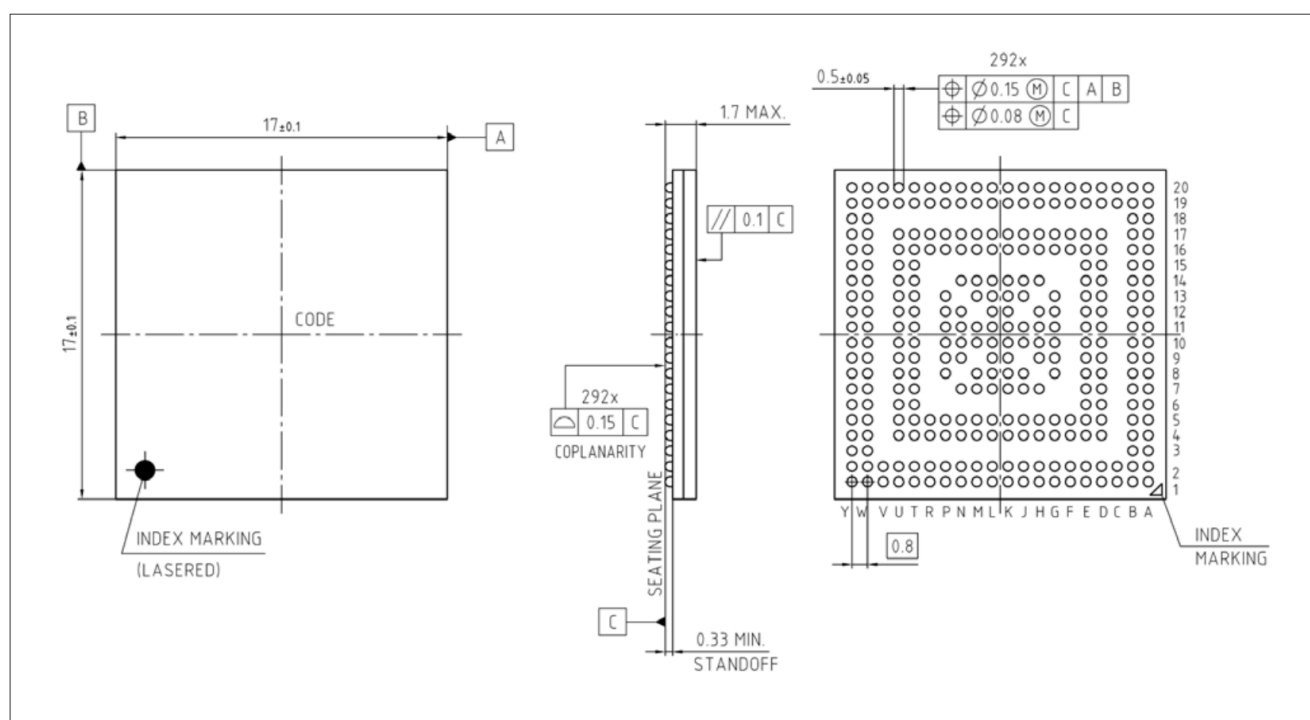


图 3-24 LFBGA-292 封装外形

电气规格 封装外形

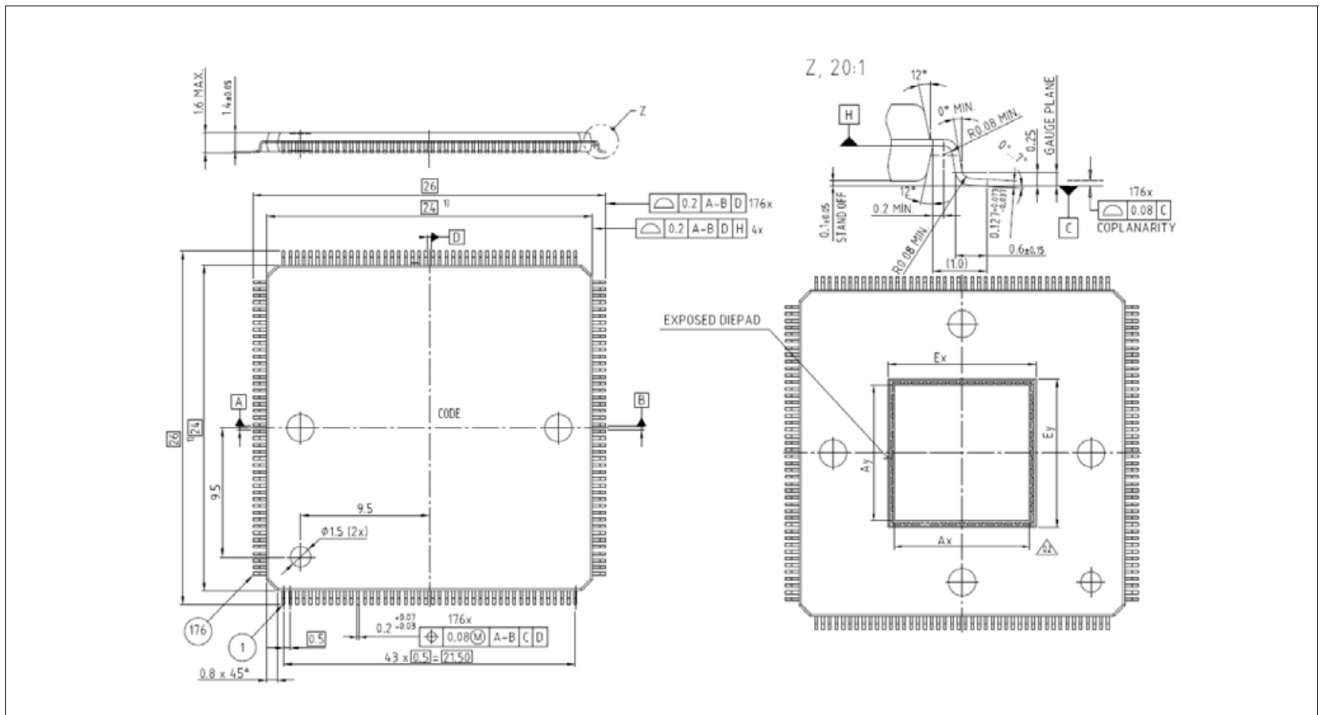


图 3-25 LQFP-176 封装外形

表 3-69 焊盘尺寸

Ex; nominal EPad size	8.7 mm $\pm$ 50 μ m
Ey; nominal EPad size	8.7 mm $\pm$ 50 μ m
Ax; solderable EPad size	7.9 mm $\pm$ 50 μ m
Ay; solderable EPad size	7.9 mm $\pm$ 50 μ m

您可以在我们的英飞凌互联网分页“产品”中找到我们所有的封装、包装种类和其他信息：
<http://www.infineon.com/packages>。

3.30.1 封装参数

表 3-70 封装参数

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance (junction to ambient) ¹⁾	RTH_JA CC	-	-	22	K/W	LFBGA-292
		-	-	17	K/W	LQFP-176
Thermal resistance (junction to case bottom) ¹⁾	RTH_JCB CC	-	-	4.5	K/W	LFBGA 292
		-	-	2	K/W	LQFP-176
Thermal resistance (junction to case top) ¹⁾	RTH_JCT CC	-	-	5	K/W	LFBGA-292
		-	-	10	K/W	LQFP-176

电气规格 封装外形

- 1) 外壳与环境之间的顶部和底部热阻 (R_{TH_CTA} , R_{TH_CBA}) 将与上面给出的结与外壳之间的热阻 (R_{TH_JCT} , R_{TH_JCB}) 相结合, 以计算结与环境之间的总热阻 (R_{TH_JA})。外壳和环境之间的热阻 (R_{TH_CTA} 、 R_{TH_CBA}) 取决于外部系统 (PCB、外壳) 的特性, 由用户负责。

结温可使用以下公式计算: $T_J = T_A + R_{TH_JA} * P_D$, 其中 R_{TH_JA} 是结点与环境之间的总热阻。

采用“冷板法” (MIL SPEC-883 方法 1012.1) 测量的热阻。

4 修订记录

0.4 版是本文档的第一个版本。

4.1 从版本0.4到版本0.6 的变更

“引脚定义和功能”章节的变更

- TC37x T 和 TP 章节的变化 - 封装变体 LFBGA-292 的引脚定义和功能
 - LFBGA-292 封装变体“端口 P00 功能”表中的变化；P00.0、P00.1、P00.2、P00.3、P00.4、P00.5、P00.6、P00.7、P00.8、P00.9、P00.10、P00.11、P00.12
 - LFBGA-292 封装变体“端口 P01 功能”表的变化；P01.5
 - LFBGA-292 封装变体“端口 P02 功能”表中的变化；P02.0、P02.1、P02.2、P02.3、P02.4、P02.5、P02.6、P02.7、P02.8、
 - LFBGA-292 封装变体“端口 P10 功能”表中的变化；P10.2、P10.5、P10.6、P10.7、P10.8
 - LFBGA-292 封装变体“端口 P11 功能”表中的变化；P11.0、P11.1、P11.2、P11.3、P11.4、P11.5、P11.6、P11.10、P11.12、P11.14
 - LFBGA-292 封装变体“端口 P13 功能”表中的更改；P13.1、P13.2
 - LFBGA-292 封装变体“端口 P14 功能”表中的变化；P14.2、P14.3、P14.4、P14.5、P14.9、P14.10
 - LFBGA-292 封装变体“端口 P15 功能”表中的更改；P15.4、P15.5
 - LFBGA-292 封装变体“端口 P20 功能”表中的变化；P20.0、P20.3、P20.14
 - LFBGA-292 封装变体“端口 P21 功能”表中的变化；P21.0、P21.2、P21.3、P21.4、P21.5
 - LFBGA-292 封装变体“端口 P22 功能”表中的变化；P22.0、P22.1、P22.2、P22.4、P22.5、P22.6、P22.7、P22.8、P22.9、P22.10、P22.11
 - LFBGA-292 封装变体“端口 P23 功能”表中的变化；P23.1、P23.2、P23.3、P23.4、P23.5、P23.6、P23.7
 - LFBGA-292 封装变体“端口 P32 功能”表中的变化；P32.0、P32.1、P32.2、P32.3、P32.4、P32.6、P32.7
 - LFBGA-292 封装变体“端口 P33 功能”表中的变化；P33.0、P33.2、P33.5、P33.7、P33.10、P33.12、P33.13
 - LFBGA-292 封装变体“端口 P34 功能”表的变化；P34.1、P34.2
 - LFBGA-292 封装变体的变化；所有端口的缓冲器类型均已更改
 - LFBGA-292 封装变体“模拟输入”表中的变更；所有球的缓冲器类型和功能均已更改
 - LFBGA-292 封装变体“系统 I/O”表的变化；所有球的缓冲器类型均已更改
 - LFBGA-292 封装变体“系统 I/O”表的变化；球 Y17、W17 的符号已更改
 - LFBGA-292 封装变体“系统 I/O”表中的变化；球 Y17、W17 的功能进行了更改，
 - LFBGA-292 封装变体的变化；“电源”表；球 L20、N19、N20 的符号和功能发生变化
- TC37x TE 章节中的变更 - 封装变体 LFBGA-292 的引脚定义和功能
 - LFBGA-292 封装变体“端口 P00 功能”表中的变化；P00.1、P00.2、P00.3、P00.4、P00.7、P00.8、P00.9、P00.10、P00.11、P00.12
 - LFBGA-292 封装变体“端口 P01 功能”表的更改；P01.5
 - LFBGA-292 封装变体“端口 P02 功能”表中的变化；P02.3、P02.4、P02.5

从版本0.4到版本0.6的变更

- LFBGA-292 封装变体“端口 P10 功能”表中的变化；P10.2、P10.5、P10.6
- LFBGA-292 封装变体“端口 P11 功能”表中的更改；P11.0、P11.1、P11.2、P11.3、P11.4、P11.5、P11.10、P11.12
- LFBGA-292 封装变体“端口 P13 功能”表中的更改；P13.1、P13.2
- LFBGA-292 封装变体“端口 P14 功能”表中的变化；P14.2、P14.3、P14.4、P14.5
- LFBGA-292 封装变体“端口 P15 功能”表中的更改；P15.4、P15.5
- LFBGA-292 封装变体“端口 P20 功能”表中的变化；P20.0、P20.6
- LFBGA-292 封装变体“端口 P21 功能”表中的变化；P21.2、P21.3、P21.4、P21.5
- LFBGA-292 封装变体“端口 P23 功能”表的变化；P23.1
- LFBGA-292 封装变体“端口 P32 功能”表中的变化；P32.1、P32.2、P32.4
- LFBGA-292 封装变体“端口 P33 功能”表中的变化；P33.0、P33.2、P33.5、P33.7、P33.10
- LFBGA-292 封装变体的变化；所有端口的缓冲器类型均已更改
- LFBGA-292 封装变体“模拟输入”表中的更改；所有球的缓冲器类型和功能均已更改
- LFBGA-292 封装变体“系统 I/O”表的更改；所有球的缓冲器类型均已更改
- LFBGA-292 封装变体“系统 I/O”表中的更改；球 Y17、W17、M20 的符号已更改，M19
- LFBGA-292 封装变体的更改；“电源”表；球 L20、N19、N20 的符号和功能已更改
- TC37x T 和 TP 章节的变更 - 封装变体 LQFP-176 的引脚定义和功能
 - LQFP-176 封装变体“端口 P00 功能”表中的变化；P00.1、P00.2、P00.3、P00.4、P00.7、P00.8、P00.9、P00.10、P00.11、P00.12
 - LQFP-176 封装变体“端口 P02 功能”表中的变化；P02.3、P02.4、P02.5
 - LQFP-176 封装变体“端口 P10 功能”表中的变化；P10.2、P10.5、P10.6
 - LQFP-176 封装变体“端口 P11 功能”表的变化；P11.2、P11.3、P11.6、P11.10、P11.12
 - LQFP-176 封装变体“端口 P13 功能”表的变化；P13.1、P13.2
 - LQFP-176 封装变体“端口 P14 功能”表中的变化；P14.2、P14.3、P14.4、P14.5
 - LQFP-176 封装变体“端口 P15 功能”表的变化；P15.4、P15.5
 - LQFP-176 封装变体“端口 P20 功能”表的变化；P20.0
 - LQFP-176 封装变体“端口 P21 功能”表的变化；P21.2、P21.3、P21.4、P21.5
 - LQFP-176 封装变体“端口 P23 功能”表的变化；P23.1
 - LQFP-176 封装变体“端口 P32 功能”表中的变化；P32.0、P32.1、P32.2、P32.4
 - LQFP-176 封装变体“端口 P33 功能”表中的变化；P33.0、P33.2、P33.5、P33.7、P33.10
 - LQFP-176 封装变体的变化；所有端口的缓冲器类型均已更改
 - LQFP-176 封装变体“模拟输入”表中的变更；所有引脚的缓冲器类型和功能均已更改
 - LQFP-176 封装变体“系统 I/O”表中的变更；所有引脚的缓冲器类型均已更改
 - LQFP-176 封装变体“系统 I/O”表的变化；引脚 84、85 的符号和功能已更改
 - LQFP-176 封装变体的变化；“电源”表；引脚 e_pad、101、104 的符号和功能已更改
- TC37x TE 章节中的变更 - 封装变体 LQFP-176 的引脚定义和功能
 - LQFP-176 封装变体“端口 P00 功能”表中的变化；P00.0、P00.1、P00.2、P00.3、P00.4、P00.5、P00.6、P00.7、P00.8、P00.9、P00.10、P00.11、P00.12

从版本0.4到版本0.6的变更

- LQFP-176 封装变体“端口 P02 功能”表中的变化；P02.0、P02.1、P02.2、P02.3、P02.4、P02.5、P02.6、P02.7、P02.8
- LQFP-176 封装变体“端口 P10 功能”表的变化；P10.2、P10.5、P10.6、P10.7、P10.8
- LQFP-176 封装变体“端口 P11 功能”表的更改；P11.2、P11.3、P11.6、P11.10、P11.12
- LQFP-176 封装变体“端口 P13 功能”表的更改；P13.1、P13.2
- LQFP-176 封装变体“端口 P14 功能”表中的变化；P14.2、P14.3、P14.4、P14.5、P14.9、P14.10
- LQFP-176 封装变体“端口 P15 功能”表的更改；P15.4、P15.5
- LQFP-176 封装变体“端口 P20 功能”表中的变化；P20.0、P20.3、
- LQFP-176 封装变体“端口 P21 功能”表中的变化；P21.0、P21.2、P21.3、P21.4、P21.5
- LQFP-176 封装变体“端口 P22 功能”表中的变化；P22.0、P22.1、P22.2
- LQFP-176 封装变体“端口 P23 功能”表中的变化；P23.1、P23.2、P23.3、P23.4、P23.5
- LQFP-176 封装变体“端口 P32 功能”表中的变化；P32.0、P32.1、P32.2、P32.3、P32.4
- LQFP-176 封装变体“端口 P33 功能”表中的变化；P33.0、P33.2、P33.5、P33.7、P33.10、P33.12、P33.13
- LQFP-176 封装变体的更改；所有端口的缓冲器类型均已更改
- LQFP-176 封装变体“模拟输入”表中的更改；所有引脚的缓冲器类型和功能均已更改
- LQFP-176 封装变体“系统 I/O”表中的变更；所有引脚的缓冲器类型均已更改
- LQFP-176 封装变体“系统 I/O”表的变化；引脚 84、85 的符号和功能已更改
- LQFP-176 封装变体“系统 I/O”表中的更改；引脚 102、103 的功能已更改
- LQFP-176 封装变体的变化；“电源”表；引脚 101、104 的符号和功能已更改
- LQFP-176 封装变体的变化；“电源”表；为引脚 177 添加了符号和功能
- TC37x TE 章节中的变更 - 封装变体 LQFP-144 的引脚定义和功能
 - LQFP-144 封装变体“端口 P00 功能”表中的变化；P00.0、P00.1、P00.2、P00.3、P00.4、P00.5、P00.6、P00.7、P00.8、P00.9、P00.12
 - LQFP-144 封装变体“端口 P02 功能”表中的变化；P02.0、P02.1、P02.2、P02.3、P02.4、P02.5、P02.6、P02.7、P02.8
 - LQFP-144 封装变体“端口 P10 功能”表的变化；P10.2、P10.5、P10.6
 - LQFP-144 封装变体“端口 P11 功能”表的变化；P11.2、P11.3、P11.6、P11.10、P11.12
 - LQFP-144 封装变体“端口 P13 功能”表的变化；P13.1、P13.2
 - LQFP-144 封装变体“端口 P14 功能”表中的变化；P14.2、P14.3、P14.4、P14.5
 - LQFP-144 封装变体“端口 P15 功能”表的变化；P15.4、P15.5
 - LQFP-144 封装变体“端口 P20 功能”表的变化；P20.0、P20.3
 - LQFP-144 封装变体“端口 P21 功能”表的变化；P21.2、P21.3、P21.4、P21.5
 - LQFP-144 封装变体“端口 P22 功能”表中的变化；P22.0、P22.1、P22.2
 - LQFP-144 封装变体“端口 P23 功能”表的变化；P23.1
 - LQFP-144 封装变体“端口 P32 功能”表中的变化；P32.0、P32.1、P32.4
 - LQFP-144 封装变体“端口 P33 功能”表的变化；P33.5、P33.7、P33.10、P33.12、P33.13
 - LQFP-144 封装变体的变化；所有端口的缓冲器类型均已更改
 - LQFP-144 封装变体“模拟输入”表中的变更；所有引脚的缓冲器类型和功能均已更改
 - LQFP-144 封装变体“系统 I/O”表中的变更；所有引脚的缓冲器类型均已更改

从版本0.4到版本0.6的变更

- LQFP-144 封装变体“系统 I/O”表的变化；引脚 70、71 的符号和功能已更改
- LQFP-144 封装变体“系统 I/O”表的变化；引脚 81、82 的功能已更改
- LQFP-144 封装变体的变化；“电源”表；引脚 83、80 的符号和功能已更改
- LQFP-144 封装变体的变化；“电源”表；为引脚 145 添加了符号和功能
- 章节“TC37x 焊盘位置配置”的变更
 - 表格“焊盘清单”所有位置的变动
- 章节“焊盘位置定义”的变更
 - 更改了“图例”子章节中的描述 - “缓冲器类型”栏：PU2

“电气规格”一章的变更

- ‘绝对最大额定值’表的变化
 - 将 V_{IN} 的最大值从 7.0 V 更改为 6.75 V
 - 将 V_{DDM} 的描述从‘ V_{DDM} 、 V_{EXT} 和 V_{FLEX} 电源引脚相对于 V_{SS} 的电压’更改为‘ V_{DDM} 、 V_{EXT} 、 V_{FLEX} 和 V_{EVRSB} 电源引脚相对于 V_{SS} 的电压’
 - 将 V_{DDM} 的注释从“7.0 V”更改为“6.75 V”
 - 在 V_{DD} 中添加了脚注 2)
 - 更改了脚注的顺序
- ‘过载参数’表的变化
 - 更改了 I_{INANA} 的注释
 - 删除了 I_{ID} 的参数
 - 更改了 K_{OVAN} 的注释
 - 更改了 K_{OVAP} 的参数条件
 - 在 K_{OVAP} 和 K_{OVAN} 中添加了脚注 2)
- “工作条件”表的变化
 - 在 V_{DD} 中添加了脚注 1)
 - 更改了脚注的顺序
- 标准焊盘表格“PORST 焊盘”的变更
 - 更改参数 HYS 的数值名称
 - 更改参数 I_{OZ} 的注释
 - 增加参数 V_{IH}
 - 增加参数 V_{IL}
 - 在 I_{PDL} 中添加脚注 2)
- 标准焊盘‘快速 5V GPIO’表的变化
 - 更改参数 I_{OZ} 的值和条件
 - 合并了单行中 I_{OZ} 的相等值
 - 更改参数 t_{RF} 的条件
 - 更改了参数 V_{IH} 的值名称
 - 更改参数 HYS 的值名称
 - 更改参数 V_{IL} 的值名称
 - 更改参数 V_{ILD} 的条件
 - 更改参数 t_{SET}
 - 为 t_{RF} 添加了脚注 1)
 - 更改了 t_{RF} 的脚注 2)

从版本0.4到版本0.6的变更

- 为 I_{PUH} 添加了脚注 4)
- 为 I_{PDL} 添加了脚注 5)
- 更改了脚注的顺序
- 标准焊盘的“快速 3.3V GPIO”表的变化
 - 更改参数 HYS 的值名称
 - 更改参数 t_{RF} 的条件
 - 更改参数 V_{IH} 的值
 - 更改参数 V_{IL} 的值
 - 更改参数 V_{ILD} 的条件
 - 更改参数 I_{OZ} 的值和条件
 - 合并了单行中 I_{OZ} 的相等值
 - 更改了参数 t_{SET}
 - 为 t_{RF} 添加了脚注 1)
 - 更改了 t_{RF} 的脚注 2)
 - 为 I_{PUH} 添加了脚注 4)
 - 为 I_{PDL} 添加了脚注 5)
 - 更改了脚注的顺序
- 标准焊盘‘慢速 5V GPIO’表的变化
 - 更改参数 HYS 的值名称
 - 更改参数 I_{PUH} 的条件
 - 更改参数 I_{OZ} 的值和条件
 - 合并了单行中 I_{OZ} 的相等值
 - 更改参数 V_{IL} 的值名称
 - 更改参数 V_{IH} 的值
 - 更改参数 V_{ILD} 的条件
 - 更改参数 t_{SET}
 - 为 t_{RF} 添加了脚注 1)
 - 更改 t_{RF} 的脚注 2)
 - 为 I_{PUH} 添加了脚注 4)
 - 为 I_{PDL} 添加了脚注 5)
 - 更改了脚注的顺序
- 标准焊盘的“慢速 3.3V GPIO”表的变化
 - 更改参数 HYS 的值名称
 - 更改参数 I_{PUH} 的条件
 - 更改参数 I_{OZ} 的值和条件
 - 合并了单行中 I_{OZ} 的相等值
 - 删除了 I_{OZ} 的参数
 - 更改参数 V_{IL} 的值和名称
 - 更改参数 V_{IH} 的值
 - 更改参数 V_{ILD} 的条件
 - 更改参数 t_{SET} 的值
 - 为 t_{RF} 加了脚注 1)

从版本0.4到版本0.6的变更

- 更改了 t_{RF} 的脚注2)
- 为 I_{PUH} 添加了脚注4)
- 为 I_{PDL} 添加了脚注5)
- 更改了脚注的顺序
- 标准焊盘的“RFast 5V GPIO”表的变化
 - 更改参数 t_{RF} 的条件
 - 更改参数 HYS 的值名称
 - 更改参数 I_{OZ} 的条件
 - 更改参数 V_{IH} 的值
 - 更改参数 V_{IL} 的值名称
 - 更改参数 V_{ILD} 的条件
 - 更改参数 t_{SET} 的值
 - 为 t_{RF} 添加了脚注 1)
 - 更改了 t_{RF} 的脚注2)
 - 为 I_{PUH} 添加了脚注4)
 - 为 I_{PDL} 添加了脚注5)
 - 更改了脚注的顺序
- 标准焊盘表格‘RFast 3.3V 焊盘’的变更
 - 更改参数 t_{RF} 的条件
 - 更改参数 HYS 的值名称
 - 更改参数 I_{OZ} 的条件
 - 更改参数 V_{IH} 的值名称
 - 更改参数 V_{IL} 的值和名称
 - 更改参数 V_{ILD} 的条件
 - 更改参数 t_{SET}
 - 为 t_{RF} 添加了脚注 1)
 - 更改了 t_{RF} 的脚注2)
 - 为 I_{PUH} 添加了脚注4)
 - 为 I_{PDL} 添加了脚注5)
 - 更改了脚注的顺序
- 标准焊盘的“S 类 5V”表的变更
 - 更改参数 HYS 的值名称
 - 更改参数 I_{OZ} 的值
 - 更改参数 V_{IH} 的值名称
 - 更改参数 V_{IL} 的值名称
 - 更改参数 t_{SET} 的值
 - 为 I_{PUH} 添加了脚注 2)
 - 为 I_{PDL} 添加了脚注 3)
- 标准焊盘‘D 类’表的变更
 - 更改参数 I_{OZ} 的值
- 表格“ADC 基准 Pads”与“标准 Pads”的变更
 - 更改了参数 I_{OZZ} 的注释

从版本0.4到版本0.6的变更

- 为 I_{OZ2} 加了脚注 1)
- LVDS Pads 表‘LVDS - IEEE 标准 LVDS 通用链路 (GPL)’中的变更
 - 更改参数 R_m 的条件
 - 添加了参数 t_{SET_LVDS}
 - 为 t_{RISE20} 添加了脚注 1)
 - 为 t_{FALL20} 添加了脚注 2)
 - 更改了脚注的顺序
- 表‘VADC 5V’中的更改
 - 增加参数 V_{DDK} 的条件
 - 更改了 dV_{DDK} 的参数命名
 - 增加参数 V_{AREF} 的条件
 - 更改了 V_{AREF} 的值和条件
 - 增加了参数 R_{PDD} 的注释
 - 为 V_{AREF} 添加了脚注 1)
 - 更改了 TUE , EA_{INL} , EA_{DNL} , EA_{GAIN} , EA_{OFF} , EN_{RMS} 的注释2)
 - 为 Q_{CONV} 添加了脚注 9)
 - 更改了脚注的顺序
 - 更改了图片“模拟输入的等效电路”
- 表‘DSADC 5V’中的变化
 - 增加了 R_{BIAS} 的参数
 - 更改 V_{AREF} 的参数
 - 更改 I_{REF} 的参数
 - 增加了 I_{REF} 的参数
 - 更改了 I_{RMS} 的参数
 - 更改了 ED_{GAIN} 的参数
 - 更改了 ED_{OFF} 的参数
 - 为 I_{RMS} , SNR 增加了脚注2)
 - 为 $SFDR$, ED_{GAIN} , ED_{OFF} 增加了脚注3)
 - 更改了脚注的顺序
- 表‘OSC_XTAL’中的变化
 - 删除了 V_{IHBX} 参数
 - 删除了 V_{ILBX} 参数
 - 增加了 DC_{X1} 参数
 - 增加了 J_{ABSX1} 参数
 - 增加了 SR_{XTAL1} 参数
 - 为 DC_{X1} , J_{ABSX1} , SR_{XTAL1} 添加了脚注3)
- ‘备用时钟’表的变化
 - 更改了 f_{SB} 的值
 - 更改了 f_{BACKT} 的脚注 1)
- 表格“DTS PMS”中的更改
 - 增加了参数 T_{NL} 的条件
- 表“DTS Core”中的更改

从版本0.4到版本0.6的变更

- 添加参数 ΔT
 - 为 T_{NL} 添加了参数条件
 - 电流消耗
 - 增加了 I_{DDRAIL} 的值和注释
 - 更改了 I_{DDRAIL} 的值
 - 增加了 $I_{DDPORST}$ 的值和注释
 - 更改了 $I_{DDPORST}$ 的值和注释
 - 更改了 $I_{STANDBY}$ 的值和注释
 - 更改 I_{DDTOT} 的值
 - 更改 PD 的值
 - 更改了 $I_{EXTFLEX}$ 的脚注 4)
 - 更改了 $I_{STANDBY}$ 的脚注 7)
 - ‘模块电流消耗’表中的变化
 - 更改 $I_{DDP3PROG}$ 参数的值
 - 更改 $I_{EXTLVDS}$ 参数的值
 - 更改 $I_{DDP3ERASE}$ 的值
 - 更改参数 I_{SCRSB} 的值
 - 更改参数 $I_{SCRIDLE}$ 的值
 - 为 I_{SCRSB} 添加了脚注 5)
 - 更改了脚注的顺序
 - ‘模块核心电流消耗’表格的变化
 - 更改 I_{DDSPU1} 的命名
 - 更改了参数 $I_{DDLBIST}$ 的条件
 - 更改参数 $I_{DDLMBIST}$ 的值和条件
 - 修改了 I_{DDHSM} 的脚注 1)
 - 为 $I_{DDLBIST}$ 添加了脚注 2)
 - “单一电源模式”章节的变更
 - 更改了“单电源模式 (a)”的图片和描述
 - 更改了“单电源模式 (e)”的图片和描述
 - 更改了“单电源模式 (d)”的图片和描述
 - 更改了“单电源模式 (h)”的图片和描述
 - ‘复位’表的变更
 - 更改参数 t_b 的值
 - 更改参数 t_{BS} 的值
 - 添加参数 $t_{WARMRSTSEQ}$
 - 更改参数 t_{BWP} 的值
 - 更改参数 t_{LBIST} 的命名和条件
 - 为 t_{EVRPOR} 添加了脚注 2)
 - 更改了脚注的顺序
- 表“EVR33 LDO”中的更改
- 更改参数 t_{STR} 的条件
 - 为 “ ΔV_{OUTTC} ” 增加了参数

从版本0.4到版本0.6的变更

- 更改参数 dV_{OUT} / dV_{IN} 的值和条件
- 为 dV_{OUT} / dI_{OUT} 添加了脚注 7)
- ‘电源监测器’表中的变化
 - 更改 V_{RSTC} 的值
 - 更改参数 V_{EXTMON} 的值
 - 更改了参数 t_{MON} 的条件
 - 更改 $V_{EXTPRIUV}$, $V_{DDP3PRIUV}$, $V_{DDPRIUV}$ 的脚注 2)
 - 更改了 $V_{DDP3PRIUV}$, $V_{DDPRIUV}$ 的脚注 3)
 - 为 V_{EXTMON} 添加了脚注 4)
 - 为 V_{EXTMON} , $V_{DDP3MON}$, V_{DDMON} 添加了脚注 5)
- 表‘EVRC SMPS’中的变化
 - 更改 ' f_{DCDC} ' 参数的值和注释
 - 更改 ' ΔV_{DDC} ' 参数的值
 - 删除了参数 C_{OUT} 的值和注释
 - 添加了参数“ L_{DC} ”的值
 - 更改参数 dV_{DDCT} / dI_{OUT} 的条件
- 将章节名称从‘锁相环 (PLL)’更改为‘系统锁相环 (SYS_PLL)’
- 表格‘PLL 系统’中的更改
 - 删除了参数 ' f_{MV} ' 的值
- 表格‘PLL 外设’中的更改
 - 更改了参数 D_{PP} 的描述和值
 - 添加参数 D_{PPI}
 - 更改了参数 D_{RMS} 的注释
 - 更改参数 DP 的注释
 - 增加参数 J_{ABS25}
- 表“主模式时序”的变化
 - 为所有参数添加了脚注 1)
- ‘LVDS 时钟/数据’表的变化
 - 为所有参数添加了脚注 3)
- ERAY 的“接收参数”表的变化
 - 更改了 $t_{dCCRxD10}$ 的描述
- 表“Flash”中的更改
 - 修改了参数 N_{DFD} 的描述
 - 添加参数 N_{DFDC}
 - 添加参数 N_{UCBD}
 - 更改了参数 N_{E_EEP10S} 的条件
 - 添加了参数 N_{E_EEP10S} 的值
 - 更改参数 N_{E_HSMS} 的条件
 - 添加了参数 N_{E_HSMS} 的值
 - 添加参数 $t_{VER_PAGE_DC}$
 - 添加了参数 $t_{VER_PAGE_DS}$
 - 删除了参数 $t_{VER_PAGE_D}$

从版本0.6到版本0.61的变更

- 更改了脚注的顺序
- “质量参数”表的变化
 - 更改了参数 V_{HBM1} 的条件
 - 为 V_{CDM} 添加了脚注 1)
 - 为 V_{HBM} 添加了脚注 2)
- “封装外形”表的变化
 - 添加了封装外形图
 - 添加了表格“散热焊盘尺寸”
- ‘封装参数’表中的更改
 - 添加表格‘封装参数’
 - 为所有参数添加了脚注1)

4.2 从版本0.6到版本0.61的变更

“特性描述”一章中的变更

- Debug/AGBT 和封装变体的“平台特性概述”表中的变更

“TC37x 引脚定义和功能”一章的变更

- 概述列表中的更改：LFBGA-292 的拼写
- LFBGA-292 封装类型概述列表变更
- 添加了 TP、TE 和 TX 变体的焊盘位置配置
- 删除封装变体 LQFP-144
- TC37x TP 章节的变更 - 针对封装变体 LFBGA-292 的引脚定义和功能
 - “端口 P00 功能”表的变化；P00.1、P00.2、P00.3、P00.4、P00.5、P00.6、P00.7、P00.8、P00.9、P00.10、P00.11、P00.12
 - ‘端口 P01 功能’表的变化；P01.6
 - ‘端口 P02 功能’表中的变化；P02.3、P02.4、P02.5、P02.6、P02.7、P02.8
 - ‘端口 P10 功能’表中的变化；P10.3、P10.4、P10.5、P10.6
 - ‘端口 P11 功能’表中的变化；P11.5、P11.7、P11.8、P11.9、P11.10、P11.11、P11.12、P11.15
 - ‘端口 P12 功能’表的变化；P12.0
 - ‘端口 P13 功能’表的变化；P13.1、P13.2
 - ‘端口 P14 功能’表中的变化；P14.2、P14.3、P14.4、P14.5
 - ‘端口 P15 功能’表中的变化；P15.4、P15.5、P15.6
 - ‘端口 P20 功能’表中的变化；P20.0、P20.8、P20.14
 - ‘端口 P21 功能’表中的变化；P21.0、P21.2、P21.3、P21.4、P21.5、P21.6、P21.7
 - ‘端口 P22 功能’表中的变化；P22.0、P22.1、P22.4、P22.5、P22.6、P22.7、P22.8、P22.9、P22.10、P22.11
 - ‘端口 P23 功能’表中的变化；P23.1、P23.2、P23.3、P23.4、P23.5、P23.6、P23.7
 - ‘端口 P32 功能’表中的变化；P32.2、P32.4
 - ‘端口 P33 功能’表中的变化；P33.0、P33.1、P33.2、P33.3、P33.4、P33.5、P33.6、P33.10、P33.12
 - ‘端口 P34 功能’表的变化；P34.5
 - “系统 I/O”表中的更改
 - “电源”表格的变化

从版本0.6到版本0.61的变更

- TC37x TE 和 TX 章节中的变更 - 针对封装变体 LFBGA-292 的引脚定义和功能
 - 更改了端口函数表的顺序
 - 更改 LFBGA-292 的拼写
 - ‘端口 P00 功能’表的变化；P00.8
 - ‘端口 P02 功能’表中的变化；P02.4, P02.5
 - ‘端口 P11 功能’表的变化；P11.5、P11.12
 - ‘端口 P13 功能’表的变化；P13.1、P13.2
 - ‘端口 P20 功能’表的变化；P20.0
 - ‘端口 P23 功能’表的变化；P23.1
 - ‘端口 P32 功能’表的变化；P32.4
- TC37x T 和 TP 章节的变更 - 封装变体 LQFP-176 的引脚定义和功能
 - ‘端口 P00 功能’表中的变化；P00.1、P00.2、P00.3、P00.4、P00.5、P00.6、P00.7、P00.8、P00.9、P00.10, P00.11, P00.12
 - ‘端口 P02 功能’表中的变化；P02.3、P02.4、P02.5,P02.6,P02.7,P02.8
 - ‘端口 P10 功能’表中的变化；P10.3、P10.4、P10.5, P10.6
 - ‘端口 P11 功能’表中的变化；P11.9、P11.10、P11.11、P11.12
 - ‘端口 P13 功能’表的变化；P13.1、P13.2
 - ‘端口 P14 功能’表中的变化；P14.2、P14.3、P14.4、P14.5
 - ‘端口 P15 功能’表中的变化；P15.4, P15.5, P15.6
 - ‘端口 P20 功能’表中的变化；P20.0、P20.8、P20.14
 - ‘端口 P21 功能’表中的变化；P21.0、P21.2、P21.3、P21.4、P21.5, P21.6, P21.7
 - ‘端口 P22 功能’表中的变化；P22.0、P22.1
 - ‘端口 P23 功能’表中的变化；P23.1、P23.2、P23.3、P23.4、P23.5
 - ‘端口 P32 功能’表中的变化；P32.2、P32.4
 - ‘端口 P33 功能’表中的变化；P33.0、P33.1、P33.2、P33.3、P33.4、P33.5, P33.6, P33.10, P33.12
 - “系统 I/O”表中的更改
 - “电源”表格中的更改
- TC37x TE 章节中的更改 - 封装变体 LQFP-176 的引脚定义和功能
 - ‘端口 P00 功能’表的变化；P00.8
 - ‘端口 P02 功能’表中的变化；P02.4, P02.5
 - ‘端口 P11 功能’表的变化；P11.12
 - ‘端口 P13 功能’表的变化；P13.1、P13.2
 - ‘端口 P15 功能’表中的变化；P15.4, P15.5
 - ‘端口 P20 功能’表的变化；P20.0
 - ‘端口 P23 功能’表的变化；P23.1
 - ‘端口 P32 功能’表的变化；P32.4
 - “电源”表格中的更改
- 删除了章节 TC37x TE - 封装变体 LQFP-144 的引脚定义和功能
- 章节“TC37x TP 焊盘位置配置”的更改
 - 表格“焊盘清单”按不同位置的变化
- 增加章节“TC37x TE 和 TX 焊盘位置配置”
- “图例”章节的改动

从版本0.6到版本0.61的变更

- 添加了有关固定软件包的 DB 版本的描述

“电气规格”章节中的变化

- 表“RFast 3.3V 焊盘”的变化
 - 添加了参数 f_{IND}
- 表‘VADC 5V’中的更改
 - 添加参数 V_{AIN} 的条件
- 表‘DSADC 5V’中的更改
 - 添加/更改了参数 I_{RMS} 和 ED_{GAIN} 的值
 - 增加脚注4)
 - 更改了脚注的顺序
- “模块电流消耗”表中的变化
 - 为 $I_{EXTFLEX}$ 添加了脚注
 - 更改了 $I_{DDTOTDC3}$ 的脚注
 - 更改了 $I_{DDTOTDC5}$ 的脚注
 - 更改了 $I_{STANDBY}$ 的脚注
 - 修改了脚注 2)
 - 增加了脚注 4) 和 6)
 - 更改了脚注的顺序
- ‘模块电流消耗’表中的变化
 - 更改了 $I_{EXTLVDS}$ 的条件
 - 更改了 I_{DDM} 的脚注
 - 更改了 I_{SCR5B} 的脚注
 - 更改了 $I_{SCRIDLE}$ 的脚注
 - 增加脚注 3) 和 5)
 - 更改了脚注的顺序
- ‘模块核心电流消耗’表中的变化
 - 更改/添加参数 I_{DDGTM} 的值
- “复位”表中的变化
 - 更改了参数 T_{BWP} 的值
 - 更改了参数 T_{SCR} 的值
- “电源监测器”表中的变化
 - 更改参数 V_{RST33} 的条件
 - 更改了参数 V_{RSTC} 的条件
- “封装外形”表的变化
 - 将图片的拼写从 LF-BGA-292 更改为 LFBGA-292
 - 删除了 QFP144 的图表
- “封装参数”表的变化
 - 删除了 QFP144 的值和注释
 - 更改了 RTH_JACC 的值

4.3 从版本0.61到版本0.7 的变更

“特性描述”章节中的改动

- “平台特性概述”表格中的变更
 - 添加封装 LQFP-144
 - 将封装名称从 LFBGA-292-10 更改为 LFBGA-292

“TC37x 引脚定义和功能”一章的变更

- 概述列表中的更改 - LFBGA-292 的封装变体
 - LFBGA-292 封装变体描述拆分 - TE 和 TX 版本
 - 增加了封装变体 LQFP-144
 - 更改了封装变体的图形编号
- “TC37x TE 的 LFBGA-292 封装引脚”一章中的变更
 - ‘端口 P00 功能’表中的变化；P00.3、P00.4、P00.8、P00.9、P00.10
 - ‘端口 P01 功能’表的变化；P01.6
 - ‘端口 P02 功能’表中的变化；P02.4、P02.5、P02.6、P02.7、P02.8、P02.11
 - ‘端口 P10 功能’表中的变化；P10.3、P10.4、P10.6
 - ‘端口 P11 功能’表的变化；P11.9、P11.15
 - ‘端口 P13 功能’表的变化；P13.1、P13.2
 - ‘端口 P14 功能’表的变化；P14.4
 - ‘端口 P15 功能’表中的变化；P15.4、P15.5、P15.6
 - ‘端口 P20 功能’表中的变化；P20.0、P20.8、P20.14
 - ‘端口 P21 功能’表的变化；P21.2、P21.3、P21.4、P21.5
 - ‘端口 P22 功能’表中的变化；P22.0、P22.5、P22.10
 - ‘端口 P23 功能’表的变化；P23.3、P23.4
 - ‘端口 P32 功能’表中的变化；P32.2、P32.4
 - ‘端口 P33 功能’表中的变化；P33.3、P33.10、P33.12
 - ‘端口 P34 功能’表的变化；P34.5
 - 表格“模拟输入”中的变化；ball U6, EDSADC；ball T6, EDSADC；ball W2, EDSADC；ball W1, EDSADC；ball M1, EDSADC；ball M2, EDSADC “系统 I/O”表中的变化；ball L7、K7、P10、P11、L14、G11、K14

添加了章节“TC37x TX 的 LFBGA-292 封装引脚”

- “TC37x TE 的 LQFP-176 封装引脚”一章的变更
 - ‘端口 P00 功能’表中的变化；P00.3、P00.4、P00.8、P00.9、P00.10
 - ‘端口 P02 功能’表中的变化；P02.4、P02.5、P02.6、P02.7、P02.8
 - ‘端口 P10 功能’表中的变化；P10.3、P10.4、P10.6
 - ‘端口 P11 功能’表的变化；P11.9
 - ‘端口 P13 功能’表的变化；P13.1、P13.2
 - ‘端口 P14 功能’表的变化；P14.4
 - ‘端口 P15 功能’表中的变化；P15.4、P15.5、P15.6
 - ‘端口 P20 功能’表中的变化；P20.0、P20.8、P20.14
 - ‘端口 P21 功能’表的变化；P21.2、P21.3、P21.4、P21.5
 - ‘端口 P22 功能’表的变化；P22.0

从版本0.61到版本0.7的变更

- ‘端口 P23 功能’表的变化；P23.3、P23.4
- ‘端口 P32 功能’表中的变化；P32.2、P32.4
- ‘端口 P33 功能’表中的变化；P33.3、P33.10、P33.12
- “模拟输入”表中的变化；引脚 44，EDSADC；引脚 43，EDSADC；引脚 29，EDSADC；引脚 28，EDSADC；

增加了章节“TC37x TE 的 LQFP-144 封装引脚”

更改了章节“TC37x TE/TX 的焊盘位置配置”

- 表格“焊盘清单”变更，编号34、35、219、220、223、224、225、307、
- 添加了关于“相邻焊盘”的描述

“图例”章节的改动

- 更改了引用 IO_Spirit_file 版本

“电气规格”章节中的变化

- “工作条件”表的变化
 - 删除了 f_{EBU} 的参数
- 表‘LVDS - IEEE 标准 LVDS 通用链路 (GPL)’中的变更
 - 更改参数 V_I 的值
 - 更改了参数 V_{idth} 的测试条件
 - 添加参数 V_{idth} 的值
 - 更改了参数 R_{in} 的测试条件
 - 为 LVDS 表添加了注释
- 表“消耗电流”的变化
 - 删除了参数 I_{DDRAIL} 的值
 - 删除了参数 $I_{DDPORST}$ 的值
 - 更改参数 $I_{EXTRAIL}$ 的值
 - 更改了参数 I_{DDTOT} 的测试条件
 - 增加了 I_{DDTOT} 的值和测试条件
 - 增加了参数 $I_{DDTOTDC3}$ 的值
 - 更改了 $I_{DDTOTDC3}$ 的测试参数
 - 增加了参数 $I_{DDTOTDC5}$ 的值
 - 更改了 $I_{DDTOTDC5}$ 的测试条件
 - 更改了参数 PD 的测试条件
 - 增加了参数 PD 的值
 - 更改了参数 PD 中的脚注 9)
- ‘模块核心电流消耗’表中的变化
 - 更改参数 I_{DDCX0} 的值
 - 更改参数 I_{DDCXx} 的值
 - 删除了 I_{DDSPU1} 的参数
 - 增加了参数 I_{DDCIF} 的值
- 添加了子章节“计算 1.25 V 消耗电流”
- “复位”表中的变化
 - 更改了参数 t_{PIP} 的值
- 表格‘PLL 系统’中的更改
 - 更改了参数 f_{REF} 的值

从版本0.7到版本0.71的变更

- 子章节‘ETH RGMII 参数’中的变化
 - 添加了 ETH RGMII TX 和 RX 信号的图片
- 添加了子章节‘SDMMC 接口时序’
- 表“Flash”中的更改
 - 更改参数 t_{PRPB5_PF} 的值
 - 更改参数 t_{ER_Dev} 的值
- 添加了 LQFP-144 封装外形图
- “封装参数”表的变化
 - 添加参数 RTH_JA 的数值 - QFP144
 - 添加参数 RTH_JCB 的数值 - QFP144
 - 添加参数 RTH_JCT 的数值 - QFP144

4.4 从版本 0.7 到版本 0.71 的变更

- 数据手册 TC37x 中的常规更改：数据手册拆分并重命名为功能包 TE/TX 的 TC37xEXT 和功能包 T/TP 的 TC37x
- 数据手册版本已从 0.7 更改为 0.71
- “平台功能概述”表格中的变更
 - 更改了 GTM 功能
 - 删除 ASIL 级别
 - 删除调试功能
 - 删除 SDMMC 功能
 - 更改了包名称的拼写
 - 更改了千兆以太网实例数量
 - 已删除的 CIF 特征
 - 更改了 CAN 特性
 - 更改了数据托架尺寸
- “TC37x 引脚定义和功能”一章的变更
 - 删除了 LFBGA-292-10、TC37x TE 和 TX 的封装引脚
 - 删除了 LQFP-176、TC37x TE 的封装引脚
 - 删除了 LQFP-144、TC37x TE 的封装引脚
 - 删除了 TC37x TE 和 TX 的焊盘位置配置
 - 更改了封装名称拼写 (LFBGA-292)
- 表格“图例”中的变更
 - 删除了适用于 TC37x TE 和 TX 套件的 Spirit 版本
- “电气规格”章节的变更
 - 更改了“绝对最大额定值”表中参数 ΣI_{IN} 的描述
 - 在“绝对最大额定值”表中添加了脚注
 - 在参数 I_{IN} 的“绝对最大额定值”表中添加了脚注
 - 更改了“过载参数”表中 V_{OUS} 参数的值
 - 更改了“工作条件”表中参数 V_{FLEX} 的条件
 - 在 V_{FLEX2} 的“工作条件”表中添加了参数

从版本0.7到版本0.71的变更

- 更改了“快速 5V GPIO”表中参数 t_{RF} 的条件
- 更改了“快速 5V GPIO”表中 HYS 参数的值
- 更改了“快速 5V GPIO”表中参数 I_{OZ} 的条件
- 更改了“快速 5V GPIO”表中参数 V_{IH} 的值
- 更改了“快速 5V GPIO”表中参数 V_{IL} 的值
- 更改了“快速 5V GPIO”表中参数 V_{ILD} 的条件
- 更改了“快速 3.3V GPIO”表中参数 t_{RF} 的条件
- 更改了“快速 3.3V GPIO”表中 HYS 参数的值
- 更改了“快速 3.3V GPIO”表中参数 I_{OZ} 的条件
- 更改了“快速 3.3V GPIO”表中参数 V_{IH} 的值
- 更改了“快速 3.3V GPIO”表中参数 V_{IL} 的值
- 更改了“快速 5V GPIO”表中参数 V_{ILD} 的条件
- 更改了“慢速 5V GPIO”表中 HYS 参数的值
- 更改了“慢速 5V GPIO”表中参数 I_{OZ} 的条件
- 更改了“慢速 5V GPIO”表中参数 V_{IH} 的值
- 更改了“慢速 5V GPIO”表中参数 V_{IL} 的值
- 更改了“慢速 5V GPIO”表中参数 V_{ILD} 的条件
- 更改了“慢速 3.3V GPIO”表中 HYS 参数的值
- 更改了“慢速 3.3V GPIO”表中参数 I_{OZ} 的条件
- 更改了“慢速 3.3V GPIO”表中参数 V_{IH} 的值
- 更改了“慢速 3.3V GPIO”表中参数 V_{IL} 的值
- 更改了“慢速 3.3V GPIO”表中参数 V_{ILD} 的条件
- 更改了“RFast 5V GPIO”表中参数 t_{RF} 的条件
- 更改了“RFast 5V GPIO”表中 HYS 参数的值
- 更改了“RFast 5V GPIO”表中参数 I_{OZ} 的条件
- 更改了“RFast 5V GPIO”表中参数 V_{IH} 的值
- 更改了“RFast 5V GPIO”表中参数 V_{IL} 的值
- 更改了“RFast 5V GPIO”表中参数 V_{ILD} 的条件
- 更改了表格“RFast 3.3V 焊盘”中参数 t_{RF} 条件
- 更改了表格“RFast 3.3V 焊盘”中参数 HYS 的值
- 更改了表格“RFast 3.3V 焊盘”中参数 I_{OZ} 的条件
- 更改了表格“RFast 3.3V 焊盘”中参数 V_{IH} 的值
- 更改了表格“RFast 3.3V 焊盘”中参数 V_{IL} 的值
- 在子章节“5V/3.3V 可切换焊盘”中添加了“Class S 3.3V”参数表
- 修改了表“OSC_XTAL”的脚注 1)
- 在“电源电流”子章节中添加了电源模式信息
- 删除了表“消耗电流”中参数 I_{DDRAIL} 的值
- 删除了表“消耗电流”中参数 $I_{DDPORST}$ 的值
- 更改了表“消耗电流”中参数 $I_{DDP3RAIL}$ 的脚注编号
- 更改了表“消耗电流”中参数 $I_{EXTRAIL}$ 的值
- 更改了表“消耗电流”中参数 $I_{EXTRAIL}$ 的脚注编号
- 更改了表“消耗电流”中参数 $I_{EXTFLEX}$ 的脚注编号

从版本0.71到版本1.0的变更

- 更改了表“消耗电流”中参数 I_{EVRSB} 的值
- 更改了参数 I_{EVRSB} 表“消耗电流”中的脚注编号
- 删除了表“消耗电流”中参数 I_{DDTOT} 的值
- 更改了表“消耗电流”中参数 $I_{DDTOTDC3}$ 的脚注编号
- 更改了表“消耗电流”中参数 $I_{DDTOTDC5}$ 的脚注编号
- 更改了表“消耗电流”中参数 I_{SLEEP} 的脚注编号
- 更改了表“消耗电流”中参数 $I_{STANDBY}$ 的脚注编号
- 删除了表“消耗电流”中参数 PD 的值
- 删除表“消耗电流”中的脚注 1)
- 删除了表“模块磁芯消耗电流”中的参数 I_{DDCIF}
- 更改了子章节“计算 1.25V 消耗电流”中的方程
- 更改了表“复位”中参数 $t_{SUPHOLD}$ 的条件
- 添加“电源监视器”表中参数 V_{EXTMON} 值和条件
- 更改了“电源监视器”表中参数 $V_{DDP3MON}$ 的条件
- 更改了“电源监视器”表中参数 V_{DDMON} 的条件
- 在“电源斜坡”表中添加了有关电源循环的注释
- 更改了“EVRC SMPS”表中参数 Δf_{DCSPR} 的符号
- 更改了“EVRC SMPS”表中参数 η_{DC} 的符号
- 删除了子章节“SDMMC 接口时序”
- 更改了“质量参数”表中参数 V_{HBM1} 的值
- “封装外形”的变更
 - 更改了图形标题的封装名称拼写
 - 删除了 LQFP-144 封装外形图
 - 删除封装参数表中封装 LQFP-144 的值
 - 更改了“封装参数”表中包名称的拼写

4.5 从版本0.71 到版本1.0的变更

- 将数据手册从 0.71 版本更改为 1.0 版本。
- “TC37x 引脚定义和功能”一章的变更
 - 更正了脚注中表格“焊盘列表”的拼写错误。
- “电气规格”章节的变更
 - 更正了表“过载参数”的注释中的拼写错误
 - 更正了表“PORST 焊盘”的注释中的拼写错误
 - 更正了表“快速 5V GPIO”注释中的拼写错误
 - 更正了表“快速 3.3V GPIO”注释中的拼写错误
 - 更正了表“慢速 5V GPIO”注释中的拼写错误
 - 更正了表“慢速 3.3V GPIO”注释中的拼写错误
 - 更正了表“RFast 5V GPIO”注释中的拼写错误
 - 更正了表“RFast 3.3V 焊盘”的注释中的拼写错误
 - 更正了表“S 5V 级”注释中的拼写错误
 - 更正了表“S 级 3.3V”注释中的拼写错误

从版本1.0到版本1.1的变更

- 修改了表"OSC_XTAL 脚注 2 中的措辞"
- 更改了“VADC 参数”一章中的“模拟输入等效电路”图
- 修改了“DSADC 参数”章节中表 DSADC 5V 的脚注 4)
- 删除了表“消耗电流”中参数 I_{DDRAIL} 的值
- 删除了表“消耗电流”中参数 $I_{DDPORST}$ 的值
- 删除了表“消耗电流”中参数 I_{DDTOT} 的值
- 删除了表“消耗电流”中参数 P_D 的值
- 更改了表“消耗电流”中参数 $I_{DDP3RAIL}$ 的脚注编号
- 更改了表“消耗电流”中参数 $I_{EXTRAIL}$ 的值
- 更改了表“消耗电流”中参数 $I_{EXTFLEX}$ 的脚注编号
- 更改了表“消耗电流”中参数 I_{EVRSB} 的脚注编号
- 更改了表“消耗电流”中参数 $I_{DDTOTDC3}$ 的脚注编号
- 更改了表“消耗电流”中参数 $I_{DDTOTDC5}$ 的脚注编号
- 更改了表“消耗电流”中参数 I_{SLEEP} 的脚注编号
- 更改了表“消耗电流”中参数 $I_{STANDBY}$ 的脚注编号
- 删除表“消耗电流”中的脚注 1)
- 更改了表“消耗电流”中的脚注编号
- 更改了“电源监视器”表中参数 V_{EXTMON} 的条件
- 修改了“电源上升”表中有关上电循环的脚注措辞
- 更改了表“复位”中参数 t_{PI} 的频率变量
- 删除了表格“ETH RGMII 信号时序参数（适用于 3.3V）”中参数 t_{21} 的注释

4.6 从版本 1.0 到版本 1.1 的变更

- “修订记录”章节的变化
 - 年表已完成
- “特性描述”章节中的改动
 - 更改了“DFLASH”的措辞
 - 增加了“AEC-Q100”的描述
 - 添加了“ISO 26262 安全要素”的描述
 - 在表“平台特性概述”中添加了数据负载/快闪式电站的描述
 - 在表“平台特性概述”中添加了参数 GTM/ Clusters 的详细信息
- “TC37x 引脚定义和功能”一章的变更
 - 将子章节标题从“TC37x TP的焊盘位置配置”更改为“焊盘框中焊盘排列顺序”
 - 为“TC37x TP 的 LFBGA-292 封装引脚”的“系统 I/O”表添加了注释
 - 在“TC37x T 和 TP 的 LQFP-176 封装引脚”一章中添加了注释
 - 为“TC37x TP 的 LQFP-176 封装引脚”的“系统 I/O”表添加了注释
 - 将子章节“TC37x TP焊盘位置配置”的措辞改为“焊盘框中的焊盘排列顺序”。

从版本1.0到版本1.1的变更

- “图例”章节的改动
 - 更改了“TC37xed_IO_Spirit”文件的版本号
- “电气规格”章节中的变化
 - 修正了子章节“绝对最大额定值”脚注中的拼写错误
 - 扩充了子章节“过载下的引脚可靠性”的介绍文本
 - 修正了子章节“过载下的引脚可靠性”“过载参数”表中参数 I_{INSA} 的拼写错误
 - 更改了“工作条件”表中 GETH 频率参数的值
 - 更改了子章节“5V/3.3V 可切换焊盘”中表格“快速 5V GPIO”中参数 $t_{\text{TX_ASYM}}$ 的注释
 - 修正了“PORST 焊盘”、“快速 5V GPIO”、“快速 3.3V GPIO”、“慢速 5V GPIO”、“慢速 3.3V GPIO”、“RFast 5V GPIO”、“RFast 3.3V 焊盘”、“Class S 5V”、“Class S 3.3V”表中不同参数的拼写错误
 - 更改了子章节“5V/3.3V 可切换焊盘”中表格“快速 3.3V GPIO”中参数 $t_{\text{TX_ASYM}}$ 的注释
 - 更改了子章节“5V/3.3V 可切换焊盘”中表格“慢速 5V GPIO”中参数 $t_{\text{TX_ASYM}}$ 的注释
 - 更改了子章节“5V/3.3V 可切换焊盘”中表格“慢速 3.3V GPIO”中参数 $t_{\text{TX_ASYM}}$ 的注释
 - 更改了子章节“5V/3.3V 可切换焊盘”中表格“RFast 5V GPIO”中参数 $t_{\text{TX_ASYM}}$ 的注释
 - 更改了子章节“5V/3.3V 可切换焊盘”中表格“RFast 3.3V 焊盘”中参数 $t_{\text{TX_ASYM}}$ 的注释
 - 修正了子章节“高性能 LVDS 焊盘”中“LVDS – IEEE 标准 LVDS 通用链路 (GPL)”表脚注3) 中的拼写错误
 - 修正了子章节“VADC 参数”中“VADC 5V”表中 dV_{CSD} 参数的拼写错误
 - 更改了子章节“VADC 参数”中表“VADC 5V”的脚注 3) 和 6)
 - 更改了子章节“VADC 参数”中“VADC 5V”表的脚注 7)
 - 更改了子章节“DSADC 参数”中“DSADC 5V”表中参数 I_{RMS} 的值
 - 更改了子章节“电源电流”的 V_{EXT} 描述的介绍
 - 新增子章节“电源电流”“消耗电流”表中参数 I_{DDRAIL} 的数值及注释
 - 新增子章节“电源电流”“消耗电流”表中参数 I_{DDPORST} 的数值及注释
 - 更改了子章节“电源电流”“电流消耗”表中的参数 I_{DDP3RAIL} 、 I_{EXTRAIL} 、 I_{EXTFLEX} 、 I_{EVRSB} 、 I_{DDTOTDC3} 、 I_{DDTOTDC5} 、 I_{SLEEP} 、 I_{STANDBY} 、 PD 的脚注编号
 - 增加子章节“电源电流”“消耗电流”表中参数 I_{DDTOT} 的数值和注释
 - 增加子章节“电源电流”“消耗电流”表中 PD 参数的数值及注释
 - 在子章节“电源电流”“消耗电流”表中增加脚注1)
 - 更改子章节“电源电流”“消耗电流”表的脚注3)
 - 更改子章节“电源电流”“消耗电流”表的脚注顺序
 - 在子章节“电源电流”“消耗电流”表增加脚注10)
 - 在子章节“供电上升和下降行为”中添加了一句话
 - 更改/添加了子章节“复位时序”中“复位”表中的参数 t_{PI} 的值
 - 更改了子章节“PMS”中“EVRC SMPS 外部组件”表中的参数 R_{ON} 的值（从最大值改为典型值）。
 - 更改了子章节“ETH MII 参数”中“ETH MII 信号时序参数”表中参数 t_7 的值(从最小值改为典型值)。

从版本1.0到版本1.1的变更

- 更改了子章节“ETH RMII 参数”中“适用于3.3V的ETH RMII 信号时序参数”表中参数 t_{13} 、 t_{14} 、 t_{15} 的符号
- 更改了子章节“ETH RMII 参数”中“适用于3.3V的ETH RMII 信号时序参数”，将参数 t_{13} 的值（从“最小值”更改为“典型值”）
- 在子章节“ETH RMII 参数”中的“适用于3.3V的ETH RMII 信号时序参数”表中的参数 t_{16} 、 t_{17} 中添加了脚注 3)
- 在子章节“ETH RMII 参数”中为表格“适用于3.3V的ETH RMII 信号时序参数”添加了脚注 3)
- 在“质量声明”子章节中添加了“非活动寿命温度曲线示例”表格

www.infineon.cn

Published by Infineon Technologies AG

公开市场版本



免责声明

请注意，本文件的原文使用英文撰写，为方便客户浏览英飞凌提供了中文译文。该中文译文仅供参考，并不可作为任何论点之依据。

由于翻译过程中可能使用了自动化程序，以及语言翻译和转换过程中的差异，最后的中文译文与最新的英文版本原文含义可能存在不尽相同之处。

因此，我们同时提供该中文译文版本的最新英文原文供您阅读，请参见 <http://www.infineon.com>

英文原文和中文译文版本之间若存有任何歧异，以最新的英文版本为准，并且仅认可英文版本为正式文件。

您如果使用本文件，即表示您同意并理解上述说明。英飞凌不对因翻译过程中可能存在的任何不完整或不准确信息而产生的任何直接或间接损失或损害负责。英飞凌不承担中文译文版本的完整性和准确性责任。如果您不同意上述说明，请不要使用本文件。

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

版本 2026-08-28

Infineon Technologies AG 出版，
德国 Neubiberg 85579

版权 © 2026 Infineon Technologies AG
及其关联公司。
保留所有权利。

**Do you have a question about this
document?**

Email:

erratum@infineon.com

重要通知

Infineon Technologies AG 及其关联公司（以下简称“英飞凌”）销售或提供和交付的产品（可能也包括样品，且可能由硬件或软件或两者组成）（以下简称“产品”），应遵守客户与英飞凌签订的框架供应合同或其他书面协议的条款和条件，如无上合同或其他书面协议，则应遵守适用的英飞凌销售条件。只有在英飞凌明确书面同意的情况下，客户的一般条款和条件或对适用的英飞凌销售条件的偏离才对英飞凌具有约束力。

为避免疑义，英飞凌不承担侵犯第三方权利的所有保证和默示保证，例如对特定用途/目的的适用性或适销性的保证。

英飞凌对与样品、应用或客户对任何产品的具体使用有关的任何信息或本文件中给出的任何示例或典型值概不负责。

本文件中包含的数据仅供具有技术资格和技能的客户代表使用。客户有责任评估产品对预期应用和客户特定用途的适用性，并在预期应用和客户特定用途中验证本文件中包含的所有相关技术数据。客户有责任正确设计、编程和测试预期应用的功能性和安全性，并遵守与其使用相关的法律要求。

除非英飞凌另行明确批准，否则产品不得用于任何因产品故障或使用产品的任何后果可合理预期会导致人身伤害的应用。但是，上述规定并不妨碍客户在英飞凌明确设计和销售的使用领域中使用任何产品，但是客户对应用负有全部责任。

英飞凌明确保留根据适用法律，如《德国版权法》（UrhG）第 44b 条，将其内容用于商业资料和数据勘探（TDM）的权利。

如果产品包含安全功能：

由于任何计算设备都不可能绝对安全，尽管产品采取了安全措施，但英飞凌不保证产品不会被入侵、数据不会被盗或遗失，或不会发生其他漏洞（以下简称“安全漏洞”），英飞凌对任何安全漏洞不承担任何责任。

如果本文件包含或引用软件：

根据美国、德国和世界其他国家的知识产权法律和条约，该软件归英飞凌所有。英飞凌保留所有权利。因此，您只能按照软件附带的软件授权协议的规定使用本软件。

如果没有适用的软件授权协议，英飞凌特此授予您个人的、非排他性的、不可转让的软件知识产权授权（无权转授权）：(a) 对于以源代码形式提供的软件，仅在贵组织内部修改和复制该软件用于英飞凌硬件产品；及 (b) 对于以二进制代码 (binary code) 形式对外向终端用户分发该软件，仅得用于英飞凌硬件产品。禁止对本软件进行任何其他使用、复制、修改、翻译或编译。有关产品、技术、交货条款和条件以及价格的详细信息，请联系离您最近的英飞凌办公室或访问 <https://www.infineon.com>。