英飞凌 32 位

微控制器

TC36x

32 位单片机

AA版

32 位单片机

数据手册

V 1.1, 2021-03

微控制器

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修订记录

Page or Item	Subjects (major changes since previous revision)
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Last Trademarks Update 2011-11-11

目录

1 特性概要

TC36x产品系列具有以下特点：

- 具有两个CPU核心的高性能微控制器
- 两个 32 位超标量 TriCore CPU (TC1.6.2P)，每个都具有以下特点：
  - 卓越的实时性能
  - 强大的位处理能力
  - 完全集成的 DSP 功能
  - 乘法累加单元能够实现每个周期2次MAC运算
  - 全流水线浮点单元(FPU)
  - 全温度范围内运行速度高达 300 MHz
  - 最高达 192 KB 的数据暂存 RAM (DSPR)
  - 最高达 32 KB 的指令暂存器 RAM (PSPR)
  - 高达 64 KB 的数据 RAM (DLMU)
  - 32 KB 指令高速缓存 (ICACHE)
  - 16 KB 数据缓存 (DCACHE)
- 所有 TC1.6.2P均配备锁步核
- 多个片上存储器
  - 所有嵌入式 NVM 和 SRAM 均受到 ECC 保护
  - 高达 4 MB 的闪存式程序存储器 (PFLASH)
  - 高达 128 KB 数据闪存式存储器 (DFLASH 0) 可用于 EEPROM 仿真
  - 引导只读存储器 (BROM)
- 具有安全数据传输的 64 通道 DMA 控制器
- 先进的中断系统（ECC保护）
- 高性能片上总线结构
  - 可提供总线主控器、CPU 和存储器之间快速并行访问的64 位交叉互连总线 (SRI)
  - 用于片上外设和功能单元的 32 位系统外设总线 (SPB)
  - SRI 至 SPB 总线桥（SFI 桥）
- 某些型号可选配硬件安全模块 (HSM)
- 处理安全监测警报的安全管理单元（SMU）
- 具有 ECC、存储器初始化和 MBIST 功能 (MTU) 的内存测试单元
- 用于检查数字 I/O 的硬件 I/O 监视器 (IOM)
- 多功能片上外设单元
  - 12 个异步/同步串行通道 (ASCLIN)，支持硬件 LIN（V1.3、V2.0、V2.1 和 J2602），速率高达 50 MBaud
  - 4 个队列 SPI 接口通道 (QSPI)，具有主从功能，速率高达 50 Mbit/s
  - 1 个高速串行链路 (HSSL)，用于处理器间串行通讯，速度高达 320 Mbit/s
  - 1 个串行微秒总线接口 (MSC)，用于将串行端口扩展到外部电源设备
  - 2 个 MCMCAN 模块，每个模块带有 4 个 CAN 节点，可通过 FIFO 缓冲实现高效数据处理
  - 10 个单边半字节传输 (SENT) 通道，用于连接传感器
  - 1 个 FlexRay ™模块，带 2 个通道 (E-Ray)，支持 V2.1
  - 一个通用定时器模块 (GTM)，提供一组强大的数字信号滤波和定时器功能，以实现自主和复杂的输入/输出管理

  - 1个捕获/比较 6 模块（两个内核：CCU60 和 CCU61）
  - 1个通用 12 定时器单元（GPT120）
  - 2 个通道外设传感器接口符合V1.3（PSI5）
  - 1 个带串行 PHY 的外围传感器接口 (PSI5-S)
  - 1 个符合 V2.1 的集成电路总线接口 (I2C)
  - 1个 IEEE 802.3 以太网 MAC (ETH)，带有 RGMII、RMII 和 MII 接口 (ETH)
- 多功能逐次逼近型 ADC (VADC)
  - 8 个独立 ADC 内核集群
  - 输入电压范围为 0 V 至 5.5V（ADC 电源）
- Delta-Sigma ADC (DSADC)
  - 4个通道
- 数字可编程 I/O 端口
- 支持OCDS Level 1 片上调试（CPU、DMA、片上总线）
- 多核调试、实时跟踪和校准
- 四/五线JTAG (IEEE 1149.1) 或 DAP (器件访问端口) 接口
- 电源管理系统和片上稳压器
- 带有系统 PLL 和外设 PLL 的时钟生成单元
- 嵌入式稳压器
- 符合 AEC-Q100 的汽车应用要求（仅适用于相应销售代码的交付发布后）
- ISO 26262 安全要素，不依赖于上下文，安全要求高达 ASIL D（仅适用于 IFX 发布的“安全包发布说明”中列出的销售代码）

订购信息

英飞凌微控制器的订购代码提供了特定产品的准确参考。此订购代码标识：

- 衍生物本身，即其功能集、温度范围和电源电压
- 封装和供应类型

表 1-1 平台特性概要

Feature		TC36x
CPUs	Type	TC1.6.2
	Cores / Checker Cores	2 / 2
	Max. Freq.	300 MHz
Cache per CPU	Program	32 KB
	Data	16 KB
SRAM per CPU	PSPR	32 KB
	DSPR	192 KB
	DLMU	64 KB
Program Flash	Size	4 MB
	Banks	2 x 2 MB
Data Flash	Size (single-ended)	128 kB (DF0) + 128 KB (DF1)
DMA	Channels	64
CONVCTRL	Modules	1
EVADC	Primary Groups/Channels	4 / 32
	Secondary Groups/Channels	2 / 32
	Fast Compare Channels	2
EDSADC	Channels	4
GTM	Clusters	4 @ 200MHz
	TIM (8 ch)	3
	TOM (16 ch)	2
	ATOM (8 ch)	4
	MCS (8 ch)	3
	CMU / ICM	1 / 1
	PSM	1
	TBU channels[1)]	4 (TBU0-3)
	SPE	2
	CMP / MON	1 / 1
	BRC / DPLL	1 / 1
	CDTM modules	4
	DTM modules	12 (4 on TOM, 8 on ATOM)
Timer	GPT12	1
	CCU6	1
STM	Modules	2

表 1-1　　平台特性概要（续）

Feature		TC36x
FlexRay	Modules	1
	Channels	2
CAN	Modules	2
	Nodes	2 x 4
	of which support TT-CAN	1
QSPI	Modules	4
	HSCI Channels	0
ASCLIN	Modules	12
I2C	Interfaces	1
SENT	Channels	10
PSI5	Modules	2
PSI5-S	Modules	1
HSSL	Channels	1
MSC	Channels	1
EBU	External Bus	0
SDMMC	eMMC/SD Interface	0
Ethernet (10/100Mbit/1Gbit)	Modules	1
FCE	Modules	1
Safety Support	SMU	yes
	IOM	yes
SPU	Modules	0
RIF	Modules	0
HSPDM	Modules	0
Security	HSM+	1
Debug	OCDS	yes
	MCDS	no
	miniMCDS	no
	miniMCDS TRAM	-
	AGBT	no
Low Power Features	Standby RAM	2 (DLMU0 + DLMU1)
	SCR	yes
Packages	Type	LFBGA-292 / LFBGA-180 / LQFP-176 /LQFP-144 / TQFP-144
I/O	Type	5 V CMOS / 3.3 V CMOS / LVDS
$T_{ambient}$	Range	−40 … +150°C

1）TBU3 具有作为角度时钟的特殊用途。

2 TC36x 引脚定义和功能

下图显示了不同封装变体的 TC36x 逻辑符号：

- LFBGA-292 (图 2-1)
- LFBGA-180 (图 2-2)
- LQFP-176（图 2-3)
- LQFP-144（图 2-4)
- TQFP-144（图 2-5)

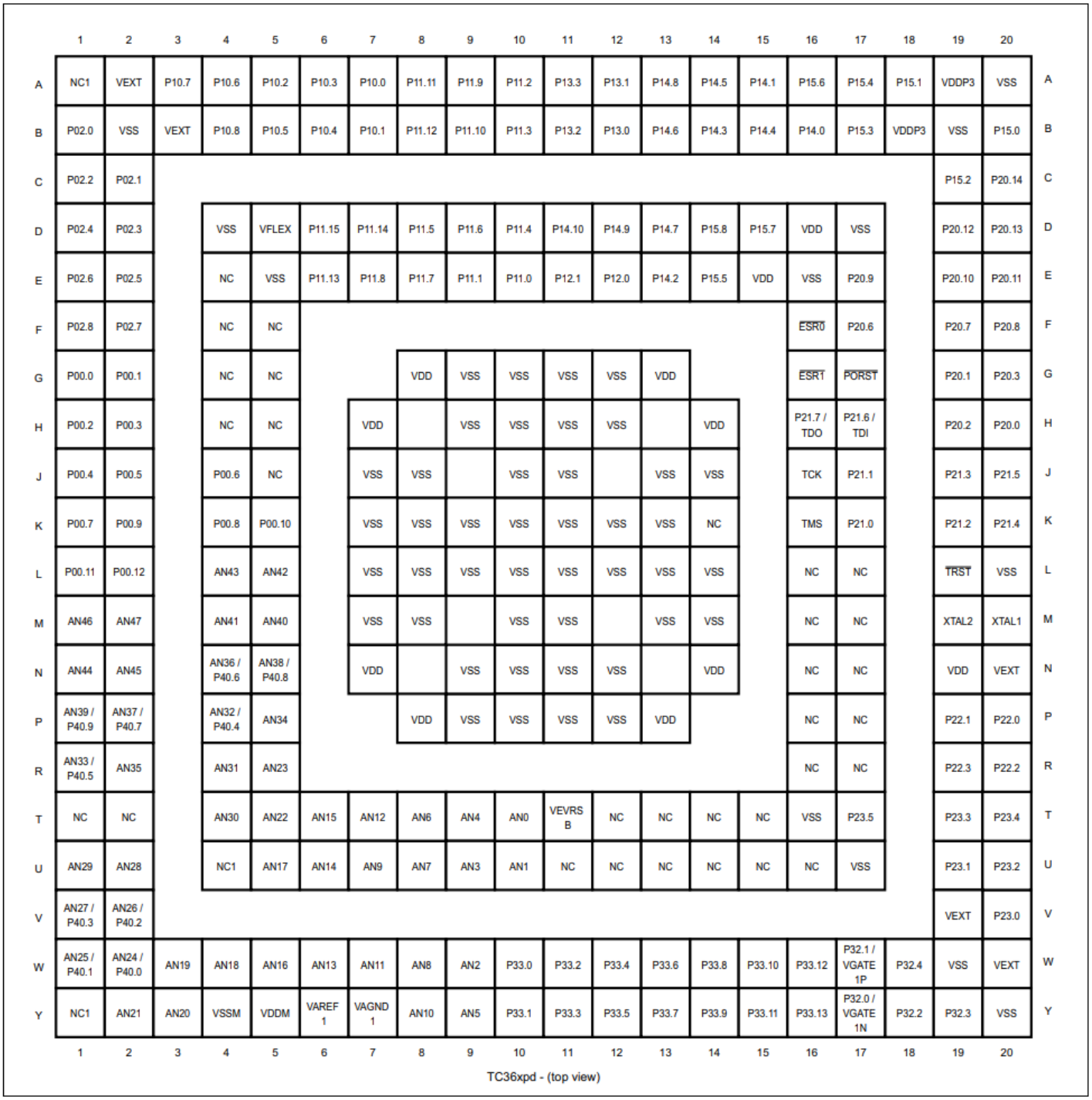

图 2-1 封装变体 LFBGA-292 的TC36x 逻辑符号

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NC	P10.3	P10.2	P11.12	P11.9	P11.2	P13.0	P13.2	P14.0	P15.3	P15.6	P15.1	P15.0	NC	A
B	P02.0	VSS	P10.1	P10.4	P11.10	P11.3	P13.1	P13.3	P14.5	P14.1	P15.4	P15.2	VSS	P20.14	B
C	P02.1	P02.2	VSS	P10.0	P11.11	P11.6	P14.8	P14.10	P14.6	P14.4	P14.3	VSS	P20.13	P20.10	C
D	P02.5	P02.4	P02.3	VSS	VFLEX	P11.8	P15.8	P15.7	P14.2	P15.5	VSS	P20.9	P20.12	P20.11	D
E	P02.6	P02.7	P02.8	P10.6	VSS					VSS	$\overline{\text{ESR1}}$	P20.7	$\overline{\text{PORST}}$	$\overline{\text{ESR0}}$	E
F	P00.4	P00.3	P00.2	P10.5		VEXT	VDDP3	VEXT	VDD		P20.6	P20.8	P21.6 / TDI	P21.7 / TDO	F
G	P00.8	P00.7	P00.6	P00.0		VEXT	VSS	VSS	VDD		TMS	P20.3	P20.2	TCK	G
H	P00.12	P00.9	P00.5	P00.1		VDD	VSS	VSS	VEVRSB		P22.2	P21.0	P20.0	P21.5	H
J	AN36 / P40.6	AN37 / P40.7	AN38 / P40.8	AN39 / P40.9		VSS	VDD	VDD	VEXT		P22.0	P22.3	P21.4	P21.3	J
K	AN32 / P40.4	AN33 / P40.5	AN34	AN35	VSS					VSS	P23.3	$\overline{\text{TRST}}$	P21.2	VSS	K
L	AN24 / P40.0	AN25 / P40.1	NC	AN14	AN5	AN2	AN0	P33.4	P33.8	P33.7	VSS	P22.1	XTAL2	XTAL1	L
M	AN16	AN17	AN12	AN10	AN6	AN3	NC	P33.1	P33.0	P33.12	P33.13	VSS	VDD	VEXT	M
N	AN15	AN13	AN9	AN11	AN8	AN4	NC	P33.3	P33.5	P33.11	P33.10	P32.1 / VGATE1P	VSS	P23.1	N
P	NC	VSSM / VAGND1	VDDM	VAREF1	AN7	AN1	NC	P33.2	P33.6	P33.9	VEXT	P32.0 / VGATE1N	P32.4	NC	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

TC36xpd - (top view)

图 2-2 封装变体 LFBGA-180 的TC36x 逻辑符号

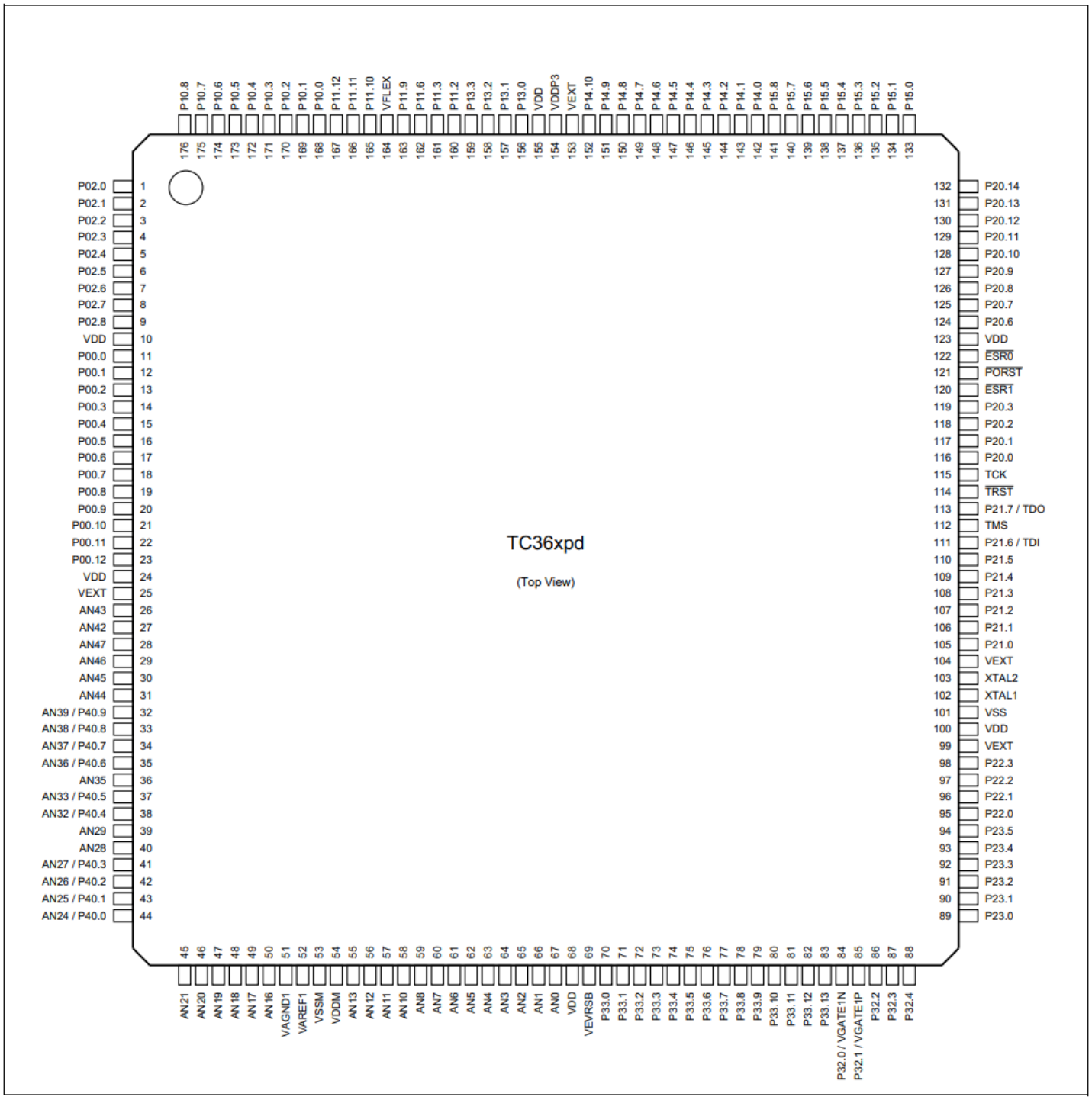

图 2-3 封装变体 LQFP-176 的TC36x 逻辑符号

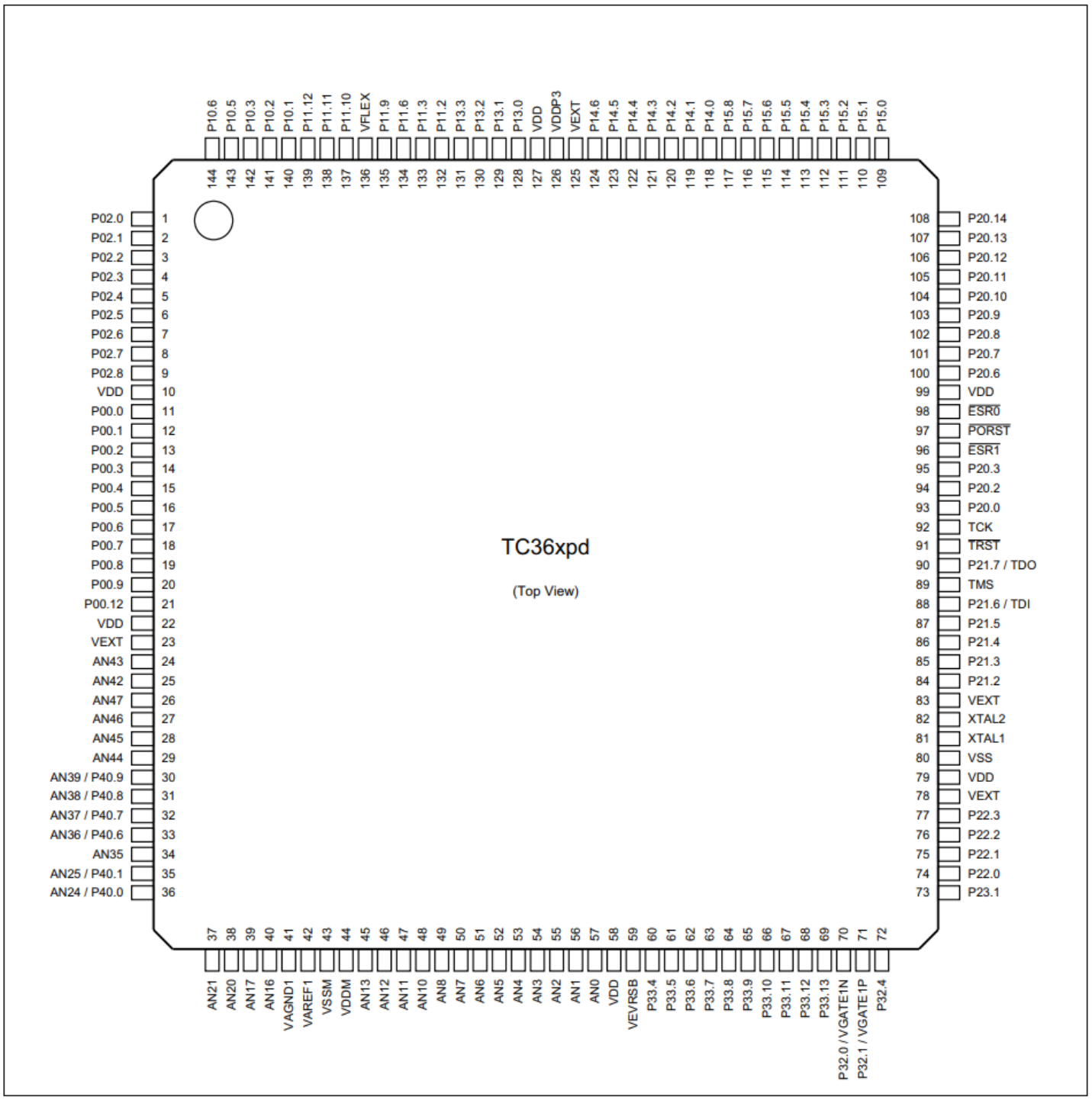

图 2-4 封装变体 LQFP-144 的TC36x 逻辑符号

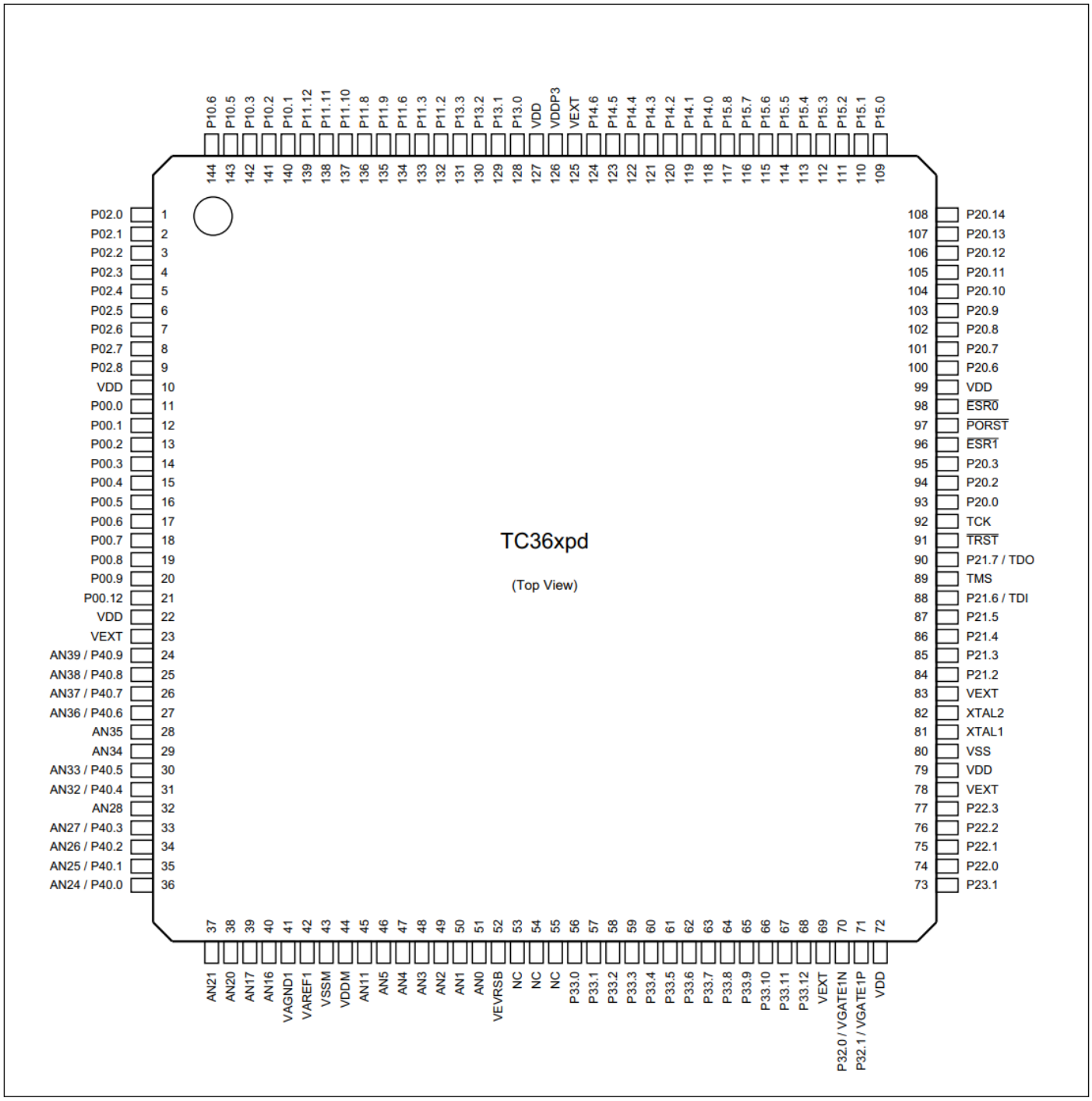

图 2-5 封装变体 TQFP-144 的 TC36x 逻辑符号

2.1 TC36x LFBGA-292 封装变体引脚配置

表 2-1 端口 P00 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
G1	P00.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN0_1			**Mux input channel 0 of TIM module 2**
	CCU61_CTRAPA			**Trap input capture**
	CCU60_T12HRE			**External timer start 12**
	MSC0_INJ0			**Injection signal from port**
	GETH_MDIOA			**MDIO Input**
	P00.0	O0		**General-purpose output**
	GTM_TOUT9	O1		**GTM muxed output**
	IOM_REF0_9			**Reference input 0**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN3_ATX	O3		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O4		**Reserved**
	CAN10_TXD	O5		**CAN transmit output node 0**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
	GETH_MDIO	O		**MDIO Output**

表 2-1 端口 P00 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
G2	P00.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN1_1			**Mux input channel 1 of TIM module 2**
	CCU60_CC60INB			**T12 capture input 60**
	ASCLIN3_ARXE			**Receive input**
	CAN10_RXDA			**CAN receive input node 0**
	PSI5_RX0A			**RXD inputs (receive data) channel 0**
	CCU61_CC60INA			**T12 capture input 60**
	SENT_SENT0B			**Receive input channel 0**
	EVADC_G9CH11	AI		**Analog input channel 11, group 9**
	P00.1	O0		**General-purpose output**
	GTM_TOUT10	O1		**GTM muxed output**
	IOM_REF0_10			**Reference input 0**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	SENT_SPC0	O6		**Transmit output**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

表 2-1 端口 00 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
H1	P00.2	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM2_IN1_2			**Mux input channel 1 of TIM module 2**
	SENT_SENT1B			**Receive input channel 1**
	EVADC_G9CH10	AI		**Analog input channel 10, group 9**
	P00.2	O0		**General-purpose output**
	GTM_TOUT11	O1		**GTM muxed output**
	IOM_REF0_11			**Reference input 0**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	PSI5_TX0	O4		**TXD outputs (send data)**
	IOM_MON1_14			**Monitor input 1**
	IOM_REF1_14			**Reference input 1**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	QSPI3_SLSO4	O6		**Master slave select output**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**

表 2-1 端口 P00 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
H2	P00.3	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM2_IN2_1			**Mux input channel 2 of TIM module 2**
	CCU60_CC61INB			**T12 capture input 61**
	EDSADC_DSCIN3A			**Modulator clock input, channel 3**
	PSI5_RX1A			**RXD inputs (receive data) channel 1**
	CAN03_RXDA			**CAN receive input node 3**
	PSI5S_RXA			**RX data input**
	SENT_SENT2B			**Receive input channel 2**
	CCU61_CC61INA			**T12 capture input 61**
	EVADC_G9CH9	AI		**Analog input channel 9, group 9**
	P00.3	O0		**General-purpose output**
	GTM_TOUT12	O1		**GTM muxed output**
	IOM_REF0_12			**Reference input 0**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	EDSADC_DSCOUT3	O4		**Modulator clock output**
	—	O5		**Reserved**
	SENT_SPC2	O6		**Transmit output**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**

表 2-1 端口 P00 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
J1	P00.4	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM2_IN3_1			Mux input channel 3 of TIM module 2
	SCU_E_REQ2_2			ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	SENT_SENT3B			Receive input channel 3
	EDSADC_DSDIN3A			Digital datastream input, channel 3
	EDSADC_SGNA			Carrier sign signal input
	ASCLIN10_ARXA			Receive input
	EVADC_G9CH8	AI		Analog input channel 8, group 9
	P00.4	O0		General-purpose output
	GTM_TOUT13	O1		GTM muxed output
	IOM_REF0_13			Reference input 0
	PSI5S_TX	O2		TX data output
	CAN11_TXD	O3		CAN transmit output node 1
	PSI5_TX1	O4		TXD outputs (send data)
	IOM_MON1_15			Monitor input 1
	—	O5		Reserved
	SENT_SPC3	O6		Transmit output
	CCU61_COUT61	O7		T12 PWM channel 61
	IOM_MON1_12			Monitor input 1
	IOM_REF1_9			Reference input 1

表 2-1 端口 P00 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
J2	P00.5	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM2_IN4_1			Mux input channel 4 of TIM module 2
	CCU60_CC62INB			T12 capture input 62
	EDSADC_DSCIN2A			Modulator clock input, channel 2
	CCU61_CC62INA			T12 capture input 62
	SENT_SENT4B			Receive input channel 4
	CAN11_RXDB			CAN receive input node 1
	GTM_DTMT1_1			CDTM1_DTM0
	EVADC_G9CH7	AI		Analog input channel 7, group 9
	P00.5	O0		General-purpose output
	GTM_TOUT14	O1		GTM muxed output
	IOM_REF0_14			Reference input 0
	EDSADC_CGPWMN	O2		Negative carrier generator output
	QSPI3_SLSO3	O3		Master slave select output
	EDSADC_DSCOUT2	O4		Modulator clock output
	EVADC_FC0BFLOUT	O5		Boundary flag output, FC channel 0
	SENT_SPC4	O6		Transmit output
	CCU61_CC62	O7		T12 PWM channel 62
	IOM_MON1_10			Monitor input 1
	IOM_REF1_11			Reference input 1
J4	P00.6	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM2_IN5_1			Mux input channel 5 of TIM module 2
	EDSADC_DSDIN2A			Digital datastream input, channel 2
	SENT_SENT5B			Receive input channel 5
	ASCLIN5_ARXA			Receive input
	EVADC_G9CH6	AI		Analog input channel 6, group 9
	P00.6	O0		General-purpose output
	GTM_TOUT15	O1		GTM muxed output
	IOM_REF0_15			Reference input 0
	EDSADC_CGPWMP	O2		Positive carrier generator output
	—	O3		Reserved
	—	O4		Reserved
	EVADC_EMUX10	O5		Control of external analog multiplexer interface 1
	SENT_SPC5	O6		Transmit output
	CCU61_COUT62	O7		T12 PWM channel 62
	IOM_MON1_13			Monitor input 1
	IOM_REF1_8			Reference input 1

表 2-1 端口 P00 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
K1	P00.7	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM2_IN6_1			Mux input channel 6 of TIM module 2
	CCU61_CC60INC			T12 capture input 60
	SENT_SENT6B			Receive input channel 6
	GPT120_T2INA			Trigger/gate input of timer T2
	CCU61_CCPOS0A			Hall capture input 0
	CCU60_T12HRB			External timer start 12
	GTM_DTMT0_2			CDTM0_DTM0
	EVADC_G9CH5	AI		Analog input channel 5, group 9
	P00.7	O0		General-purpose output
	GTM_TOUT16	O1		GTM muxed output
	ASCLIN5_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	EVADC_EMUX11	O5		Control of external analog multiplexer interface 1
	SENT_SPC6	O6		Transmit output
	CCU61_CC60	O7		T12 PWM channel 60
	IOM_MON1_8			Monitor input 1
	IOM_REF1_13			Reference input 1
K4	P00.8	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM2_IN7_1			Mux input channel 7 of TIM module 2
	CCU61_CC61INC			T12 capture input 61
	SENT_SENT7B			Receive input channel 7
	GPT120_T2EUDA			Count direction control input of timer T2
	CCU61_CCPOS1A			Hall capture input 1
	CCU60_T13HRB			External timer start 13
	ASCLIN10_ARXB			Receive input
	EVADC_G9CH4	AI		Analog input channel 4, group 9
	P00.8	O0		General-purpose output
	GTM_TOUT17	O1		GTM muxed output
	QSPI3_SLSO6	O2		Master slave select output
	ASCLIN10_ATX	O3		Transmit output
	—	O4		Reserved
	EVADC_EMUX12	O5		Control of external analog multiplexer interface 1
	SENT_SPC7	O6		Transmit output
	CCU61_CC61	O7		T12 PWM channel 61
	IOM_MON1_9			Monitor input 1
	IOM_REF1_12			Reference input 1

表 2-1 端口 P00 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
K2	P00.9	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM1_IN0_1			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_1			Mux input channel 0 of TIM module 0
	CCU61_CC62INC			T12 capture input 62
	SENT_SENT8B			Receive input channel 8
	CCU61_CCPOS2A			Hall capture input 2
	EDSADC_DSCIN1A			Modulator clock input, channel 1
	EDSADC_ITR3F			Trigger/Gate input, channel 3
	GPT120_T4EUDA			Count direction control input of timer T4
	CCU60_T13HRC			External timer start 13
	CCU60_T12HRC			External timer start 12
	EVADC_G9CH3	AI		Analog input channel 3, group 9
	P00.9	O0		General-purpose output
	GTM_TOUT18	O1		GTM muxed output
	QSPI3_SLSO7	O2		Master slave select output
	ASCLIN3_ARTS	O3		Ready to send output
	EDSADC_DSCOUT1	O4		Modulator clock output
	ASCLIN4_ATX	O5		Transmit output
	SENT_SPC8	O6		Transmit output
	CCU61_CC62	O7		T12 PWM channel 62
	IOM_MON1_10			Monitor input 1
	IOM_REF1_11			Reference input 1
K5	P00.10	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM1_IN1_1			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_1			Mux input channel 1 of TIM module 0
	SENT_SENT9B			Receive input channel 9
	EDSADC_DSDIN1A			Digital datastream input, channel 1
	EVADC_G9CH2	AI		Analog input channel 2, group 9
	P00.10	O0		General-purpose output
	GTM_TOUT19	O1		GTM muxed output
	ASCLIN4_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	SENT_SPC9	O6		Transmit output
	CCU61_COUT63	O7		T13 PWM channel 63
	IOM_MON1_7			Monitor input 1
	IOM_REF1_7			Reference input 1

表 2-1 端口 P00 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
L1	P00.11	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM1_IN2_1			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_1			**Mux input channel 2 of TIM module 0**
	CCU60_CTRAPA			**Trap input capture**
	EDSADC_DSCIN0A			**Modulator clock input, channel 0**
	CCU61_T12HRE			**External timer start 12**
	EVADC_G9CH1	AI		**Analog input channel 1, group 9**
	P00.11	O0		**General-purpose output**
	GTM_TOUT20	O1		**GTM muxed output**
	ASCLIN4_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	EDSADC_DSCOUT0	O4		**Modulator clock output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
L2	P00.12	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM1_IN3_1			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_1			**Mux input channel 3 of TIM module 0**
	ASCLIN3_ACTSA			**Clear to send input**
	EDSADC_DSDIN0A			**Digital datastream input, channel 0**
	ASCLIN4_ARXA			**Receive input**
	EVADC_G9CH0	AI		**Analog input channel 0, group 9**
	P00.12	O0		**General-purpose output**
	GTM_TOUT21	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_7			**Monitor input 1**
	IOM_REF1_7			**Reference input 1**

表 2-2 端口 P02 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
B1	P02.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_2			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_2			Mux input channel 0 of TIM module 0
	CCU61_CC60INB			T12 capture input 60
	ASCLIN2_ARXG			Receive input
	CCU60_CC60INA			T12 capture input 60
	SCU_E_REQ3_2			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	GTM_DTMA0_0			CDTM0_DTM4
	P02.0	O0		General-purpose output
	GTM_TOUT0	O1		GTM muxed output
	IOM_REF0_0			Reference input 0
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI3_SLSO1	O3		Master slave select output
	EDSADC_CGPWMN	O4		Negative carrier generator output
	CAN00_TXD	O5		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	ERAY0_TXDA	O6		Transmit Channel A
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
	IOM_REF1_6			Reference input 1

表 2-2 端口 P02 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
C2	P02.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN1_2			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_2			**Mux input channel 1 of TIM module 0**
	ERAY0_RXDA2			**Receive Channel A2**
	ASCLIN2_ARXB			**Receive input**
	CAN00_RXDA			**CAN receive input node 0**
	SCU_E_REQ2_1			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P02.1	O0		**General-purpose output**
	GTM_TOUT1	O1		**GTM muxed output**
	IOM_REF0_1			**Reference input 0**
	—	O2		**Reserved**
	QSPI3_SLSO2	O3		**Master slave select output**
	EDSADC_CGPWMP	O4		**Positive carrier generator output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**

表 2-2 端口 P02 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
C1	P02.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN2_2			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_2			**Mux input channel 2 of TIM module 0**
	CCU61_CC61INB			**T12 capture input 61**
	CCU60_CC61INA			**T12 capture input 61**
	P02.2	O0		**General-purpose output**
	GTM_TOUT2	O1		**GTM muxed output**
	IOM_REF0_2			**Reference input 0**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI3_SLSO3	O3		**Master slave select output**
	PSI5_TX0	O4		**TXD outputs (send data)**
	IOM_MON1_14			**Monitor input 1**
	IOM_REF1_14			**Reference input 1**
	CAN02_TXD	O5		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	ERAY0_TXDB	O6		**Transmit Channel B**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**

表 2-2 端口 P02 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
D2	P02.3	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN3_2			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_2			Mux input channel 3 of TIM module 0
	ERAY0_RXDB2			Receive Channel B2
	CAN02_RXDB			CAN receive input node 2
	ASCLIN1_ARXG			Receive input
	PSI5_RX0B			RXD inputs (receive data) channel 0
	P02.3	O0		General-purpose output
	GTM_TOUT3	O1		GTM muxed output
	IOM_REF0_3			Reference input 0
	ASCLIN2_ASLSO	O2		Slave select signal output
	QSPI3_SLSO4	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT61	O7		T12 PWM channel 61
	IOM_MON1_4			Monitor input 1
	IOM_REF1_2			Reference input 1

表 2-2 端口 P02 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
D1	P02.4	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN4_1			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_1			Mux input channel 4 of TIM module 0
	CCU61_CC62INB			T12 capture input 62
	QSPI3_SLSIA			Slave select input
	CCU60_CC62INA			T12 capture input 62
	I2C0_SDAA			Serial Data Input 0
	CAN11_RXDA			CAN receive input node 1
	CAN0_ECTT1			External CAN time trigger input
	P02.4	O0		General-purpose output
	GTM_TOUT4	O1		GTM muxed output
	IOM_REF0_4			Reference input 0
	ASCLIN2_ASCLK	O2		Shift clock output
	QSPI3_SLSO0	O3		Master slave select output
	PSI5S_CLK	O4		PSI5S CLK is a clock that can be used on a pin to drive the external PHY.
	I2C0_SDA	O5		Serial Data Output
	ERAY0_TXENA	O6		Transmit Enable Channel A
	CCU60_CC62	O7		T12 PWM channel 62
	IOM_MON1_0			Monitor input 1
	IOM_REF1_4			Reference input 1

表 2-2 端口 P02 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
E2	P02.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN5_1			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_1			**Mux input channel 5 of TIM module 0**
	I2C0_SCLA			**Serial Clock Input 0**
	PSI5_RX1B			**RXD inputs (receive data) channel 1**
	PSI5S_RXB			**RX data input**
	QSPI3_MRSTA			**Master SPI data input**
	SENT_SENT3C			**Receive input channel 3**
	CAN0_ECTT2			**External CAN time trigger input**
	P02.5	O0		**General-purpose output**
	GTM_TOUT5	O1		**GTM muxed output**
	IOM_REF0_5			**Reference input 0**
	CAN11_TXD	O2		**CAN transmit output node 1**
	QSPI3_MRST	O3		**Slave SPI data output**
	IOM_MON2_3			**Monitor input 2**
	IOM_REF2_3			**Reference input 2**
	—	O4		**Reserved**
	I2C0_SCL	O5		**Serial Clock Output**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**

表 2-2 端口 P02 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
E1	P02.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_1			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_1			**Mux input channel 6 of TIM module 0**
	CCU60_CC60INC			**T12 capture input 60**
	SENT_SENT2C			**Receive input channel 2**
	GPT120_T3INA			**Trigger/gate input of core timer T3**
	CCU60_CCPOS0A			**Hall capture input 0**
	CCU61_T12HRB			**External timer start 12**
	QSPI3_MTSRA			**Slave SPI data input**
	P02.6	O0		**General-purpose output**
	GTM_TOUT6	O1		**GTM muxed output**
	IOM_REF0_6			**Reference input 0**
	PSI5S_TX	O2		**TX data output**
	QSPI3_MTSR	O3		**Master SPI data output**
	PSI5_TX1	O4		**TXD outputs (send data)**
	IOM_MON1_15			**Monitor input 1**
	EVADC_EMUX00	O5		**Control of external analog multiplexer interface 0**
	—	O6		**Reserved**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

表 2-2 端口 P02 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
F2	P02.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN7_1			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_1			**Mux input channel 7 of TIM module 0**
	CCU60_CC61INC			**T12 capture input 61**
	SENT_SENT1C			**Receive input channel 1**
	EDSADC_DSCIN3B			**Modulator clock input, channel 3**
	GPT120_T3EUDA			**Count direction control input of core timer T3**
	CCU60_CCPOS1A			**Hall capture input 1**
	QSPI3_SCLKA			**Slave SPI clock inputs**
	CCU61_T13HRB			**External timer start 13**
	P02.7	O0		**General-purpose output**
	GTM_TOUT7	O1		**GTM muxed output**
	IOM_REF0_7			**Reference input 0**
	—	O2		**Reserved**
	QSPI3_SCLK	O3		**Master SPI clock output**
	EDSADC_DSCOUT3	O4		**Modulator clock output**
	EVADC_EMUX01	O5		**Control of external analog multiplexer interface 0**
	SENT_SPC1	O6		**Transmit output**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**

表 2-2 端口 P02 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
F1	P02.8	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN0_2			Mux input channel 0 of TIM module 2
	CCU60_CC62INC			T12 capture input 62
	SENT_SENT0C			Receive input channel 0
	CCU60_CCPOS2A			Hall capture input 2
	EDSADC_DSDIN3B			Digital datastream input, channel 3
	EDSADC_ITR3E			Trigger/Gate input, channel 3
	GPT120_T4INA			Trigger/gate input of timer T4
	CCU61_T12HRC			External timer start 12
	CCU61_T13HRC			External timer start 13
	GTM_DTMA0_1			CDTM0_DTM4
	P02.8	O0		General-purpose output
	GTM_TOUT8	O1		GTM muxed output
	IOM_REF0_8			Reference input 0
	QSPI3_SLSO5	O2		Master slave select output
	ASCLIN8_ASCLK	O3		Shift clock output
	—	O4		Reserved
	EVADC_EMUX02	O5		Control of external analog multiplexer interface 0
	GETH_MDC	O6		MDIO clock
	CCU60_CC62	O7		T12 PWM channel 62
	IOM_MON1_0			Monitor input 1
	IOM_REF1_4			Reference input 1

表 2-3 端口 P10 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
A7	P10.0	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN4_2			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_2			Mux input channel 4 of TIM module 0
	GPT120_T6EUDB			Count direction control input of core timer T6
	ASCLIN11_ARXA			Receive input
	GETH_RXERC			Receive Error MII
	P10.0	O0		General-purpose output
	GTM_TOUT102	O1		GTM muxed output
	ASCLIN11_ATX	O2		Transmit output
	QSPI1_SLSO10	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
B7	P10.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_3			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_3			Mux input channel 1 of TIM module 0
	GPT120_T5EUDB			Count direction control input of timer T5
	QSPI1_MRSTA			Master SPI data input
	GTM_DTMT0_1			CDTM0_DTM0
	P10.1	O0		General-purpose output
	GTM_TOUT103	O1		GTM muxed output
	QSPI1_MTSR	O2		Master SPI data output
	QSPI1_MRST	O3		Slave SPI data output
	IOM_MON2_1			Monitor input 2
	IOM_REF2_1			Reference input 2
	MSC0_EN1	O4		Chip Select
	EVADC_FC1BFLOUT	O5		Boundary flag output, FC channel 1
	—	O6		Reserved
	—	O7		Reserved

表 2-3 端口 P10 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
A5	P10.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_3			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_3			Mux input channel 2 of TIM module 0
	CAN02_RXDE			CAN receive input node 2
	MSC0_SDI1			Upstream assynchronous input signal
	QSPI1_SCLKA			Slave SPI clock inputs
	GPT120_T6INB			Trigger/gate input of core timer T6
	SCU_E_REQ2_0			ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P10.2	O0		General-purpose output
	GTM_TOUT104	O1		GTM muxed output
	IOM_MON2_9			Monitor input 2
	—	O2		Reserved
	QSPI1_SCLK	O3		Master SPI clock output
	MSC0_EN0	O4		Chip Select
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
A6	P10.3	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN3_3			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_3			Mux input channel 3 of TIM module 0
	QSPI1_MTSRA			Slave SPI data input
	SCU_E_REQ3_0			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	GPT120_T5INB			Trigger/gate input of timer T5
	P10.3	O0		General-purpose output
	GTM_TOUT105	O1		GTM muxed output
	IOM_MON2_10			Monitor input 2
	—	O2		Reserved
	QSPI1_MTSR	O3		Master SPI data output
	MSC0_EN0	O4		Chip Select
	—	O5		Reserved
	CAN02_TXD	O6		CAN transmit output node 2
	IOM_MON2_7			Monitor input 2
	IOM_REF2_7			Reference input 2
	—	O7		Reserved

表 2-3 端口 P10 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
B6	P10.4	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_2			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_2			Mux input channel 6 of TIM module 0
	QSPI1_MTSRC			Slave SPI data input
	CCU60_CCPOS0C			Hall capture input 0
	GPT120_T3INB			Trigger/gate input of core timer T3
	ASCLIN11_ARXB			Receive input
	P10.4	O0		General-purpose output
	GTM_TOUT106	O1		GTM muxed output
	IOM_MON2_11			Monitor input 2
	—	O2		Reserved
	QSPI1_SLSO8	O3		Master slave select output
	QSPI1_MTSR	O4		Master SPI data output
	MSC0_EN0	O5		Chip Select
	—	O6		Reserved
	—	O7		Reserved
B5	P10.5	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_4			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_4			Mux input channel 2 of TIM module 0
	PMS_HWCFG4IN			HWCFG4 pin input
	MSC0_INJ1			Injection signal from port
	P10.5	O0		General-purpose output
	GTM_TOUT107	O1		GTM muxed output
	IOM_REF2_9			Reference input 2
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI3_SLSO8	O3		Master slave select output
	QSPI1_SLSO9	O4		Master slave select output
	GPT120_T6OUT	O5		External output for overflow/underflow detection of core timer T6
	ASCLIN2_ASLSO	O6		Slave select signal output
	—	O7		Reserved

表 2-3 端口 P10 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
A4	P10.6	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN3_4			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_4			Mux input channel 3 of TIM module 0
	ASCLIN2_ARXD			Receive input
	QSPI3_MTSRB			Slave SPI data input
	PMS_HWCFG5IN			HWCFG5 pin input
	P10.6	O0		General-purpose output
	GTM_TOUT108	O1		GTM muxed output
	IOM_REF2_10			Reference input 2
	ASCLIN2_ASCLK	O2		Shift clock output
	QSPI3_MTSR	O3		Master SPI data output
	GPT120_T3OUT	O4		External output for overflow/underflow detection of core timer T3
	—	O5		Reserved
	QSPI1_MRST	O6		Slave SPI data output
	IOM_MON2_1			Monitor input 2
	IOM_REF2_1			Reference input 2
	—	O7		Reserved
A3	P10.7	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_3			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_3			Mux input channel 0 of TIM module 0
	GPT120_T3EUDB			Count direction control input of core timer T3
	ASCLIN2_ACTSA			Clear to send input
	QSPI3_MRSTB			Master SPI data input
	SCU_E_REQ0_2			ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	CCU60_CCPOS1C			Hall capture input 1
	P10.7	O0		General-purpose output
	GTM_TOUT109	O1		GTM muxed output
	IOM_REF2_11			Reference input 2
	—	O2		Reserved
	QSPI3_MRST	O3		Slave SPI data output
	IOM_MON2_3			Monitor input 2
	IOM_REF2_3			Reference input 2
	—	O4		Reserved
	—	O5		Reserved
	CAN12_TXD	O6		CAN transmit output node 2
	—	O7		Reserved

表 2-3 端口 P10 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
B4	P10.8	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN5_2			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_2			Mux input channel 5 of TIM module 0
	CAN12_RXDB			CAN receive input node 2
	GPT120_T4INB			Trigger/gate input of timer T4
	QSPI3_SCLKB			Slave SPI clock inputs
	SCU_E_REQ1_2			ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	CCU60_CCPOS2C			Hall capture input 2
	P10.8	O0		General-purpose output
	GTM_TOUT110	O1		GTM muxed output
	ASCLIN2_ARTS	O2		Ready to send output
	QSPI3_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-4 端口 P11 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
E10	P11.0	I	RFAST / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM2_IN0_7			Mux input channel 0 of TIM module 2
	ASCLIN3_ARXB			Receive input
	GTM_DTMA2_1			CDTM2_DTM4
	P11.0	O0		General-purpose output
	GTM_TOUT119	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	—	O3		Reserved
	—	O4		Reserved
	CAN11_TXD	O5		CAN transmit output node 1
	GETH_TXD3	O6		Transmit Data
	—	O7		Reserved

表 2-4 端口 P11 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
E9	P11.1	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM2_IN1_6			**Mux input channel 1 of TIM module 2**
	P11.1	O0		**General-purpose output**
	GTM_TOUT120	O1		**GTM muxed output**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN3_ATX	O3		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O4		**Reserved**
	CAN12_TXD	O5		**CAN transmit output node 2**
	GETH_TXD2	O6		**Transmit Data**
	—	O7		**Reserved**
A10	P11.2	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM2_IN1_3			**Mux input channel 1 of TIM module 2**
	P11.2	O0		**General-purpose output**
	GTM_TOUT95	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SLSO5	O3		**Master slave select output**
	QSPI1_SLSO5	O4		**Master slave select output**
	MSC0_EN1	O5		**Chip Select**
	GETH_TXD1	O6		**Transmit Data**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**

表 2-4 端口 P11 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
B10	P11.3	I	RFAST / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM2_IN2_2			Mux input channel 2 of TIM module 2
	MSC0_SDI3			Upstream assynchronous input signal
	QSPI1_MRSTB			Master SPI data input
	P11.3	O0		General-purpose output
	GTM_TOUT96	O1		GTM muxed output
	—	O2		Reserved
	QSPI1_MRST	O3		Slave SPI data output
	IOM_MON2_1			Monitor input 2
	IOM_REF2_1			Reference input 2
	ERAY0_TXDA	O4		Transmit Channel A
	—	O5		Reserved
	GETH_TXD0	O6		Transmit Data
	CCU60_COUT62	O7		T12 PWM channel 62
	IOM_MON1_5			Monitor input 1
	IOM_REF1_1			Reference input 1
D10	P11.4	I	RFAST / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM2_IN2_6			Mux input channel 2 of TIM module 2
	GETH_RXCLKB			Receive Clock MII
	P11.4	O0		General-purpose output
	GTM_TOUT121	O1		GTM muxed output
	ASCLIN3_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	CAN13_TXD	O5		CAN transmit output node 3
	GETH_TXER	O6		Transmit Error MII
	GETH_TXCLK	O7		Transmit Clock Output for RGMII

表 2-4 端口 P11 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
D8	P11.5	I	SLOW / RGMII_Input / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM2_IN3_8			Mux input channel 3 of TIM module 2
	GETH_TXCLKA			Transmit Clock Input for MII
	GETH_GREFCLK			Gigabit Reference Clock input for RGMII (125 MHz high precission)
	P11.5	O0		General-purpose output
	GTM_TOUT122	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
D9	P11.6	I	RFAST / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM2_IN3_2			Mux input channel 3 of TIM module 2
	QSPI1_SCLKB			Slave SPI clock inputs
	P11.6	O0		General-purpose output
	GTM_TOUT97	O1		GTM muxed output
	ERAY0_TXENB	O2		Transmit Enable Channel B
	QSPI1_SCLK	O3		Master SPI clock output
	ERAY0_TXENA	O4		Transmit Enable Channel A
	MSC0_FCLP	O5		Shift-clock direct part of the differential signal
	GETH_TXEN	O6		Transmit Enable MII and RMII
	GETH_TCTL			Transmit Control for RGMII
	CCU60_COUT61	O7		T12 PWM channel 61
	IOM_MON1_4			Monitor input 1
	IOM_REF1_2			Reference input 1

表 2-4 端口 P11 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
E8	P11.7	I	SLOW / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM2_IN4_7			**Mux input channel 4 of TIM module 2**
	GETH_RXD3A			**Receive Data 3 MII and RGMII (RGMII can use RXD3A only)**
	CAN11_RXDD			**CAN receive input node 1**
	P11.7	O0		**General-purpose output**
	GTM_TOUT123	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
E7	P11.8	I	SLOW / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM2_IN5_8			**Mux input channel 5 of TIM module 2**
	GETH_RXD2A			**Receive Data 2 MII and RGMII (RGMII can use RXD2A only)**
	CAN12_RXDD			**CAN receive input node 2**
	P11.8	O0		**General-purpose output**
	GTM_TOUT124	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

表 2-4 端口 P11 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
A9	P11.9	I	FAST / RGMII_Input / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM2_IN4_2			Mux input channel 4 of TIM module 2
	QSPI1_MTSRB			Slave SPI data input
	ERAY0_RXDA1			Receive Channel A1
	GETH_RXD1A			Receive Data 1 MII, RMII and RGMII (RGMII can use RXD1A only)
	P11.9	O0		General-purpose output
	GTM_TOUT98	O1		GTM muxed output
	—	O2		Reserved
	QSPI1_MTSR	O3		Master SPI data output
	—	O4		Reserved
	MSC0_SOP	O5		Data output - direct part of the differential signal
	—	O6		Reserved
	CCU60_COUT60	O7		T12 PWM channel 60
	IOM_MON1_3			Monitor input 1
	IOM_REF1_3			Reference input 1
B9	P11.10	I	FAST / RGMII_Input / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM2_IN5_2			Mux input channel 5 of TIM module 2
	GTM_TIM2_IN0_9			Mux input channel 0 of TIM module 2
	CAN03_RXDD			CAN receive input node 3
	ERAY0_RXDB1			Receive Channel B1
	ASCLIN1_ARXE			Receive input
	SCU_E_REQ6_3			ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	MSC0_SDI0			Upstream assynchronous input signal
	GETH_RXD0A			Receive Data 0 MII, RMII and RGMII (RGMII can use RXD0A only)
	QSPI1_SLSIA			Slave select input
	P11.10	O0		General-purpose output
	GTM_TOUT99	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO3	O3		Master slave select output
	QSPI1_SLSO3	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	CCU60_CC62	O7		T12 PWM channel 62
	IOM_MON1_0			Monitor input 1
	IOM_REF1_4			Reference input 1

表 2-4 端口 P11 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
A8	P11.11	I	FAST / RGMII_Input / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM2_IN6_2			Mux input channel 6 of TIM module 2
	GETH_CRSDVA			Carrier Sense / Data Valid combi-signal for RMII
	GETH_RXDVA			Receive Data Valid MII
	GETH_CRSB			Carrier Sense MII
	GETH_RCTLA			Receive Control for RGMII
	P11.11	O0		General-purpose output
	GTM_TOUT100	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO4	O3		Master slave select output
	QSPI1_SLSO4	O4		Master slave select output
	MSC0_EN0	O5		Chip Select
	ERAY0_TXENB	O6		Transmit Enable Channel B
	CCU60_CC61	O7		T12 PWM channel 61
	IOM_MON1_1			Monitor input 1
	IOM_REF1_5			Reference input 1
B8	P11.12	I	FAST / RGMII_Input / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM2_IN7_2			Mux input channel 7 of TIM module 2
	GETH_REFCLKA			Reference Clock input for RMII (50 MHz)
	GETH_TXCLKB			Transmit Clock Input for MII
	GETH_RXCLKA			Receive Clock MII
	P11.12	O0		General-purpose output
	GTM_TOUT101	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	GTM_CLK2	O3		CGM generated clock
	ERAY0_TXDB	O4		Transmit Channel B
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	CCU_EXTCLK1	O6		External Clock 1
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
	IOM_REF1_6			Reference input 1

表 2-4 端口 P11 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
E6	P11.13	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM2_IN6_7			**Mux input channel 6 of TIM module 2**
	GETH_RXERA			**Receive Error MII**
	CAN13_RXDD			**CAN receive input node 3**
	P11.13	O0		**General-purpose output**
	GTM_TOUT125	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
D7	P11.14	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM2_IN7_8			**Mux input channel 7 of TIM module 2**
	GETH_CRSDVB			**Carrier Sense / Data Valid combi-signal for RMII**
	GETH_RXDVB			**Receive Data Valid MII**
	GETH_CRSA			**Carrier Sense MII**
	P11.14	O0		**General-purpose output**
	GTM_TOUT126	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
D6	P11.15	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM0_IN7_8			**Mux input channel 7 of TIM module 0**
	GETH_COLA			**Collision MII**
	P11.15	O0		**General-purpose output**
	GTM_TOUT127	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

表 2-5 端口 P12 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
E12	P12.0	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	CAN00_RXDC			**CAN receive input node 0**
	GETH_RXCLKC			**Receive Clock MII**
	P12.0	O0		**General-purpose output**
	GTM_TOUT128	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	GETH_MDC	O6		**MDIO clock**
	—	O7		**Reserved**
E11	P12.1	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GETH_MDIOC			**MDIO Input**
	P12.1	O0		**General-purpose output**
	GTM_TOUT129	O1		**GTM muxed output**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	—	O7		**Reserved**
	GETH_MDIO	O		**MDIO Output**

表 2-6 端口 P13 的功能

Ball	Symbol	Ctrl.	Buffer Type	Function
B12	P13.0	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM2_IN5_3			Mux input channel 5 of TIM module 2
	ASCLIN10_ARXC			Receive input
	P13.0	O0		General-purpose output
	GTM_TOUT91	O1		GTM muxed output
	ASCLIN10_ATX	O2		Transmit output
	QSPI2_SCLKN	O3		Master SPI clock output (LVDS N line)
	MSC0_EN1	O4		Chip Select
	MSC0_FCLN	O5		Shift-clock inverted part of the differential signal
	—	O6		Reserved
	CAN10_TXD	O7		CAN transmit output node 0
A12	P13.1	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM2_IN6_3			Mux input channel 6 of TIM module 2
	I2C0_SCLB			Serial Clock Input 1
	CAN10_RXDD			CAN receive input node 0
	ASCLIN10_ARXD			Receive input
	P13.1	O0		General-purpose output
	GTM_TOUT92	O1		GTM muxed output
	—	O2		Reserved
	QSPI2_SCLKP	O3		Master SPI clock output (LVDS P line)
	—	O4		Reserved
	MSC0_FCLP	O5		Shift-clock direct part of the differential signal
	I2C0_SCL	O6		Serial Clock Output
	—	O7		Reserved
B11	P13.2	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM2_IN7_3			Mux input channel 7 of TIM module 2
	GPT120_CAPINA			Trigger input to capture value of timer T5 into CAPREL register
	I2C0_SDAB			Serial Data Input 1
	P13.2	O0		General-purpose output
	GTM_TOUT93	O1		GTM muxed output
	ASCLIN10_ASCLK	O2		Shift clock output
	QSPI2_MTSRN	O3		Master SPI data output (LVDS N line)
	MSC0_FCLP	O4		Shift-clock direct part of the differential signal
	MSC0_SON	O5		Data output - inverted part of the differential signal
	I2C0_SDA	O6		Serial Data Output
	—	O7		Reserved

表 2-6 端口 P13 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
A11	P13.3	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM2_IN0_3			Mux input channel 0 of TIM module 2
	P13.3	O0		General-purpose output
	GTM_TOUT94	O1		GTM muxed output
	ASCLIN10_ASLSO	O2		Slave select signal output
	QSPI2_MTSRP	O3		Master SPI data output (LVDS P line)
	—	O4		Reserved
	MSC0_SOP	O5		Data output - direct part of the differential signal
	—	O6		Reserved
	—	O7		Reserved

表 2-7 端口 P14 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
B16	P14.0	I	FAST / PU1 / VEXT / ES2	General-purpose input
	GTM_TIM1_IN3_5			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_5			Mux input channel 3 of TIM module 0
	P14.0	O0		General-purpose output
	GTM_TOUT80	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	ERAY0_TXDA	O3		Transmit Channel A
	ERAY0_TXDB	O4		Transmit Channel B
	CAN01_TXD	O5		CAN transmit output node 1
	IOM_MON2_6			Monitor input 2
	IOM_REF2_6			Reference input 2
	ASCLIN0_ASCLK	O6		Shift clock output
	CCU60_COUT62	O7		T12 PWM channel 62
	IOM_MON1_5			Monitor input 1
	IOM_REF1_1			Reference input 1

表 2-7 端口 P14 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
A15	P14.1	I	FAST / PU1 / VEXT / ES2	General-purpose input
	GTM_TIM1_IN4_3			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_3			Mux input channel 4 of TIM module 0
	ERAY0_RXDA3			Receive Channel A3
	ASCLIN0_ARXA			Receive input
	ERAY0_RXDB3			Receive Channel B3
	CAN01_RXDB			CAN receive input node 1
	SCU_E_REQ3_1			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	PMS_PINAWKP			PINA (P14.1) pin input
	P14.1	O0		General-purpose output
	GTM_TOUT81	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1
E13	P14.2	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN5_3			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_3			Mux input channel 5 of TIM module 0
	PMS_HWCFG2IN			HWCFG2 pin input
	P14.2	O0		General-purpose output
	GTM_TOUT82	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI2_SLSO1	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	ASCLIN2_ASCLK	O6		Shift clock output
	—	O7		Reserved

表 2-7 端口 P14 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
B14	P14.3	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_3			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_3			Mux input channel 6 of TIM module 0
	PMS_HWCFG3IN			HWCFG3 pin input
	ASCLIN2_ARXA			Receive input
	MSC0_SDI2			Upstream assynchronous input signal
	SCU_E_REQ1_0			ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P14.3	O0		General-purpose output
	GTM_TOUT83	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI2_SLSO3	O3		Master slave select output
	ASCLIN1_ASLSO	O4		Slave select signal output
	ASCLIN3_ASLSO	O5		Slave select signal output
	—	O6		Reserved
	—	O7		Reserved
B15	P14.4	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN7_2			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_2			Mux input channel 7 of TIM module 0
	PMS_HWCFG6IN			HWCFG6 pin input
	GTM_DTMT0_0			CDTM0_DTM0
	P14.4	O0		General-purpose output
	GTM_TOUT84	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	GETH_PPS	O6		Pulse Per Second
	—	O7		Reserved

表 2-7 端口 P14 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
A14	P14.5	I	FAST / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN0_4			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_4			**Mux input channel 0 of TIM module 0**
	PMS_HWCFG1IN			**HWCFG1 pin input**
	GTM_DTMA2_0			**CDTM2_DTM4**
	P14.5	O0		**General-purpose output**
	GTM_TOUT85	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ERAY0_TXDB	O6		**Transmit Channel B**
	—	O7		**Reserved**
B13	P14.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN1_4			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_4			**Mux input channel 1 of TIM module 0**
	P14.6	O0		**General-purpose output**
	GTM_TOUT86	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SLSO2	O3		**Master slave select output**
	CAN13_TXD	O4		**CAN transmit output node 3**
	—	O5		**Reserved**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	—	O7		**Reserved**

表 2-7 端口 P14 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
D13	P14.7	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_5			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_5			Mux input channel 0 of TIM module 0
	ERAY0_RXDB0			Receive Channel B0
	CAN10_RXDB			CAN receive input node 0
	CAN13_RXDA			CAN receive input node 3
	ASCLIN9_ARXC			Receive input
	P14.7	O0		General-purpose output
	GTM_TOUT87	O1		GTM muxed output
	ASCLIN0_ARTS	O2		Ready to send output
	QSPI2_SLSO4	O3		Master slave select output
	ASCLIN9_ATX	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
A13	P14.8	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN2_3			Mux input channel 2 of TIM module 2
	ERAY0_RXDA0			Receive Channel A0
	CAN02_RXDD			CAN receive input node 2
	ASCLIN1_ARXD			Receive input
	P14.8	O0		General-purpose output
	GTM_TOUT88	O1		GTM muxed output
	ASCLIN5_ASLSO	O2		Slave select signal output
	ASCLIN7_ASLSO	O3		Slave select signal output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-7 端口 P14 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
D12	P14.9	I	LVDS_RX / FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN3_3			Mux input channel 3 of TIM module 2
	ASCLIN0_ACTSA			Clear to send input
	QSPI2_MRSTFN			Master SPI data input (LVDS N line)
	ASCLIN9_ARXD			Receive input
	P14.9	O0		General-purpose output
	GTM_TOUT89	O1		GTM muxed output
	—	O2		Reserved
	MSC0_EN1	O3		Chip Select
	CAN10_TXD	O4		CAN transmit output node 0
	ERAY0_TXENB	O5		Transmit Enable Channel B
	ERAY0_TXENA	O6		Transmit Enable Channel A
	—	O7		Reserved
D11	P14.10	I	LVDS_RX / FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN4_3			Mux input channel 4 of TIM module 2
	QSPI2_MRSTFP			Master SPI data input (LVDS P line)
	P14.10	O0		General-purpose output
	GTM_TOUT90	O1		GTM muxed output
	—	O2		Reserved
	MSC0_EN0	O3		Chip Select
	ASCLIN1_ATX	O4		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	CAN02_TXD	O5		CAN transmit output node 2
	IOM_MON2_7			Monitor input 2
	IOM_REF2_7			Reference input 2
	ERAY0_TXDA	O6		Transmit Channel A
	—	O7		Reserved

表 2-8 端口 P15 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
B20	P15.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN3_4			Mux input channel 3 of TIM module 2
	P15.0	O0		General-purpose output
	GTM_TOUT71	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI0_SLSO13	O3		Master slave select output
	—	O4		Reserved
	CAN02_TXD	O5		CAN transmit output node 2
	IOM_MON2_7			Monitor input 2
	IOM_REF2_7			Reference input 2
	ASCLIN1_ASCLK	O6		Shift clock output
	—	O7		Reserved
A18	P15.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN4_4			Mux input channel 4 of TIM module 2
	CAN02_RXDA			CAN receive input node 2
	ASCLIN1_ARXA			Receive input
	QSPI2_SLSIB			Slave select input
	SCU_E_REQ7_2			ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P15.1	O0		General-purpose output
	GTM_TOUT72	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI2_SLSO5	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-8 端口 P15 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
C19	P15.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN5_4			Mux input channel 5 of TIM module 2
	QSPI2_SLSIA			Slave select input
	QSPI2_MRSTE			Master SPI data input
	P15.2	O0		General-purpose output
	GTM_TOUT73	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	QSPI2_SLSO0	O3		Master slave select output
	—	O4		Reserved
	CAN01_TXD	O5		CAN transmit output node 1
	IOM_MON2_6			Monitor input 2
	IOM_REF2_6			Reference input 2
	ASCLIN0_ASCLK	O6		Shift clock output
	—	O7		Reserved
B17	P15.3	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN6_4			Mux input channel 6 of TIM module 2
	CAN01_RXDA			CAN receive input node 1
	ASCLIN0_ARXB			Receive input
	QSPI2_SCLKA			Slave SPI clock inputs
	P15.3	O0		General-purpose output
	GTM_TOUT74	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	MSC0_EN1	O5		Chip Select
	—	O6		Reserved
	—	O7		Reserved

表 2-8 端口 P15 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
A17	P15.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN7_4			**Mux input channel 7 of TIM module 2**
	I2C0_SCLC			**Serial Clock Input 2**
	QSPI2_MRSTA			**Master SPI data input**
	SCU_E_REQ0_0			**ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.4	O0		**General-purpose output**
	GTM_TOUT75	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI2_MRST	O3		**Slave SPI data output**
	IOM_MON2_2			**Monitor input 2**
	IOM_REF2_2			**Reference input 2**
	—	O4		**Reserved**
	—	O5		**Reserved**
	I2C0_SCL	O6		**Serial Clock Output**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

表 2-8 端口 P15 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
E14	P15.5	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN0_4			Mux input channel 0 of TIM module 2
	ASCLIN1_ARXB			Receive input
	I2C0_SDAC			Serial Data Input 2
	QSPI2_MTSRA			Slave SPI data input
	SCU_E_REQ4_3			ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P15.5	O0		General-purpose output
	GTM_TOUT76	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI2_MTSR	O3		Master SPI data output
	—	O4		Reserved
	MSC0_EN0	O5		Chip Select
	I2C0_SDA	O6		Serial Data Output
	CCU60_CC61	O7		T12 PWM channel 61
	IOM_MON1_1			Monitor input 1
	IOM_REF1_5			Reference input 1
A16	P15.6	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN2_14			Mux input channel 2 of TIM module 2
	GTM_TIM1_IN0_6			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_6			Mux input channel 0 of TIM module 0
	QSPI2_MTSRB			Slave SPI data input
	P15.6	O0		General-purpose output
	GTM_TOUT77	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	QSPI2_MTSR	O3		Master SPI data output
	—	O4		Reserved
	QSPI2_SCLK	O5		Master SPI clock output
	ASCLIN3_ASCLK	O6		Shift clock output
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
	IOM_REF1_6			Reference input 1

表 2-8 端口 P15 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
D15	P15.7	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_5			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_5			Mux input channel 1 of TIM module 0
	ASCLIN3_ARXA			Receive input
	QSPI2_MRSTB			Master SPI data input
	P15.7	O0		General-purpose output
	GTM_TOUT78	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	QSPI2_MRST	O3		Slave SPI data output
	IOM_MON2_2			Monitor input 2
	IOM_REF2_2			Reference input 2
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT60	O7		T12 PWM channel 60
	IOM_MON1_3			Monitor input 1
	IOM_REF1_3			Reference input 1
D14	P15.8	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_5			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_5			Mux input channel 2 of TIM module 0
	QSPI2_SCLKB			Slave SPI clock inputs
	SCU_E_REQ5_0			ERU Channel 5 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P15.8	O0		General-purpose output
	GTM_TOUT79	O1		GTM muxed output
	—	O2		Reserved
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	ASCLIN3_ASCLK	O6		Shift clock output
	CCU60_COUT61	O7		T12 PWM channel 61
	IOM_MON1_4			Monitor input 1
	IOM_REF1_2			Reference input 1

表 2-9 端口 P20 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
H20	P20.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_7			**Mux input channel 6 of TIM module 1**
	GTM_TIM1_IN4_9			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN6_7			**Mux input channel 6 of TIM module 0**
	CAN03_RXDC			**CAN receive input node 3**
	CCU_PAD_SYSCLK			**Sysclk input**
	CBS_TGI0			**Trigger input**
	SCU_E_REQ6_0			**ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GPT120_T6EUDA			**Count direction control input of core timer T6**
	P20.0	O0		**General-purpose output**
	GTM_TOUT59	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	ASCLIN3_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	HSCT0_SYSCLK_OUT	O5		**sys clock output**
	—	O6		**Reserved**
	—	O7		**Reserved**
	CBS_TGO0	O		**Trigger output**
G19	P20.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN3_5			**Mux input channel 3 of TIM module 2**
	CBS_TGI1			**Trigger input**
	GTM_DTMA1_1			**CDTM1_DTM4**
	P20.1	O0		**General-purpose output**
	GTM_TOUT60	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	CBS_TGO1	O		**Trigger output**
H19	P20.2	I	S / PU / VEXT	**General-purpose input** This pin is latched at power on reset release to enter test mode.
	$\overline{\text{TESTMODE}}$			**Testmode Enable Input**

表 2-9 端口 P20 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
G20	P20.3	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN4_5			Mux input channel 4 of TIM module 2
	ASCLIN3_ARXC			Receive input
	GPT120_T6INA			Trigger/gate input of core timer T6
	P20.3	O0		General-purpose output
	GTM_TOUT61	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	QSPI0_SLSO9	O3		Master slave select output
	QSPI2_SLSO9	O4		Master slave select output
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	—	O6		Reserved
	—	O7		Reserved
F17	P20.6	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN6_5			Mux input channel 6 of TIM module 2
	CAN12_RXDA			CAN receive input node 2
	ASCLIN9_ARXE			Receive input
	P20.6	O0		General-purpose output
	GTM_TOUT62	O1		GTM muxed output
	ASCLIN1_ARTS	O2		Ready to send output
	QSPI0_SLSO8	O3		Master slave select output
	QSPI2_SLSO8	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-9 端口 P20 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
F19	P20.7	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN7_5			Mux input channel 7 of TIM module 2
	GTM_TIM1_IN5_8			Mux input channel 5 of TIM module 1
	CAN00_RXDB			CAN receive input node 0
	ASCLIN1_ACTSA			Clear to send input
	ASCLIN9_ARXF			Receive input
	P20.7	O0		General-purpose output
	GTM_TOUT63	O1		GTM muxed output
	ASCLIN9_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	CAN12_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	CCU61_COUT63	O7		T13 PWM channel 63
	IOM_MON1_7			Monitor input 1
	IOM_REF1_7			Reference input 1
F20	P20.8	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN7_3			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_3			Mux input channel 7 of TIM module 0
	P20.8	O0		General-purpose output
	GTM_TOUT64	O1		GTM muxed output
	ASCLIN1_ASLSO	O2		Slave select signal output
	QSPI0_SLSO0	O3		Master slave select output
	QSPI1_SLSO0	O4		Master slave select output
	CAN00_TXD	O5		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	—	O6		Reserved
	CCU61_CC60	O7		T12 PWM channel 60
	IOM_MON1_8			Monitor input 1
	IOM_REF1_13			Reference input 1

表 2-9 端口 P20 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
E17	P20.9	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN5_5			Mux input channel 5 of TIM module 2
	CAN03_RXDE			CAN receive input node 3
	ASCLIN1_ARXC			Receive input
	QSPI0_SLSIB			Slave select input
	SCU_E_REQ7_0			ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P20.9	O0		General-purpose output
	GTM_TOUT65	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO1	O3		Master slave select output
	QSPI1_SLSO1	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	CCU61_CC61	O7		T12 PWM channel 61
	IOM_MON1_9			Monitor input 1
	IOM_REF1_12			Reference input 1
E19	P20.10	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN6_6			Mux input channel 6 of TIM module 2
	P20.10	O0		General-purpose output
	GTM_TOUT66	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI0_SLSO6	O3		Master slave select output
	QSPI2_SLSO7	O4		Master slave select output
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	ASCLIN1_ASCLK	O6		Shift clock output
	CCU61_CC62	O7		T12 PWM channel 62
	IOM_MON1_10			Monitor input 1
	IOM_REF1_11			Reference input 1

表 2-9 端口 P20 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
E20	P20.11	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN7_6			Mux input channel 7 of TIM module 2
	QSPI0_SCLKA			Slave SPI clock inputs
	P20.11	O0		General-purpose output
	GTM_TOUT67	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU61_COUT60	O7		T12 PWM channel 60
	IOM_MON1_11			Monitor input 1
	IOM_REF1_10			Reference input 1
D19	P20.12	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN0_5			Mux input channel 0 of TIM module 2
	QSPI0_MRSTA			Master SPI data input
	IOM_PIN_13			GPIO pad input to FPC
	P20.12	O0		General-purpose output
	GTM_TOUT68	O1		GTM muxed output
	IOM_MON0_13			Monitor input 0
	—	O2		Reserved
	QSPI0_MRST	O3		Slave SPI data output
	IOM_MON2_0			Monitor input 2
	IOM_REF2_0			Reference input 2
	QSPI0_MTSR	O4		Master SPI data output
	—	O5		Reserved
	—	O6		Reserved
	CCU61_COUT61	O7		T12 PWM channel 61
	IOM_MON1_12			Monitor input 1
	IOM_REF1_9			Reference input 1

表 2-9 端口 P20 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
D20	P20.13	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN1_4			Mux input channel 1 of TIM module 2
	QSPI0_SLSIA			Slave select input
	IOM_PIN_14			GPIO pad input to FPC
	P20.13	O0		General-purpose output
	GTM_TOUT69	O1		GTM muxed output
	IOM_MON0_14			Monitor input 0
	—	O2		Reserved
	QSPI0_SLSO2	O3		Master slave select output
	QSPI1_SLSO2	O4		Master slave select output
	QSPI0_SCLK	O5		Master SPI clock output
	—	O6		Reserved
	CCU61_COUT62	O7		T12 PWM channel 62
	IOM_MON1_13			Monitor input 1
	IOM_REF1_8			Reference input 1
C20	P20.14	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN2_4			Mux input channel 2 of TIM module 2
	QSPI0_MTSRA			Slave SPI data input
	IOM_PIN_15			GPIO pad input to FPC
	DMU_FDEST			Enter destructive debug mode
	P20.14	O0		General-purpose output
	GTM_TOUT70	O1		GTM muxed output
	IOM_MON0_15			Monitor input 0
	—	O2		Reserved
	QSPI0_MTSR	O3		Master SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-10 端口 P21 的功能

Ball	Symbol	Ctrl.	Buffer Type	Function
K17	P21.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN4_6			**Mux input channel 4 of TIM module 2**
	ASCLIN11_ARXC			**Receive input**
	P21.0	O0		**General-purpose output**
	GTM_TOUT51	O1		**GTM muxed output**
	ASCLIN11_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSM_HSM1	O		**Pin Output Value**
J17	P21.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN5_6			**Mux input channel 5 of TIM module 2**
	ASCLIN11_ARXD			**Receive input**
	P21.1	O0		**General-purpose output**
	GTM_TOUT52	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSM_HSM2	O		**Pin Output Value**

表 2-10 端口 P21 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
K19	P21.2	I	LVDS_RX / FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_7			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_7			Mux input channel 0 of TIM module 0
	QSPI2_MRSTCN			Master SPI data input (LVDS N line)
	SCU_EMGSTOP_PORT_B			Emergency stop Port Pin B input request
	ASCLIN3_ARXGN			Differential Receive input (low active)
	HSCT0_RXDN			Rx data
	ASCLIN11_ARXE			Receive input
	GTM_DTMA1_0			CDTM1_DTM4
	P21.2	O0		General-purpose output
	GTM_TOUT53	O1		GTM muxed output
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	GETH_MDC	O5		MDIO clock
	—	O6		Reserved
	—	O7		Reserved
J19	P21.3	I	LVDS_RX / FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_6			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_6			Mux input channel 1 of TIM module 0
	QSPI2_MRSTCP			Master SPI data input (LVDS P line)
	ASCLIN3_ARXGP			Differential Receive input (high active)
	GETH_MDIOD			MDIO Input
	HSCT0_RXDP			Rx data
	P21.3	O0		General-purpose output
	GTM_TOUT54	O1		GTM muxed output
	ASCLIN11_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	GETH_MDIO	O		MDIO Output

表 2-10 端口 P21 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
K20	P21.4	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM1_IN2_6			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_6			**Mux input channel 2 of TIM module 0**
	P21.4	O0		**General-purpose output**
	GTM_TOUT55	O1		**GTM muxed output**
	ASCLIN11_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSCT0_TXDN	O		**Tx data**
J20	P21.5	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM1_IN3_6			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_6			**Mux input channel 3 of TIM module 0**
	ASCLIN11_ARXF			**Receive input**
	P21.5	O0		**General-purpose output**
	GTM_TOUT56	O1		**GTM muxed output**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN11_ATX	O3		**Transmit output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSCT0_TXDP	O		**Tx data**

表 2-10 端口 P21 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
H17	P21.6/TDI	I	FAST / PD / PU2 / VEXT / ES3	**General-purpose input** PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ.
	GTM_TIM1_IN4_8			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_8			**Mux input channel 4 of TIM module 0**
	GPT120_T5EUDA			**Count direction control input of timer T5**
	ASCLIN3_ARXF			**Receive input**
	CBS_TGI2			**Trigger input**
	TDI			**JTAG Module Data Input**
	P21.6	O0		**General-purpose output**
	GTM_TOUT57	O1		**GTM muxed output**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	GPT120_T3OUT	O7		**External output for overflow/underflow detection of core timer T3**
	CBS_TGO2	O		**Trigger output**
	DAP3	I/O		**DAP: DAP3 Data I/O**

表 2-10 端口 P21 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
H16	P21.7/TDO	I	FAST / PU2 / VEXT / ES4	General-purpose input
	GTM_TIM1_IN5_7			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_7			Mux input channel 5 of TIM module 0
	GPT120_T5INA			Trigger/gate input of timer T5
	CBS_TGI3			Trigger input
	GETH_RXERB			Receive Error MII
	P21.7	O0		General-purpose output
	GTM_TOUT58	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	ASCLIN3_ASCLK	O3		Shift clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	GPT120_T6OUT	O7		External output for overflow/underflow detection of core timer T6
	CBS_TGO3	O		Trigger output
	DAP2	I/O		DAP: DAP2 Data I/O
	TDO	O		JTAG Module Data Output

表 2-11 端口 P22 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
P20	P22.0	I	FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN1_7			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_7			Mux input channel 1 of TIM module 0
	ASCLIN6_ARXE			Receive input
	QSPI3_MTSRD			Slave SPI data input
	P22.0	O0		General-purpose output
	GTM_TOUT47	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	QSPI3_MTSR	O3		Master SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	ASCLIN6_ATX	O7		Transmit output
P19	P22.1	I	FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN0_8			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_8			Mux input channel 0 of TIM module 0
	ASCLIN7_ARXE			Receive input
	QSPI3_MRSTD			Master SPI data input
	P22.1	O0		General-purpose output
	GTM_TOUT48	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	QSPI3_MRST	O3		Slave SPI data output
	IOM_MON2_3			Monitor input 2
	IOM_REF2_3			Reference input 2
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	ASCLIN7_ATX	O7		Transmit output

表 2-11 端口 P22 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
R20	P22.2	I	FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN3_7			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_7			Mux input channel 3 of TIM module 0
	P22.2	O0		General-purpose output
	GTM_TOUT49	O1		GTM muxed output
	ASCLIN5_ATX	O2		Transmit output
	QSPI3_SLSO12	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
R19	P22.3	I	FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN4_4			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_4			Mux input channel 4 of TIM module 0
	ASCLIN5_ARXC			Receive input
	QSPI3_SCLKD			Slave SPI clock inputs
	P22.3	O0		General-purpose output
	GTM_TOUT50	O1		GTM muxed output
	—	O2		Reserved
	QSPI3_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-12 端口 P23 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
V20	P23.0	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN5_4			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_4			Mux input channel 5 of TIM module 0
	CAN10_RXDC			CAN receive input node 0
	P23.0	O0		General-purpose output
	GTM_TOUT41	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
U19	P23.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_4			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_4			Mux input channel 6 of TIM module 0
	ASCLIN6_ARXF			Receive input
	P23.1	O0		General-purpose output
	GTM_TOUT42	O1		GTM muxed output
	ASCLIN1_ARTS	O2		Ready to send output
	—	O3		Reserved
	GTM_CLK0	O4		CGM generated clock
	CAN10_TXD	O5		CAN transmit output node 0
	CCU_EXTCLK0	O6		External Clock 0
	ASCLIN6_ASCLK	O7		Shift clock output
U20	P23.2	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_5			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_5			Mux input channel 6 of TIM module 0
	ASCLIN7_ARXC			Receive input
	P23.2	O0		General-purpose output
	GTM_TOUT43	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	CAN12_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	—	O7		Reserved

表 2-12 端口 P23 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
T19	P23.3	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN7_4			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_4			Mux input channel 7 of TIM module 0
	ASCLIN6_ARXA			Receive input
	CAN12_RXDC			CAN receive input node 2
	P23.3	O0		General-purpose output
	GTM_TOUT44	O1		GTM muxed output
	ASCLIN7_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
T20	P23.4	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN7_5			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_5			Mux input channel 7 of TIM module 0
	P23.4	O0		General-purpose output
	GTM_TOUT45	O1		GTM muxed output
	ASCLIN6_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
T17	P23.5	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_7			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_7			Mux input channel 2 of TIM module 0
	P23.5	O0		General-purpose output
	GTM_TOUT46	O1		GTM muxed output
	ASCLIN6_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-13 端口 P32 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
Y17	P32.0	I	SLOW / PU1 / VEXT / ES	**General-purpose input** P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
	GTM_TIM2_IN2_5			**Mux input channel 2 of TIM module 2**
	P32.0	O0		**General-purpose output**
	GTM_TOUT36	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
W17	P32.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input** P32.1 / External Pass Device gate control for EVRC
	P32.1	O0		**General-purpose output**
	GTM_TOUT37	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
Y18	P32.2	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN3_8			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_8			**Mux input channel 3 of TIM module 0**
	CAN03_RXDB			**CAN receive input node 3**
	ASCLIN3_ARXD			**Receive input**
	P32.2	O0		**General-purpose output**
	GTM_TOUT38	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	PMS_DCDCSYNCO	O6		**DC-DC synchronization output**
	—	O7		**Reserved**

表 2-13 端口 P32 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
Y19	P32.3	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN4_5			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_5			Mux input channel 4 of TIM module 0
	P32.3	O0		General-purpose output
	GTM_TOUT39	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	—	O3		Reserved
	ASCLIN3_ASCLK	O4		Shift clock output
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	—	O6		Reserved
	—	O7		Reserved
W18	P32.4	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN5_5			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_5			Mux input channel 5 of TIM module 0
	ASCLIN1_ACTSB			Clear to send input
	P32.4	O0		General-purpose output
	GTM_TOUT40	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	GTM_CLK1	O4		CGM generated clock
	—	O5		Reserved
	CCU_EXTCLK1	O6		External Clock 1
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1
	PMS_DCDCSYNCO	O		DC-DC synchronization output

表 2-14 端口 P33 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
W10	P33.0	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN4_6			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_6			Mux input channel 4 of TIM module 0
	EDSADC_ITR0E			Trigger/Gate input, channel 0
	IOM_PIN_0			GPIO pad input to FPC
	GTM_DTMT1_2			CDTM1_DTM0
	P33.0	O0		General-purpose output
	GTM_TOUT22	O1		GTM muxed output
	IOM_MON0_0			Monitor input 0
	IOM_GTM_0			GTM-provided inputs to EXOR combiner
	ASCLIN5_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
Y10	P33.1	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN5_6			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_6			Mux input channel 5 of TIM module 0
	EDSADC_ITR1E			Trigger/Gate input, channel 1
	PSI5_RX0C			RXD inputs (receive data) channel 0
	EDSADC_DSCIN2B			Modulator clock input, channel 2
	SENT_SENT9C			Receive input channel 9
	ASCLIN8_ARXC			Receive input
	IOM_PIN_1			GPIO pad input to FPC
	P33.1	O0		General-purpose output
	GTM_TOUT23	O1		GTM muxed output
	IOM_MON0_1			Monitor input 0
	IOM_GTM_1			GTM-provided inputs to EXOR combiner
	ASCLIN3_ASLSO	O2		Slave select signal output
	QSPI2_SCLK	O3		Master SPI clock output
	EDSADC_DSCOUT2	O4		Modulator clock output
	EVADC_EMUX02	O5		Control of external analog multiplexer interface 0
	—	O6		Reserved
	—	O7		Reserved

表 2-14 端口 P33 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
W11	P33.2	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN6_6			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_6			Mux input channel 6 of TIM module 0
	EDSADC_ITR2E			Trigger/Gate input, channel 2
	SENT_SENT8C			Receive input channel 8
	EDSADC_DSDIN2B			Digital datastream input, channel 2
	IOM_PIN_2			GPIO pad input to FPC
	P33.2	O0		General-purpose output
	GTM_TOUT24	O1		GTM muxed output
	IOM_MON0_2			Monitor input 0
	IOM_GTM_2			GTM-provided inputs to EXOR combiner
	ASCLIN3_ASCLK	O2		Shift clock output
	QSPI2_SLSO10	O3		Master slave select output
	PSI5_TX0	O4		TXD outputs (send data)
	IOM_MON1_14			Monitor input 1
	IOM_REF1_14			Reference input 1
	EVADC_EMUX01	O5		Control of external analog multiplexer interface 0
	—	O6		Reserved
	—	O7		Reserved
Y11	P33.3	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN7_6			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_6			Mux input channel 7 of TIM module 0
	PSI5_RX1C			RXD inputs (receive data) channel 1
	SENT_SENT7C			Receive input channel 7
	EDSADC_DSCIN1B			Modulator clock input, channel 1
	IOM_PIN_3			GPIO pad input to FPC
	P33.3	O0		General-purpose output
	GTM_TOUT25	O1		GTM muxed output
	IOM_MON0_3			Monitor input 0
	IOM_GTM_3			GTM-provided inputs to EXOR combiner
	ASCLIN5_ASCLK	O2		Shift clock output
	—	O3		Reserved
	EDSADC_DSCOUT1	O4		Modulator clock output
	EVADC_EMUX00	O5		Control of external analog multiplexer interface 0
	—	O6		Reserved
	—	O7		Reserved

表 2-14 端口 P33 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
W12	P33.4	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN0_10			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_10			Mux input channel 0 of TIM module 0
	EDSADC_ITR0F			Trigger/Gate input, channel 0
	SENT_SENT6C			Receive input channel 6
	EDSADC_DSDIN1B			Digital datastream input, channel 1
	CCU61_CTRAPC			Trap input capture
	ASCLIN5_ARXB			Receive input
	IOM_PIN_4			GPIO pad input to FPC
	P33.4	O0		General-purpose output
	GTM_TOUT26	O1		GTM muxed output
	IOM_MON0_4			Monitor input 0
	IOM_GTM_4			GTM-provided inputs to EXOR combiner
	ASCLIN2_ARTS	O2		Ready to send output
	QSPI2_SLSO12	O3		Master slave select output
	PSI5_TX1	O4		TXD outputs (send data)
	IOM_MON1_15			Monitor input 1
	EVADC_EMUX12	O5		Control of external analog multiplexer interface 1
	EVADC_FC0BFLOUT	O6		Boundary flag output, FC channel 0
	CAN13_TXD	O7		CAN transmit output node 3

表 2-14 端口 P33 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
Y12	P33.5	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN1_8			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_8			Mux input channel 1 of TIM module 0
	EDSADC_DSCIN0B			Modulator clock input, channel 0
	EDSADC_ITR1F			Trigger/Gate input, channel 1
	GPT120_T4EUDB			Count direction control input of timer T4
	PSI5S_RXC			RX data input
	ASCLIN2_ACTSB			Clear to send input
	CCU61_CCPOS2C			Hall capture input 2
	SENT_SENT5C			Receive input channel 5
	CAN13_RXDB			CAN receive input node 3
	IOM_PIN_5			GPIO pad input to FPC
	P33.5	O0		General-purpose output
	GTM_TOUT27	O1		GTM muxed output
	IOM_MON0_5			Monitor input 0
	IOM_GTM_5			GTM-provided inputs to EXOR combiner
	QSPI0_SLSO7	O2		Master slave select output
	QSPI1_SLSO7	O3		Master slave select output
	EDSADC_DSCOUT0	O4		Modulator clock output
	EVADC_EMUX11	O5		Control of external analog multiplexer interface 1
	—	O6		Reserved
	ASCLIN5_ASLSO	O7		Slave select signal output

表 2-14 端口 P33 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
W13	P33.6	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN2_9			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_9			Mux input channel 2 of TIM module 0
	EDSADC_ITR2F			Trigger/Gate input, channel 2
	GPT120_T2EUDB			Count direction control input of timer T2
	SENT_SENT4C			Receive input channel 4
	CCU61_CCPOS1C			Hall capture input 1
	EDSADC_DSDIN0B			Digital datastream input, channel 0
	ASCLIN8_ARXD			Receive input
	IOM_PIN_6			GPIO pad input to FPC
	P33.6	O0		General-purpose output
	GTM_TOUT28	O1		GTM muxed output
	IOM_MON0_6			Monitor input 0
	IOM_GTM_6			GTM-provided inputs to EXOR combiner
	ASCLIN2_ASLSO	O2		Slave select signal output
	QSPI2_SLSO11	O3		Master slave select output
	—	O4		Reserved
	EVADC_EMUX10	O5		Control of external analog multiplexer interface 1
	EVADC_FC1BFLOUT	O6		Boundary flag output, FC channel 1
	PSI5S_TX	O7		TX data output

表 2-14 端口 P33 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
Y13	P33.7	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN3_9			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_9			Mux input channel 3 of TIM module 0
	CAN00_RXDE			CAN receive input node 0
	GPT120_T2INB			Trigger/gate input of timer T2
	CCU61_CCPOS0C			Hall capture input 0
	SCU_E_REQ4_0			ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	IOM_PIN_7			GPIO pad input to FPC
	P33.7	O0		General-purpose output
	GTM_TOUT29	O1		GTM muxed output
	IOM_MON0_7			Monitor input 0
	IOM_GTM_7			GTM-provided inputs to EXOR combiner
	ASCLIN2_ASCLK	O2		Shift clock output
	—	O3		Reserved
	ASCLIN8_ATX	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-14 端口 P33 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
W14	P33.8	I	FAST / HighZ / VEVRSB	General-purpose input
	GTM_TIM1_IN4_7			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_7			Mux input channel 4 of TIM module 0
	ASCLIN2_ARXE			Receive input
	SCU_EMGSTOP_PORT_A			Emergency stop Port Pin A input request
	IOM_PIN_8			GPIO pad input to FPC
	P33.8	O0		General-purpose output
	GTM_TOUT30	O1		GTM muxed output
	IOM_MON0_8			Monitor input 0
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	—	O3		Reserved
	—	O4		Reserved
	CAN00_TXD	O5		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	—	O6		Reserved
	CCU61_COUT62	O7		T12 PWM channel 62
	IOM_MON1_13			Monitor input 1
	IOM_REF1_8			Reference input 1
	SMU_FSP0	O		FSP[1..0] Output Signals - Generated by SMU_core

表 2-14 端口 P33 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
Y14	P33.9	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN1_9			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_9			Mux input channel 1 of TIM module 0
	IOM_PIN_9			GPIO pad input to FPC
	P33.9	O0		General-purpose output
	GTM_TOUT31	O1		GTM muxed output
	IOM_MON0_9			Monitor input 0
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	—	O3		Reserved
	ASCLIN2_ASCLK	O4		Shift clock output
	CAN01_TXD	O5		CAN transmit output node 1
	IOM_MON2_6			Monitor input 2
	IOM_REF2_6			Reference input 2
	ASCLIN0_ATX	O6		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	CCU61_CC62	O7		T12 PWM channel 62
	IOM_MON1_10			Monitor input 1
	IOM_REF1_11			Reference input 1

表 2-14 端口 P33 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
W15	P33.10	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN0_9			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_9			Mux input channel 0 of TIM module 0
	CAN01_RXDD			CAN receive input node 1
	ASCLIN0_ARXD			Receive input
	IOM_PIN_10			GPIO pad input to FPC
	P33.10	O0		General-purpose output
	GTM_TOUT32	O1		GTM muxed output
	IOM_MON0_10			Monitor input 0
	QSPI1_SLSO6	O2		Master slave select output
	—	O3		Reserved
	ASCLIN1_ASLSO	O4		Slave select signal output
	PSI5S_CLK	O5		PSI5S CLK is a clock that can be used on a pin to drive the external PHY.
	—	O6		Reserved
	CCU61_COUT61	O7		T12 PWM channel 61
	IOM_MON1_12			Monitor input 1
	IOM_REF1_9			Reference input 1
	SMU_FSP1	O		FSP[1..0] Output Signals - Generated by SMU_core
Y15	P33.11	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN2_8			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_8			Mux input channel 2 of TIM module 0
	IOM_PIN_11			GPIO pad input to FPC
	P33.11	O0		General-purpose output
	GTM_TOUT33	O1		GTM muxed output
	IOM_MON0_11			Monitor input 0
	ASCLIN1_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	EDSADC_CGPWMN	O6		Negative carrier generator output
	CCU61_CC61	O7		T12 PWM channel 61
	IOM_MON1_9			Monitor input 1
	IOM_REF1_12			Reference input 1

表 2-14 端口 P33 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
W16	P33.12	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM2_IN0_6			Mux input channel 0 of TIM module 2
	CAN00_RXDD			CAN receive input node 0
	PMS_PINBWKP			PINB (P33.12) pin input
	IOM_PIN_12			GPIO pad input to FPC
	P33.12	O0		General-purpose output
	GTM_TOUT34	O1		GTM muxed output
	IOM_MON0_12			Monitor input 0
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	—	O3		Reserved
	ASCLIN1_ASCLK	O4		Shift clock output
	—	O5		Reserved
	EDSADC_CGPWMP	O6		Positive carrier generator output
	CCU61_COUT60	O7		T12 PWM channel 60
	IOM_MON1_11			Monitor input 1
	IOM_REF1_10			Reference input 1
Y16	P33.13	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM2_IN1_5			Mux input channel 1 of TIM module 2
	ASCLIN1_ARXF			Receive input
	EDSADC_SGNB			Carrier sign signal input
	P33.13	O0		General-purpose output
	GTM_TOUT35	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	—	O3		Reserved
	QSPI2_SLSO6	O4		Master slave select output
	CAN00_TXD	O5		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	—	O6		Reserved
	CCU61_CC60	O7		T12 PWM channel 60
	IOM_MON1_8			Monitor input 1
	IOM_REF1_13			Reference input 1

表 2-15 模拟输入

Ball	Symbol	Ctrl.	Buffer Type	Function
T10	AN0	I	D / HighZ / VDDM	**Analog Input 0**
	EVADC_G0CH0			**Analog input channel 0, group 0**
	EDSADC_EDS3PA			**Positive analog input channel 3, pin A**
U10	AN1	I	D / HighZ / VDDM	**Analog Input 1**
	EVADC_G0CH1			**Analog input channel 1, group 0**
	EDSADC_EDS3NA			**Negative analog input channel 3, pin A**
W9	AN2	I	D / HighZ / VDDM	**Analog Input 2**
	EVADC_G0CH2			**Analog input channel 2, group 0**
	EDSADC_EDS0PA			**Positive analog input channel 0, pin A**
U9	AN3	I	D / HighZ / VDDM	**Analog Input 3**
	EVADC_G0CH3			**Analog input channel 3, group 0**
	EDSADC_EDS0NA			**Negative analog input channel 0, pin A**
T9	AN4	I	D / HighZ / VDDM	**Analog Input 4**
	EVADC_G0CH4			**Analog input channel 4, group 0**
Y9	AN5	I	D / HighZ / VDDM	**Analog Input 5**
	EVADC_G0CH5			**Analog input channel 5, group 0**
T8	AN6	I	D / HighZ / VDDM	**Analog Input 6**
	EVADC_G0CH6			**Analog input channel 6, group 0**
U8	AN7	I	D / HighZ / VDDM	**Analog Input 7**
	EVADC_G0CH7			**Analog input channel 7, group 0**
W8	AN8	I	D / HighZ / VDDM	**Analog Input 8**
	EVADC_G1CH0			**Analog input channel 0, group 1**
U7	AN9	I	D / HighZ / VDDM	**Analog Input 9**
	EVADC_G1CH1			**Analog input channel 1, group 1**
Y8	AN10	I	D / HighZ / VDDM	**Analog Input 10**
	EVADC_G1CH2			**Analog input channel 2, group 1**
W7	AN11	I	D / HighZ / VDDM	**Analog Input 11**
	EVADC_G1CH3			**Analog input channel 3, group 1**
T7	AN12	I	D / HighZ / VDDM	**Analog Input 12**
	EVADC_G1CH4			**Analog input channel 4, group 1**
	EDSADC_EDS0PB			**Positive analog input channel 0, pin B**
W6	AN13	I	D / HighZ / VDDM	**Analog Input 13**
	EVADC_G1CH5			**Analog input channel 5, group 1**
	EDSADC_EDS0NB			**Negative analog input channel 0, pin B**
U6	AN14	I	D / HighZ / VDDM	**Analog Input 14**
	EVADC_G1CH6			**Analog input channel 6, group 1**
	EDSADC_EDS3PB			**Positive analog input channel 3, pin B**

表 2-15 模拟输入（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
T6	AN15	I	D / HighZ / VDDM	**Analog Input 15**
	EVADC_G1CH7			**Analog input channel 7, group 1**
	EDSADC_EDS3NB			**Negative analog input channel 3, pin N**
W5	AN16	I	D / HighZ / VDDM	**Analog Input 16**
	EVADC_G2CH0			**Analog input channel 0, group 2**
	EVADC_FC0CH0			**Analog input FC channel 0**
U5	AN17	I	D / HighZ / VDDM	**Analog Input 17**
	EVADC_G2CH1			**Analog input channel 1, group 2**
	EVADC_FC1CH0			**Analog input FC channel 1**
W4	AN18	I	D / HighZ / VDDM	**Analog Input 18**
	EVADC_G2CH2			**Analog input channel 2, group 2**
W3	AN19	I	D / HighZ / VDDM	**Analog Input 19**
	EVADC_G2CH3			**Analog input channel 3, group 2**
Y3	AN20	I	D / HighZ / VDDM	**Analog Input 20**
	EVADC_G2CH4			**Analog input channel 4, group 2**
	EDSADC_EDS2PA			**Positive analog input channel 2, pin A**
Y2	AN21	I	D / HighZ / VDDM	**Analog Input 21**
	EVADC_G2CH5			**Analog input channel 5, group 2**
	EDSADC_EDS2NA			**Negative analog input channel 2, pin A**
T5	AN22	I	D / HighZ / VDDM	**Analog Input 22**
	EVADC_G2CH6			**Analog input channel 6, group 2**
R5	AN23	I	D / HighZ / VDDM	**Analog Input 23**
	EVADC_G2CH7			**Analog input channel 7, group 2**
W2	AN24/P40.0	I	S / HighZ / VDDM	**Analog Input 24**
	SENT_SENT0A			**Receive input channel 0**
	EVADC_G3CH0			**Analog input channel 0, group 3**
	CCU60_CCPOS0D			**Hall capture input 0**
	EDSADC_EDS2PB			**Positive analog input channel 2, pin B**
W1	AN25/P40.1	I	S / HighZ / VDDM	**Analog Input 25**
	SENT_SENT1A			**Receive input channel 1**
	EVADC_G3CH1			**Analog input channel 1, group 3**
	CCU60_CCPOS1B			**Hall capture input 1**
	EDSADC_EDS2NB			**Negative analog input channel 2, pin B**
V2	AN26/P40.2	I	S / HighZ / VDDM	**Analog Input 26**
	SENT_SENT2A			**Receive input channel 2**
	EVADC_G3CH2			**Analog input channel 2, group 3**
	CCU60_CCPOS1D			**Hall capture input 1**

表 2-15 模拟输入（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
V1	AN27/P40.3	I	S / HighZ / VDDM	**Analog Input 27**
	SENT_SENT3A			**Receive input channel 3**
	EVADC_G3CH3			**Analog input channel 3, group 3**
	CCU60_CCPOS2B			**Hall capture input 2**
U2	AN28	I	D / HighZ / VDDM	**Analog Input 28**
	EVADC_G3CH4			**Analog input channel 4, group 3**
U1	AN29	I	D / HighZ / VDDM	**Analog Input 29**
	EVADC_G3CH5			**Analog input channel 5, group 3**
T4	AN30	I	D / HighZ / VDDM	**Analog Input 30**
	EVADC_G3CH6			**Analog input channel 6, group 3**
R4	AN31	I	D / HighZ / VDDM	**Analog Input 31**
	EVADC_G3CH7			**Analog input channel 7, group 3**
P4	AN32/P40.4	I	S / HighZ / VDDM	**Analog Input 32**
	SENT_SENT4A			**Receive input channel 4**
	EVADC_G8CH0			**Analog input channel 0, group 8**
	CCU60_CCPOS2D			**Hall capture input 2**
R1	AN33/P40.5	I	S / HighZ / VDDM	**Analog Input 33**
	SENT_SENT5A			**Receive input channel 5**
	EVADC_G8CH1			**Analog input channel 1, group 8**
	CCU61_CCPOS0D			**Hall capture input 0**
P5	AN34	I	D / HighZ / VDDM	**Analog Input 34**
	EVADC_G8CH2			**Analog input channel 2, group 8**
R2	AN35	I	D / HighZ / VDDM	**Analog Input 35**
	EVADC_G8CH3			**Analog input channel 3, group 8**
N4	AN36/P40.6	I	S / HighZ / VDDM	**Analog Input 36**
	SENT_SENT6A			**Receive input channel 6**
	EVADC_G8CH4			**Analog input channel 4, group 8**
	CCU61_CCPOS1B			**Hall capture input 1**
	EDSADC_EDS1PA			**Positive analog input channel 1, pin A**
P2	AN37/P40.7	I	S / HighZ / VDDM	**Analog Input 37**
	SENT_SENT7A			**Receive input channel 7**
	EVADC_G8CH5			**Analog input channel 5, group 8**
	CCU61_CCPOS1D			**Hall capture input 1**
	EDSADC_EDS1NA			**Negative analog input channel 1, pin A**

表 2-15 模拟输入（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
N5	AN38/P40.8	I	S / HighZ / VDDM	**Analog Input 38**
	SENT_SENT8A			**Receive input channel 8**
	EVADC_G8CH6			**Analog input channel 6, group 8**
	CCU61_CCPOS2B			**Hall capture input 2**
	EDSADC_EDS1PB			**Positive analog input channel 1, pin B**
P1	AN39/P40.9	I	S / HighZ / VDDM	**Analog Input 39**
	SENT_SENT9A			**Receive input channel 9**
	EVADC_G8CH7			**Analog input channel 7, group 8**
	CCU61_CCPOS2D			**Hall capture input 2**
	EDSADC_EDS1NB			**Negative analog input channel 1, pin B**
M5	AN40	I	D / HighZ / VDDM	**Analog Input 40**
	EVADC_G8CH8			**Analog input channel 8, group 8**
M4	AN41	I	D / HighZ / VDDM	**Analog Input 41**
	EVADC_G8CH9			**Analog input channel 9, group 8**
L5	AN42	I	D / HighZ / VDDM	**Analog Input 42**
	EVADC_G8CH10			**Analog input channel 10, group 8**
L4	AN43	I	D / HighZ / VDDM	**Analog Input 43**
	EVADC_G8CH11			**Analog input channel 11, group 8**
N1	AN44	I	D / HighZ / VDDM	**Analog Input 44**
	EVADC_G8CH12			**Analog input channel 12, group 8**
	EDSADC_EDS1PC			**Positive analog input channel 1, pin C**
N2	AN45	I	D / HighZ / VDDM	**Analog Input 45**
	EVADC_G8CH13			**Analog input channel 13, group 8**
	EDSADC_EDS1NC			**Negative analog input channel 1, pin C**
M1	AN46	I	D / HighZ / VDDM	**Analog Input 46**
	EVADC_G8CH14			**Analog input channel 14, group 8**
	EDSADC_EDS1PD			**Positive analog input channel 1, pin D**
M2	AN47	I	D / HighZ / VDDM	**Analog Input 47**
	EVADC_G8CH15			**Analog input channel 15, group 8**
	EDSADC_EDS1ND			**Negative analog input channel 1, pin D**

注释：端口引脚P32.0 和P32.1 是双向引脚，具有以下两个功能：

1. *如果将这些引脚用作标准GPIO，则可以使用P32.0 和P32.1 引脚配置表中定义的功能。*
2. *如果引脚用作外部MOSFET 的预驱动器（内部DCDC 情况），P32.0 和P32.1 将充当名为VGATE1N 和VGATE1P 的模拟IO。*

表 2-16 系统 I/O

Ball	Symbol	Ctrl.	Buffer Type	Function
Y17	VGATE1N	O	—	**DCDC N ch. MOSFET gate driver output** P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
W17	VGATE1P	O	—	**DCDC P ch. MOSFET gate driver output** P32.1 / External Pass Device gate control for EVRC
M20	XTAL1	I	XTAL / VEXT	**XTAL pad1** XTAL1. Main Oscillator/PLL/Clock Generator Input.
M19	XTAL2	O	XTAL / VEXT	**XTAL pad2** XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT
K16	TMS	I	FAST / PD2 / VEXT	**JTAG Module State Machine Control Input**
	DAP1	I/O		**DAP: DAP1 Data I/O**
L19	$\overline{\text{TRST}}$	I	FAST / PU2 / VEXT	**JTAG Module Reset/Enable Input**
J16	TCK	I	FAST / PD2 / VEXT	**JTAG Module Clock Input**
	DAP0	I		**DAP: DAP0 Clock Input**
G16	$\overline{\text{ESR1}}$	I/O	FAST / PU1 / VEXT	**ESR1 Port Pin input - can be used to trigger a reset or an NMI** ESR1: External System Request Reset 1. Default NMI function. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
	PMS_ESR1WKP	I		**ESR1 pin input**
G17	$\overline{\text{PORST}}$	I/O	PORST / PD / VEXT	**PORST pin** Power On Reset Input. Additional strong PD in case of power fail.

表 2-16 系统 I/O （续）

Ball	Symbol	Ctrl.	Buffer Type	Function
F16	$\overline{\text{ESR0}}$	I/O	FAST / OD / VEXT	**ESR0 Port Pin input - can be used to trigger a reset or an NMI** ESR0: External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
	PMS_ESR0WKP	I		**ESR0 pin input**

表 2-17 电源

Ball	Symbol	Ctrl.	Buffer Type	Function
Y5	VDDM	I	—	**ADC Analog Power Supply (5V / 3.3V)**
D5	VFLEX	I	—	**Digital Power Supply for Flex Port Pads (5V / 3.3V)**
P8, P13, N7, N14, E15, H14, D16, G13, G8, H7	VDD	I	—	**Digital Core Power Supply (1.25V)**
A2, B3, V19, W20	VEXT	I	—	**External Power Supply (5V / 3.3V)**
B18, A19	VDDP3	I	—	**Flash Power Supply (3.3V)**
B2, D4, E5, T16, U17, W19, Y20, E16, D17, B19, A20	VSS	I	—	**Digital Ground**
Y4	VSSM	I	—	**Analog Ground for VDDM**

表 2-17 电源（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
P9, P12, N9, N10, N11, N12, M7, M8, M10, M11, M13, M14, L8, L9, L10, L11, L12, L13, K8, K9, K10, K11, K12, K13, J7, J8, J10, J11, J13, J14, H9, H10, H11, H12, G9, G10, G11, G12, L14, P10, P11, K7, L7	VSS	I	—	**Digital Ground**
L20	VSS	I	—	**Oscillator Ground**
Y6	VAREF1	I	—	**Positive Analog Reference Voltage 1**
Y7	VAGND1	I	—	**Negative Analog Reference Voltage 1**
E4, F4, F5, G4, G5, H4, H5, J5, K14, L16, L17, M16, M17, N16, N17, P16, P17, R16, R17, T1, T2, T12, T13, T14, T15, U11, U12, U13, U14, U15, U16	NC	I	—	**Not connected. These pins are reserved for future extensions and shall not be connected externally**
A1, Y1, U4	NC1	I	—	**Not connected. These pins are not connected on package level and will not be used for future extensions**
T11	VEVRSB	I	—	**Standby Power Supply (5V / 3.3V) for the Standby SRAM**
N19	VDD	I	—	**Digital Power Supply for Oscillator (1.25V)**
N20	VEXT	I	—	**Digital Power Supply for Oscillator (shall be supplied with same level as used for VEXT)**

2.2 TC36x LFBGA-180 封装变体引脚配置

表 2-18 端口 00 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
G4	P00.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN0_1			**Mux input channel 0 of TIM module 2**
	CCU61_CTRAPA			**Trap input capture**
	CCU60_T12HRE			**External timer start 12**
	MSC0_INJ0			**Injection signal from port**
	GETH_MDIOA			**MDIO Input**
	P00.0	O0		**General-purpose output**
	GTM_TOUT9	O1		**GTM muxed output**
	IOM_REF0_9			**Reference input 0**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN3_ATX	O3		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O4		**Reserved**
	CAN10_TXD	O5		**CAN transmit output node 0**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
	GETH_MDIO	O		**MDIO Output**

表 2-18 端口 P00 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
H4	P00.1	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN1_1			Mux input channel 1 of TIM module 2
	CCU60_CC60INB			T12 capture input 60
	ASCLIN3_ARXE			Receive input
	CAN10_RXDA			CAN receive input node 0
	PSI5_RX0A			RXD inputs (receive data) channel 0
	CCU61_CC60INA			T12 capture input 60
	SENT_SENT0B			Receive input channel 0
	EVADC_G9CH11	AI		Analog input channel 11, group 9
	P00.1	O0		General-purpose output
	GTM_TOUT10	O1		GTM muxed output
	IOM_REF0_10			Reference input 0
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	SENT_SPC0	O6		Transmit output
	CCU61_CC60	O7		T12 PWM channel 60
	IOM_MON1_8			Monitor input 1
	IOM_REF1_13			Reference input 1

表 2-18 端口 P00 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
F3	P00.2	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM2_IN1_2			**Mux input channel 1 of TIM module 2**
	SENT_SENT1B			**Receive input channel 1**
	EVADC_G9CH10	AI		**Analog input channel 10, group 9**
	P00.2	O0		**General-purpose output**
	GTM_TOUT11	O1		**GTM muxed output**
	IOM_REF0_11			**Reference input 0**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	PSI5_TX0	O4		**TXD outputs (send data)**
	IOM_MON1_14			**Monitor input 1**
	IOM_REF1_14			**Reference input 1**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	QSPI3_SLSO4	O6		**Master slave select output**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**

表 2-18 端口 P00 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
F2	P00.3	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM2_IN2_1			Mux input channel 2 of TIM module 2
	CCU60_CC61INB			T12 capture input 61
	EDSADC_DSCIN3A			Modulator clock input, channel 3
	PSI5_RX1A			RXD inputs (receive data) channel 1
	CAN03_RXDA			CAN receive input node 3
	PSI5S_RXA			RX data input
	SENT_SENT2B			Receive input channel 2
	CCU61_CC61INA			T12 capture input 61
	EVADC_G9CH9	AI		Analog input channel 9, group 9
	P00.3	O0		General-purpose output
	GTM_TOUT12	O1		GTM muxed output
	IOM_REF0_12			Reference input 0
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	EDSADC_DSCOUT3	O4		Modulator clock output
	—	O5		Reserved
	SENT_SPC2	O6		Transmit output
	CCU61_CC61	O7		T12 PWM channel 61
	IOM_MON1_9			Monitor input 1
	IOM_REF1_12			Reference input 1

表 2-18 端口 P00 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
F1	P00.4	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM2_IN3_1			**Mux input channel 3 of TIM module 2**
	SCU_E_REQ2_2			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	SENT_SENT3B			**Receive input channel 3**
	EDSADC_DSDIN3A			**Digital datastream input, channel 3**
	EDSADC_SGNA			**Carrier sign signal input**
	ASCLIN10_ARXA			**Receive input**
	EVADC_G9CH8	AI		**Analog input channel 8, group 9**
	P00.4	O0		**General-purpose output**
	GTM_TOUT13	O1		**GTM muxed output**
	IOM_REF0_13			**Reference input 0**
	PSI5S_TX	O2		**TX data output**
	CAN11_TXD	O3		**CAN transmit output node 1**
	PSI5_TX1	O4		**TXD outputs (send data)**
	IOM_MON1_15			**Monitor input 1**
	—	O5		**Reserved**
	SENT_SPC3	O6		**Transmit output**
	CCU61_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_12			**Monitor input 1**
	IOM_REF1_9			**Reference input 1**

表 2-18 端口 P00 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
H3	P00.5	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM2_IN4_1			Mux input channel 4 of TIM module 2
	CCU60_CC62INB			T12 capture input 62
	EDSADC_DSCIN2A			Modulator clock input, channel 2
	CCU61_CC62INA			T12 capture input 62
	SENT_SENT4B			Receive input channel 4
	CAN11_RXDB			CAN receive input node 1
	GTM_DTMT1_1			CDTM1_DTM0
	EVADC_G9CH7	AI		Analog input channel 7, group 9
	P00.5	O0		General-purpose output
	GTM_TOUT14	O1		GTM muxed output
	IOM_REF0_14			Reference input 0
	EDSADC_CGPWMN	O2		Negative carrier generator output
	QSPI3_SLSO3	O3		Master slave select output
	EDSADC_DSCOUT2	O4		Modulator clock output
	EVADC_FC0BFLOUT	O5		Boundary flag output, FC channel 0
	SENT_SPC4	O6		Transmit output
	CCU61_CC62	O7		T12 PWM channel 62
	IOM_MON1_10			Monitor input 1
	IOM_REF1_11			Reference input 1
G3	P00.6	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM2_IN5_1			Mux input channel 5 of TIM module 2
	EDSADC_DSDIN2A			Digital datastream input, channel 2
	SENT_SENT5B			Receive input channel 5
	ASCLIN5_ARXA			Receive input
	EVADC_G9CH6	AI		Analog input channel 6, group 9
	P00.6	O0		General-purpose output
	GTM_TOUT15	O1		GTM muxed output
	IOM_REF0_15			Reference input 0
	EDSADC_CGPWMP	O2		Positive carrier generator output
	—	O3		Reserved
	—	O4		Reserved
	EVADC_EMUX10	O5		Control of external analog multiplexer interface 1
	SENT_SPC5	O6		Transmit output
	CCU61_COUT62	O7		T12 PWM channel 62
	IOM_MON1_13			Monitor input 1
	IOM_REF1_8			Reference input 1

表 2-18 端口 P00 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
G2	P00.7	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM2_IN6_1			Mux input channel 6 of TIM module 2
	CCU61_CC60INC			T12 capture input 60
	SENT_SENT6B			Receive input channel 6
	GPT120_T2INA			Trigger/gate input of timer T2
	CCU61_CCPOS0A			Hall capture input 0
	CCU60_T12HRB			External timer start 12
	GTM_DTMT0_2			CDTM0_DTM0
	EVADC_G9CH5	AI		Analog input channel 5, group 9
	P00.7	O0		General-purpose output
	GTM_TOUT16	O1		GTM muxed output
	ASCLIN5_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	EVADC_EMUX11	O5		Control of external analog multiplexer interface 1
	SENT_SPC6	O6		Transmit output
	CCU61_CC60	O7		T12 PWM channel 60
	IOM_MON1_8			Monitor input 1
	IOM_REF1_13			Reference input 1
G1	P00.8	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM2_IN7_1			Mux input channel 7 of TIM module 2
	CCU61_CC61INC			T12 capture input 61
	SENT_SENT7B			Receive input channel 7
	GPT120_T2EUDA			Count direction control input of timer T2
	CCU61_CCPOS1A			Hall capture input 1
	CCU60_T13HRB			External timer start 13
	ASCLIN10_ARXB			Receive input
	EVADC_G9CH4	AI		Analog input channel 4, group 9
	P00.8	O0		General-purpose output
	GTM_TOUT17	O1		GTM muxed output
	QSPI3_SLSO6	O2		Master slave select output
	ASCLIN10_ATX	O3		Transmit output
	—	O4		Reserved
	EVADC_EMUX12	O5		Control of external analog multiplexer interface 1
	SENT_SPC7	O6		Transmit output
	CCU61_CC61	O7		T12 PWM channel 61
	IOM_MON1_9			Monitor input 1
	IOM_REF1_12			Reference input 1

表 2-18 端口 P00 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
H2	P00.9	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM1_IN0_1			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_1			Mux input channel 0 of TIM module 0
	CCU61_CC62INC			T12 capture input 62
	SENT_SENT8B			Receive input channel 8
	CCU61_CCPOS2A			Hall capture input 2
	EDSADC_DSCIN1A			Modulator clock input, channel 1
	EDSADC_ITR3F			Trigger/Gate input, channel 3
	GPT120_T4EUDA			Count direction control input of timer T4
	CCU60_T13HRC			External timer start 13
	CCU60_T12HRC			External timer start 12
	EVADC_G9CH3	AI		Analog input channel 3, group 9
	P00.9	O0		General-purpose output
	GTM_TOUT18	O1		GTM muxed output
	QSPI3_SLSO7	O2		Master slave select output
	ASCLIN3_ARTS	O3		Ready to send output
	EDSADC_DSCOUT1	O4		Modulator clock output
	ASCLIN4_ATX	O5		Transmit output
	SENT_SPC8	O6		Transmit output
	CCU61_CC62	O7		T12 PWM channel 62
	IOM_MON1_10			Monitor input 1
	IOM_REF1_11			Reference input 1

表 2-18 端口 P00 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
H1	P00.12	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM1_IN3_1			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_1			**Mux input channel 3 of TIM module 0**
	ASCLIN3_ACTSA			**Clear to send input**
	EDSADC_DSDIN0A			**Digital datastream input, channel 0**
	ASCLIN4_ARXA			**Receive input**
	EVADC_G9CH0	AI		**Analog input channel 0, group 9**
	P00.12	O0		**General-purpose output**
	GTM_TOUT21	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_7			**Monitor input 1**
	IOM_REF1_7			**Reference input 1**

表 2-19 端口 P02 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
B1	P02.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_2			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_2			Mux input channel 0 of TIM module 0
	CCU61_CC60INB			T12 capture input 60
	ASCLIN2_ARXG			Receive input
	CCU60_CC60INA			T12 capture input 60
	SCU_E_REQ3_2			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	GTM_DTMA0_0			CDTM0_DTM4
	P02.0	O0		General-purpose output
	GTM_TOUT0	O1		GTM muxed output
	IOM_REF0_0			Reference input 0
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI3_SLSO1	O3		Master slave select output
	EDSADC_CGPWMN	O4		Negative carrier generator output
	CAN00_TXD	O5		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	ERAY0_TXDA	O6		Transmit Channel A
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
	IOM_REF1_6			Reference input 1

表 2-19 端口 P02 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
C1	P02.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN1_2			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_2			**Mux input channel 1 of TIM module 0**
	ERAY0_RXDA2			**Receive Channel A2**
	ASCLIN2_ARXB			**Receive input**
	CAN00_RXDA			**CAN receive input node 0**
	SCU_E_REQ2_1			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P02.1	O0		**General-purpose output**
	GTM_TOUT1	O1		**GTM muxed output**
	IOM_REF0_1			**Reference input 0**
	—	O2		**Reserved**
	QSPI3_SLSO2	O3		**Master slave select output**
	EDSADC_CGPWMP	O4		**Positive carrier generator output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**

表 2-19 端口 P02 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
C2	P02.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_2			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_2			Mux input channel 2 of TIM module 0
	CCU61_CC61INB			T12 capture input 61
	CCU60_CC61INA			T12 capture input 61
	P02.2	O0		General-purpose output
	GTM_TOUT2	O1		GTM muxed output
	IOM_REF0_2			Reference input 0
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI3_SLSO3	O3		Master slave select output
	PSI5_TX0	O4		TXD outputs (send data)
	IOM_MON1_14			Monitor input 1
	IOM_REF1_14			Reference input 1
	CAN02_TXD	O5		CAN transmit output node 2
	IOM_MON2_7			Monitor input 2
	IOM_REF2_7			Reference input 2
	ERAY0_TXDB	O6		Transmit Channel B
	CCU60_CC61	O7		T12 PWM channel 61
	IOM_MON1_1			Monitor input 1
	IOM_REF1_5			Reference input 1

表 2-19 端口 P02 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
D3	P02.3	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN3_2			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_2			Mux input channel 3 of TIM module 0
	ERAY0_RXDB2			Receive Channel B2
	CAN02_RXDB			CAN receive input node 2
	ASCLIN1_ARXG			Receive input
	PSI5_RX0B			RXD inputs (receive data) channel 0
	P02.3	O0		General-purpose output
	GTM_TOUT3	O1		GTM muxed output
	IOM_REF0_3			Reference input 0
	ASCLIN2_ASLSO	O2		Slave select signal output
	QSPI3_SLSO4	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT61	O7		T12 PWM channel 61
	IOM_MON1_4			Monitor input 1
	IOM_REF1_2			Reference input 1

表 2-19 端口 P02 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
D2	P02.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN4_1			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_1			**Mux input channel 4 of TIM module 0**
	CCU61_CC62INB			**T12 capture input 62**
	QSPI3_SLSIA			**Slave select input**
	CCU60_CC62INA			**T12 capture input 62**
	I2C0_SDAA			**Serial Data Input 0**
	CAN11_RXDA			**CAN receive input node 1**
	CAN0_ECTT1			**External CAN time trigger input**
	P02.4	O0		**General-purpose output**
	GTM_TOUT4	O1		**GTM muxed output**
	IOM_REF0_4			**Reference input 0**
	ASCLIN2_ASCLK	O2		**Shift clock output**
	QSPI3_SLSO0	O3		**Master slave select output**
	PSI5S_CLK	O4		**PSI5S CLK is a clock that can be used on a pin to drive the external PHY.**
	I2C0_SDA	O5		**Serial Data Output**
	ERAY0_TXENA	O6		**Transmit Enable Channel A**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

表 2-19 端口 P02 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
D1	P02.5	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN5_1			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_1			Mux input channel 5 of TIM module 0
	I2C0_SCLA			Serial Clock Input 0
	PSI5_RX1B			RXD inputs (receive data) channel 1
	PSI5S_RXB			RX data input
	QSPI3_MRSTA			Master SPI data input
	SENT_SENT3C			Receive input channel 3
	CAN0_ECTT2			External CAN time trigger input
	P02.5	O0		General-purpose output
	GTM_TOUT5	O1		GTM muxed output
	IOM_REF0_5			Reference input 0
	CAN11_TXD	O2		CAN transmit output node 1
	QSPI3_MRST	O3		Slave SPI data output
	IOM_MON2_3			Monitor input 2
	IOM_REF2_3			Reference input 2
	—	O4		Reserved
	I2C0_SCL	O5		Serial Clock Output
	ERAY0_TXENB	O6		Transmit Enable Channel B
	CCU60_COUT62	O7		T12 PWM channel 62
	IOM_MON1_5			Monitor input 1
	IOM_REF1_1			Reference input 1

表 2-19 端口 P02 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
E1	P02.6	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_1			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_1			Mux input channel 6 of TIM module 0
	CCU60_CC60INC			T12 capture input 60
	SENT_SENT2C			Receive input channel 2
	GPT120_T3INA			Trigger/gate input of core timer T3
	CCU60_CCPOS0A			Hall capture input 0
	CCU61_T12HRB			External timer start 12
	QSPI3_MTSRA			Slave SPI data input
	P02.6	O0		General-purpose output
	GTM_TOUT6	O1		GTM muxed output
	IOM_REF0_6			Reference input 0
	PSI5S_TX	O2		TX data output
	QSPI3_MTSR	O3		Master SPI data output
	PSI5_TX1	O4		TXD outputs (send data)
	IOM_MON1_15			Monitor input 1
	EVADC_EMUX00	O5		Control of external analog multiplexer interface 0
	—	O6		Reserved
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
	IOM_REF1_6			Reference input 1

表 2-19 端口 P02 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
E2	P02.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN7_1			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_1			**Mux input channel 7 of TIM module 0**
	CCU60_CC61INC			**T12 capture input 61**
	SENT_SENT1C			**Receive input channel 1**
	EDSADC_DSCIN3B			**Modulator clock input, channel 3**
	GPT120_T3EUDA			**Count direction control input of core timer T3**
	CCU60_CCPOS1A			**Hall capture input 1**
	QSPI3_SCLKA			**Slave SPI clock inputs**
	CCU61_T13HRB			**External timer start 13**
	P02.7	O0		**General-purpose output**
	GTM_TOUT7	O1		**GTM muxed output**
	IOM_REF0_7			**Reference input 0**
	—	O2		**Reserved**
	QSPI3_SCLK	O3		**Master SPI clock output**
	EDSADC_DSCOUT3	O4		**Modulator clock output**
	EVADC_EMUX01	O5		**Control of external analog multiplexer interface 0**
	SENT_SPC1	O6		**Transmit output**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**

表 2-19 端口 P02 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
E3	P02.8	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN0_2			**Mux input channel 0 of TIM module 2**
	CCU60_CC62INC			**T12 capture input 62**
	SENT_SENT0C			**Receive input channel 0**
	CCU60_CCPOS2A			**Hall capture input 2**
	EDSADC_DSDIN3B			**Digital datastream input, channel 3**
	EDSADC_ITR3E			**Trigger/Gate input, channel 3**
	GPT120_T4INA			**Trigger/gate input of timer T4**
	CCU61_T12HRC			**External timer start 12**
	CCU61_T13HRC			**External timer start 13**
	GTM_DTMA0_1			**CDTM0_DTM4**
	P02.8	O0		**General-purpose output**
	GTM_TOUT8	O1		**GTM muxed output**
	IOM_REF0_8			**Reference input 0**
	QSPI3_SLSO5	O2		**Master slave select output**
	ASCLIN8_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	EVADC_EMUX02	O5		**Control of external analog multiplexer interface 0**
	GETH_MDC	O6		**MDIO clock**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

表 2-20 端口 P10 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
C4	P10.0	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN4_2			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_2			Mux input channel 4 of TIM module 0
	GPT120_T6EUDB			Count direction control input of core timer T6
	ASCLIN11_ARXA			Receive input
	GETH_RXERC			Receive Error MII
	P10.0	O0		General-purpose output
	GTM_TOUT102	O1		GTM muxed output
	ASCLIN11_ATX	O2		Transmit output
	QSPI1_SLSO10	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
B3	P10.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_3			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_3			Mux input channel 1 of TIM module 0
	GPT120_T5EUDB			Count direction control input of timer T5
	QSPI1_MRSTA			Master SPI data input
	GTM_DTMT0_1			CDTM0_DTM0
	P10.1	O0		General-purpose output
	GTM_TOUT103	O1		GTM muxed output
	QSPI1_MTSR	O2		Master SPI data output
	QSPI1_MRST	O3		Slave SPI data output
	IOM_MON2_1			Monitor input 2
	IOM_REF2_1			Reference input 2
	MSC0_EN1	O4		Chip Select
	EVADC_FC1BFLOUT	O5		Boundary flag output, FC channel 1
	—	O6		Reserved
	—	O7		Reserved

表 2-20 端口 P10 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
A3	P10.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_3			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_3			Mux input channel 2 of TIM module 0
	CAN02_RXDE			CAN receive input node 2
	MSC0_SDI1			Upstream assynchronous input signal
	QSPI1_SCLKA			Slave SPI clock inputs
	GPT120_T6INB			Trigger/gate input of core timer T6
	SCU_E_REQ2_0			ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P10.2	O0		General-purpose output
	GTM_TOUT104	O1		GTM muxed output
	IOM_MON2_9			Monitor input 2
	—	O2		Reserved
	QSPI1_SCLK	O3		Master SPI clock output
	MSC0_EN0	O4		Chip Select
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
A2	P10.3	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN3_3			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_3			Mux input channel 3 of TIM module 0
	QSPI1_MTSRA			Slave SPI data input
	SCU_E_REQ3_0			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	GPT120_T5INB			Trigger/gate input of timer T5
	P10.3	O0		General-purpose output
	GTM_TOUT105	O1		GTM muxed output
	IOM_MON2_10			Monitor input 2
	—	O2		Reserved
	QSPI1_MTSR	O3		Master SPI data output
	MSC0_EN0	O4		Chip Select
	—	O5		Reserved
	CAN02_TXD	O6		CAN transmit output node 2
	IOM_MON2_7			Monitor input 2
	IOM_REF2_7			Reference input 2
	—	O7		Reserved

表 2-20 端口 P10 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
B4	P10.4	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_2			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_2			Mux input channel 6 of TIM module 0
	QSPI1_MTSRC			Slave SPI data input
	CCU60_CCPOS0C			Hall capture input 0
	GPT120_T3INB			Trigger/gate input of core timer T3
	ASCLIN11_ARXB			Receive input
	P10.4	O0		General-purpose output
	GTM_TOUT106	O1		GTM muxed output
	IOM_MON2_11			Monitor input 2
	—	O2		Reserved
	QSPI1_SLSO8	O3		Master slave select output
	QSPI1_MTSR	O4		Master SPI data output
	MSC0_EN0	O5		Chip Select
	—	O6		Reserved
	—	O7		Reserved
F4	P10.5	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_4			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_4			Mux input channel 2 of TIM module 0
	PMS_HWCFG4IN			HWCFG4 pin input
	MSC0_INJ1			Injection signal from port
	P10.5	O0		General-purpose output
	GTM_TOUT107	O1		GTM muxed output
	IOM_REF2_9			Reference input 2
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI3_SLSO8	O3		Master slave select output
	QSPI1_SLSO9	O4		Master slave select output
	GPT120_T6OUT	O5		External output for overflow/underflow detection of core timer T6
	ASCLIN2_ASLSO	O6		Slave select signal output
	—	O7		Reserved

表 2-20 端口 P10 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
E4	P10.6	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN3_4			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_4			Mux input channel 3 of TIM module 0
	ASCLIN2_ARXD			Receive input
	QSPI3_MTSRB			Slave SPI data input
	PMS_HWCFG5IN			HWCFG5 pin input
	P10.6	O0		General-purpose output
	GTM_TOUT108	O1		GTM muxed output
	IOM_REF2_10			Reference input 2
	ASCLIN2_ASCLK	O2		Shift clock output
	QSPI3_MTSR	O3		Master SPI data output
	GPT120_T3OUT	O4		External output for overflow/underflow detection of core timer T3
	—	O5		Reserved
	QSPI1_MRST	O6		Slave SPI data output
	IOM_MON2_1			Monitor input 2
	IOM_REF2_1			Reference input 2
	—	O7		Reserved

表 2-21 端口 P11 的功能

Ball	Symbol	Ctrl.	Buffer Type	Function
A6	P11.2	I	RFAST / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM2_IN1_3			Mux input channel 1 of TIM module 2
	P11.2	O0		General-purpose output
	GTM_TOUT95	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO5	O3		Master slave select output
	QSPI1_SLSO5	O4		Master slave select output
	MSC0_EN1	O5		Chip Select
	GETH_TXD1	O6		Transmit Data
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1

表 2-21 端口 P11 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
B6	P11.3	I	RFAST / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM2_IN2_2			Mux input channel 2 of TIM module 2
	MSC0_SDI3			Upstream assynchronous input signal
	QSPI1_MRSTB			Master SPI data input
	P11.3	O0		General-purpose output
	GTM_TOUT96	O1		GTM muxed output
	—	O2		Reserved
	QSPI1_MRST	O3		Slave SPI data output
	IOM_MON2_1			Monitor input 2
	IOM_REF2_1			Reference input 2
	ERAY0_TXDA	O4		Transmit Channel A
	—	O5		Reserved
	GETH_TXD0	O6		Transmit Data
	CCU60_COUT62	O7		T12 PWM channel 62
	IOM_MON1_5			Monitor input 1
	IOM_REF1_1			Reference input 1
C6	P11.6	I	RFAST / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM2_IN3_2			Mux input channel 3 of TIM module 2
	QSPI1_SCLKB			Slave SPI clock inputs
	P11.6	O0		General-purpose output
	GTM_TOUT97	O1		GTM muxed output
	ERAY0_TXENB	O2		Transmit Enable Channel B
	QSPI1_SCLK	O3		Master SPI clock output
	ERAY0_TXENA	O4		Transmit Enable Channel A
	MSC0_FCLP	O5		Shift-clock direct part of the differential signal
	GETH_TXEN	O6		Transmit Enable MII and RMII
	GETH_TCTL			Transmit Control for RGMII
	CCU60_COUT61	O7		T12 PWM channel 61
	IOM_MON1_4			Monitor input 1
	IOM_REF1_2			Reference input 1

表 2-21 端口 P11 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
D6	P11.8	I	SLOW / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM2_IN5_8			**Mux input channel 5 of TIM module 2**
	GETH_RXD2A			**Receive Data 2 MII and RGMII (RGMII can use RXD2A only)**
	CAN12_RXDD			**CAN receive input node 2**
	P11.8	O0		**General-purpose output**
	GTM_TOUT124	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
A5	P11.9	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM2_IN4_2			**Mux input channel 4 of TIM module 2**
	QSPI1_MTSRB			**Slave SPI data input**
	ERAY0_RXDA1			**Receive Channel A1**
	GETH_RXD1A			**Receive Data 1 MII, RMII and RGMII (RGMII can use RXD1A only)**
	P11.9	O0		**General-purpose output**
	GTM_TOUT98	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI1_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	MSC0_SOP	O5		**Data output - direct part of the differential signal**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**

表 2-21 端口 P11 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
B5	P11.10	I	FAST / RGMII_Input / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM2_IN5_2			Mux input channel 5 of TIM module 2
	GTM_TIM2_IN0_9			Mux input channel 0 of TIM module 2
	CAN03_RXDD			CAN receive input node 3
	ERAY0_RXDB1			Receive Channel B1
	ASCLIN1_ARXE			Receive input
	SCU_E_REQ6_3			ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	MSC0_SDI0			Upstream assynchronous input signal
	GETH_RXD0A			Receive Data 0 MII, RMII and RGMII (RGMII can use RXD0A only)
	QSPI1_SLSIA			Slave select input
	P11.10	O0		General-purpose output
	GTM_TOUT99	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO3	O3		Master slave select output
	QSPI1_SLSO3	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	CCU60_CC62	O7		T12 PWM channel 62
	IOM_MON1_0			Monitor input 1
	IOM_REF1_4			Reference input 1
C5	P11.11	I	FAST / RGMII_Input / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM2_IN6_2			Mux input channel 6 of TIM module 2
	GETH_CRSDVA			Carrier Sense / Data Valid combi-signal for RMII
	GETH_RXDVA			Receive Data Valid MII
	GETH_CRSB			Carrier Sense MII
	GETH_RCTLA			Receive Control for RGMII
	P11.11	O0		General-purpose output
	GTM_TOUT100	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO4	O3		Master slave select output
	QSPI1_SLSO4	O4		Master slave select output
	MSC0_EN0	O5		Chip Select
	ERAY0_TXENB	O6		Transmit Enable Channel B
	CCU60_CC61	O7		T12 PWM channel 61
	IOM_MON1_1			Monitor input 1
	IOM_REF1_5			Reference input 1

表 2-21 端口 P11 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
A4	P11.12	I	FAST / RGMII_Input / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM2_IN7_2			Mux input channel 7 of TIM module 2
	GETH_REFCLKA			Reference Clock input for RMII (50 MHz)
	GETH_TXCLKB			Transmit Clock Input for MII
	GETH_RXCLKA			Receive Clock MII
	P11.12	O0		General-purpose output
	GTM_TOUT101	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	GTM_CLK2	O3		CGM generated clock
	ERAY0_TXDB	O4		Transmit Channel B
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	CCU_EXTCLK1	O6		External Clock 1
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
	IOM_REF1_6			Reference input 1

表 2-22 端口 P13 的功能

Ball	Symbol	Ctrl.	Buffer Type	Function
A7	P13.0	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM2_IN5_3			Mux input channel 5 of TIM module 2
	ASCLIN10_ARXC			Receive input
	P13.0	O0		General-purpose output
	GTM_TOUT91	O1		GTM muxed output
	ASCLIN10_ATX	O2		Transmit output
	QSPI2_SCLKN	O3		Master SPI clock output (LVDS N line)
	MSC0_EN1	O4		Chip Select
	MSC0_FCLN	O5		Shift-clock inverted part of the differential signal
	—	O6		Reserved
	CAN10_TXD	O7		CAN transmit output node 0

表 2-22 端口 P13 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
B7	P13.1	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM2_IN6_3			Mux input channel 6 of TIM module 2
	I2C0_SCLB			Serial Clock Input 1
	CAN10_RXDD			CAN receive input node 0
	ASCLIN10_ARXD			Receive input
	P13.1	O0		General-purpose output
	GTM_TOUT92	O1		GTM muxed output
	—	O2		Reserved
	QSPI2_SCLKP	O3		Master SPI clock output (LVDS P line)
	—	O4		Reserved
	MSC0_FCLP	O5		Shift-clock direct part of the differential signal
	I2C0_SCL	O6		Serial Clock Output
	—	O7		Reserved
A8	P13.2	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM2_IN7_3			Mux input channel 7 of TIM module 2
	GPT120_CAPINA			Trigger input to capture value of timer T5 into CAPREL register
	I2C0_SDAB			Serial Data Input 1
	P13.2	O0		General-purpose output
	GTM_TOUT93	O1		GTM muxed output
	ASCLIN10_ASCLK	O2		Shift clock output
	QSPI2_MTSRN	O3		Master SPI data output (LVDS N line)
	MSC0_FCLP	O4		Shift-clock direct part of the differential signal
	MSC0_SON	O5		Data output - inverted part of the differential signal
	I2C0_SDA	O6		Serial Data Output
	—	O7		Reserved
B8	P13.3	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM2_IN0_3			Mux input channel 0 of TIM module 2
	P13.3	O0		General-purpose output
	GTM_TOUT94	O1		GTM muxed output
	ASCLIN10_ASLSO	O2		Slave select signal output
	QSPI2_MTSRP	O3		Master SPI data output (LVDS P line)
	—	O4		Reserved
	MSC0_SOP	O5		Data output - direct part of the differential signal
	—	O6		Reserved
	—	O7		Reserved

表 2-23 端口 P14 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
A9	P14.0	I	FAST / PU1 / VEXT / ES2	General-purpose input
	GTM_TIM1_IN3_5			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_5			Mux input channel 3 of TIM module 0
	P14.0	O0		General-purpose output
	GTM_TOUT80	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	ERAY0_TXDA	O3		Transmit Channel A
	ERAY0_TXDB	O4		Transmit Channel B
	CAN01_TXD	O5		CAN transmit output node 1
	IOM_MON2_6			Monitor input 2
	IOM_REF2_6			Reference input 2
	ASCLIN0_ASCLK	O6		Shift clock output
	CCU60_COUT62	O7		T12 PWM channel 62
	IOM_MON1_5			Monitor input 1
	IOM_REF1_1			Reference input 1

表 2-23 端口 P14 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
B10	P14.1	I	FAST / PU1 / VEXT / ES2	General-purpose input
	GTM_TIM1_IN4_3			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_3			Mux input channel 4 of TIM module 0
	ERAY0_RXDA3			Receive Channel A3
	ASCLIN0_ARXA			Receive input
	ERAY0_RXDB3			Receive Channel B3
	CAN01_RXDB			CAN receive input node 1
	SCU_E_REQ3_1			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	PMS_PINAWKP			PINA (P14.1) pin input
	P14.1	O0		General-purpose output
	GTM_TOUT81	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1
D9	P14.2	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN5_3			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_3			Mux input channel 5 of TIM module 0
	PMS_HWCFG2IN			HWCFG2 pin input
	P14.2	O0		General-purpose output
	GTM_TOUT82	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI2_SLSO1	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	ASCLIN2_ASCLK	O6		Shift clock output
	—	O7		Reserved

表 2-23 端口 P14 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
C11	P14.3	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_3			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_3			Mux input channel 6 of TIM module 0
	PMS_HWCFG3IN			HWCFG3 pin input
	ASCLIN2_ARXA			Receive input
	MSC0_SDI2			Upstream assynchronous input signal
	SCU_E_REQ1_0			ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P14.3	O0		General-purpose output
	GTM_TOUT83	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI2_SLSO3	O3		Master slave select output
	ASCLIN1_ASLSO	O4		Slave select signal output
	ASCLIN3_ASLSO	O5		Slave select signal output
	—	O6		Reserved
	—	O7		Reserved
C10	P14.4	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN7_2			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_2			Mux input channel 7 of TIM module 0
	PMS_HWCFG6IN			HWCFG6 pin input
	GTM_DTMT0_0			CDTM0_DTM0
	P14.4	O0		General-purpose output
	GTM_TOUT84	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	GETH_PPS	O6		Pulse Per Second
	—	O7		Reserved

表 2-23 端口 P14 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
B9	P14.5	I	FAST / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_4			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_4			Mux input channel 0 of TIM module 0
	PMS_HWCFG1IN			HWCFG1 pin input
	GTM_DTMA2_0			CDTM2_DTM4
	P14.5	O0		General-purpose output
	GTM_TOUT85	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	ERAY0_TXDB	O6		Transmit Channel B
	—	O7		Reserved
C9	P14.6	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_4			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_4			Mux input channel 1 of TIM module 0
	P14.6	O0		General-purpose output
	GTM_TOUT86	O1		GTM muxed output
	—	O2		Reserved
	QSPI2_SLSO2	O3		Master slave select output
	CAN13_TXD	O4		CAN transmit output node 3
	—	O5		Reserved
	ERAY0_TXENB	O6		Transmit Enable Channel B
	—	O7		Reserved
C7	P14.8	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN2_3			Mux input channel 2 of TIM module 2
	ERAY0_RXDA0			Receive Channel A0
	CAN02_RXDD			CAN receive input node 2
	ASCLIN1_ARXD			Receive input
	P14.8	O0		General-purpose output
	GTM_TOUT88	O1		GTM muxed output
	ASCLIN5_ASLSO	O2		Slave select signal output
	ASCLIN7_ASLSO	O3		Slave select signal output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-23 端口 P14 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
C8	P14.10	I	LVDS_R X / FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN4_3			Mux input channel 4 of TIM module 2
	QSPI2_MRSTFP			Master SPI data input (LVDS P line)
	P14.10	O0		General-purpose output
	GTM_TOUT90	O1		GTM muxed output
	—	O2		Reserved
	MSC0_EN0	O3		Chip Select
	ASCLIN1_ATX	O4		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	CAN02_TXD	O5		CAN transmit output node 2
	IOM_MON2_7			Monitor input 2
	IOM_REF2_7			Reference input 2
	ERAY0_TXDA	O6		Transmit Channel A
	—	O7		Reserved

表 2-24 端口 P15 的功能

Ball	Symbol	Ctrl.	Buffer Type	Function
A13	P15.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN3_4			Mux input channel 3 of TIM module 2
	P15.0	O0		General-purpose output
	GTM_TOUT71	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI0_SLSO13	O3		Master slave select output
	—	O4		Reserved
	CAN02_TXD	O5		CAN transmit output node 2
	IOM_MON2_7			Monitor input 2
	IOM_REF2_7			Reference input 2
	ASCLIN1_ASCLK	O6		Shift clock output
	—	O7		Reserved

表 2-24 端口 P15 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
A12	P15.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN4_4			Mux input channel 4 of TIM module 2
	CAN02_RXDA			CAN receive input node 2
	ASCLIN1_ARXA			Receive input
	QSPI2_SLSIB			Slave select input
	SCU_E_REQ7_2			ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P15.1	O0		General-purpose output
	GTM_TOUT72	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI2_SLSO5	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
B12	P15.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN5_4			Mux input channel 5 of TIM module 2
	QSPI2_SLSIA			Slave select input
	QSPI2_MRSTE			Master SPI data input
	P15.2	O0		General-purpose output
	GTM_TOUT73	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	QSPI2_SLSO0	O3		Master slave select output
	—	O4		Reserved
	CAN01_TXD	O5		CAN transmit output node 1
	IOM_MON2_6			Monitor input 2
	IOM_REF2_6			Reference input 2
	ASCLIN0_ASCLK	O6		Shift clock output
	—	O7		Reserved

表 2-24 端口 P15 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
A10	P15.3	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN6_4			Mux input channel 6 of TIM module 2
	CAN01_RXDA			CAN receive input node 1
	ASCLIN0_ARXB			Receive input
	QSPI2_SCLKA			Slave SPI clock inputs
	P15.3	O0		General-purpose output
	GTM_TOUT74	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	MSC0_EN1	O5		Chip Select
	—	O6		Reserved
	—	O7		Reserved
B11	P15.4	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN7_4			Mux input channel 7 of TIM module 2
	I2C0_SCLC			Serial Clock Input 2
	QSPI2_MRSTA			Master SPI data input
	SCU_E_REQ0_0			ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P15.4	O0		General-purpose output
	GTM_TOUT75	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI2_MRST	O3		Slave SPI data output
	IOM_MON2_2			Monitor input 2
	IOM_REF2_2			Reference input 2
	—	O4		Reserved
	—	O5		Reserved
	I2C0_SCL	O6		Serial Clock Output
	CCU60_CC62	O7		T12 PWM channel 62
	IOM_MON1_0			Monitor input 1
	IOM_REF1_4			Reference input 1

表 2-24 端口 P15 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
D10	P15.5	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN0_4			Mux input channel 0 of TIM module 2
	ASCLIN1_ARXB			Receive input
	I2C0_SDAC			Serial Data Input 2
	QSPI2_MTSRA			Slave SPI data input
	SCU_E_REQ4_3			ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P15.5	O0		General-purpose output
	GTM_TOUT76	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI2_MTSR	O3		Master SPI data output
	—	O4		Reserved
	MSC0_EN0	O5		Chip Select
	I2C0_SDA	O6		Serial Data Output
	CCU60_CC61	O7		T12 PWM channel 61
	IOM_MON1_1			Monitor input 1
	IOM_REF1_5			Reference input 1
A11	P15.6	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN2_14			Mux input channel 2 of TIM module 2
	GTM_TIM1_IN0_6			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_6			Mux input channel 0 of TIM module 0
	QSPI2_MTSRB			Slave SPI data input
	P15.6	O0		General-purpose output
	GTM_TOUT77	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	QSPI2_MTSR	O3		Master SPI data output
	—	O4		Reserved
	QSPI2_SCLK	O5		Master SPI clock output
	ASCLIN3_ASCLK	O6		Shift clock output
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
	IOM_REF1_6			Reference input 1

表 2-24 端口 P15 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
D8	P15.7	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_5			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_5			Mux input channel 1 of TIM module 0
	ASCLIN3_ARXA			Receive input
	QSPI2_MRSTB			Master SPI data input
	P15.7	O0		General-purpose output
	GTM_TOUT78	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	QSPI2_MRST	O3		Slave SPI data output
	IOM_MON2_2			Monitor input 2
	IOM_REF2_2			Reference input 2
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT60	O7		T12 PWM channel 60
	IOM_MON1_3			Monitor input 1
	IOM_REF1_3			Reference input 1
D7	P15.8	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_5			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_5			Mux input channel 2 of TIM module 0
	QSPI2_SCLKB			Slave SPI clock inputs
	SCU_E_REQ5_0			ERU Channel 5 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P15.8	O0		General-purpose output
	GTM_TOUT79	O1		GTM muxed output
	—	O2		Reserved
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	ASCLIN3_ASCLK	O6		Shift clock output
	CCU60_COUT61	O7		T12 PWM channel 61
	IOM_MON1_4			Monitor input 1
	IOM_REF1_2			Reference input 1

表 2-25 端口 P20 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
H13	P20.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_7			**Mux input channel 6 of TIM module 1**
	GTM_TIM1_IN4_9			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN6_7			**Mux input channel 6 of TIM module 0**
	CAN03_RXDC			**CAN receive input node 3**
	CCU_PAD_SYSCLK			**Sysclk input**
	CBS_TGI0			**Trigger input**
	SCU_E_REQ6_0			**ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GPT120_T6EUDA			**Count direction control input of core timer T6**
	P20.0	O0		**General-purpose output**
	GTM_TOUT59	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	ASCLIN3_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	HSCT0_SYSCLK_OUT	O5		**sys clock output**
	—	O6		**Reserved**
	—	O7		**Reserved**
	CBS_TGO0	O		**Trigger output**
G13	P20.2	I	S / PU / VEXT	**General-purpose input** This pin is latched at power on reset release to enter test mode.
	$\overline{\text{TESTMODE}}$			**Testmode Enable Input**

表 2-25 端口 P20 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
G12	P20.3	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN4_5			Mux input channel 4 of TIM module 2
	ASCLIN3_ARXC			Receive input
	GPT120_T6INA			Trigger/gate input of core timer T6
	P20.3	O0		General-purpose output
	GTM_TOUT61	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	QSPI0_SLSO9	O3		Master slave select output
	QSPI2_SLSO9	O4		Master slave select output
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	—	O6		Reserved
	—	O7		Reserved
F11	P20.6	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN6_5			Mux input channel 6 of TIM module 2
	CAN12_RXDA			CAN receive input node 2
	ASCLIN9_ARXE			Receive input
	P20.6	O0		General-purpose output
	GTM_TOUT62	O1		GTM muxed output
	ASCLIN1_ARTS	O2		Ready to send output
	QSPI0_SLSO8	O3		Master slave select output
	QSPI2_SLSO8	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-25 端口 P20 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
E12	P20.7	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN7_5			Mux input channel 7 of TIM module 2
	GTM_TIM1_IN5_8			Mux input channel 5 of TIM module 1
	CAN00_RXDB			CAN receive input node 0
	ASCLIN1_ACTSA			Clear to send input
	ASCLIN9_ARXF			Receive input
	P20.7	O0		General-purpose output
	GTM_TOUT63	O1		GTM muxed output
	ASCLIN9_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	CAN12_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	CCU61_COUT63	O7		T13 PWM channel 63
	IOM_MON1_7			Monitor input 1
	IOM_REF1_7			Reference input 1
F12	P20.8	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN7_3			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_3			Mux input channel 7 of TIM module 0
	P20.8	O0		General-purpose output
	GTM_TOUT64	O1		GTM muxed output
	ASCLIN1_ASLSO	O2		Slave select signal output
	QSPI0_SLSO0	O3		Master slave select output
	QSPI1_SLSO0	O4		Master slave select output
	CAN00_TXD	O5		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	—	O6		Reserved
	CCU61_CC60	O7		T12 PWM channel 60
	IOM_MON1_8			Monitor input 1
	IOM_REF1_13			Reference input 1

表 2-25 端口 P20 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
D12	P20.9	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN5_5			Mux input channel 5 of TIM module 2
	CAN03_RXDE			CAN receive input node 3
	ASCLIN1_ARXC			Receive input
	QSPI0_SLSIB			Slave select input
	SCU_E_REQ7_0			ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P20.9	O0		General-purpose output
	GTM_TOUT65	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO1	O3		Master slave select output
	QSPI1_SLSO1	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	CCU61_CC61	O7		T12 PWM channel 61
	IOM_MON1_9			Monitor input 1
	IOM_REF1_12			Reference input 1
C14	P20.10	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN6_6			Mux input channel 6 of TIM module 2
	P20.10	O0		General-purpose output
	GTM_TOUT66	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI0_SLSO6	O3		Master slave select output
	QSPI2_SLSO7	O4		Master slave select output
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	ASCLIN1_ASCLK	O6		Shift clock output
	CCU61_CC62	O7		T12 PWM channel 62
	IOM_MON1_10			Monitor input 1
	IOM_REF1_11			Reference input 1

表 2-25 端口 P20 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
D14	P20.11	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN7_6			Mux input channel 7 of TIM module 2
	QSPI0_SCLKA			Slave SPI clock inputs
	P20.11	O0		General-purpose output
	GTM_TOUT67	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU61_COUT60	O7		T12 PWM channel 60
	IOM_MON1_11			Monitor input 1
	IOM_REF1_10			Reference input 1
D13	P20.12	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN0_5			Mux input channel 0 of TIM module 2
	QSPI0_MRSTA			Master SPI data input
	IOM_PIN_13			GPIO pad input to FPC
	P20.12	O0		General-purpose output
	GTM_TOUT68	O1		GTM muxed output
	IOM_MON0_13			Monitor input 0
	—	O2		Reserved
	QSPI0_MRST	O3		Slave SPI data output
	IOM_MON2_0			Monitor input 2
	IOM_REF2_0			Reference input 2
	QSPI0_MTSR	O4		Master SPI data output
	—	O5		Reserved
	—	O6		Reserved
	CCU61_COUT61	O7		T12 PWM channel 61
	IOM_MON1_12			Monitor input 1
	IOM_REF1_9			Reference input 1

表 2-25 端口 P20 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
C13	P20.13	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN1_4			Mux input channel 1 of TIM module 2
	QSPI0_SLSIA			Slave select input
	IOM_PIN_14			GPIO pad input to FPC
	P20.13	O0		General-purpose output
	GTM_TOUT69	O1		GTM muxed output
	IOM_MON0_14			Monitor input 0
	—	O2		Reserved
	QSPI0_SLSO2	O3		Master slave select output
	QSPI1_SLSO2	O4		Master slave select output
	QSPI0_SCLK	O5		Master SPI clock output
	—	O6		Reserved
	CCU61_COUT62	O7		T12 PWM channel 62
	IOM_MON1_13			Monitor input 1
	IOM_REF1_8			Reference input 1
B14	P20.14	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN2_4			Mux input channel 2 of TIM module 2
	QSPI0_MTSRA			Slave SPI data input
	IOM_PIN_15			GPIO pad input to FPC
	DMU_FDEST			Enter destructive debug mode
	P20.14	O0		General-purpose output
	GTM_TOUT70	O1		GTM muxed output
	IOM_MON0_15			Monitor input 0
	—	O2		Reserved
	QSPI0_MTSR	O3		Master SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-26 端口 P21 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
H12	P21.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN4_6			Mux input channel 4 of TIM module 2
	ASCLIN11_ARXC			Receive input
	P21.0	O0		General-purpose output
	GTM_TOUT51	O1		GTM muxed output
	ASCLIN11_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	HSM_HSM1	O		Pin Output Value
K13	P21.2	I	LVDS_RX / FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_7			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_7			Mux input channel 0 of TIM module 0
	QSPI2_MRSTCN			Master SPI data input (LVDS N line)
	SCU_EMGSTOP_PORT_B			Emergency stop Port Pin B input request
	ASCLIN3_ARXGN			Differential Receive input (low active)
	HSCT0_RXDN			Rx data
	ASCLIN11_ARXE			Receive input
	GTM_DTMA1_0			CDTM1_DTM4
	P21.2	O0		General-purpose output
	GTM_TOUT53	O1		GTM muxed output
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	GETH_MDC	O5		MDIO clock
	—	O6		Reserved
	—	O7		Reserved

表 2-26 端口 P21 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
J14	P21.3	I	LVDS_R X / FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_6			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_6			Mux input channel 1 of TIM module 0
	QSPI2_MRSTCP			Master SPI data input (LVDS P line)
	ASCLIN3_ARXGP			Differential Receive input (high active)
	GETH_MDIOD			MDIO Input
	HSCT0_RXDP			Rx data
	P21.3	O0		General-purpose output
	GTM_TOUT54	O1		GTM muxed output
	ASCLIN11_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	GETH_MDIO	O		MDIO Output
J13	P21.4	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN2_6			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_6			Mux input channel 2 of TIM module 0
	P21.4	O0		General-purpose output
	GTM_TOUT55	O1		GTM muxed output
	ASCLIN11_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	HSCT0_TXDN	O		Tx data

表 2-26 端口 P21 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
H14	P21.5	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM1_IN3_6			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_6			**Mux input channel 3 of TIM module 0**
	ASCLIN11_ARXF			**Receive input**
	P21.5	O0		**General-purpose output**
	GTM_TOUT56	O1		**GTM muxed output**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN11_ATX	O3		**Transmit output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSCT0_TXDP	O		**Tx data**
F13	P21.6/TDI	I	FAST / PD / PU2 / VEXT / ES3	**General-purpose input** PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ.
	GTM_TIM1_IN4_8			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_8			**Mux input channel 4 of TIM module 0**
	GPT120_T5EUDA			**Count direction control input of timer T5**
	ASCLIN3_ARXF			**Receive input**
	CBS_TGI2			**Trigger input**
	TDI			**JTAG Module Data Input**
	P21.6	O0		**General-purpose output**
	GTM_TOUT57	O1		**GTM muxed output**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	GPT120_T3OUT	O7		**External output for overflow/underflow detection of core timer T3**
	CBS_TGO2	O		**Trigger output**
	DAP3	I/O		**DAP: DAP3 Data I/O**

表 2-26 端口 P21 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
F14	P21.7/TDO	I	FAST / PU2 / VEXT / ES4	**General-purpose input**
	GTM_TIM1_IN5_7			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_7			**Mux input channel 5 of TIM module 0**
	GPT120_T5INA			**Trigger/gate input of timer T5**
	CBS_TGI3			**Trigger input**
	GETH_RXERB			**Receive Error MII**
	P21.7	O0		**General-purpose output**
	GTM_TOUT58	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	ASCLIN3_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	GPT120_T6OUT	O7		**External output for overflow/underflow detection of core timer T6**
	CBS_TGO3	O		**Trigger output**
	DAP2	I/O		**DAP: DAP2 Data I/O**
	TDO	O		**JTAG Module Data Output**

表 2-27 端口 P22 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
J11	P22.0	I	FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN1_7			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_7			Mux input channel 1 of TIM module 0
	ASCLIN6_ARXE			Receive input
	QSPI3_MTSRD			Slave SPI data input
	P22.0	O0		General-purpose output
	GTM_TOUT47	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	QSPI3_MTSR	O3		Master SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	ASCLIN6_ATX	O7		Transmit output
L12	P22.1	I	FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN0_8			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_8			Mux input channel 0 of TIM module 0
	ASCLIN7_ARXE			Receive input
	QSPI3_MRSTD			Master SPI data input
	P22.1	O0		General-purpose output
	GTM_TOUT48	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	QSPI3_MRST	O3		Slave SPI data output
	IOM_MON2_3			Monitor input 2
	IOM_REF2_3			Reference input 2
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	ASCLIN7_ATX	O7		Transmit output

表 2-27 端口 P22 功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
H11	P22.2	I	FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN3_7			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_7			Mux input channel 3 of TIM module 0
	P22.2	O0		General-purpose output
	GTM_TOUT49	O1		GTM muxed output
	ASCLIN5_ATX	O2		Transmit output
	QSPI3_SLSO12	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
J12	P22.3	I	FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN4_4			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_4			Mux input channel 4 of TIM module 0
	ASCLIN5_ARXC			Receive input
	QSPI3_SCLKD			Slave SPI clock inputs
	P22.3	O0		General-purpose output
	GTM_TOUT50	O1		GTM muxed output
	—	O2		Reserved
	QSPI3_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-28 端口 P23 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
N14	P23.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_4			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_4			**Mux input channel 6 of TIM module 0**
	ASCLIN6_ARXF			**Receive input**
	P23.1	O0		**General-purpose output**
	GTM_TOUT42	O1		**GTM muxed output**
	ASCLIN1_ARTS	O2		**Ready to send output**
	—	O3		**Reserved**
	GTM_CLK0	O4		**CGM generated clock**
	CAN10_TXD	O5		**CAN transmit output node 0**
	CCU_EXTCLK0	O6		**External Clock 0**
	ASCLIN6_ASCLK	O7		**Shift clock output**
K11	P23.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN7_4			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_4			**Mux input channel 7 of TIM module 0**
	ASCLIN6_ARXA			**Receive input**
	CAN12_RXDC			**CAN receive input node 2**
	P23.3	O0		**General-purpose output**
	GTM_TOUT44	O1		**GTM muxed output**
	ASCLIN7_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

表 2-29 端口 P32 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
P12	P32.0	I	SLOW / PU1 / VEXT / ES	**General-purpose input** P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
	GTM_TIM2_IN2_5			**Mux input channel 2 of TIM module 2**
	P32.0	O0		**General-purpose output**
	GTM_TOUT36	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
N12	P32.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input** P32.1 / External Pass Device gate control for EVRC
	P32.1	O0		**General-purpose output**
	GTM_TOUT37	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
P13	P32.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN5_5			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_5			**Mux input channel 5 of TIM module 0**
	ASCLIN1_ACTSB			**Clear to send input**
	P32.4	O0		**General-purpose output**
	GTM_TOUT40	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	GTM_CLK1	O4		**CGM generated clock**
	—	O5		**Reserved**
	CCU_EXTCLK1	O6		**External Clock 1**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
	PMS_DCDCSYNCO	O		**DC-DC synchronization output**

表 2-30 端口 P33 功能

Ball	Symbol	Ctrl.	Buffer Type	Function
M9	P33.0	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN4_6			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_6			Mux input channel 4 of TIM module 0
	EDSADC_ITR0E			Trigger/Gate input, channel 0
	IOM_PIN_0			GPIO pad input to FPC
	GTM_DTMT1_2			CDTM1_DTM0
	P33.0	O0		General-purpose output
	GTM_TOUT22	O1		GTM muxed output
	IOM_MON0_0			Monitor input 0
	IOM_GTM_0			GTM-provided inputs to EXOR combiner
	ASCLIN5_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
M8	P33.1	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN5_6			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_6			Mux input channel 5 of TIM module 0
	EDSADC_ITR1E			Trigger/Gate input, channel 1
	PSI5_RX0C			RXD inputs (receive data) channel 0
	EDSADC_DSCIN2B			Modulator clock input, channel 2
	SENT_SENT9C			Receive input channel 9
	ASCLIN8_ARXC			Receive input
	IOM_PIN_1			GPIO pad input to FPC
	P33.1	O0		General-purpose output
	GTM_TOUT23	O1		GTM muxed output
	IOM_MON0_1			Monitor input 0
	IOM_GTM_1			GTM-provided inputs to EXOR combiner
	ASCLIN3_ASLSO	O2		Slave select signal output
	QSPI2_SCLK	O3		Master SPI clock output
	EDSADC_DSCOUT2	O4		Modulator clock output
	EVADC_EMUX02	O5		Control of external analog multiplexer interface 0
	—	O6		Reserved
	—	O7		Reserved

表 2-30 端口 P33 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
P8	P33.2	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN6_6			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_6			Mux input channel 6 of TIM module 0
	EDSADC_ITR2E			Trigger/Gate input, channel 2
	SENT_SENT8C			Receive input channel 8
	EDSADC_DSDIN2B			Digital datastream input, channel 2
	IOM_PIN_2			GPIO pad input to FPC
	P33.2	O0		General-purpose output
	GTM_TOUT24	O1		GTM muxed output
	IOM_MON0_2			Monitor input 0
	IOM_GTM_2			GTM-provided inputs to EXOR combiner
	ASCLIN3_ASCLK	O2		Shift clock output
	QSPI2_SLSO10	O3		Master slave select output
	PSI5_TX0	O4		TXD outputs (send data)
	IOM_MON1_14			Monitor input 1
	IOM_REF1_14			Reference input 1
	EVADC_EMUX01	O5		Control of external analog multiplexer interface 0
	—	O6		Reserved
	—	O7		Reserved
N8	P33.3	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN7_6			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_6			Mux input channel 7 of TIM module 0
	PSI5_RX1C			RXD inputs (receive data) channel 1
	SENT_SENT7C			Receive input channel 7
	EDSADC_DSCIN1B			Modulator clock input, channel 1
	IOM_PIN_3			GPIO pad input to FPC
	P33.3	O0		General-purpose output
	GTM_TOUT25	O1		GTM muxed output
	IOM_MON0_3			Monitor input 0
	IOM_GTM_3			GTM-provided inputs to EXOR combiner
	ASCLIN5_ASCLK	O2		Shift clock output
	—	O3		Reserved
	EDSADC_DSCOUT1	O4		Modulator clock output
	EVADC_EMUX00	O5		Control of external analog multiplexer interface 0
	—	O6		Reserved
	—	O7		Reserved

表 2-30 端口 P33 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
L8	P33.4	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN0_10			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_10			Mux input channel 0 of TIM module 0
	EDSADC_ITR0F			Trigger/Gate input, channel 0
	SENT_SENT6C			Receive input channel 6
	EDSADC_DSDIN1B			Digital datastream input, channel 1
	CCU61_CTRAPC			Trap input capture
	ASCLIN5_ARXB			Receive input
	IOM_PIN_4			GPIO pad input to FPC
	P33.4	O0		General-purpose output
	GTM_TOUT26	O1		GTM muxed output
	IOM_MON0_4			Monitor input 0
	IOM_GTM_4			GTM-provided inputs to EXOR combiner
	ASCLIN2_ARTS	O2		Ready to send output
	QSPI2_SLSO12	O3		Master slave select output
	PSI5_TX1	O4		TXD outputs (send data)
	IOM_MON1_15			Monitor input 1
	EVADC_EMUX12	O5		Control of external analog multiplexer interface 1
	EVADC_FC0BFLOUT	O6		Boundary flag output, FC channel 0
	CAN13_TXD	O7		CAN transmit output node 3

表 2-30 端口 P33 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
N9	P33.5	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN1_8			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_8			Mux input channel 1 of TIM module 0
	EDSADC_DSCIN0B			Modulator clock input, channel 0
	EDSADC_ITR1F			Trigger/Gate input, channel 1
	GPT120_T4EUDB			Count direction control input of timer T4
	PSI5S_RXC			RX data input
	ASCLIN2_ACTSB			Clear to send input
	CCU61_CCPOS2C			Hall capture input 2
	SENT_SENT5C			Receive input channel 5
	CAN13_RXDB			CAN receive input node 3
	IOM_PIN_5			GPIO pad input to FPC
	P33.5	O0		General-purpose output
	GTM_TOUT27	O1		GTM muxed output
	IOM_MON0_5			Monitor input 0
	IOM_GTM_5			GTM-provided inputs to EXOR combiner
	QSPI0_SLSO7	O2		Master slave select output
	QSPI1_SLSO7	O3		Master slave select output
	EDSADC_DSCOUT0	O4		Modulator clock output
	EVADC_EMUX11	O5		Control of external analog multiplexer interface 1
	—	O6		Reserved
	ASCLIN5_ASLSO	O7		Slave select signal output

表 2-30 端口 P33 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
P9	P33.6	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN2_9			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_9			Mux input channel 2 of TIM module 0
	EDSADC_ITR2F			Trigger/Gate input, channel 2
	GPT120_T2EUDB			Count direction control input of timer T2
	SENT_SENT4C			Receive input channel 4
	CCU61_CCPOS1C			Hall capture input 1
	EDSADC_DSDIN0B			Digital datastream input, channel 0
	ASCLIN8_ARXD			Receive input
	IOM_PIN_6			GPIO pad input to FPC
	P33.6	O0		General-purpose output
	GTM_TOUT28	O1		GTM muxed output
	IOM_MON0_6			Monitor input 0
	IOM_GTM_6			GTM-provided inputs to EXOR combiner
	ASCLIN2_ASLSO	O2		Slave select signal output
	QSPI2_SLSO11	O3		Master slave select output
	—	O4		Reserved
	EVADC_EMUX10	O5		Control of external analog multiplexer interface 1
	EVADC_FC1BFLOUT	O6		Boundary flag output, FC channel 1
	PSI5S_TX	O7		TX data output

表 2-30 端口 P33 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
L10	P33.7	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN3_9			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_9			Mux input channel 3 of TIM module 0
	CAN00_RXDE			CAN receive input node 0
	GPT120_T2INB			Trigger/gate input of timer T2
	CCU61_CCPOS0C			Hall capture input 0
	SCU_E_REQ4_0			ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	IOM_PIN_7			GPIO pad input to FPC
	P33.7	O0		General-purpose output
	GTM_TOUT29	O1		GTM muxed output
	IOM_MON0_7			Monitor input 0
	IOM_GTM_7			GTM-provided inputs to EXOR combiner
	ASCLIN2_ASCLK	O2		Shift clock output
	—	O3		Reserved
	ASCLIN8_ATX	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-30 端口 P33 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
L9	P33.8	I	FAST / HighZ / VEVRSB	General-purpose input
	GTM_TIM1_IN4_7			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_7			Mux input channel 4 of TIM module 0
	ASCLIN2_ARXE			Receive input
	SCU_EMGSTOP_PORT_A			Emergency stop Port Pin A input request
	IOM_PIN_8			GPIO pad input to FPC
	P33.8	O0		General-purpose output
	GTM_TOUT30	O1		GTM muxed output
	IOM_MON0_8			Monitor input 0
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	—	O3		Reserved
	—	O4		Reserved
	CAN00_TXD	O5		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	—	O6		Reserved
	CCU61_COUT62	O7		T12 PWM channel 62
	IOM_MON1_13			Monitor input 1
	IOM_REF1_8			Reference input 1
	SMU_FSP0	O		FSP[1..0] Output Signals - Generated by SMU_core

表 2-30 端口 P33 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
P10	P33.9	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN1_9			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_9			Mux input channel 1 of TIM module 0
	IOM_PIN_9			GPIO pad input to FPC
	P33.9	O0		General-purpose output
	GTM_TOUT31	O1		GTM muxed output
	IOM_MON0_9			Monitor input 0
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	—	O3		Reserved
	ASCLIN2_ASCLK	O4		Shift clock output
	CAN01_TXD	O5		CAN transmit output node 1
	IOM_MON2_6			Monitor input 2
	IOM_REF2_6			Reference input 2
	ASCLIN0_ATX	O6		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	CCU61_CC62	O7		T12 PWM channel 62
	IOM_MON1_10			Monitor input 1
	IOM_REF1_11			Reference input 1

表 2-30 端口 P33 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
N11	P33.10	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN0_9			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_9			Mux input channel 0 of TIM module 0
	CAN01_RXDD			CAN receive input node 1
	ASCLIN0_ARXD			Receive input
	IOM_PIN_10			GPIO pad input to FPC
	P33.10	O0		General-purpose output
	GTM_TOUT32	O1		GTM muxed output
	IOM_MON0_10			Monitor input 0
	QSPI1_SLSO6	O2		Master slave select output
	—	O3		Reserved
	ASCLIN1_ASLSO	O4		Slave select signal output
	PSI5S_CLK	O5		PSI5S CLK is a clock that can be used on a pin to drive the external PHY.
	—	O6		Reserved
	CCU61_COUT61	O7		T12 PWM channel 61
	IOM_MON1_12			Monitor input 1
	IOM_REF1_9			Reference input 1
	SMU_FSP1	O		FSP[1..0] Output Signals - Generated by SMU_core
N10	P33.11	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN2_8			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_8			Mux input channel 2 of TIM module 0
	IOM_PIN_11			GPIO pad input to FPC
	P33.11	O0		General-purpose output
	GTM_TOUT33	O1		GTM muxed output
	IOM_MON0_11			Monitor input 0
	ASCLIN1_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	EDSADC_CGPWMN	O6		Negative carrier generator output
	CCU61_CC61	O7		T12 PWM channel 61
	IOM_MON1_9			Monitor input 1
	IOM_REF1_12			Reference input 1

表 2-30 端口 P33 的功能（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
M10	P33.12	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM2_IN0_6			Mux input channel 0 of TIM module 2
	CAN00_RXDD			CAN receive input node 0
	PMS_PINBWKP			PINB (P33.12) pin input
	IOM_PIN_12			GPIO pad input to FPC
	P33.12	O0		General-purpose output
	GTM_TOUT34	O1		GTM muxed output
	IOM_MON0_12			Monitor input 0
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	—	O3		Reserved
	ASCLIN1_ASCLK	O4		Shift clock output
	—	O5		Reserved
	EDSADC_CGPWMP	O6		Positive carrier generator output
	CCU61_COUT60	O7		T12 PWM channel 60
	IOM_MON1_11			Monitor input 1
	IOM_REF1_10			Reference input 1
M11	P33.13	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM2_IN1_5			Mux input channel 1 of TIM module 2
	ASCLIN1_ARXF			Receive input
	EDSADC_SGNB			Carrier sign signal input
	P33.13	O0		General-purpose output
	GTM_TOUT35	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	—	O3		Reserved
	QSPI2_SLSO6	O4		Master slave select output
	CAN00_TXD	O5		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	—	O6		Reserved
	CCU61_CC60	O7		T12 PWM channel 60
	IOM_MON1_8			Monitor input 1
	IOM_REF1_13			Reference input 1

表 2-31 模拟输入

Ball	Symbol	Ctrl.	Buffer Type	Function
L7	AN0	I	D / HighZ / VDDM	**Analog Input 0**
	EVADC_G0CH0			**Analog input channel 0, group 0**
	EDSADC_EDS3PA			**Positive analog input channel 3, pin A**
P6	AN1	I	D / HighZ / VDDM	**Analog Input 1**
	EVADC_G0CH1			**Analog input channel 1, group 0**
	EDSADC_EDS3NA			**Negative analog input channel 3, pin A**
L6	AN2	I	D / HighZ / VDDM	**Analog Input 2**
	EVADC_G0CH2			**Analog input channel 2, group 0**
	EDSADC_EDS0PA			**Positive analog input channel 0, pin A**
M6	AN3	I	D / HighZ / VDDM	**Analog Input 3**
	EVADC_G0CH3			**Analog input channel 3, group 0**
	EDSADC_EDS0NA			**Negative analog input channel 0, pin A**
N6	AN4	I	D / HighZ / VDDM	**Analog Input 4**
	EVADC_G0CH4			**Analog input channel 4, group 0**
L5	AN5	I	D / HighZ / VDDM	**Analog Input 5**
	EVADC_G0CH5			**Analog input channel 5, group 0**
M5	AN6	I	D / HighZ / VDDM	**Analog Input 6**
	EVADC_G0CH6			**Analog input channel 6, group 0**
P5	AN7	I	D / HighZ / VDDM	**Analog Input 7**
	EVADC_G0CH7			**Analog input channel 7, group 0**
N5	AN8	I	D / HighZ / VDDM	**Analog Input 8**
	EVADC_G1CH0			**Analog input channel 0, group 1**
N3	AN9	I	D / HighZ / VDDM	**Analog Input 9**
	EVADC_G1CH1			**Analog input channel 1, group 1**
M4	AN10	I	D / HighZ / VDDM	**Analog Input 10**
	EVADC_G1CH2			**Analog input channel 2, group 1**
N4	AN11	I	D / HighZ / VDDM	**Analog Input 11**
	EVADC_G1CH3			**Analog input channel 3, group 1**
M3	AN12	I	D / HighZ / VDDM	**Analog Input 12**
	EVADC_G1CH4			**Analog input channel 4, group 1**
	EDSADC_EDS0PB			**Positive analog input channel 0, pin B**
N2	AN13	I	D / HighZ / VDDM	**Analog Input 13**
	EVADC_G1CH5			**Analog input channel 5, group 1**
	EDSADC_EDS0NB			**Negative analog input channel 0, pin B**
L4	AN14	I	D / HighZ / VDDM	**Analog Input 14**
	EVADC_G1CH6			**Analog input channel 6, group 1**
	EDSADC_EDS3PB			**Positive analog input channel 3, pin B**

表 2-31 模拟输入（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
N1	AN15	I	D / HighZ / VDDM	**Analog Input 15**
	EVADC_G1CH7			**Analog input channel 7, group 1**
	EDSADC_EDS3NB			**Negative analog input channel 3, pin N**
M1	AN16	I	D / HighZ / VDDM	**Analog Input 16**
	EVADC_G2CH0			**Analog input channel 0, group 2**
	EVADC_FC0CH0			**Analog input FC channel 0**
M2	AN17	I	D / HighZ / VDDM	**Analog Input 17**
	EVADC_G2CH1			**Analog input channel 1, group 2**
	EVADC_FC1CH0			**Analog input FC channel 1**
L1	AN24/P40.0	I	S / HighZ / VDDM	**Analog Input 24**
	SENT_SENT0A			**Receive input channel 0**
	EVADC_G3CH0			**Analog input channel 0, group 3**
	CCU60_CCPOS0D			**Hall capture input 0**
	EDSADC_EDS2PB			**Positive analog input channel 2, pin B**
L2	AN25/P40.1	I	S / HighZ / VDDM	**Analog Input 25**
	SENT_SENT1A			**Receive input channel 1**
	EVADC_G3CH1			**Analog input channel 1, group 3**
	CCU60_CCPOS1B			**Hall capture input 1**
	EDSADC_EDS2NB			**Negative analog input channel 2, pin B**
K1	AN32/P40.4	I	S / HighZ / VDDM	**Analog Input 32**
	SENT_SENT4A			**Receive input channel 4**
	EVADC_G8CH0			**Analog input channel 0, group 8**
	CCU60_CCPOS2D			**Hall capture input 2**
K2	AN33/P40.5	I	S / HighZ / VDDM	**Analog Input 33**
	SENT_SENT5A			**Receive input channel 5**
	EVADC_G8CH1			**Analog input channel 1, group 8**
	CCU61_CCPOS0D			**Hall capture input 0**
K3	AN34	I	D / HighZ / VDDM	**Analog Input 34**
	EVADC_G8CH2			**Analog input channel 2, group 8**
K4	AN35	I	D / HighZ / VDDM	**Analog Input 35**
	EVADC_G8CH3			**Analog input channel 3, group 8**
J1	AN36/P40.6	I	S / HighZ / VDDM	**Analog Input 36**
	SENT_SENT6A			**Receive input channel 6**
	EVADC_G8CH4			**Analog input channel 4, group 8**
	CCU61_CCPOS1B			**Hall capture input 1**
	EDSADC_EDS1PA			**Positive analog input channel 1, pin A**

表 2-31 模拟输入（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
J2	AN37/P40.7	I	S / HighZ / VDDM	**Analog Input 37**
	SENT_SENT7A			**Receive input channel 7**
	EVADC_G8CH5			**Analog input channel 5, group 8**
	CCU61_CCPOS1D			**Hall capture input 1**
	EDSADC_EDS1NA			**Negative analog input channel 1, pin A**
J3	AN38/P40.8	I	S / HighZ / VDDM	**Analog Input 38**
	SENT_SENT8A			**Receive input channel 8**
	EVADC_G8CH6			**Analog input channel 6, group 8**
	CCU61_CCPOS2B			**Hall capture input 2**
	EDSADC_EDS1PB			**Positive analog input channel 1, pin B**
J4	AN39/P40.9	I	S / HighZ / VDDM	**Analog Input 39**
	SENT_SENT9A			**Receive input channel 9**
	EVADC_G8CH7			**Analog input channel 7, group 8**
	CCU61_CCPOS2D			**Hall capture input 2**
	EDSADC_EDS1NB			**Negative analog input channel 1, pin B**

注释：端口引脚P32.0 和P32.1 是双向引脚，具有以下两个功能：

3. *如果将这些引脚用作标准GPIO，则可以使用P32.0 和P32.1 引脚配置表中定义的功能。*
4. *如果引脚用作外部MOSFET 的预驱动器（内部DCDC 情况），P32.0 和P32.1 将充当名为VGATE1N 和VGATE1P 的模拟IO。*

表 2-32 系统 I/O

Ball	Symbol	Ctrl.	Buffer Type	Function
P12	VGATE1N	O	—	**DCDC N ch. MOSFET gate driver output** P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
N12	VGATE1P	O	—	**DCDC P ch. MOSFET gate driver output** P32.1 / External Pass Device gate control for EVRC
L14	XTAL1	I	XTAL / VEXT	**XTAL pad1** XTAL1. Main Oscillator/PLL/Clock Generator Input.
L13	XTAL2	O	XTAL / VEXT	**XTAL pad2** XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT
G11	TMS	I	FAST / PD2 / VEXT	**JTAG Module State Machine Control Input**
	DAP1	I/O		**DAP: DAP1 Data I/O**

TC36x 引脚定义和功能：LFBGA-180 封装变体引脚

表 2-32 系统 I/O（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
K12	TRST	I	FAST / PU2 / VEXT	**JTAG Module Reset/Enable Input**
G14	TCK	I	FAST / PD2 / VEXT	**JTAG Module Clock Input**
	DAP0	I		**DAP: DAP0 Clock Input**
E11	ESR1	I/O	FAST / PU1 / VEXT	**ESR1 Port Pin input - can be used to trigger a reset or an NMI** ESR1: External System Request Reset 1. Default NMI function. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
	PMS_ESR1WKP	I		**ESR1 pin input**
E13	PORST	I/O	PORST / PD / VEXT	**PORST pin** Power On Reset Input. Additional strong PD in case of power fail.
E14	ESR0	I/O	FAST / OD / VEXT	**ESR0 Port Pin input - can be used to trigger a reset or an NMI** ESR0: External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
	PMS_ESR0WKP	I		**ESR0 pin input**

表 2-33 电源

Ball	Symbol	Ctrl.	Buffer Type	Function
P3	VDDM	I	—	**ADC Analog Power Supply (5V / 3.3V)**
D5	VFLEX	I	—	**Digital Power Supply for Flex Port Pads (5V / 3.3V)**
F9, G9, H6, J7, J8	VDD	I	—	**Digital Core Power Supply (1.25V)**
F6, F8, G6, J9, P11	VEXT	I	—	**External Power Supply (5V / 3.3V)**
F7	VDDP3	I	—	**Flash Power Supply (3.3V)**
B2, C3, D4, E5, K10, L11, M12, N13	VSS	I	—	**Digital Ground**

表 2-33 电源（续）

Ball	Symbol	Ctrl.	Buffer Type	Function
B13, C12, D11, E10, G7, G8, H7, H8, J6, K5	VSS	I	—	**Digital Ground**
K14	VSS	I	—	**Oscillator Ground**
P4	VAREF1	I	—	**Positive Analog Reference Voltage 1**
A1, A14, L3, M7, N7, P1, P7, P14	NC	I	—	**Not connected. These pins are reserved for future extensions and shall not be connected externally**
H9	VEVRSB	I	—	**Standby Power Supply (5V / 3.3V) for the Standby SRAM**
M13	VDD	I	—	**Digital Power Supply for Oscillator (1.25V)**
M14	VEXT	I	—	**Digital Power Supply for Oscillator (shall be supplied with same level as used for VEXT)**
P2	VSSM/VAGND1	I	—	**Analog Ground for VDDM / Negative Analog Reference Voltage 1**

2.3 TC36x LQFP-176 封装变体引脚配置

注意：在以下QFP封装中，VFLEX 电源内部连接到VEXT 电源，因此不会在相应的封装图中或电源表中显示为专用引脚。

表 2-34 端口 P00 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
11	P00.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN0_1			**Mux input channel 0 of TIM module 2**
	CCU61_CTRAPA			**Trap input capture**
	CCU60_T12HRE			**External timer start 12**
	MSC0_INJ0			**Injection signal from port**
	GETH_MDIOA			**MDIO Input**
	P00.0	O0		**General-purpose output**
	GTM_TOUT9	O1		**GTM muxed output**
	IOM_REF0_9			**Reference input 0**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN3_ATX	O3		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O4		**Reserved**
	CAN10_TXD	O5		**CAN transmit output node 0**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
	GETH_MDIO	O		**MDIO Output**

表 2-34 端口 P00 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
12	P00.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN1_1			**Mux input channel 1 of TIM module 2**
	CCU60_CC60INB			**T12 capture input 60**
	ASCLIN3_ARXE			**Receive input**
	CAN10_RXDA			**CAN receive input node 0**
	PSI5_RX0A			**RXD inputs (receive data) channel 0**
	CCU61_CC60INA			**T12 capture input 60**
	SENT_SENT0B			**Receive input channel 0**
	EVADC_G9CH11	AI		**Analog input channel 11, group 9**
	P00.1	O0		**General-purpose output**
	GTM_TOUT10	O1		**GTM muxed output**
	IOM_REF0_10			**Reference input 0**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	SENT_SPC0	O6		**Transmit output**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

表 2-34 端口 P00 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
13	P00.2	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM2_IN1_2			**Mux input channel 1 of TIM module 2**
	SENT_SENT1B			**Receive input channel 1**
	EVADC_G9CH10	AI		**Analog input channel 10, group 9**
	P00.2	O0		**General-purpose output**
	GTM_TOUT11	O1		**GTM muxed output**
	IOM_REF0_11			**Reference input 0**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	PSI5_TX0	O4		**TXD outputs (send data)**
	IOM_MON1_14			**Monitor input 1**
	IOM_REF1_14			**Reference input 1**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	QSPI3_SLSO4	O6		**Master slave select output**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**

表 2-34 端口 P00 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
14	P00.3	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM2_IN2_1			**Mux input channel 2 of TIM module 2**
	CCU60_CC61INB			**T12 capture input 61**
	EDSADC_DSCIN3A			**Modulator clock input, channel 3**
	PSI5_RX1A			**RXD inputs (receive data) channel 1**
	CAN03_RXDA			**CAN receive input node 3**
	PSI5S_RXA			**RX data input**
	SENT_SENT2B			**Receive input channel 2**
	CCU61_CC61INA			**T12 capture input 61**
	EVADC_G9CH9	AI		**Analog input channel 9, group 9**
	P00.3	O0		**General-purpose output**
	GTM_TOUT12	O1		**GTM muxed output**
	IOM_REF0_12			**Reference input 0**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	EDSADC_DSCOUT3	O4		**Modulator clock output**
	—	O5		**Reserved**
	SENT_SPC2	O6		**Transmit output**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**

表 2-34 端口 P00 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
15	P00.4	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM2_IN3_1			**Mux input channel 3 of TIM module 2**
	SCU_E_REQ2_2			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	SENT_SENT3B			**Receive input channel 3**
	EDSADC_DSDIN3A			**Digital datastream input, channel 3**
	EDSADC_SGNA			**Carrier sign signal input**
	ASCLIN10_ARXA			**Receive input**
	EVADC_G9CH8	AI		**Analog input channel 8, group 9**
	P00.4	O0		**General-purpose output**
	GTM_TOUT13	O1		**GTM muxed output**
	IOM_REF0_13			**Reference input 0**
	PSI5S_TX	O2		**TX data output**
	CAN11_TXD	O3		**CAN transmit output node 1**
	PSI5_TX1	O4		**TXD outputs (send data)**
	IOM_MON1_15			**Monitor input 1**
	—	O5		**Reserved**
	SENT_SPC3	O6		**Transmit output**
	CCU61_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_12			**Monitor input 1**
	IOM_REF1_9			**Reference input 1**

表 2-34 端口 P00 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
16	P00.5	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM2_IN4_1			Mux input channel 4 of TIM module 2
	CCU60_CC62INB			T12 capture input 62
	EDSADC_DSCIN2A			Modulator clock input, channel 2
	CCU61_CC62INA			T12 capture input 62
	SENT_SENT4B			Receive input channel 4
	CAN11_RXDB			CAN receive input node 1
	GTM_DTMT1_1			CDTM1_DTM0
	EVADC_G9CH7	AI		Analog input channel 7, group 9
	P00.5	O0		General-purpose output
	GTM_TOUT14	O1		GTM muxed output
	IOM_REF0_14			Reference input 0
	EDSADC_CGPWMN	O2		Negative carrier generator output
	QSPI3_SLSO3	O3		Master slave select output
	EDSADC_DSCOUT2	O4		Modulator clock output
	EVADC_FC0BFLOUT	O5		Boundary flag output, FC channel 0
	SENT_SPC4	O6		Transmit output
	CCU61_CC62	O7		T12 PWM channel 62
	IOM_MON1_10			Monitor input 1
	IOM_REF1_11			Reference input 1
17	P00.6	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM2_IN5_1			Mux input channel 5 of TIM module 2
	EDSADC_DSDIN2A			Digital datastream input, channel 2
	SENT_SENT5B			Receive input channel 5
	ASCLIN5_ARXA			Receive input
	EVADC_G9CH6	AI		Analog input channel 6, group 9
	P00.6	O0		General-purpose output
	GTM_TOUT15	O1		GTM muxed output
	IOM_REF0_15			Reference input 0
	EDSADC_CGPWMP	O2		Positive carrier generator output
	—	O3		Reserved
	—	O4		Reserved
	EVADC_EMUX10	O5		Control of external analog multiplexer interface 1
	SENT_SPC5	O6		Transmit output
	CCU61_COUT62	O7		T12 PWM channel 62
	IOM_MON1_13			Monitor input 1
	IOM_REF1_8			Reference input 1

表 2-34 端口 P00 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
18	P00.7	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM2_IN6_1			Mux input channel 6 of TIM module 2
	CCU61_CC60INC			T12 capture input 60
	SENT_SENT6B			Receive input channel 6
	GPT120_T2INA			Trigger/gate input of timer T2
	CCU61_CCPOS0A			Hall capture input 0
	CCU60_T12HRB			External timer start 12
	GTM_DTMT0_2			CDTM0_DTM0
	EVADC_G9CH5	AI		Analog input channel 5, group 9
	P00.7	O0		General-purpose output
	GTM_TOUT16	O1		GTM muxed output
	ASCLIN5_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	EVADC_EMUX11	O5		Control of external analog multiplexer interface 1
	SENT_SPC6	O6		Transmit output
	CCU61_CC60	O7		T12 PWM channel 60
	IOM_MON1_8			Monitor input 1
	IOM_REF1_13			Reference input 1
19	P00.8	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM2_IN7_1			Mux input channel 7 of TIM module 2
	CCU61_CC61INC			T12 capture input 61
	SENT_SENT7B			Receive input channel 7
	GPT120_T2EUDA			Count direction control input of timer T2
	CCU61_CCPOS1A			Hall capture input 1
	CCU60_T13HRB			External timer start 13
	ASCLIN10_ARXB			Receive input
	EVADC_G9CH4	AI		Analog input channel 4, group 9
	P00.8	O0		General-purpose output
	GTM_TOUT17	O1		GTM muxed output
	QSPI3_SLSO6	O2		Master slave select output
	ASCLIN10_ATX	O3		Transmit output
	—	O4		Reserved
	EVADC_EMUX12	O5		Control of external analog multiplexer interface 1
	SENT_SPC7	O6		Transmit output
	CCU61_CC61	O7		T12 PWM channel 61
	IOM_MON1_9			Monitor input 1
	IOM_REF1_12			Reference input 1

表 2-34 端口 P00 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
20	P00.9	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM1_IN0_1			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_1			Mux input channel 0 of TIM module 0
	CCU61_CC62INC			T12 capture input 62
	SENT_SENT8B			Receive input channel 8
	CCU61_CCPOS2A			Hall capture input 2
	EDSADC_DSCIN1A			Modulator clock input, channel 1
	EDSADC_ITR3F			Trigger/Gate input, channel 3
	GPT120_T4EUDA			Count direction control input of timer T4
	CCU60_T13HRC			External timer start 13
	CCU60_T12HRC			External timer start 12
	EVADC_G9CH3	AI		Analog input channel 3, group 9
	P00.9	O0		General-purpose output
	GTM_TOUT18	O1		GTM muxed output
	QSPI3_SLSO7	O2		Master slave select output
	ASCLIN3_ARTS	O3		Ready to send output
	EDSADC_DSCOUT1	O4		Modulator clock output
	ASCLIN4_ATX	O5		Transmit output
	SENT_SPC8	O6		Transmit output
	CCU61_CC62	O7		T12 PWM channel 62
	IOM_MON1_10			Monitor input 1
	IOM_REF1_11			Reference input 1
21	P00.10	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM1_IN1_1			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_1			Mux input channel 1 of TIM module 0
	SENT_SENT9B			Receive input channel 9
	EDSADC_DSDIN1A			Digital datastream input, channel 1
	EVADC_G9CH2	AI		Analog input channel 2, group 9
	P00.10	O0		General-purpose output
	GTM_TOUT19	O1		GTM muxed output
	ASCLIN4_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	SENT_SPC9	O6		Transmit output
	CCU61_COUT63	O7		T13 PWM channel 63
	IOM_MON1_7			Monitor input 1
	IOM_REF1_7			Reference input 1

表 2-34 端口 P00 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
22	P00.11	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM1_IN2_1			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_1			**Mux input channel 2 of TIM module 0**
	CCU60_CTRAPA			**Trap input capture**
	EDSADC_DSCIN0A			**Modulator clock input, channel 0**
	CCU61_T12HRE			**External timer start 12**
	EVADC_G9CH1	AI		**Analog input channel 1, group 9**
	P00.11	O0		**General-purpose output**
	GTM_TOUT20	O1		**GTM muxed output**
	ASCLIN4_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	EDSADC_DSCOUT0	O4		**Modulator clock output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
23	P00.12	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM1_IN3_1			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_1			**Mux input channel 3 of TIM module 0**
	ASCLIN3_ACTSA			**Clear to send input**
	EDSADC_DSDIN0A			**Digital datastream input, channel 0**
	ASCLIN4_ARXA			**Receive input**
	EVADC_G9CH0	AI		**Analog input channel 0, group 9**
	P00.12	O0		**General-purpose output**
	GTM_TOUT21	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_7			**Monitor input 1**
	IOM_REF1_7			**Reference input 1**

表 2-35 端口 P02 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
1	P02.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN0_2			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_2			**Mux input channel 0 of TIM module 0**
	CCU61_CC60INB			**T12 capture input 60**
	ASCLIN2_ARXG			**Receive input**
	CCU60_CC60INA			**T12 capture input 60**
	SCU_E_REQ3_2			**ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GTM_DTMA0_0			**CDTM0_DTM4**
	P02.0	O0		**General-purpose output**
	GTM_TOUT0	O1		**GTM muxed output**
	IOM_REF0_0			**Reference input 0**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI3_SLSO1	O3		**Master slave select output**
	EDSADC_CGPWMN	O4		**Negative carrier generator output**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	ERAY0_TXDA	O6		**Transmit Channel A**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

表 2-35 端口 P02 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
2	P02.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN1_2			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_2			**Mux input channel 1 of TIM module 0**
	ERAY0_RXDA2			**Receive Channel A2**
	ASCLIN2_ARXB			**Receive input**
	CAN00_RXDA			**CAN receive input node 0**
	SCU_E_REQ2_1			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P02.1	O0		**General-purpose output**
	GTM_TOUT1	O1		**GTM muxed output**
	IOM_REF0_1			**Reference input 0**
	—	O2		**Reserved**
	QSPI3_SLSO2	O3		**Master slave select output**
	EDSADC_CGPWMP	O4		**Positive carrier generator output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**

表 2-35 端口 P02 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
3	P02.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN2_2			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_2			**Mux input channel 2 of TIM module 0**
	CCU61_CC61INB			**T12 capture input 61**
	CCU60_CC61INA			**T12 capture input 61**
	P02.2	O0		**General-purpose output**
	GTM_TOUT2	O1		**GTM muxed output**
	IOM_REF0_2			**Reference input 0**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI3_SLSO3	O3		**Master slave select output**
	PSI5_TX0	O4		**TXD outputs (send data)**
	IOM_MON1_14			**Monitor input 1**
	IOM_REF1_14			**Reference input 1**
	CAN02_TXD	O5		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	ERAY0_TXDB	O6		**Transmit Channel B**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**

表 2-35 端口 P02 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
4	P02.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN3_2			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_2			**Mux input channel 3 of TIM module 0**
	ERAY0_RXDB2			**Receive Channel B2**
	CAN02_RXDB			**CAN receive input node 2**
	ASCLIN1_ARXG			**Receive input**
	PSI5_RX0B			**RXD inputs (receive data) channel 0**
	P02.3	O0		**General-purpose output**
	GTM_TOUT3	O1		**GTM muxed output**
	IOM_REF0_3			**Reference input 0**
	ASCLIN2_ASLSO	O2		**Slave select signal output**
	QSPI3_SLSO4	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

表 2-35 端口 P02 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
5	P02.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN4_1			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_1			**Mux input channel 4 of TIM module 0**
	CCU61_CC62INB			**T12 capture input 62**
	QSPI3_SLSIA			**Slave select input**
	CCU60_CC62INA			**T12 capture input 62**
	I2C0_SDAA			**Serial Data Input 0**
	CAN11_RXDA			**CAN receive input node 1**
	CAN0_ECTT1			**External CAN time trigger input**
	P02.4	O0		**General-purpose output**
	GTM_TOUT4	O1		**GTM muxed output**
	IOM_REF0_4			**Reference input 0**
	ASCLIN2_ASCLK	O2		**Shift clock output**
	QSPI3_SLSO0	O3		**Master slave select output**
	PSI5S_CLK	O4		**PSI5S CLK is a clock that can be used on a pin to drive the external PHY.**
	I2C0_SDA	O5		**Serial Data Output**
	ERAY0_TXENA	O6		**Transmit Enable Channel A**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

表 2-35 端口 P02 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
6	P02.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN5_1			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_1			**Mux input channel 5 of TIM module 0**
	I2C0_SCLA			**Serial Clock Input 0**
	PSI5_RX1B			**RXD inputs (receive data) channel 1**
	PSI5S_RXB			**RX data input**
	QSPI3_MRSTA			**Master SPI data input**
	SENT_SENT3C			**Receive input channel 3**
	CAN0_ECTT2			**External CAN time trigger input**
	P02.5	O0		**General-purpose output**
	GTM_TOUT5	O1		**GTM muxed output**
	IOM_REF0_5			**Reference input 0**
	CAN11_TXD	O2		**CAN transmit output node 1**
	QSPI3_MRST	O3		**Slave SPI data output**
	IOM_MON2_3			**Monitor input 2**
	IOM_REF2_3			**Reference input 2**
	—	O4		**Reserved**
	I2C0_SCL	O5		**Serial Clock Output**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**

表 2-35 端口 P02 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
7	P02.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_1			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_1			**Mux input channel 6 of TIM module 0**
	CCU60_CC60INC			**T12 capture input 60**
	SENT_SENT2C			**Receive input channel 2**
	GPT120_T3INA			**Trigger/gate input of core timer T3**
	CCU60_CCPOS0A			**Hall capture input 0**
	CCU61_T12HRB			**External timer start 12**
	QSPI3_MTSRA			**Slave SPI data input**
	P02.6	O0		**General-purpose output**
	GTM_TOUT6	O1		**GTM muxed output**
	IOM_REF0_6			**Reference input 0**
	PSI5S_TX	O2		**TX data output**
	QSPI3_MTSR	O3		**Master SPI data output**
	PSI5_TX1	O4		**TXD outputs (send data)**
	IOM_MON1_15			**Monitor input 1**
	EVADC_EMUX00	O5		**Control of external analog multiplexer interface 0**
	—	O6		**Reserved**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

表 2-35 端口 P02 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
8	P02.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN7_1			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_1			**Mux input channel 7 of TIM module 0**
	CCU60_CC61INC			**T12 capture input 61**
	SENT_SENT1C			**Receive input channel 1**
	EDSADC_DSCIN3B			**Modulator clock input, channel 3**
	GPT120_T3EUDA			**Count direction control input of core timer T3**
	CCU60_CCPOS1A			**Hall capture input 1**
	QSPI3_SCLKA			**Slave SPI clock inputs**
	CCU61_T13HRB			**External timer start 13**
	P02.7	O0		**General-purpose output**
	GTM_TOUT7	O1		**GTM muxed output**
	IOM_REF0_7			**Reference input 0**
	—	O2		**Reserved**
	QSPI3_SCLK	O3		**Master SPI clock output**
	EDSADC_DSCOUT3	O4		**Modulator clock output**
	EVADC_EMUX01	O5		**Control of external analog multiplexer interface 0**
	SENT_SPC1	O6		**Transmit output**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**

表 2-35 端口 P02 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
9	P02.8	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN0_2			**Mux input channel 0 of TIM module 2**
	CCU60_CC62INC			**T12 capture input 62**
	SENT_SENT0C			**Receive input channel 0**
	CCU60_CCPOS2A			**Hall capture input 2**
	EDSADC_DSDIN3B			**Digital datastream input, channel 3**
	EDSADC_ITR3E			**Trigger/Gate input, channel 3**
	GPT120_T4INA			**Trigger/gate input of timer T4**
	CCU61_T12HRC			**External timer start 12**
	CCU61_T13HRC			**External timer start 13**
	GTM_DTMA0_1			**CDTM0_DTM4**
	P02.8	O0		**General-purpose output**
	GTM_TOUT8	O1		**GTM muxed output**
	IOM_REF0_8			**Reference input 0**
	QSPI3_SLSO5	O2		**Master slave select output**
	ASCLIN8_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	EVADC_EMUX02	O5		**Control of external analog multiplexer interface 0**
	GETH_MDC	O6		**MDIO clock**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

表 2-36 端口 P10 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
168	P10.0	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN4_2			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_2			Mux input channel 4 of TIM module 0
	GPT120_T6EUDB			Count direction control input of core timer T6
	ASCLIN11_ARXA			Receive input
	GETH_RXERC			Receive Error MII
	P10.0	O0		General-purpose output
	GTM_TOUT102	O1		GTM muxed output
	ASCLIN11_ATX	O2		Transmit output
	QSPI1_SLSO10	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
169	P10.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_3			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_3			Mux input channel 1 of TIM module 0
	GPT120_T5EUDB			Count direction control input of timer T5
	QSPI1_MRSTA			Master SPI data input
	GTM_DTMT0_1			CDTM0_DTM0
	P10.1	O0		General-purpose output
	GTM_TOUT103	O1		GTM muxed output
	QSPI1_MTSR	O2		Master SPI data output
	QSPI1_MRST	O3		Slave SPI data output
	IOM_MON2_1			Monitor input 2
	IOM_REF2_1			Reference input 2
	MSC0_EN1	O4		Chip Select
	EVADC_FC1BFLOUT	O5		Boundary flag output, FC channel 1
	—	O6		Reserved
	—	O7		Reserved

表 2-36 端口 P10 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
170	P10.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_3			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_3			Mux input channel 2 of TIM module 0
	CAN02_RXDE			CAN receive input node 2
	MSC0_SDI1			Upstream assynchronous input signal
	QSPI1_SCLKA			Slave SPI clock inputs
	GPT120_T6INB			Trigger/gate input of core timer T6
	SCU_E_REQ2_0			ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P10.2	O0		General-purpose output
	GTM_TOUT104	O1		GTM muxed output
	IOM_MON2_9			Monitor input 2
	—	O2		Reserved
	QSPI1_SCLK	O3		Master SPI clock output
	MSC0_EN0	O4		Chip Select
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
171	P10.3	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN3_3			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_3			Mux input channel 3 of TIM module 0
	QSPI1_MTSRA			Slave SPI data input
	SCU_E_REQ3_0			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	GPT120_T5INB			Trigger/gate input of timer T5
	P10.3	O0		General-purpose output
	GTM_TOUT105	O1		GTM muxed output
	IOM_MON2_10			Monitor input 2
	—	O2		Reserved
	QSPI1_MTSR	O3		Master SPI data output
	MSC0_EN0	O4		Chip Select
	—	O5		Reserved
	CAN02_TXD	O6		CAN transmit output node 2
	IOM_MON2_7			Monitor input 2
	IOM_REF2_7			Reference input 2
	—	O7		Reserved

表 2-36 端口 P10 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
172	P10.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_2			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_2			**Mux input channel 6 of TIM module 0**
	QSPI1_MTSRC			**Slave SPI data input**
	CCU60_CCPOS0C			**Hall capture input 0**
	GPT120_T3INB			**Trigger/gate input of core timer T3**
	ASCLIN11_ARXB			**Receive input**
	P10.4	O0		**General-purpose output**
	GTM_TOUT106	O1		**GTM muxed output**
	IOM_MON2_11			**Monitor input 2**
	—	O2		**Reserved**
	QSPI1_SLSO8	O3		**Master slave select output**
	QSPI1_MTSR	O4		**Master SPI data output**
	MSC0_EN0	O5		**Chip Select**
	—	O6		**Reserved**
	—	O7		**Reserved**
173	P10.5	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN2_4			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_4			**Mux input channel 2 of TIM module 0**
	PMS_HWCFG4IN			**HWCFG4 pin input**
	MSC0_INJ1			**Injection signal from port**
	P10.5	O0		**General-purpose output**
	GTM_TOUT107	O1		**GTM muxed output**
	IOM_REF2_9			**Reference input 2**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI3_SLSO8	O3		**Master slave select output**
	QSPI1_SLSO9	O4		**Master slave select output**
	GPT120_T6OUT	O5		**External output for overflow/underflow detection of core timer T6**
	ASCLIN2_ASLSO	O6		**Slave select signal output**
	—	O7		**Reserved**

表 2-36 端口 P10 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
174	P10.6	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN3_4			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_4			**Mux input channel 3 of TIM module 0**
	ASCLIN2_ARXD			**Receive input**
	QSPI3_MTSRB			**Slave SPI data input**
	PMS_HWCFG5IN			**HWCFG5 pin input**
	P10.6	O0		**General-purpose output**
	GTM_TOUT108	O1		**GTM muxed output**
	IOM_REF2_10			**Reference input 2**
	ASCLIN2_ASCLK	O2		**Shift clock output**
	QSPI3_MTSR	O3		**Master SPI data output**
	GPT120_T3OUT	O4		**External output for overflow/underflow detection of core timer T3**
	—	O5		**Reserved**
	QSPI1_MRST	O6		**Slave SPI data output**
	IOM_MON2_1			**Monitor input 2**
	IOM_REF2_1			**Reference input 2**
	—	O7		**Reserved**
175	P10.7	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN0_3			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_3			**Mux input channel 0 of TIM module 0**
	GPT120_T3EUDB			**Count direction control input of core timer T3**
	ASCLIN2_ACTSA			**Clear to send input**
	QSPI3_MRSTB			**Master SPI data input**
	SCU_E_REQ0_2			**ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	CCU60_CCPOS1C			**Hall capture input 1**
	P10.7	O0		**General-purpose output**
	GTM_TOUT109	O1		**GTM muxed output**
	IOM_REF2_11			**Reference input 2**
	—	O2		**Reserved**
	QSPI3_MRST	O3		**Slave SPI data output**
	IOM_MON2_3			**Monitor input 2**
	IOM_REF2_3			**Reference input 2**
	—	O4		**Reserved**
	—	O5		**Reserved**
	CAN12_TXD	O6		**CAN transmit output node 2**
	—	O7		**Reserved**

表 2-36 端口 P10 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
176	P10.8	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN5_2			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_2			**Mux input channel 5 of TIM module 0**
	CAN12_RXDB			**CAN receive input node 2**
	GPT120_T4INB			**Trigger/gate input of timer T4**
	QSPI3_SCLKB			**Slave SPI clock inputs**
	SCU_E_REQ1_2			**ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	CCU60_CCPOS2C			**Hall capture input 2**
	P10.8	O0		**General-purpose output**
	GTM_TOUT110	O1		**GTM muxed output**
	ASCLIN2_ARTS	O2		**Ready to send output**
	QSPI3_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

表 2-37 端口 P11 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
160	P11.2	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM2_IN1_3			**Mux input channel 1 of TIM module 2**
	P11.2	O0		**General-purpose output**
	GTM_TOUT95	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SLSO5	O3		**Master slave select output**
	QSPI1_SLSO5	O4		**Master slave select output**
	MSC0_EN1	O5		**Chip Select**
	GETH_TXD1	O6		**Transmit Data**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**

表 2-37 端口 P11 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
161	P11.3	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM2_IN2_2			**Mux input channel 2 of TIM module 2**
	MSC0_SDI3			**Upstream assynchronous input signal**
	QSPI1_MRSTB			**Master SPI data input**
	P11.3	O0		**General-purpose output**
	GTM_TOUT96	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI1_MRST	O3		**Slave SPI data output**
	IOM_MON2_1			**Monitor input 2**
	IOM_REF2_1			**Reference input 2**
	ERAY0_TXDA	O4		**Transmit Channel A**
	—	O5		**Reserved**
	GETH_TXD0	O6		**Transmit Data**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**
162	P11.6	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM2_IN3_2			**Mux input channel 3 of TIM module 2**
	QSPI1_SCLKB			**Slave SPI clock inputs**
	P11.6	O0		**General-purpose output**
	GTM_TOUT97	O1		**GTM muxed output**
	ERAY0_TXENB	O2		**Transmit Enable Channel B**
	QSPI1_SCLK	O3		**Master SPI clock output**
	ERAY0_TXENA	O4		**Transmit Enable Channel A**
	MSC0_FCLP	O5		**Shift-clock direct part of the differential signal**
	GETH_TXEN	O6		**Transmit Enable MII and RMII**
	GETH_TCTL			**Transmit Control for RGMII**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

表 2-37 端口 P11 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
163	P11.9	I	FAST / RGMII_Input / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM2_IN4_2			Mux input channel 4 of TIM module 2
	QSPI1_MTSRB			Slave SPI data input
	ERAY0_RXDA1			Receive Channel A1
	GETH_RXD1A			Receive Data 1 MII, RMII and RGMII (RGMII can use RXD1A only)
	P11.9	O0		General-purpose output
	GTM_TOUT98	O1		GTM muxed output
	—	O2		Reserved
	QSPI1_MTSR	O3		Master SPI data output
	—	O4		Reserved
	MSC0_SOP	O5		Data output - direct part of the differential signal
	—	O6		Reserved
	CCU60_COUT60	O7		T12 PWM channel 60
	IOM_MON1_3			Monitor input 1
	IOM_REF1_3			Reference input 1
165	P11.10	I	FAST / RGMII_Input / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM2_IN5_2			Mux input channel 5 of TIM module 2
	GTM_TIM2_IN0_9			Mux input channel 0 of TIM module 2
	CAN03_RXDD			CAN receive input node 3
	ERAY0_RXDB1			Receive Channel B1
	ASCLIN1_ARXE			Receive input
	SCU_E_REQ6_3			ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	MSC0_SDI0			Upstream assynchronous input signal
	GETH_RXD0A			Receive Data 0 MII, RMII and RGMII (RGMII can use RXD0A only)
	QSPI1_SLSIA			Slave select input
	P11.10	O0		General-purpose output
	GTM_TOUT99	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO3	O3		Master slave select output
	QSPI1_SLSO3	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	CCU60_CC62	O7		T12 PWM channel 62
	IOM_MON1_0			Monitor input 1
	IOM_REF1_4			Reference input 1

表 2-37 端口 P11 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
166	P11.11	I	FAST / RGMII_Input / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM2_IN6_2			Mux input channel 6 of TIM module 2
	GETH_CRSDVA			Carrier Sense / Data Valid combi-signal for RMII
	GETH_RXDVA			Receive Data Valid MII
	GETH_CRSB			Carrier Sense MII
	GETH_RCTLA			Receive Control for RGMII
	P11.11	O0		General-purpose output
	GTM_TOUT100	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO4	O3		Master slave select output
	QSPI1_SLSO4	O4		Master slave select output
	MSC0_EN0	O5		Chip Select
	ERAY0_TXENB	O6		Transmit Enable Channel B
	CCU60_CC61	O7		T12 PWM channel 61
	IOM_MON1_1			Monitor input 1
	IOM_REF1_5			Reference input 1
167	P11.12	I	FAST / RGMII_Input / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM2_IN7_2			Mux input channel 7 of TIM module 2
	GETH_REFCLKA			Reference Clock input for RMII (50 MHz)
	GETH_TXCLKB			Transmit Clock Input for MII
	GETH_RXCLKA			Receive Clock MII
	P11.12	O0		General-purpose output
	GTM_TOUT101	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	GTM_CLK2	O3		CGM generated clock
	ERAY0_TXDB	O4		Transmit Channel B
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	CCU_EXTCLK1	O6		External Clock 1
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
	IOM_REF1_6			Reference input 1

表 2-38 端口 P13 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
156	P13.0	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM2_IN5_3			Mux input channel 5 of TIM module 2
	ASCLIN10_ARXC			Receive input
	P13.0	O0		General-purpose output
	GTM_TOUT91	O1		GTM muxed output
	ASCLIN10_ATX	O2		Transmit output
	QSPI2_SCLKN	O3		Master SPI clock output (LVDS N line)
	MSC0_EN1	O4		Chip Select
	MSC0_FCLN	O5		Shift-clock inverted part of the differential signal
	—	O6		Reserved
	CAN10_TXD	O7		CAN transmit output node 0
157	P13.1	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM2_IN6_3			Mux input channel 6 of TIM module 2
	I2C0_SCLB			Serial Clock Input 1
	CAN10_RXDD			CAN receive input node 0
	ASCLIN10_ARXD			Receive input
	P13.1	O0		General-purpose output
	GTM_TOUT92	O1		GTM muxed output
	—	O2		Reserved
	QSPI2_SCLKP	O3		Master SPI clock output (LVDS P line)
	—	O4		Reserved
	MSC0_FCLP	O5		Shift-clock direct part of the differential signal
	I2C0_SCL	O6		Serial Clock Output
	—	O7		Reserved
158	P13.2	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM2_IN7_3			Mux input channel 7 of TIM module 2
	GPT120_CAPINA			Trigger input to capture value of timer T5 into CAPREL register
	I2C0_SDAB			Serial Data Input 1
	P13.2	O0		General-purpose output
	GTM_TOUT93	O1		GTM muxed output
	ASCLIN10_ASCLK	O2		Shift clock output
	QSPI2_MTSRN	O3		Master SPI data output (LVDS N line)
	MSC0_FCLP	O4		Shift-clock direct part of the differential signal
	MSC0_SON	O5		Data output - inverted part of the differential signal
	I2C0_SDA	O6		Serial Data Output
	—	O7		Reserved

表 2-38 端口 P13 功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
159	P13.3	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM2_IN0_3			Mux input channel 0 of TIM module 2
	P13.3	O0		General-purpose output
	GTM_TOUT94	O1		GTM muxed output
	ASCLIN10_ASLSO	O2		Slave select signal output
	QSPI2_MTSRP	O3		Master SPI data output (LVDS P line)
	—	O4		Reserved
	MSC0_SOP	O5		Data output - direct part of the differential signal
	—	O6		Reserved
	—	O7		Reserved

表 2-39 端口 P14 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
142	P14.0	I	FAST / PU1 / VEXT / ES2	General-purpose input
	GTM_TIM1_IN3_5			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_5			Mux input channel 3 of TIM module 0
	P14.0	O0		General-purpose output
	GTM_TOUT80	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	ERAY0_TXDA	O3		Transmit Channel A
	ERAY0_TXDB	O4		Transmit Channel B
	CAN01_TXD	O5		CAN transmit output node 1
	IOM_MON2_6			Monitor input 2
	IOM_REF2_6			Reference input 2
	ASCLIN0_ASCLK	O6		Shift clock output
	CCU60_COUT62	O7		T12 PWM channel 62
	IOM_MON1_5			Monitor input 1
	IOM_REF1_1			Reference input 1

表 2-39 端口 P14 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
143	P14.1	I	FAST / PU1 / VEXT / ES2	General-purpose input
	GTM_TIM1_IN4_3			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_3			Mux input channel 4 of TIM module 0
	ERAY0_RXDA3			Receive Channel A3
	ASCLIN0_ARXA			Receive input
	ERAY0_RXDB3			Receive Channel B3
	CAN01_RXDB			CAN receive input node 1
	SCU_E_REQ3_1			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	PMS_PINAWKP			PINA (P14.1) pin input
	P14.1	O0		General-purpose output
	GTM_TOUT81	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1
144	P14.2	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN5_3			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_3			Mux input channel 5 of TIM module 0
	PMS_HWCFG2IN			HWCFG2 pin input
	P14.2	O0		General-purpose output
	GTM_TOUT82	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI2_SLSO1	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	ASCLIN2_ASCLK	O6		Shift clock output
	—	O7		Reserved

表 2-39 端口 P14 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
145	P14.3	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_3			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_3			**Mux input channel 6 of TIM module 0**
	PMS_HWCFG3IN			**HWCFG3 pin input**
	ASCLIN2_ARXA			**Receive input**
	MSC0_SDI2			**Upstream assynchronous input signal**
	SCU_E_REQ1_0			**ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P14.3	O0		**General-purpose output**
	GTM_TOUT83	O1		**GTM muxed output**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI2_SLSO3	O3		**Master slave select output**
	ASCLIN1_ASLSO	O4		**Slave select signal output**
	ASCLIN3_ASLSO	O5		**Slave select signal output**
	—	O6		**Reserved**
	—	O7		**Reserved**
146	P14.4	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN7_2			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_2			**Mux input channel 7 of TIM module 0**
	PMS_HWCFG6IN			**HWCFG6 pin input**
	GTM_DTMT0_0			**CDTM0_DTM0**
	P14.4	O0		**General-purpose output**
	GTM_TOUT84	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	GETH_PPS	O6		**Pulse Per Second**
	—	O7		**Reserved**

表 2-39 端口 P14 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
147	P14.5	I	FAST / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN0_4			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_4			**Mux input channel 0 of TIM module 0**
	PMS_HWCFG1IN			**HWCFG1 pin input**
	GTM_DTMA2_0			**CDTM2_DTM4**
	P14.5	O0		**General-purpose output**
	GTM_TOUT85	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ERAY0_TXDB	O6		**Transmit Channel B**
	—	O7		**Reserved**
148	P14.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN1_4			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_4			**Mux input channel 1 of TIM module 0**
	P14.6	O0		**General-purpose output**
	GTM_TOUT86	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SLSO2	O3		**Master slave select output**
	CAN13_TXD	O4		**CAN transmit output node 3**
	—	O5		**Reserved**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	—	O7		**Reserved**

表 2-39 端口 P14 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
149	P14.7	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN0_5			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_5			**Mux input channel 0 of TIM module 0**
	ERAY0_RXDB0			**Receive Channel B0**
	CAN10_RXDB			**CAN receive input node 0**
	CAN13_RXDA			**CAN receive input node 3**
	ASCLIN9_ARXC			**Receive input**
	P14.7	O0		**General-purpose output**
	GTM_TOUT87	O1		**GTM muxed output**
	ASCLIN0_ARTS	O2		**Ready to send output**
	QSPI2_SLSO4	O3		**Master slave select output**
	ASCLIN9_ATX	O4		**Transmit output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
150	P14.8	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN2_3			**Mux input channel 2 of TIM module 2**
	ERAY0_RXDA0			**Receive Channel A0**
	CAN02_RXDD			**CAN receive input node 2**
	ASCLIN1_ARXD			**Receive input**
	P14.8	O0		**General-purpose output**
	GTM_TOUT88	O1		**GTM muxed output**
	ASCLIN5_ASLSO	O2		**Slave select signal output**
	ASCLIN7_ASLSO	O3		**Slave select signal output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

表 2-39 端口 P14 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
151	P14.9	I	LVDS_R X / FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN3_3			Mux input channel 3 of TIM module 2
	ASCLIN0_ACTSA			Clear to send input
	QSPI2_MRSTFN			Master SPI data input (LVDS N line)
	ASCLIN9_ARXD			Receive input
	P14.9	O0		General-purpose output
	GTM_TOUT89	O1		GTM muxed output
	—	O2		Reserved
	MSC0_EN1	O3		Chip Select
	CAN10_TXD	O4		CAN transmit output node 0
	ERAY0_TXENB	O5		Transmit Enable Channel B
	ERAY0_TXENA	O6		Transmit Enable Channel A
	—	O7		Reserved
152	P14.10	I	LVDS_R X / FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN4_3			Mux input channel 4 of TIM module 2
	QSPI2_MRSTFP			Master SPI data input (LVDS P line)
	P14.10	O0		General-purpose output
	GTM_TOUT90	O1		GTM muxed output
	—	O2		Reserved
	MSC0_EN0	O3		Chip Select
	ASCLIN1_ATX	O4		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	CAN02_TXD	O5		CAN transmit output node 2
	IOM_MON2_7			Monitor input 2
	IOM_REF2_7			Reference input 2
	ERAY0_TXDA	O6		Transmit Channel A
	—	O7		Reserved

表 2-40 端口 P15 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
133	P15.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN3_4			Mux input channel 3 of TIM module 2
	P15.0	O0		General-purpose output
	GTM_TOUT71	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI0_SLSO13	O3		Master slave select output
	—	O4		Reserved
	CAN02_TXD	O5		CAN transmit output node 2
	IOM_MON2_7			Monitor input 2
	IOM_REF2_7			Reference input 2
	ASCLIN1_ASCLK	O6		Shift clock output
	—	O7		Reserved
134	P15.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN4_4			Mux input channel 4 of TIM module 2
	CAN02_RXDA			CAN receive input node 2
	ASCLIN1_ARXA			Receive input
	QSPI2_SLSIB			Slave select input
	SCU_E_REQ7_2			ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P15.1	O0		General-purpose output
	GTM_TOUT72	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI2_SLSO5	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-40 端口 P15 功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
135	P15.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN5_4			Mux input channel 5 of TIM module 2
	QSPI2_SLSIA			Slave select input
	QSPI2_MRSTE			Master SPI data input
	P15.2	O0		General-purpose output
	GTM_TOUT73	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	QSPI2_SLSO0	O3		Master slave select output
	—	O4		Reserved
	CAN01_TXD	O5		CAN transmit output node 1
	IOM_MON2_6			Monitor input 2
	IOM_REF2_6			Reference input 2
	ASCLIN0_ASCLK	O6		Shift clock output
	—	O7		Reserved
136	P15.3	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN6_4			Mux input channel 6 of TIM module 2
	CAN01_RXDA			CAN receive input node 1
	ASCLIN0_ARXB			Receive input
	QSPI2_SCLKA			Slave SPI clock inputs
	P15.3	O0		General-purpose output
	GTM_TOUT74	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	MSC0_EN1	O5		Chip Select
	—	O6		Reserved
	—	O7		Reserved

表 2-40 端口 P15 功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
137	P15.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN7_4			**Mux input channel 7 of TIM module 2**
	I2C0_SCLC			**Serial Clock Input 2**
	QSPI2_MRSTA			**Master SPI data input**
	SCU_E_REQ0_0			**ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.4	O0		**General-purpose output**
	GTM_TOUT75	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI2_MRST	O3		**Slave SPI data output**
	IOM_MON2_2			**Monitor input 2**
	IOM_REF2_2			**Reference input 2**
	—	O4		**Reserved**
	—	O5		**Reserved**
	I2C0_SCL	O6		**Serial Clock Output**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

表 2-40 端口 P15 功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
138	P15.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN0_4			**Mux input channel 0 of TIM module 2**
	ASCLIN1_ARXB			**Receive input**
	I2C0_SDAC			**Serial Data Input 2**
	QSPI2_MTSRA			**Slave SPI data input**
	SCU_E_REQ4_3			**ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.5	O0		**General-purpose output**
	GTM_TOUT76	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI2_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	MSC0_EN0	O5		**Chip Select**
	I2C0_SDA	O6		**Serial Data Output**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**
139	P15.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN2_14			**Mux input channel 2 of TIM module 2**
	GTM_TIM1_IN0_6			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_6			**Mux input channel 0 of TIM module 0**
	QSPI2_MTSRB			**Slave SPI data input**
	P15.6	O0		**General-purpose output**
	GTM_TOUT77	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	QSPI2_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	QSPI2_SCLK	O5		**Master SPI clock output**
	ASCLIN3_ASCLK	O6		**Shift clock output**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

表 2-40 端口 P15 功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
140	P15.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN1_5			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_5			**Mux input channel 1 of TIM module 0**
	ASCLIN3_ARXA			**Receive input**
	QSPI2_MRSTB			**Master SPI data input**
	P15.7	O0		**General-purpose output**
	GTM_TOUT78	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	QSPI2_MRST	O3		**Slave SPI data output**
	IOM_MON2_2			**Monitor input 2**
	IOM_REF2_2			**Reference input 2**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**
141	P15.8	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN2_5			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_5			**Mux input channel 2 of TIM module 0**
	QSPI2_SCLKB			**Slave SPI clock inputs**
	SCU_E_REQ5_0			**ERU Channel 5 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.8	O0		**General-purpose output**
	GTM_TOUT79	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ASCLIN3_ASCLK	O6		**Shift clock output**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

表 2-41 端口 P20 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
116	P20.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_7			**Mux input channel 6 of TIM module 1**
	GTM_TIM1_IN4_9			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN6_7			**Mux input channel 6 of TIM module 0**
	CAN03_RXDC			**CAN receive input node 3**
	CCU_PAD_SYSCLK			**Sysclk input**
	CBS_TGI0			**Trigger input**
	SCU_E_REQ6_0			**ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GPT120_T6EUDA			**Count direction control input of core timer T6**
	P20.0	O0		**General-purpose output**
	GTM_TOUT59	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	ASCLIN3_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	HSCT0_SYSCLK_OUT	O5		**sys clock output**
	—	O6		**Reserved**
	—	O7		**Reserved**
	CBS_TGO0	O		**Trigger output**
117	P20.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN3_5			**Mux input channel 3 of TIM module 2**
	CBS_TGI1			**Trigger input**
	GTM_DTMA1_1			**CDTM1_DTM4**
	P20.1	O0		**General-purpose output**
	GTM_TOUT60	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	CBS_TGO1	O		**Trigger output**
118	P20.2	I	S / PU / VEXT	**General-purpose input** This pin is latched at power on reset release to enter test mode.
	$\overline{\text{TESTMODE}}$			**Testmode Enable Input**

表 2-41 端口 P20 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
119	P20.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN4_5			**Mux input channel 4 of TIM module 2**
	ASCLIN3_ARXC			**Receive input**
	GPT120_T6INA			**Trigger/gate input of core timer T6**
	P20.3	O0		**General-purpose output**
	GTM_TOUT61	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	QSPI0_SLSO9	O3		**Master slave select output**
	QSPI2_SLSO9	O4		**Master slave select output**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	—	O6		**Reserved**
	—	O7		**Reserved**
124	P20.6	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN6_5			**Mux input channel 6 of TIM module 2**
	CAN12_RXDA			**CAN receive input node 2**
	ASCLIN9_ARXE			**Receive input**
	P20.6	O0		**General-purpose output**
	GTM_TOUT62	O1		**GTM muxed output**
	ASCLIN1_ARTS	O2		**Ready to send output**
	QSPI0_SLSO8	O3		**Master slave select output**
	QSPI2_SLSO8	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

表 2-41 端口 P20 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
125	P20.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN7_5			**Mux input channel 7 of TIM module 2**
	GTM_TIM1_IN5_8			**Mux input channel 5 of TIM module 1**
	CAN00_RXDB			**CAN receive input node 0**
	ASCLIN1_ACTSA			**Clear to send input**
	ASCLIN9_ARXF			**Receive input**
	P20.7	O0		**General-purpose output**
	GTM_TOUT63	O1		**GTM muxed output**
	ASCLIN9_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN12_TXD	O5		**CAN transmit output node 2**
	—	O6		**Reserved**
	CCU61_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_7			**Monitor input 1**
	IOM_REF1_7			**Reference input 1**
126	P20.8	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN7_3			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_3			**Mux input channel 7 of TIM module 0**
	P20.8	O0		**General-purpose output**
	GTM_TOUT64	O1		**GTM muxed output**
	ASCLIN1_ASLSO	O2		**Slave select signal output**
	QSPI0_SLSO0	O3		**Master slave select output**
	QSPI1_SLSO0	O4		**Master slave select output**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

表 2-41 端口 P20 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
127	P20.9	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN5_5			**Mux input channel 5 of TIM module 2**
	CAN03_RXDE			**CAN receive input node 3**
	ASCLIN1_ARXC			**Receive input**
	QSPI0_SLSIB			**Slave select input**
	SCU_E_REQ7_0			**ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P20.9	O0		**General-purpose output**
	GTM_TOUT65	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SLSO1	O3		**Master slave select output**
	QSPI1_SLSO1	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**
128	P20.10	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN6_6			**Mux input channel 6 of TIM module 2**
	P20.10	O0		**General-purpose output**
	GTM_TOUT66	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI0_SLSO6	O3		**Master slave select output**
	QSPI2_SLSO7	O4		**Master slave select output**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	ASCLIN1_ASCLK	O6		**Shift clock output**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**

表 2-41 端口 P20 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
129	P20.11	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN7_6			**Mux input channel 7 of TIM module 2**
	QSPI0_SCLKA			**Slave SPI clock inputs**
	P20.11	O0		**General-purpose output**
	GTM_TOUT67	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**
130	P20.12	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN0_5			**Mux input channel 0 of TIM module 2**
	QSPI0_MRSTA			**Master SPI data input**
	IOM_PIN_13			**GPIO pad input to FPC**
	P20.12	O0		**General-purpose output**
	GTM_TOUT68	O1		**GTM muxed output**
	IOM_MON0_13			**Monitor input 0**
	—	O2		**Reserved**
	QSPI0_MRST	O3		**Slave SPI data output**
	IOM_MON2_0			**Monitor input 2**
	IOM_REF2_0			**Reference input 2**
	QSPI0_MTSR	O4		**Master SPI data output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_12			**Monitor input 1**
	IOM_REF1_9			**Reference input 1**

表 2-41 端口 P20 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
131	P20.13	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN1_4			**Mux input channel 1 of TIM module 2**
	QSPI0_SLSIA			**Slave select input**
	IOM_PIN_14			**GPIO pad input to FPC**
	P20.13	O0		**General-purpose output**
	GTM_TOUT69	O1		**GTM muxed output**
	IOM_MON0_14			**Monitor input 0**
	—	O2		**Reserved**
	QSPI0_SLSO2	O3		**Master slave select output**
	QSPI1_SLSO2	O4		**Master slave select output**
	QSPI0_SCLK	O5		**Master SPI clock output**
	—	O6		**Reserved**
	CCU61_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_13			**Monitor input 1**
	IOM_REF1_8			**Reference input 1**
132	P20.14	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN2_4			**Mux input channel 2 of TIM module 2**
	QSPI0_MTSRA			**Slave SPI data input**
	IOM_PIN_15			**GPIO pad input to FPC**
	DMU_FDEST			**Enter destructive debug mode**
	P20.14	O0		**General-purpose output**
	GTM_TOUT70	O1		**GTM muxed output**
	IOM_MON0_15			**Monitor input 0**
	—	O2		**Reserved**
	QSPI0_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

表 2-42 端口 P21 的功能

Pin	Symbol	Ctrl.	Buffer Type	Function
105	P21.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN4_6			**Mux input channel 4 of TIM module 2**
	ASCLIN11_ARXC			**Receive input**
	P21.0	O0		**General-purpose output**
	GTM_TOUT51	O1		**GTM muxed output**
	ASCLIN11_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSM_HSM1	O		**Pin Output Value**
106	P21.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN5_6			**Mux input channel 5 of TIM module 2**
	ASCLIN11_ARXD			**Receive input**
	P21.1	O0		**General-purpose output**
	GTM_TOUT52	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSM_HSM2	O		**Pin Output Value**

表 2-42 端口 P21 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
107	P21.2	I	LVDS_RX / FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_7			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_7			Mux input channel 0 of TIM module 0
	QSPI2_MRSTCN			Master SPI data input (LVDS N line)
	SCU_EMGSTOP_PORT_B			Emergency stop Port Pin B input request
	ASCLIN3_ARXGN			Differential Receive input (low active)
	HSCT0_RXDN			Rx data
	ASCLIN11_ARXE			Receive input
	GTM_DTMA1_0			CDTM1_DTM4
	P21.2	O0		General-purpose output
	GTM_TOUT53	O1		GTM muxed output
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	GETH_MDC	O5		MDIO clock
	—	O6		Reserved
	—	O7		Reserved
108	P21.3	I	LVDS_RX / FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_6			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_6			Mux input channel 1 of TIM module 0
	QSPI2_MRSTCP			Master SPI data input (LVDS P line)
	ASCLIN3_ARXGP			Differential Receive input (high active)
	GETH_MDIOD			MDIO Input
	HSCT0_RXDP			Rx data
	P21.3	O0		General-purpose output
	GTM_TOUT54	O1		GTM muxed output
	ASCLIN11_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	GETH_MDIO	O		MDIO Output

表 2-42 端口 P21 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
109	P21.4	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM1_IN2_6			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_6			**Mux input channel 2 of TIM module 0**
	P21.4	O0		**General-purpose output**
	GTM_TOUT55	O1		**GTM muxed output**
	ASCLIN11_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSCT0_TXDN	O		**Tx data**
110	P21.5	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM1_IN3_6			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_6			**Mux input channel 3 of TIM module 0**
	ASCLIN11_ARXF			**Receive input**
	P21.5	O0		**General-purpose output**
	GTM_TOUT56	O1		**GTM muxed output**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN11_ATX	O3		**Transmit output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSCT0_TXDP	O		**Tx data**

表 2-42 端口 P21 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
111	P21.6/TDI	I	FAST / PD / PU2 / VEXT / ES3	**General-purpose input** PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ.
	GTM_TIM1_IN4_8			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_8			**Mux input channel 4 of TIM module 0**
	GPT120_T5EUDA			**Count direction control input of timer T5**
	ASCLIN3_ARXF			**Receive input**
	CBS_TGI2			**Trigger input**
	TDI			**JTAG Module Data Input**
	P21.6	O0		**General-purpose output**
	GTM_TOUT57	O1		**GTM muxed output**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	GPT120_T3OUT	O7		**External output for overflow/underflow detection of core timer T3**
	CBS_TGO2	O		**Trigger output**
	DAP3	I/O		**DAP: DAP3 Data I/O**

表 2-42 端口 P21 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
113	P21.7/TDO	I	FAST / PU2 / VEXT / ES4	**General-purpose input**
	GTM_TIM1_IN5_7			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_7			**Mux input channel 5 of TIM module 0**
	GPT120_T5INA			**Trigger/gate input of timer T5**
	CBS_TGI3			**Trigger input**
	GETH_RXERB			**Receive Error MII**
	P21.7	O0		**General-purpose output**
	GTM_TOUT58	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	ASCLIN3_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	GPT120_T6OUT	O7		**External output for overflow/underflow detection of core timer T6**
	CBS_TGO3	O		**Trigger output**
	DAP2	I/O		**DAP: DAP2 Data I/O**
	TDO	O		**JTAG Module Data Output**

表 2-43 端口 P22 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
95	P22.0	I	FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN1_7			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_7			Mux input channel 1 of TIM module 0
	ASCLIN6_ARXE			Receive input
	QSPI3_MTSRD			Slave SPI data input
	P22.0	O0		General-purpose output
	GTM_TOUT47	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	QSPI3_MTSR	O3		Master SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	ASCLIN6_ATX	O7		Transmit output
96	P22.1	I	FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN0_8			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_8			Mux input channel 0 of TIM module 0
	ASCLIN7_ARXE			Receive input
	QSPI3_MRSTD			Master SPI data input
	P22.1	O0		General-purpose output
	GTM_TOUT48	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	QSPI3_MRST	O3		Slave SPI data output
	IOM_MON2_3			Monitor input 2
	IOM_REF2_3			Reference input 2
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	ASCLIN7_ATX	O7		Transmit output

表 2-43 端口 P22 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
97	P22.2	I	FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM1_IN3_7			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_7			**Mux input channel 3 of TIM module 0**
	P22.2	O0		**General-purpose output**
	GTM_TOUT49	O1		**GTM muxed output**
	ASCLIN5_ATX	O2		**Transmit output**
	QSPI3_SLSO12	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
98	P22.3	I	FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM1_IN4_4			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_4			**Mux input channel 4 of TIM module 0**
	ASCLIN5_ARXC			**Receive input**
	QSPI3_SCLKD			**Slave SPI clock inputs**
	P22.3	O0		**General-purpose output**
	GTM_TOUT50	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI3_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

表 2-44 端口 P23 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
89	P23.0	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN5_4			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_4			Mux input channel 5 of TIM module 0
	CAN10_RXDC			CAN receive input node 0
	P23.0	O0		General-purpose output
	GTM_TOUT41	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
90	P23.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_4			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_4			Mux input channel 6 of TIM module 0
	ASCLIN6_ARXF			Receive input
	P23.1	O0		General-purpose output
	GTM_TOUT42	O1		GTM muxed output
	ASCLIN1_ARTS	O2		Ready to send output
	—	O3		Reserved
	GTM_CLK0	O4		CGM generated clock
	CAN10_TXD	O5		CAN transmit output node 0
	CCU_EXTCLK0	O6		External Clock 0
	ASCLIN6_ASCLK	O7		Shift clock output
91	P23.2	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_5			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_5			Mux input channel 6 of TIM module 0
	ASCLIN7_ARXC			Receive input
	P23.2	O0		General-purpose output
	GTM_TOUT43	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	CAN12_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	—	O7		Reserved

表 2-44 端口 P23 功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
92	P23.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN7_4			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_4			**Mux input channel 7 of TIM module 0**
	ASCLIN6_ARXA			**Receive input**
	CAN12_RXDC			**CAN receive input node 2**
	P23.3	O0		**General-purpose output**
	GTM_TOUT44	O1		**GTM muxed output**
	ASCLIN7_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
93	P23.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN7_5			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_5			**Mux input channel 7 of TIM module 0**
	P23.4	O0		**General-purpose output**
	GTM_TOUT45	O1		**GTM muxed output**
	ASCLIN6_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
94	P23.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN2_7			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_7			**Mux input channel 2 of TIM module 0**
	P23.5	O0		**General-purpose output**
	GTM_TOUT46	O1		**GTM muxed output**
	ASCLIN6_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

表 2-45 端口 P32 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
84	P32.0	I	SLOW / PU1 / VEXT / ES	**General-purpose input** P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
	GTM_TIM2_IN2_5			**Mux input channel 2 of TIM module 2**
	P32.0	O0		**General-purpose output**
	GTM_TOUT36	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
85	P32.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input** P32.1 / External Pass Device gate control for EVRC
	P32.1	O0		**General-purpose output**
	GTM_TOUT37	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
86	P32.2	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN3_8			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_8			**Mux input channel 3 of TIM module 0**
	CAN03_RXDB			**CAN receive input node 3**
	ASCLIN3_ARXD			**Receive input**
	P32.2	O0		**General-purpose output**
	GTM_TOUT38	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	PMS_DCDCSYNCO	O6		**DC-DC synchronization output**
	—	O7		**Reserved**

表 2-45 端口 P32 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
87	P32.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN4_5			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_5			**Mux input channel 4 of TIM module 0**
	P32.3	O0		**General-purpose output**
	GTM_TOUT39	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	ASCLIN3_ASCLK	O4		**Shift clock output**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	—	O6		**Reserved**
	—	O7		**Reserved**
88	P32.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN5_5			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_5			**Mux input channel 5 of TIM module 0**
	ASCLIN1_ACTSB			**Clear to send input**
	P32.4	O0		**General-purpose output**
	GTM_TOUT40	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	GTM_CLK1	O4		**CGM generated clock**
	—	O5		**Reserved**
	CCU_EXTCLK1	O6		**External Clock 1**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
	PMS_DCDCSYNCO	O		**DC-DC synchronization output**

表 2-46 端口 P33 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
70	P33.0	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN4_6			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_6			Mux input channel 4 of TIM module 0
	EDSADC_ITR0E			Trigger/Gate input, channel 0
	IOM_PIN_0			GPIO pad input to FPC
	GTM_DTMT1_2			CDTM1_DTM0
	P33.0	O0		General-purpose output
	GTM_TOUT22	O1		GTM muxed output
	IOM_MON0_0			Monitor input 0
	IOM_GTM_0			GTM-provided inputs to EXOR combiner
	ASCLIN5_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
71	P33.1	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN5_6			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_6			Mux input channel 5 of TIM module 0
	EDSADC_ITR1E			Trigger/Gate input, channel 1
	PSI5_RX0C			RXD inputs (receive data) channel 0
	EDSADC_DSCIN2B			Modulator clock input, channel 2
	SENT_SENT9C			Receive input channel 9
	ASCLIN8_ARXC			Receive input
	IOM_PIN_1			GPIO pad input to FPC
	P33.1	O0		General-purpose output
	GTM_TOUT23	O1		GTM muxed output
	IOM_MON0_1			Monitor input 0
	IOM_GTM_1			GTM-provided inputs to EXOR combiner
	ASCLIN3_ASLSO	O2		Slave select signal output
	QSPI2_SCLK	O3		Master SPI clock output
	EDSADC_DSCOUT2	O4		Modulator clock output
	EVADC_EMUX02	O5		Control of external analog multiplexer interface 0
	—	O6		Reserved
	—	O7		Reserved

表 2-46 端口 P33 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
72	P33.2	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN6_6			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_6			Mux input channel 6 of TIM module 0
	EDSADC_ITR2E			Trigger/Gate input, channel 2
	SENT_SENT8C			Receive input channel 8
	EDSADC_DSDIN2B			Digital datastream input, channel 2
	IOM_PIN_2			GPIO pad input to FPC
	P33.2	O0		General-purpose output
	GTM_TOUT24	O1		GTM muxed output
	IOM_MON0_2			Monitor input 0
	IOM_GTM_2			GTM-provided inputs to EXOR combiner
	ASCLIN3_ASCLK	O2		Shift clock output
	QSPI2_SLSO10	O3		Master slave select output
	PSI5_TX0	O4		TXD outputs (send data)
	IOM_MON1_14			Monitor input 1
	IOM_REF1_14			Reference input 1
	EVADC_EMUX01	O5		Control of external analog multiplexer interface 0
	—	O6		Reserved
	—	O7		Reserved
73	P33.3	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN7_6			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_6			Mux input channel 7 of TIM module 0
	PSI5_RX1C			RXD inputs (receive data) channel 1
	SENT_SENT7C			Receive input channel 7
	EDSADC_DSCIN1B			Modulator clock input, channel 1
	IOM_PIN_3			GPIO pad input to FPC
	P33.3	O0		General-purpose output
	GTM_TOUT25	O1		GTM muxed output
	IOM_MON0_3			Monitor input 0
	IOM_GTM_3			GTM-provided inputs to EXOR combiner
	ASCLIN5_ASCLK	O2		Shift clock output
	—	O3		Reserved
	EDSADC_DSCOUT1	O4		Modulator clock output
	EVADC_EMUX00	O5		Control of external analog multiplexer interface 0
	—	O6		Reserved
	—	O7		Reserved

表 2-46 端口 P33 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
74	P33.4	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN0_10			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_10			Mux input channel 0 of TIM module 0
	EDSADC_ITR0F			Trigger/Gate input, channel 0
	SENT_SENT6C			Receive input channel 6
	EDSADC_DSDIN1B			Digital datastream input, channel 1
	CCU61_CTRAPC			Trap input capture
	ASCLIN5_ARXB			Receive input
	IOM_PIN_4			GPIO pad input to FPC
	P33.4	O0		General-purpose output
	GTM_TOUT26	O1		GTM muxed output
	IOM_MON0_4			Monitor input 0
	IOM_GTM_4			GTM-provided inputs to EXOR combiner
	ASCLIN2_ARTS	O2		Ready to send output
	QSPI2_SLSO12	O3		Master slave select output
	PSI5_TX1	O4		TXD outputs (send data)
	IOM_MON1_15			Monitor input 1
	EVADC_EMUX12	O5		Control of external analog multiplexer interface 1
	EVADC_FC0BFLOUT	O6		Boundary flag output, FC channel 0
	CAN13_TXD	O7		CAN transmit output node 3

表 2-46 端口 P33 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
75	P33.5	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN1_8			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_8			Mux input channel 1 of TIM module 0
	EDSADC_DSCIN0B			Modulator clock input, channel 0
	EDSADC_ITR1F			Trigger/Gate input, channel 1
	GPT120_T4EUDB			Count direction control input of timer T4
	PSI5S_RXC			RX data input
	ASCLIN2_ACTSB			Clear to send input
	CCU61_CCPOS2C			Hall capture input 2
	SENT_SENT5C			Receive input channel 5
	CAN13_RXDB			CAN receive input node 3
	IOM_PIN_5			GPIO pad input to FPC
	P33.5	O0		General-purpose output
	GTM_TOUT27	O1		GTM muxed output
	IOM_MON0_5			Monitor input 0
	IOM_GTM_5			GTM-provided inputs to EXOR combiner
	QSPI0_SLSO7	O2		Master slave select output
	QSPI1_SLSO7	O3		Master slave select output
	EDSADC_DSCOUT0	O4		Modulator clock output
	EVADC_EMUX11	O5		Control of external analog multiplexer interface 1
	—	O6		Reserved
	ASCLIN5_ASLSO	O7		Slave select signal output

表 2-46 端口 P33 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
76	P33.6	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN2_9			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_9			Mux input channel 2 of TIM module 0
	EDSADC_ITR2F			Trigger/Gate input, channel 2
	GPT120_T2EUDB			Count direction control input of timer T2
	SENT_SENT4C			Receive input channel 4
	CCU61_CCPOS1C			Hall capture input 1
	EDSADC_DSDIN0B			Digital datastream input, channel 0
	ASCLIN8_ARXD			Receive input
	IOM_PIN_6			GPIO pad input to FPC
	P33.6	O0		General-purpose output
	GTM_TOUT28	O1		GTM muxed output
	IOM_MON0_6			Monitor input 0
	IOM_GTM_6			GTM-provided inputs to EXOR combiner
	ASCLIN2_ASLSO	O2		Slave select signal output
	QSPI2_SLSO11	O3		Master slave select output
	—	O4		Reserved
	EVADC_EMUX10	O5		Control of external analog multiplexer interface 1
	EVADC_FC1BFLOUT	O6		Boundary flag output, FC channel 1
	PSI5S_TX	O7		TX data output

表 2-46 端口 P33 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
77	P33.7	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN3_9			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_9			Mux input channel 3 of TIM module 0
	CAN00_RXDE			CAN receive input node 0
	GPT120_T2INB			Trigger/gate input of timer T2
	CCU61_CCPOS0C			Hall capture input 0
	SCU_E_REQ4_0			ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	IOM_PIN_7			GPIO pad input to FPC
	P33.7	O0		General-purpose output
	GTM_TOUT29	O1		GTM muxed output
	IOM_MON0_7			Monitor input 0
	IOM_GTM_7			GTM-provided inputs to EXOR combiner
	ASCLIN2_ASCLK	O2		Shift clock output
	—	O3		Reserved
	ASCLIN8_ATX	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-46 端口 P33 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
78	P33.8	I	FAST / HighZ / VEVRSB	**General-purpose input**
	GTM_TIM1_IN4_7			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_7			**Mux input channel 4 of TIM module 0**
	ASCLIN2_ARXE			**Receive input**
	SCU_EMGSTOP_PORT_A			**Emergency stop Port Pin A input request**
	IOM_PIN_8			**GPIO pad input to FPC**
	P33.8	O0		**General-purpose output**
	GTM_TOUT30	O1		**GTM muxed output**
	IOM_MON0_8			**Monitor input 0**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	CCU61_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_13			**Monitor input 1**
	IOM_REF1_8			**Reference input 1**
	SMU_FSP0	O		**FSP[1..0] Output Signals - Generated by SMU_core**

表 2-46 端口 P33 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
79	P33.9	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM1_IN1_9			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_9			**Mux input channel 1 of TIM module 0**
	IOM_PIN_9			**GPIO pad input to FPC**
	P33.9	O0		**General-purpose output**
	GTM_TOUT31	O1		**GTM muxed output**
	IOM_MON0_9			**Monitor input 0**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	—	O3		**Reserved**
	ASCLIN2_ASCLK	O4		**Shift clock output**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	ASCLIN0_ATX	O6		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**

表 2-46 端口 P33 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
80	P33.10	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN0_9			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_9			Mux input channel 0 of TIM module 0
	CAN01_RXDD			CAN receive input node 1
	ASCLIN0_ARXD			Receive input
	IOM_PIN_10			GPIO pad input to FPC
	P33.10	O0		General-purpose output
	GTM_TOUT32	O1		GTM muxed output
	IOM_MON0_10			Monitor input 0
	QSPI1_SLSO6	O2		Master slave select output
	—	O3		Reserved
	ASCLIN1_ASLSO	O4		Slave select signal output
	PSI5S_CLK	O5		PSI5S CLK is a clock that can be used on a pin to drive the external PHY.
	—	O6		Reserved
	CCU61_COUT61	O7		T12 PWM channel 61
	IOM_MON1_12			Monitor input 1
	IOM_REF1_9			Reference input 1
	SMU_FSP1	O		FSP[1..0] Output Signals - Generated by SMU_core
81	P33.11	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN2_8			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_8			Mux input channel 2 of TIM module 0
	IOM_PIN_11			GPIO pad input to FPC
	P33.11	O0		General-purpose output
	GTM_TOUT33	O1		GTM muxed output
	IOM_MON0_11			Monitor input 0
	ASCLIN1_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	EDSADC_CGPWMN	O6		Negative carrier generator output
	CCU61_CC61	O7		T12 PWM channel 61
	IOM_MON1_9			Monitor input 1
	IOM_REF1_12			Reference input 1

表 2-46 端口 P33 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
82	P33.12	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM2_IN0_6			Mux input channel 0 of TIM module 2
	CAN00_RXDD			CAN receive input node 0
	PMS_PINBWKP			PINB (P33.12) pin input
	IOM_PIN_12			GPIO pad input to FPC
	P33.12	O0		General-purpose output
	GTM_TOUT34	O1		GTM muxed output
	IOM_MON0_12			Monitor input 0
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	—	O3		Reserved
	ASCLIN1_ASCLK	O4		Shift clock output
	—	O5		Reserved
	EDSADC_CGPWMP	O6		Positive carrier generator output
	CCU61_COUT60	O7		T12 PWM channel 60
	IOM_MON1_11			Monitor input 1
	IOM_REF1_10			Reference input 1
83	P33.13	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM2_IN1_5			Mux input channel 1 of TIM module 2
	ASCLIN1_ARXF			Receive input
	EDSADC_SGNB			Carrier sign signal input
	P33.13	O0		General-purpose output
	GTM_TOUT35	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	—	O3		Reserved
	QSPI2_SLSO6	O4		Master slave select output
	CAN00_TXD	O5		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	—	O6		Reserved
	CCU61_CC60	O7		T12 PWM channel 60
	IOM_MON1_8			Monitor input 1
	IOM_REF1_13			Reference input 1

表 2-47 模拟输入

Pin	Symbol	Ctrl.	Buffer Type	Function
67	AN0	I	D / HighZ / VDDM	**Analog Input 0**
	EVADC_G0CH0			**Analog input channel 0, group 0**
	EDSADC_EDS3PA			**Positive analog input channel 3, pin A**
66	AN1	I	D / HighZ / VDDM	**Analog Input 1**
	EVADC_G0CH1			**Analog input channel 1, group 0**
	EDSADC_EDS3NA			**Negative analog input channel 3, pin A**
65	AN2	I	D / HighZ / VDDM	**Analog Input 2**
	EVADC_G0CH2			**Analog input channel 2, group 0**
	EDSADC_EDS0PA			**Positive analog input channel 0, pin A**
64	AN3	I	D / HighZ / VDDM	**Analog Input 3**
	EVADC_G0CH3			**Analog input channel 3, group 0**
	EDSADC_EDS0NA			**Negative analog input channel 0, pin A**
63	AN4	I	D / HighZ / VDDM	**Analog Input 4**
	EVADC_G0CH4			**Analog input channel 4, group 0**
62	AN5	I	D / HighZ / VDDM	**Analog Input 5**
	EVADC_G0CH5			**Analog input channel 5, group 0**
61	AN6	I	D / HighZ / VDDM	**Analog Input 6**
	EVADC_G0CH6			**Analog input channel 6, group 0**
60	AN7	I	D / HighZ / VDDM	**Analog Input 7**
	EVADC_G0CH7			**Analog input channel 7, group 0**
59	AN8	I	D / HighZ / VDDM	**Analog Input 8**
	EVADC_G1CH0			**Analog input channel 0, group 1**
58	AN10	I	D / HighZ / VDDM	**Analog Input 10**
	EVADC_G1CH2			**Analog input channel 2, group 1**
57	AN11	I	D / HighZ / VDDM	**Analog Input 11**
	EVADC_G1CH3			**Analog input channel 3, group 1**
56	AN12	I	D / HighZ / VDDM	**Analog Input 12**
	EVADC_G1CH4			**Analog input channel 4, group 1**
	EDSADC_EDS0PB			**Positive analog input channel 0, pin B**
55	AN13	I	D / HighZ / VDDM	**Analog Input 13**
	EVADC_G1CH5			**Analog input channel 5, group 1**
	EDSADC_EDS0NB			**Negative analog input channel 0, pin B**
50	AN16	I	D / HighZ / VDDM	**Analog Input 16**
	EVADC_G2CH0			**Analog input channel 0, group 2**
	EVADC_FC0CH0			**Analog input FC channel 0**

表 2-47 模拟输入（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
49	AN17	I	D / HighZ / VDDM	**Analog Input 17**
	EVADC_G2CH1			**Analog input channel 1, group 2**
	EVADC_FC1CH0			**Analog input FC channel 1**
48	AN18	I	D / HighZ / VDDM	**Analog Input 18**
	EVADC_G2CH2			**Analog input channel 2, group 2**
47	AN19	I	D / HighZ / VDDM	**Analog Input 19**
	EVADC_G2CH3			**Analog input channel 3, group 2**
46	AN20	I	D / HighZ / VDDM	**Analog Input 20**
	EVADC_G2CH4			**Analog input channel 4, group 2**
	EDSADC_EDS2PA			**Positive analog input channel 2, pin A**
45	AN21	I	D / HighZ / VDDM	**Analog Input 21**
	EVADC_G2CH5			**Analog input channel 5, group 2**
	EDSADC_EDS2NA			**Negative analog input channel 2, pin A**
44	AN24/P40.0	I	S / HighZ / VDDM	**Analog Input 24**
	SENT_SENT0A			**Receive input channel 0**
	EVADC_G3CH0			**Analog input channel 0, group 3**
	CCU60_CCPOS0D			**Hall capture input 0**
	EDSADC_EDS2PB			**Positive analog input channel 2, pin B**
43	AN25/P40.1	I	S / HighZ / VDDM	**Analog Input 25**
	SENT_SENT1A			**Receive input channel 1**
	EVADC_G3CH1			**Analog input channel 1, group 3**
	CCU60_CCPOS1B			**Hall capture input 1**
	EDSADC_EDS2NB			**Negative analog input channel 2, pin B**
42	AN26/P40.2	I	S / HighZ / VDDM	**Analog Input 26**
	SENT_SENT2A			**Receive input channel 2**
	EVADC_G3CH2			**Analog input channel 2, group 3**
	CCU60_CCPOS1D			**Hall capture input 1**
41	AN27/P40.3	I	S / HighZ / VDDM	**Analog Input 27**
	SENT_SENT3A			**Receive input channel 3**
	EVADC_G3CH3			**Analog input channel 3, group 3**
	CCU60_CCPOS2B			**Hall capture input 2**
40	AN28	I	D / HighZ / VDDM	**Analog Input 28**
	EVADC_G3CH4			**Analog input channel 4, group 3**
39	AN29	I	D / HighZ / VDDM	**Analog Input 29**
	EVADC_G3CH5			**Analog input channel 5, group 3**

表 2-47 模拟输入（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
38	AN32/P40.4	I	S / HighZ / VDDM	**Analog Input 32**
	SENT_SENT4A			**Receive input channel 4**
	EVADC_G8CH0			**Analog input channel 0, group 8**
	CCU60_CCPOS2D			**Hall capture input 2**
37	AN33/P40.5	I	S / HighZ / VDDM	**Analog Input 33**
	SENT_SENT5A			**Receive input channel 5**
	EVADC_G8CH1			**Analog input channel 1, group 8**
	CCU61_CCPOS0D			**Hall capture input 0**
36	AN35	I	D / HighZ / VDDM	**Analog Input 35**
	EVADC_G8CH3			**Analog input channel 3, group 8**
35	AN36/P40.6	I	S / HighZ / VDDM	**Analog Input 36**
	SENT_SENT6A			**Receive input channel 6**
	EVADC_G8CH4			**Analog input channel 4, group 8**
	CCU61_CCPOS1B			**Hall capture input 1**
	EDSADC_EDS1PA			**Positive analog input channel 1, pin A**
34	AN37/P40.7	I	S / HighZ / VDDM	**Analog Input 37**
	SENT_SENT7A			**Receive input channel 7**
	EVADC_G8CH5			**Analog input channel 5, group 8**
	CCU61_CCPOS1D			**Hall capture input 1**
	EDSADC_EDS1NA			**Negative analog input channel 1, pin A**
33	AN38/P40.8	I	S / HighZ / VDDM	**Analog Input 38**
	SENT_SENT8A			**Receive input channel 8**
	EVADC_G8CH6			**Analog input channel 6, group 8**
	CCU61_CCPOS2B			**Hall capture input 2**
	EDSADC_EDS1PB			**Positive analog input channel 1, pin B**
32	AN39/P40.9	I	S / HighZ / VDDM	**Analog Input 39**
	SENT_SENT9A			**Receive input channel 9**
	EVADC_G8CH7			**Analog input channel 7, group 8**
	CCU61_CCPOS2D			**Hall capture input 2**
	EDSADC_EDS1NB			**Negative analog input channel 1, pin B**
27	AN42	I	D / HighZ / VDDM	**Analog Input 42**
	EVADC_G8CH10			**Analog input channel 10, group 8**
26	AN43	I	D / HighZ / VDDM	**Analog Input 43**
	EVADC_G8CH11			**Analog input channel 11, group 8**
31	AN44	I	D / HighZ / VDDM	**Analog Input 44**
	EVADC_G8CH12			**Analog input channel 12, group 8**
	EDSADC_EDS1PC			**Positive analog input channel 1, pin C**

表 2-47 模拟输入（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
30	AN45	I	D / HighZ / VDDM	**Analog Input 45**
	EVADC_G8CH13			**Analog input channel 13, group 8**
	EDSADC_EDS1NC			**Negative analog input channel 1, pin C**
29	AN46	I	D / HighZ / VDDM	**Analog Input 46**
	EVADC_G8CH14			**Analog input channel 14, group 8**
	EDSADC_EDS1PD			**Positive analog input channel 1, pin D**
28	AN47	I	D / HighZ / VDDM	**Analog Input 47**
	EVADC_G8CH15			**Analog input channel 15, group 8**
	EDSADC_EDS1ND			**Negative analog input channel 1, pin D**

注释：端口引脚P32.0 和P32.1 是双向引脚，具有以下两个功能：

5. *如果将这些引脚用作标准GPIO，则可以使用P32.0 和P32.1 引脚配置表中定义的功能。*
6. *如果引脚用作外部MOSFET 的预驱动器（内部DCDC 情况），P32.0 和P32.1 将充当名为VGATE1N 和VGATE1P 的模拟IO。*

表 2-48 系统 I/O

Pin	Symbol	Ctrl.	Buffer Type	Function
84	VGATE1N	O	—	**DCDC N ch. MOSFET gate driver output** P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
85	VGATE1P	O	—	**DCDC P ch. MOSFET gate driver output** P32.1 / External Pass Device gate control for EVRC
102	XTAL1	I	XTAL / VEXT	**XTAL pad1** XTAL1. Main Oscillator/PLL/Clock Generator Input.
103	XTAL2	O	XTAL / VEXT	**XTAL pad2** XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT
112	TMS	I	FAST / PD2 / VEXT	**JTAG Module State Machine Control Input**
	DAP1	I/O		**DAP: DAP1 Data I/O**
114	$\overline{\text{TRST}}$	I	FAST / PU2 / VEXT	**JTAG Module Reset/Enable Input**
115	TCK	I	FAST / PD2 / VEXT	**JTAG Module Clock Input**
	DAP0	I		**DAP: DAP0 Clock Input**

表 2-48 系统 I/O（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
120	$\overline{\text{ESR1}}$	I/O	FAST / PU1 / VEXT	**ESR1 Port Pin input - can be used to trigger a reset or an NMI** ESR1: External System Request Reset 1. Default NMI function. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
	PMS_ESR1WKP	I		**ESR1 pin input**
121	$\overline{\text{PORST}}$	I/O	PORST / PD / VEXT	**PORST pin** Power On Reset Input. Additional strong PD in case of power fail.
122	$\overline{\text{ESR0}}$	I/O	FAST / OD / VEXT	**ESR0 Port Pin input - can be used to trigger a reset or an NMI** ESR0: External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
	PMS_ESR0WKP	I		**ESR0 pin input**

表 2-49 电源

Pin	Symbol	Ctrl.	Buffer Type	Function
54	VDDM	I	—	**ADC Analog Power Supply (5V / 3.3V)**
164	VFLEX	I	—	**Digital Power Supply for Flex Port Pads (5V / 3.3V)**
154	VDDP3	I	—	**Flash Power Supply (3.3V)**
52	VAREF1	I	—	**Positive Analog Reference Voltage 1**
69	VEVRSB	I	—	**Standby Power Supply (5V / 3.3V) for the Standby SRAM**
155	VDD	I	—	**Digital Core Power Supply (1.25V)**
10	VDD	I	—	**Digital Core Power Supply (1.25V)**
24	VDD	I	—	**Digital Core Power Supply (1.25V)**
68	VDD	I	—	**Digital Core Power Supply (1.25V)**
100	VDD	I	—	**Digital Core Power Supply (1.25V)**
123	VDD	I	—	**Digital Core Power Supply (1.25V)**
153	VEXT	I	—	**External Power Supply (5V / 3.3V)**
25	VEXT	I	—	**External Power Supply (5V / 3.3V)**
99	VEXT	I	—	**External Power Supply (5V / 3.3V)**
E-PAD	VSS	I	—	**Digital Ground (Exposed PAD), VSS**

表 2-49 电源（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
53	VSSM	I	—	**Analog Ground for VDDM**
51	VAGND1	I	—	**Negative Analog Reference Voltage 1**
101	VSS	I	—	**Oscillator Ground, VSS(OSC)**
104	VEXT	I	—	**Digital Power Supply for Oscillator (shall be supplied with same level as used for VEXT), VEXT(OSC)**

2.4 TC36x LQFP-144 封装变体引脚配置

注释：在以下QFP封装中，VFLEX 电源内部连接到VEXT 电源，因此不会在相应的封装图中或电源表中显示为专用引脚。

表 2-50 端口 P00 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
11	P00.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN0_1			**Mux input channel 0 of TIM module 2**
	CCU61_CTRAPA			**Trap input capture**
	CCU60_T12HRE			**External timer start 12**
	MSC0_INJ0			**Injection signal from port**
	GETH_MDIOA			**MDIO Input**
	P00.0	O0		**General-purpose output**
	GTM_TOUT9	O1		**GTM muxed output**
	IOM_REF0_9			**Reference input 0**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN3_ATX	O3		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O4		**Reserved**
	CAN10_TXD	O5		**CAN transmit output node 0**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
	GETH_MDIO	O		**MDIO Output**

表 2-50 端口 P00 功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
12	P00.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN1_1			**Mux input channel 1 of TIM module 2**
	CCU60_CC60INB			**T12 capture input 60**
	ASCLIN3_ARXE			**Receive input**
	CAN10_RXDA			**CAN receive input node 0**
	PSI5_RX0A			**RXD inputs (receive data) channel 0**
	CCU61_CC60INA			**T12 capture input 60**
	SENT_SENT0B			**Receive input channel 0**
	EVADC_G9CH11	AI		**Analog input channel 11, group 9**
	P00.1	O0		**General-purpose output**
	GTM_TOUT10	O1		**GTM muxed output**
	IOM_REF0_10			**Reference input 0**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	SENT_SPC0	O6		**Transmit output**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

表 2-50 端口 P00 功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
13	P00.2	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM2_IN1_2			**Mux input channel 1 of TIM module 2**
	SENT_SENT1B			**Receive input channel 1**
	EVADC_G9CH10	AI		**Analog input channel 10, group 9**
	P00.2	O0		**General-purpose output**
	GTM_TOUT11	O1		**GTM muxed output**
	IOM_REF0_11			**Reference input 0**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	PSI5_TX0	O4		**TXD outputs (send data)**
	IOM_MON1_14			**Monitor input 1**
	IOM_REF1_14			**Reference input 1**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	QSPI3_SLSO4	O6		**Master slave select output**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**

表 2-50 端口 P00 功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
14	P00.3	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM2_IN2_1			**Mux input channel 2 of TIM module 2**
	CCU60_CC61INB			**T12 capture input 61**
	EDSADC_DSCIN3A			**Modulator clock input, channel 3**
	PSI5_RX1A			**RXD inputs (receive data) channel 1**
	CAN03_RXDA			**CAN receive input node 3**
	PSI5S_RXA			**RX data input**
	SENT_SENT2B			**Receive input channel 2**
	CCU61_CC61INA			**T12 capture input 61**
	EVADC_G9CH9	AI		**Analog input channel 9, group 9**
	P00.3	O0		**General-purpose output**
	GTM_TOUT12	O1		**GTM muxed output**
	IOM_REF0_12			**Reference input 0**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	EDSADC_DSCOUT3	O4		**Modulator clock output**
	—	O5		**Reserved**
	SENT_SPC2	O6		**Transmit output**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**

表 2-50 端口 P00 功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
15	P00.4	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM2_IN3_1			**Mux input channel 3 of TIM module 2**
	SCU_E_REQ2_2			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	SENT_SENT3B			**Receive input channel 3**
	EDSADC_DSDIN3A			**Digital datastream input, channel 3**
	EDSADC_SGNA			**Carrier sign signal input**
	ASCLIN10_ARXA			**Receive input**
	EVADC_G9CH8	AI		**Analog input channel 8, group 9**
	P00.4	O0		**General-purpose output**
	GTM_TOUT13	O1		**GTM muxed output**
	IOM_REF0_13			**Reference input 0**
	PSI5S_TX	O2		**TX data output**
	CAN11_TXD	O3		**CAN transmit output node 1**
	PSI5_TX1	O4		**TXD outputs (send data)**
	IOM_MON1_15			**Monitor input 1**
	—	O5		**Reserved**
	SENT_SPC3	O6		**Transmit output**
	CCU61_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_12			**Monitor input 1**
	IOM_REF1_9			**Reference input 1**

表 2-50 端口 P00 功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
16	P00.5	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM2_IN4_1			Mux input channel 4 of TIM module 2
	CCU60_CC62INB			T12 capture input 62
	EDSADC_DSCIN2A			Modulator clock input, channel 2
	CCU61_CC62INA			T12 capture input 62
	SENT_SENT4B			Receive input channel 4
	CAN11_RXDB			CAN receive input node 1
	GTM_DTMT1_1			CDTM1_DTM0
	EVADC_G9CH7	AI		Analog input channel 7, group 9
	P00.5	O0		General-purpose output
	GTM_TOUT14	O1		GTM muxed output
	IOM_REF0_14			Reference input 0
	EDSADC_CGPWMN	O2		Negative carrier generator output
	QSPI3_SLSO3	O3		Master slave select output
	EDSADC_DSCOUT2	O4		Modulator clock output
	EVADC_FC0BFLOUT	O5		Boundary flag output, FC channel 0
	SENT_SPC4	O6		Transmit output
	CCU61_CC62	O7		T12 PWM channel 62
	IOM_MON1_10			Monitor input 1
	IOM_REF1_11			Reference input 1
17	P00.6	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM2_IN5_1			Mux input channel 5 of TIM module 2
	EDSADC_DSDIN2A			Digital datastream input, channel 2
	SENT_SENT5B			Receive input channel 5
	ASCLIN5_ARXA			Receive input
	EVADC_G9CH6	AI		Analog input channel 6, group 9
	P00.6	O0		General-purpose output
	GTM_TOUT15	O1		GTM muxed output
	IOM_REF0_15			Reference input 0
	EDSADC_CGPWMP	O2		Positive carrier generator output
	—	O3		Reserved
	—	O4		Reserved
	EVADC_EMUX10	O5		Control of external analog multiplexer interface 1
	SENT_SPC5	O6		Transmit output
	CCU61_COUT62	O7		T12 PWM channel 62
	IOM_MON1_13			Monitor input 1
	IOM_REF1_8			Reference input 1

表 2-50 端口 P00 功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
18	P00.7	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM2_IN6_1			**Mux input channel 6 of TIM module 2**
	CCU61_CC60INC			**T12 capture input 60**
	SENT_SENT6B			**Receive input channel 6**
	GPT120_T2INA			**Trigger/gate input of timer T2**
	CCU61_CCPOS0A			**Hall capture input 0**
	CCU60_T12HRB			**External timer start 12**
	GTM_DTMT0_2			**CDTM0_DTM0**
	EVADC_G9CH5	AI		**Analog input channel 5, group 9**
	P00.7	O0		**General-purpose output**
	GTM_TOUT16	O1		**GTM muxed output**
	ASCLIN5_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	EVADC_EMUX11	O5		**Control of external analog multiplexer interface 1**
	SENT_SPC6	O6		**Transmit output**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**
19	P00.8	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM2_IN7_1			**Mux input channel 7 of TIM module 2**
	CCU61_CC61INC			**T12 capture input 61**
	SENT_SENT7B			**Receive input channel 7**
	GPT120_T2EUDA			**Count direction control input of timer T2**
	CCU61_CCPOS1A			**Hall capture input 1**
	CCU60_T13HRB			**External timer start 13**
	ASCLIN10_ARXB			**Receive input**
	EVADC_G9CH4	AI		**Analog input channel 4, group 9**
	P00.8	O0		**General-purpose output**
	GTM_TOUT17	O1		**GTM muxed output**
	QSPI3_SLSO6	O2		**Master slave select output**
	ASCLIN10_ATX	O3		**Transmit output**
	—	O4		**Reserved**
	EVADC_EMUX12	O5		**Control of external analog multiplexer interface 1**
	SENT_SPC7	O6		**Transmit output**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**

表 2-50 端口 P00 功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
20	P00.9	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM1_IN0_1			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_1			**Mux input channel 0 of TIM module 0**
	CCU61_CC62INC			**T12 capture input 62**
	SENT_SENT8B			**Receive input channel 8**
	CCU61_CCPOS2A			**Hall capture input 2**
	EDSADC_DSCIN1A			**Modulator clock input, channel 1**
	EDSADC_ITR3F			**Trigger/Gate input, channel 3**
	GPT120_T4EUDA			**Count direction control input of timer T4**
	CCU60_T13HRC			**External timer start 13**
	CCU60_T12HRC			**External timer start 12**
	EVADC_G9CH3	AI		**Analog input channel 3, group 9**
	P00.9	O0		**General-purpose output**
	GTM_TOUT18	O1		**GTM muxed output**
	QSPI3_SLSO7	O2		**Master slave select output**
	ASCLIN3_ARTS	O3		**Ready to send output**
	EDSADC_DSCOUT1	O4		**Modulator clock output**
	ASCLIN4_ATX	O5		**Transmit output**
	SENT_SPC8	O6		**Transmit output**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**

表 2-50 端口 P00 功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
21	P00.12	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM1_IN3_1			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_1			**Mux input channel 3 of TIM module 0**
	ASCLIN3_ACTSA			**Clear to send input**
	EDSADC_DSDIN0A			**Digital datastream input, channel 0**
	ASCLIN4_ARXA			**Receive input**
	EVADC_G9CH0	AI		**Analog input channel 0, group 9**
	P00.12	O0		**General-purpose output**
	GTM_TOUT21	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_7			**Monitor input 1**
	IOM_REF1_7			**Reference input 1**

表 2-51 端口 P02 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
1	P02.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN0_2			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_2			**Mux input channel 0 of TIM module 0**
	CCU61_CC60INB			**T12 capture input 60**
	ASCLIN2_ARXG			**Receive input**
	CCU60_CC60INA			**T12 capture input 60**
	SCU_E_REQ3_2			**ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GTM_DTMA0_0			**CDTM0_DTM4**
	P02.0	O0		**General-purpose output**
	GTM_TOUT0	O1		**GTM muxed output**
	IOM_REF0_0			**Reference input 0**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI3_SLSO1	O3		**Master slave select output**
	EDSADC_CGPWMN	O4		**Negative carrier generator output**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	ERAY0_TXDA	O6		**Transmit Channel A**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

表 2-51 端口 P02 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
2	P02.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN1_2			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_2			**Mux input channel 1 of TIM module 0**
	ERAY0_RXDA2			**Receive Channel A2**
	ASCLIN2_ARXB			**Receive input**
	CAN00_RXDA			**CAN receive input node 0**
	SCU_E_REQ2_1			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P02.1	O0		**General-purpose output**
	GTM_TOUT1	O1		**GTM muxed output**
	IOM_REF0_1			**Reference input 0**
	—	O2		**Reserved**
	QSPI3_SLSO2	O3		**Master slave select output**
	EDSADC_CGPWMP	O4		**Positive carrier generator output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**

表 2-51 端口 P02 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
3	P02.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN2_2			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_2			**Mux input channel 2 of TIM module 0**
	CCU61_CC61INB			**T12 capture input 61**
	CCU60_CC61INA			**T12 capture input 61**
	P02.2	O0		**General-purpose output**
	GTM_TOUT2	O1		**GTM muxed output**
	IOM_REF0_2			**Reference input 0**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI3_SLSO3	O3		**Master slave select output**
	PSI5_TX0	O4		**TXD outputs (send data)**
	IOM_MON1_14			**Monitor input 1**
	IOM_REF1_14			**Reference input 1**
	CAN02_TXD	O5		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	ERAY0_TXDB	O6		**Transmit Channel B**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**

表 2-51 端口 P02 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
4	P02.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN3_2			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_2			**Mux input channel 3 of TIM module 0**
	ERAY0_RXDB2			**Receive Channel B2**
	CAN02_RXDB			**CAN receive input node 2**
	ASCLIN1_ARXG			**Receive input**
	PSI5_RX0B			**RXD inputs (receive data) channel 0**
	P02.3	O0		**General-purpose output**
	GTM_TOUT3	O1		**GTM muxed output**
	IOM_REF0_3			**Reference input 0**
	ASCLIN2_ASLSO	O2		**Slave select signal output**
	QSPI3_SLSO4	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

表 2-51 端口 P02 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
5	P02.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN4_1			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_1			**Mux input channel 4 of TIM module 0**
	CCU61_CC62INB			**T12 capture input 62**
	QSPI3_SLSIA			**Slave select input**
	CCU60_CC62INA			**T12 capture input 62**
	I2C0_SDAA			**Serial Data Input 0**
	CAN11_RXDA			**CAN receive input node 1**
	CAN0_ECTT1			**External CAN time trigger input**
	P02.4	O0		**General-purpose output**
	GTM_TOUT4	O1		**GTM muxed output**
	IOM_REF0_4			**Reference input 0**
	ASCLIN2_ASCLK	O2		**Shift clock output**
	QSPI3_SLSO0	O3		**Master slave select output**
	PSI5S_CLK	O4		**PSI5S CLK is a clock that can be used on a pin to drive the external PHY.**
	I2C0_SDA	O5		**Serial Data Output**
	ERAY0_TXENA	O6		**Transmit Enable Channel A**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

表 2-51 端口 P02 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
6	P02.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN5_1			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_1			**Mux input channel 5 of TIM module 0**
	I2C0_SCLA			**Serial Clock Input 0**
	PSI5_RX1B			**RXD inputs (receive data) channel 1**
	PSI5S_RXB			**RX data input**
	QSPI3_MRSTA			**Master SPI data input**
	SENT_SENT3C			**Receive input channel 3**
	CAN0_ECTT2			**External CAN time trigger input**
	P02.5	O0		**General-purpose output**
	GTM_TOUT5	O1		**GTM muxed output**
	IOM_REF0_5			**Reference input 0**
	CAN11_TXD	O2		**CAN transmit output node 1**
	QSPI3_MRST	O3		**Slave SPI data output**
	IOM_MON2_3			**Monitor input 2**
	IOM_REF2_3			**Reference input 2**
	—	O4		**Reserved**
	I2C0_SCL	O5		**Serial Clock Output**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**

表 2-51 端口 P02 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
7	P02.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_1			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_1			**Mux input channel 6 of TIM module 0**
	CCU60_CC60INC			**T12 capture input 60**
	SENT_SENT2C			**Receive input channel 2**
	GPT120_T3INA			**Trigger/gate input of core timer T3**
	CCU60_CCPOS0A			**Hall capture input 0**
	CCU61_T12HRB			**External timer start 12**
	QSPI3_MTSRA			**Slave SPI data input**
	P02.6	O0		**General-purpose output**
	GTM_TOUT6	O1		**GTM muxed output**
	IOM_REF0_6			**Reference input 0**
	PSI5S_TX	O2		**TX data output**
	QSPI3_MTSR	O3		**Master SPI data output**
	PSI5_TX1	O4		**TXD outputs (send data)**
	IOM_MON1_15			**Monitor input 1**
	EVADC_EMUX00	O5		**Control of external analog multiplexer interface 0**
	—	O6		**Reserved**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

表 2-51 端口 P02 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
8	P02.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN7_1			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_1			**Mux input channel 7 of TIM module 0**
	CCU60_CC61INC			**T12 capture input 61**
	SENT_SENT1C			**Receive input channel 1**
	EDSADC_DSCIN3B			**Modulator clock input, channel 3**
	GPT120_T3EUDA			**Count direction control input of core timer T3**
	CCU60_CCPOS1A			**Hall capture input 1**
	QSPI3_SCLKA			**Slave SPI clock inputs**
	CCU61_T13HRB			**External timer start 13**
	P02.7	O0		**General-purpose output**
	GTM_TOUT7	O1		**GTM muxed output**
	IOM_REF0_7			**Reference input 0**
	—	O2		**Reserved**
	QSPI3_SCLK	O3		**Master SPI clock output**
	EDSADC_DSCOUT3	O4		**Modulator clock output**
	EVADC_EMUX01	O5		**Control of external analog multiplexer interface 0**
	SENT_SPC1	O6		**Transmit output**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**

表 2-51 端口 P02 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
9	P02.8	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN0_2			**Mux input channel 0 of TIM module 2**
	CCU60_CC62INC			**T12 capture input 62**
	SENT_SENT0C			**Receive input channel 0**
	CCU60_CCPOS2A			**Hall capture input 2**
	EDSADC_DSDIN3B			**Digital datastream input, channel 3**
	EDSADC_ITR3E			**Trigger/Gate input, channel 3**
	GPT120_T4INA			**Trigger/gate input of timer T4**
	CCU61_T12HRC			**External timer start 12**
	CCU61_T13HRC			**External timer start 13**
	GTM_DTMA0_1			**CDTM0_DTM4**
	P02.8	O0		**General-purpose output**
	GTM_TOUT8	O1		**GTM muxed output**
	IOM_REF0_8			**Reference input 0**
	QSPI3_SLSO5	O2		**Master slave select output**
	ASCLIN8_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	EVADC_EMUX02	O5		**Control of external analog multiplexer interface 0**
	GETH_MDC	O6		**MDIO clock**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

表 2-52 端口 P10 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
140	P10.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_3			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_3			Mux input channel 1 of TIM module 0
	GPT120_T5EUDB			Count direction control input of timer T5
	QSPI1_MRSTA			Master SPI data input
	GTM_DTMT0_1			CDTM0_DTM0
	P10.1	O0		General-purpose output
	GTM_TOUT103	O1		GTM muxed output
	QSPI1_MTSR	O2		Master SPI data output
	QSPI1_MRST	O3		Slave SPI data output
	IOM_MON2_1			Monitor input 2
	IOM_REF2_1			Reference input 2
	MSC0_EN1	O4		Chip Select
	EVADC_FC1BFLOUT	O5		Boundary flag output, FC channel 1
	—	O6		Reserved
	—	O7		Reserved
141	P10.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_3			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_3			Mux input channel 2 of TIM module 0
	CAN02_RXDE			CAN receive input node 2
	MSC0_SDI1			Upstream assynchronous input signal
	QSPI1_SCLKA			Slave SPI clock inputs
	GPT120_T6INB			Trigger/gate input of core timer T6
	SCU_E_REQ2_0			ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P10.2	O0		General-purpose output
	GTM_TOUT104	O1		GTM muxed output
	IOM_MON2_9			Monitor input 2
	—	O2		Reserved
	QSPI1_SCLK	O3		Master SPI clock output
	MSC0_EN0	O4		Chip Select
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-52 端口 P10 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
142	P10.3	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN3_3			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_3			**Mux input channel 3 of TIM module 0**
	QSPI1_MTSRA			**Slave SPI data input**
	SCU_E_REQ3_0			**ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GPT120_T5INB			**Trigger/gate input of timer T5**
	P10.3	O0		**General-purpose output**
	GTM_TOUT105	O1		**GTM muxed output**
	IOM_MON2_10			**Monitor input 2**
	—	O2		**Reserved**
	QSPI1_MTSR	O3		**Master SPI data output**
	MSC0_EN0	O4		**Chip Select**
	—	O5		**Reserved**
	CAN02_TXD	O6		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	—	O7		**Reserved**
143	P10.5	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN2_4			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_4			**Mux input channel 2 of TIM module 0**
	PMS_HWCFG4IN			**HWCFG4 pin input**
	MSC0_INJ1			**Injection signal from port**
	P10.5	O0		**General-purpose output**
	GTM_TOUT107	O1		**GTM muxed output**
	IOM_REF2_9			**Reference input 2**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI3_SLSO8	O3		**Master slave select output**
	QSPI1_SLSO9	O4		**Master slave select output**
	GPT120_T6OUT	O5		**External output for overflow/underflow detection of core timer T6**
	ASCLIN2_ASLSO	O6		**Slave select signal output**
	—	O7		**Reserved**

表 2-52 端口 P10 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
144	P10.6	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN3_4			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_4			**Mux input channel 3 of TIM module 0**
	ASCLIN2_ARXD			**Receive input**
	QSPI3_MTSRB			**Slave SPI data input**
	PMS_HWCFG5IN			**HWCFG5 pin input**
	P10.6	O0		**General-purpose output**
	GTM_TOUT108	O1		**GTM muxed output**
	IOM_REF2_10			**Reference input 2**
	ASCLIN2_ASCLK	O2		**Shift clock output**
	QSPI3_MTSR	O3		**Master SPI data output**
	GPT120_T3OUT	O4		**External output for overflow/underflow detection of core timer T3**
	—	O5		**Reserved**
	QSPI1_MRST	O6		**Slave SPI data output**
	IOM_MON2_1			**Monitor input 2**
	IOM_REF2_1			**Reference input 2**
	—	O7		**Reserved**

表 2-53 端口 P11 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
132	P11.2	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM2_IN1_3			**Mux input channel 1 of TIM module 2**
	P11.2	O0		**General-purpose output**
	GTM_TOUT95	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SLSO5	O3		**Master slave select output**
	QSPI1_SLSO5	O4		**Master slave select output**
	MSC0_EN1	O5		**Chip Select**
	GETH_TXD1	O6		**Transmit Data**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**

表 2-53 端口 P11 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
133	P11.3	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM2_IN2_2			**Mux input channel 2 of TIM module 2**
	MSC0_SDI3			**Upstream assynchronous input signal**
	QSPI1_MRSTB			**Master SPI data input**
	P11.3	O0		**General-purpose output**
	GTM_TOUT96	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI1_MRST	O3		**Slave SPI data output**
	IOM_MON2_1			**Monitor input 2**
	IOM_REF2_1			**Reference input 2**
	ERAY0_TXDA	O4		**Transmit Channel A**
	—	O5		**Reserved**
	GETH_TXD0	O6		**Transmit Data**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**
134	P11.6	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM2_IN3_2			**Mux input channel 3 of TIM module 2**
	QSPI1_SCLKB			**Slave SPI clock inputs**
	P11.6	O0		**General-purpose output**
	GTM_TOUT97	O1		**GTM muxed output**
	ERAY0_TXENB	O2		**Transmit Enable Channel B**
	QSPI1_SCLK	O3		**Master SPI clock output**
	ERAY0_TXENA	O4		**Transmit Enable Channel A**
	MSC0_FCLP	O5		**Shift-clock direct part of the differential signal**
	GETH_TXEN	O6		**Transmit Enable MII and RMII**
	GETH_TCTL			**Transmit Control for RGMII**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

表 2-53 端口 P11 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
135	P11.9	I	FAST / RGMII_Input / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM2_IN4_2			Mux input channel 4 of TIM module 2
	QSPI1_MTSRB			Slave SPI data input
	ERAY0_RXDA1			Receive Channel A1
	GETH_RXD1A			Receive Data 1 MII, RMII and RGMII (RGMII can use RXD1A only)
	P11.9	O0		General-purpose output
	GTM_TOUT98	O1		GTM muxed output
	—	O2		Reserved
	QSPI1_MTSR	O3		Master SPI data output
	—	O4		Reserved
	MSC0_SOP	O5		Data output - direct part of the differential signal
	—	O6		Reserved
	CCU60_COUT60	O7		T12 PWM channel 60
	IOM_MON1_3			Monitor input 1
	IOM_REF1_3			Reference input 1
137	P11.10	I	FAST / RGMII_Input / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM2_IN5_2			Mux input channel 5 of TIM module 2
	GTM_TIM2_IN0_9			Mux input channel 0 of TIM module 2
	CAN03_RXDD			CAN receive input node 3
	ERAY0_RXDB1			Receive Channel B1
	ASCLIN1_ARXE			Receive input
	SCU_E_REQ6_3			ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	MSC0_SDI0			Upstream assynchronous input signal
	GETH_RXD0A			Receive Data 0 MII, RMII and RGMII (RGMII can use RXD0A only)
	QSPI1_SLSIA			Slave select input
	P11.10	O0		General-purpose output
	GTM_TOUT99	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO3	O3		Master slave select output
	QSPI1_SLSO3	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	CCU60_CC62	O7		T12 PWM channel 62
	IOM_MON1_0			Monitor input 1
	IOM_REF1_4			Reference input 1

表 2-53 端口 P11 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
138	P11.11	I	FAST / RGMII_Input / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM2_IN6_2			Mux input channel 6 of TIM module 2
	GETH_CRSDVA			Carrier Sense / Data Valid combi-signal for RMII
	GETH_RXDVA			Receive Data Valid MII
	GETH_CRSB			Carrier Sense MII
	GETH_RCTLA			Receive Control for RGMII
	P11.11	O0		General-purpose output
	GTM_TOUT100	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO4	O3		Master slave select output
	QSPI1_SLSO4	O4		Master slave select output
	MSC0_EN0	O5		Chip Select
	ERAY0_TXENB	O6		Transmit Enable Channel B
	CCU60_CC61	O7		T12 PWM channel 61
	IOM_MON1_1			Monitor input 1
	IOM_REF1_5			Reference input 1
139	P11.12	I	FAST / RGMII_Input / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM2_IN7_2			Mux input channel 7 of TIM module 2
	GETH_REFCLKA			Reference Clock input for RMII (50 MHz)
	GETH_TXCLKB			Transmit Clock Input for MII
	GETH_RXCLKA			Receive Clock MII
	P11.12	O0		General-purpose output
	GTM_TOUT101	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	GTM_CLK2	O3		CGM generated clock
	ERAY0_TXDB	O4		Transmit Channel B
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	CCU_EXTCLK1	O6		External Clock 1
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
	IOM_REF1_6			Reference input 1

表 2-54 端口 P13 的功能

Pin	Symbol	Ctrl.	Buffer Type	Function
128	P13.0	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM2_IN5_3			Mux input channel 5 of TIM module 2
	ASCLIN10_ARXC			Receive input
	P13.0	O0		General-purpose output
	GTM_TOUT91	O1		GTM muxed output
	ASCLIN10_ATX	O2		Transmit output
	QSPI2_SCLKN	O3		Master SPI clock output (LVDS N line)
	MSC0_EN1	O4		Chip Select
	MSC0_FCLN	O5		Shift-clock inverted part of the differential signal
	—	O6		Reserved
	CAN10_TXD	O7		CAN transmit output node 0
129	P13.1	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM2_IN6_3			Mux input channel 6 of TIM module 2
	I2C0_SCLB			Serial Clock Input 1
	CAN10_RXDD			CAN receive input node 0
	ASCLIN10_ARXD			Receive input
	P13.1	O0		General-purpose output
	GTM_TOUT92	O1		GTM muxed output
	—	O2		Reserved
	QSPI2_SCLKP	O3		Master SPI clock output (LVDS P line)
	—	O4		Reserved
	MSC0_FCLP	O5		Shift-clock direct part of the differential signal
	I2C0_SCL	O6		Serial Clock Output
	—	O7		Reserved
130	P13.2	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM2_IN7_3			Mux input channel 7 of TIM module 2
	GPT120_CAPINA			Trigger input to capture value of timer T5 into CAPREL register
	I2C0_SDAB			Serial Data Input 1
	P13.2	O0		General-purpose output
	GTM_TOUT93	O1		GTM muxed output
	ASCLIN10_ASCLK	O2		Shift clock output
	QSPI2_MTSRN	O3		Master SPI data output (LVDS N line)
	MSC0_FCLP	O4		Shift-clock direct part of the differential signal
	MSC0_SON	O5		Data output - inverted part of the differential signal
	I2C0_SDA	O6		Serial Data Output
	—	O7		Reserved

表 2-54 端口 P13 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
131	P13.3	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM2_IN0_3			**Mux input channel 0 of TIM module 2**
	P13.3	O0		**General-purpose output**
	GTM_TOUT94	O1		**GTM muxed output**
	ASCLIN10_ASLSO	O2		**Slave select signal output**
	QSPI2_MTSRP	O3		**Master SPI data output (LVDS P line)**
	—	O4		**Reserved**
	MSC0_SOP	O5		**Data output - direct part of the differential signal**
	—	O6		**Reserved**
	—	O7		**Reserved**

表 2-55 端口 P14 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
118	P14.0	I	FAST / PU1 / VEXT / ES2	**General-purpose input**
	GTM_TIM1_IN3_5			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_5			**Mux input channel 3 of TIM module 0**
	P14.0	O0		**General-purpose output**
	GTM_TOUT80	O1		**GTM muxed output**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	ERAY0_TXDA	O3		**Transmit Channel A**
	ERAY0_TXDB	O4		**Transmit Channel B**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	ASCLIN0_ASCLK	O6		**Shift clock output**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**

表 2-55 端口 P14 功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
119	P14.1	I	FAST / PU1 / VEXT / ES2	General-purpose input
	GTM_TIM1_IN4_3			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_3			Mux input channel 4 of TIM module 0
	ERAY0_RXDA3			Receive Channel A3
	ASCLIN0_ARXA			Receive input
	ERAY0_RXDB3			Receive Channel B3
	CAN01_RXDB			CAN receive input node 1
	SCU_E_REQ3_1			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	PMS_PINAWKP			PINA (P14.1) pin input
	P14.1	O0		General-purpose output
	GTM_TOUT81	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1
120	P14.2	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN5_3			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_3			Mux input channel 5 of TIM module 0
	PMS_HWCFG2IN			HWCFG2 pin input
	P14.2	O0		General-purpose output
	GTM_TOUT82	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI2_SLSO1	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	ASCLIN2_ASCLK	O6		Shift clock output
	—	O7		Reserved

表 2-55 端口 P14 功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
121	P14.3	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_3			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_3			**Mux input channel 6 of TIM module 0**
	PMS_HWCFG3IN			**HWCFG3 pin input**
	ASCLIN2_ARXA			**Receive input**
	MSC0_SDI2			**Upstream assynchronous input signal**
	SCU_E_REQ1_0			**ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P14.3	O0		**General-purpose output**
	GTM_TOUT83	O1		**GTM muxed output**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI2_SLSO3	O3		**Master slave select output**
	ASCLIN1_ASLSO	O4		**Slave select signal output**
	ASCLIN3_ASLSO	O5		**Slave select signal output**
	—	O6		**Reserved**
	—	O7		**Reserved**
122	P14.4	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN7_2			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_2			**Mux input channel 7 of TIM module 0**
	PMS_HWCFG6IN			**HWCFG6 pin input**
	GTM_DTMT0_0			**CDTM0_DTM0**
	P14.4	O0		**General-purpose output**
	GTM_TOUT84	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	GETH_PPS	O6		**Pulse Per Second**
	—	O7		**Reserved**

表 2-55 端口 P14 功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
123	P14.5	I	FAST / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN0_4			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_4			**Mux input channel 0 of TIM module 0**
	PMS_HWCFG1IN			**HWCFG1 pin input**
	GTM_DTMA2_0			**CDTM2_DTM4**
	P14.5	O0		**General-purpose output**
	GTM_TOUT85	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ERAY0_TXDB	O6		**Transmit Channel B**
	—	O7		**Reserved**
124	P14.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN1_4			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_4			**Mux input channel 1 of TIM module 0**
	P14.6	O0		**General-purpose output**
	GTM_TOUT86	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SLSO2	O3		**Master slave select output**
	CAN13_TXD	O4		**CAN transmit output node 3**
	—	O5		**Reserved**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	—	O7		**Reserved**

表 2-56 端口 P15 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
109	P15.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN3_4			Mux input channel 3 of TIM module 2
	P15.0	O0		General-purpose output
	GTM_TOUT71	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI0_SLSO13	O3		Master slave select output
	—	O4		Reserved
	CAN02_TXD	O5		CAN transmit output node 2
	IOM_MON2_7			Monitor input 2
	IOM_REF2_7			Reference input 2
	ASCLIN1_ASCLK	O6		Shift clock output
	—	O7		Reserved
110	P15.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN4_4			Mux input channel 4 of TIM module 2
	CAN02_RXDA			CAN receive input node 2
	ASCLIN1_ARXA			Receive input
	QSPI2_SLSIB			Slave select input
	SCU_E_REQ7_2			ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P15.1	O0		General-purpose output
	GTM_TOUT72	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI2_SLSO5	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-56 端口 P15 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
111	P15.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN5_4			**Mux input channel 5 of TIM module 2**
	QSPI2_SLSIA			**Slave select input**
	QSPI2_MRSTE			**Master SPI data input**
	P15.2	O0		**General-purpose output**
	GTM_TOUT73	O1		**GTM muxed output**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	QSPI2_SLSO0	O3		**Master slave select output**
	—	O4		**Reserved**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	ASCLIN0_ASCLK	O6		**Shift clock output**
	—	O7		**Reserved**
112	P15.3	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN6_4			**Mux input channel 6 of TIM module 2**
	CAN01_RXDA			**CAN receive input node 1**
	ASCLIN0_ARXB			**Receive input**
	QSPI2_SCLKA			**Slave SPI clock inputs**
	P15.3	O0		**General-purpose output**
	GTM_TOUT74	O1		**GTM muxed output**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	QSPI2_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	MSC0_EN1	O5		**Chip Select**
	—	O6		**Reserved**
	—	O7		**Reserved**

表 2-56 端口 P15 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
113	P15.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN7_4			**Mux input channel 7 of TIM module 2**
	I2C0_SCLC			**Serial Clock Input 2**
	QSPI2_MRSTA			**Master SPI data input**
	SCU_E_REQ0_0			**ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.4	O0		**General-purpose output**
	GTM_TOUT75	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI2_MRST	O3		**Slave SPI data output**
	IOM_MON2_2			**Monitor input 2**
	IOM_REF2_2			**Reference input 2**
	—	O4		**Reserved**
	—	O5		**Reserved**
	I2C0_SCL	O6		**Serial Clock Output**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

表 2-56 端口 P15 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
114	P15.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN0_4			**Mux input channel 0 of TIM module 2**
	ASCLIN1_ARXB			**Receive input**
	I2C0_SDAC			**Serial Data Input 2**
	QSPI2_MTSRA			**Slave SPI data input**
	SCU_E_REQ4_3			**ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.5	O0		**General-purpose output**
	GTM_TOUT76	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI2_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	MSC0_EN0	O5		**Chip Select**
	I2C0_SDA	O6		**Serial Data Output**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**
115	P15.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN2_14			**Mux input channel 2 of TIM module 2**
	GTM_TIM1_IN0_6			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_6			**Mux input channel 0 of TIM module 0**
	QSPI2_MTSRB			**Slave SPI data input**
	P15.6	O0		**General-purpose output**
	GTM_TOUT77	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	QSPI2_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	QSPI2_SCLK	O5		**Master SPI clock output**
	ASCLIN3_ASCLK	O6		**Shift clock output**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

表 2-56 端口 P15 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
116	P15.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN1_5			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_5			**Mux input channel 1 of TIM module 0**
	ASCLIN3_ARXA			**Receive input**
	QSPI2_MRSTB			**Master SPI data input**
	P15.7	O0		**General-purpose output**
	GTM_TOUT78	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	QSPI2_MRST	O3		**Slave SPI data output**
	IOM_MON2_2			**Monitor input 2**
	IOM_REF2_2			**Reference input 2**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**
117	P15.8	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN2_5			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_5			**Mux input channel 2 of TIM module 0**
	QSPI2_SCLKB			**Slave SPI clock inputs**
	SCU_E_REQ5_0			**ERU Channel 5 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.8	O0		**General-purpose output**
	GTM_TOUT79	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ASCLIN3_ASCLK	O6		**Shift clock output**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

表 2-57 端口 P20 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
93	P20.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_7			**Mux input channel 6 of TIM module 1**
	GTM_TIM1_IN4_9			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN6_7			**Mux input channel 6 of TIM module 0**
	CAN03_RXDC			**CAN receive input node 3**
	CCU_PAD_SYSCLK			**Sysclk input**
	CBS_TGI0			**Trigger input**
	SCU_E_REQ6_0			**ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GPT120_T6EUDA			**Count direction control input of core timer T6**
	P20.0	O0		**General-purpose output**
	GTM_TOUT59	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	ASCLIN3_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	HSCT0_SYSCLK_OUT	O5		**sys clock output**
	—	O6		**Reserved**
	—	O7		**Reserved**
	CBS_TGO0	O		**Trigger output**
94	P20.2	I	S / PU / VEXT	**General-purpose input** This pin is latched at power on reset release to enter test mode.
	$\overline{\text{TESTMODE}}$			**Testmode Enable Input**

表 2-57 端口 P20 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
95	P20.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN4_5			**Mux input channel 4 of TIM module 2**
	ASCLIN3_ARXC			**Receive input**
	GPT120_T6INA			**Trigger/gate input of core timer T6**
	P20.3	O0		**General-purpose output**
	GTM_TOUT61	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	QSPI0_SLSO9	O3		**Master slave select output**
	QSPI2_SLSO9	O4		**Master slave select output**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	—	O6		**Reserved**
	—	O7		**Reserved**
100	P20.6	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN6_5			**Mux input channel 6 of TIM module 2**
	CAN12_RXDA			**CAN receive input node 2**
	ASCLIN9_ARXE			**Receive input**
	P20.6	O0		**General-purpose output**
	GTM_TOUT62	O1		**GTM muxed output**
	ASCLIN1_ARTS	O2		**Ready to send output**
	QSPI0_SLSO8	O3		**Master slave select output**
	QSPI2_SLSO8	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

表 2-57 端口 P20 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
101	P20.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN7_5			**Mux input channel 7 of TIM module 2**
	GTM_TIM1_IN5_8			**Mux input channel 5 of TIM module 1**
	CAN00_RXDB			**CAN receive input node 0**
	ASCLIN1_ACTSA			**Clear to send input**
	ASCLIN9_ARXF			**Receive input**
	P20.7	O0		**General-purpose output**
	GTM_TOUT63	O1		**GTM muxed output**
	ASCLIN9_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN12_TXD	O5		**CAN transmit output node 2**
	—	O6		**Reserved**
	CCU61_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_7			**Monitor input 1**
	IOM_REF1_7			**Reference input 1**
102	P20.8	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN7_3			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_3			**Mux input channel 7 of TIM module 0**
	P20.8	O0		**General-purpose output**
	GTM_TOUT64	O1		**GTM muxed output**
	ASCLIN1_ASLSO	O2		**Slave select signal output**
	QSPI0_SLSO0	O3		**Master slave select output**
	QSPI1_SLSO0	O4		**Master slave select output**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

表 2-57 端口 P20 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
103	P20.9	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN5_5			**Mux input channel 5 of TIM module 2**
	CAN03_RXDE			**CAN receive input node 3**
	ASCLIN1_ARXC			**Receive input**
	QSPI0_SLSIB			**Slave select input**
	SCU_E_REQ7_0			**ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P20.9	O0		**General-purpose output**
	GTM_TOUT65	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SLSO1	O3		**Master slave select output**
	QSPI1_SLSO1	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**
104	P20.10	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN6_6			**Mux input channel 6 of TIM module 2**
	P20.10	O0		**General-purpose output**
	GTM_TOUT66	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI0_SLSO6	O3		**Master slave select output**
	QSPI2_SLSO7	O4		**Master slave select output**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	ASCLIN1_ASCLK	O6		**Shift clock output**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**

表 2-57 端口 P20 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
105	P20.11	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN7_6			**Mux input channel 7 of TIM module 2**
	QSPI0_SCLKA			**Slave SPI clock inputs**
	P20.11	O0		**General-purpose output**
	GTM_TOUT67	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**
106	P20.12	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN0_5			**Mux input channel 0 of TIM module 2**
	QSPI0_MRSTA			**Master SPI data input**
	IOM_PIN_13			**GPIO pad input to FPC**
	P20.12	O0		**General-purpose output**
	GTM_TOUT68	O1		**GTM muxed output**
	IOM_MON0_13			**Monitor input 0**
	—	O2		**Reserved**
	QSPI0_MRST	O3		**Slave SPI data output**
	IOM_MON2_0			**Monitor input 2**
	IOM_REF2_0			**Reference input 2**
	QSPI0_MTSR	O4		**Master SPI data output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_12			**Monitor input 1**
	IOM_REF1_9			**Reference input 1**

表 2-57 端口 P20 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
107	P20.13	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN1_4			**Mux input channel 1 of TIM module 2**
	QSPI0_SLSIA			**Slave select input**
	IOM_PIN_14			**GPIO pad input to FPC**
	P20.13	O0		**General-purpose output**
	GTM_TOUT69	O1		**GTM muxed output**
	IOM_MON0_14			**Monitor input 0**
	—	O2		**Reserved**
	QSPI0_SLSO2	O3		**Master slave select output**
	QSPI1_SLSO2	O4		**Master slave select output**
	QSPI0_SCLK	O5		**Master SPI clock output**
	—	O6		**Reserved**
	CCU61_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_13			**Monitor input 1**
	IOM_REF1_8			**Reference input 1**
108	P20.14	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN2_4			**Mux input channel 2 of TIM module 2**
	QSPI0_MTSRA			**Slave SPI data input**
	IOM_PIN_15			**GPIO pad input to FPC**
	DMU_FDEST			**Enter destructive debug mode**
	P20.14	O0		**General-purpose output**
	GTM_TOUT70	O1		**GTM muxed output**
	IOM_MON0_15			**Monitor input 0**
	—	O2		**Reserved**
	QSPI0_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

表 2-28 端口 P21 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
84	P21.2	I	LVDS_RX / FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_7			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_7			Mux input channel 0 of TIM module 0
	QSPI2_MRSTCN			Master SPI data input (LVDS N line)
	SCU_EMGSTOP_PORT_B			Emergency stop Port Pin B input request
	ASCLIN3_ARXGN			Differential Receive input (low active)
	HSCT0_RXDN			Rx data
	ASCLIN11_ARXE			Receive input
	GTM_DTMA1_0			CDTM1_DTM4
	P21.2	O0		General-purpose output
	GTM_TOUT53	O1		GTM muxed output
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	GETH_MDC	O5		MDIO clock
	—	O6		Reserved
	—	O7		Reserved
85	P21.3	I	LVDS_RX / FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_6			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_6			Mux input channel 1 of TIM module 0
	QSPI2_MRSTCP			Master SPI data input (LVDS P line)
	ASCLIN3_ARXGP			Differential Receive input (high active)
	GETH_MDIOD			MDIO Input
	HSCT0_RXDP			Rx data
	P21.3	O0		General-purpose output
	GTM_TOUT54	O1		GTM muxed output
	ASCLIN11_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	GETH_MDIO	O		MDIO Output

表 2-58 端口 P21 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
86	P21.4	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM1_IN2_6			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_6			**Mux input channel 2 of TIM module 0**
	P21.4	O0		**General-purpose output**
	GTM_TOUT55	O1		**GTM muxed output**
	ASCLIN11_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSCT0_TXDN	O		**Tx data**
87	P21.5	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM1_IN3_6			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_6			**Mux input channel 3 of TIM module 0**
	ASCLIN11_ARXF			**Receive input**
	P21.5	O0		**General-purpose output**
	GTM_TOUT56	O1		**GTM muxed output**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN11_ATX	O3		**Transmit output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSCT0_TXDP	O		**Tx data**

表 2-58 端口 P21 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
88	P21.6/TDI	I	FAST / PD / PU2 / VEXT / ES3	**General-purpose input** PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ.
	GTM_TIM1_IN4_8			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_8			**Mux input channel 4 of TIM module 0**
	GPT120_T5EUDA			**Count direction control input of timer T5**
	ASCLIN3_ARXF			**Receive input**
	CBS_TGI2			**Trigger input**
	TDI			**JTAG Module Data Input**
	P21.6	O0		**General-purpose output**
	GTM_TOUT57	O1		**GTM muxed output**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	GPT120_T3OUT	O7		**External output for overflow/underflow detection of core timer T3**
	CBS_TGO2	O		**Trigger output**
	DAP3	I/O		**DAP: DAP3 Data I/O**

表 2-58 端口 P21 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
90	P21.7/TDO	I	FAST / PU2 / VEXT / ES4	**General-purpose input**
	GTM_TIM1_IN5_7			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_7			**Mux input channel 5 of TIM module 0**
	GPT120_T5INA			**Trigger/gate input of timer T5**
	CBS_TGI3			**Trigger input**
	GETH_RXERB			**Receive Error MII**
	P21.7	O0		**General-purpose output**
	GTM_TOUT58	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	ASCLIN3_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	GPT120_T6OUT	O7		**External output for overflow/underflow detection of core timer T6**
	CBS_TGO3	O		**Trigger output**
	DAP2	I/O		**DAP: DAP2 Data I/O**
	TDO	O		**JTAG Module Data Output**

表 2-59 端口 P22 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
74	P22.0	I	FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN1_7			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_7			Mux input channel 1 of TIM module 0
	ASCLIN6_ARXE			Receive input
	QSPI3_MTSRD			Slave SPI data input
	P22.0	O0		General-purpose output
	GTM_TOUT47	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	QSPI3_MTSR	O3		Master SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	ASCLIN6_ATX	O7		Transmit output
75	P22.1	I	FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN0_8			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_8			Mux input channel 0 of TIM module 0
	ASCLIN7_ARXE			Receive input
	QSPI3_MRSTD			Master SPI data input
	P22.1	O0		General-purpose output
	GTM_TOUT48	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	QSPI3_MRST	O3		Slave SPI data output
	IOM_MON2_3			Monitor input 2
	IOM_REF2_3			Reference input 2
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	ASCLIN7_ATX	O7		Transmit output

表 2-59端口 P22 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
76	P22.2	I	FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM1_IN3_7			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_7			**Mux input channel 3 of TIM module 0**
	P22.2	O0		**General-purpose output**
	GTM_TOUT49	O1		**GTM muxed output**
	ASCLIN5_ATX	O2		**Transmit output**
	QSPI3_SLSO12	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
77	P22.3	I	FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM1_IN4_4			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_4			**Mux input channel 4 of TIM module 0**
	ASCLIN5_ARXC			**Receive input**
	QSPI3_SCLKD			**Slave SPI clock inputs**
	P22.3	O0		**General-purpose output**
	GTM_TOUT50	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI3_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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表 2-60 端口 P23 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
73	P23.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_4			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_4			**Mux input channel 6 of TIM module 0**
	ASCLIN6_ARXF			**Receive input**
	P23.1	O0		**General-purpose output**
	GTM_TOUT42	O1		**GTM muxed output**
	ASCLIN1_ARTS	O2		**Ready to send output**
	—	O3		**Reserved**
	GTM_CLK0	O4		**CGM generated clock**
	CAN10_TXD	O5		**CAN transmit output node 0**
	CCU_EXTCLK0	O6		**External Clock 0**
	ASCLIN6_ASCLK	O7		**Shift clock output**

表 2-61 端口 P32 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
70	P32.0	I	SLOW / PU1 / VEXT / ES	**General-purpose input** P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
	GTM_TIM2_IN2_5			**Mux input channel 2 of TIM module 2**
	P32.0	O0		**General-purpose output**
	GTM_TOUT36	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
71	P32.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input** P32.1 / External Pass Device gate control for EVRC
	P32.1	O0		**General-purpose output**
	GTM_TOUT37	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

表 2-61 端口 P32 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
72	P32.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN5_5			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_5			**Mux input channel 5 of TIM module 0**
	ASCLIN1_ACTSB			**Clear to send input**
	P32.4	O0		**General-purpose output**
	GTM_TOUT40	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	GTM_CLK1	O4		**CGM generated clock**
	—	O5		**Reserved**
	CCU_EXTCLK1	O6		**External Clock 1**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
	PMS_DCDCSYNCO	O		**DC-DC synchronization output**

表 2-62 端口 P33 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
60	P33.4	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN0_10			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_10			Mux input channel 0 of TIM module 0
	EDSADC_ITR0F			Trigger/Gate input, channel 0
	SENT_SENT6C			Receive input channel 6
	EDSADC_DSDIN1B			Digital datastream input, channel 1
	CCU61_CTRAPC			Trap input capture
	ASCLIN5_ARXB			Receive input
	IOM_PIN_4			GPIO pad input to FPC
	P33.4	O0		General-purpose output
	GTM_TOUT26	O1		GTM muxed output
	IOM_MON0_4			Monitor input 0
	IOM_GTM_4			GTM-provided inputs to EXOR combiner
	ASCLIN2_ARTS	O2		Ready to send output
	QSPI2_SLSO12	O3		Master slave select output
	PSI5_TX1	O4		TXD outputs (send data)
	IOM_MON1_15			Monitor input 1
	EVADC_EMUX12	O5		Control of external analog multiplexer interface 1
	EVADC_FC0BFLOUT	O6		Boundary flag output, FC channel 0
	CAN13_TXD	O7		CAN transmit output node 3

表 2-62 端口 P33 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
61	P33.5	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN1_8			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_8			Mux input channel 1 of TIM module 0
	EDSADC_DSCIN0B			Modulator clock input, channel 0
	EDSADC_ITR1F			Trigger/Gate input, channel 1
	GPT120_T4EUDB			Count direction control input of timer T4
	PSI5S_RXC			RX data input
	ASCLIN2_ACTSB			Clear to send input
	CCU61_CCPOS2C			Hall capture input 2
	SENT_SENT5C			Receive input channel 5
	CAN13_RXDB			CAN receive input node 3
	IOM_PIN_5			GPIO pad input to FPC
	P33.5	O0		General-purpose output
	GTM_TOUT27	O1		GTM muxed output
	IOM_MON0_5			Monitor input 0
	IOM_GTM_5			GTM-provided inputs to EXOR combiner
	QSPI0_SLSO7	O2		Master slave select output
	QSPI1_SLSO7	O3		Master slave select output
	EDSADC_DSCOUT0	O4		Modulator clock output
	EVADC_EMUX11	O5		Control of external analog multiplexer interface 1
	—	O6		Reserved
	ASCLIN5_ASLSO	O7		Slave select signal output

表 2-62 端口 P33 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
62	P33.6	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN2_9			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_9			Mux input channel 2 of TIM module 0
	EDSADC_ITR2F			Trigger/Gate input, channel 2
	GPT120_T2EUDB			Count direction control input of timer T2
	SENT_SENT4C			Receive input channel 4
	CCU61_CCPOS1C			Hall capture input 1
	EDSADC_DSDIN0B			Digital datastream input, channel 0
	ASCLIN8_ARXD			Receive input
	IOM_PIN_6			GPIO pad input to FPC
	P33.6	O0		General-purpose output
	GTM_TOUT28	O1		GTM muxed output
	IOM_MON0_6			Monitor input 0
	IOM_GTM_6			GTM-provided inputs to EXOR combiner
	ASCLIN2_ASLSO	O2		Slave select signal output
	QSPI2_SLSO11	O3		Master slave select output
	—	O4		Reserved
	EVADC_EMUX10	O5		Control of external analog multiplexer interface 1
	EVADC_FC1BFLOUT	O6		Boundary flag output, FC channel 1
	PSI5S_TX	O7		TX data output

表 2-62 端口 P33 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
63	P33.7	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN3_9			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_9			Mux input channel 3 of TIM module 0
	CAN00_RXDE			CAN receive input node 0
	GPT120_T2INB			Trigger/gate input of timer T2
	CCU61_CCPOS0C			Hall capture input 0
	SCU_E_REQ4_0			ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	IOM_PIN_7			GPIO pad input to FPC
	P33.7	O0		General-purpose output
	GTM_TOUT29	O1		GTM muxed output
	IOM_MON0_7			Monitor input 0
	IOM_GTM_7			GTM-provided inputs to EXOR combiner
	ASCLIN2_ASCLK	O2		Shift clock output
	—	O3		Reserved
	ASCLIN8_ATX	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-62 端口 P33 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
64	P33.8	I	FAST / HighZ / VEVRSB	**General-purpose input**
	GTM_TIM1_IN4_7			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_7			**Mux input channel 4 of TIM module 0**
	ASCLIN2_ARXE			**Receive input**
	SCU_EMGSTOP_PORT_A			**Emergency stop Port Pin A input request**
	IOM_PIN_8			**GPIO pad input to FPC**
	P33.8	O0		**General-purpose output**
	GTM_TOUT30	O1		**GTM muxed output**
	IOM_MON0_8			**Monitor input 0**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	CCU61_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_13			**Monitor input 1**
	IOM_REF1_8			**Reference input 1**
	SMU_FSP0	O		**FSP[1..0] Output Signals - Generated by SMU_core**

表 2-62 端口 P33 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
65	P33.9	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM1_IN1_9			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_9			**Mux input channel 1 of TIM module 0**
	IOM_PIN_9			**GPIO pad input to FPC**
	P33.9	O0		**General-purpose output**
	GTM_TOUT31	O1		**GTM muxed output**
	IOM_MON0_9			**Monitor input 0**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	—	O3		**Reserved**
	ASCLIN2_ASCLK	O4		**Shift clock output**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	ASCLIN0_ATX	O6		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**

表 2-62 端口 P33 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
66	P33.10	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN0_9			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_9			Mux input channel 0 of TIM module 0
	CAN01_RXDD			CAN receive input node 1
	ASCLIN0_ARXD			Receive input
	IOM_PIN_10			GPIO pad input to FPC
	P33.10	O0		General-purpose output
	GTM_TOUT32	O1		GTM muxed output
	IOM_MON0_10			Monitor input 0
	QSPI1_SLSO6	O2		Master slave select output
	—	O3		Reserved
	ASCLIN1_ASLSO	O4		Slave select signal output
	PSI5S_CLK	O5		PSI5S CLK is a clock that can be used on a pin to drive the external PHY.
	—	O6		Reserved
	CCU61_COUT61	O7		T12 PWM channel 61
	IOM_MON1_12			Monitor input 1
	IOM_REF1_9			Reference input 1
	SMU_FSP1	O		FSP[1..0] Output Signals - Generated by SMU_core
67	P33.11	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN2_8			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_8			Mux input channel 2 of TIM module 0
	IOM_PIN_11			GPIO pad input to FPC
	P33.11	O0		General-purpose output
	GTM_TOUT33	O1		GTM muxed output
	IOM_MON0_11			Monitor input 0
	ASCLIN1_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	EDSADC_CGPWMN	O6		Negative carrier generator output
	CCU61_CC61	O7		T12 PWM channel 61
	IOM_MON1_9			Monitor input 1
	IOM_REF1_12			Reference input 1

表 2-62 端口 P33 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
68	P33.12	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM2_IN0_6			Mux input channel 0 of TIM module 2
	CAN00_RXDD			CAN receive input node 0
	PMS_PINBWKP			PINB (P33.12) pin input
	IOM_PIN_12			GPIO pad input to FPC
	P33.12	O0		General-purpose output
	GTM_TOUT34	O1		GTM muxed output
	IOM_MON0_12			Monitor input 0
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	—	O3		Reserved
	ASCLIN1_ASCLK	O4		Shift clock output
	—	O5		Reserved
	EDSADC_CGPWMP	O6		Positive carrier generator output
	CCU61_COUT60	O7		T12 PWM channel 60
	IOM_MON1_11			Monitor input 1
	IOM_REF1_10			Reference input 1
69	P33.13	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM2_IN1_5			Mux input channel 1 of TIM module 2
	ASCLIN1_ARXF			Receive input
	EDSADC_SGNB			Carrier sign signal input
	P33.13	O0		General-purpose output
	GTM_TOUT35	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	—	O3		Reserved
	QSPI2_SLSO6	O4		Master slave select output
	CAN00_TXD	O5		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	—	O6		Reserved
	CCU61_CC60	O7		T12 PWM channel 60
	IOM_MON1_8			Monitor input 1
	IOM_REF1_13			Reference input 1

表 2-63 模拟输入

Pin	Symbol	Ctrl.	Buffer Type	Function
57	AN0	I	D / HighZ / VDDM	**Analog Input 0**
	EVADC_G0CH0			**Analog input channel 0, group 0**
	EDSADC_EDS3PA			**Positive analog input channel 3, pin A**
56	AN1	I	D / HighZ / VDDM	**Analog Input 1**
	EVADC_G0CH1			**Analog input channel 1, group 0**
	EDSADC_EDS3NA			**Negative analog input channel 3, pin A**
55	AN2	I	D / HighZ / VDDM	**Analog Input 2**
	EVADC_G0CH2			**Analog input channel 2, group 0**
	EDSADC_EDS0PA			**Positive analog input channel 0, pin A**
54	AN3	I	D / HighZ / VDDM	**Analog Input 3**
	EVADC_G0CH3			**Analog input channel 3, group 0**
	EDSADC_EDS0NA			**Negative analog input channel 0, pin A**
53	AN4	I	D / HighZ / VDDM	**Analog Input 4**
	EVADC_G0CH4			**Analog input channel 4, group 0**
52	AN5	I	D / HighZ / VDDM	**Analog Input 5**
	EVADC_G0CH5			**Analog input channel 5, group 0**
51	AN6	I	D / HighZ / VDDM	**Analog Input 6**
	EVADC_G0CH6			**Analog input channel 6, group 0**
50	AN7	I	D / HighZ / VDDM	**Analog Input 7**
	EVADC_G0CH7			**Analog input channel 7, group 0**
49	AN8	I	D / HighZ / VDDM	**Analog Input 8**
	EVADC_G1CH0			**Analog input channel 0, group 1**
48	AN10	I	D / HighZ / VDDM	**Analog Input 10**
	EVADC_G1CH2			**Analog input channel 2, group 1**
47	AN11	I	D / HighZ / VDDM	**Analog Input 11**
	EVADC_G1CH3			**Analog input channel 3, group 1**
46	AN12	I	D / HighZ / VDDM	**Analog Input 12**
	EVADC_G1CH4			**Analog input channel 4, group 1**
	EDSADC_EDS0PB			**Positive analog input channel 0, pin B**
45	AN13	I	D / HighZ / VDDM	**Analog Input 13**
	EVADC_G1CH5			**Analog input channel 5, group 1**
	EDSADC_EDS0NB			**Negative analog input channel 0, pin B**
40	AN16	I	D / HighZ / VDDM	**Analog Input 16**
	EVADC_G2CH0			**Analog input channel 0, group 2**
	EVADC_FC0CH0			**Analog input FC channel 0**

表 2-63 模拟输入（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
39	AN17	I	D / HighZ / VDDM	**Analog Input 17**
	EVADC_G2CH1			**Analog input channel 1, group 2**
	EVADC_FC1CH0			**Analog input FC channel 1**
38	AN20	I	D / HighZ / VDDM	**Analog Input 20**
	EVADC_G2CH4			**Analog input channel 4, group 2**
	EDSADC_EDS2PA			**Positive analog input channel 2, pin A**
37	AN21	I	D / HighZ / VDDM	**Analog Input 21**
	EVADC_G2CH5			**Analog input channel 5, group 2**
	EDSADC_EDS2NA			**Negative analog input channel 2, pin A**
36	AN24/P40.0	I	S / HighZ / VDDM	**Analog Input 24**
	SENT_SENT0A			**Receive input channel 0**
	EVADC_G3CH0			**Analog input channel 0, group 3**
	CCU60_CCPOS0D			**Hall capture input 0**
	EDSADC_EDS2PB			**Positive analog input channel 2, pin B**
35	AN25/P40.1	I	S / HighZ / VDDM	**Analog Input 25**
	SENT_SENT1A			**Receive input channel 1**
	EVADC_G3CH1			**Analog input channel 1, group 3**
	CCU60_CCPOS1B			**Hall capture input 1**
	EDSADC_EDS2NB			**Negative analog input channel 2, pin B**
34	AN35	I	D / HighZ / VDDM	**Analog Input 35**
	EVADC_G8CH3			**Analog input channel 3, group 8**
33	AN36/P40.6	I	S / HighZ / VDDM	**Analog Input 36**
	SENT_SENT6A			**Receive input channel 6**
	EVADC_G8CH4			**Analog input channel 4, group 8**
	CCU61_CCPOS1B			**Hall capture input 1**
	EDSADC_EDS1PA			**Positive analog input channel 1, pin A**
32	AN37/P40.7	I	S / HighZ / VDDM	**Analog Input 37**
	SENT_SENT7A			**Receive input channel 7**
	EVADC_G8CH5			**Analog input channel 5, group 8**
	CCU61_CCPOS1D			**Hall capture input 1**
	EDSADC_EDS1NA			**Negative analog input channel 1, pin A**
31	AN38/P40.8	I	S / HighZ / VDDM	**Analog Input 38**
	SENT_SENT8A			**Receive input channel 8**
	EVADC_G8CH6			**Analog input channel 6, group 8**
	CCU61_CCPOS2B			**Hall capture input 2**
	EDSADC_EDS1PB			**Positive analog input channel 1, pin B**

表 2-63 模拟输入（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
30	AN39/P40.9	I	S / HighZ / VDDM	**Analog Input 39**
	SENT_SENT9A			**Receive input channel 9**
	EVADC_G8CH7			**Analog input channel 7, group 8**
	CCU61_CCPOS2D			**Hall capture input 2**
	EDSADC_EDS1NB			**Negative analog input channel 1, pin B**
25	AN42	I	D / HighZ / VDDM	**Analog Input 42**
	EVADC_G8CH10			**Analog input channel 10, group 8**
24	AN43	I	D / HighZ / VDDM	**Analog Input 43**
	EVADC_G8CH11			**Analog input channel 11, group 8**
29	AN44	I	D / HighZ / VDDM	**Analog Input 44**
	EVADC_G8CH12			**Analog input channel 12, group 8**
	EDSADC_EDS1PC			**Positive analog input channel 1, pin C**
28	AN45	I	D / HighZ / VDDM	**Analog Input 45**
	EVADC_G8CH13			**Analog input channel 13, group 8**
	EDSADC_EDS1NC			**Negative analog input channel 1, pin C**
27	AN46	I	D / HighZ / VDDM	**Analog Input 46**
	EVADC_G8CH14			**Analog input channel 14, group 8**
	EDSADC_EDS1PD			**Positive analog input channel 1, pin D**
26	AN47	I	D / HighZ / VDDM	**Analog Input 47**
	EVADC_G8CH15			**Analog input channel 15, group 8**
	EDSADC_EDS1ND			**Negative analog input channel 1, pin D**

注释：端口引脚P32.0 和P32.1 是双向引脚，具有以下两个功能：

7. *如果将这些引脚用作标准GPIO，则可以使用P32.0 和P32.1 引脚配置表中定义的功能。*
8. *如果引脚用作外部MOSFET 的预驱动器（内部DCDC 情况），P32.0 和P32.1 将充当名为VGATE1N 和VGATE1P 的模拟IO。*

表 2-64 系统 I/O

Pin	Symbol	Ctrl.	Buffer Type	Function
70	VGATE1N	O	—	**DCDC N ch. MOSFET gate driver output** P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
71	VGATE1P	O	—	**DCDC P ch. MOSFET gate driver output** P32.1 / External Pass Device gate control for EVRC
81	XTAL1	I	XTAL / VEXT	**XTAL pad1** XTAL1. Main Oscillator/PLL/Clock Generator Input.

TC36x 引脚定义和功能：LQFP-144 封装变体引脚

表 2-64 系统 I/O（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
82	XTAL2	O	XTAL / VEXT	**XTAL pad2** XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT
89	TMS	I	FAST / PD2 / VEXT	**JTAG Module State Machine Control Input**
	DAP1	I/O		**DAP: DAP1 Data I/O**
91	$\overline{\text{TRST}}$	I	FAST / PU2 / VEXT	**JTAG Module Reset/Enable Input**
92	TCK	I	FAST / PD2 / VEXT	**JTAG Module Clock Input**
	DAP0	I		**DAP: DAP0 Clock Input**
96	$\overline{\text{ESR1}}$	I/O	FAST / PU1 / VEXT	**ESR1 Port Pin input - can be used to trigger a reset or an NMI** ESR1: External System Request Reset 1. Default NMI function. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
	PMS_ESR1WKP	I		**ESR1 pin input**
97	$\overline{\text{PORST}}$	I/O	PORST / PD / VEXT	**PORST pin** Power On Reset Input. Additional strong PD in case of power fail.
98	$\overline{\text{ESR0}}$	I/O	FAST / OD / VEXT	**ESR0 Port Pin input - can be used to trigger a reset or an NMI** ESR0: External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
	PMS_ESR0WKP	I		**ESR0 pin input**

表 2-65 电源

Pin	Symbol	Ctrl.	Buffer Type	Function
44	VDDM	I	—	**ADC Analog Power Supply (5V / 3.3V)**
136	VFLEX	I	—	**Digital Power Supply for Flex Port Pads (5V / 3.3V)**
126	VDDP3	I	—	**Flash Power Supply (3.3V)**
42	VAREF1	I	—	**Positive Analog Reference Voltage 1**
59	VEVRSB	I	—	**Standby Power Supply (5V / 3.3V) for the Standby SRAM**

表 2-65 电源（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
10	VDD	I	—	**Digital Core Power Supply (1.25V)**
125	VEXT	I	—	**External Power Supply (5V / 3.3V)**
23	VEXT	I	—	**External Power Supply (5V / 3.3V)**
78	VEXT	I	—	**External Power Supply (5V / 3.3V)**
127	VDD	I	—	**Digital Core Power Supply (1.25V)**
22	VDD	I	—	**Digital Core Power Supply (1.25V)**
58	VDD	I	—	**Digital Core Power Supply (1.25V)**
79	VDD	I	—	**Digital Core Power Supply (1.25V)**
99	VDD	I	—	**Digital Core Power Supply (1.25V)**
E-PAD	VSS	I	—	**Digital Ground (Exposed PAD), VSS**
43	VSSM	I	—	**Analog Ground for VDDM**
41	VAGND1	I	—	**Negative Analog Reference Voltage 1**
80	VSS	I	—	**Oscillator Ground, VSS(OSC)**
83	VEXT	I	—	**Digital Power Supply for Oscillator (shall be supplied with same level as used for VEXT), VEXT(OSC)**

2.5 TC36x TQFP-144 封装变体引脚配置

注释：在以下QFP封装中，VFLEX 电源内部连接到VEXT 电源，因此不会在相应的封装图中或电源表中显示为专用引脚。

表 2-66 端口 P00 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
11	P00.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN0_1			**Mux input channel 0 of TIM module 2**
	CCU61_CTRAPA			**Trap input capture**
	CCU60_T12HRE			**External timer start 12**
	MSC0_INJ0			**Injection signal from port**
	GETH_MDIOA			**MDIO Input**
	P00.0	O0		**General-purpose output**
	GTM_TOUT9	O1		**GTM muxed output**
	IOM_REF0_9			**Reference input 0**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN3_ATX	O3		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O4		**Reserved**
	CAN10_TXD	O5		**CAN transmit output node 0**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
	GETH_MDIO	O		**MDIO Output**

表 2-66 端口 P00 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
12	P00.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN1_1			**Mux input channel 1 of TIM module 2**
	CCU60_CC60INB			**T12 capture input 60**
	ASCLIN3_ARXE			**Receive input**
	CAN10_RXDA			**CAN receive input node 0**
	PSI5_RX0A			**RXD inputs (receive data) channel 0**
	CCU61_CC60INA			**T12 capture input 60**
	SENT_SENT0B			**Receive input channel 0**
	EVADC_G9CH11	AI		**Analog input channel 11, group 9**
	P00.1	O0		**General-purpose output**
	GTM_TOUT10	O1		**GTM muxed output**
	IOM_REF0_10			**Reference input 0**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	SENT_SPC0	O6		**Transmit output**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

表 2-66 端口 P00 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
13	P00.2	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM2_IN1_2			**Mux input channel 1 of TIM module 2**
	SENT_SENT1B			**Receive input channel 1**
	EVADC_G9CH10	AI		**Analog input channel 10, group 9**
	P00.2	O0		**General-purpose output**
	GTM_TOUT11	O1		**GTM muxed output**
	IOM_REF0_11			**Reference input 0**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	PSI5_TX0	O4		**TXD outputs (send data)**
	IOM_MON1_14			**Monitor input 1**
	IOM_REF1_14			**Reference input 1**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	QSPI3_SLSO4	O6		**Master slave select output**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**

表 2-66 端口 P00 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
14	P00.3	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM2_IN2_1			Mux input channel 2 of TIM module 2
	CCU60_CC61INB			T12 capture input 61
	EDSADC_DSCIN3A			Modulator clock input, channel 3
	PSI5_RX1A			RXD inputs (receive data) channel 1
	CAN03_RXDA			CAN receive input node 3
	PSI5S_RXA			RX data input
	SENT_SENT2B			Receive input channel 2
	CCU61_CC61INA			T12 capture input 61
	EVADC_G9CH9	AI		Analog input channel 9, group 9
	P00.3	O0		General-purpose output
	GTM_TOUT12	O1		GTM muxed output
	IOM_REF0_12			Reference input 0
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	EDSADC_DSCOUT3	O4		Modulator clock output
	—	O5		Reserved
	SENT_SPC2	O6		Transmit output
	CCU61_CC61	O7		T12 PWM channel 61
	IOM_MON1_9			Monitor input 1
	IOM_REF1_12			Reference input 1

表 2-66 端口 P00 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
15	P00.4	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM2_IN3_1			**Mux input channel 3 of TIM module 2**
	SCU_E_REQ2_2			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	SENT_SENT3B			**Receive input channel 3**
	EDSADC_DSDIN3A			**Digital datastream input, channel 3**
	EDSADC_SGNA			**Carrier sign signal input**
	ASCLIN10_ARXA			**Receive input**
	EVADC_G9CH8	AI		**Analog input channel 8, group 9**
	P00.4	O0		**General-purpose output**
	GTM_TOUT13	O1		**GTM muxed output**
	IOM_REF0_13			**Reference input 0**
	PSI5S_TX	O2		**TX data output**
	CAN11_TXD	O3		**CAN transmit output node 1**
	PSI5_TX1	O4		**TXD outputs (send data)**
	IOM_MON1_15			**Monitor input 1**
	—	O5		**Reserved**
	SENT_SPC3	O6		**Transmit output**
	CCU61_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_12			**Monitor input 1**
	IOM_REF1_9			**Reference input 1**

表 2-66 端口 P00 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
16	P00.5	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM2_IN4_1			Mux input channel 4 of TIM module 2
	CCU60_CC62INB			T12 capture input 62
	EDSADC_DSCIN2A			Modulator clock input, channel 2
	CCU61_CC62INA			T12 capture input 62
	SENT_SENT4B			Receive input channel 4
	CAN11_RXDB			CAN receive input node 1
	GTM_DTMT1_1			CDTM1_DTM0
	EVADC_G9CH7	AI		Analog input channel 7, group 9
	P00.5	O0		General-purpose output
	GTM_TOUT14	O1		GTM muxed output
	IOM_REF0_14			Reference input 0
	EDSADC_CGPWMN	O2		Negative carrier generator output
	QSPI3_SLSO3	O3		Master slave select output
	EDSADC_DSCOUT2	O4		Modulator clock output
	EVADC_FC0BFLOUT	O5		Boundary flag output, FC channel 0
	SENT_SPC4	O6		Transmit output
	CCU61_CC62	O7		T12 PWM channel 62
	IOM_MON1_10			Monitor input 1
	IOM_REF1_11			Reference input 1
17	P00.6	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM2_IN5_1			Mux input channel 5 of TIM module 2
	EDSADC_DSDIN2A			Digital datastream input, channel 2
	SENT_SENT5B			Receive input channel 5
	ASCLIN5_ARXA			Receive input
	EVADC_G9CH6	AI		Analog input channel 6, group 9
	P00.6	O0		General-purpose output
	GTM_TOUT15	O1		GTM muxed output
	IOM_REF0_15			Reference input 0
	EDSADC_CGPWMP	O2		Positive carrier generator output
	—	O3		Reserved
	—	O4		Reserved
	EVADC_EMUX10	O5		Control of external analog multiplexer interface 1
	SENT_SPC5	O6		Transmit output
	CCU61_COUT62	O7		T12 PWM channel 62
	IOM_MON1_13			Monitor input 1
	IOM_REF1_8			Reference input 1

表 2-66 端口 P00 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
18	P00.7	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM2_IN6_1			**Mux input channel 6 of TIM module 2**
	CCU61_CC60INC			**T12 capture input 60**
	SENT_SENT6B			**Receive input channel 6**
	GPT120_T2INA			**Trigger/gate input of timer T2**
	CCU61_CCPOS0A			**Hall capture input 0**
	CCU60_T12HRB			**External timer start 12**
	GTM_DTMT0_2			**CDTM0_DTM0**
	EVADC_G9CH5	AI		**Analog input channel 5, group 9**
	P00.7	O0		**General-purpose output**
	GTM_TOUT16	O1		**GTM muxed output**
	ASCLIN5_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	EVADC_EMUX11	O5		**Control of external analog multiplexer interface 1**
	SENT_SPC6	O6		**Transmit output**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**
19	P00.8	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM2_IN7_1			**Mux input channel 7 of TIM module 2**
	CCU61_CC61INC			**T12 capture input 61**
	SENT_SENT7B			**Receive input channel 7**
	GPT120_T2EUDA			**Count direction control input of timer T2**
	CCU61_CCPOS1A			**Hall capture input 1**
	CCU60_T13HRB			**External timer start 13**
	ASCLIN10_ARXB			**Receive input**
	EVADC_G9CH4	AI		**Analog input channel 4, group 9**
	P00.8	O0		**General-purpose output**
	GTM_TOUT17	O1		**GTM muxed output**
	QSPI3_SLSO6	O2		**Master slave select output**
	ASCLIN10_ATX	O3		**Transmit output**
	—	O4		**Reserved**
	EVADC_EMUX12	O5		**Control of external analog multiplexer interface 1**
	SENT_SPC7	O6		**Transmit output**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**

表 2-66 端口 P00 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
20	P00.9	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM1_IN0_1			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_1			Mux input channel 0 of TIM module 0
	CCU61_CC62INC			T12 capture input 62
	SENT_SENT8B			Receive input channel 8
	CCU61_CCPOS2A			Hall capture input 2
	EDSADC_DSCIN1A			Modulator clock input, channel 1
	EDSADC_ITR3F			Trigger/Gate input, channel 3
	GPT120_T4EUDA			Count direction control input of timer T4
	CCU60_T13HRC			External timer start 13
	CCU60_T12HRC			External timer start 12
	EVADC_G9CH3	AI		Analog input channel 3, group 9
	P00.9	O0		General-purpose output
	GTM_TOUT18	O1		GTM muxed output
	QSPI3_SLSO7	O2		Master slave select output
	ASCLIN3_ARTS	O3		Ready to send output
	EDSADC_DSCOUT1	O4		Modulator clock output
	ASCLIN4_ATX	O5		Transmit output
	SENT_SPC8	O6		Transmit output
	CCU61_CC62	O7		T12 PWM channel 62
	IOM_MON1_10			Monitor input 1
	IOM_REF1_11			Reference input 1

表 2-66 端口 P00 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
21	P00.12	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM1_IN3_1			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_1			**Mux input channel 3 of TIM module 0**
	ASCLIN3_ACTSA			**Clear to send input**
	EDSADC_DSDIN0A			**Digital datastream input, channel 0**
	ASCLIN4_ARXA			**Receive input**
	EVADC_G9CH0	AI		**Analog input channel 0, group 9**
	P00.12	O0		**General-purpose output**
	GTM_TOUT21	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_7			**Monitor input 1**
	IOM_REF1_7			**Reference input 1**

表 2-67 端口 P02 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
1	P02.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_2			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_2			Mux input channel 0 of TIM module 0
	CCU61_CC60INB			T12 capture input 60
	ASCLIN2_ARXG			Receive input
	CCU60_CC60INA			T12 capture input 60
	SCU_E_REQ3_2			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	GTM_DTMA0_0			CDTM0_DTM4
	P02.0	O0		General-purpose output
	GTM_TOUT0	O1		GTM muxed output
	IOM_REF0_0			Reference input 0
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI3_SLSO1	O3		Master slave select output
	EDSADC_CGPWMN	O4		Negative carrier generator output
	CAN00_TXD	O5		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	ERAY0_TXDA	O6		Transmit Channel A
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
	IOM_REF1_6			Reference input 1

表 2-67 端口 P02 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
2	P02.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN1_2			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_2			**Mux input channel 1 of TIM module 0**
	ERAY0_RXDA2			**Receive Channel A2**
	ASCLIN2_ARXB			**Receive input**
	CAN00_RXDA			**CAN receive input node 0**
	SCU_E_REQ2_1			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P02.1	O0		**General-purpose output**
	GTM_TOUT1	O1		**GTM muxed output**
	IOM_REF0_1			**Reference input 0**
	—	O2		**Reserved**
	QSPI3_SLSO2	O3		**Master slave select output**
	EDSADC_CGPWMP	O4		**Positive carrier generator output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**

表 2-67 端口 P02 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
3	P02.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN2_2			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_2			**Mux input channel 2 of TIM module 0**
	CCU61_CC61INB			**T12 capture input 61**
	CCU60_CC61INA			**T12 capture input 61**
	P02.2	O0		**General-purpose output**
	GTM_TOUT2	O1		**GTM muxed output**
	IOM_REF0_2			**Reference input 0**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI3_SLSO3	O3		**Master slave select output**
	PSI5_TX0	O4		**TXD outputs (send data)**
	IOM_MON1_14			**Monitor input 1**
	IOM_REF1_14			**Reference input 1**
	CAN02_TXD	O5		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	ERAY0_TXDB	O6		**Transmit Channel B**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**

表 2-67 端口 P02 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
4	P02.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN3_2			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_2			**Mux input channel 3 of TIM module 0**
	ERAY0_RXDB2			**Receive Channel B2**
	CAN02_RXDB			**CAN receive input node 2**
	ASCLIN1_ARXG			**Receive input**
	PSI5_RX0B			**RXD inputs (receive data) channel 0**
	P02.3	O0		**General-purpose output**
	GTM_TOUT3	O1		**GTM muxed output**
	IOM_REF0_3			**Reference input 0**
	ASCLIN2_ASLSO	O2		**Slave select signal output**
	QSPI3_SLSO4	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

表 2-67 端口 P02 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
5	P02.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN4_1			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_1			**Mux input channel 4 of TIM module 0**
	CCU61_CC62INB			**T12 capture input 62**
	QSPI3_SLSIA			**Slave select input**
	CCU60_CC62INA			**T12 capture input 62**
	I2C0_SDAA			**Serial Data Input 0**
	CAN11_RXDA			**CAN receive input node 1**
	CAN0_ECTT1			**External CAN time trigger input**
	P02.4	O0		**General-purpose output**
	GTM_TOUT4	O1		**GTM muxed output**
	IOM_REF0_4			**Reference input 0**
	ASCLIN2_ASCLK	O2		**Shift clock output**
	QSPI3_SLSO0	O3		**Master slave select output**
	PSI5S_CLK	O4		**PSI5S CLK is a clock that can be used on a pin to drive the external PHY.**
	I2C0_SDA	O5		**Serial Data Output**
	ERAY0_TXENA	O6		**Transmit Enable Channel A**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

表 2-67 端口 P02 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
6	P02.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN5_1			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_1			**Mux input channel 5 of TIM module 0**
	I2C0_SCLA			**Serial Clock Input 0**
	PSI5_RX1B			**RXD inputs (receive data) channel 1**
	PSI5S_RXB			**RX data input**
	QSPI3_MRSTA			**Master SPI data input**
	SENT_SENT3C			**Receive input channel 3**
	CAN0_ECTT2			**External CAN time trigger input**
	P02.5	O0		**General-purpose output**
	GTM_TOUT5	O1		**GTM muxed output**
	IOM_REF0_5			**Reference input 0**
	CAN11_TXD	O2		**CAN transmit output node 1**
	QSPI3_MRST	O3		**Slave SPI data output**
	IOM_MON2_3			**Monitor input 2**
	IOM_REF2_3			**Reference input 2**
	—	O4		**Reserved**
	I2C0_SCL	O5		**Serial Clock Output**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**

表 2-67 端口 P02 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
7	P02.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_1			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_1			**Mux input channel 6 of TIM module 0**
	CCU60_CC60INC			**T12 capture input 60**
	SENT_SENT2C			**Receive input channel 2**
	GPT120_T3INA			**Trigger/gate input of core timer T3**
	CCU60_CCPOS0A			**Hall capture input 0**
	CCU61_T12HRB			**External timer start 12**
	QSPI3_MTSRA			**Slave SPI data input**
	P02.6	O0		**General-purpose output**
	GTM_TOUT6	O1		**GTM muxed output**
	IOM_REF0_6			**Reference input 0**
	PSI5S_TX	O2		**TX data output**
	QSPI3_MTSR	O3		**Master SPI data output**
	PSI5_TX1	O4		**TXD outputs (send data)**
	IOM_MON1_15			**Monitor input 1**
	EVADC_EMUX00	O5		**Control of external analog multiplexer interface 0**
	—	O6		**Reserved**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

表 2-67 端口 P02 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
8	P02.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN7_1			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_1			**Mux input channel 7 of TIM module 0**
	CCU60_CC61INC			**T12 capture input 61**
	SENT_SENT1C			**Receive input channel 1**
	EDSADC_DSCIN3B			**Modulator clock input, channel 3**
	GPT120_T3EUDA			**Count direction control input of core timer T3**
	CCU60_CCPOS1A			**Hall capture input 1**
	QSPI3_SCLKA			**Slave SPI clock inputs**
	CCU61_T13HRB			**External timer start 13**
	P02.7	O0		**General-purpose output**
	GTM_TOUT7	O1		**GTM muxed output**
	IOM_REF0_7			**Reference input 0**
	—	O2		**Reserved**
	QSPI3_SCLK	O3		**Master SPI clock output**
	EDSADC_DSCOUT3	O4		**Modulator clock output**
	EVADC_EMUX01	O5		**Control of external analog multiplexer interface 0**
	SENT_SPC1	O6		**Transmit output**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**

表 2-67 端口 P02 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
9	P02.8	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN0_2			**Mux input channel 0 of TIM module 2**
	CCU60_CC62INC			**T12 capture input 62**
	SENT_SENT0C			**Receive input channel 0**
	CCU60_CCPOS2A			**Hall capture input 2**
	EDSADC_DSDIN3B			**Digital datastream input, channel 3**
	EDSADC_ITR3E			**Trigger/Gate input, channel 3**
	GPT120_T4INA			**Trigger/gate input of timer T4**
	CCU61_T12HRC			**External timer start 12**
	CCU61_T13HRC			**External timer start 13**
	GTM_DTMA0_1			**CDTM0_DTM4**
	P02.8	O0		**General-purpose output**
	GTM_TOUT8	O1		**GTM muxed output**
	IOM_REF0_8			**Reference input 0**
	QSPI3_SLSO5	O2		**Master slave select output**
	ASCLIN8_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	EVADC_EMUX02	O5		**Control of external analog multiplexer interface 0**
	GETH_MDC	O6		**MDIO clock**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

表 2-68 端口 P10 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
140	P10.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_3			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_3			Mux input channel 1 of TIM module 0
	GPT120_T5EUDB			Count direction control input of timer T5
	QSPI1_MRSTA			Master SPI data input
	GTM_DTMT0_1			CDTM0_DTM0
	P10.1	O0		General-purpose output
	GTM_TOUT103	O1		GTM muxed output
	QSPI1_MTSR	O2		Master SPI data output
	QSPI1_MRST	O3		Slave SPI data output
	IOM_MON2_1			Monitor input 2
	IOM_REF2_1			Reference input 2
	MSC0_EN1	O4		Chip Select
	EVADC_FC1BFLOUT	O5		Boundary flag output, FC channel 1
	—	O6		Reserved
	—	O7		Reserved
141	P10.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_3			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_3			Mux input channel 2 of TIM module 0
	CAN02_RXDE			CAN receive input node 2
	MSC0_SDI1			Upstream assynchronous input signal
	QSPI1_SCLKA			Slave SPI clock inputs
	GPT120_T6INB			Trigger/gate input of core timer T6
	SCU_E_REQ2_0			ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P10.2	O0		General-purpose output
	GTM_TOUT104	O1		GTM muxed output
	IOM_MON2_9			Monitor input 2
	—	O2		Reserved
	QSPI1_SCLK	O3		Master SPI clock output
	MSC0_EN0	O4		Chip Select
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-68 端口 P10 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
142	P10.3	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN3_3			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_3			Mux input channel 3 of TIM module 0
	QSPI1_MTSRA			Slave SPI data input
	SCU_E_REQ3_0			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	GPT120_T5INB			Trigger/gate input of timer T5
	P10.3	O0		General-purpose output
	GTM_TOUT105	O1		GTM muxed output
	IOM_MON2_10			Monitor input 2
	—	O2		Reserved
	QSPI1_MTSR	O3		Master SPI data output
	MSC0_EN0	O4		Chip Select
	—	O5		Reserved
	CAN02_TXD	O6		CAN transmit output node 2
	IOM_MON2_7			Monitor input 2
	IOM_REF2_7			Reference input 2
	—	O7		Reserved
143	P10.5	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_4			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_4			Mux input channel 2 of TIM module 0
	PMS_HWCFG4IN			HWCFG4 pin input
	MSC0_INJ1			Injection signal from port
	P10.5	O0		General-purpose output
	GTM_TOUT107	O1		GTM muxed output
	IOM_REF2_9			Reference input 2
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI3_SLSO8	O3		Master slave select output
	QSPI1_SLSO9	O4		Master slave select output
	GPT120_T6OUT	O5		External output for overflow/underflow detection of core timer T6
	ASCLIN2_ASLSO	O6		Slave select signal output
	—	O7		Reserved

表 2-68 端口 P10 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
144	P10.6	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN3_4			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_4			Mux input channel 3 of TIM module 0
	ASCLIN2_ARXD			Receive input
	QSPI3_MTSRB			Slave SPI data input
	PMS_HWCFG5IN			HWCFG5 pin input
	P10.6	O0		General-purpose output
	GTM_TOUT108	O1		GTM muxed output
	IOM_REF2_10			Reference input 2
	ASCLIN2_ASCLK	O2		Shift clock output
	QSPI3_MTSR	O3		Master SPI data output
	GPT120_T3OUT	O4		External output for overflow/underflow detection of core timer T3
	—	O5		Reserved
	QSPI1_MRST	O6		Slave SPI data output
	IOM_MON2_1			Monitor input 2
	IOM_REF2_1			Reference input 2
	—	O7		Reserved

表 2-69 端口 P11 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
132	P11.2	I	RFAST / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM2_IN1_3			Mux input channel 1 of TIM module 2
	P11.2	O0		General-purpose output
	GTM_TOUT95	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO5	O3		Master slave select output
	QSPI1_SLSO5	O4		Master slave select output
	MSC0_EN1	O5		Chip Select
	GETH_TXD1	O6		Transmit Data
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1

表 2-69 端口 P11 功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
133	P11.3	I	RFAST / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM2_IN2_2			Mux input channel 2 of TIM module 2
	MSC0_SDI3			Upstream assynchronous input signal
	QSPI1_MRSTB			Master SPI data input
	P11.3	O0		General-purpose output
	GTM_TOUT96	O1		GTM muxed output
	—	O2		Reserved
	QSPI1_MRST	O3		Slave SPI data output
	IOM_MON2_1			Monitor input 2
	IOM_REF2_1			Reference input 2
	ERAY0_TXDA	O4		Transmit Channel A
	—	O5		Reserved
	GETH_TXD0	O6		Transmit Data
	CCU60_COUT62	O7		T12 PWM channel 62
	IOM_MON1_5			Monitor input 1
	IOM_REF1_1			Reference input 1
134	P11.6	I	RFAST / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM2_IN3_2			Mux input channel 3 of TIM module 2
	QSPI1_SCLKB			Slave SPI clock inputs
	P11.6	O0		General-purpose output
	GTM_TOUT97	O1		GTM muxed output
	ERAY0_TXENB	O2		Transmit Enable Channel B
	QSPI1_SCLK	O3		Master SPI clock output
	ERAY0_TXENA	O4		Transmit Enable Channel A
	MSC0_FCLP	O5		Shift-clock direct part of the differential signal
	GETH_TXEN	O6		Transmit Enable MII and RMII
	GETH_TCTL			Transmit Control for RGMII
	CCU60_COUT61	O7		T12 PWM channel 61
	IOM_MON1_4			Monitor input 1
	IOM_REF1_2			Reference input 1

表 2-69 端口 P11 功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
136	P11.8	I	SLOW / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM2_IN5_8			**Mux input channel 5 of TIM module 2**
	GETH_RXD2A			**Receive Data 2 MII and RGMII (RGMII can use RXD2A only)**
	CAN12_RXDD			**CAN receive input node 2**
	P11.8	O0		**General-purpose output**
	GTM_TOUT124	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
135	P11.9	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM2_IN4_2			**Mux input channel 4 of TIM module 2**
	QSPI1_MTSRB			**Slave SPI data input**
	ERAY0_RXDA1			**Receive Channel A1**
	GETH_RXD1A			**Receive Data 1 MII, RMII and RGMII (RGMII can use RXD1A only)**
	P11.9	O0		**General-purpose output**
	GTM_TOUT98	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI1_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	MSC0_SOP	O5		**Data output - direct part of the differential signal**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**

表 2-69 端口 P11 功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
137	P11.10	I	FAST / RGMII_Input / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM2_IN5_2			Mux input channel 5 of TIM module 2
	GTM_TIM2_IN0_9			Mux input channel 0 of TIM module 2
	CAN03_RXDD			CAN receive input node 3
	ERAY0_RXDB1			Receive Channel B1
	ASCLIN1_ARXE			Receive input
	SCU_E_REQ6_3			ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	MSC0_SDI0			Upstream assynchronous input signal
	GETH_RXD0A			Receive Data 0 MII, RMII and RGMII (RGMII can use RXD0A only)
	QSPI1_SLSIA			Slave select input
	P11.10	O0		General-purpose output
	GTM_TOUT99	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO3	O3		Master slave select output
	QSPI1_SLSO3	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	CCU60_CC62	O7		T12 PWM channel 62
	IOM_MON1_0			Monitor input 1
	IOM_REF1_4			Reference input 1
138	P11.11	I	FAST / RGMII_Input / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM2_IN6_2			Mux input channel 6 of TIM module 2
	GETH_CRSDVA			Carrier Sense / Data Valid combi-signal for RMII
	GETH_RXDVA			Receive Data Valid MII
	GETH_CRSB			Carrier Sense MII
	GETH_RCTLA			Receive Control for RGMII
	P11.11	O0		General-purpose output
	GTM_TOUT100	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO4	O3		Master slave select output
	QSPI1_SLSO4	O4		Master slave select output
	MSC0_EN0	O5		Chip Select
	ERAY0_TXENB	O6		Transmit Enable Channel B
	CCU60_CC61	O7		T12 PWM channel 61
	IOM_MON1_1			Monitor input 1
	IOM_REF1_5			Reference input 1

表 2-69 端口 P11 功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
139	P11.12	I	FAST / RGMII_Input / PU1 / VFLEX / ES	General-purpose input
	GTM_TIM2_IN7_2			Mux input channel 7 of TIM module 2
	GETH_REFCLKA			Reference Clock input for RMII (50 MHz)
	GETH_TXCLKB			Transmit Clock Input for MII
	GETH_RXCLKA			Receive Clock MII
	P11.12	O0		General-purpose output
	GTM_TOUT101	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	GTM_CLK2	O3		CGM generated clock
	ERAY0_TXDB	O4		Transmit Channel B
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	CCU_EXTCLK1	O6		External Clock 1
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
	IOM_REF1_6			Reference input 1

表 2-70 端口 P13 的功能

Pin	Symbol	Ctrl.	Buffer Type	Function
128	P13.0	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM2_IN5_3			Mux input channel 5 of TIM module 2
	ASCLIN10_ARXC			Receive input
	P13.0	O0		General-purpose output
	GTM_TOUT91	O1		GTM muxed output
	ASCLIN10_ATX	O2		Transmit output
	QSPI2_SCLKN	O3		Master SPI clock output (LVDS N line)
	MSC0_EN1	O4		Chip Select
	MSC0_FCLN	O5		Shift-clock inverted part of the differential signal
	—	O6		Reserved
	CAN10_TXD	O7		CAN transmit output node 0

表 2-70 端口 P13 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
129	P13.1	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM2_IN6_3			Mux input channel 6 of TIM module 2
	I2C0_SCLB			Serial Clock Input 1
	CAN10_RXDD			CAN receive input node 0
	ASCLIN10_ARXD			Receive input
	P13.1	O0		General-purpose output
	GTM_TOUT92	O1		GTM muxed output
	—	O2		Reserved
	QSPI2_SCLKP	O3		Master SPI clock output (LVDS P line)
	—	O4		Reserved
	MSC0_FCLP	O5		Shift-clock direct part of the differential signal
	I2C0_SCL	O6		Serial Clock Output
	—	O7		Reserved
130	P13.2	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM2_IN7_3			Mux input channel 7 of TIM module 2
	GPT120_CAPINA			Trigger input to capture value of timer T5 into CAPREL register
	I2C0_SDAB			Serial Data Input 1
	P13.2	O0		General-purpose output
	GTM_TOUT93	O1		GTM muxed output
	ASCLIN10_ASCLK	O2		Shift clock output
	QSPI2_MTSRN	O3		Master SPI data output (LVDS N line)
	MSC0_FCLP	O4		Shift-clock direct part of the differential signal
	MSC0_SON	O5		Data output - inverted part of the differential signal
	I2C0_SDA	O6		Serial Data Output
	—	O7		Reserved
131	P13.3	I	LVDS_TX / FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM2_IN0_3			Mux input channel 0 of TIM module 2
	P13.3	O0		General-purpose output
	GTM_TOUT94	O1		GTM muxed output
	ASCLIN10_ASLSO	O2		Slave select signal output
	QSPI2_MTSRP	O3		Master SPI data output (LVDS P line)
	—	O4		Reserved
	MSC0_SOP	O5		Data output - direct part of the differential signal
	—	O6		Reserved
	—	O7		Reserved

表 2-71 端口 P14 的功能

Pin	Symbol	Ctrl.	Buffer Type	Function
118	P14.0	I	FAST / PU1 / VEXT / ES2	**General-purpose input**
	GTM_TIM1_IN3_5			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_5			**Mux input channel 3 of TIM module 0**
	P14.0	O0		**General-purpose output**
	GTM_TOUT80	O1		**GTM muxed output**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	ERAY0_TXDA	O3		**Transmit Channel A**
	ERAY0_TXDB	O4		**Transmit Channel B**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	ASCLIN0_ASCLK	O6		**Shift clock output**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**

表 2-71 端口 P14 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
119	P14.1	I	FAST / PU1 / VEXT / ES2	General-purpose input
	GTM_TIM1_IN4_3			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_3			Mux input channel 4 of TIM module 0
	ERAY0_RXDA3			Receive Channel A3
	ASCLIN0_ARXA			Receive input
	ERAY0_RXDB3			Receive Channel B3
	CAN01_RXDB			CAN receive input node 1
	SCU_E_REQ3_1			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	PMS_PINAWKP			PINA (P14.1) pin input
	P14.1	O0		General-purpose output
	GTM_TOUT81	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1
120	P14.2	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN5_3			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_3			Mux input channel 5 of TIM module 0
	PMS_HWCFG2IN			HWCFG2 pin input
	P14.2	O0		General-purpose output
	GTM_TOUT82	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI2_SLSO1	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	ASCLIN2_ASCLK	O6		Shift clock output
	—	O7		Reserved

表 2-71 端口 P14 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
121	P14.3	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_3			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_3			**Mux input channel 6 of TIM module 0**
	PMS_HWCFG3IN			**HWCFG3 pin input**
	ASCLIN2_ARXA			**Receive input**
	MSC0_SDI2			**Upstream assynchronous input signal**
	SCU_E_REQ1_0			**ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P14.3	O0		**General-purpose output**
	GTM_TOUT83	O1		**GTM muxed output**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI2_SLSO3	O3		**Master slave select output**
	ASCLIN1_ASLSO	O4		**Slave select signal output**
	ASCLIN3_ASLSO	O5		**Slave select signal output**
	—	O6		**Reserved**
	—	O7		**Reserved**
122	P14.4	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN7_2			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_2			**Mux input channel 7 of TIM module 0**
	PMS_HWCFG6IN			**HWCFG6 pin input**
	GTM_DTMT0_0			**CDTM0_DTM0**
	P14.4	O0		**General-purpose output**
	GTM_TOUT84	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	GETH_PPS	O6		**Pulse Per Second**
	—	O7		**Reserved**

表 2-71 端口 P14 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
123	P14.5	I	FAST / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN0_4			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_4			**Mux input channel 0 of TIM module 0**
	PMS_HWCFG1IN			**HWCFG1 pin input**
	GTM_DTMA2_0			**CDTM2_DTM4**
	P14.5	O0		**General-purpose output**
	GTM_TOUT85	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ERAY0_TXDB	O6		**Transmit Channel B**
	—	O7		**Reserved**
124	P14.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN1_4			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_4			**Mux input channel 1 of TIM module 0**
	P14.6	O0		**General-purpose output**
	GTM_TOUT86	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SLSO2	O3		**Master slave select output**
	CAN13_TXD	O4		**CAN transmit output node 3**
	—	O5		**Reserved**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	—	O7		**Reserved**

表 2-72 端口 P15 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
109	P15.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN3_4			Mux input channel 3 of TIM module 2
	P15.0	O0		General-purpose output
	GTM_TOUT71	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI0_SLSO13	O3		Master slave select output
	—	O4		Reserved
	CAN02_TXD	O5		CAN transmit output node 2
	IOM_MON2_7			Monitor input 2
	IOM_REF2_7			Reference input 2
	ASCLIN1_ASCLK	O6		Shift clock output
	—	O7		Reserved
110	P15.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN4_4			Mux input channel 4 of TIM module 2
	CAN02_RXDA			CAN receive input node 2
	ASCLIN1_ARXA			Receive input
	QSPI2_SLSIB			Slave select input
	SCU_E_REQ7_2			ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P15.1	O0		General-purpose output
	GTM_TOUT72	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI2_SLSO5	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-72 端口 P15 功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
111	P15.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN5_4			Mux input channel 5 of TIM module 2
	QSPI2_SLSIA			Slave select input
	QSPI2_MRSTE			Master SPI data input
	P15.2	O0		General-purpose output
	GTM_TOUT73	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	QSPI2_SLSO0	O3		Master slave select output
	—	O4		Reserved
	CAN01_TXD	O5		CAN transmit output node 1
	IOM_MON2_6			Monitor input 2
	IOM_REF2_6			Reference input 2
	ASCLIN0_ASCLK	O6		Shift clock output
	—	O7		Reserved
112	P15.3	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN6_4			Mux input channel 6 of TIM module 2
	CAN01_RXDA			CAN receive input node 1
	ASCLIN0_ARXB			Receive input
	QSPI2_SCLKA			Slave SPI clock inputs
	P15.3	O0		General-purpose output
	GTM_TOUT74	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	MSC0_EN1	O5		Chip Select
	—	O6		Reserved
	—	O7		Reserved

表 2-72 端口 P15 功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
113	P15.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN7_4			**Mux input channel 7 of TIM module 2**
	I2C0_SCLC			**Serial Clock Input 2**
	QSPI2_MRSTA			**Master SPI data input**
	SCU_E_REQ0_0			**ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.4	O0		**General-purpose output**
	GTM_TOUT75	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI2_MRST	O3		**Slave SPI data output**
	IOM_MON2_2			**Monitor input 2**
	IOM_REF2_2			**Reference input 2**
	—	O4		**Reserved**
	—	O5		**Reserved**
	I2C0_SCL	O6		**Serial Clock Output**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

表 2-72 端口 P15 功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
114	P15.5	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN0_4			Mux input channel 0 of TIM module 2
	ASCLIN1_ARXB			Receive input
	I2C0_SDAC			Serial Data Input 2
	QSPI2_MTSRA			Slave SPI data input
	SCU_E_REQ4_3			ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P15.5	O0		General-purpose output
	GTM_TOUT76	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI2_MTSR	O3		Master SPI data output
	—	O4		Reserved
	MSC0_EN0	O5		Chip Select
	I2C0_SDA	O6		Serial Data Output
	CCU60_CC61	O7		T12 PWM channel 61
	IOM_MON1_1			Monitor input 1
	IOM_REF1_5			Reference input 1
115	P15.6	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM2_IN2_14			Mux input channel 2 of TIM module 2
	GTM_TIM1_IN0_6			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_6			Mux input channel 0 of TIM module 0
	QSPI2_MTSRB			Slave SPI data input
	P15.6	O0		General-purpose output
	GTM_TOUT77	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	QSPI2_MTSR	O3		Master SPI data output
	—	O4		Reserved
	QSPI2_SCLK	O5		Master SPI clock output
	ASCLIN3_ASCLK	O6		Shift clock output
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
	IOM_REF1_6			Reference input 1

表 2-72 端口 P15 功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
116	P15.7	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_5			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_5			Mux input channel 1 of TIM module 0
	ASCLIN3_ARXA			Receive input
	QSPI2_MRSTB			Master SPI data input
	P15.7	O0		General-purpose output
	GTM_TOUT78	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	QSPI2_MRST	O3		Slave SPI data output
	IOM_MON2_2			Monitor input 2
	IOM_REF2_2			Reference input 2
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT60	O7		T12 PWM channel 60
	IOM_MON1_3			Monitor input 1
	IOM_REF1_3			Reference input 1
117	P15.8	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_5			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_5			Mux input channel 2 of TIM module 0
	QSPI2_SCLKB			Slave SPI clock inputs
	SCU_E_REQ5_0			ERU Channel 5 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P15.8	O0		General-purpose output
	GTM_TOUT79	O1		GTM muxed output
	—	O2		Reserved
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	ASCLIN3_ASCLK	O6		Shift clock output
	CCU60_COUT61	O7		T12 PWM channel 61
	IOM_MON1_4			Monitor input 1
	IOM_REF1_2			Reference input 1

表 2-73 端口 P20 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
93	P20.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_7			**Mux input channel 6 of TIM module 1**
	GTM_TIM1_IN4_9			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN6_7			**Mux input channel 6 of TIM module 0**
	CAN03_RXDC			**CAN receive input node 3**
	CCU_PAD_SYSCLK			**Sysclk input**
	CBS_TGI0			**Trigger input**
	SCU_E_REQ6_0			**ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GPT120_T6EUDA			**Count direction control input of core timer T6**
	P20.0	O0		**General-purpose output**
	GTM_TOUT59	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	ASCLIN3_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	HSCT0_SYSCLK_OUT	O5		**sys clock output**
	—	O6		**Reserved**
	—	O7		**Reserved**
	CBS_TGO0	O		**Trigger output**
94	P20.2	I	S / PU / VEXT	**General-purpose input** This pin is latched at power on reset release to enter test mode.
	$\overline{\text{TESTMODE}}$			**Testmode Enable Input**

表 2-73 端口 P20 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
95	P20.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN4_5			**Mux input channel 4 of TIM module 2**
	ASCLIN3_ARXC			**Receive input**
	GPT120_T6INA			**Trigger/gate input of core timer T6**
	P20.3	O0		**General-purpose output**
	GTM_TOUT61	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	QSPI0_SLSO9	O3		**Master slave select output**
	QSPI2_SLSO9	O4		**Master slave select output**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	—	O6		**Reserved**
	—	O7		**Reserved**
100	P20.6	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN6_5			**Mux input channel 6 of TIM module 2**
	CAN12_RXDA			**CAN receive input node 2**
	ASCLIN9_ARXE			**Receive input**
	P20.6	O0		**General-purpose output**
	GTM_TOUT62	O1		**GTM muxed output**
	ASCLIN1_ARTS	O2		**Ready to send output**
	QSPI0_SLSO8	O3		**Master slave select output**
	QSPI2_SLSO8	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

表 2-73 端口 P20 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
101	P20.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN7_5			**Mux input channel 7 of TIM module 2**
	GTM_TIM1_IN5_8			**Mux input channel 5 of TIM module 1**
	CAN00_RXDB			**CAN receive input node 0**
	ASCLIN1_ACTSA			**Clear to send input**
	ASCLIN9_ARXF			**Receive input**
	P20.7	O0		**General-purpose output**
	GTM_TOUT63	O1		**GTM muxed output**
	ASCLIN9_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN12_TXD	O5		**CAN transmit output node 2**
	—	O6		**Reserved**
	CCU61_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_7			**Monitor input 1**
	IOM_REF1_7			**Reference input 1**
102	P20.8	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN7_3			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_3			**Mux input channel 7 of TIM module 0**
	P20.8	O0		**General-purpose output**
	GTM_TOUT64	O1		**GTM muxed output**
	ASCLIN1_ASLSO	O2		**Slave select signal output**
	QSPI0_SLSO0	O3		**Master slave select output**
	QSPI1_SLSO0	O4		**Master slave select output**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

表 2-73 端口 P20 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
103	P20.9	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN5_5			**Mux input channel 5 of TIM module 2**
	CAN03_RXDE			**CAN receive input node 3**
	ASCLIN1_ARXC			**Receive input**
	QSPI0_SLSIB			**Slave select input**
	SCU_E_REQ7_0			**ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P20.9	O0		**General-purpose output**
	GTM_TOUT65	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SLSO1	O3		**Master slave select output**
	QSPI1_SLSO1	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**
104	P20.10	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN6_6			**Mux input channel 6 of TIM module 2**
	P20.10	O0		**General-purpose output**
	GTM_TOUT66	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI0_SLSO6	O3		**Master slave select output**
	QSPI2_SLSO7	O4		**Master slave select output**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	ASCLIN1_ASCLK	O6		**Shift clock output**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**

表 2-73 端口 P20 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
105	P20.11	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN7_6			**Mux input channel 7 of TIM module 2**
	QSPI0_SCLKA			**Slave SPI clock inputs**
	P20.11	O0		**General-purpose output**
	GTM_TOUT67	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**
106	P20.12	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN0_5			**Mux input channel 0 of TIM module 2**
	QSPI0_MRSTA			**Master SPI data input**
	IOM_PIN_13			**GPIO pad input to FPC**
	P20.12	O0		**General-purpose output**
	GTM_TOUT68	O1		**GTM muxed output**
	IOM_MON0_13			**Monitor input 0**
	—	O2		**Reserved**
	QSPI0_MRST	O3		**Slave SPI data output**
	IOM_MON2_0			**Monitor input 2**
	IOM_REF2_0			**Reference input 2**
	QSPI0_MTSR	O4		**Master SPI data output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_12			**Monitor input 1**
	IOM_REF1_9			**Reference input 1**

表 2-73 端口 P20 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
107	P20.13	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN1_4			**Mux input channel 1 of TIM module 2**
	QSPI0_SLSIA			**Slave select input**
	IOM_PIN_14			**GPIO pad input to FPC**
	P20.13	O0		**General-purpose output**
	GTM_TOUT69	O1		**GTM muxed output**
	IOM_MON0_14			**Monitor input 0**
	—	O2		**Reserved**
	QSPI0_SLSO2	O3		**Master slave select output**
	QSPI1_SLSO2	O4		**Master slave select output**
	QSPI0_SCLK	O5		**Master SPI clock output**
	—	O6		**Reserved**
	CCU61_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_13			**Monitor input 1**
	IOM_REF1_8			**Reference input 1**
108	P20.14	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN2_4			**Mux input channel 2 of TIM module 2**
	QSPI0_MTSRA			**Slave SPI data input**
	IOM_PIN_15			**GPIO pad input to FPC**
	DMU_FDEST			**Enter destructive debug mode**
	P20.14	O0		**General-purpose output**
	GTM_TOUT70	O1		**GTM muxed output**
	IOM_MON0_15			**Monitor input 0**
	—	O2		**Reserved**
	QSPI0_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

表 2-74 端口 P21 的功能

Pin	Symbol	Ctrl.	Buffer Type	Function
84	P21.2	I	LVDS_RX / FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_7			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_7			Mux input channel 0 of TIM module 0
	QSPI2_MRSTCN			Master SPI data input (LVDS N line)
	SCU_EMGSTOP_PORT_B			Emergency stop Port Pin B input request
	ASCLIN3_ARXGN			Differential Receive input (low active)
	HSCT0_RXDN			Rx data
	ASCLIN11_ARXE			Receive input
	GTM_DTMA1_0			CDTM1_DTM4
	P21.2	O0		General-purpose output
	GTM_TOUT53	O1		GTM muxed output
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	GETH_MDC	O5		MDIO clock
	—	O6		Reserved
	—	O7		Reserved
85	P21.3	I	LVDS_RX / FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_6			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_6			Mux input channel 1 of TIM module 0
	QSPI2_MRSTCP			Master SPI data input (LVDS P line)
	ASCLIN3_ARXGP			Differential Receive input (high active)
	GETH_MDIOD			MDIO Input
	HSCT0_RXDP			Rx data
	P21.3	O0		General-purpose output
	GTM_TOUT54	O1		GTM muxed output
	ASCLIN11_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	GETH_MDIO	O		MDIO Output

表 2-74 端口 P21 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
86	P21.4	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM1_IN2_6			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_6			**Mux input channel 2 of TIM module 0**
	P21.4	O0		**General-purpose output**
	GTM_TOUT55	O1		**GTM muxed output**
	ASCLIN11_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSCT0_TXDN	O		**Tx data**
87	P21.5	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM1_IN3_6			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_6			**Mux input channel 3 of TIM module 0**
	ASCLIN11_ARXF			**Receive input**
	P21.5	O0		**General-purpose output**
	GTM_TOUT56	O1		**GTM muxed output**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN11_ATX	O3		**Transmit output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSCT0_TXDP	O		**Tx data**

表 2-74 端口 P21 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
88	P21.6/TDI	I	FAST / PD / PU2 / VEXT / ES3	**General-purpose input** PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ.
	GTM_TIM1_IN4_8			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_8			**Mux input channel 4 of TIM module 0**
	GPT120_T5EUDA			**Count direction control input of timer T5**
	ASCLIN3_ARXF			**Receive input**
	CBS_TGI2			**Trigger input**
	TDI			**JTAG Module Data Input**
	P21.6	O0		**General-purpose output**
	GTM_TOUT57	O1		**GTM muxed output**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	GPT120_T3OUT	O7		**External output for overflow/underflow detection of core timer T3**
	CBS_TGO2	O		**Trigger output**
	DAP3	I/O		**DAP: DAP3 Data I/O**

表 2-74 端口 P21 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
90	P21.7/TDO	I	FAST / PU2 / VEXT / ES4	**General-purpose input**
	GTM_TIM1_IN5_7			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_7			**Mux input channel 5 of TIM module 0**
	GPT120_T5INA			**Trigger/gate input of timer T5**
	CBS_TGI3			**Trigger input**
	GETH_RXERB			**Receive Error MII**
	P21.7	O0		**General-purpose output**
	GTM_TOUT58	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	ASCLIN3_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	GPT120_T6OUT	O7		**External output for overflow/underflow detection of core timer T6**
	CBS_TGO3	O		**Trigger output**
	DAP2	I/O		**DAP: DAP2 Data I/O**
	TDO	O		**JTAG Module Data Output**

表 2-75 端口 P22 的功能

Pin	Symbol	Ctrl.	Buffer Type	Function
74	P22.0	I	FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN1_7			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_7			Mux input channel 1 of TIM module 0
	ASCLIN6_ARXE			Receive input
	QSPI3_MTSRD			Slave SPI data input
	P22.0	O0		General-purpose output
	GTM_TOUT47	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	QSPI3_MTSR	O3		Master SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	ASCLIN6_ATX	O7		Transmit output
75	P22.1	I	FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN0_8			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_8			Mux input channel 0 of TIM module 0
	ASCLIN7_ARXE			Receive input
	QSPI3_MRSTD			Master SPI data input
	P22.1	O0		General-purpose output
	GTM_TOUT48	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	QSPI3_MRST	O3		Slave SPI data output
	IOM_MON2_3			Monitor input 2
	IOM_REF2_3			Reference input 2
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	ASCLIN7_ATX	O7		Transmit output

表 2-75端口 P22 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
76	P22.2	I	FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM1_IN3_7			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_7			**Mux input channel 3 of TIM module 0**
	P22.2	O0		**General-purpose output**
	GTM_TOUT49	O1		**GTM muxed output**
	ASCLIN5_ATX	O2		**Transmit output**
	QSPI3_SLSO12	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
77	P22.3	I	FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM1_IN4_4			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_4			**Mux input channel 4 of TIM module 0**
	ASCLIN5_ARXC			**Receive input**
	QSPI3_SCLKD			**Slave SPI clock inputs**
	P22.3	O0		**General-purpose output**
	GTM_TOUT50	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI3_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

表 2-76 端口 P23 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
73	P23.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_4			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_4			**Mux input channel 6 of TIM module 0**
	ASCLIN6_ARXF			**Receive input**
	P23.1	O0		**General-purpose output**
	GTM_TOUT42	O1		**GTM muxed output**
	ASCLIN1_ARTS	O2		**Ready to send output**
	—	O3		**Reserved**
	GTM_CLK0	O4		**CGM generated clock**
	CAN10_TXD	O5		**CAN transmit output node 0**
	CCU_EXTCLK0	O6		**External Clock 0**
	ASCLIN6_ASCLK	O7		**Shift clock output**

表 2-77 端口 P32 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
70	P32.0	I	SLOW / PU1 / VEXT / ES	**General-purpose input** P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
	GTM_TIM2_IN2_5			**Mux input channel 2 of TIM module 2**
	P32.0	O0		**General-purpose output**
	GTM_TOUT36	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
71	P32.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input** P32.1 / External Pass Device gate control for EVRC
	P32.1	O0		**General-purpose output**
	GTM_TOUT37	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

表 2-78 端口 P33 功能

Pin	Symbol	Ctrl.	Buffer Type	Function
56	P33.0	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN4_6			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_6			Mux input channel 4 of TIM module 0
	EDSADC_ITR0E			Trigger/Gate input, channel 0
	IOM_PIN_0			GPIO pad input to FPC
	GTM_DTMT1_2			CDTM1_DTM0
	P33.0	O0		General-purpose output
	GTM_TOUT22	O1		GTM muxed output
	IOM_MON0_0			Monitor input 0
	IOM_GTM_0			GTM-provided inputs to EXOR combiner
	ASCLIN5_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
57	P33.1	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN5_6			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_6			Mux input channel 5 of TIM module 0
	EDSADC_ITR1E			Trigger/Gate input, channel 1
	PSI5_RX0C			RXD inputs (receive data) channel 0
	EDSADC_DSCIN2B			Modulator clock input, channel 2
	SENT_SENT9C			Receive input channel 9
	ASCLIN8_ARXC			Receive input
	IOM_PIN_1			GPIO pad input to FPC
	P33.1	O0		General-purpose output
	GTM_TOUT23	O1		GTM muxed output
	IOM_MON0_1			Monitor input 0
	IOM_GTM_1			GTM-provided inputs to EXOR combiner
	ASCLIN3_ASLSO	O2		Slave select signal output
	QSPI2_SCLK	O3		Master SPI clock output
	EDSADC_DSCOUT2	O4		Modulator clock output
	EVADC_EMUX02	O5		Control of external analog multiplexer interface 0
	—	O6		Reserved
	—	O7		Reserved

表 2-78 端口 P33 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
58	P33.2	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN6_6			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_6			Mux input channel 6 of TIM module 0
	EDSADC_ITR2E			Trigger/Gate input, channel 2
	SENT_SENT8C			Receive input channel 8
	EDSADC_DSDIN2B			Digital datastream input, channel 2
	IOM_PIN_2			GPIO pad input to FPC
	P33.2	O0		General-purpose output
	GTM_TOUT24	O1		GTM muxed output
	IOM_MON0_2			Monitor input 0
	IOM_GTM_2			GTM-provided inputs to EXOR combiner
	ASCLIN3_ASCLK	O2		Shift clock output
	QSPI2_SLSO10	O3		Master slave select output
	PSI5_TX0	O4		TXD outputs (send data)
	IOM_MON1_14			Monitor input 1
	IOM_REF1_14			Reference input 1
	EVADC_EMUX01	O5		Control of external analog multiplexer interface 0
	—	O6		Reserved
	—	O7		Reserved
59	P33.3	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN7_6			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_6			Mux input channel 7 of TIM module 0
	PSI5_RX1C			RXD inputs (receive data) channel 1
	SENT_SENT7C			Receive input channel 7
	EDSADC_DSCIN1B			Modulator clock input, channel 1
	IOM_PIN_3			GPIO pad input to FPC
	P33.3	O0		General-purpose output
	GTM_TOUT25	O1		GTM muxed output
	IOM_MON0_3			Monitor input 0
	IOM_GTM_3			GTM-provided inputs to EXOR combiner
	ASCLIN5_ASCLK	O2		Shift clock output
	—	O3		Reserved
	EDSADC_DSCOUT1	O4		Modulator clock output
	EVADC_EMUX00	O5		Control of external analog multiplexer interface 0
	—	O6		Reserved
	—	O7		Reserved

表 2-78 端口 P33 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
60	P33.4	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN0_10			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_10			Mux input channel 0 of TIM module 0
	EDSADC_ITR0F			Trigger/Gate input, channel 0
	SENT_SENT6C			Receive input channel 6
	EDSADC_DSDIN1B			Digital datastream input, channel 1
	CCU61_CTRAPC			Trap input capture
	ASCLIN5_ARXB			Receive input
	IOM_PIN_4			GPIO pad input to FPC
	P33.4	O0		General-purpose output
	GTM_TOUT26	O1		GTM muxed output
	IOM_MON0_4			Monitor input 0
	IOM_GTM_4			GTM-provided inputs to EXOR combiner
	ASCLIN2_ARTS	O2		Ready to send output
	QSPI2_SLSO12	O3		Master slave select output
	PSI5_TX1	O4		TXD outputs (send data)
	IOM_MON1_15			Monitor input 1
	EVADC_EMUX12	O5		Control of external analog multiplexer interface 1
	EVADC_FC0BFLOUT	O6		Boundary flag output, FC channel 0
	CAN13_TXD	O7		CAN transmit output node 3

表 2-78 端口 P33 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
61	P33.5	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN1_8			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_8			Mux input channel 1 of TIM module 0
	EDSADC_DSCIN0B			Modulator clock input, channel 0
	EDSADC_ITR1F			Trigger/Gate input, channel 1
	GPT120_T4EUDB			Count direction control input of timer T4
	PSI5S_RXC			RX data input
	ASCLIN2_ACTSB			Clear to send input
	CCU61_CCPOS2C			Hall capture input 2
	SENT_SENT5C			Receive input channel 5
	CAN13_RXDB			CAN receive input node 3
	IOM_PIN_5			GPIO pad input to FPC
	P33.5	O0		General-purpose output
	GTM_TOUT27	O1		GTM muxed output
	IOM_MON0_5			Monitor input 0
	IOM_GTM_5			GTM-provided inputs to EXOR combiner
	QSPI0_SLSO7	O2		Master slave select output
	QSPI1_SLSO7	O3		Master slave select output
	EDSADC_DSCOUT0	O4		Modulator clock output
	EVADC_EMUX11	O5		Control of external analog multiplexer interface 1
	—	O6		Reserved
	ASCLIN5_ASLSO	O7		Slave select signal output

表 2-78 端口 P33 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
62	P33.6	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN2_9			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_9			Mux input channel 2 of TIM module 0
	EDSADC_ITR2F			Trigger/Gate input, channel 2
	GPT120_T2EUDB			Count direction control input of timer T2
	SENT_SENT4C			Receive input channel 4
	CCU61_CCPOS1C			Hall capture input 1
	EDSADC_DSDIN0B			Digital datastream input, channel 0
	ASCLIN8_ARXD			Receive input
	IOM_PIN_6			GPIO pad input to FPC
	P33.6	O0		General-purpose output
	GTM_TOUT28	O1		GTM muxed output
	IOM_MON0_6			Monitor input 0
	IOM_GTM_6			GTM-provided inputs to EXOR combiner
	ASCLIN2_ASLSO	O2		Slave select signal output
	QSPI2_SLSO11	O3		Master slave select output
	—	O4		Reserved
	EVADC_EMUX10	O5		Control of external analog multiplexer interface 1
	EVADC_FC1BFLOUT	O6		Boundary flag output, FC channel 1
	PSI5S_TX	O7		TX data output

表 2-78 端口 P33 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
63	P33.7	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN3_9			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_9			Mux input channel 3 of TIM module 0
	CAN00_RXDE			CAN receive input node 0
	GPT120_T2INB			Trigger/gate input of timer T2
	CCU61_CCPOS0C			Hall capture input 0
	SCU_E_REQ4_0			ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	IOM_PIN_7			GPIO pad input to FPC
	P33.7	O0		General-purpose output
	GTM_TOUT29	O1		GTM muxed output
	IOM_MON0_7			Monitor input 0
	IOM_GTM_7			GTM-provided inputs to EXOR combiner
	ASCLIN2_ASCLK	O2		Shift clock output
	—	O3		Reserved
	ASCLIN8_ATX	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

表 2-78 端口 P33 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
64	P33.8	I	FAST / HighZ / VEVRSB	**General-purpose input**
	GTM_TIM1_IN4_7			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_7			**Mux input channel 4 of TIM module 0**
	ASCLIN2_ARXE			**Receive input**
	SCU_EMGSTOP_PORT_A			**Emergency stop Port Pin A input request**
	IOM_PIN_8			**GPIO pad input to FPC**
	P33.8	O0		**General-purpose output**
	GTM_TOUT30	O1		**GTM muxed output**
	IOM_MON0_8			**Monitor input 0**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	CCU61_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_13			**Monitor input 1**
	IOM_REF1_8			**Reference input 1**
	SMU_FSP0	O		**FSP[1..0] Output Signals - Generated by SMU_core**

表 2-78 端口 P33 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
65	P33.9	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN1_9			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_9			Mux input channel 1 of TIM module 0
	IOM_PIN_9			GPIO pad input to FPC
	P33.9	O0		General-purpose output
	GTM_TOUT31	O1		GTM muxed output
	IOM_MON0_9			Monitor input 0
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	—	O3		Reserved
	ASCLIN2_ASCLK	O4		Shift clock output
	CAN01_TXD	O5		CAN transmit output node 1
	IOM_MON2_6			Monitor input 2
	IOM_REF2_6			Reference input 2
	ASCLIN0_ATX	O6		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	CCU61_CC62	O7		T12 PWM channel 62
	IOM_MON1_10			Monitor input 1
	IOM_REF1_11			Reference input 1

表 2-78 端口 P33 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
66	P33.10	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN0_9			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_9			Mux input channel 0 of TIM module 0
	CAN01_RXDD			CAN receive input node 1
	ASCLIN0_ARXD			Receive input
	IOM_PIN_10			GPIO pad input to FPC
	P33.10	O0		General-purpose output
	GTM_TOUT32	O1		GTM muxed output
	IOM_MON0_10			Monitor input 0
	QSPI1_SLSO6	O2		Master slave select output
	—	O3		Reserved
	ASCLIN1_ASLSO	O4		Slave select signal output
	PSI5S_CLK	O5		PSI5S CLK is a clock that can be used on a pin to drive the external PHY.
	—	O6		Reserved
	CCU61_COUT61	O7		T12 PWM channel 61
	IOM_MON1_12			Monitor input 1
	IOM_REF1_9			Reference input 1
	SMU_FSP1	O		FSP[1..0] Output Signals - Generated by SMU_core
67	P33.11	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN2_8			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_8			Mux input channel 2 of TIM module 0
	IOM_PIN_11			GPIO pad input to FPC
	P33.11	O0		General-purpose output
	GTM_TOUT33	O1		GTM muxed output
	IOM_MON0_11			Monitor input 0
	ASCLIN1_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	EDSADC_CGPWMN	O6		Negative carrier generator output
	CCU61_CC61	O7		T12 PWM channel 61
	IOM_MON1_9			Monitor input 1
	IOM_REF1_12			Reference input 1

表 2-78 端口 P33 的功能（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
68	P33.12	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM2_IN0_6			Mux input channel 0 of TIM module 2
	CAN00_RXDD			CAN receive input node 0
	PMS_PINBWKP			PINB (P33.12) pin input
	IOM_PIN_12			GPIO pad input to FPC
	P33.12	O0		General-purpose output
	GTM_TOUT34	O1		GTM muxed output
	IOM_MON0_12			Monitor input 0
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	—	O3		Reserved
	ASCLIN1_ASCLK	O4		Shift clock output
	—	O5		Reserved
	EDSADC_CGPWMP	O6		Positive carrier generator output
	CCU61_COUT60	O7		T12 PWM channel 60
	IOM_MON1_11			Monitor input 1
	IOM_REF1_10			Reference input 1

表 2-79 模拟输入

Pin	Symbol	Ctrl.	Buffer Type	Function
51	AN0	I	D / HighZ / VDDM	Analog Input 0
	EVADC_G0CH0			Analog input channel 0, group 0
	EDSADC_EDS3PA			Positive analog input channel 3, pin A
50	AN1	I	D / HighZ / VDDM	Analog Input 1
	EVADC_G0CH1			Analog input channel 1, group 0
	EDSADC_EDS3NA			Negative analog input channel 3, pin A
49	AN2	I	D / HighZ / VDDM	Analog Input 2
	EVADC_G0CH2			Analog input channel 2, group 0
	EDSADC_EDS0PA			Positive analog input channel 0, pin A
48	AN3	I	D / HighZ / VDDM	Analog Input 3
	EVADC_G0CH3			Analog input channel 3, group 0
	EDSADC_EDS0NA			Negative analog input channel 0, pin A
47	AN4	I	D / HighZ / VDDM	Analog Input 4
	EVADC_G0CH4			Analog input channel 4, group 0
46	AN5	I	D / HighZ / VDDM	Analog Input 5
	EVADC_G0CH5			Analog input channel 5, group 0

表 2-79 模拟输入（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
45	AN11	I	D / HighZ / VDDM	**Analog Input 11**
	EVADC_G1CH3			**Analog input channel 3, group 1**
40	AN16	I	D / HighZ / VDDM	**Analog Input 16**
	EVADC_G2CH0			**Analog input channel 0, group 2**
	EVADC_FC0CH0			**Analog input FC channel 0**
39	AN17	I	D / HighZ / VDDM	**Analog Input 17**
	EVADC_G2CH1			**Analog input channel 1, group 2**
	EVADC_FC1CH0			**Analog input FC channel 1**
38	AN20	I	D / HighZ / VDDM	**Analog Input 20**
	EVADC_G2CH4			**Analog input channel 4, group 2**
	EDSADC_EDS2PA			**Positive analog input channel 2, pin A**
37	AN21	I	D / HighZ / VDDM	**Analog Input 21**
	EVADC_G2CH5			**Analog input channel 5, group 2**
	EDSADC_EDS2NA			**Negative analog input channel 2, pin A**
36	AN24/P40.0	I	S / HighZ / VDDM	**Analog Input 24**
	SENT_SENT0A			**Receive input channel 0**
	EVADC_G3CH0			**Analog input channel 0, group 3**
	CCU60_CCPOS0D			**Hall capture input 0**
	EDSADC_EDS2PB			**Positive analog input channel 2, pin B**
35	AN25/P40.1	I	S / HighZ / VDDM	**Analog Input 25**
	SENT_SENT1A			**Receive input channel 1**
	EVADC_G3CH1			**Analog input channel 1, group 3**
	CCU60_CCPOS1B			**Hall capture input 1**
	EDSADC_EDS2NB			**Negative analog input channel 2, pin B**
34	AN26/P40.2	I	S / HighZ / VDDM	**Analog Input 26**
	SENT_SENT2A			**Receive input channel 2**
	EVADC_G3CH2			**Analog input channel 2, group 3**
	CCU60_CCPOS1D			**Hall capture input 1**
33	AN27/P40.3	I	S / HighZ / VDDM	**Analog Input 27**
	SENT_SENT3A			**Receive input channel 3**
	EVADC_G3CH3			**Analog input channel 3, group 3**
	CCU60_CCPOS2B			**Hall capture input 2**
32	AN28	I	D / HighZ / VDDM	**Analog Input 28**
	EVADC_G3CH4			**Analog input channel 4, group 3**
31	AN32/P40.4	I	S / HighZ / VDDM	**Analog Input 32**
	SENT_SENT4A			**Receive input channel 4**
	EVADC_G8CH0			**Analog input channel 0, group 8**
	CCU60_CCPOS2D			**Hall capture input 2**

表 2-79 模拟输入（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
30	AN33/P40.5	I	S / HighZ / VDDM	**Analog Input 33**
	SENT_SENT5A			**Receive input channel 5**
	EVADC_G8CH1			**Analog input channel 1, group 8**
	CCU61_CCPOS0D			**Hall capture input 0**
29	AN34	I	D / HighZ / VDDM	**Analog Input 34**
	EVADC_G8CH2			**Analog input channel 2, group 8**
28	AN35	I	D / HighZ / VDDM	**Analog Input 35**
	EVADC_G8CH3			**Analog input channel 3, group 8**
27	AN36/P40.6	I	S / HighZ / VDDM	**Analog Input 36**
	SENT_SENT6A			**Receive input channel 6**
	EVADC_G8CH4			**Analog input channel 4, group 8**
	CCU61_CCPOS1B			**Hall capture input 1**
	EDSADC_EDS1PA			**Positive analog input channel 1, pin A**
26	AN37/P40.7	I	S / HighZ / VDDM	**Analog Input 37**
	SENT_SENT7A			**Receive input channel 7**
	EVADC_G8CH5			**Analog input channel 5, group 8**
	CCU61_CCPOS1D			**Hall capture input 1**
	EDSADC_EDS1NA			**Negative analog input channel 1, pin A**
25	AN38/P40.8	I	S / HighZ / VDDM	**Analog Input 38**
	SENT_SENT8A			**Receive input channel 8**
	EVADC_G8CH6			**Analog input channel 6, group 8**
	CCU61_CCPOS2B			**Hall capture input 2**
	EDSADC_EDS1PB			**Positive analog input channel 1, pin B**
24	AN39/P40.9	I	S / HighZ / VDDM	**Analog Input 39**
	SENT_SENT9A			**Receive input channel 9**
	EVADC_G8CH7			**Analog input channel 7, group 8**
	CCU61_CCPOS2D			**Hall capture input 2**
	EDSADC_EDS1NB			**Negative analog input channel 1, pin B**

注释：端口引脚P32.0 和P32.1 是双向引脚，具有以下两个功能：

9. 如果将这些引脚用作标准GPIO，则可以使用P32.0 和P32.1 引脚配置表中定义的功能。

10. 如果引脚用作外部MOSFET 的预驱动器（内部DCDC 情况），P32.0 和P32.1 将充当名为VGATE1N 和VGATE1P 的模拟IO。

表 2-80 系统 I/O

Pin	Symbol	Ctrl.	Buffer Type	Function
70	VGATE1N	O	—	**DCDC N ch. MOSFET gate driver output** P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
71	VGATE1P	O	—	**DCDC P ch. MOSFET gate driver output** P32.1 / External Pass Device gate control for EVRC
81	XTAL1	I	XTAL / VEXT	**XTAL pad1** XTAL1. Main Oscillator/PLL/Clock Generator Input.
82	XTAL2	O	XTAL / VEXT	**XTAL pad2** XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT
89	TMS	I	FAST / PD2 / VEXT	**JTAG Module State Machine Control Input**
	DAP1	I/O		**DAP: DAP1 Data I/O**
91	$\overline{\text{TRST}}$	I	FAST / PU2 / VEXT	**JTAG Module Reset/Enable Input**
92	TCK	I	FAST / PD2 / VEXT	**JTAG Module Clock Input**
	DAP0	I		**DAP: DAP0 Clock Input**
96	$\overline{\text{ESR1}}$	I/O	FAST / PU1 / VEXT	**ESR1 Port Pin input - can be used to trigger a reset or an NMI** ESR1: External System Request Reset 1. Default NMI function. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
	PMS_ESR1WKP	I		**ESR1 pin input**
97	$\overline{\text{PORST}}$	I/O	PORST / PD / VEXT	**PORST pin** Power On Reset Input. Additional strong PD in case of power fail.

表 2-80 系统 I/O（续）

Pin	Symbol	Ctrl.	Buffer Type	Function
98	$\overline{\text{ESR0}}$	I/O	FAST / OD / VEXT	**ESR0 Port Pin input - can be used to trigger a reset or an NMI** ESR0: External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
	PMS_ESR0WKP	I		**ESR0 pin input**

表 2-81 电源

Pin	Symbol	Ctrl.	Buffer Type	Function
44	VDDM	I	—	**ADC Analog Power Supply (5V / 3.3V)**
126	VDDP3	I	—	**Flash Power Supply (3.3V)**
42	VAREF1	I	—	**Positive Analog Reference Voltage 1**
53, 54, 55	NC	I	—	**Not connected. These pins are reserved for future extensions and shall not be connected externally**
52	VEVRSB	I	—	**Standby Power Supply (5V / 3.3V) for the Standby SRAM**
10	VDD	I	—	**Digital Core Power Supply (1.25V)**
125	VEXT	I	—	**External Power Supply (5V / 3.3V)**
23	VEXT	I	—	**External Power Supply (5V / 3.3V)**
78	VEXT	I	—	**External Power Supply (5V / 3.3V)**
69	VEXT	I	—	**External Power Supply (5V / 3.3V)**
127	VDD	I	—	**Digital Core Power Supply (1.25V)**
22	VDD	I	—	**Digital Core Power Supply (1.25V)**
79	VDD	I	—	**Digital Core Power Supply (1.25V)**
99	VDD	I	—	**Digital Core Power Supply (1.25V)**
72	VDD	I	—	**Digital Core Power Supply (1.25V)**
E-PAD	VSS	I	—	**Digital Ground (Exposed PAD), VSS**
43	VSSM	I	—	**Analog Ground for VDDM**
41	VAGND1	I	—	**Negative Analog Reference Voltage 1**
80	VSS	I	—	**Oscillator Ground, VSS(OSC)**
83	VEXT	I	—	**Digital Power Supply for Oscillator (shall be supplied with same level as used for VEXT), VEXT(OSC)**

2.6 焊盘框中焊盘的顺序

表2-82 焊盘列表

Number	Pad Name	Pad Type	X	Y	Comment
1	P15.0	FAST / PU1 / VEXT / ES	291978	185148	General-purpose I/O
2	P15.1	FAST / PU1 / VEXT / ES	392976	185148	General-purpose I/O
3	P15.2	FAST / PU1 / VEXT / ES	495972	185148	General-purpose I/O
4	P15.3	FAST / PU1 / VEXT / ES	600930	362646	General-purpose I/O
5	P15.4	FAST / PU1 / VEXT / ES	650934	185148	General-purpose I/O
6	P15.5	FAST / PU1 / VEXT / ES	700938	362646	General-purpose I/O
7	VSS	Vx	750942	185148	Supply Voltage
8	VEXT	Vx	802980	362646	Supply Voltage
9	P15.6	FAST / PU1 / VEXT / ES	852984	185148	General-purpose I/O
10	P15.7	FAST / PU1 / VEXT / ES	902988	362646	General-purpose I/O
11	VSS	Vx	978948	185148	Supply Voltage
12	VDD	Vx	1054494	362646	Supply Voltage
13	P15.8	FAST / PU1 / VEXT / ES	1106532	185148	General-purpose I/O
14	VDDP3	Vx	1158570	362646	Supply Voltage
15	P14.0	FAST / PU1 / VEXT / ES2	1210608	185148	General-purpose I/O
16	P14.1	FAST / PU1 / VEXT / ES2	1262646	362646	General-purpose I/O
17	P14.2	SLOW / PU2 / VEXT / ES	1314684	185148	General-purpose I/O
18	P14.3	SLOW / PU2 / VEXT / ES	1366722	362646	General-purpose I/O
19	P14.4	SLOW / PU2 / VEXT / ES	1418760	185148	General-purpose I/O
20	P14.5	FAST / PU2 / VEXT / ES	1470798	362646	General-purpose I/O
21	P14.6	FAST / PU1 / VEXT / ES	1522836	185148	General-purpose I/O
22	P14.7	SLOW / PU1 / VEXT / ES	1572840	362646	General-purpose I/O

TC36x 引脚定义和功能：焊盘框中焊盘的顺序

表2-82 焊盘列表（续）

Number	Pad Name	Pad Type	X	Y	Comment
23	P14.8	SLOW / PU1 / VEXT / ES	1624293	185148	General-purpose I/O
24	P14.9	LVDS_RX / FAST / PU1 / VEXT / ES	1694340	362646	General-purpose I/O
25	P14.10	LVDS_RX / FAST / PU1 / VEXT / ES	1793340	362646	General-purpose I/O
26	VSS	Vx	1868391	185148	Supply Voltage
27	VEXT	Vx	1924389	362646	Supply Voltage
28	VSS	Vx	1976427	185148	Supply Voltage
29	VEXT	Vx	2028465	362646	Supply Voltage
30	VEXT	Vx	2080503	185148	Supply Voltage
31	VDDP3	Vx	2262501	185148	Supply Voltage
32	VDDP3	Vx	2312505	362646	Supply Voltage
33	VDDP3	Vx	2362509	185148	Supply Voltage
34	VDD	Vx	2442267	362646	Supply Voltage
35	VSS	Vx	2516445	185148	Supply Voltage
36	VDD	Vx	2586627	362646	Supply Voltage
37	VSS	Vx	2654505	185148	Supply Voltage
38	VDD	Vx	2720385	362646	Supply Voltage
39	VSS	Vx	2778876	185148	Supply Voltage
40	P13.0	LVDS_TX / FAST / PU1 / VEXT / ES6	2878884	185148	General-purpose I/O
41	P13.1	LVDS_TX / FAST / PU1 / VEXT / ES6	2977884	185148	General-purpose I/O
42	P13.2	LVDS_TX / FAST / PU1 / VEXT / ES6	3148884	362646	General-purpose I/O
43	P13.3	LVDS_TX / FAST / PU1 / VEXT / ES6	3247884	362646	General-purpose I/O
44	P12.0	SLOW / PU1 / VFLEX / ES	3381597	179145	General-purpose I/O
45	P12.1	SLOW / PU1 / VFLEX / ES	3428595	348147	General-purpose I/O
46	P11.14	SLOW / PU1 / VFLEX / ES	3531933	179145	General-purpose I/O
47	P11.13	SLOW / PU1 / VFLEX / ES	3580191	348147	General-purpose I/O

表2-82 焊盘列表（续）

Number	Pad Name	Pad Type	X	Y	Comment
48	P11.15	SLOW / PU1 / VFLEX / ES	3627189	179145	General-purpose I/O
49	P11.0	RFAST / PU1 / VFLEX / ES	3700593	356643	General-purpose I/O
50	VFLEX	Vx	3749391	185148	Supply Voltage
51	P11.1	RFAST / PU1 / VFLEX / ES	3822795	356643	General-purpose I/O
52	VSS	Vx	3871593	185148	Supply Voltage
53	P11.2	RFAST / PU1 / VFLEX / ES	3944997	362646	General-purpose I/O
54	VDD	Vx	3993795	185148	Supply Voltage
55	P11.4	RFAST / PU1 / VFLEX / ES	4109499	348147	General-purpose I/O
56	VSS	Vx	4196997	185148	Supply Voltage
57	P11.3	RFAST / PU1 / VFLEX / ES	4270401	362646	General-purpose I/O
58	VFLEX	Vx	4319199	185148	Supply Voltage
59	P11.6	RFAST / PU1 / VFLEX / ES	4390803	362646	General-purpose I/O
60	VSS	Vx	4441401	185148	Supply Voltage
61	P11.5	SLOW / RGMII_Input / PU1 / VFLEX / ES	4491099	356643	General-purpose I/O
62	P11.7	SLOW / RGMII_Input / PU1 / VFLEX / ES	4554387	179145	General-purpose I/O
63	P11.9	FAST / RGMII_Input / PU1 / VFLEX / ES	4602285	362646	General-purpose I/O
64	VFLEX	Vx	4652883	185148	Supply Voltage
65	P11.8	SLOW / RGMII_Input / PU1 / VFLEX / ES	4702581	362646	General-purpose I/O
66	P11.10	FAST / RGMII_Input / PU1 / VFLEX / ES	4753179	185148	General-purpose I/O

TC36x 引脚定义和功能：焊盘框中焊盘的顺序

表2-82 焊盘列表（续）

Number	Pad Name	Pad Type	X	Y	Comment
67	P11.11	FAST / RGMII_Input / PU1 / VFLEX / ES	4803777	362646	General-purpose I/O
68	VSS	Vx	4854375	185148	Supply Voltage
69	P11.12	FAST / RGMII_Input / PU1 / VFLEX / ES	4903173	362646	General-purpose I/O
70	P10.0	SLOW / PU1 / VEXT / ES	4979187	185148	General-purpose I/O
71	P10.1	FAST / PU1 / VEXT / ES	5029191	362646	General-purpose I/O
72	P10.2	FAST / PU1 / VEXT / ES	5079195	185148	General-purpose I/O
73	P10.3	FAST / PU1 / VEXT / ES	5129199	362646	General-purpose I/O
74	VSS	Vx	5179203	185148	Supply Voltage
75	VEXT	Vx	5231241	362646	Supply Voltage
76	P10.4	FAST / PU1 / VEXT / ES	5281245	185148	General-purpose I/O
77	VDD	Vx	5331249	362646	Supply Voltage
78	P10.5	SLOW / PU2 / VEXT / ES	5383287	185148	General-purpose I/O
79	P10.7	SLOW / PU1 / VEXT / ES	5435325	362646	General-purpose I/O
80	VSS	Vx	5494005	185148	Supply Voltage
81	P10.6	SLOW / PU2 / VEXT / ES	5595003	185148	General-purpose I/O
82	P10.8	SLOW / PU1 / VEXT / ES	5697999	185148	General-purpose I/O
83	P02.0	FAST / PU1 / VEXT / ES	5801292	291978	General-purpose I/O
84	P02.1	SLOW / PU1 / VEXT / ES	5801292	392976	General-purpose I/O
85	P02.2	FAST / PU1 / VEXT / ES	5801292	495972	General-purpose I/O
86	P02.3	SLOW / PU1 / VEXT / ES	5801292	600966	General-purpose I/O
87	P02.4	FAST / PU1 / VEXT / ES	5801292	700974	General-purpose I/O
88	VSS	Vx	5801292	800982	Supply Voltage

TC36x 引脚定义和功能：焊盘框中焊盘的顺序

表2-82 焊盘列表（续）

Number	Pad Name	Pad Type	X	Y	Comment
89	P02.5	FAST / PU1 / VEXT / ES	5801292	900990	General-purpose I/O
90	P02.6	FAST / PU1 / VEXT / ES	5801292	1000998	General-purpose I/O
91	P02.7	FAST / PU1 / VEXT / ES	5801292	1101006	General-purpose I/O
92	P02.8	SLOW / PU1 / VEXT / ES	5801292	1201014	General-purpose I/O
93	VEXT	Vx	5801292	1301022	Supply Voltage
94	VSS	Vx	5801292	1401030	Supply Voltage
95	VDD	Vx	5801292	1501038	Supply Voltage
96	VDD	Vx	5801292	1601046	Supply Voltage
97	VSS	Vx	5801292	1701054	Supply Voltage
98	VDD	Vx	5801292	1801062	Supply Voltage
99	VSS	Vx	5801292	1902060	Supply Voltage
100	VSS	Vx	5801292	2005056	Supply Voltage
101	VDD	Vx	5623794	2108052	Supply Voltage
102	P00.0	FAST / PU1 / VEXT / ES	5801292	2165049	General-purpose I/O
103	P00.1	SLOW / PU1 / VEXT / ES	5801292	2273540	General-purpose I/O
104	P00.2	SLOW / PU1 / VEXT / ES1	5623794	2328538	General-purpose I/O
105	P00.3	SLOW / PU1 / VEXT / ES1	5801292	2383538	General-purpose I/O
106	P00.4	SLOW / PU1 / VEXT / ES1	5623794	2438536	General-purpose I/O
107	P00.5	SLOW / PU1 / VEXT / ES1	5801292	2493536	General-purpose I/O
108	P00.6	SLOW / PU1 / VEXT / ES1	5623794	2548534	General-purpose I/O
109	P00.7	SLOW / PU1 / VEXT / ES1	5801292	2603534	General-purpose I/O
110	P00.8	SLOW / PU1 / VEXT / ES1	5623794	2658532	General-purpose I/O
111	P00.9	SLOW / PU1 / VEXT / ES1	5801292	2713532	General-purpose I/O
112	P00.10	SLOW / PU1 / VEXT / ES1	5623794	2768530	General-purpose I/O
113	P00.11	SLOW / PU1 / VEXT / ES1	5801292	2823530	General-purpose I/O

TC36x 引脚定义和功能：焊盘框中焊盘的顺序

表2-82 焊盘列表（续）

Number	Pad Name	Pad Type	X	Y	Comment
114	P00.12	SLOW / PU1 / VEXT / ES1	5623794	2878528	General-purpose I/O
115	VSS	Vx	5801292	2933528	Supply Voltage
116	VSS	Vx	5801292	3032626	Supply Voltage
117	VDD	Vx	5801292	3131726	Supply Voltage
118	VDD	Vx	5623794	3186724	Supply Voltage
119	VEXT	Vx	5801292	3285824	Supply Voltage
120	VEXT	Vx	5623794	3340822	Supply Voltage
121	AN43	D / HighZ / VDDM	5801292	3439922	Analog Input 43
122	AN42	D / HighZ / VDDM	5623794	3494920	Analog Input 42
123	AN47	D / HighZ / VDDM	5801292	3549920	Analog Input 47
124	AN46	D / HighZ / VDDM	5623794	3604918	Analog Input 46
125	AN45	D / HighZ / VDDM	5801292	3659918	Analog Input 45
126	AN44	D / HighZ / VDDM	5623794	3714916	Analog Input 44
127	AN39/P40.9	S / HighZ / VDDM	5801292	3879914	Analog Input 39
128	AN38/P40.8	S / HighZ / VDDM	5623794	3934912	Analog Input 38
129	AN37/P40.7	S / HighZ / VDDM	5801292	3989912	Analog Input 37
130	AN36/P40.6	S / HighZ / VDDM	5623794	4044910	Analog Input 36
131	AN35	D / HighZ / VDDM	5801292	4099910	Analog Input 35
132	AN34	D / HighZ / VDDM	5623794	4154908	Analog Input 34
133	AN33/P40.5	S / HighZ / VDDM	5801292	4209908	Analog Input 33
134	AN32/P40.4	S / HighZ / VDDM	5623794	4264906	Analog Input 32
135	AN29	D / HighZ / VDDM	5801292	4319906	Analog Input 29
136	AN28	D / HighZ / VDDM	5623794	4374904	Analog Input 28
137	AN27/P40.3	S / HighZ / VDDM	5801292	4429904	Analog Input 27

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表2-82 焊盘列表（续）

Number	Pad Name	Pad Type	X	Y	Comment
138	AN26/P40.2	S / HighZ / VDDM	5623794	4484902	Analog Input 26
139	AN25/P40.1	S / HighZ / VDDM	5801292	4539902	Analog Input 25
140	AN24/P40.0	S / HighZ / VDDM	5801292	4663300	Analog Input 24
141	AN23	D / HighZ / VDDM	5716440	4748292	Analog Input 23
142	AN22	D / HighZ / VDDM	5593140	4748292	Analog Input 22
143	AN41	D / HighZ / VDDM	5538141	4570794	Analog Input 41
144	AN21	D / HighZ / VDDM	5483142	4748292	Analog Input 21
145	AN40	D / HighZ / VDDM	5428143	4570794	Analog Input 40
146	AN20	D / HighZ / VDDM	5373144	4748292	Analog Input 20
147	AN31	D / HighZ / VDDM	5318145	4570794	Analog Input 31
148	AN19	D / HighZ / VDDM	5263146	4748292	Analog Input 19
149	AN30	D / HighZ / VDDM	5208147	4570794	Analog Input 30
150	AN18	D / HighZ / VDDM	5153148	4748292	Analog Input 18
151	AN17	D / HighZ / VDDM	5098149	4570794	Analog Input 17
152	AN16	D / HighZ / VDDM	5043150	4748292	Analog Input 16
153	AN15	D / HighZ / VDDM	4988151	4570794	Analog Input 15
154	VAGND1	Vx	4933152	4748292	Supply Voltage
155	VAREF1	Vx	4878153	4570794	Supply Voltage
156	VAGND0	Vx	4823154	4748292	Supply Voltage
157	VAREF0	Vx	4768155	4570794	Supply Voltage
158	VSSM	Vx	4713156	4748292	Supply Voltage
159	VDDM	Vx	4658157	4570794	Supply Voltage
160	VSSM	Vx	4603158	4748292	Supply Voltage
161	VDDM	Vx	4548159	4570794	Supply Voltage
162	VSSM	Vx	4369514	4748292	Supply Voltage
163	VDDM	Vx	4314514	4570794	Supply Voltage

TC36x 引脚定义和功能：焊盘框中焊盘的顺序

表2-82 焊盘列表（续）

Number	Pad Name	Pad Type	X	Y	Comment
164	AN14	D / HighZ / VDDM	4259516	4748292	Analog Input 14
165	AN13	D / HighZ / VDDM	4204516	4570794	Analog Input 13
166	AN12	D / HighZ / VDDM	4149518	4748292	Analog Input 12
167	AN11	D / HighZ / VDDM	4094518	4570794	Analog Input 11
168	AN10	D / HighZ / VDDM	4039520	4748292	Analog Input 10
169	AN9	D / HighZ / VDDM	3984520	4570794	Analog Input 9
170	AN8	D / HighZ / VDDM	3929522	4748292	Analog Input 8
171	AN7	D / HighZ / VDDM	3874522	4570794	Analog Input 7
172	AN6	D / HighZ / VDDM	3819524	4748292	Analog Input 6
173	AN5	D / HighZ / VDDM	3764524	4570794	Analog Input 5
174	AN4	D / HighZ / VDDM	3709526	4748292	Analog Input 4
175	AN3	D / HighZ / VDDM	3654526	4570794	Analog Input 3
176	AN2	D / HighZ / VDDM	3599528	4748292	Analog Input 2
177	AN1	D / HighZ / VDDM	3544528	4570794	Analog Input 1
178	AN0	D / HighZ / VDDM	3489530	4748292	Analog Input 0
179	VSS	Vx	3371427	4748292	Supply Voltage
180	VDD	Vx	3293469	4570794	Supply Voltage
181	VSS	Vx	3219507	4748292	Supply Voltage
182	VDD	Vx	3141549	4570794	Supply Voltage
183	VSS	Vx	3067587	4748292	Supply Voltage
184	VDD	Vx	2991789	4570794	Supply Voltage
185	VEVRSB	Vx	2910159	4748292	Supply Voltage
186	VEVRSB	Vx	2858121	4570794	Supply Voltage
187	VSS	Vx	2806083	4748292	Supply Voltage
188	P33.0	SLOW / PU1 / VEVRSB / ES5	2683107	4748292	General-purpose I/O

表2-82 焊盘列表（续）

Number	Pad Name	Pad Type	X	Y	Comment
189	P33.1	SLOW / PU1 / VEVRSB / ES5	2627109	4570794	General-purpose I/O
190	P33.2	SLOW / PU1 / VEVRSB / ES5	2577105	4748292	General-purpose I/O
191	P33.3	SLOW / PU1 / VEVRSB / ES5	2527101	4570794	General-purpose I/O
192	P33.4	SLOW / PU1 / VEVRSB / ES5	2477097	4748292	General-purpose I/O
193	P33.5	SLOW / PU1 / VEVRSB / ES5	2422107	4570794	General-purpose I/O
194	VSS	Vx	2334015	4748292	Supply Voltage
195	VDD	Vx	2258217	4570794	Supply Voltage
196	P33.6	SLOW / PU1 / VEVRSB / ES5	2208519	4748292	General-purpose I/O
197	P33.8	FAST / HighZ / VEVRSB	2158515	4570794	General-purpose I/O
198	P33.7	SLOW / PU1 / VEVRSB / ES5	2108511	4748292	General-purpose I/O
199	VDD	Vx	2059173	4570794	Supply Voltage
200	VSS	Vx	2009475	4748292	Supply Voltage
201	P33.10	FAST / PU1 / VEVRSB / ES5	1954179	4570794	General-purpose I/O
202	P33.9	SLOW / PU1 / VEVRSB / ES5	1903185	4748292	General-purpose I/O
203	P33.11	FAST / PU1 / VEVRSB / ES5	1853181	4570794	General-purpose I/O
204	P33.12	FAST / PU1 / VEVRSB / ES5	1803177	4748292	General-purpose I/O
205	VDD	Vx	1752309	4570794	Supply Voltage
206	VSS	Vx	1684044	4748292	Supply Voltage
207	VEVRSB	Vx	1584036	4748292	Supply Voltage
208	VSS	Vx	1484028	4748292	Supply Voltage

TC36x 引脚定义和功能：焊盘框中焊盘的顺序

表2-82 焊盘列表（续）

Number	Pad Name	Pad Type	X	Y	Comment
209	P33.13	FAST / PU1 / VEVRSB / ES5	1379034	4748292	General-purpose I/O
210	VSS	Vx	1278036	4748292	Supply Voltage
211	VDD	Vx	1178028	4748292	Supply Voltage
212	VEXT	Vx	1078020	4748292	Supply Voltage
213	P32.0	SLOW / PU1 / VEXT / ES	978012	4748292	General-purpose I/O
214	VGATE1N	Vx	878004	4748292	DCDC N ch. MOSFET gate driver output
215	P32.1	SLOW / PU1 / VEXT / ES	777996	4748292	General-purpose I/O
216	VGATE1P	Vx	677988	4748292	DCDC P ch. MOSFET gate driver output
217	VSS	Vx	577980	4748292	Supply Voltage
218	P32.2	SLOW / PU1 / VEXT / ES	477972	4748292	General-purpose I/O
219	P32.3	SLOW / PU1 / VEXT / ES	372978	4748292	General-purpose I/O
220	P32.4	FAST / PU1 / VEXT / ES	269982	4748292	General-purpose I/O
221	P23.0	SLOW / PU1 / VEXT / ES	185148	4596759	General-purpose I/O
222	P23.1	FAST / PU1 / VEXT / ES	185148	4493763	General-purpose I/O
223	VEXT	Vx	362646	4441725	Supply Voltage
224	P23.3	SLOW / PU1 / VEXT / ES	185148	4364199	General-purpose I/O
225	P23.2	SLOW / PU1 / VEXT / ES	362646	4312161	General-purpose I/O
226	P23.5	FAST / PU1 / VEXT / ES	185148	4260123	General-purpose I/O
227	P23.4	FAST / PU1 / VEXT / ES	362646	4208085	General-purpose I/O
228	P22.0	FAST / PU1 / VEXT / ES6	185148	4156047	General-purpose I/O
229	P22.1	FAST / PU1 / VEXT / ES6	362646	4104009	General-purpose I/O
230	P22.2	FAST / PU1 / VEXT / ES6	185148	4048011	General-purpose I/O
231	P22.3	FAST / PU1 / VEXT / ES6	362646	3995973	General-purpose I/O

表2-82 焊盘列表（续）

Number	Pad Name	Pad Type	X	Y	Comment
232	RESERVED	Vx	185148	3943935	Must be bonded to VSS
233	VEXT	Vx	362646	3891897	Supply Voltage
234	VSS	Vx	185148	3839859	Supply Voltage
235	VEXT	Vx	362646	3787821	Supply Voltage
236	VSS	Vx	185148	3735783	Supply Voltage
237	VDD	Vx	362646	3683745	Supply Voltage
238	VSS	Vx	185148	3604815	Supply Voltage
239	VDD	Vx	362646	3523887	Supply Voltage
240	VSS	Vx	185148	3446955	Supply Voltage
241	VDD	Vx	362646	3356172	Supply Voltage
242	VSS	Vx	185148	3306762	Supply Voltage
243	XTAL1	XTAL / VEXT	185148	3149613	XTAL pad1 XTAL1. Main Oscillator/PLL/Clock Generator Input.
244	XTAL2	XTAL / VEXT	185148	3050613	XTAL pad2 XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT
245	VSS	Vx	185148	2893464	Supply Voltage
246	VEXT	Vx	362646	2844054	Supply Voltage
247	VEXT	Vx	362646	2709414	Supply Voltage
248	VSS	Vx	185148	2659374	Supply Voltage
249	P21.0	FAST / PU1 / VEXT / ES	362646	2605338	General-purpose I/O
250	P21.1	FAST / PU1 / VEXT / ES	185148	2551338	General-purpose I/O
251	P21.2	LVDS_RX / FAST / PU1 / VEXT / ES	362646	2476287	General-purpose I/O
252	P21.3	LVDS_RX / FAST / PU1 / VEXT / ES	362646	2377287	General-purpose I/O
253	P21.4	LVDS_TX / FAST / PU1 / VEXT / ES6	362646	2247741	General-purpose I/O
254	P21.5	LVDS_TX / FAST / PU1 / VEXT / ES6	362646	2148741	General-purpose I/O

TC36x 引脚定义和功能：焊盘框中焊盘的顺序

表2-82 焊盘列表（续）

Number	Pad Name	Pad Type	X	Y	Comment
255	P21.6/TDI	FAST / PD / PU2 / VEXT / ES3	185148	2037240	General-purpose I/O PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ.
256	TMS	FAST / PD2 / VEXT	362646	1987236	JTAG Module State Machine Control Input
257	P21.7/TDO	FAST / PU2 / VEXT / ES4	185148	1937232	General-purpose I/O
258	$\overline{\text{TRST}}$	FAST / PU2 / VEXT	362646	1887228	JTAG Module Reset/Enable Input
259	TCK	FAST / PD2 / VEXT	185148	1837224	JTAG Module Clock Input
260	P20.0	FAST / PU1 / VEXT / ES	362646	1787220	General-purpose I/O
261	VSS	Vx	185148	1737216	Supply Voltage
262	VEXT	Vx	362646	1685178	Supply Voltage
263	P20.1	SLOW / PU1 / VEXT / ES	185148	1635174	General-purpose I/O
264	P20.2	S / PU / VEXT	362646	1585170	General-purpose I/O This pin is latched at power on reset release to enter test mode.
265	P20.3	SLOW / PU1 / VEXT / ES	185148	1535166	General-purpose I/O
266	$\overline{\text{ESR1}}$	FAST / PU1 / VEXT	362646	1485162	ESR1 Port Pin input - can be used to trigger a reset or an NMI ESR1: External System Request Reset 1. Default NMI function. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
267	$\overline{\text{PORST}}$	PORST / PD / VEXT	185148	1435158	PORST pin Power On Reset Input. Additional strong PD in case of power fail.

表2-82 焊盘列表（续）

Number	Pad Name	Pad Type	X	Y	Comment
268	$\overline{\text{ESR0}}$	FAST / OD / VEXT	362646	1385154	ESR0 Port Pin input - can be used to trigger a reset or an NMI ESR0: External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
269	VSS	Vx	185148	1312974	Supply Voltage
270	VDD	Vx	362646	1240794	Supply Voltage
271	VSS	Vx	185148	1168614	Supply Voltage
272	VDD	Vx	362646	1096434	Supply Voltage
273	VSS	Vx	185148	1024254	Supply Voltage
274	VDD	Vx	362646	952074	Supply Voltage
275	P20.6	SLOW / PU1 / VEXT / ES	185148	900036	General-purpose I/O
276	P20.7	FAST / PU1 / VEXT / ES	362646	847998	General-purpose I/O
277	P20.8	FAST / PU1 / VEXT / ES	185148	797994	General-purpose I/O
278	P20.9	FAST / PU1 / VEXT / ES	362646	747990	General-purpose I/O
279	VEXT	Vx	185148	697986	Supply Voltage
280	P20.10	FAST / PU1 / VEXT / ES	362646	647982	General-purpose I/O
281	VSS	Vx	185148	597978	Supply Voltage
282	P20.12	FAST / PU1 / VEXT / ES	362646	547974	General-purpose I/O
283	P20.11	FAST / PU1 / VEXT / ES	185148	497970	General-purpose I/O

表2-82 焊盘列表（续）

Number	Pad Name	Pad Type	X	Y	Comment
284	P20.13	FAST / PU1 / VEXT / ES	185148	392976	General-purpose I/O
285	P20.14	FAST / PU1 / VEXT / ES	185148	289980	General-purpose I/O

在第3节“电气规格”的表格中，每当使用术语“相邻焊盘”时，详细定义如图 2-82 所示。此表述也适用于次邻/最近邻焊盘。

为了找出谁在影响目标焊盘上的运行（干扰），必须定义大量活动的近邻焊盘（ACNP）。

寻找近邻焊盘。

焊盘环有四个边：底部、左侧、顶部、右侧。每条边都是有限的，即有两个端点。

每个焊盘都有两个直接（第一个）邻居，除非它位于边缘的末端。在这种情况下，它只有一个相邻焊盘。类似地，每个焊盘都有两个间接（第二个）邻居，除非它或它的第一个邻居位于边缘的末端。我们将这些第一和第二个邻居统称为近邻焊盘。因此每个焊盘都有 2 到 4 个近邻焊盘。

可以按照以下顺序寻找近邻：

1.) 选择目标焊盘并在图 2-82中查找其“X”和“Y”坐标。

2.) 通过计算与选定焊盘的“X”和“Y”距离来找到第一和第二个邻居。图 2-82 按“Y”坐标排序，这可能有助于定位 4 个近邻候选者（如果焊盘靠近边缘，则最终可能有少于 4 个近邻）。

定义活跃焊盘：

如果焊盘当前正在使用并且名称中没有“Vxx”，则表示焊盘活跃。确定活跃的邻近焊盘的数量遵循以下规则：

- 如果第一个邻居是活跃的，那么我们对其进行计数，并检查第二个邻居（在选定焊盘的同一侧）是否活跃。

- 如果第一个邻居不活跃，那么我们就不会检查同一侧的第二个邻居。

2.7 图例

本第 2 章中有关的数据与文件 TC36xpd_IO_Spirit_v1.0.0.1.12.xml 匹配。

Ctrl 列：

I = 输入（对于具有 IOCR 位字段选择 PCx = $0XXX_B$ 的GPIO 端口）

O = 输出（对于 GPIO 端口，“O”在大多数情况下代表端口 HWOUT 功能）

O0 = 带 IOCR 位字段选择的输出 PCx = $1X000_B$

O1 = 带 IOCR 位字段选择的输出 PCx = $1X001_B$ (ALT1)

O2 = 带 IOCR 位字段选择的输出 PCx = $1X010_B$ (ALT2)

O3 = 带 IOCR 位字段选择的输出 PCx = $1X011_B$ (ALT3)

O4 = 带 IOCR 位字段选择的输出 PCx = $1X100_B$ (ALT4)

O5 = 带 IOCR 位字段选择的输出 PCx = $1X101_B$ (ALT5)

O6 = 带 IOCR 位字段选择的输出 PCx = $1X110_B$ (ALT6)

O7 = 带 IOCR 位字段选择的输出 PCx = $1X111_B$ (ALT7)

“缓冲区类型”列：

FAST = 焊盘类 FAST (5V/3.3V)

RFAST = 焊盘类 RFAST (5V/3.3V)

SLOW = 焊盘类 SLOW (5V/3.3V)

LVDS_TX = 焊盘类 LVDS 发送

LVDS_RX = 焊盘类 LVDS 接收

RGMII_Input = 用可控 RGMII 输入缓冲器实现的焊盘。章节 -> '通用端口和 I/O'

S = 焊盘类 S（模拟输入覆盖通用输入）

D = 焊盘类 D （模拟输入）

Porst = Porst 输入焊盘

XTAL1 = XTAL1 输入焊盘

XTAL2 = XTAL2 输入焊盘

PU = 复位期间连接上拉器件（$\overline{PORST}$ = 0）

PU1 = 复位期间连接上拉器件（$\overline{PORST}$ = 0）[1)]

PU2 = 启动和复位期间连接上拉器件，待机模式下为 HighZ

PD = 复位期间连接下拉器件（$\overline{PORST}$ = 0）

PD1 = 在复位期间连接下拉器件 ($\overline{PORST}$ = 0) [1)]

PD2 = 在启动和复位期间连接下拉器件，待机模式下为高阻态

OD = 复位期间开漏（$\overline{PORST}$ = 0）

ES = 支持紧急停止

ES1=ES。ES 可被重用于 VADC ，通过 P00_PCSR 控制

ES2=ES。ES 可以被用于 DXCPL - DAP 通过 CAN 物理层，不能被用于 DXCM - 通过 CAN 消息调试

ES3=ES。如果此引脚用作 TDI 则 ES 可以被用于JTAG 模式。

ES4=ES。ES 可由 JTAG 或三引脚 DAP 模式控制

1）PORST 下拉期间和之后，GPIO（Px.y）的默认状态通过 HWCFG6（P14.4）控制。请另参阅 PMS、HWCFG[6] 章节

ES5=ES。如果实施的话，备用控制器 (SCR) 可以重用 ES。可以通过控制寄存器 P33_PCSR 和 P34_PCSR 禁用重用

ES6=ES。在 LVDS TX 焊盘上，ES 仅在 CMOS 模式下影响焊盘，而不在 LVDS 模式下影响焊盘。因此，仅当 LPCRx.TX_EN 选择 CMOS 模式时，ES 事件中输出才会关闭。

3 电气规格

3.1 参数解释

本节列出的参数部分代表 TC36x 的特性，部分代表其对系统的要求。为了帮助在评估设计时轻松解释参数，它们在“符号”列中用两个字母的缩写标记：

- **CC**
  这些参数表明了控制器参数特性（**C**ontroller **C**haracteristics），这是 TC36x 的一个显著特点，在系统设计中必须加以考虑
- **SR**
  这些参数表明了系统要求（**S**ystem **R**equirements），必须由采用 TC36x 设计的微处理器系统提供。

3.2 绝对最大额定值

超过“绝对最大额定值”所列值的应力可能会对器件造成永久性损坏。这仅仅是一个应力额定值，并不意味着设备在这些条件下或任何其他高于本规格操作部分所示条件的情况下能够正常运行。长时间暴露于绝对最大额定条件可能会影响器件的可靠性。

表 3-1 绝对最大额定值

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Storage Temperature	T_{ST} SR	-65	-	150	°C	upto 65h @ T_J = 150°C
Voltage at V_{DD} power supply pins with respect to V_{SS} 1) 2)	V_{DD} SR	-	-	1.65	V	upto 2.8h
		-	-	1.45	V	upto 72h
Voltage at V_{DDP3} power supply pins with respect to V_{SS}	V_{DDP3} SR	-	-	4.43	V	
Voltage at V_{DDM}, V_{EXT}, V_{FLEX} and V_{EVRSB} power supply pins with respect to V_{SS}	V_{DDM} SR	-	-	6.75	V	upto 2.8h
		-	-	5.6	V	upto 72h
Voltage on all other input pins with respect to V_{SS} 3)	V_{IN} SR	-0.7	-	6.75	V	
Voltage on all analog and class S input pins with respect to V_{SS} 3)	V_{IN} SR	-0.7	-	6.75	V	
Input current on any pin during overload condition 4) 5)	I_{IN} SR	-10	-	10	mA	
Absolute maximum sum of all input circuit currents during overload condition. 4)	ΣI_{IN} SR	-100	-	100	mA	

1) 有效期累计长达2.8小时，脉冲形式跟随电源接通阶段，其中上升和下降时间与系统电容和电感有关。

2) 由于EVRC输出电压在开关关闭阶段振荡， V_{DD}可能降至-0.72V，对于V_{DD}, 输入电平降至关闭阶段的 -0.72V 不会造成任何损坏或可靠性问题。

3) 只要不违反受影响焊盘的过载引脚可靠性部分中定义的时间和电流， 低于 V_{INmin} 的电压就不会对器件可靠性产生影响。

4) 此参数是绝对最大额定值，长时间暴露于绝对最大额定值可能会损坏器件。

5) 指定的最小和最大值表示在运行期间未使用的任何快速、RFast、Slow和 S 级焊盘的输出端出现短路条件时必须维持的电流限值。
这也涵盖了 C_L=200pF 时由于操作切换而产生的输出电流。

3.3 过载时的引脚可靠性

当接收来自高压设备的信号时，低压设备会出现超出其自身 IO 电源规格的过载电流和电压。

下表定义了在满足以下所有条件的情况下不会对可靠性造成任何负面影响的过载条件：

- 不超过过载条件允许的时间间隔（在注释栏中定义）。如果没有定义时间限制，则允许的时间包括“运行寿命小时数”和“非活动寿命小时数”。 **表 3-66** 和 **表3-67** 中的小时数仅作为示例，适用的数字由英飞凌接受的客户资料定义。
- **工作条件**满足
  - 焊盘供电电平
  - 温度

如果引脚电流超出**工作条件** 但在过载参数范围内，则无法再保证此引脚的参数功能符合工作条件中的规定。但在大多数情况下，操作仍可进行，因为参数宽松。

表 3-2 过载参数

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current on any digital pin during overload condition	I_{IN}	-5	-	5	mA	except LVDS pins
		-15 [1]	-	15 [1]	mA	except LVDS pins; limited to max. 20 pulses with 1ms pulse length
Input current on LVDS pin during overload condition	I_{INLVDS}	-3	-	3	mA	
Input current on analog input pin during overload condition	I_{INANA}	-3	-	3	mA	
		-5	-	5	mA	limited to 60h over lifetime
Absolute sum of all analog input currents for analog inputs during overload condition	I_{INSA}	-20	-	20	mA	
Absolute maximum sum of all input circuit currents during overload condition (digital and analog combined)	ΣI_{INS}	-100	-	100	mA	
Signal voltage over/undershoot at GPIOs	V_{OUS}	V_{SS} - 2	-	$V_{EXT/FLEX}$ + 2	V	limited to 60h over lifetime; Valid for non LVDS and analoge pads
Sum of all inactive device pin currents	I_{IDS}	-100	-	100	mA	
Static pin output current	I_{OUT} CC	-	-	2.5	mA	100% duty cycle; output driver = medium
		-	-	5	mA	100% duty cycle; output driver = strong

表 3-2 过载参数（续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overload coupling factor for digital inputs, negative	K_{OVDN} CC	-	-	$3*10^{-4}$		Overload injected on GPIO non LVDS pad and affecting neighbor fast pads; -5mA < I_{IN} < 0mA
		-	-	$2*10^{-3}$		Overload injected on GPIO non LVDS pad and affecting neighbor slow pads VGASTE1N and VGATE1P; -5mA < I_{IN} < 0mA
		-	-	$1*10^{-4}$		Overload injected on GPIO non LVDS pad and affecting neighbor slow pads; -5mA < I_{IN} < 0mA
		-	-	0.8		Overload injected on LVDS RX pad and affecting neighbor LVDS pads
		-	-	0.5		Overload injected on LVDS TX pad and affecting neighbor LVDS pads
Overload coupling factor for digital inputs, positive	K_{OVDP} CC	-	-	$1.5*10^{-3}$		Overload injected on GPIO non LVDS pad and affecting neighbor GPIO non LVDS pads
		-	-	1		Overload injected on LVDS RX pad and affecting neighbor LVDS pads
		-	-	$5*10^{-3}$		Overload injected on LVDS TX pad and affecting neighbor LVDS pads
Overload coupling factor for analog inputs, negative [2]	K_{OVAN} CC	-	-	$1*10^{-4}$		Analog inputs overlaid with slow pads or pull down diagnostics; -5mA < I_{IN} < 0mA
		-	-	$1*10^{-5}$		else; -5mA < I_{IN} < 0mA

表 3-2　　过载参数（续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overload coupling factor for analog inputs, positive [2]	K_{OVAP} CC	-	-	$2*10^{-4}$		Analoge inputs overlaid with slow pads or pull down diagnostics; 0mA < I_{IN} < 5mA
		-	-	$2*10^{-5}$		else; 0mA < I_{IN} < 5mA

1) 降低的 VADC / DSADC 结果精度和 / 或 GPIO 输入电平 (V_{IL}和V_{IH}) 可能与指定参数不同。

2) 模拟输入上的过载耦合是由焊盘、输入多路复用器和周围结构之间的寄生效应引起的。已针对所有通道排列验证了给定的参数。还观察一个引脚与多个通道的多个连接。

3.4 工作条件

为了确保 TC36x 的正确操作和可靠性，不得超过以下工作条件。除非另有说明，以下部分中指定的所有参数均指这些工作条件。

施加到 TC36x 的数字电源电压必须是静态调节电压。

下表中指定的所有参数均指这些工作条件（见下表），除非在注释/测试条件栏中另有说明。

表 3-3 工作条件

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SRI frequency	f_{SRI} SR	-	-	300	MHz	
CPU Frequency (All CPUs)	f_{CPUx} SR	-	-	300	MHz	
PLL0 output frequency	f_{PLL0} SR	20	-	300	MHz	
SPB frequency	f_{SPB} SR	-	-	100	MHz	
FSI2 frequency	f_{FSI2} SR	-	-	300	MHz	
FSI frequency	f_{FSI} SR	20	-	100	MHz	
GTM frequency	f_{GTM} SR	-	-	200	MHz	
STM frequency	f_{STM} SR	-	-	100	MHz	
ERAY frequency	f_{ERAY} SR	-	80	-	MHz	
BBB frequency	f_{BBB} SR	-	-	150	MHz	
VADC frequency	f_{ADC} SR	-	-	160	MHz	
ASCLIN Operating Frequency	$f_{ASCLINx}$ SR	-	-	200	MHz	
CAN frequency	f_{CAN} SR	-	-	80	MHz	
I2C frequency	f_{I2C} SR	-	-	100	MHz	
Operating MSC Frequency	f_{MSC} SR	-	-	200	MHz	
PLL1 output frequency from PER PLL	f_{PLL1} SR	20	-	320	MHz	
PLL2 output frequency from PER PLL	f_{PLL2} SR	20	-	200	MHz	
QSPI Frequency	f_{QSPI} SR	-	-	200	MHz	
MCANH frequency	f_{MCANH} CC	-	-	100	MHz	
GETH frequency	f_{GETH} CC	100	-	150	MHz	
Ambient Temperature	T_A SR	-40	-	125	°C	valid for all SAK products
		-40	-	150	°C	valid for all SAL products with package
		-40	-	170	°C	valid for all SAL products without package

表 3-3 工作条件（续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Junction Temperature	T_J SR	-40	-	150	°C	valid for all SAK products
		-40	-	170	°C	valid for all SAL products
Core Supply Voltage	V_{DD} SR	1.125 [1]	1.25	1.375 [2]	V	
ADC analog supply voltage	V_{DDM} SR	2.97	5.0	5.5 [3]	V	
Digital external supply voltage for pads and EVR	V_{EXT} SR	4.5	5.0	5.5 [3]	V	Nominal 5V Pad / Port Pin supply range. 5V pad parameters are valid.
		2.97	3.3	3.63	V	Nominal 3.3V Pad / Port Pin supply range with VDDP3 supplied externally and EVR33 inactive. 3.3V pad parameters are valid.
		3.6	-	4.5	V	Flash configured in cranking mode; Flash read operation with reduced performance. EVR33 active in low voltage mode. 3.3V pad parameters are valid.
		2.97	-	3.6	V	Incase EVR33 is active, Flash configured in sleep mode and execution switched to RAM. 3.3V pad parameters are valid.
Digital supply voltage for Flex port	V_{FLEX} SR	2.97	-	4.0	V	3.3V pad parameters are valid
		4.5	5.0	5.5 [3]	V	5V pad parameters are valid
Digital supply voltage for Flash	V_{DDP3} SR	2.97	3.3	3.63 [4]	V	
		2.6	-	3.63	V	Flash configured in cranking mode; Flash read operation with reduced performance.
Digital ground voltage	V_{SS} SR	0	-	-	V	
Analog ground voltage for V_{DDM}	V_{SSM} CC	-0.1	0	0.1	V	

表 3-3 工作条件（续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital external supply voltage for EVR and during Standby mode	V_{EVRSB} SR	2.97 5)	-	5.5	V	
Voltage to ensure defined pad states	V_{DDPPA} CC	1.3 6)	-	-	V	

1) 对于V_{DD}，当 1.08V ≤ V_{DD} < 1.125V 时，仍可进行操作，参数宽松。

2) 允许过冲电压至 1.69V，但累计持续时间不得超过 2 小时，ADC 精度降低且漏电增加。

3) 允许过冲电压至 6.5V，但累计持续时间不得超过 2 小时，ADC 精度降低且漏电增加。

4) 允许过冲电压至 4.29V，但累计持续时间不得超过 2 小时，ADC 精度降低且漏电增加。

5) V_{EVRSB} 供电电压在待机模式下可降至 2.6V。V_{EVRSB} 上需接一个 100nF 电容供电引脚。

6) 当 VEXT 达到此电平时，HWCFG[6] 引脚被锁存，并且在端口引脚处激活上拉或三态。

供电电压随时间的限制

$V_{EXT/FLEX/DDM}$ 电源轨的最大工作电压在整个使用寿命期间受到限制。

下面的电压曲线就是一个例子。为了满足质量和可靠性目标，特定应用的电压分布需要经过英飞凌科技公司的调整和批准。

表 3-4 电压曲线示例

$V_{EXT/FLEX/DDM}$=	Duration [h]
5.4 V < $V_{EXT/FLEX/DDM}$ ≤ 5.5 V	≤ 5% of lifetime
5.15 V < $V_{EXT/FLEX/DDM}$ ≤ 5.4 V	≤ 15% of lifetime
4.85 V < $V_{EXT/FLEX/DDM}$ ≤ 5.15 V	≤ 60% of lifetime
4.6 V < $V_{EXT/FLEX/DDM}$ ≤ 4.85 V	≤ 15% of lifetime
4.5 V < $V_{EXT/FLEX/DDM}$ ≤ 4.6 V	≤ 5% of lifetime

在整个使用寿命期间，V_{DD} 电源轨的最大工作电压是有限的。

下面的电压曲线就是一个例子。为了满足质量和可靠性目标，特定应用的电压分布需要经过英飞凌科技公司的调整和批准。

表 3-5 电压曲线示例

V_{DD}=	Duration [h]
1.325 V < V_{DD} ≤ 1.375 V	≤ 5% of lifetime
1.275 V < V_{DD} ≤ 1.325 V	≤ 15% of lifetime
1.225 V < V_{DD} ≤ 1.275 V	≤ 60% of lifetime
1.175 V < V_{DD} ≤ 1.225 V	≤ 15% of lifetime
1.125 V < V_{DD} ≤ 1.175V	≤ 5% of lifetime

3.5 5 V / 3.3 V 可切换焊盘

焊盘类别为慢速 GPIO 和快速 GPIO，支持汽车级 (AL) 或 TTL 级 (TTL) 操作。参数是为 AL 操作定义的，并在 TTL 操作中降低。

表 3-6 $\overline{\text{PORST}}$ 焊盘

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
$\overline{\text{PORST}}$ pad Output current	I_{PORST} CC	13	-	-	mA	V_{EXT} = 2.97V; V_{PORST} = 0.9V
Spike filter always blocked pulse duration	t_{SF1} CC	-	-	80	ns	
Spike filter pass-through blocked pulse duration	t_{SF2} CC	260	-	-	ns	without additional PORST Digtial Filter active (PORSTDF = 0).
Input hysteresis [1]	HYS CC	0.055 * V_{EXT}	-	-	V	non of the neighbor pads are used as output;TTL (degraded, used for CIF)
Pull-down current [2]	I_{PDL} CC	-	-	|130|	µA	V_{IH}; TTL (degraded, used for CIF)
		|15|	-	-	µA	V_{IL}; TTL (degraded, used for CIF)
Input leakage current	I_{OZ} CC	-450	-	450	nA	TJ≤150°C ; (0.1 * V_{EXT}) < V_{IN} < (0.9 * V_{EXT})
		-500	-	500	nA	TJ≤150°C ;else
		-900	-	900	nA	TJ≤170°C ; (0.1 * V_{EXT}) < V_{IN} < (0.9 * V_{EXT})
		-950	-	950	nA	TJ≤170°C ; else
Input high voltage level	V_{IH} SR	1.4	-	-	V	TTL (degraded, used for CIF); V_{EXT} = 2.97V
		2.0	-	-	V	TTL; V_{EXT} = 4.5V
Input low voltage level	V_{IL} SR	-	-	0.5	V	TTL (degraded, used for CIF); V_{EXT} = 2.97V
		-	-	0.8	V	TTL; V_{EXT} = 4.5V
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added

1) 实施滞回是为了避免亚稳态和由于内部地弹而引起的切换。不能保证它能抑制由于外部系统噪声而引起的切换。

2) 下拉电阻的值通过表 VADC 5V 中的参数 R_{MDD} 定义。

表 3-7 快速 5V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} CC	125	225	320	Ohm	medium driver; $I_{OH/OL}$ = 2mA
		31	55	80	Ohm	strong driver; $I_{OH/OL}$ = 8mA
Rise / Fall time [1) 2)]	t_{RF} CC	1.6	-	3.2	ns	C_L = 25pF; driver = strong sharp edge; from 0.2 * $V_{EXT/FLEX/EVRSB}$ to 0.8 * $V_{EXT/FLEX/EVRSB}$
		4+0.55*C_L	4+0.75*C_L	12+1.0*C_L	ns	driver = medium; C_L≤200pF
		1.0+0.18* C_L	2.5+0.27* C_L	5.0+0.35* C_L	ns	driver = strong edge = medium; C_L≤200pF
		0.5+0.08* C_L	0.5+0.11* C_L	1.0+0.17* C_L	ns	driver = strong edge = sharp ; C_L≤200pF
Asymmetry of sending	t_{TX_ASYM} CC	-1	-	1	ns	valid for all data rates excluding clock tolerance
Input frequency	f_{IN} CC	-	-	160	MHz	
Input hysteresis [3)]	HYS CC	0.09 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; AL
		0.075 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; TTL
		75	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current [4)]	I_{PUH} CC	|30|	-	-	µA	V_{IH}; AL or TTL
		-	-	|130|	µA	V_{IL}; AL or TTL
Pull-down current [5)]	I_{PDL} CC	-	-	|130|	µA	V_{IH}; AL or TTL
		|30|	-	-	µA	V_{IL}; AL
		|28|	-	-	µA	V_{IL}; TTL

表 3-7 快速 5V GPIO （续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current	I_{OZ} CC	-1100	-	1100	nA	$T_J \leq 150°C$; (0.1 * $V_{EXT/FLEX/EVRSB}$) < V_{IN} < (0.9 * $V_{EXT/FLEX/EVRSB}$)
		-2500	-	2500	nA	$T_J \leq 150°C$; (0.1 * $V_{EXT/FLEX}$) < V_{IN} < (0.9 * $V_{EXT/FLEX}$) ; LVDS_TX / Fast pad type
		-6000	-	6000	nA	$T_J \leq 150°C$; LVDS_RX / Fast pad type ; else
		-3200	-	3200	nA	$T_J \leq 150°C$; LVDS_TX / Fast pad type ; else
		-1500	-	1500	nA	$T_J \leq 150°C$; else
		-2000	-	2000	nA	$T_J \leq 170°C$; (0.1 * $V_{EXT/FLEX/EVRSB}$) < V_{IN} < (0.9 * $V_{EXT/FLEX/EVRSB}$)
		-4000	-	4000	nA	$T_J \leq 170°C$; (0.1 * $V_{EXT/FLEX}$) < V_{IN} < (0.9 * $V_{EXT/FLEX}$) ; LVDS_TX / Fast pad type
		-13500	-	13500	nA	$T_J \leq 170°C$; LVDS_RX / Fast pad type ; else
		-5100	-	5100	nA	$T_J \leq 170°C$; LVDS_TX / Fast pad type ; else
		-2500	-	2500	nA	$T_J \leq 170°C$; else
Input high voltage level	V_{IH} SR	0.7 * $V_{EXT/FLEX/EVRSB}$	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} SR	-	-	0.44 * $V_{EXT/FLEX/EVRSB}$	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	V_{ILD} SR	-50	-	50	mV	max. variation of 1ms; $V_{EXT/FLEX/EVRSB}$ = constant; AL
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) 在公式中，需要以 pF 为单位输入 C_L 的值才能获得 ns 为单位的结果。

2) 上升/下降时间定义为焊盘供电电压的 10% - 90%。

3) 实施滞回是为了避免亚稳态和由于内部地弹而引起的切换。不能保证它能抑制由于外部系统噪声而引起的切换。

4) 上拉电阻的值通过表 VADC 5V 中的参数R_{MDU}定义。

5) 下拉电阻的值通过表 VADC 5V 中的参数 R_{MDD}定义。

表 3-8 快速 3.3V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} CC	125	225	320	Ohm	medium driver; $I_{OH/OL}$ = 2mA
		31	55	80	Ohm	strong driver; $I_{OH/OL}$ = 8mA
Rise / Fall time [1) 2)]	t_{RF} CC	1.6	-	4.5	ns	C_L = 25pF; driver = strong sharp edge; from 0.2 * $V_{EXT/FLEX/EVRSB}$ to 0.8 * $V_{EXT/FLEX/EVRSB}$
		-	-	5	ns	C_L = 25pF; driver = strong sharp edge; from 0.8V to 2.0V (RMII)
		2+0.57*C_L	5.5+0.75* C_L	10+1.25* C_L	ns	driver = medium; C_L≤200pF
		1.5+0.18* C_L	1.5+0.28* C_L	8+0.4*C_L	ns	driver = strong edge = medium; C_L≤200pF
		0.75+0.08 *C_L	0.75+0.11 *C_L	2.5+0.21* C_L	ns	driver = strong edge = sharp ; C_L≤200pF
Asymmetry of sending	t_{TX_ASYM} CC	-1	-	1	ns	valid for all data rates excluding clock tolerance
Input frequency	f_{IN} CC	-	-	160	MHz	
Input hysteresis [3)]	HYS CC	0.055 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; AL
		0.09 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; TTL
		0.055 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output;TTL (degraded, used for CIF)
		125	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL

表 3-8 快速 3.3V GPIO （续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pull-up current [4]	I_{PUH} CC	|17|	-	-	µA	V_{IH}; AL and TTL (degraded, used for CIF)
		|11|	-	-	µA	V_{IH}; TTL
		-	-	|80|	µA	V_{IL}; AL and TTL and TTL (degraded, used for CIF)
Pull-down current [5]	I_{PDL} CC	-	-	|105|	µA	V_{IH}; AL and TTL (degraded, used for CIF)
		-	-	|115|	µA	V_{IH}; TTL
		|19|	-	-	µA	V_{IL}; AL and TTL
		|15|	-	-	µA	V_{IL}; TTL (degraded, used for CIF)
Input leakage current	I_{OZ} CC	-1100	-	1100	nA	$T_J \leq 150°C$; $(0.1 * V_{EXT/FLEX/EVRSB}) < V_{IN} < (0.9 * V_{EXT/FLEX/EVRSB})$
		-2500	-	2500	nA	$T_J \leq 150°C$; $(0.1 * V_{EXT/FLEX}) < V_{IN} < (0.9 * V_{EXT/FLEX})$; LVDS_TX / Fast pad type
		-6000	-	6000	nA	$T_J \leq 150°C$; LVDS_RX / Fast pad type ; else
		-3200	-	3200	nA	$T_J \leq 150°C$; LVDS_TX / Fast pad type ; else
		-1500	-	1500	nA	$T_J \leq 150°C$; else
		-2000	-	2000	nA	$T_J \leq 170°C$; $(0.1 * V_{EXT/FLEX/EVRSB}) < V_{IN} < (0.9 * V_{EXT/FLEX/EVRSB})$
		-4000	-	4000	nA	$T_J \leq 170°C$; $(0.1 * V_{EXT/FLEX}) < V_{IN} < (0.9 * V_{EXT/FLEX})$; LVDS_TX / Fast pad type
		-13500	-	13500	nA	$T_J \leq 170°C$; LVDS_RX / Fast pad type ; else
		-5100	-	5100	nA	$T_J \leq 170°C$; LVDS_TX / Fast pad type ; else
		-2500	-	2500	nA	$T_J \leq 170°C$; else

表 3-8 快速 3.3V GPIO （续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input high voltage level	V_{IH} SR	0.7 * $V_{EXT/FLEX/EVRSB}$	-	-	V	AL
		2.0	-	-	V	TTL
		1.4	-	-	V	TTL (degraded, used for CIF)
Input low voltage level	V_{IL} SR	-	-	0.42 * $V_{EXT/FLEX/EVRSB}$	V	AL
		-	-	0.8	V	TTL
		-	-	0.5	V	TTL (degraded, used for CIF)
Input low/high voltage level	V_{ILH} SR	1.0	-	1.9	V	RGMII; no hysteresis available
Input low threshold variation	V_{ILD} SR	-33	-	33	mV	max. variation of 1ms; $V_{EXT/FLEX/EVRSB}$ = constant; AL
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) 在公式中，需要以 pF 为单位输入 C_L 的值才能获得 ns 为单位的结果。

2) 上升/下降时间定义为焊盘供电电压的 10% - 90%。

3) 实施滞回是为了避免亚稳态和由于内部地弹而引起的切换。不能保证它能抑制由于外部系统噪声而引起的切换。

4) 上拉电阻的值通过表 VADC 5V 中的参数R_{MDU}定义。

5) 下拉电阻的值通过表 VADC 5V 中的参数 R_{MDD} 定义。

表 3-9 慢速 5V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} CC	125	225	320	Ohm	medium driver; $I_{OH/OL}$ = 2mA
Rise / Fall time [1) 2)]	t_{RF} CC	4+0.55*C_L	4+0.75*C_L	12+1*C_L	ns	driver = medium edge = medium ; C_L≤200pF
		1.5+0.25* C_L	2.5+0.40* C_L	7+0.55*C_L	ns	driver = medium edge = sharp ; C_L≤200pF
Asymmetry of sending	t_{TX_ASYM} CC	-1	-	1	ns	valid for all data rates excluding clock tolerance
Input frequency	f_{IN} CC	-	-	160	MHz	

表 3-9 慢速 5V GPIO （续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input hysteresis [3]	HYS CC	0.09 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; AL
		0.075 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; TTL
		75	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current [4]	I_{PUH} CC	|30|	-	-	µA	V_{IH};AL or TTL; exept VGATE1P; except VGATE1N and T_J > 150°C
		-	-	|130|	µA	V_{IL}; AL or TTL; exept VGATE1P; except VGATE1N and T_J > 150°C
Pull-down current [5]	I_{PDL} CC	-	-	|130|	µA	V_{IH}; AL or TTL
		|30|	-	-	µA	V_{IL}; AL
		|28|	-	-	µA	V_{IL}; TTL
Input leakage current	I_{OZ} CC	-300	-	300	nA	T_J ≤ 150°C; (0.1 * $V_{EXT/FLEX/EVRSB}$) < V_{IN} < (0.9 * $V_{EXT/FLEX/EVRSB}$)
		-400	-	400	nA	T_J ≤ 150°C; else
		-600	-	600	nA	T_J ≤ 170°C; (0.1 * $V_{EXT/FLEX/EVRSB}$) < V_{IN} < (0.9 * $V_{EXT/FLEX/EVRSB}$)
		-750	-	750	nA	T_J ≤ 170°C; else
		-18000	-	18000	nA	P32.0 and P32.1;T_J≤150°C
		-38000	-	38000	nA	P32.0 and P32.1;T_J≤170°C
Input high voltage level	V_{IH} SR	0.7 * $V_{EXT/FLEX/EVRSB}$	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} SR	-	-	0.44 * $V_{EXT/FLEX/EVRSB}$	V	AL
		-	-	0.8	V	TTL

表 3-9 慢速 5V GPIO （续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low threshold variation	V_{ILD} SR	-50	-	50	mV	max. variation of 1ms; $V_{EXT/FLEX/EVRSB}$ = constant; AL
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) 在公式中，需要以 pF 为单位输入 C_L 的值才能获得 ns 为单位的结果。

2) 上升/下降时间定义为焊盘供电电压的 10% - 90%。

3) 实施滞回是为了避免亚稳态和由于内部地弹而引起的切换。不能保证它能抑制由于外部系统噪声而引起的切换。

4) 上拉电阻的值通过表 VADC 5V 中的参数R_{MDU}定义。

5) 下拉电阻的值通过表 VADC 5V 中的参数 R_{MDD} 定义。

表 3-10 慢速 3.3V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} CC	125	225	320	Ohm	medium driver; $I_{OH/OL}$ = 2mA
Rise / Fall time [1) 2)]	t_{RF} CC	2+0.57*C_L	5.5+0.75* C_L	10+1.25* C_L	ns	driver = medium edge = medium ; C_L≤200pF
		2+0.30*C_L	3.5+0.50* C_L	5+0.70*C_L	ns	driver = medium edge = sharp ; C_L≤200pF
Asymmetry of sending	t_{TX_ASYM} CC	-1	-	1	ns	valid for all data rates excluding clock tolerance
Input frequency	f_{IN} CC	-	-	160	MHz	
Input hysteresis [3)]	HYS CC	0.055 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; AL
		0.09 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; TTL
		0.055 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output;TTL (degraded, used for CIF)
		125	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL

表 3-10 慢速 3.3V GPIO （续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pull-up current [4]	I_{PUH} CC	|17|	-	-	µA	V_{IH}; AL and TTL (degraded, used for CIF); exept VGATE1P; except VGATE1N and T_J > 150°C
		|11|	-	-	µA	V_{IH}; TTL; exept VGATE1P; except VGATE1N and T_J > 150°C
		-	-	|80|	µA	V_{IL}; AL and TTL and TTL (degraded, used for CIF); exept VGATE1P; except VGATE1N and T_J > 150°C
Pull-down current [5]	I_{PDL} CC	-	-	|105|	µA	V_{IH}; AL and TTL (degraded, used for CIF)
		-	-	|115|	µA	V_{IH}; TTL
		|19|	-	-	µA	V_{IL}; AL and TTL
		|15|	-	-	µA	V_{IL}; TTL (degraded, used for CIF)
Input leakage current	I_{OZ} CC	-300	-	300	nA	T_J ≤ 150°C; (0.1 * $V_{EXT/FLEX/EVRSB}$) < V_{IN} < (0.9 * $V_{EXT/FLEX/EVRSB}$)
		-400	-	400	nA	T_J ≤ 150°C; else
		-600	-	600	nA	T_J ≤ 170°C; (0.1 * $V_{EXT/FLEX/EVRSB}$) < V_{IN} < (0.9 * $V_{EXT/FLEX/EVRSB}$)
		-750	-	750	nA	T_J ≤ 170°C; else
		-18000	-	18000	nA	P32.0 and P32.1; T_J≤150°C
		-38000	-	38000	nA	P32.0 and P32.1; T_J≤170°C
Input high voltage level	V_{IH} SR	0.7 * $V_{EXT/FLEX/EVRSB}$	-	-	V	AL
		2.0	-	-	V	TTL
		1.4	-	-	V	TTL (degraded, used for CIF)

表 3-10 慢速 3.3V GPIO （续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage level	V_{IL} SR	-	-	0.42 * $V_{EXT/FLEX/EVRSB}$	V	AL
		-	-	0.8	V	TTL
		-	-	0.5	V	TTL (degraded, used for CIF)
Input low/high voltage level	V_{ILH} SR	1.0	-	1.9	V	RGMII; no hysteresis available
Input low threshold variation	V_{ILD} SR	-33	-	33	mV	max. variation of 1ms; $V_{EXT/FLEX/EVRSB}$ = constant; AL
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) 在公式中，需要以 pF 为单位输入 C_L 的值才能获得 ns 为单位的结果。

2) 上升/下降时间定义为焊盘供电电压的 10% - 90%。

3) 实施滞回是为了避免亚稳态和由于内部地弹而引起的切换。不能保证它能抑制由于外部系统噪声而引起的切换。

4) 上拉电阻的值通过表 VADC 5V 中的参数R_{MDU}定义。

5) 下拉电阻的值通过表 VADC 5V 中的参数 R_{MDD} 定义。

表 3-11 RFast 5V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} CC	125	225	320	Ohm	medium driver; $I_{OH/OL}$ = 2mA
		31	55	80	Ohm	strong driver; $I_{OH/OL}$ = 8mA
Rise / Fall time [1) 2)]	t_{RF} CC	1.6	-	3.2	ns	C_L = 25pF; driver = strong sharp edge; from 0.2 * V_{FLEX} to 0.8 * V_{FLEX}
		4+0.55*C_L	4+0.75*C_L	12+1.0*C_L	ns	driver = medium; C_L≤200pF
		1.0+0.18* C_L	2.5+0.27* C_L	5.0+0.35* C_L	ns	driver = strong edge = medium; C_L≤200pF
		0.5+0.08* C_L	0.5+0.11* C_L	1.0+0.17* C_L	ns	driver = strong edge = sharp ; C_L≤200pF
Asymmetry of sending	t_{TX_ASYM} CC	-0.5	-	0.5	ns	valid for all data rates excluding clock tolerance

表 3-11 RFast 5V GPIO （续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{IN} CC	-	-	160	MHz	
Input hysteresis [3]	HYS CC	0.09 * V_{FLEX}	-	-	V	non of the neighbor pads are used as output; AL
		0.075 * V_{FLEX}	-	-	V	non of the neighbor pads are used as output; TTL
		75	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current [4]	I_{PUH} CC	|30|	-	-	µA	V_{IH}; AL or TTL
		-	-	|130|	µA	V_{IL}; AL or TTL
Pull-down current [5]	I_{PDL} CC	-	-	|130|	µA	V_{IH}; AL or TTL
		|30|	-	-	µA	V_{IL}; AL
		|28|	-	-	µA	V_{IL}; TTL
Input leakage current	I_{OZ} CC	-1700	-	1700	nA	$T_J \leq 150°C$; (0.1 * V_{FLEX}) < V_{IN} < (0.9 * V_{FLEX})
		-2100	-	2100	nA	$T_J \leq 150°C$; else
		-3000	-	3000	nA	$T_J \leq 170°C$; (0.1 * V_{FLEX}) < V_{IN} < (0.9 * V_{FLEX})
		-4000	-	4000	nA	$T_J \leq 170°C$; else
Input high voltage level	V_{IH} SR	0.7 * V_{FLEX}	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} SR	-	-	0.44 * V_{FLEX}	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	V_{ILD} SR	-50	-	50	mV	max. variation of 1ms; V_{FLEX} = constant; AL
Pin capacitance	C_{IO} CC	-	2	3.5	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) 在公式中，需要以 pF 为单位输入 C_L 的值才能获得 ns 为单位的结果。

2) 上升/下降时间定义为焊盘供电电压的 10% - 90%。

3) 实施滞回是为了避免亚稳态和由于内部地弹而引起的切换。不能保证它能抑制由于外部系统噪声而引起的切换。

4) 上拉电阻的值通过表 VADC 5V 中的参数R_{MDU}定义。

5) 下拉电阻的值通过表 VADC 5V 中的参数 R_{MDD} 定义。

表 3-12 RFast 3.3V 焊盘

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} CC	8	20	30	Ohm	Driver = RGMII; $I_{OH/OL}$ = 8mA
		125	225	320	Ohm	medium driver; $I_{OH/OL}$ = 2mA
		31	55	80	Ohm	strong driver; $I_{OH/OL}$ = 8mA
Input Duty Cycle	f_D SR	47.5	50	52.5		
Rise / Fall time [1) 2)]	t_{RF} CC	1.6	-	4.5	ns	C_L = 25pF; driver = strong sharp edge; from 0.2 * V_{FLEX} to 0.8 * V_{FLEX}
		-	-	5	ns	C_L = 25pF; driver = strong sharp edge; from 0.8V to 2.0V (RMII)
		-	-	1	ns	Driver = RGMII; from 20%V to 80%V; C_L=15pF
		2+0.57*C_L	5.5+0.75* C_L	10+1.25* C_L	ns	driver = medium; C_L≤200pF
		1.5+0.18* C_L	1.5+0.28* C_L	8+0.4*C_L	ns	driver = strong edge = medium; C_L≤200pF
		0.75+0.08 *C_L	0.75+0.11 *C_L	2.5+0.21* C_L	ns	driver = strong edge = sharp ; C_L≤200pF
Asymmetry of sending	t_{TX_ASYM} CC	-0.4	-	0.4	ns	valid for all data rates excluding clock tolerance
Input frequency	f_{IN} CC	-	-	160	MHz	

表 3-12 RFast 3.3V 焊盘（续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input hysteresis [3]	HYS CC	0.055 * V_{FLEX}	-	-	V	non of the neighbor pads are used as output; AL
		0.09 * V_{FLEX}	-	-	V	non of the neighbor pads are used as output; TTL
		0.055 * V_{FLEX}	-	-	V	non of the neighbor pads are used as output;TTL (degraded, used for CIF)
		125	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current [4]	I_{PUH} CC	|17|	-	-	µA	V_{IH}; AL and TTL (degraded, used for CIF)
		|11|	-	-	µA	V_{IH}; TTL
		-	-	|80|	µA	V_{IL}; AL and TTL and TTL (degraded, used for CIF)
Pull-down current [5]	I_{PDL} CC	-	-	|105|	µA	V_{IH}; AL and TTL (degraded, used for CIF)
		-	-	|115|	µA	V_{IH}; TTL
		|19|	-	-	µA	V_{IL}; AL and TTL
		|15|	-	-	µA	V_{IL}; TTL (degraded, used for CIF)
Input leakage current	I_{OZ} CC	-1700	-	1700	nA	$T_J \leq 150°C$; (0.1 * V_{FLEX}) < V_{IN} < (0.9 * V_{FLEX})
		-2100	-	2100	nA	$T_J \leq 150°C$; else
		-3000	-	3000	nA	$T_J \leq 170°C$; (0.1 * V_{FLEX}) < V_{IN} < (0.9 * V_{FLEX})
		-4000	-	4000	nA	$T_J \leq 170°C$; else
Input high voltage level	V_{IH} SR	0.7 * V_{FLEX}	-	-	V	AL
		2.0	-	-	V	TTL
		1.4	-	-	V	TTL (degraded, used for CIF)

表 3-12 RFast 3.3V 焊盘（续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage level	V_{IL} SR	-	-	0.42 * V_{FLEX}	V	AL
		-	-	0.8	V	TTL
		-	-	0.5	V	TTL (degraded, used for CIF)
Input low threshold variation	V_{ILD} SR	-33	-	33	mV	max. variation of 1ms; V_{FLEX} = constant; AL
Pin capacitance	C_{IO} CC	-	2	3.5	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) 在公式中，需要以 pF 为单位输入 C_L 的值才能获得 ns 为单位的结果。

2) 上升/下降时间定义为焊盘供电电压的 10% - 90%。

3) 实施滞回是为了避免亚稳态和由于内部地弹而引起的切换。不能保证它能抑制由于外部系统噪声而引起的切换。

4) 上拉电阻的值通过表 VADC 5V 中的参数R_{MDU}定义。

5) 下拉电阻的值通过表 VADC 5V 中的参数 R_{MDD} 定义。

表 3-13 S 类 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{IN} CC	-	-	160	MHz	
Input hysteresis [1]	HYS CC	0.09 * V_{DDM}	-	-	V	non of the neighbor pads are used as output; AL
		0.075 * V_{DDM}	-	-	V	non of the neighbor pads are used as output; TTL
		75	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current [2]	I_{PUH} CC	|30|	-	-	µA	V_{IH}; AL or TTL
		-	-	|130|	µA	V_{IL}; AL or TTL
Pull-down current [3]	I_{PDL} CC	-	-	|130|	µA	V_{IH}; AL or TTL
		|30|	-	-	µA	V_{IL}; AL
		|28|	-	-	µA	V_{IL}; TTL

表 3-13 S 类 5V （续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current	I_{OZ} CC	-150	-	150	nA	$T_J \leq$ 150°C; else
		-300	-	300	nA	$T_J \leq$ 150°C; PDD option available, or AltRef option available and EDSADC channel connected
		-300	-	300	nA	$T_J \leq$ 170°C; else
		-600	-	600	nA	$T_J \leq$ 170°C; PDD option available, or AltRef option available and EDSADC channel connected
Input high voltage level	V_{IH} SR	0.7 * V_{DDM}	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} SR	-	-	0.44 * V_{DDM}	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	V_{ILD} SR	-50	-	50	mV	max. variation of 1ms; V_{DDM} = constant; AL
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) 实施滞回是为了避免亚稳态和由于内部地弹而引起的切换。不能保证它能抑制由于外部系统噪声而引起的切换。

2) 上拉电阻的值通过表 VADC 5V 中的参数R_{MDU}定义。

3) 下拉电阻的值通过表 VADC 5V 中的参数 R_{MDD}定义。

表 3-14 D类

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current	I_{OZ} CC	-150	-	150	nA	$T_J \leq 150°C$; else
		-300 [1]	-	300 [1]	nA	$T_J \leq 150°C$; PDD option available, or AltRef option available and EDSADC channel connected
		-300	-	300	nA	$T_J \leq 170°C$; else
		-600 [2]	-	600 [2]	nA	$T_J \leq 170°C$; PDD option available, or AltRef option available and EDSADC channel connected
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added

1) 对于 AN11，需要添加 100 nA。

2) 对于 AN11，需要添加 200 nA。

表 3-15 ADC 基准焊盘

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current for V_{AREF}	I_{OZ2} CC	-1	-	1	µA	$T_J \leq 150°C$; $V_{AREF} < V_{DDM}$; used for EVADC
		-2	-	2	µA	$T_J \leq 170°C$; $V_{AREF} < V_{DDM}$; used for EVADC
		-3.5	-	3.5	µA	$T_J \leq 150°C$; $V_{AREF} \leq V_{DDM}$+50mV; used for EVADC
		-7	-	7	µA	$T_J \leq 170°C$; $V_{AREF} \leq V_{DDM}$+50mV; used for EVADC
		-2	-	2	µA	$T_J \leq 150°C$; $V_{AREF} < V_{DDM}$; used for EDSADC
		-4	-	4	µA	$T_J \leq 170°C$; $V_{AREF} < V_{DDM}$; used for EDSADC
		-6	-	6	µA	$T_J \leq 150°C$; $V_{AREF} \leq V_{DDM}$+50mV; used for EDSADC
		-12	-	12	µA	$T_J \leq 170°C$; $V_{AREF} \leq V_{DDM}$+50mV; used for EDSADC

表 3-16 Slow 焊盘驱动器模式选择

PDx.2	PDx.1	PDx.0	Port Functionality	Driver Setting
X	X	0	Speed grade 1	medium sharp edge (sm)
X	X	1	Speed grade 2	medium medium edge (m)

表 3-17 Fast 焊盘驱动器模式选择

PDx.2	PDx.1	PDx.0	Port Functionality	Driver Setting
X	0	0	Speed grade 1	Strong sharp edge (ss)
X	0	1	Speed grade 2	Strong medium edge (sm)
X	1	0	Speed grade 3	medium (m)
X	1	1	Speed grade 4	Reserved, do not use this combination

表 3-18 RFast 焊盘驱动器模式选择

PDx.2	PDx.1	PDx.0	Port Functionality	Driver Setting
X	0	0	Speed grade 1	Strong sharp edge (ss)
X	0	1	Speed grade 2	Strong medium edge (sm)
X	1	0	Speed grade 3	medium (m)
X	1	1	Speed grade 4	RGMII function is active

3.6 高性能 LVDS 焊盘

该 LVDS 焊盘类型用于新型 TC36x 的高速芯片到芯片通信接口。它由一个LVDS焊盘和一个快速焊盘组成。

对于所有 LVDS 参数，C_L = 2.5 pF。

表 3-19 LVDS - IEEE 标准 LVDS 通用链路（GPL）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output impedance	R_0 CC	40	-	140	Ohm	V_{cm} = 1.0 V and 1.4 V
Rise time (20% - 80%)	t_{rise20} CC	-	-	0.75 [1]	ns	Z_L = 100 Ohm ±20% @2pF external load
Output differential voltage [2]	V_{OD} CC	240	-	330	mV	R_T = 100 Ohm ±1%; LPCRx.VDIFFADJ=00
		280	-	370	mV	R_T = 100 Ohm ±1%; LPCRx.VDIFFADJ=01
		320	-	410	mV	R_T = 100 Ohm ±1%; LPCRx.VDIFFADJ=10
		380	-	500	mV	RT = 100 Ohm ± 1%; LPCRx.VDIFFADJ=11; Multi slave operation
Output voltage high	V_{OH} CC	-	-	1475	mV	RT = 100 Ohm +/- 1% VDIFFADJ=00 and 01
		-	-	1500	mV	RT = 100 Ohm ± 1% VDIFFADJ=10 and 11
Output voltage low	V_{OL} CC	925	-	-	mV	RT = 100 Ohm ± 1% VDIFFADJ=00 and 01
		900	-	-	mV	RT = 100 Ohm +/- 1% VDIFFADJ=10 and 11
Output offset (Common mode) voltage	V_{OS} CC	1125	-	1275	mV	RT = 100 Ohm ± 1%
Input voltage range	V_I SR	0	-	1600	mV	Driver ground potential difference < 925 mV; R_T = 100 Ohm ±10%
		0	-	2400	mV	Driver ground potential difference < 925 mV; R_T = 100 Ohm ±20%
Input differential threshold	V_{idth} SR	-100	-	100	mV	Driver ground potential difference < 900 mV; VDIFFADJ=10 and 11
		-100	-	-	mV	Driver ground potential difference < 925 mV; VDIFFADJ=00 and 01
Receiver differential input impedance	R_{in} CC	80	-	120	Ohm	V_I ≤ 2400 mV

表 3-19 LVDS - IEEE 标准 LVDS 通用链路 (GPL) （续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output differential voltage Sleep Mode [3]	V_{ODSM} CC	-5	-	20	mV	RT = 100 Ohm ± 20%; LPCRx.VDIFFADJ=xx
Delta output impedance	$dR0$ SR	-	-	10	%	V_{cm} = 1.0 V and 1.4 V
Change in VOS between 0 and 1	$dVOS$ CC	-	-	25	mV	R_T = 100 Ohm ±1%
Change in Vod between 0 and 1	$dVod$ CC	-	-	25	mV	R_T = 100 Ohm ±1%
Pad set-up time	t_{SET_LVDS} CC	-	10	13	µs	
Duty cycle	t_{duty} CC	45	-	55	%	

1) t_{rise20} = 0.75ns + (C_L - 2)[pF]*20ps，C_L 定义外部负载。

2) 潜在的对IEEE 标准 1596.3 的违反是为了新的多从站支持的特点，符合 IEEE 标准 1596.3LPCRx.VDIFFADJ 必须配置为 01。

3) Tx的共模电压得以维持。

注释：驱动器接地电位的差异定义为驱动器-接收器电位差，在比较驱动器输出电压电平和接收器输入传输信号的电压电平时，可能会导致电压偏移。

*注释：表"LVDS - IEEE 标准 LVDS 通用链路 (GPL)"中的R_T作为 IEEE Std 1596.3-1996 图3-5 中的接收器终端电阻，并在**图3-1** 中由R_{in}或R_T=100 Ohm表示，但不能同时出现。如果在注释/测试条件栏中提到R_T，则始终以**图3-1** 中的内部电阻R_{in}作为选定项。*

启动后默认=CMOS功能

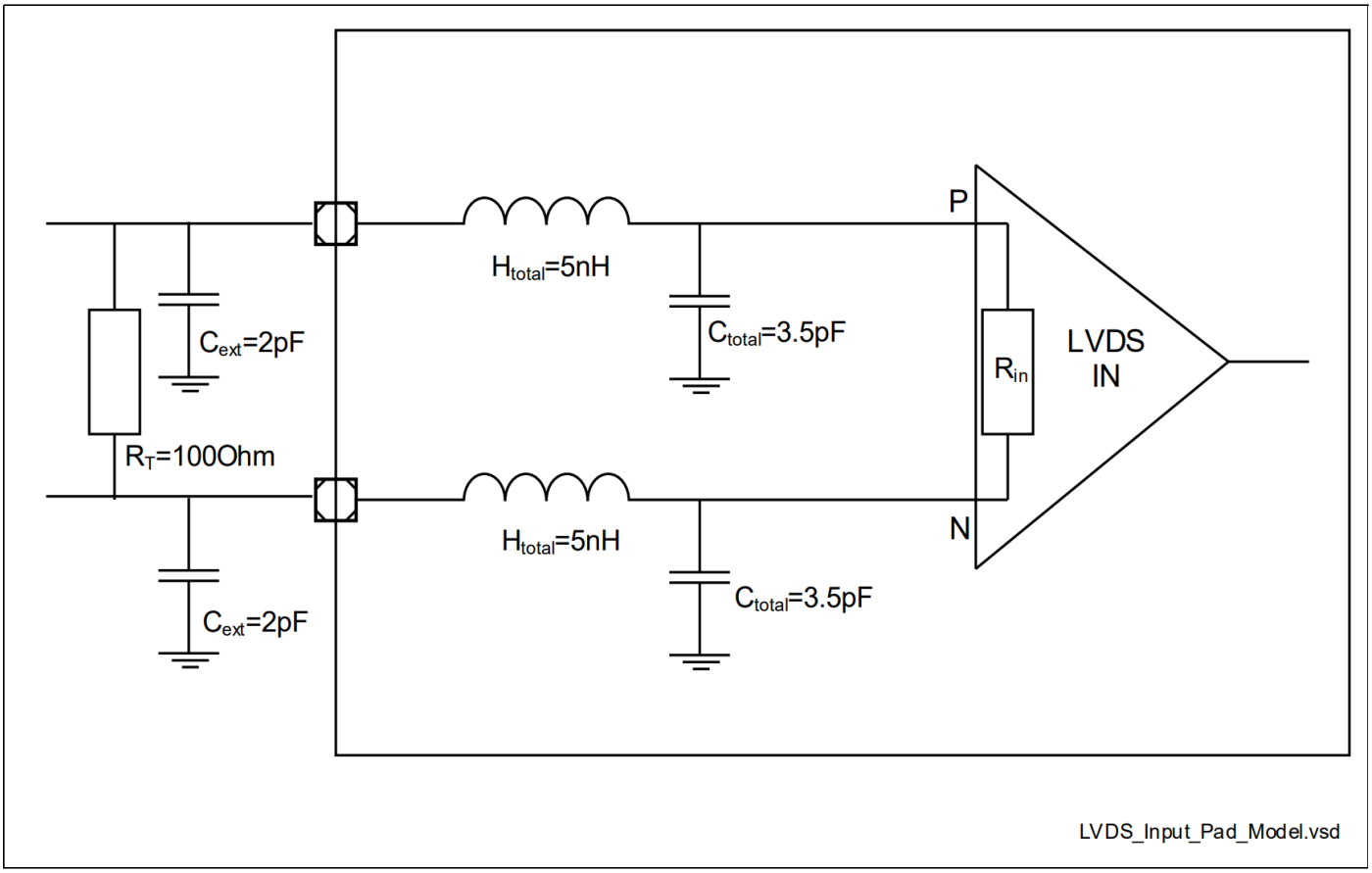


图 3-1 LVDS 焊盘输入模型

3.7 VADC 参数

转换器结果的准确性取决于基准电压范围。下表中的参数适用于 (V_{AREF} - V_{AGND}) >= 4.5 V 的基准电压范围。如果基准电压范围低于 4.5 V k 倍（例如 3.3 V），则精度参数将增加 1.1/k 倍（例如 1.1 × 4.5 / 3.3 = 1.5）。

供电电压V_{DDM}上的噪声会影响转换。精度（误差）参数定义为供电电压纹波在 10 MHz 以内低于 20 mVpp（在 10 MHz 以上低于 5 mVpp）。

数字功能与模拟输入重叠会影响准确性。

总计不可调整误差（TUE）的定义是无噪音的。总体偏差取决于TUE和EN_{RMS}（取决于噪声分布）。示例：对于 4 sigma 的噪声分布且EN_{RMS} = 1.0，附加峰峰值噪声误差为±(4 × 1.0) = 8 LSB_{12}。

快速比较操作以 10 位值执行。

降噪功能通过增加额外的转换步骤来改善结果。因此，转换时间也相应增加（对于1、3或7个步骤，每个步骤的转换时间分别为 4 × t_{ADCI} + 3 × t_{ADC} ）。

表 3-20 VADC 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
EVADC IVR output voltage	V_{DDK} CC	1.15	-	1.35	V	Measured at low temperature.
Deviation of IVR output voltage V_{DDK}	dV_{DDK} CC	-2	-	2	%	Based on device-specific value
Analog reference voltage [1]	V_{AREF} SR	4.5	5.0	V_{DDM} + 0.05	V	4.5 V ≤ V_{DDM} ≤ 5.5 V
		2.97	3.3	V_{DDM} + 0.05	V	2.97 V ≤ V_{DDM} < 4.5 V
Analog reference ground	V_{AGND} SR	V_{SSM}	V_{SSM}	V_{SSM}	V	V_{SSM} and V_{AGND} are connected together
Analog input voltage range	V_{AIN} SR	V_{AGND}	-	V_{AREF}	V	V_{AIN} is limited by the respective pad supply voltage; see pin configuration (buffer type)
Converter reference clock	f_{ADCI} SR	16	40	53.33	MHz	4.5 V ≤ V_{DDM} ≤ 5.5 V
		16	20	26.67	MHz	2.97 V ≤ V_{DDM} < 4.5 V
Total Unadjusted Error [2] [3]	TUE CC	-4	-	4	LSB	12-bit resolution for primary/secondary groups, 10-bit resolution for fast compare channels
INL Error [2]	EA_{INL} CC	-3	-	3	LSB	
DNL error [2] [4]	EA_{DNL} CC	-1	-	3	LSB	
Gain Error [2]	EA_{GAIN} CC	-3.5	-	3.5	LSB	
Offset Error [2] [3]	EA_{OFF} CC	-4	-	4	LSB	
RMS Noise [2] [5] [6]	EN_{RMS} CC	-	0.5	0.8	LSB	Noise reduction level 3
		-	0.5	1.0	LSB	Standard conversion

表 3-20 VADC 5V （续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reference input charge consumption per conversion (from V_{AREF}) [7) 8) 9)]	Q_{CONV} CC	-	-	20	pC	V_{AIN} = 0 V (worst case), precharging disabled
		-	-	10	pC	V_{AIN} = 0 V (worst case), precharging enabled, V_{DDM} - 5% < V_{AREF} < V_{DDM} + 50 mV
Switched capacitance of an analog input	C_{AINS} CC	-	2.5	3.4	pF	Input buffer disabled
Analog input charge consumption [10)]	Q_{AINS} CC	-	-	3.5	pC	Primary groups and fast compare channels; V_{AIN} = V_{AREF}; V_{DDM} = 5.0 V; input buffer enabled; T_J ≤ 150°C
		-	-	3.8	pC	Primary groups and fast compare channels; V_{AIN} = V_{AREF}; V_{DDM} = 5.0 V; input buffer enabled; T_J > 150°C
		-	-	4.4	pC	Secondary groups; V_{AIN} = V_{AREF}; V_{DDM} = 5.0 V; input buffer enabled; T_J ≤ 150 °C
		-	-	4.8	pC	Secondary groups; V_{AIN} = V_{AREF}; V_{DDM} = 5.0 V; input buffer enabled; T_J > 150°C

表 3-20 VADC 5V （续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Sampling time	t_S SR	100	-	-	ns	Primary group or fast compare channel, 4.5 V ≤ V_{DDM} ≤ 5.5 V; input buffer disabled
		300	-	-	ns	Primary group or fast compare channel, 4.5 V ≤ V_{DDM} ≤ 5.5 V; input buffer enabled
		500	-	-	ns	Secondary group, 4.5 V ≤ V_{DDM} ≤ 5.5 V; input buffer disabled
		700	-	-	ns	Secondary group, 4.5 V ≤ V_{DDM} ≤ 5.5 V; input buffer enabled
		200	-	-	ns	Primary Group or fast compare channel, 2.97 V ≤ V_{DDM} < 4.5 V; input buffer disabled
		400	-	-	ns	Primary group or fast compare channel, 2.97 V ≤ V_{DDM} < 4.5 V; input buffer enabled
		1000	-	-	ns	Secondary group, 2.97 V ≤ V_{DDM} < 4.5 V; input buffer disabled
		1200	-	-	ns	Secondary group, 2.97 V ≤ V_{DDM} < 4.5 V; input buffer enabled
Sampling time for calibration	t_{SCAL} SR	50	-	-	ns	4.5 V ≤ V_{DDM} ≤ 5.5 V
		100	-	-	ns	2.97 V ≤ V_{DDM} < 4.5 V
Input buffer switch-on time	t_{BUF} CC	-	0.4	1	µs	
Wakeup time	t_{WU} CC	-	0.1	0.2	µs	Fast standby mode
		-	1.6	3	µs	Slow standby mode
Broken wire detection delay against V_{AREF}	t_{BWR} CC	-	100	-	cycles	Result above 80% of full scale range, analog input buffer disabled
Broken wire detection delay against V_{AGND}	t_{BWG} CC	-	100	-	cycles	Result below 10% of full scale range, analog input buffer disabled
Converter diagnostics unit resistance [11]	R_{CSD} CC	45	-	75	kOhm	
Converter diagnostics voltage accuracy	dV_{CSD} CC	-10	-	10	%	Percentage refers to V_{DDM}

表 3-20 VADC 5V （续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Resistance of the multiplexer diagnostics pull-up device	R_{MDU} CC	30	-	42	kOhm	0 V ≤ V_{IN} ≤ 0.9* V_{DDM}, Automotive Levels
		56	-	78	kOhm	0 V ≤ V_{IN} ≤ 0.9* V_{DDM}, TTL Levels
Resistance of the multiplexer diagnostics pull-down device	R_{MDD} CC	43	-	58	kOhm	0.1*V_{DDM} ≤ V_{IN} ≤ V_{DDM}, Automotive level
		18	-	25	kOhm	0.1*V_{DDM} ≤ V_{IN} ≤ V_{DDM}, TTL level
Resistance of the pull-down test device	R_{PDD} CC	-	-	0.3	kOhm	Measured at pad input voltage V_{IN} = V_{DDM} / 2.

1) 这些限制适用于标准基准输入以及备用基准输入。
2) 该参数取决于基准电压范围和电源纹波，请参阅简介。
   最坏情况下的组合误差是 TUE 和 EN_{RMS} 的算术组合。
   测试是在完成启动校准后禁用后校准的情况下进行的。
3) 映射到 SLOW 类型焊盘的模拟输入会影响精度。此参数的值以 3 LSB_{12}为单位递增。
4) 单调性特性，校准时不会漏码。
5) 参数 EN_{RMS}指的是 1 sigma 分布。
6) 映射到 SLOW 类型焊盘的模拟输入 RMS 噪声（EN_{RMS}）最高可达 2 LSB_{12} （启用 DC/DC 软开关）。
7) 对于降低的参考电压 VAREF < 3.375V，消耗的电荷 QCONV 会减少 k2 = VAREF [V] / 3.375。对于降低的参考电压 4.5V < VAREF ≤ 3.375V，QCONV 不会降低。
8) 当 BWD（断线检测）处于活动状态时，最大电荷增加 15 pC。
9) 快速比较通道仅消耗主/次组电荷的 1/3。
10) 对于具有叠加数字 GPIO 或 PDD 功能的模拟输入，该值增加 1 pC。
11) 使用至少 1.1 µs 的采样时间以确保测试电压正确稳定。

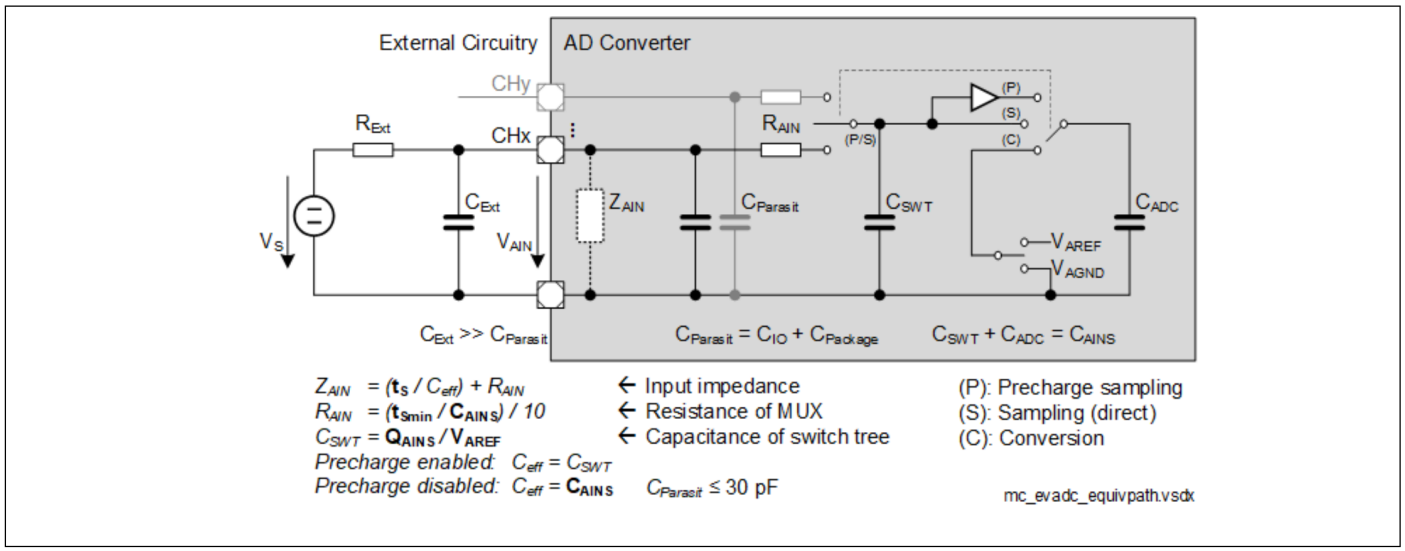


图 3-2 模拟输入等效电路

3.8 DSADC 参数

DSADC 参数仅对电压范围 4.5 V <= V_{DDM} <= 5.5 V 有效。

这些参数描述产品特性，不包括外部电路。如无明确定义，这些值适用于结温T_J <= 150°C 的情况。

校准针对增益因子 1 和 2 指定，校准值参考这些设置。

信噪比 (SNR) 针对差分输入进行指定。对于单端工作模式，信噪比会降低 6 dB。对于准差分模式（即使用V_{CM}），当增益 = 1 时，信噪比会降低 6dB，当增益 = 2 时，信噪比会降低 3dB。

表 3-21 DSADC 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Common mode voltage bias resistance	R_{BIAS} CC	105	130	155	kOhm	On-chip variation ≤ ±2.5%.
Positive reference voltage	V_{AREF} SR	4.5	-	V_{DDM} + 0.05	V	
Reference ground voltage	V_{AGND} SR	V_{SSM}	-	V_{SSM}	V	V_{SSM} and V_{AGND} are connected together
Reference load current	I_{REF} CC	-	10	12	µA	Per modulator
		-	-	14	µA	Per modulator, T_J>150°C
Common mode voltage accuracy [1]	dV_{CM} CC	-100	-	100	mV	Deviation from selected voltage
Analog input voltage range	V_{DSIN} SR	V_{SSM}	-	2 * V_{DDM}	V	Differential; V_{DSxP} - V_{DSxN}
		V_{SSM}	-	V_{DDM}	V	Single ended
Input current [2]	I_{RMS} CC	7	10	13	µA	Exact value (±1%) available in UCB; valid for gain = 1 and f_{MOD} = 26.7 MHz
On-chip modulator clock frequency	f_{MOD} SR	16	-	40	MHz	
Gain error [3] [4]	ED_{GAIN} CC	-0.2 [5]	±0.1 [5]	0.2 [5]	%	T_J≤150°C; Target, calibrated, V_{AREF} constant after calibration; f_{MOD} = 26.67 MHz
		-	±0.25	-	%	T_J>150°C; V_{AREF} constant after calibration; f_{MOD} = 26.67 MHz
		-1	-	1	%	Calibrated once; f_{MOD} = 26.67 MHz
		-2.5	-	2.5	%	Uncalibrated; f_{MOD} = 26.67 MHz

表 3-21 DSADC 5V （续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DC offset error [3]	ED_{OFF} CC	-5 [5]	-	5 [5]	mV	Calibrated; f_{MOD} = 26.67 MHz
		-10	-	10	mV	Calibrated once; f_{MOD} = 26.67 MHz
		-30	-	30	mV	Uncalibrated; f_{MOD} = 26.67 MHz
Signal-Noise Ratio for differential input signals [2][6][7]	SNR CC	80	-	-	dB	T_J≤150°C; f_{PB} = 30 kHz; f_{MOD} = 26.67 MHz
		78	-	-	dB	T_J≤150°C; f_{PB} = 50 kHz; f_{MOD} = 26.67 MHz
		74	-	-	dB	T_J≤150°C; f_{PB} = 100 kHz; f_{MOD} = 26.67 MHz
Signal-Noise Ratio degradation	$DSNR$ CC	-	-	3	dB	T_J>150°C; Resulting Signal-Noise Ratio value is SNR - DSNR
Spurious-free dynamic range [3]	$SFDR$ CC	60	-	-	dB	f_{MOD} = 26.67 MHz
Output sampling rate	f_D CC	3.906	-	300	kHz	16 MHz / 4096, without integrator
Pass band	f_{PB} CC	1.302	-	100	kHz	Output data rate: $f_D = f_{PB}$ * 3; without integrator
		1.302	-	10	kHz	Output data rate: $f_D = f_{PB}$ * 6; without integrator
Pass band ripple	df_{PB} CC	-0.08	-	0.08	dB	FIR filters enabled
Stop band attenuation	SBA CC	40	-	-	dB	$0.5 f_D$ ..... $1.0 f_D$
		45	-	-	dB	$1.0 f_D$ ..... $1.5 f_D$
		50	-	-	dB	$1.5 f_D$ ..... $2.0 f_D$
		55	-	-	dB	$2.0 f_D$ ..... $2.5 f_D$
		60	-	-	dB	$2.5 f_D$ ... OSR/2 f_D
DC compensation factor	DCF CC	-3	-	-	dB	$10^{-5} f_D$, offset compensation filter enabled (FCFGMx.OCEN = 001_B)
Modulator settling time	t_{MSET} CC	-	-	20	µs	After switching on, voltage regulator already running

1) 在具有叠加 GPIO 功能的引脚上，由于 T_J > 150°C 时的漏电流，最大限值最多增加 25 mV 。

2) 有关详细信息，请参阅用户手册章节。

3) 此参数在 f_{MOD} 定义的范围内有效。

4) 如果采用相同的校准策略，不同 EDSADC 通道之间的增益不匹配误差在 ±0.5% 以内

5) 如果温度变化 >20°C，则需要重新校准

6) 这些值对于模拟增益因子 1 有效，每增加一个增益因子，减去 3 dB。

7) 对于单端输入信号和增益 1，SNR 降低 6 dB。

3.9 MHz 振荡器

OSC_XTAL 用作精确的时钟源。OSC_XTAL 支持 16 MHz 至 40 MHz 外部晶振。还支持陶瓷谐振器。

表 3-22 OSC_XTAL

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current at XTAL1	I_{IX1} CC	-70	-	70	µA	V_{IN}>0V ; V_{IN}<V_{EXT}
Oscillator frequency	f_{OSC} SR	4	-	40	MHz	Direct Input Mode selected, if shaper is not bypassed
		16	-	40	MHz	External Crystal Mode selected
Oscillator start-up time	t_{OSCS} CC	-	-	3 [1]	ms	20MHz ≤ f_{OSC} and 8pF load capacitance
Input voltage at XTAL1 [2]	V_{IX} SR	-0.7	-	V_{EXT} + 0.5	V	If shaper is not bypassed
Input amplitude (peak to peak) at XTAL1	V_{PPX} SR	0.3*V_{EXT}	-	V_{EXT} + 1.0	V	If shaper is not bypassed; f_{OSC} > 25MHz
		0.35*V_{EXT}	-	V_{EXT} + 1.0	V	If shaper is not bypassed; f_{OSC} ≤ 25MHz
Internal load capacitor	C_{L0} CC	1.30	1.40	1.55	pF	enabled via bit OSCCON.CAP0EN
Internal load capacitor	C_{L1} CC	3.05	3.35	3.70	pF	enabled via bit OSCCON.CAP1EN
Internal load capacitor	C_{L2} CC	7.85	8.70	9.55	pF	enabled via bit OSCCON.CAP2EN
Internal load capacitor	C_{L3} CC	12.05	13.35	14.65	pF	enabled via bit OSCCON.CAP3EN
Internal load stray capacitor between XTAL1 and XTAL2	C_{XINTS} CC	1.15	1.20	1.25	pF	
Internal load stray capacitor between XTAL1 and ground	C_{XTAL1} CC	-	2.5	4	pF	
Duty cycle at XTAL1 [3]	DC_{X1} SR	35	-	65	%	V_{XTAL1} = 0.5*V_{PPX}
Absolute RMS jitter at XTAL1 [3]	J_{ABSX1} SR	-	-	28	ps	10 KHz to f_{OSC}/2
Slew rate at XTAL1 [3]	SR_{XTAL1} SR	0.3	-	-	V/ns	Maximum 30% difference between rising and falling slew rate

1) t_{OSCS}定义为从振荡器模式设置为外部晶振模式的时刻开始，直到振荡在 XTAL1 处达到 0.3 * VEXT 的幅度。该值取决于所用外部晶振的频率。对于更快的晶振频率，该值会减小。

2) 对于电源 (V_{EXT} < 5.3V V_{IX}) 最小可低至 -0.9V。对于 XTAL1，低至 -0.9V 的输入电平不会导致使用外部晶振时损坏或出现可靠性问题。

3) XTAL1 的方波输入信号。

注释：强烈建议测量最终目标系统（布局）中的振荡裕度（负阻），以确定振荡器运行的最佳参数。请参考晶振或陶瓷谐振器供应商指定的限制。

3.10 备用时钟

备用时钟提供了替代时钟源。

表 3-23 备用时钟

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Back-up clock accuracy before trimming	f_{BACKUT} CC	70	100	130	MHz	V_{EXT}≥2.97V
Back-up clock accuracy after trimming [1]	f_{BACKT} CC	98	100	102	MHz	V_{EXT}≥2.97V
Standby clock	f_{SB} CC	25	70	110	kHz	V_{EXT}≥2.97V

1) 通过每 2 ms定期调整温度和电压漂移，可以实现短期调整，从而满足 LIN 通信所需的精度，最高温度可达 125 °C

3.11 温度传感器

表3-24 DTS PMS

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time for each conversion [1]	t_M CC	-	-	2.7	ms	Measured from cold power-on reset release
Calibration reference accuracy	T_{CALACC} CC	-1	-	1	°C	calibration points @ T_J=-40°C and T_J=127°C
Accuracy over temperature range	T_{NL} CC	-2	-	2	°C	T_{CALACC} has to be added in addition
DTS temperature range	T_{SR} SR	-40	-	170	°C	

1) 热复位后，t_M 不会重新启动，而是从上次转换开始测量。

表 3-25 DTS 核心

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time for each conversion [1]	t_M CC	-	-	2.7	ms	Measured from cold power-on reset release
Temperature difference between on chip temperature sensors	ΔT CC	-3	-	3	°C	
Calibration reference accuracy	T_{CALACC} CC	-2	-	2	°C	calibration points @ T_J=-40°C and T_J=127°C
Accuracy over temperature range	T_{NL} CC	-2	-	2	°C	T_{CALACC} has to be added in addition
DTS temperature range	T_{SR} SR	-40	-	170	°C	

1) 热复位后，t_M 不会重新启动，而是从上次转换开始测量。

3.12 电源电流

下面定义的总电源电流由漏电流和开关分量组成。

应用相关值通常低于下表给出的值，并且取决于客户的系统运行条件（例如热连接或使用的应用配置）。

下表中参数的工作条件为：

实际（现实）功率模式定义了以下条件：

- T_J = 150 °C
- f_{SRI} = f_{CPUx} = 300 MHz
- f_{GTM} = 200 MHz
- f_{SPB} = f_{STM} = f_{BAUD1} = f_{BAUD2} = $f_{ASCLINx}$ = 100 MHz
- V_{DD} = 1.275 V
- V_{DDP3} / FLEX = 3.366 V
- $V_{EXT / EVRSB}$ = V_{DDM} = 5.1 V
- 所有核心都激活，包括两个锁步核（IPC =0.6）
- 以下外设处于非活动状态：HSM、以太网、PSI5、I2C、FCE 和 MTU

最大功率模式定义了以下条件：

- T_J = 150 °C
- f_{SRI} = f_{CPUx} = 300 MHz
- f_{GTM} = 200 MHz
- f_{SPB} = f_{STM} = f_{BAUD1} = f_{BAUD2} = $f_{ASCLINx}$ = 100 MHz
- V_{DD} = 1.375 V
- V_{DDP3} / FLEX = 3.63 V
- $V_{EXT / EVRSB}$ = V_{DDM} = 5.5 V
- 所有核心都激活，包括两个锁步核（IPC =0.6）
- 以下外设未激活：GETH、FCE 和 MTU

表 3-26 电流消耗

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
∑ Sum of I_{DD} core and peripheral supply currents (incl. $I_{DDPORST}$ + ∑ I_{DDCx0} + ∑ I_{DDCxx} + I_{DDGTM} + I_{DDSB})	I_{DDRAIL} CC	-	-	650	mA	max power pattern
		-	-	500	mA	real power pattern
I_{DD} core current during active power-on reset (PORST pin held low). Leakage current of core domain. [1]	$I_{DDPORST}$ CC	-	-	95	mA	V_{DD} = 1.275V; T_J=125°C
		-	-	166	mA	V_{DD} = 1.275V; T_J=150°C
		-	-	230	mA	V_{DD} = 1.275V; T_J=165°C

表 3-26 电流消耗（续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
∑ Sum of I_{DDP3} 3.3 V supply currents	$I_{DDP3RAIL}$ CC	-	-	45	mA	max power pattern incl. Flash read current and Dflash programming current.
		-	-	36 [2]	mA	real power pattern incl. Flash read current and Dflash programming current.
∑ Sum of external I_{EXT} supply currents (incl. $I_{EXTFLEX}$+I_{EVRSB}+$I_{EXTLVDS}$)	$I_{EXTRAIL}$ CC	-	-	44	mA	max power pattern
		-	-	34	mA	real power pattern
I_{EXT} and I_{FLEX} supply current	$I_{EXTFLEX}$ CC	-	-	18 [3]	mA	real power pattern with port activity absent; PORST output inactive.
I_{EVRSB} supply current [1]	I_{EVRSB} CC	-	-	8.5	mA	real power pattern; PMS/EVR module current considered without SCR and Standby RAM during RUN mode.
∑ Sum of external I_{DDM} supply currents (incl. $I_{DDMEVADC}$+$I_{DDMEDSADC}$)	I_{DDM} CC	-	-	27	mA	real power pattern; sum of currents of EDSADC and EVADC modules
∑ Sum of all currents (incl. $I_{EXTRAIL}$+$I_{DDMRAIL}$+$I_{DDx3RAIL}$+I_{DD})	I_{DDTOT} CC	-	-	597	mA	real power pattern; T_J=150°C
∑ Sum of all currents with DC-DC EVRC regulator active [4]	$I_{DDTOTDC3}$ CC	-	-	380	mA	real power pattern; EVRC reset settings with 72% efficiency; V_{EXT} = 3.3V
∑ Sum of all currents with DC-DC EVRC regulator active [4]	$I_{DDTOTDC5}$ CC	-	-	280	mA	real power pattern; EVRC reset settings with 72% efficiency; V_{EXT} = 5V
∑ Sum of all currents (SLEEP mode) [1]	I_{SLEEP} CC	-	-	25	mA	All CPUs in idle, All peripherals in sleep, $f_{SRI/SPB}$ = 1 MHz via LPDIV divider; T_J = 25 $°C$
∑ Sum of all currents (STANDBY mode) drawn at V_{EVRSB} supply pin [5]	$I_{STANDBY}$ CC	-	-	130 [6]	µA	32 kB Standby RAM block active. SCR inactive. Power to remaining domains switched off. T_J = 25 $°C$; V_{EVRSB} = 5 V

表 3-26 电流消耗（续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum power dissipation [7]	PD SR	-	-	1495	mW	max power pattern
		-	-	1080	mW	real power pattern

1) 限值是根据实际功率模式 (V_{DD} =1.275V) 定义的。对于最大功率模式，限值必须乘以系数 1.22。

2) 实际的 Pflash 读取模式，Pflash 带宽利用率为 50%，代码混合为 50% 的 0 和 50% 的 1。使用至少 100nF 的公共去耦电容 (V_{DDP3})。在 3.3 V 电源下以突发模式连续进行 Dflash 编程，并并行进行实际的 Pflash 读取访问。相应闪存模块的擦除电流小于V_{DDP3}引脚上的相应编程电流。编程和擦除闪存可能会产生高达 45 mA / 20 ns 的瞬态电流尖峰。
由去耦电容器和缓冲电容器处理。此参数与外部电源尺寸有关，与热无关。

3) 电流消耗仅包括最小的端口活动。

4) 从外部稳压器汲取的总电流是根据 72% EVRC SMPS 稳压器效率估算的。IDDTOTDCx 是使用缩放的核心电流 [(IDD x VDD)/(VinxEfficiency)] 根据 IDDTOT 计算得出的，并构成所有其他轨电流和 IDDM。

5) 同样的电流限制也适用于其他功率模式。

6) ∑ 运行模式下 VEVRSB 电源引脚上所有电流的总和小于（IEVRSB + 4 mA 待机 RAM 电流 + ISCRSB（如果 SCR 处于活动状态）。∑ 建议在此引脚上至少使用 100 nF 去耦电容。32kB 待机 SRAM 对 ITANDBY 电流的使用不到 10uA。

7) 仅当所有电源均由外部供电且不包含 EVR33 和 EVRC 的功率损耗时，这些值才有效。

表 3-27 模块电流消耗

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
I_{DDP3} supply current for programming of a Pflash or Dflash bank [1]	$I_{DDP3PROG}$ CC	-	-	25	mA	Pflash 3.3V programming current adder when using external 3.3V supply.
		-	-	9 [2]	mA	Pflash 3.3V programming current adder when using external 5V supply.
I_{EXT} supply current added by LVDS pads in LVDS mode [1]	$I_{EXTLVDS}$ CC	-	-	3	mA	real power pattern; 2 pairs of LVDS pins active with receive function
		-	-	12	mA	real power pattern; 3 pairs of LVDS pins active with transmit function

表 3-27 模块电流消耗（续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
∑ Sum of external I_{DDM} supply currents (incl. $I_{DDMEVADC}$+$I_{DDMEDSADC}$)	I_{DDM} CC	-	-	14	mA	real power pattern; current for EDSADC modules only and EVADC modules are inactive; 4 EDSADC channels active continuously.
		-	-	22 [3]	mA	max power pattern; current for EDSADC modules only and EVADC modules are inactive; all EDSADC channels active continuously.
		-	-	13	mA	real power pattern; current for EVADC modules only and EDSADC modules are inactive; 6 EVADC modules active.
		-	-	15 [4]	mA	max power pattern; current for EVADC modules only and EDSADC modules are inactive; all EVADC modules active.
I_{DDP3} supply current for erasing of a Pflash or Dflash bank	$I_{DDP3ERASE}$ CC	-	-	25	mA	Pflash 3.3V erasing current adder when using external 3.3V supply.
SCR 8-bit Standby Controller current incl. PMS in STANDBY Mode drawn at V_{EVRSB} supply pin	I_{SCRSB} CC	-	-	7.5	mA	SCR power pattern incl. PMS current consumption with fback clock active; f_{SYS_SCR} = 20MHz; T_J=150°C
		-	0.150	-	mA	SCR power pattern incl. PMS current consumption with fback inactive; fSYS_SCR = 70kHz; T_J=25°C
SCR 8-bit Standby Controller CPU in IDLE mode [5]	$I_{SCRIDLE}$ CC	-	-	3.5	mA	real power pattern. CPU set into idle mode.

1) 同样的电流限制也适用于其他功率模式。

2) 在 5V 电压下对 Pflash 进行编程期间，VEXT 电源轨上会额外消耗 2 mA 电流。

3) 单个 DS 通道实例消耗 4 mA。

4) 单个 VADC 单元消耗 1.3 mA 的电流。
5) 限值是根据实际功率模式 (V_{DD} =1.275V) 定义的。对于最大功率模式，限值必须乘以系数 1.22。

表3-28 模块核心电流消耗

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
I_{DD} core current of CPUx main core with CPUx lockstep core inactive	I_{DDCx0} CC	-	-	70	mA	max power pattern; IPC=1.2
		-	-	45	mA	real power pattern; IPC=0.6
I_{DD} core current of CPUx main core with CPUx lockstep core active	I_{DDCxx} CC	-	-	I_{DDCx0} + 50	mA	max power pattern; IPC=1.2
		-	-	I_{DDCx0} + 40	mA	real power pattern; IPC=0.6
I_{DD} core current added by GTM	I_{DDGTM} CC	-	-	90	mA	max power pattern
		-	-	75	mA	real power pattern; TIMx, TOMx, ATOMx , MCSx active. 2 clusters at 200 MHz.
		-	-	50	mA	TIMx, TOMx active at 100MHz. ATOMx , MCSx, DPLL inactive. 2 clusters at 100 MHz.
I_{DD} core current added by HSM	I_{DDHSM} CC	-	-	20 [1]	mA	max power pattern; HSM running at 100MHz.
I_{DD} core dynamic current added by LBIST	$I_{DDLBIST}$ CC	-	-	200 [2]	mA	LBIST Configuration A; 1.2V ≤ V_{DD}
I_{DD} core dynamic current added by MBIST	$I_{DDMBIST}$ CC	-	-	200	mA	fMBIST = 300MHz; tMBIST < 6ms. MTU Ganging procedure for SRAM test and initialization; VDD = 1.375V.

1) 电流消耗包括基本 HSM 活动，如AES 模块。
2) LBIST 可在启动阶段执行，也可由应用软件触发。在 LBIST 执行时间 (t_{LBIST}) 内，次级电压监控器处于非活动状态。
在启动阶段，外部提供的V_{DD}电压必须等于或大于 1.2V （ V_{DD} 标称 - 4%），以确保静态准确性。
如果V_{DD}由 EVRC 内部供电，则 EVRC 确保不违反V_{DD}的 1.2V 静态欠压限制。

3.13 电源基础结构和电源启动

3.13.1 电源上升和下降行为

电源轨的启动斜率应符合 SR（见表 3-32 电源斜坡）。

3.13.1.1 单电源模式（a）

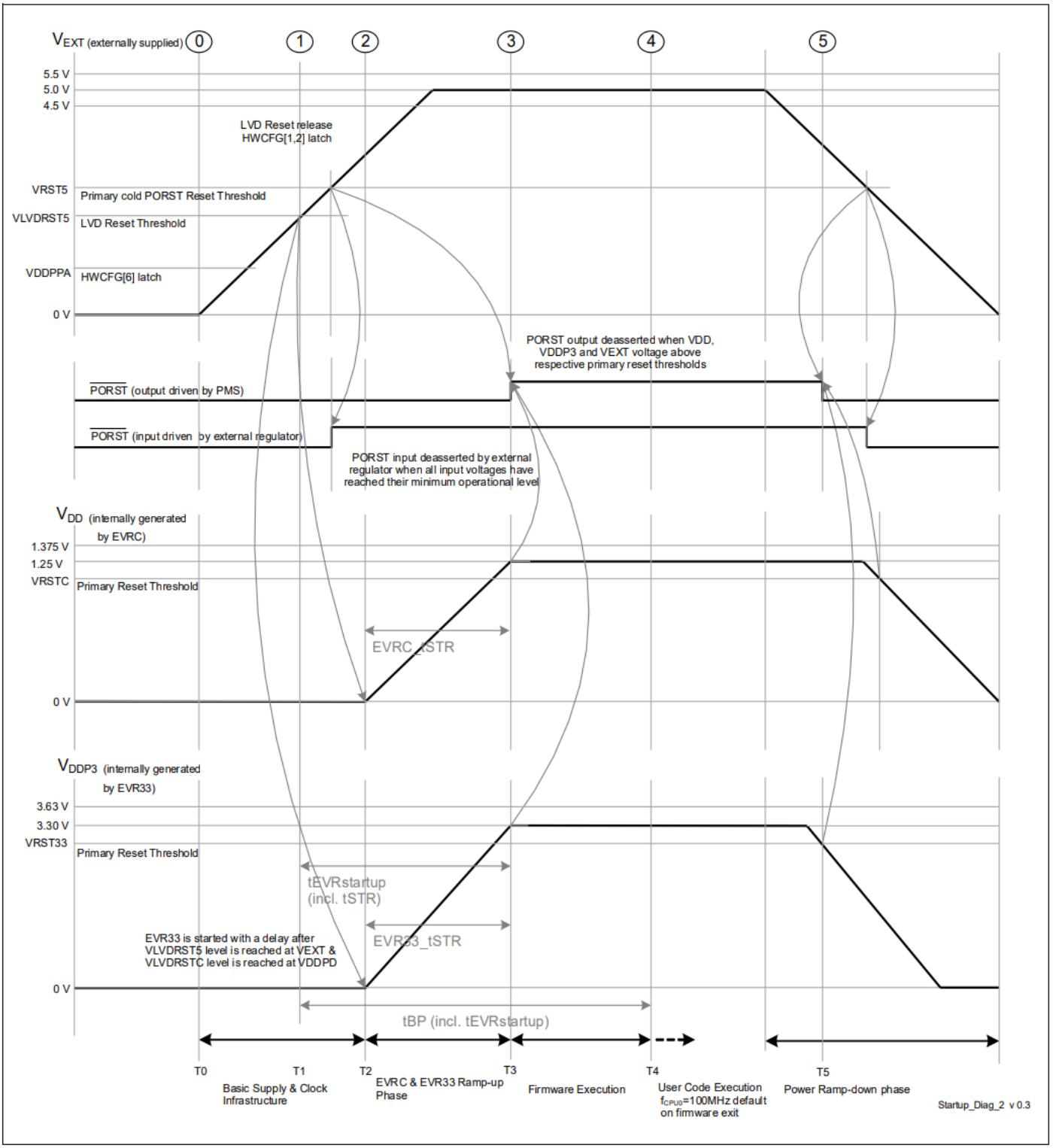


图 3-3 单电源模式（a）- V_{EXT}（5 V）单电源

V_{EXT} = 5 V 单电源模式。V_{DD}和V_{DDP3} 由内置的 EVRC 和 EVR33 稳压器从内部产生。

- 在基本基础结构和 EVRx 稳压器启动阶段（T0 至 T2），从外部稳压器 (dIEXT /dt) 吸取电流的速率受到限制，最大为 100 mA，稳定时间为 100 us。电源轨的启动斜率应符合数据手册参数 SR，斜率定义为 0% 至 100% 电压电平之间的最大切向斜率。实际波形可能不同于规格书。
- 此外，还确保在固件启动阶段（T3 至 T4）从稳压器吸取的电流（dIDD/dt）限制为最大 100 mA，稳定时间为 100 us。
- 当 PORST（输入）或 PORST（输出）激活/置位时，PORST 激活/置位。
- PORST（输入）有效意味着外部设备可通过将 PORST 引脚拉低，使复位保持有效。建议保持 PORST（输入）有效，直到外部电源电压高于相应的主复位阈值。
- PORST（输出）有效意味着 µC 在内部发出复位信号并将 PORST引脚驱动至低电平，从而将复位信号传播至外部设备。当三个电源域（V_{DD}、V_{DDP3}或V_{EXT}）中至少有一个违反其主要欠压复位阈值时，µC会发出 PORST置位（输出）信号。当所有电源均高于其主要复位阈值，且基本电源和时钟基础设施可用时，µC 会发出PORST不置位 （输出）信号。在 T3 复位释放期间，预计负载跳变高达 150 mA (dIDD) 。
- 电源时序如图 3-3 列举如下
  - T1 至 T2 指的是外部电源逐渐升高，基本电源和时钟基础设施组件可用这段时间。此时，带隙和内部时钟源启动。电源模式根据 HWCFG[2:1,4,5,6] 和 TESTMODE 引脚进行评估。这些事件在 T1 时 LVD 复位释放后触发，此时V_{EXT} ad VEVRSB 电源轨已达到 VLVDRST5 电平，内部预稳压器 VDDPD 电压已达到 VLVDRSTC 电平。
  - T2 指的是 EVRC 和 EVR33 稳压器软启动的时间点。PORST（输入）对 EVR33 或 EVRC 输出没有任何影响，尽管 PORST 已置位且器件处于复位状态，稳压器仍会继续产生相应的电压。产生的电压在 tSTR（数据手册参数）时间内呈软上升趋势，以避免过冲。
  - T3 指的是所有电源都高于其主要复位阈值（由 VRST5、VRST33 和 VRSTC 供电电压水平表示）的时间点。EVRC 和 EVR33 稳压器已经启动。

    PORST（输出）不置位，并且 HWCFG[3:5] 引脚被 SCU 锁存在 PORST 上升沿。固件执行已启动。T1 和 T3 之间的时间记录为 tEVRstartup（数据手册参数）。
  - T4 指的是固件执行完成并且用户代码以 CPU0 的默认频率 100 MHz 开始执行的时间点。T0 和 T4 之间的时间记录为 tBP（数据手册参数）。
  - T5指的是斜坡下降阶段期间至少一个外部提供或生成的电源（V_{DD}、V_{DDP3} 或V_{EXT}）降至其各自的初级欠压复位阈值以下的时间点。

3.13.1.2 单电源模式（e）

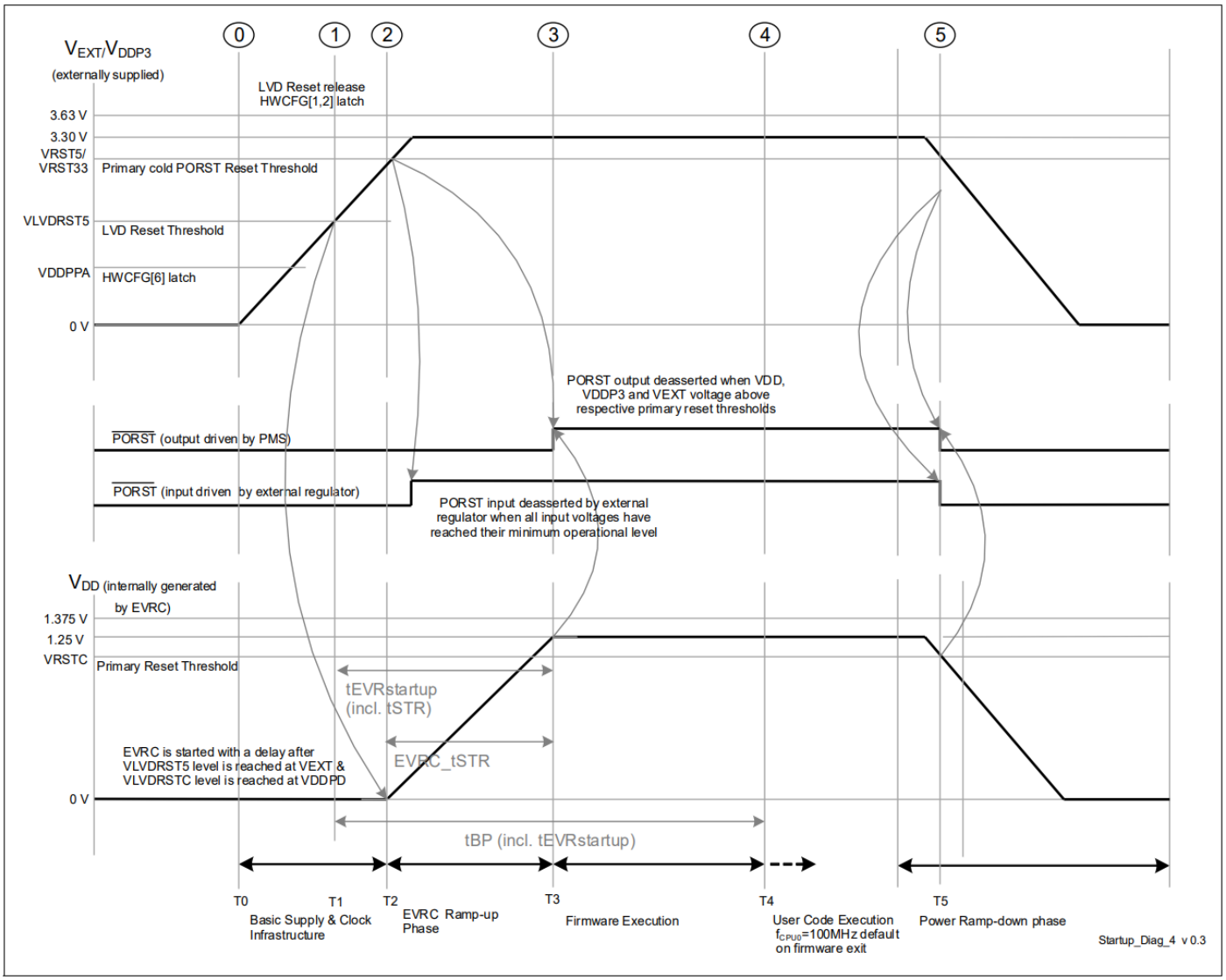


图 3-4　　单电源模式（e）-（V_{EXT} 和 V_{DDP3}）3.3 V 单电源

V_{EXT}= V_{DDP3} = 3.3 V 单电源模式。V_{DD}由 EVRC 稳压器内部产生。

- 从外部稳压器汲取电流的速率 (dIEXT /dt) 在启动阶段被限制为最大 100 mA，建立时间为 100 us。电源轨的启动斜率应符合数据手册参数 SR，斜率定义为 0% 至 100% 电压电平之间的最大切向斜率。实际波形可能不同于规格书。
- 当 PORST（输入）或 PORST（输出）激活/置位时，PORST 激活/置位。
- PORST（输入）有效意味着外部设备可通过将 PORST 引脚拉低，使复位保持有效。建议保持 PORST（输入）有效，直到外部电源电压高于相应的主复位阈值。
- PORST（输出）有效意味着 µC 在内部发出复位信号并将 PORST 引脚驱动至低电平，从而将复位信号传播至外部设备。当三个电源域（V_{DD}、V_{DDP3} 或 V_{EXT}）中至少有一个违反其主要欠压复位阈值时，µC会发出 PORST置位（输出）信号。当所有电源均高于其主要复位阈值，且基本电源和时钟基础设施可用时，µC 会发出PORST不置位 （输出）信号。基本供电和时钟基础设施可用。在 T3 复位释放期间，预计负载跳变高达 150 mA（dIDD）。

- 电源时序如图 3-4 列举如下
  - T1 至 T2 指的是外部电源逐渐升高，基本电源和时钟基础设施组件可用这段时间。此时，带隙和内部时钟源启动。电源模式根据 HWCFG[2:1,4,5,6] 和 TESTMODE 引脚进行评估。这些事件在 T1 时 LVD 复位释放后触发，此时V_{EXT}ad VEVRSB 电源轨已达到 VLVDRST5 电平，内部预稳压器 VDDPD 电压已达到 VLVDRSTC 电平。
  - T2 指的是 EVRC 稳压器软启动开始的时间点。PORST（输入）对 EVRC 输出没有任何影响，尽管 PORST 已置位且设备处于复位状态，稳压器仍会继续产生相应的电压。产生的电压在 tSTR（数据手册参数）时间内呈软上升趋势，以避免过冲。
  - T3 指的是所有电源都高于其主要复位阈值（由 VRST5、VRST33 和 VRSTC 供电电压水平表示）的时间点。EVRC 稳压器已启动。PORST（输出）不置位，并且 HWCFG[3:5] 引脚被 SCU 锁存在 PORST 上升沿。固件执行已启动。T1 和 T3 之间的时间记录为 tEVRstartup（数据手册参数）。
  - T4 指的是固件执行完成并且用户代码以 CPU0 的默认频率 100 MHz 开始执行的时间点。T0 和 T4 之间的时间记录为 tBP（数据手册参数）。
  - T5指的是斜坡下降阶段期间至少一个外部提供或生成的电源（V_{DD}、V_{DDP3} 或V_{EXT}）降至其各自的初级欠压复位阈值以下的时间点。

3.13.1.3 外部供电模式（d）

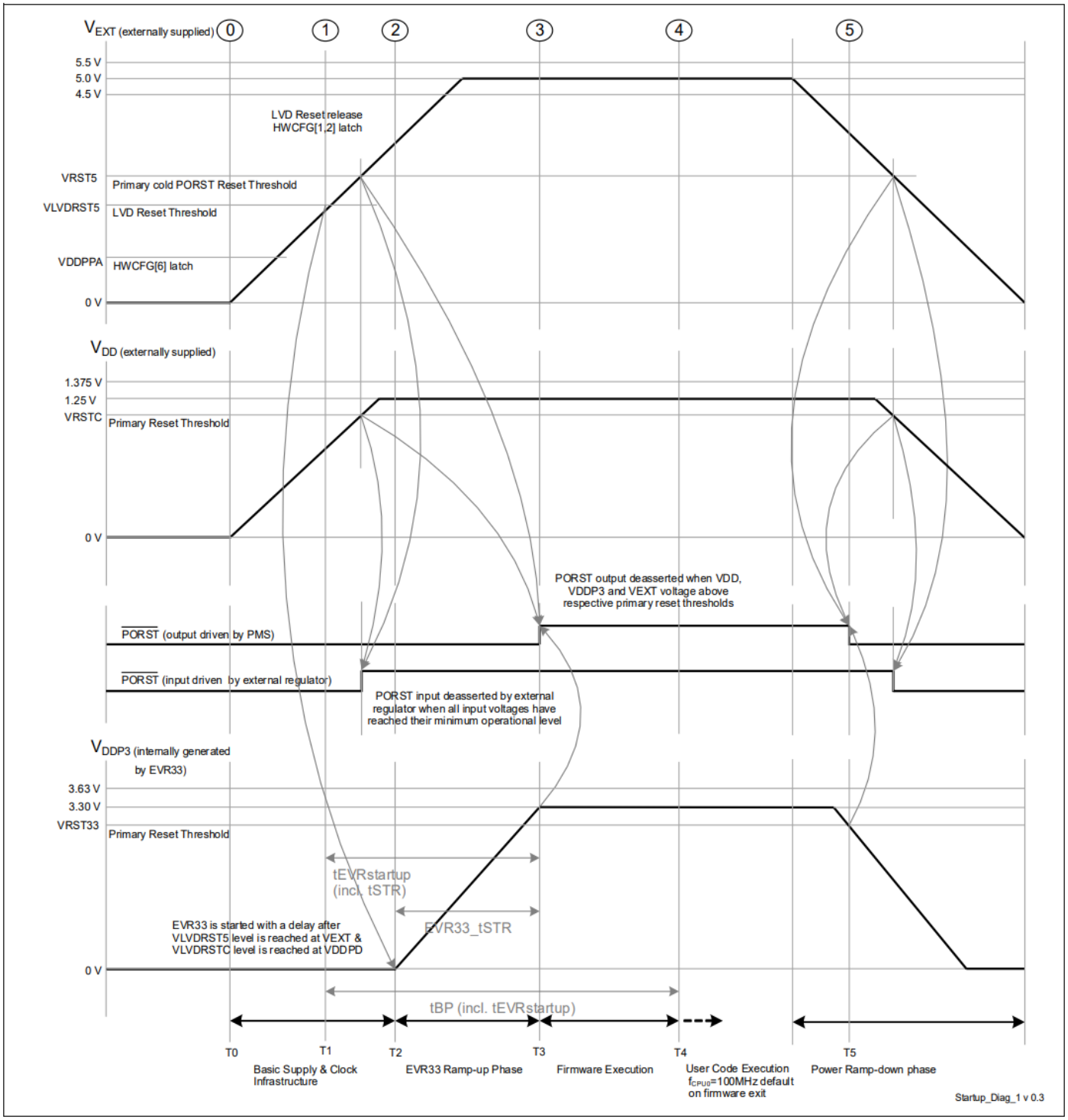


图 3-5　　外部供电模式（d）-V_{EXT}和V_{DD}外部供电

V_{EXT} = 5 V 且V_{DD} 电源由外部供电。3.3V 由 EVR33 稳压器内部产生。

- 外部电源 V_{EXT} 和 V_{DD} 的启动、上升和下降时间可能彼此独立。电源轨的启动转换速率应符合数据手册参数 SR 的规定。斜率定义为 0% 至 100% 电压范围内的最大切线斜率。实际斜率可能与规格不符。预计在启动期间，

V_{EXT} 会在 V_{DD} 轨之前上升。如果 V_{DD} 电源轨在 V_{EXT} 之前上升；启动期间的 V_{DD} 电源过冲应限制在工作电压范围内。

- 从外部稳压器汲取电流的速率（dIEXT /dt 或 dIDD /dt）在启动阶段被限制为最大 100 mA，建立时间为 100 us。
- 当 PORST（输入）或 PORST（输出）激活/置位时，PORST 激活/置位。
- PORST（输入）有效意味着外部设备可通过将 PORST 引脚拉低，使复位保持有效。建议保持 PORST（输入）有效，直到外部电源电压高于相应的主复位阈值。
- PORST（输出）有效意味着 µC 在内部发出复位信号并将 PORST 引脚驱动至低电平，从而将复位信号传播至外部设备。当三个电源域（V_{DD}、V_{DDP3} 或 V_{EXT}）中至少有一个违反其主要欠压复位阈值时，µC会发出 PORST置位（输出）信号。当所有电源均高于其主要复位阈值，且基本电源和时钟基础设施可用时，µC 会发出PORST不置位 （输出）信号。基本供电和时钟基础设施可用。在 T3 复位释放期间，预计负载跳变高达 150 mA（dIDD）。
- 电源时序如图 3-5 列举如下
  - T1 至 T2 指的是外部电源逐渐升高，基本电源和时钟基础设施组件可用这段时间。此时，带隙和内部时钟源启动。电源模式根据 HWCFG[2:1,4,5,6] 和 TESTMODE 引脚进行评估。这些事件在 T1 时 LVD 复位释放后触发，此时V_{EXT} ad VEVRSB 电源轨已达到 VLVDRST5 电平，内部预稳压器 VDDPD 电压已达到 VLVDRSTC 电平。
  - T2 指的是 EVR33 稳压器软启动开始的时间点。PORST（输入）对 EVR33 输出没有任何影响，尽管 PORST 已置位且设备处于复位状态，稳压器仍会继续产生相应的电压。产生的电压在 tSTR（数据手册参数）时间内呈软上升趋势，以避免过冲。
  - T3 指的是所有电源都高于其主要复位阈值（由 VRST5、VRST33 和 VRSTC 供电电压水平表示）的时间点。EVR33 稳压器已启动。PORST（输出）不置位，并且 HWCFG[3:5] 引脚被 SCU 锁存在 PORST 上升沿。固件执行已启动。T1 和 T3 之间的时间记录为 tEVRstartup（数据手册参数）。
  - T4 指的是固件执行完成并且用户代码以 CPU0 的默认频率 100 MHz 开始执行的时间点。T0 和 T4 之间的时间记录为 tBP（数据手册参数）。
  - T5指的是斜坡下降阶段期间至少一个外部提供或生成的电源（V_{DD}、V_{DDP3} 或V_{EXT}）降至其各自的初级欠压复位阈值以下的时间点。

3.13.1.4 外部供电模式 (h)

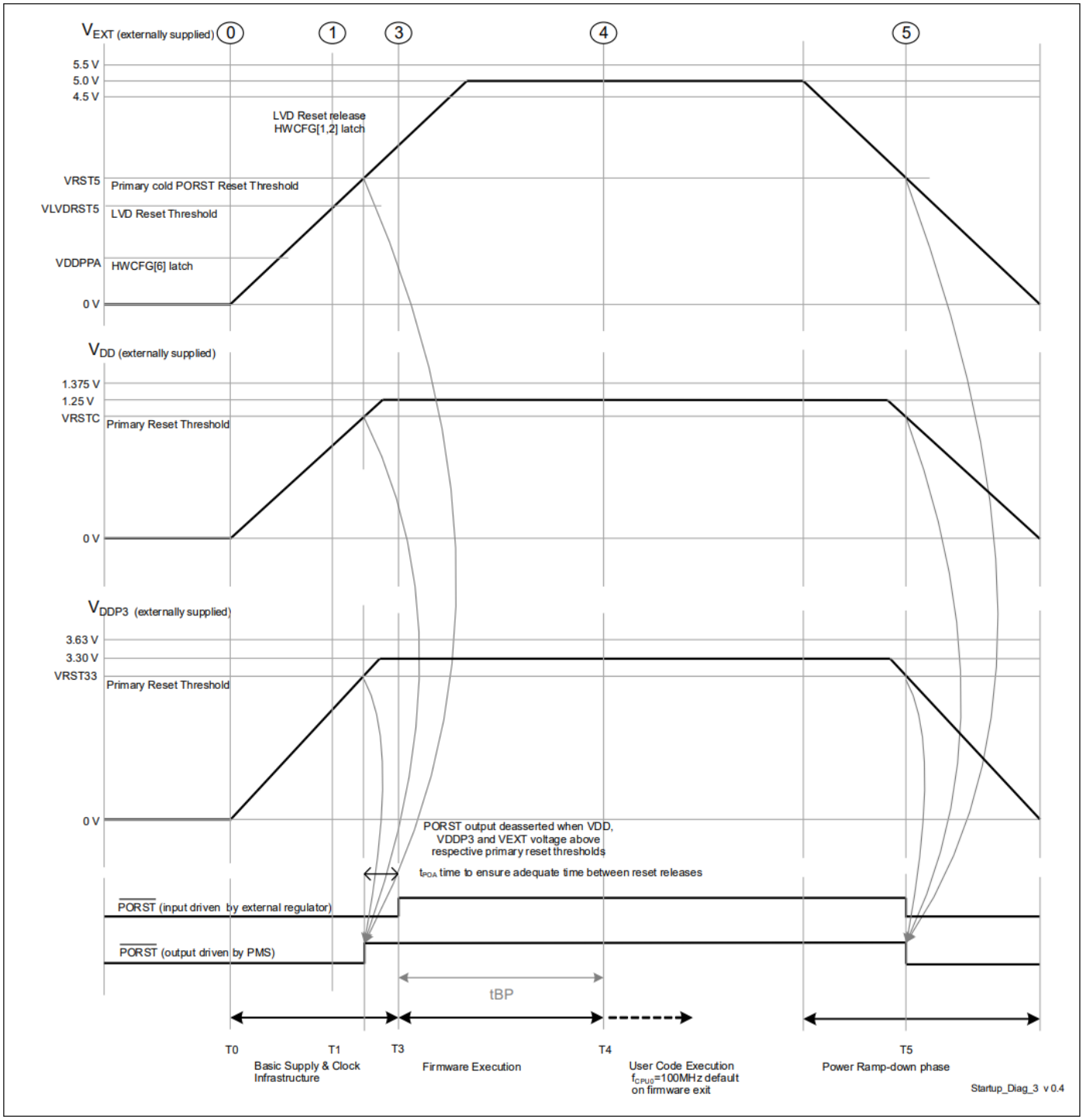


图 3-6 外部供电模式（h）- V_{EXT}、V_{DDP3} 和 V_{DD} 外部供电

所有电源，即V_{EXT}、V_{DDP3} 和 V_{DD} 均由外部供电。

- 外部电源 V_{EXT} 、 V_{DDP3} 和 V_{DD} 的启动、上升和下降时间可能彼此独立。电源轨的启动转换速率应符合（数据手册参数）SR 的要求。斜率定义为 0% 至 100% 电压范围内的最大切线斜率。实际斜率可能与规格不符。预计在启动期间，V_{EXT} 会在 V_{DDP3} 和 V_{DD} 轨之前上升。如果较小的电压轨在 V_{EXT} 之前逐渐上升；则启动期间的 V_{DD} 和 V_{DDP3} 电源过冲应限制在各自电压轨的工作电压范围内。

- 从外部稳压器汲取电流的速率（dIEXT /dt， dIDD /dt或dIDDP3 /dt）在启动阶段被限制为最大 100 mA，建立时间为 100 us。
- 当 PORST（输入）或 PORST（输出）激活/置位时，PORST 激活/置位。
- PORST（输入）有效意味着外部设备可通过将 PORST 引脚拉低，使复位保持有效。建议保持 PORST（输入）有效，直到外部电源电压高于相应的主复位阈值。
- PORST（输出）有效意味着 µC 在内部发出复位信号并将 PORST引脚驱动至低电平，从而将复位信号传播至外部设备。当三个电源域（V_{DD}、V_{DDP3}或V_{EXT}）中至少有一个违反其主要欠压复位阈值时，µC会发出 PORST置位（输出）信号。当所有电源均高于其主要复位阈值，且基本电源和时钟基础设施可用时，µC 会发出PORST不置位 （输出）信号。在 T3 复位释放期间，预计负载跳变高达 150 mA (dIDD) 。
- 电源时序如图 3-6 列举如下
  - T1 至 T3 指的是外部电源逐渐升高，基本电源和时钟基础设施组件可用这段时间。此时，带隙和内部时钟源启动。电源模式根据 HWCFG[2:1,4,5,6] 和 TESTMODE 引脚进行评估。这些事件在 T1 时 LVD 复位释放后触发，此时V_{EXT} ad VEVRSB 电源轨已达到 VLVDRST5 电平，内部预稳压器 VDDPD 电压已达到 VLVDRSTC 电平。
  - T3 指的是所有电源都高于其主要复位阈值（由 VRST5、VRST33 和 VRSTC 供电电压水平表示）的时间点。PORST（输出）不置位，并且 HWCFG[3:5] 引脚被 SCU 锁存在 PORST 上升沿。固件执行已启动。
  - T4 指的是固件执行完成并且用户代码以 CPU0 的默认频率 100 MHz 开始执行的时间点。T0 和 T4 之间的时间记录为 tBP（数据手册参数）。
  - T5指的是斜坡下降阶段期间至少一个外部提供或生成的电源（V_{DD}、V_{DDP3} 或V_{EXT}）降至其各自的初级欠压复位阈值以下的时间点。

3.14 复位时序

表 3-29 复位

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Application Reset Boot Time	t_B CC	-	-	400	µs	operating with max. frequencies, with valid BMI header
System Reset Boot Time	t_{BS} CC	-	-	1.1	ms	RAM initialization and HSM boot time are not included, with valid BMI header
Cold Power on Reset Boot Time [1]	t_{BP} CC	-	-	3.1	ms	$dVEXT/dT$=1V/ms. $VEXT$>$VLVDRST5$. Boot time after Cold PORST including EVR ramp-up and Firmware execution time; RAM initialization and HSM boot time are not included.
		-	-	1.6	ms	Firmware execution time after PORST release without EVR ramp-up; RAM initialization and HSM boot time is not included
Minimum cold PORST reset hold time in case of power fail event issued by EVR primary monitors	t_{EVRPOR} CC	10 [2]	-	-	µs	
PMS Infrastructure, EVRC and EVR33 overall start-up time till cold PORST reset release	$t_{EVRstartup}$ CC	-	-	1	ms	dV/dT=1V/ms. EVRC and EVR33 active
Minimum PORST active hold time externally after power supplies are stable at operating levels after start-up	t_{POA} SR	1 [3]	-	-	ms	
Configurable PORST digital filter delay in addition to analog pad filter delay	$t_{PORSTDF}$ CC	600	-	1200	ns	
Warm Reset Sequencing Delay	$t_{WARMRSTSEQ}$ CC	-	-	180	µs	
HWCFG pins hold time from ESR0 rising edge	t_{HDH} CC	16 / f_{SPB}	-	-	ns	

表 3-29 复位（续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
HWCFG pins setup time to ESR0 rising edge	t_{HDS} CC	0	-	-	ns	
Ports inactive after ESR0 reset active	t_{PI} CC	$8000/f_{BACKT}$	-	$18000/f_{BACKT}$	s	
Ports inactive after PORST reset active	t_{PIP} CC	-	-	160	ns	
Hold time from PORST rising edge	t_{POH} SR	150	-	-	ns	
Setup time to PORST rising edge	t_{POS} SR	0	-	-	ns	
Warm PORST reset boot time	t_{BWP} CC	-	-	1.5	ms	without RAM initalization
LBIST execution time extending the boot time	t_{LBIST} CC	-	-	6	ms	LBIST Configuration A; 1.2V ≤ V_{DD}
SCR reset boot time	t_{SCR} CC	-	-	5	µs	User Mode 0
		-	-	16	µs	User Mode 1
		-	13.3	-	µs	WDT double bit ECC, soft reset
Minimum external supplies hold time after warm reset assertion	$t_{SUPHOLD}$ CC	-	-	250	µs	external supplies are V_{EVRSB}, V_{EXT}, V_{FLEX}, V_{DDM}, V_{DDP3} and V_{DD}

1) RAM 初始化另外增加 500µs。

2) 冷 PORST 复位由 uC 驱动，并维持在 VDDPPA 限制和绝对最大额定电压限制之间的扩展电压范围内。

3) 电源上升或电源恢复时的复位释放被延迟了 1.5%（默认值）的电压滞回，该电压滞回高于 VEXT、VDDP3 和 VDD 轨上实施的欠压复位限值。这种机制有助于避免在电源缓慢上升期间，由于复位释放时压降/电流跳跃而导致的多个连续的冷 PORST 事件。

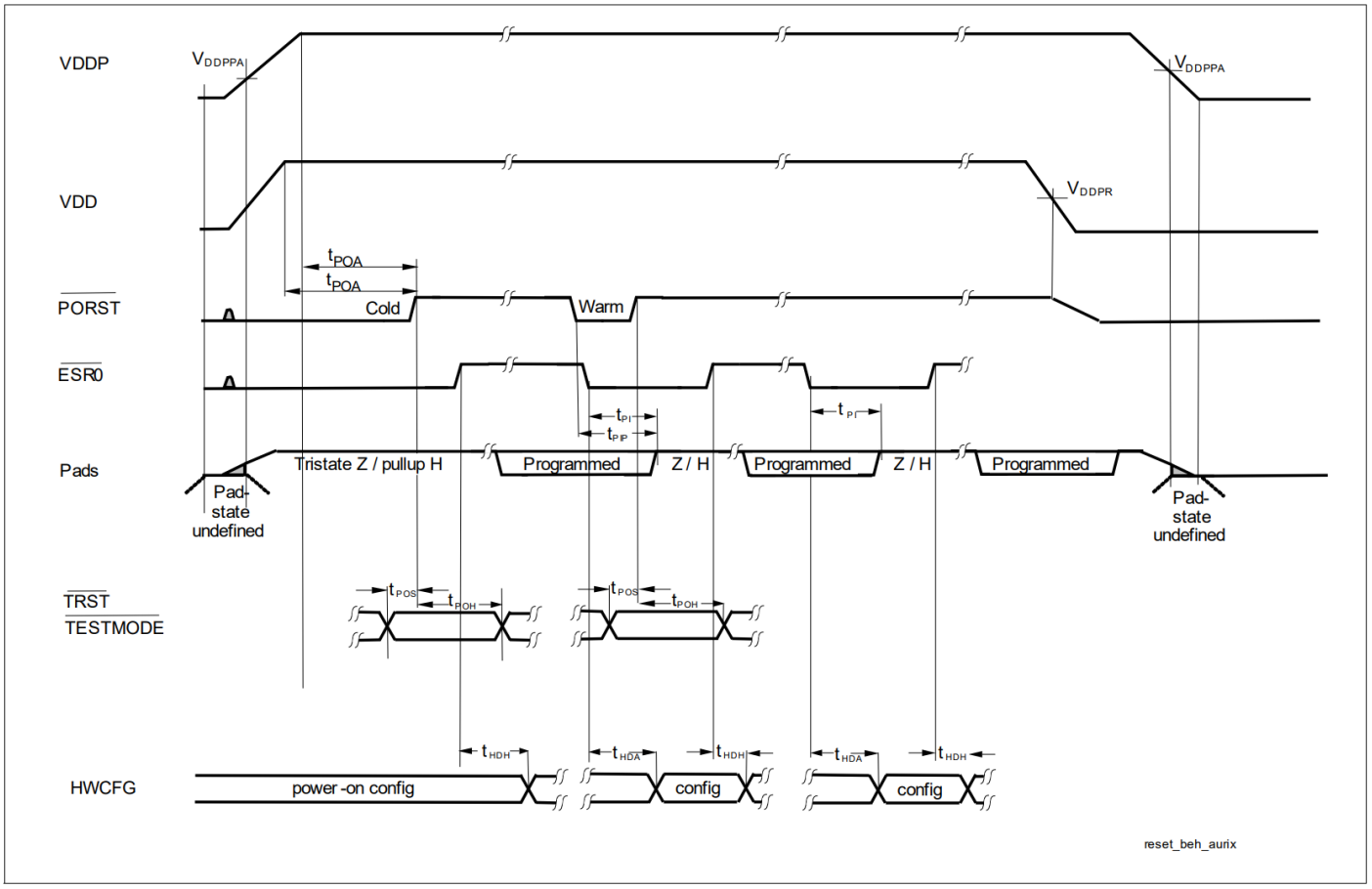


图 3-7 电源、焊盘和复位时序

3.15 EVR

表 3-30 EVR33 LDO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input voltage range	V_{IN} SR	3.60 [1]	-	5.50	V	Normal RUN mode
		2.97 [2]	-	5.50	V	Low voltage cranking mode
Output voltage operational range including load/line regulation and aging [3]	V_{OUT} CC	2.97	3.3	3.63	V	Normal RUN mode
		2.60	3.3	3.63	V	Low voltage cranking mode; I_{DDP3}=50mA
Output V_{DDx3} static voltage accuracy after trimming and aging without dynamic load/line regulation.	V_{OUTT} CC	3.225	3.3	3.375	V	Normal RUN mode
		2.78	3.3	3.375	V	Low voltage cranking mode; I_{DDP3}=50mA
Output buffer capacitance on V_{OUT}	C_{OUT} SR	1.45	2.2	3	µF	
Output buffer capacitor ESR	C_{OUTESR} SR	-	-	100 [4]	mOhm	f > 0.5MHz; f < 10MHz
Maximum output current of the regulator	I_{MAX} CC	60 [5]	-	-	mA	Normal RUN mode
Startup time	t_{STR} CC	-	500	1000	µs	Normal RUN mode
External V_{IN} supply ramp [6]	$dVin/dt$ SR	-	1	-	V/ms	
Ripple on Output Voltage	ΔV_{OUTTC} CC	-	-	33	mV	V_{EXT} ≥ 2.97V ; V_{EXT} ≤ 5.5V ; I_{OUTTC} ≥ 10mA ; I_{OUTTC} ≤ 60mA; ΔV_{OUTTC} = (peak to peak ripple / 2)
Load step response [7]	$dVout/dIout$ CC	-165	-	-	mV	Normal RUN mode; dI=10 to 60mA; dt=20ns; $Tsettle$=20us
		-	-	165	mV	Normal RUN mode; dI=60 to 10mA; dt=20ns; $Tsettle$=20us
		-180	-	-	mV	Low voltage cranking mode; dI=10 to 50 mA; dt=20ns; $Tsettle$=20us
		-	-	180	mV	Low voltage cranking mode; dI=50 to 10mA; dt=20ns; $Tsettle$=20us

表 3-30 EVR33 LDO （续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line step response	$dVout/dVin$ CC	-	-	40	mV	$dVin/dT$=1V/ms; dV= 3.6 to 5V; I_{MAX}=60mA
		-40	-	-	mV	$dVin/dT$=1V/ms; dV= 5 to 3.6V; I_{MAX}=60mA
		-	-	280	mV	$dVin/dT$=50V/ms; dV= 3.6 to 5V; I_{MAX}=60mA
		-165	-	-	mV	$dVin/dT$=50V/ms; dV= 5 to 3.6V; I_{MAX}=60mA

1) 最小输入电压中包含 300mV 的最大传输器件压差，以确保正常运行期间传输器件的最佳性能。

2) VEXT 输入电压降到 2.97V，将导致 VDDP3 输出电压降到 2.6V，如果在此之前已经将Flash切换到低性能模式，那么是可以正常工作的。

3) 如果使用 EVR33，则不允许使用外部感应负载。

4) 还建议从引脚到 EVR 输出电容器的电源走线电阻小于 100 mOhm。应在 Cout 之前靠近引脚的位置放置一个 100nF 的附加去耦电容。

5) 在低压模式（启动情况）下，使用片上传输装置时，IMAX 限制为 40 mA。在不使用 EVR33 的情况下，如果在电源上电时序中，3.3V 电压先于 5V 电压由外部稳压器供电，同时 5V VEXT 电压轨上电压不够时，则注入 3.3V VDDP3 电源轨的电流应限制在 500 mA 以内。

6) EVR 能够有效抵御 0 - 2.97 V 之间残余电压的上升。稳健性验证涵盖 0.5V/min 至 120V/ms 之间的 VEXT 电压斜坡范围。产生的电压本身在 tSTR 时间内遵循软上升趋势，以避免过冲。

7) 建立时间被定义为直到输出电压在单个器件平均值(VOUTT) 的+-1% 范围内。

表 3-31 电源监视器

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Primary Undervoltage Reset threshold for V_{DDP3} before trimming [1]	V_{RST33} CC	-	-	3.00	V	by reset release before EVR trimming on supply ramp-up
Primary undervoltage reset threshold for V_{DD} before trimming	V_{RSTC} CC	-	-	1.138	V	by reset release before trimming on supply ramp-up including 2 LSB voltage Hysteresis
V_{EXT} primary undervoltage monitor accuracy after trimming [2]	$V_{EXTPRIUV}$ CC	2.86	2.92	2.97	V	V_{EXT} = Undervoltage cold PORST Primary Monitor Threshold
V_{DDP3} primary undervoltage monitor accuracy after trimming [2]	$V_{DDP3PRIUV}$ CC	2.86 [3]	2.90	2.97	V	VDDP3 = Undervoltage cold PORST Primary Monitor Threshold
V_{DD} primary undervoltage monitor accuracy after trimming [2]	$V_{DDPRIUV}$ CC	1.08 [3]	1.105	1.125	V	VDD = Undervoltage cold PORST Primary Monitor Threshold

表 3-31 电源监视器（续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
EVR primary monitor measurement latency for a new supply value	t_{PRIUV} CC	-	-	300	ns	The supply ramp / line jump slope is limited to 50V/ms for V_{EXT}, V_{DDP3} and V_{DD} rails.

表 3-31 电源监视器（续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{EXT}, V_{DDM} & V_{EVRSB} secondary supply monitor accuracy after trimming [4) 5)]	V_{EXTMON} CC	3.2	3.3	3.4	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=3.3V=90h(OV,UV). For BGA packages: EVRMONFILT.SWDFI L=1.
		3.2	3.3	3.4	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=3.3V=90h(OV,UV). For QFP packages: EVRMONFILT.SWDFI L=2
		4.5	4.6	4.7	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=4.6V=C8h(UV)/C9h(OV). For BGA packages: EVRMONFILT.SWDFI L=1
		4.5	4.6	4.7	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=4.6V=C8h(UV)/C9h(OV). For QFP packages: EVRMONFILT.SWDFI L=2
		5.3	5.4	5.5	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=5.4V=EAh(UV)/ECh(OV). For BGA packages: EVRMONFILT.SWDFI L=1
		5.3	5.4	5.5	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=5.4V=EAh(UV)/ECh(OV). For QFP packages: EVRMONFILT.SWDFI L=2
		4.9	5.0	5.1	V	

表 3-31 电源监视器（续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{DDP3} secondary supply monitor accuracy after trimming [5]	$V_{DDP3MON}$ CC	2.97	3.035	3.1	V	EVR33xxVAL monitoring threshold=3.035V=CBh (UV)/CCh(OV). EVRMONFILT.EVR33 FIL = 3.
		3.235	3.30	3.365	V	EVR33xxVAL monitoring threshold=3.3V=DDh(OV, UV). EVRMONFILT.EVR33 FIL = 3.
		3.5	3.565	3.63	V	EVR33xxVAL monitoring threshold=3.565V=EEh (UV)/EFh(OV). EVRMONFILT.EVR33 FIL = 3.
V_{DD} & V_{DDPD} secondary supply monitor accuracy after trimming [5]	V_{DDMON} CC	1.125	1.15	1.175	V	EVRCxxVAL & PRExxVAL monitoring threshold=1.15V=C7h(UV)/C8h(OV). EVRMONFILT.EVRCFI L = 1.
		1.225	1.25	1.275	V	EVRCxxVAL & PRExxVAL monitoring threshold=1.25V=D9h(OV ,UV). EVRMONFILT.EVRCFI L = 1.
		1.325	1.35	1.375	V	EVRCxxVAL & PRExxVAL monitoring threshold=1.35V=EAh(UV)/EBh(OV). EVRMONFILT.EVRCFI L = 1.
V_{EXT} LVD Primary undervoltage reset Monitor threshold	$V_{LVDRST5}$ CC	2.3	-	2.72	V	Power-down
		2.4	-	2.75	V	Power-up
V_{EVRSB} LVD Primary undervoltage reset Monitor threshold	$V_{LVDRSTSB}$ CC	2.18	-	2.47	V	Power-down
		2.21	-	2.5	V	Power-up
V_{EXT} and V_{EVRSB} PBIST primary overvoltage Monitor threshold	V_{PBIST5} CC	5.63	-	-	V	

表 3-31 电源监视器（续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Primary undervoltage reset threshold for V_{EXT} before trimming	V_{RST5} CC	-	-	3.0	V	by last cold PORST release on supply ramp-up including voltage hysteresis.
EVR secondary monitor measurement latency for all 6 supply rails	t_{MON} CC	-	-	3.2	µs	HPOSC and SHPBG bandgap trimmed. Filter inactive.

1) 电源上升时的复位释放在达到欠压复位阈值后会延迟 20-40 ms的时间，并且电压滞回会高于欠压复位限值 1.5%。这种机制有助于避免在电源缓慢上升期间，由于复位释放时压降/电流跳跃而导致的多个连续的冷 PORST 事件。引脚的复位限制为 2.97V，适用于 EVR33 内部产生 3.3V 的情况。如果外部提供 3.3V 电源，则键合线压降将导致 VDDP3 引脚上电压达到3.0V就复位。

2) 监测器公差构成了带隙和 ADC 在工艺、电压和温度操作范围内的固有变化。VxxPRIUV 参数在生产过程中经过单独测试，与 VxxPRIUV 限值有 +-1% 的公差。所有电压均在引脚上测量。

3) VRSTxx 参数仅与第一次冷 PORST 释放相关。随后，在器件以完整性能使用之前，复位电平由固件调整并反映为 VxxPRIUV 参数。冷 PORST 通过所有主监视器上的电压滞回释放，以避免连续的 PORST 切换行为。

4) 如果应用程序使用 3.3V 单电源（单电源模式 (e)，即当 VEXT 与 VDDP3 短接时，建议在通道 VDDP3 上使用二次电源监控，因为 VDDP3MON 参数的精度更高。

5) 对于未提供监视器电压电平的条件， OV和UV阈值可以根据给定的点通过线性插值或外推生成。

表 3-32 电源斜坡

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
External V_{EXT} & V_{EVRSB} supply ramp-up and ramp-down slope 1) 2) 3)	$dVEXT/dt$ SR	8.3E-6	1	100	V/ms	
External V_{DDP3} supply ramp-up and ramp-down slope 1)3)	$dVDDP3/dt$ SR	8.3E-6	1	100	V/ms	
External V_{DD} supply ramp-up and ramp-down slope 1)3)	$dVDD/dt$ SR	8.3E-6	1	100	V/ms	
External V_{DDM} supply ramp-up and ramp-down slope 1)3)	$dVDDM/dt$ SR	8.3E-6	1	100	V/ms	

1) 该器件具有很强的抗残余电压上升能力，对于 VEXT、VEVRSB、VDDP3 和 VDDM，电压上升范围为 0 - 2.97 V，对于 VDD，电压上升范围为 0-1 V。稳健性验证涵盖 0.5V/min 至 120V/ms 之间的 VEXT 电压斜坡范围。

2) 在使用 EVR33 或 EVRC 的情况下也有效。产生的电压本身在 tSTR 时间内遵循软上升趋势，以避免过冲。

3) 斜率定义为 0% 至 100% 电压电平之间的最大切向斜率。实际波形可能不同于规格书。

TC36x 允许最多 1000000 次电源循环，符合“电源斜坡”表中定义的限制，且对可靠性没有任何限制。

表 3-33 EVRC SMPS

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input V_{EXT} Voltage range	V_{IN} SR	2.97	-	5.5	V	Start-up VEXT voltage > 2.6 V
SMPS regulator output voltage range including load/line regulation and aging	V_{DDDC} CC	1.125	-	1.375	V	$V_{EXT} \geq 2.97V$; $V_{EXT} \leq 5.5V$; $I_{DDDC} \geq 1mA$; $I_{DDDC} \leq 500mA$; untrimmed
SMPS regulator static voltage output accuracy after trimming without dynamic load/line regulation.	V_{DDDCT} CC	1.225	1.25	1.275	V	$V_{EXT} \geq 2.97V$; $V_{EXT} \leq 5.5V$; $I_{DDDC} \geq 1mA$; $I_{DDDC} \leq 500mA$
Programmable switching frequency	f_{DCDC} SR	1.6	1.82	2.0	MHz	Start-up frequency switches from 500 KHz in open loop operation to 1.82 MHz in closed loop Operation.
		-	0.8	-	MHz	Start-up frequency switches from 500 KHz in open loop operation to 1.82 MHz in closed loop Operation. 0.8 MHz to be set in SW.
Startup time	t_{STRDC} CC	-	-	900	µs	SMPS Start-up Mode. It is is defined beween $V_{EXTPRIUV}$ reset threshold till PORST release, on condition that all other PORST requirements were released before. I_{START} < 350mA.
Switching frequency modulation spread	Δf_{DCSPR} CC	-	1.8%	-	MHz	
Maximum ripple at I_{MAX}	ΔV_{DDDC} CC	-	-	16	mV	$V_{EXT} \geq 2.97V$; $V_{EXT} \leq 5.5V$; $I_{DDDC} \geq 300mA$; $I_{DDDC} \leq 500mA$; ΔV_{DDDC} = (Peak to Peak ripple / 2)
No load current consumption of SMPS regulator	I_{DCNL} CC	-	15	19	mA	f_{DCDC}=1.82MHz; I_{DDDC}=I_{SLEEP}; V_{EXT} > 2.97 V; T_J=25°C
		-	5	-	mA	LPM mode; I_{DDDC}=I_{SLEEP}; V_{EXT} > 2.97 V; T_J=25°C

表 3-33 EVRC SMPS （续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SMPS regulator load transient response	dV_{DDDCT} / dl_{OUT} CC	-50	-	75	mV	dI < -250mA ; I_{DDDC}=280-500mA; t_r=0.1us; t_f=0.1us; V_{DDDC}=1.25V; T_{settle}=100 us
		-26	-	26	mV	dI < 100mA ; I_{DDDC}=50-500mA; t_r=0.1us; t_f=0.1us; V_{DDDC}=1.25V; T_{settle}=20us;
Maximum output current	I_{MAX} CC	100	-	-	mA	LPM mode. Typical current in LPM Mode = I_{SLEEP}
		500	-	-	mA	limited by thermal constraints and component choice
SMPS regulator line transient response	dV_{DDDCT} / dV_{IN} CC	-75	-	75	mV	dV/dT=120V/ms; dV < 2.97 - 5.5V ; I_{DDDC}=50-500mA;
		-12.5	-	12.5	mV	dV/dT=1V/ms; dV < 2.97 - 5.5V ; I_{DDDC}=50-500mA;
SMPS regulator efficiency	n_{DC} CC	-	80	-	%	V_{IN}=3.3V; I_{DDDC}=500mA; f_{DCDC}=1.82MHz
		-	75	-	%	V_{IN}=5V; I_{DDDC}=500mA; f_{DCDC}=1.82MHz
Input Synchronisation frequency	$f_{DCDCSYNC}$ SR	1.6	1.82	2.0	MHz	f_{DCDC} =1.82MHz
		0.66	0.8	0.94	MHz	f_{DCDC}=0.8MHz

表 3-34 EVRC SMPS 外部组件

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
External output capacitor value [1)]	C_{OUT} SR	13	20	27	µF	I_{DDDC}=500 mA; f_{DDDC} = 0.8MHz
		9.6	14.7	19.8	µF	I_{DDDC}=500mA; f_{DDDC} = 1.82MHz
External output capacitor ESR	C_{OUT_ESR} SR	-	-	50	mOhm	f≥0.5MHz ; f≤10MHz
		-	-	100	Ohm	f=10Hz
External input capacitor value [1)]	C_{IN} SR	4.42	6.8	9.18	µF	I_{DDDC}=500mA
External input capacitor ESR	C_{IN_ESR} SR	-	-	50	mOhm	f≥0.5MHz ; f≤10MHz
		-	-	100	Ohm	f=100Hz

表 3-34 EVRC SMPS 外部组件（续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
External inductor value	L_{DC} SR	3.29	4.7	6.11		f_{DCDC}=0.8MHz
		2.31	3.3	4.29	µH	f_{DCDC}=1.82MHz
External inductor DCR	L_{DC_DCR} SR	-	-	0.2	Ohm	
P + N-channel MOSFET logic level	V_{LL} SR	-	-	2.5	V	
P + N-channel MOSFET drain source breakdown voltage	$\|V_{BR\_DS}\|$ SR	+7	-	-	V	NMOS - V_{GS} = 0.
		-	-	-7	V	PMOS - V_{GS} = 0.
P + N-channel MOSFET drain source ON-state resistance	R_{ON} SR	-	200	-	mOhm	I_{DDDC}=500mA; $\|V_{GS}\|$=2.5V ; T_A=25°C
P + N-channel MOSFET Gate Charge	Q_G SR	-	-	4	nC	I_{DDDC}=500mA; NMOS- $\|V_{GS}\|$=5V; 0.5A pulsed drain current
		-4	-	-	nC	I_{DDDC}=500mA; PMOS- $\|V_{GS}\|$=5V; 0.5A pulsed drain current
External Inductor Saturation Current Margin	ΔI_{SAT} SR	400	-	-	mA	The saturation current of the coil must be larger than I_{DDDC} + ΔI_{SAT}
P + N-channel MOSFET Gate threshold voltage	V_{GSTH} SR	-	1	-	V	NMOS
		-	-1	-	V	PMOS
N-channel MOSFET reverse diode forward voltage	V_{RDN} SR	-	0.8	-	V	

1) 电容器最小-最大范围代表典型的 +-35% 公差，包括 DC 偏置效应。从电容器到电源或接地轨的走线电阻应限制为 25 mOhm。

3.16 系统锁相环 (SYS_PLL)

表 3-35 PLL 系统

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DCO Input frequency range	f_{REF} CC	10	-	40	MHz	
Modulation Amplitude	MA CC	0	-	2	%	
Peak Period jitter	DP CC	-200	-	200	ps	without modulation (PLL output frequency)
Peak Accumulated Jitter	D_{PP} CC	-5	-	5	ns	without modulation
Total long term jitter	J_{TOT} CC	-	-	11.5	ns	including modulation; MA 1.25%; f_{REF} 20MHz
System frequency deviation	f_{SYSD} CC	-	-	0.01	%	with active modulation
DCO frequency range	f_{DCO} CC	400	-	800	MHz	
PLL lock-in time	t_L CC	4	-	100	µs	

注释：如果每个引脚的电容负载在最大驱动器和锐边的情况下不超过 C_L = 20 pF，则指定的PLL 抖动值有效。

注释：电源电压上的最大峰峰值噪声限制为：噪声频率低于300 KHz时，V_{PP} = 100 mV；噪声频率高于300 KHz时，V_{PP} = 40 mV。这些条件可以通过在尽可能靠近电源引脚的位置适当阻断电源电压，并使用PCB 电源层和接地层来实现。

3.17 外设锁相环（PER_PLL）

表 3-36 PLL 外设

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Peak Accumulated jitter at SYSCLK pin	D_{PP} CC	-1000	-	1000	ps	Peak only
Peak accumulated jitter	D_{PPI} CC	-700	-	700	ps	Peak only
RMS Accumulated jitter	D_{RMS} CC	-100	-	100	ps	measured over 1 µs; f_{REF} = 20 MHz and f_{DCO} = 640 MHz or f_{REF} = 25 MHz and f_{DCO} = 800 MHz
Peak Period jitter	DP CC	-200	-	200	ps	f_{DCO} = 640 MHz or f_{DCO} = 800 MHz
Absolute RMS jitter (PLL out)	J_{ABS10} CC	-125	-	125	ps	f_{REF} = 10 MHz; f_{DCO} = 640 MHz
Absolute RMS jitter (PLL out)	J_{ABS20} CC	-85	-	85	ps	f_{REF} = 20 MHz; f_{DCO} = 640 MHz
Absolute RMS jitter (PLL out)	J_{ABS25} CC	-85	-	85	ps	f_{REF} = 25 MHz; f_{DCO} = 800 MHz
DCO frequency range	f_{DCO} CC	400	-	800	MHz	
DCO input frequency range	f_{REF} CC	10	-	40	MHz	
PLL lock-in time	t_L CC	4	-	100	µs	

注释：如果每个引脚的电容负载在最大驱动器和锐边的情况下不超过 C_L = 20 pF，则指定的PLL 抖动值有效。

注释：电源电压上的最大峰峰值噪声限制为：噪声频率低于300 KHz时，V_{PP} = 100 mV；噪声频率高于300 KHz时，V_{PP} = 40 mV。这些条件可以通过在尽可能靠近电源引脚的位置适当阻断电源电压，并使用PCB 电源层和接地层来实现。

3.18 AC规格

所有AC参数均由3.4章节中定义的完整操作范围指定，除非在“注释/测试条件”栏中另有说明。

除非图中另有说明，否则时间定义遵循以下准则：

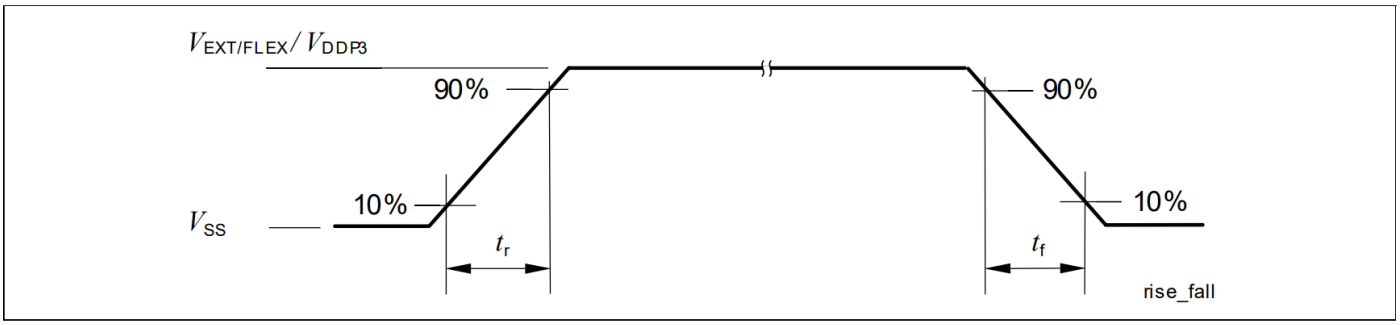


图 3-8 上升/下降时间的定义

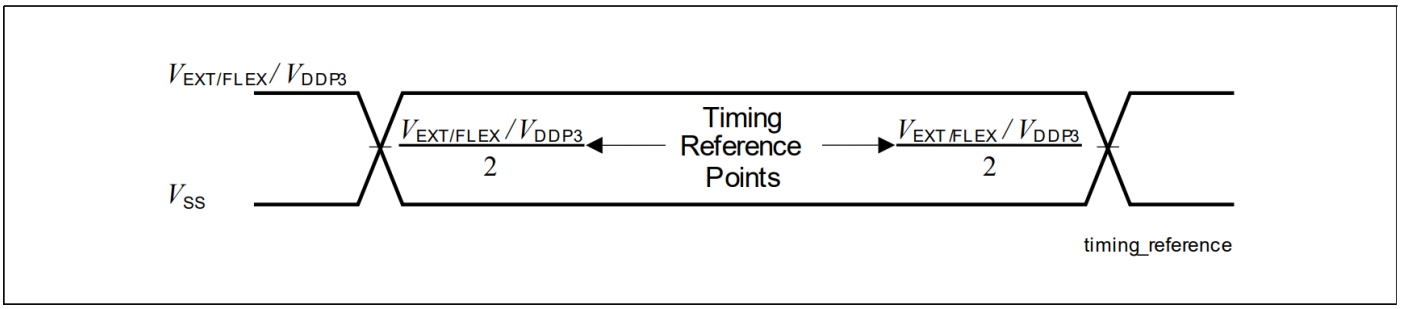


图 3-9 时间基准点定义

3.19 JTAG参数

以下参数适用于通过 JTAG 调试接口进行通信。JTAG模块完全符合IEEE1149.1-2000。

表 3-37 JTAG

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	50	-	-	ns	
TCK high time	t_2 SR	10	-	-	ns	
TCK low time	t_3 SR	10	-	-	ns	
TCK clock rise time	t_4 SR	-	-	4	ns	
TCK clock fall time	t_5 SR	-	-	4	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6.0	-	-	ns	
TDI/TMS hold after TCK rising edge	t_7 SR	6.0	-	-	ns	
TDO valid after TCK falling edge (propagation delay)	t_8 CC	3.0	-	-	ns	C_L≤20pF
		-	-	25	ns	C_L≤50pF
TDO hold after TCK falling edge	t_{18} CC	2	-	-	ns	
TDO high impedance to valid from TCK falling edge	t_9 CC	-	-	25	ns	C_L≤50pF
TDO valid output to high impedance from TCK falling edge	t_{10} CC	-	-	25	ns	C_L≤50pF

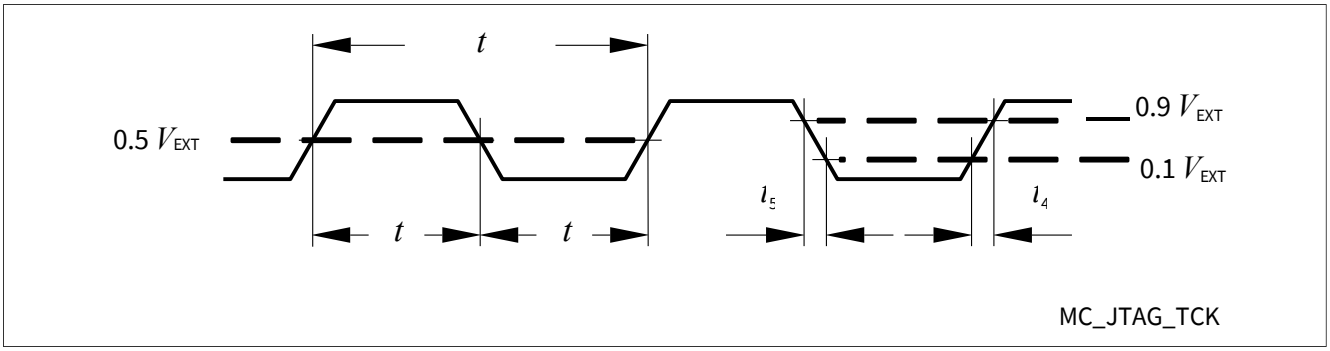


图3-10 测试时钟时序（TCK）

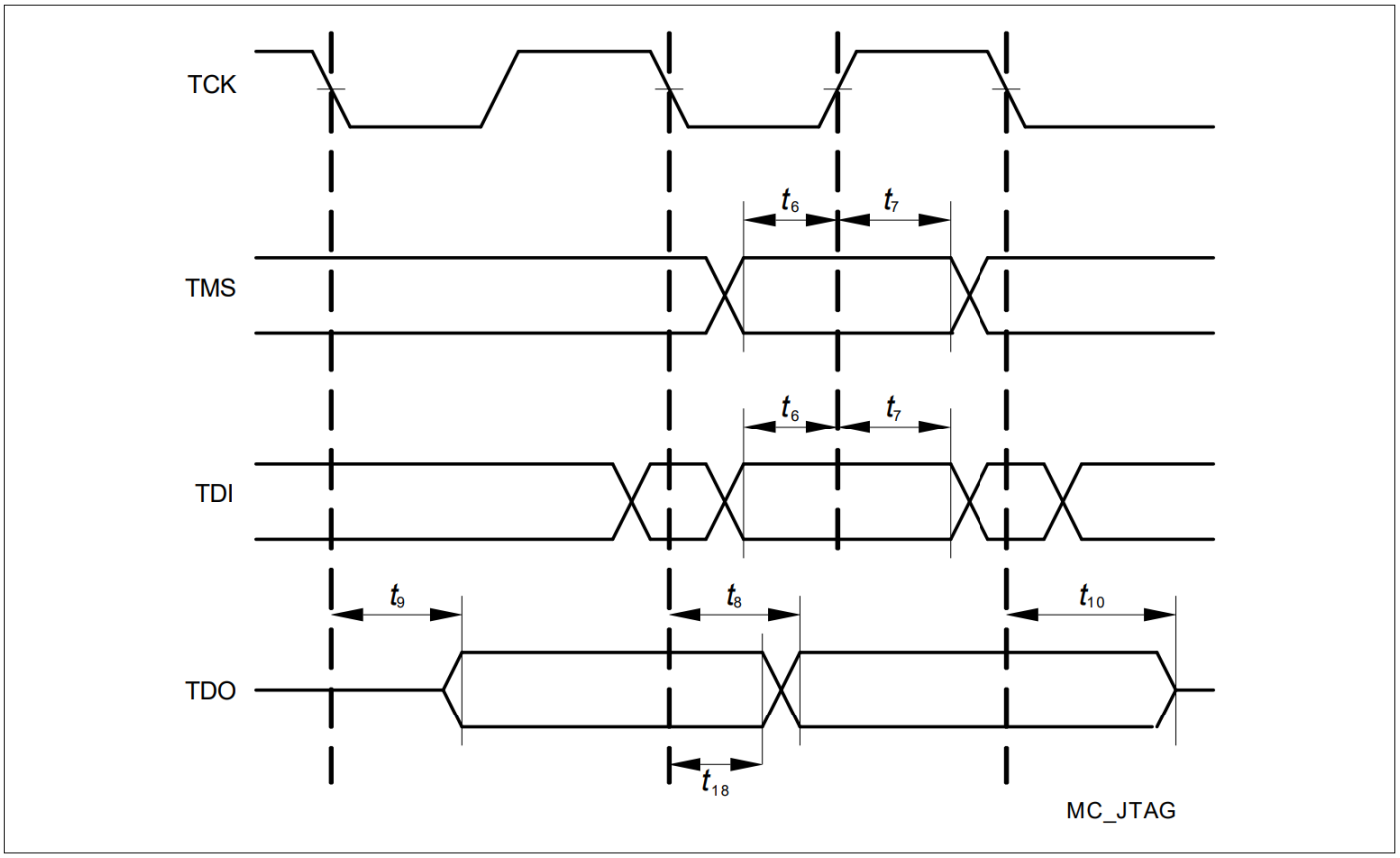


图 3-11 JTAG 时序

3.20 DAP 参数

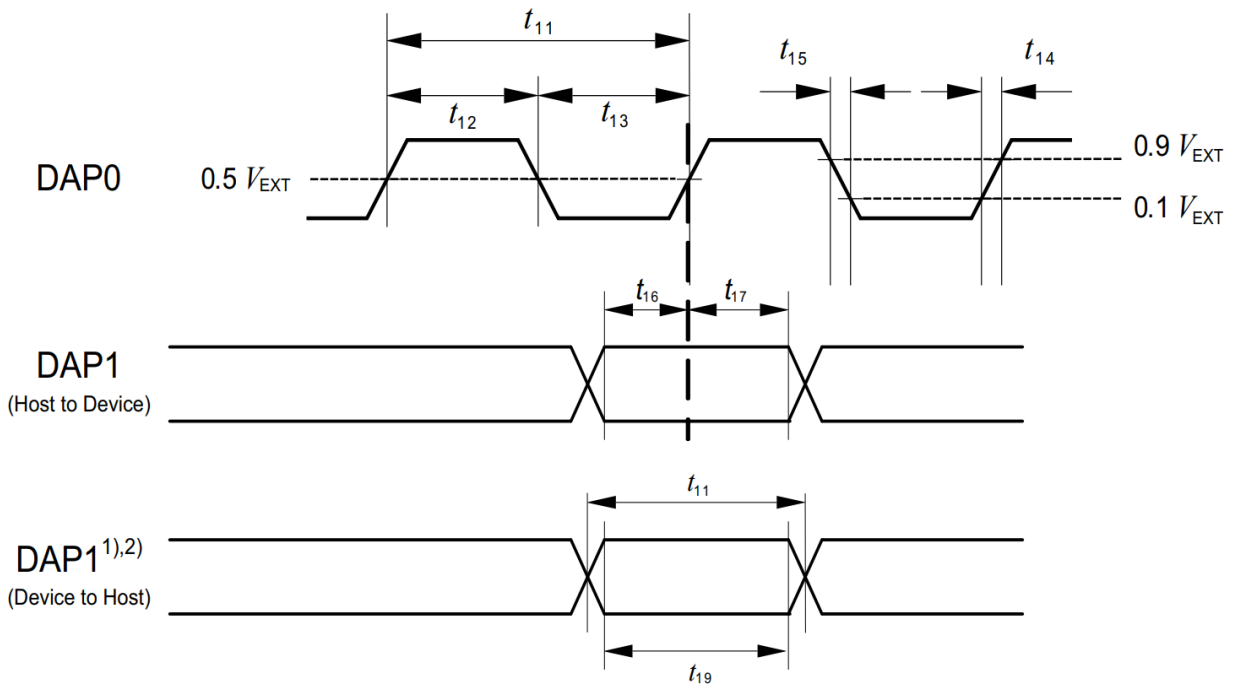
以下参数适用于通过 DAP 调试接口进行通信。

表 3-38 DAP

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock rise time	t_{14} SR	-	-	1	ns	f=160MHz
		-	-	4	ns	f=40MHz
		-	-	2	ns	f=80MHz
DAP0 clock fall time	t_{15} SR	-	-	1	ns	f=160MHz
		-	-	4	ns	f=40MHz
		-	-	2	ns	f=80MHz
DAP1 setup to DAP0 rising edge	t_{16} SR	4	-	-	ns	
		5	-	-	ns	f=40MHz
DAP1 hold after DAP0 rising edge	t_{17} SR	2	-	-	ns	
DAP1 valid per DAP0 clock period	t_{19} CC	4	-	-	ns	C_L=20pF ; f=160MHz
		8	-	-	ns	C_L=20pF ; f=80MHz
		10	-	-	ns	C_L=50pF ; f=40MHz
DAP0 high time	t_{12} SR	2	-	-	ns	
DAP0 low time	t_{13} SR	2	-	-	ns	
DAP0 clock period	t_{11} SR	6.25	-	-	ns	

表 3-39 SCR DAP

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock rise time	t_{14} SR	-	-	8	ns	f=20MHz
DAP0 clock fall time	t_{15} SR	-	-	8	ns	f=20MHz
DAP1 setup to DAP0 rising edge	t_{16} SR	10	-	-	ns	
DAP1 hold after DAP0 rising edge	t_{17} SR	10	-	-	ns	
DAP1 valid per DAP0 clock period	t_{19} CC	30	-	-	ns	C_L=20pF ; f=20MHz
DAP0 high time	t_{12} SR	15	-	-	ns	
DAP0 low time	t_{13} SR	15	-	-	ns	
DAP0 clock period	t_{11} SR	50	-	-	ns	



1) The DAP1 and DAP2 device to host timing is individual for both pins.
There is no guaranteed max. signal skew.
2) No explicite setup and hold times are given for DAP1 for the direction Device to Host.
Only t11 and t19 are guaranteed and the tool may set the sample point freely.

图 3-12 DAP 时序

注释：DAP1 和 DAP2 器件对主控器件的两个引脚都是单独的。 没有保证的最大信号偏差。

3.21 ASCLIN SPI 主时序

本节定义了 TC36x 中 ASCLIN 的时序。

注释：焊盘不对称已包含在以下时序中。

表 3-40 主模式强尖锐（ss）输出焊盘

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ASCLKO clock period	t_{50} CC	20	-	-	ns	C_L=25pF
Deviation from ideal duty cycle	t_{500} CC	-2	-	2	ns	C_L=25pF
MTSR delay from ASCLKO shifting edge	t_{51} CC	-3.5	-	3.5	ns	C_L=25pF
ASLSOn delay from the first ASCLKO edge	t_{510} CC	-3	-	3.5	ns	C_L=25pF
MRST setup to ASCLKO latching edge	t_{52} SR	25	-	-	ns	C_L=25pF
MRST hold from ASCLKO latching edge	t_{53} SR	-2	-	-	ns	C_L=25pF

表 3-41 主模式强中型（sm）输出焊盘

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ASCLKO clock period	t_{50} CC	50	-	-	ns	C_L=50pF
Deviation from ideal duty cycle	t_{500} CC	-5	-	5	ns	C_L=50pF
MTSR delay from ASCLKO shifting edge	t_{51} CC	-7	-	7	ns	C_L=50pF
ASLSOn delay from the first ASCLKO edge	t_{510} CC	-7	-	7	ns	C_L=50pF
MRST setup to ASCLKO latching edge	t_{52} SR	35	-	-	ns	C_L=50pF
MRST hold from ASCLKO latching edge	t_{53} SR	-5	-	-	ns	C_L=50pF

表 3-42 主模式中型（m）输出焊盘

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ASCLKO clock period	t_{50} CC	160	-	-	ns	C_L=50pF
Deviation from ideal duty cycle	t_{500} CC	-10	-	10	ns	C_L=50pF
MTSR delay from ASCLKO shifting edge	t_{51} CC	-20	-	20	ns	C_L=50pF
ASLSOn delay from the first ASCLKO edge	t_{510} CC	-20	-	20	ns	C_L=50pF

表 3-42 主模式中型（m）输出焊盘（续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MRST setup to ASCLKO latching edge	t_{52} SR	80	-	-	ns	C_L=50pF
MRST hold from ASCLKO latching edge	t_{53} SR	-15	-	-	ns	C_L=50pF

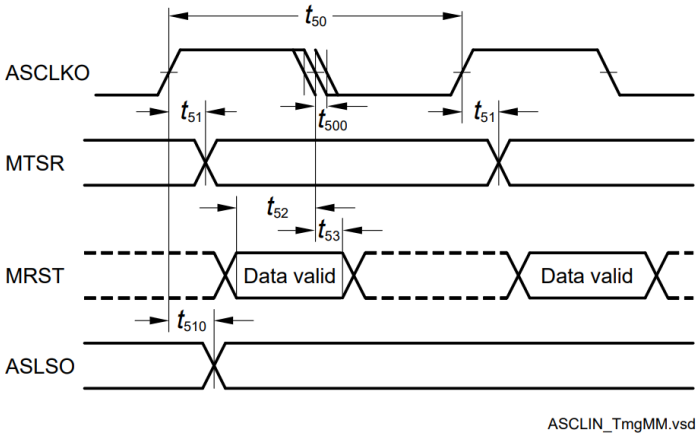


图 3-13 ASCLIN SPI 主机时序

3.22 QSPI 时序、主模式和从模式

本节定义了 TC36x 中 QSPI 的时序。

假设 SCLKO、MTSR 和 SLSO 焊盘具有相同的焊盘设置：

注释：焊盘不对称已包含在以下时序中。

表 3-43 主模式时序，LVDS 数据和时钟输出焊盘

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period	t_{50} CC	20 [1]	-	-	ns	CL=25pF
Deviation from the ideal duty cycle	t_{500} CC	-1 [1]	-	1 [1]	ns	CL=25pF
MTSR delay from SCLKO shifting edge	t_{51} CC	-3 [1]	-	4 [1]	ns	CL=25pF
SLSOn deviation from the ideal programmed position	t_{510} CC	-4 [1]	-	5.5 [1]	ns	C_L=25pF, driver strength ss
		-10 [1]	-	10 [1]	ns	C_L=25pF, driver strength sm
		-30 [1]	-	30 [1]	ns	C_L=25pF, driver strength m
MRST setup to SCLK latching edge	t_{52} SR	18 [1]	-	-	ns	CL=25pF; valid for LVDS Input pads of QSPI2 only
MRST hold from SCLK latching edge	t_{53} SR	-1 [1]	-	-	ns	CL=25pF; valid for LVDS Input pads only

1) 条件列表中定义的负载（C_L=25pF）是针对单端信号 SLSO 的负载定义，并不旨在在差分信号线内添加额外负载。对于单端信号，负载定义定义了 PCB 布局上信号的最大长度。对于 LVDS 焊盘，适用 IEEE Std 1596.3-1996 负载定义。

表 3-44 主模式强尖锐（ss）输出焊盘

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period	t_{50} CC	50	-	-	ns	CL=25pF
Deviation from the ideal duty cycle	t_{500} CC	-2	-	2	ns	CL=25pF
MTSR delay from SCLKO shifting edge	t_{51} CC	-4	-	5	ns	CL=25pF
SLSOn deviation from the ideal programmed position	t_{510} CC	-4	-	5	ns	CL=25pF
MRST setup to SCLK latching edge	t_{52} SR	25 [1] [2]	-	-	ns	CL=25pF
MRST hold from SCLK latching edge	t_{53} SR	-2 [1][2]	-	-	ns	CL=25pF

1) 为了补偿平均片上延迟，QSPI 模块提供了位域 ECONz.A、B 和 C。

2) 建立和保持时间对于输入焊盘阈值的两种设置均有效：TTL 和 AL。

表 3-45 主模式强中型（sm）输出焊盘

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period	t_{50} CC	50	-	-	ns	CL=50pF
Deviation from the ideal duty cycle	t_{500} CC	-5	-	5	ns	CL=50pF
MTSR delay from SCLKO shifting edge	t_{51} CC	-7	-	7	ns	CL=50pF
SLSOn deviation from the ideal programmed position	t_{510} CC	-7	-	7	ns	CL=50pF
MRST setup to SCLK latching edge	t_{52} SR	35 1) 2)	-	-	ns	CL=50pF
MRST hold from SCLK latching edge	t_{53} SR	-5 1)2)	-	-	ns	CL=50pF

1) 为了补偿平均片上延迟，QSPI 模块提供了位域 ECONz.A、B 和 C。

2) 建立和保持时间对于输入焊盘阈值的两种设置均有效：TTL 和 AL。

表 3-46 主模式中型（m）输出焊盘

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period	t_{50} CC	160	-	-	ns	CL=50pF
Deviation from the ideal duty cycle	t_{500} CC	-10	-	10	ns	CL=50pF
MTSR delay from SCLKO shifting edge	t_{51} CC	-20	-	20	ns	CL=50pF
SLSOn deviation from the ideal programmed position	t_{510} CC	-20	-	20	ns	CL=50pF
MRST setup to SCLK latching edge	t_{52} SR	80 1) 2)	-	-	ns	CL=50pF
MRST hold from SCLK latching edge	t_{53} SR	-15 1)2)	-	-	ns	CL=50pF
		-13 1)2)	-	-	ns	CL=50pF; SCR SSC

1) 为了补偿平均片上延迟，QSPI 模块提供了位域 ECONz.A、B 和 C。

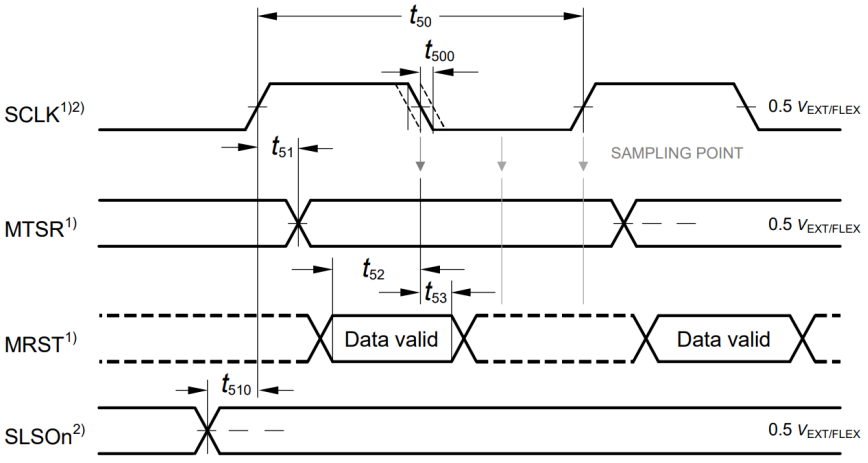
2) 建立和保持时间对于输入焊盘阈值的两种设置均有效：TTL 和 AL。

表 3-47 从模式时序

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLK clock period	t_{54} SR	4 x T_{MAX}	-	-	ns	
SCLK duty cycle	$t_{55/t54}$ SR	40	-	60	%	
MTSR setup to SCLK latching edge	t_{56} SR	6	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL

表 3-47 从模式时序（续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MTSR hold from SCLK latching edge	t_{57} SR	4	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
SLSI setup to first SCLK shift edge	t_{58} SR	4	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
SLSI hold from last SCLK latching edge	t_{59} SR	3	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
MRST delay from SCLK shift edge	t_{60} CC	5	-	35	ns	driver = strong edge = medium ; C_L=50pF
		2	-	24	ns	driver = strong edge = sharp ; C_L=50pF
		15	-	80	ns	medium driver ; C_L=50pF
		14	-	-	ns	medium driver ; C_L=50pF; SCR SSC



1) This timing is based on the following setup: ECON.CPH = 1, ECON.CPOL = 0, ECON.B=0 (no sampling point delay).

2) t510 is the deviation from the ideal position configured with the leading delay, BACON.LPRE and BACON.LEAD > 0.

QSPI_TmgMM.vsd

图 3-14 主模式时序

电气规格 QSPI 时序、主从模式

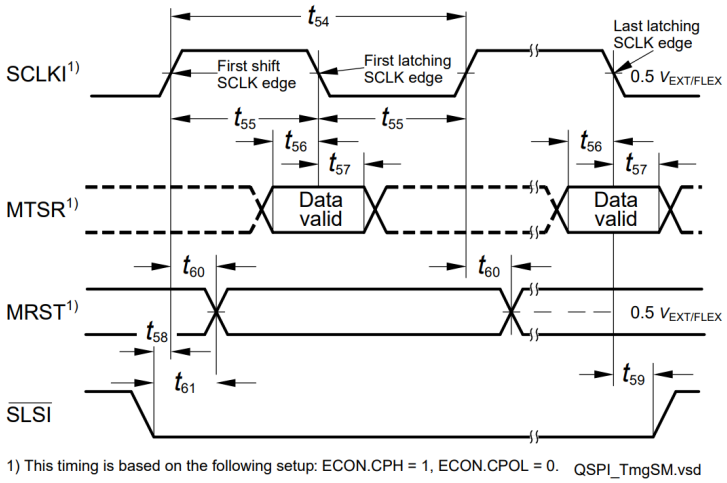


图3-15 从模式时序

3.23 MSC 时序 5 V 操作

以下部分定义了时序。

注释：焊盘不对称已包含在以下时序中。

注释：LVDS焊盘的负载在下列时序中定义为差分负载。

表 3-48 5V 下的 LVDS 时钟/数据（LVDS 模式下的 LVDS 焊盘）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FCLPx clock period	t_{40} CC	2 * T_{A} 1) 2) 3)	-	-	ns	LVDS; C_L=50pF
Deviation from ideal duty cycle	t_{400} CC	-1 3)	-	1 3)	ns	LVDS; 0 < C_L < 50pF
SOPx output delay	t_{44} CC	-3 3)	-	3 3)	ns	CL=50pF
ENx output delay	t_{45} CC	-4 3)	-	5 3)	ns	ss; C_L=50pF; ABRA block bypassed
		-4 3)	-	4 3)	ns	ss; C_L=50pF; ABRA block used
		-2 3)	-	10 3)	ns	sm; C_L=50pF
		-30 3)	-	30 3)	ns	m; C_L=50pF

1) T_A取决于为MSC的 ABRA 功能块中的波特率生成选择的时钟源。

2) LVDS引脚上的容性负载是差分的，CMOS 引脚上的容性负载是单端的。

3) 条件列表中定义的负载（ C_L =50pF）是针对单端信号 EN 的负载定义，并不旨在在差分信号线内添加额外负载。对于单端信号，负载定义定义了 PCB 布局上信号的最大长度。对于 LVDS 焊盘，适用 IEEE Std 1596.3-1996 负载定义。

表 3-49 5V下的强尖锐（ss）时钟/数据驱动器

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FCLPx clock period	t_{40} CC	2 * T_{A}	-	-	ns	CL=50pF
Deviation from ideal duty cycle	t_{400} CC	-2	-	2	ns	CL=50pF
SOPx output delay	t_{44} CC	-4	-	3.5	ns	CL=50pF
ENx output delay	t_{45} CC	-4	-	3.5	ns	CL=50pF

表 3-50 5V下的强中型（sm）时钟/数据驱动器

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FCLPx clock period	t_{40} CC	2 * T_{A}	-	-	ns	CL=50pF
Deviation from ideal duty cycle	t_{400} CC	-5	-	5	ns	CL=50pF
SOPx output delay	t_{44} CC	-7	-	7	ns	CL=50pF
ENx output delay	t_{45} CC	-7	-	7	ns	CL=50pF

表 3-51 5V下的中等（m）时钟/数据驱动器

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FCLPx clock period	t_{40} CC	2 * T_A	-	-	ns	CL=50pF
Deviation from ideal duty cycle	t_{400} CC	-10	-	10	ns	CL=50pF
SOPx output delay	t_{44} CC	-20	-	20	ns	CL=50pF
ENx output delay	t_{45} CC	-20	-	20	ns	CL=50pF

表 3-52 上行接口

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SDI bit time	t_{46} SR	8 * t_{MSC}	-	-	ns	
SDI rise time	t_{48} SR	-	-	200	ns	
SDI fall time	t_{49} SR	-	-	200	ns	

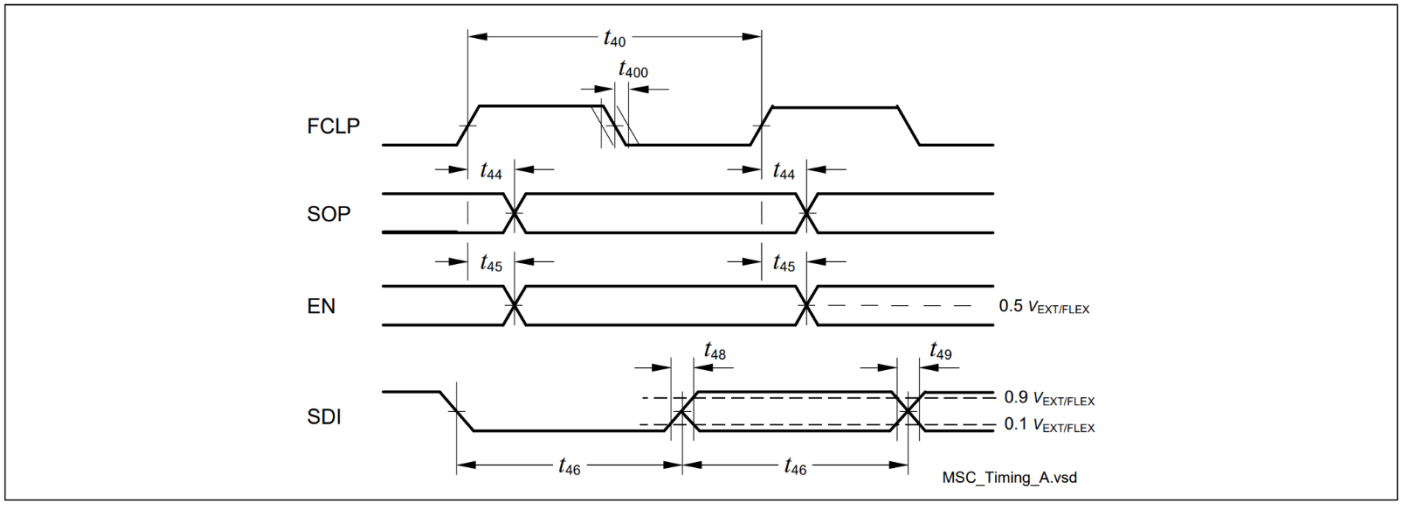


图 3-16 MSC 接口时序

注释：SOP数据信号是在目标器件中的FCLP的下降沿进行采样的。

3.24 以太网接口 (ETH) 特性

3.24.1 ETH 测量参考点

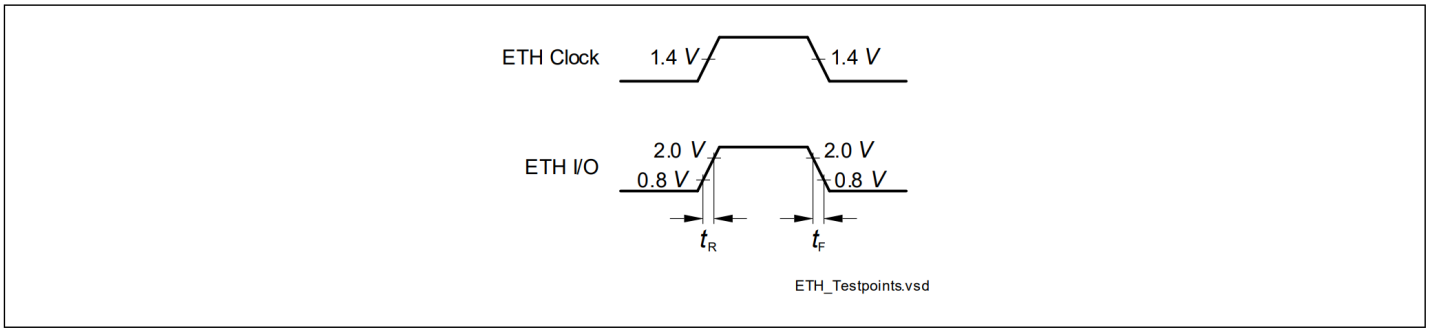


图 3-17 ETH 测量参考点

3.24.2 ETH管理信号参数（ETH_MDC、ETH_MDIO）

表 3-53 适用于 3.3 V 的 ETH 管理信号参数

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ETH_MDC period	t_1 CC	400	-	-	ns	CL=25pF
ETH_MDC high time	t_2 CC	160	-	-	ns	CL=25pF
ETH_MDC low time	t_3 CC	160	-	-	ns	CL=25pF
ETH_MDIO setup time (output)	t_4 CC	10	-	-	ns	CL=25pF
ETH_MDIO hold time (output)	t_5 CC	10	-	-	ns	CL=25pF
ETH_MDIO data valid (input)	t_6 SR	0	-	300	ns	CL=25pF

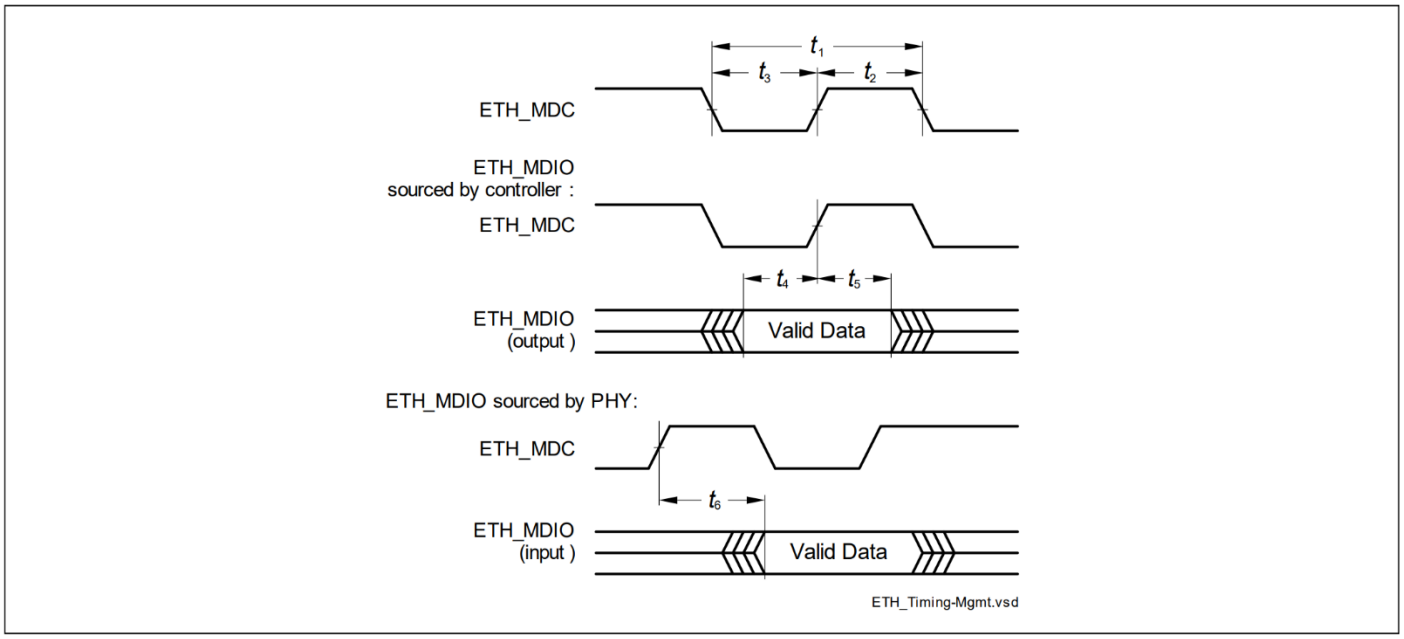


图 3-18 ETH 管理信号时序

3.24.3 ETH MII 参数

下面介绍 MII（媒体独立接口）的参数。

表 3-54 ETH MII 信号时序参数

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_7 SR	-	40	-	ns	CL=25pF ; baudrate=100Mbps
		-	400	-	ns	CL=25pF ; baudrate=10Mbps
Clock high time	t_8 SR	14	-	26	ns	CL=25pF ; baudrate=100Mbps
		140 1)	-	260 2)	ns	CL=25pF ; baudrate=10Mbps
Clock low time	t_9 SR	14	-	26	ns	CL=25pF ; baudrate=100Mbps
		140 1)	-	260 2)	ns	CL=25pF ; baudrate=10Mbps
Input setup time	t_{10} SR	10	-	-	ns	CL=25pF
Input hold time	t_{11} SR	10	-	-	ns	CL=25pF
Output valid time	t_{12} CC	0	-	25	ns	CL=25pF

1) 按时钟周期的 35% 定义。

2) 按时钟周期的 65% 定义。

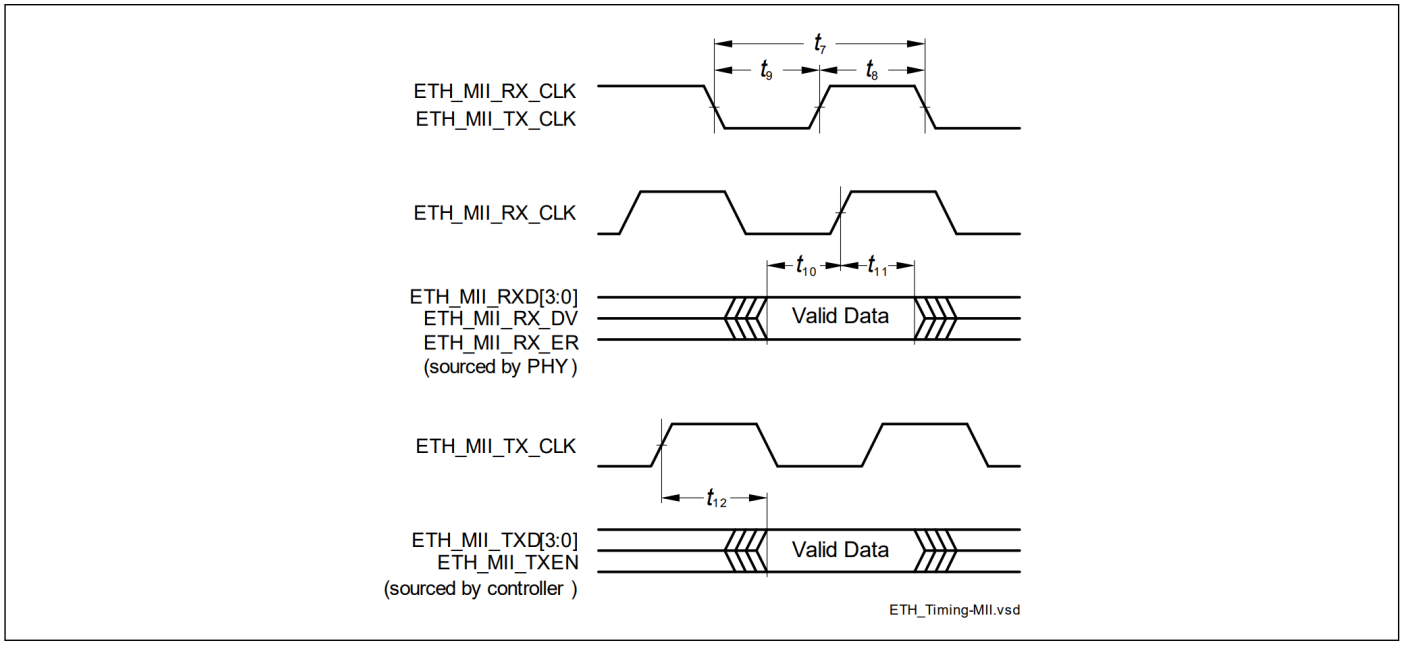


图 3-19 ETH MII 信号时序

3.24.4 ETH RMII 参数

下面介绍RMII（精简媒体独立接口）的参数。

表 3-55 适用于 3.3V 的 ETH RMII 信号时序参数

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ETH_RMII_REF_CL clock period	t_{13} SR	-	20	-	ns	50ppm ; CL=25pF
ETH_RMII_REF_CL clock high time	t_{14} SR	7 [1]	-	13 [2]	ns	CL=25pF
ETH_RMII_REF_CL clock low time	t_{15} SR	7 [1]	-	13 [2]	ns	CL=25pF
ETHTXEN, ETHTXD[1:0], ETHRXD[1:0], ETHCRSDV; setup time [3]	t_{16} CC	4	-	-	ns	CL=25pF
ETHTXEN, ETHTXD[1:0], ETHRXD[1:0], ETHCRSDV; hold time [3]	t_{17} CC	2	-	-	ns	CL=25pF

1) 按时钟周期的 35% 定义。

2) 按时钟周期的 65% 定义。

3) 对于 ETHRXD 和 ETHCRSDV 信号，此参数是 SR。

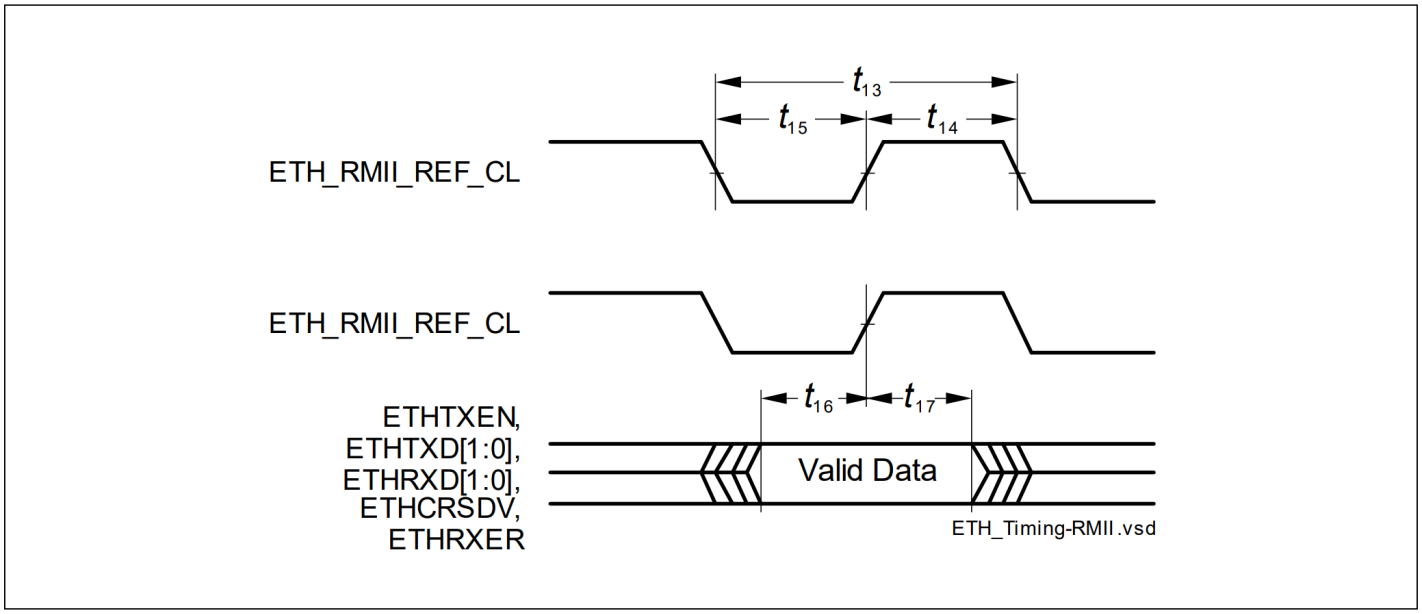


图 3-20 ETH RMII 信号时序

3.24.5 ETH RGMII 参数

下面介绍RGMII的参数。

表 3-56 适用于 3.3V 的 ETH RMII 信号时序参数

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TX Clock period	t_{19} CC	36	40	44	ns	100Mbps
		360	400	440	ns	10Mbps
		7.2	8	8.8	ns	Gigabit
Data to Clock Output skew	t_{20} CC	-500	0	500	ps	
Data to Clock input skew (at receiver)	t_{21} SR	1	1.8	2.6	ns	
Clock duty cycle	t_{duty} CC	40	50	60	%	10/100Mbps
		45	50	55	%	Gigabit
GREFCLK duty cycle	t_{duty_in} SR	45	-	55	%	
GREFCLK Input accuracy	ACC SR	-0.005	-	0.005	%	

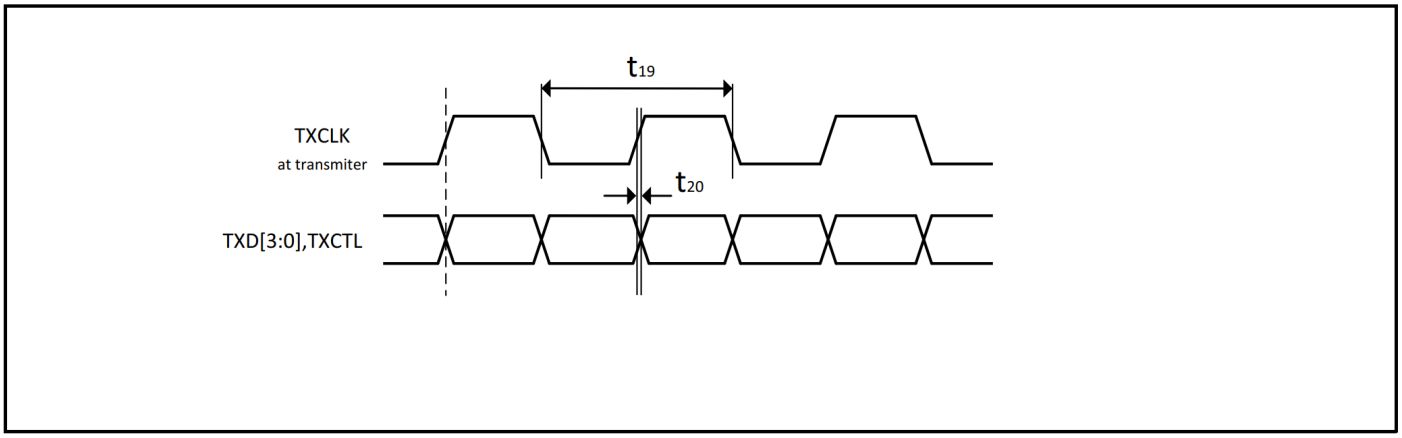


图 3-21 ETH RGMII TX 信号时序（目的地延迟 (DoD)）

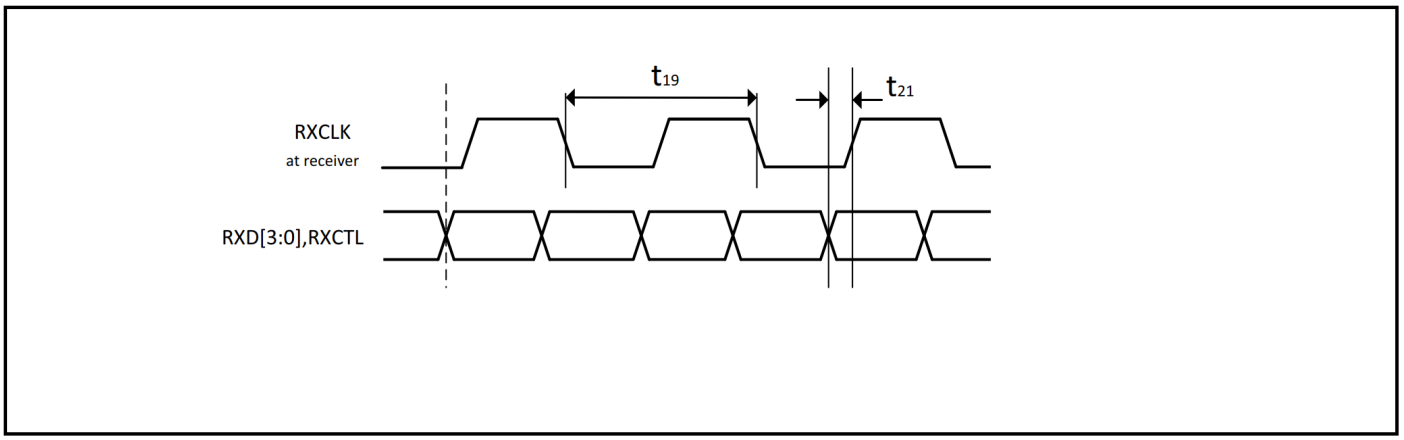


图 3-22 ETH RGMII RX 信号时序（源延迟（DoS））

3.25 E-Ray 参数

本节的时序适用于C_L = 25 pF 的输出驱动器的强驱动器和锐边设置。

表 3-57 发送参数

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise time of TxEN	$t_{dCCTxENRise25}$ CC	-	-	9	ns	C_L=25pF
Fall time of TxEN	$t_{dCCTxENFall25}$ CC	-	-	9	ns	C_L=25pF
Sum of rise and fall time	$t_{dCCTxRise25+dCCTxFall25}$ CC	-	-	9	ns	20% - 80% ; C_L=25pF
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, rising edge of TxEN	$t_{dCCTxEN01}$ CC	-	-	25	ns	
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, falling edge of TxEN	$t_{dCCTxEN10}$ CC	-	-	25	ns	
Asymmetry of sending	t_{tx_asym} CC	-2.45	-	2.45	ns	C_L=25pF
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, rising edge of TxD	$t_{dCCTxD01}$ CC	-	-	25	ns	
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, falling edge of TxD	$t_{dCCTxD10}$ CC	-	-	25	ns	
TxD signal sum of rise and fall time at TP1_BD	t_{txd_sum} CC	-	-	9	ns	

表 3-58 接收参数

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Acceptance of asymmetry at receiving part	$t_{dCCTxAsymAccept25}$ SR	-30.5	-	43.0	ns	C_L=25pF
Acceptance of asymmetry at receiving part	$t_{dCCTxAsymAccept15}$ SR	-31.5	-	44.0	ns	C_L=15pF
Threshold for detecting logical high	$T_{uCCLogic1}$ SR	35	-	70	%	
Threshold for detecting logical low	$T_{uCCLogic0}$ SR	30	-	65	%	

表 3-58 接收参数（续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Sum of delay between TP4_CC and TP4_FF and delays derived from TP4_FFi, rising edge of RxD	$t_{dCCRxD01}$ CC	-	-	10	ns	
Sum of delay between TP4_CC and TP4_FF and delays derived from TP4_FFi, falling edge of RxD	$t_{dCCRxD10}$ CC	-	-	10	ns	

3.26 HSCT 参数

表 3-59 HSCT - Rx 寄生参数和负载

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Capacitance total budget	C_{total} CC	-	3.5	5	pF	Total Budget for complete receiver including silicon, package, pins and bond wire
Parasitic inductance budget	$Htotal$ CC	-	5	-	nH	

表 3-60 HSCT - Rx/Tx 设置时序

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RX o/p duty cycle	$DCrx$ CC	40	-	60	%	
Disable time of the LVDS pad	$t_{LVDSDIS}$ CC	-	-	20	ns	
Enable time of the LVDS pad	t_{LVDSEN} CC	-	-	400	ns	
Wakeup time from Sleep Mode	t_{SWU} CC	-	-	250	ns	
Maximum length of a wake-up glitch that does not wake-up the receiver	t_{WUP} CC	-	-	0.2	ns	
Bias startup time	t_{bias} CC	-	5	10	µs	Bias distributor waking up from power down and provide stable Bias.
RX startup time	t_{rxi} CC	-	-	600	ns	Wake-up RX from power down.
TX startup time	t_{tx} CC	-	-	280	ns	Wake-up TX from power down.

3.27 Inter-IC (I2C) 接口时序

所有 I2C 时序参数均为主模式的 SR 和从模式的 CC。

表 3-61 I2C 标准模式时序

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1	-	-	300	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Capacitive load for each bus line	C_b SR	-	-	400	pF	
Bus free time between a STOP and ATART condition	t_{10}	4.7	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Rise time of both SDA and SCL	t_2	-	-	1000	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Data hold time	t_3	0	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Data set-up time	t_4	250	-	-	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Low period of SCL clock	t_5	4.7	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
High period of SCL clock	t_6	4	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Hold time for the (repeated) START condition	t_7	4	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Set-up time for (repeated) START condition	t_8	4.7	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Set-up time for STOP condition	t_9	4	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line

表 3-62 I2C 快速模式时序

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1	20+0.1*C_b	-	300	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Capacitive load for each bus line	C_b SR	-	-	400	pF	
Bus free time between a STOP and ATART condition	t_{10}	1.3	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Rise time of both SDA and SCL	t_2	20+0.1*C_b	-	300	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Data hold time	t_3	0	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Data set-up time	t_4	100	-	-	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Low period of SCL clock	t_5	1.3	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
High period of SCL clock	t_6	0.6	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Hold time for the (repeated) START condition	t_7	0.6	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Set-up time for (repeated) START condition	t_8	0.6	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Set-up time for STOP condition	t_9	0.6	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line

表 3-63 I2C 高速模式时序

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Capacitive load for each bus line	C_b SR	-	-	400	pF	
Fall time of SCL	t_{11}	10 [1]	-	40 [1]	ns	bus line load of 100pF
Fall time of SDA	t_{12}	10 [1]	-	80 [1]	ns	bus line load of 100pF
Rise time of SCL	t_{13}	10 [1]	-	40 [1]	ns	bus line load of 100pF
Rise time of SDA	t_{14}	10 [1]	-	80 [1]	ns	bus line load of 100pF
Data hold time	t_3	0 [1]	-	70 [1]	ns	bus line load of 100pF
Data set-up time	t_4	10 [1]	-	-	ns	bus line load of 100pF
Low period of SCL clock	t_5	160 [1]	-	-	ns	bus line load of 100pF
High period of SCL clock	t_6	60 [1]	-	-	ns	bus line load of 100pF
Hold time for the (repeated) START condition	t_7	160 [1]	-	-	ns	bus line load of 100pF
Set-up time for (repeated) START condition	t_8	160 [1]	-	-	ns	bus line load of 100pF
Set-up time for STOP condition	t_9	160 [1]	-	-	ns	bus line load of 100pF

1) 电容值定义为 C_b = 100pF，有关 C_b = 400pF 的时序， 请参阅 I2C 标准。

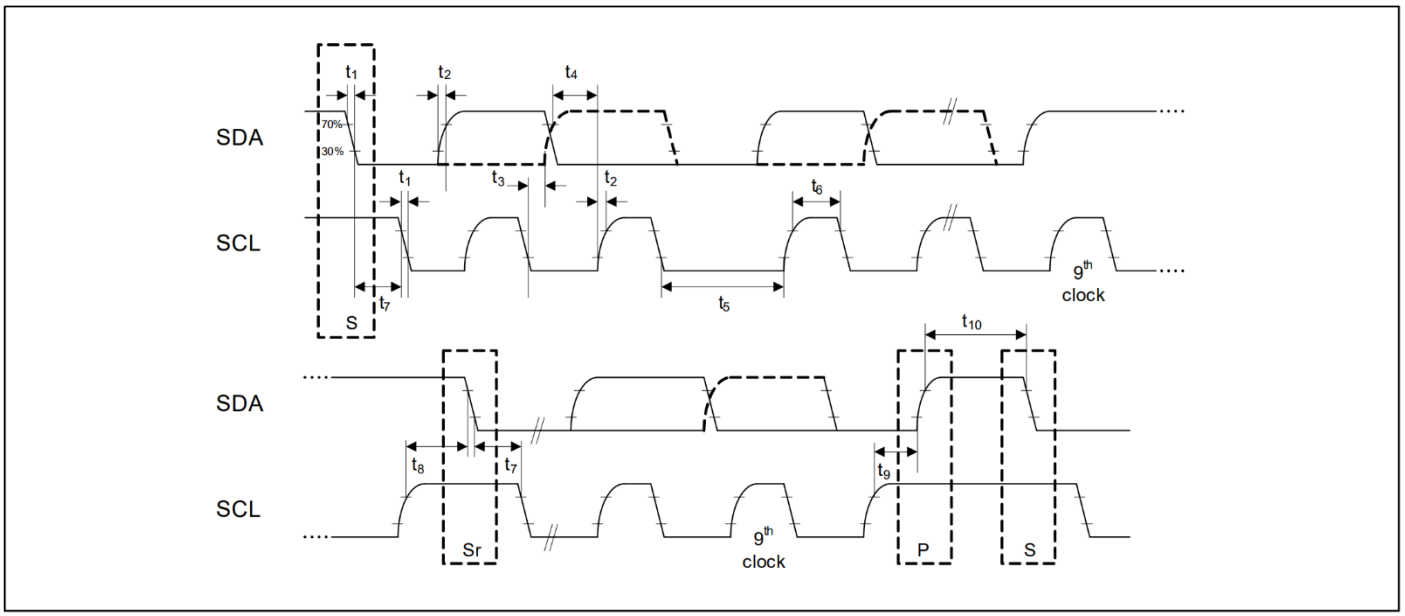


图 3-23 I2C 标准模式和快速模式时序

3.28 Flash 目标参数

表 3-64 Flash

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Program Flash Erase Time per logical sector [1]	t_{ERP} CC	-	-	0.5	s	cycle count < 1000
Program Flash Erase Time per Multi-Sector Command [1]	t_{MERP} CC	-	-	0.5	s	For consecutive logical sectors in a physical sector with total range ≤ 512 kByte; cycle count < 1000
Program Flash program time per page in 5 V mode [1]	t_{PRP5} CC	-	-	80	µs	32 Byte
Program Flash program time per page in 3.3 V mode [1]	t_{PRP3} CC	-	-	115	µs	32 Byte
Program Flash program time per burst in 5 V mode [1]	t_{PRPB5} CC	-	-	220	µs	256 Byte
Program Flash program time per burst in 3.3 V mode [1]	t_{PRPB3} CC	-	-	530	µs	256 Byte
Program Flash program time for 1 MByte with burst programming in 3.3 V mode excluding communication [1]	t_{PRPB3_1MB} CC	-	-	2.2	s	Derived value for documentation purpose
Program Flash program time for 1 MByte with burst programming in 5 V mode excluding communication [1]	t_{PRPB5_1MB} CC	-	-	1	s	Derived value for documentation purpose
Program Flash program time for complete PFlash with burst programming in 5 V mode excluding communication [1]	t_{PRPB5_PF} CC	-	-	4	s	Derived value for documentation purpose
Write Page Once adder [1]	t_{ADD} CC	-	-	20	µs	Adder to Program Time when using Write Page Once
Program Flash suspend to read latency [1]	t_{SPNDP} CC	-	-	120	µs	For Write Burst, Verify Erased and for multi-(logical) sector erase commands
Data Flash Erase Disturb Limit (single ended sensing mode)	N_{DFD} CC	-	-	50	cycles	
Data Flash Erase Disturb Limit (complement sensing mode)	N_{DFDC} CC	-	-	500	cycles	
UCB Erase Disturb Limit	N_{UCBD} CC	-	-	500	cycles	

表 3-64 Flash（续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Program time data flash per page [1)2)]	t_{PRD} CC	-	-	75	µs	8 Byte
Complete Device Flash Erase Time PFlash and DFlash [1)3) 4) 5)]	t_{ER_Dev} CC	-	3	5	s	Valid for less than 1000 cycles, w/o UCB. Derived value for documentation purpose.
Data Flash program time per burst [1)2)]	t_{PRDB} CC	-	-	140	µs	32 Byte
Data Flash suspend to read latency [1)]	t_{SPNDD} CC	-	-	120	µs	
Wait time after margin change	$t_{FL\_MarginDel}$ CC	-	-	2	µs	
Program Flash Endurance per Logical Sector	N_{E_P} CC	-	-	1000	cycles	Replace logical sector command shall be used if a sector fails during erase or program
Number of erase operations per physical sector in program flash	N_{ERP} CC	-	-	16000	cycles	
Program Flash Retention Time, Sector	t_{RET} CC	20	-	-	years	Max. 1000 erase/program cycles
UCB Retention Time	t_{RTU} CC	20	-	-	years	Max. 100 erase/program cycles per UCB, max 500 erase/program cycles for all UCBs together
Data Flash access delay	t_{DF} CC	-	-	100	ns	see RFLASH of DMU register HF_DWAIT
Data Flash ECC Delay	t_{DFECC} CC	-	-	20	ns	see RECC of DMU register HF_DWAIT
Program Flash access delay	t_{PF} CC	-	-	30	ns	see RFLASH of DMU register HF_PWAIT
Program Flash ECC delay	t_{PFECC} CC	-	-	10	ns	see RECC and CECC of DMU register HF_PWAIT
Number of erase operations on DF0 over lifetime (complement sensing mode) [6)]	N_{ERD0C} CC	-	-	4000000	cycles	
Number of erase operations on DF0 over lifetime (single ended sensing mode) [7)]	N_{ERD0S} CC	-	-	750000	cycles	

表 3-64 Flash（续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Number of erase operations on DF1 over lifetime (complement sensing mode) [6]	N_{ERD1C} CC	-	-	2000000	cycles	
Number of erase operations on DF1 over lifetime (single ended sensing mode) [7]	N_{ERD1S} CC	-	-	500000	cycles	
Data Flash Endurance per EEPROMx sector (complement sensing mode) [8]	N_{E_EEP10C} CC	-	-	500000	cycles	Max. data retention time 10 years
DataFlash Endurance per EEPROMx sector (single ended sensing mode) [8]	N_{E_EEP10S} CC	-	-	125000	cycles	Retention time and Tj according below example temperature profile
		-	-	125000	cycles	max data retention time 20y, Tj=110°C
		-	-	125000	cycles	max data retention time 8.2y, Tj=125°C
Data Flash Endurance per HSMx sector (complement sensing mode) [8]	N_{E_HSMC} CC	-	-	250000	cycles	Max. data retention time 10 years
Data Flash Endurance per HSMx sector (single ended sensing mode) [8]	N_{E_HSMS} CC	-	-	125000	cycles	Retention time and Tj according below example temperature profile
		-	-	125000	cycles	max data retention time 20y, Tj=110°C
		-	-	125000	cycles	max data retention time 8.2y, Tj=125°C
Junction temperature limit for PFlash program/erase operations	$T_{JPFlash}$ SR	-	-	150	°C	
Data Flash Erase Time per Sector [1][3][5]	t_{ERD1} CC	-	-	0.5	s	Max. 1000 erase/program cycles
Data Flash Erase Time per Sector [1][3][5]	t_{ERDM} CC	-	-	1.5	s	Max allowed cycles, see NE_EEP10 and NE_HSM parameters
DataFlash Adder on Erase Time per 32kByte erase size when using complement sensing mode [1]	$t_{ER\_ADDC32C}$ CC	-	-	50	ms	Adder per 32 kByte on erase time; applicable only when using complement mode

表 3-64 Flash（续）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data Flash Erase Time per Multi-Sector Command 1)3)5)	t_{MERD1} CC	-	-	0.5	s	Max 1000 erase/program cycles; For consecutive logical sectors ≤ 256KBytes
Data Flash Erase Time per Multi-Sector Command 1)3)5)	t_{MERDM} CC	-	-	1.5	s	Max allowed cycles, see NE_EEP10x and NE_HSMx Parameters; For consecutive logical sectors ≤ 256 kByte
Program Flash Access Delay at reduced VDDP3 voltage supply during cranking	$t_{PF\_low\_VDDP3}$ CC	-	-	60	ns	see register DMU_HF_PWAIT.CFL ASH
Data Flash Erase Verify time per page (Complement Sensing) 2)	$t_{VER\_PAGE\_DC}$ CC	-	-	10	µs	Time per 8 Byte page for Verify Erased Page command
Data Flash Erase Verify time per page (Single Ended Sensing) 1)	$t_{VER\_PAGE\_DS}$ CC	-	-	10	µs	Time per 8 Byte page for Verify Erased Page command
Program Flash Erase Verify time per page 1)	$t_{VER\_PAGE\_P}$ CC	-	-	10	µs	Time per 32 Byte page for Verify Erased Page command
Data Flash Erase Verify time per sector (Complement Sensing) 1)	$t_{VER\_SEC\_DC}$ CC	-	-	200	µs	Time per 2 KB sector for Verify Erased Logical Sector Range command
Data Flash Erase Verify time per sector (Single Ended Sensing) 1)	$t_{VER\_SEC\_DS}$ CC	-	-	360	µs	Time per 4 KB sector for Verify Erased Logical Sector Range command
Program Flash Erase Verify time per sector 1)	$t_{VER\_SEC\_P}$ CC	-	-	360	µs	Time per 16KB sector for Verify Erased Logical Sector Range command
Data Flash Erase Verify time per wordline (Complement Sensing) 1)	$t_{VER\_WL\_DC}$ CC	-	-	30	µs	
Data Flash Erase Verify time per wordline (Single Ended Sensing) 1)	$t_{VER\_WL\_DS}$ CC	-	-	50	µs	
Program Flash Erase Verify time per wordline 1)	$t_{VER\_WL\_P}$ CC	-	-	30	µs	

1) 仅对f_{FSI} = 100MHz 有效。

2) 时间不依赖于编程模式（5V 或 3.3V）

3) 在超出规格的条件下（例如,由于过度循环)或激活WL定向缺陷，擦除过程的持续时间可能会增加高达50%。

4) 使用 512 kByte / 256 kByte 擦除指令 (PFlash / DFlash)。

5) 如果 DataFlash 在互补感应模式下运行，则擦除时间将增加 erase_size / 32kByte x tER_ADDC32C

6) 允许将可寻址存储器划分为 8 个逻辑扇区；仍必须进行循环以考虑擦除干扰限制N_{DFD}。

7) 允许将可寻址存储器划分为 6 个逻辑扇区；仍必须进行循环以考虑擦除干扰限制N_{DFD}。

8) 仅在使用强大的 EEPROM 仿真算法时有效。欲了解更多详细信息，请参阅用户手册。

3.29 质量声明

表 3-65 质量参数

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Moisture Sensitivity Level	MSL CC	-	-	3		Conforming to Jedec J-STD--020C for 240C
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM} SR	-	-	500	V	for all other balls/pins; conforming to JESD22-C101-C
		-	-	750	V	for corner balls/pins; conforming to JESD22-C101-C
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	-	-	2000	V	Conforming to JESD22-A114-B
ESD susceptibility of the LVDS pins according to Human Body Model (HBM)	V_{HBM1} SR	-	-	2000	V	
Operation Lifetime	t_{OP} CC	-	-	24500	hour	see below temperature profile as an example

温度曲线示例

以下温度曲线就是一个例子。为了满足质量和可靠性目标，特定应用的温度曲线需要经过英飞凌科技公司的验证。

表 3-66 温度曲线示例

T_J=	Duration [h]	Comment
≤ 170°C	≤ 30	
≤ 160°C	≤ 120	
≤ 150°C	≤ 220	
≤ 140°C	≤ 350	
≤ 130°C	≤ 780	
≤ 120°C	≤ 1600	
≤ 110°C	≤ 3000	
≤ 100°C	≤ 7000	
≤ 90°C	≤ 8000	
≤ 80°C	≤ 2400	
≤ 70°C	≤ 1000	
	≤ 24500	total time

表 3-67 非活动寿命温度曲线示例

T_J=	Duration [h]	Comment
≤ 55°C	≤ 150700	

3.30 封装外形

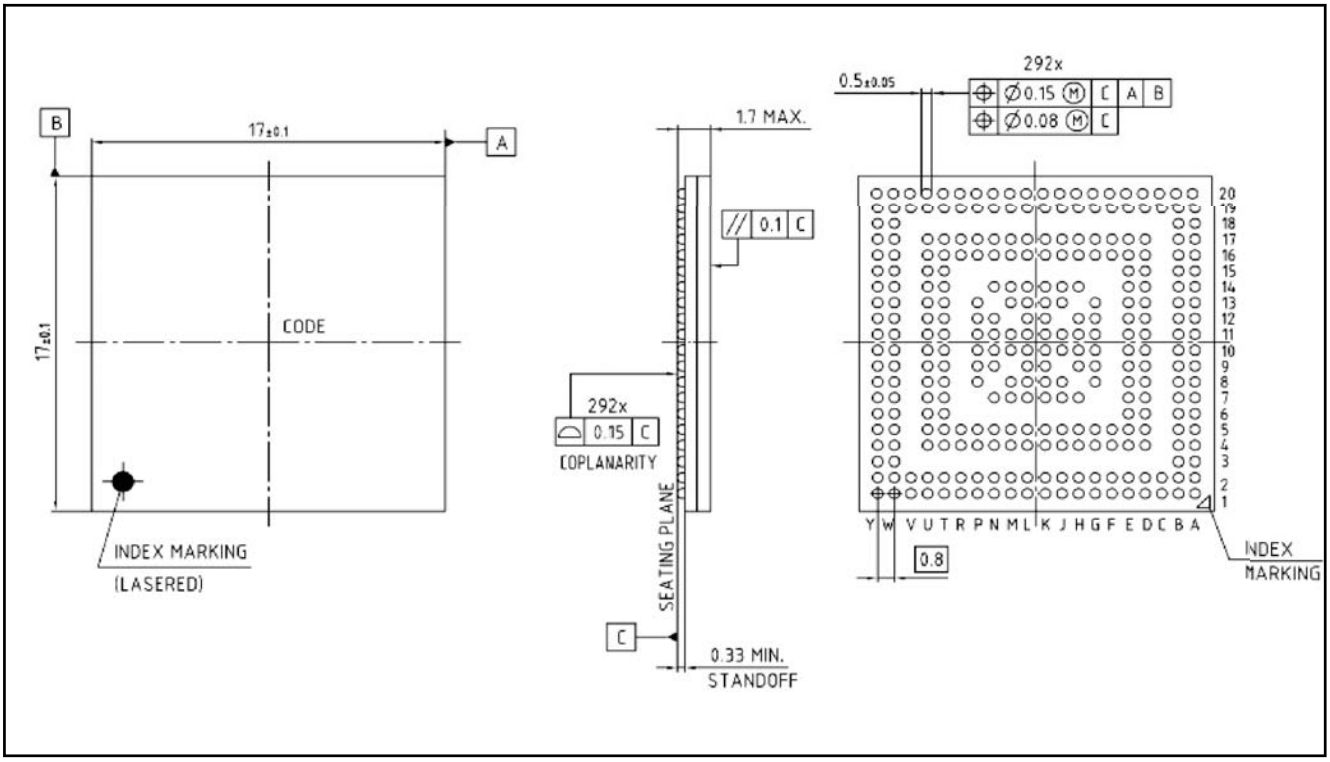


图 3-25 LFBGA-292 封装外形

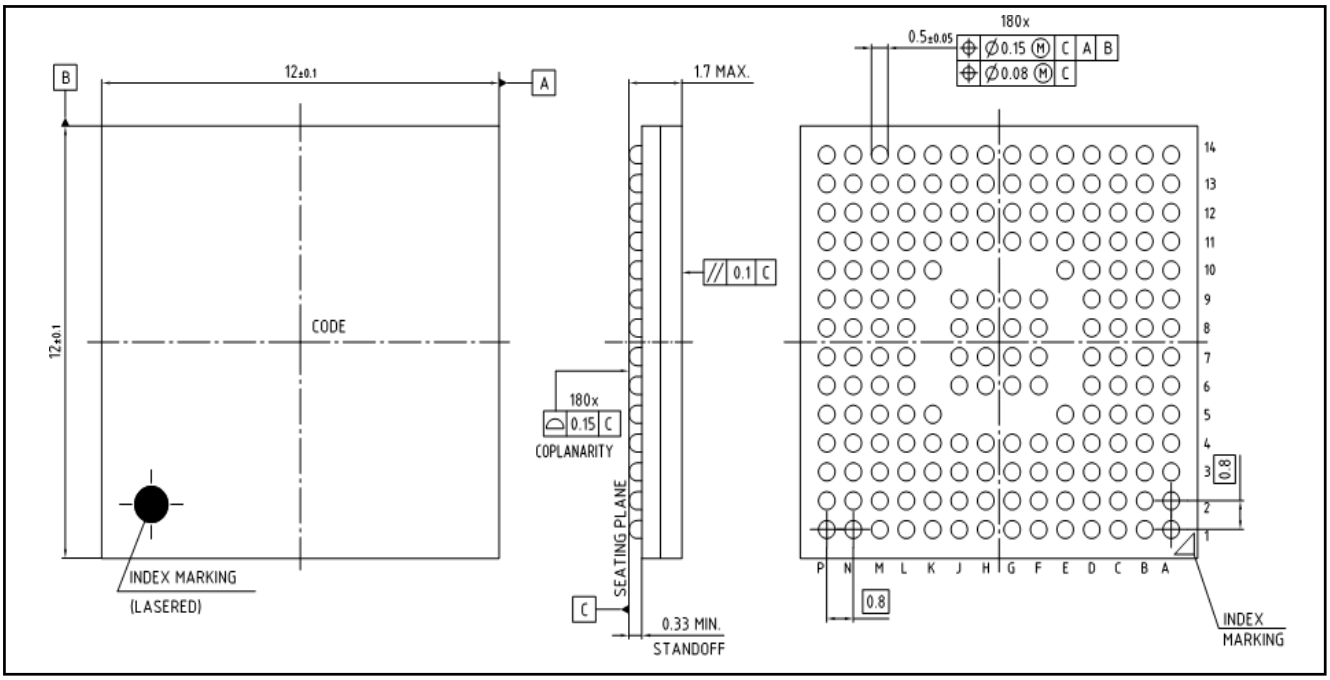


图 3-25 LFBGA-180 封装外形

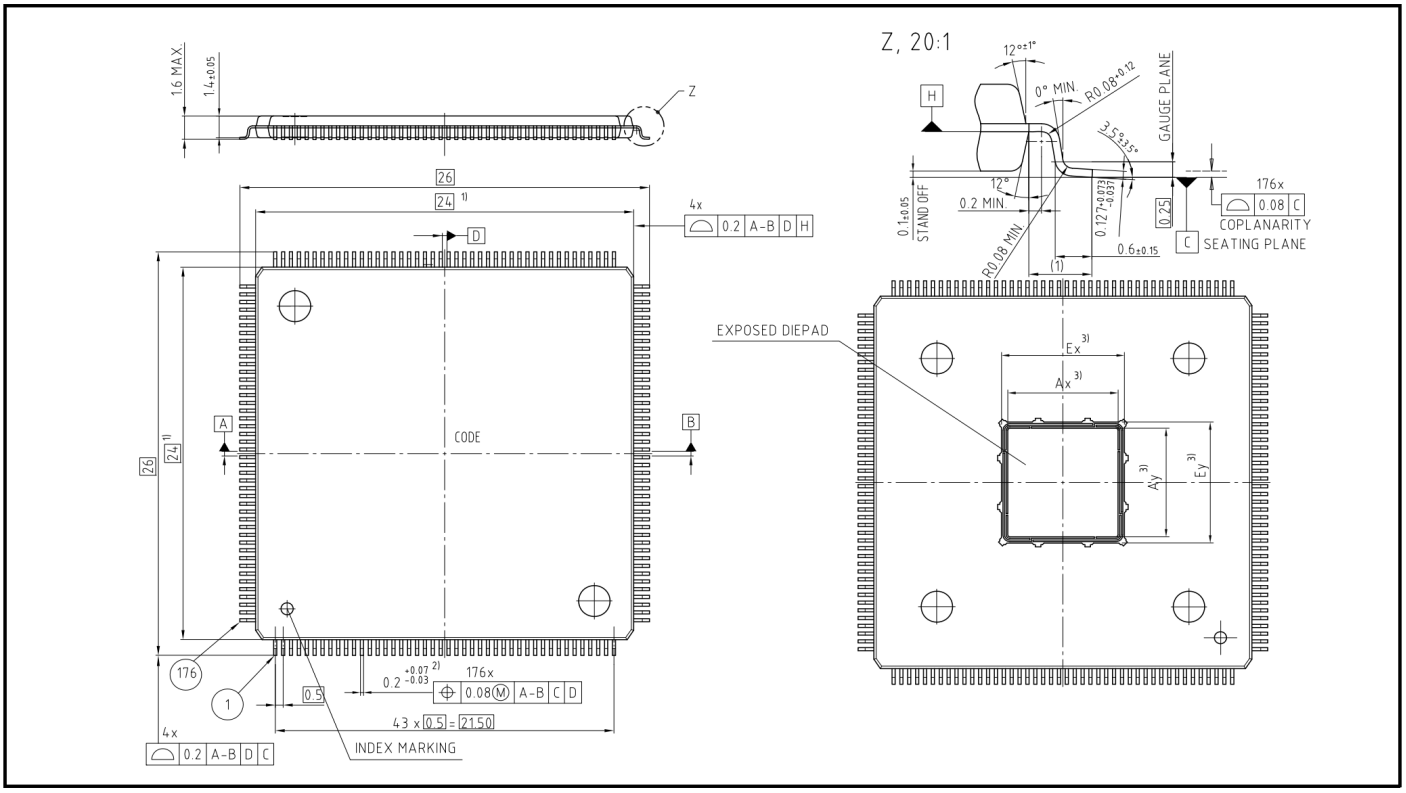


图 3-26 LQFP-176 封装外形

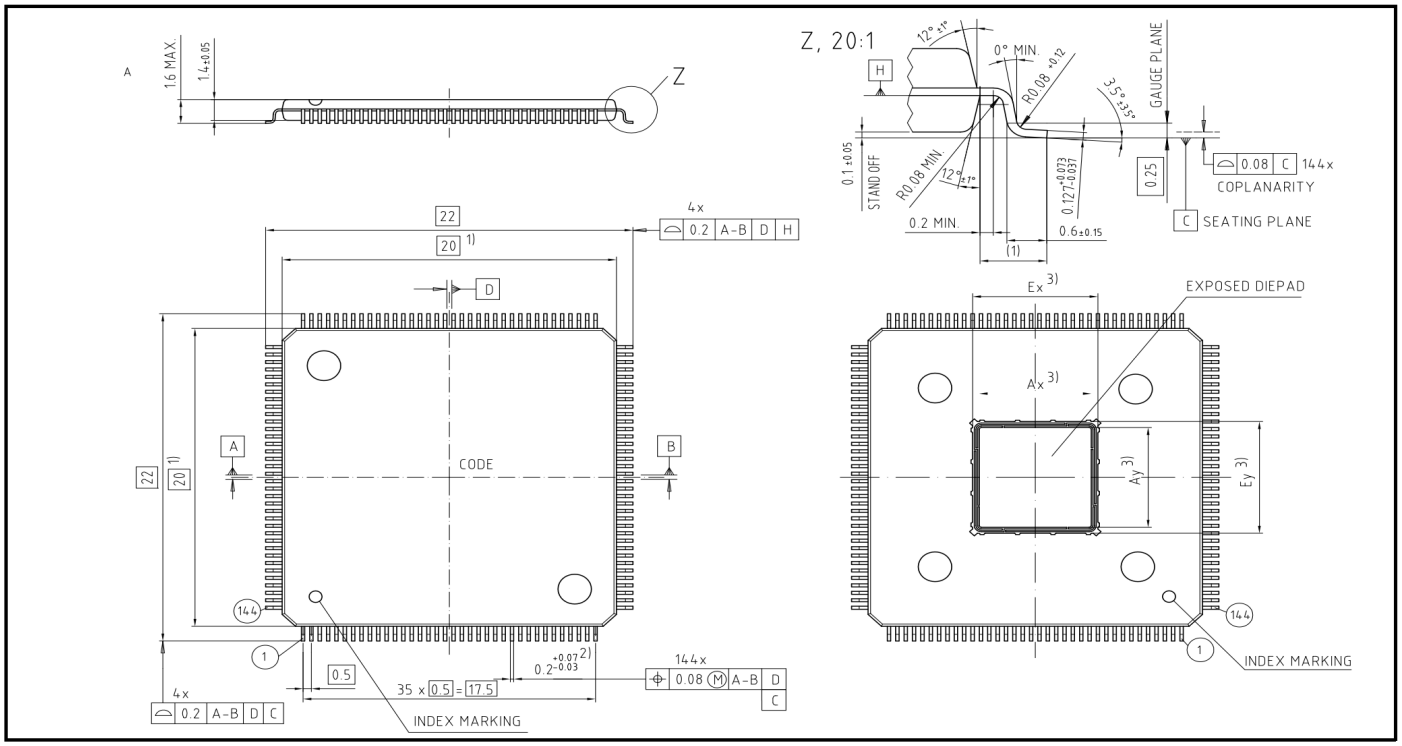


图 3-27 LQFP-144 封装外形

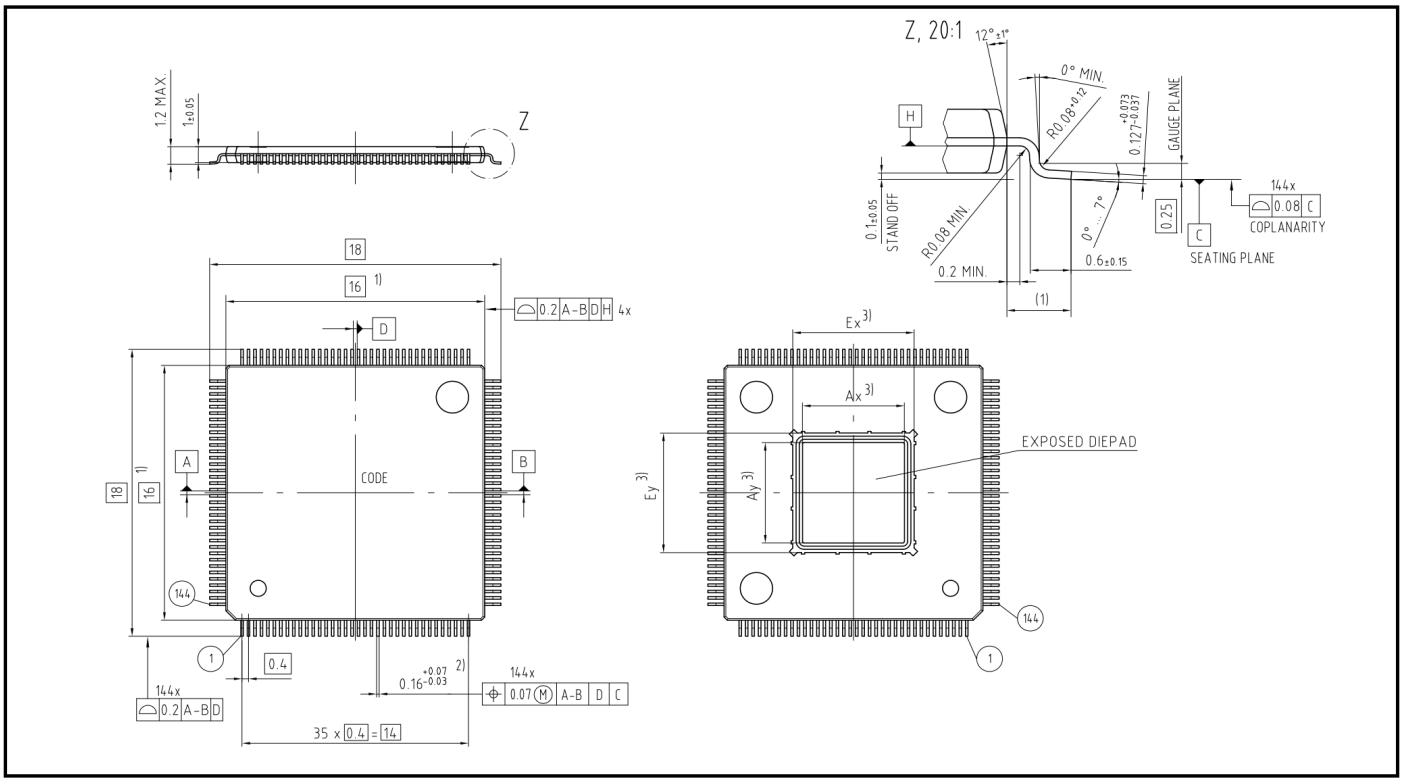


图 3-28 TQFP-144 封装外形

表 3-68 LQFP-144 和 LQFP-176 裸露焊盘尺寸

LQFP-144 (0.5 mm) and LQFP-176 (0.5 mm)	Ex; nominal EPad size	7.5 mm ± 50 µm
	Ey; nominal EPad size	7.5 mm ± 50 µm
	Ax; solderable EPad size	6.7 mm ± 50 µm
	Ay; solderable EPad size	6.7 mm ± 50 µm

表 3-69 TQFP-144 裸露焊盘尺寸

TQFP-144 (0.4 mm)	Ex; nominal EPad size	8.7 mm ± 50 µm
	Ey; nominal EPad size	8.7 mm ± 50 µm
	Ax; solderable EPad size	7.9 mm ± 50 µm
	Ay; solderable EPad size	7.9 mm ± 50 µm

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3.30.1 封装参数

表 3-70 封装参数

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance (junction to ambient) [1]	RTH_JACC	-	-	22	K/W	LFBGA-180
		-	-	23	K/W	LFBGA-292
		-	-	18	K/W	QFP-144
		-	-	17	K/W	QFP-176
Thermal resistance (junction to case bottom) [1]	RTH_JCBCC	-	-	4.5	K/W	LFBGA-180
		-	-	4.5	K/W	LFBGA-292
		-	-	2	K/W	QFP-144
		-	-	2	K/W	QFP-176
Thermal resistance (junction to case top) [1]	RTH_JCTCC	-	-	6	K/W	LFBGA-180
		-	-	5	K/W	LFBGA-292
		-	-	10	K/W	QFP-144
		-	-	10	K/W	QFP-176

1) 外壳与环境之间的顶部和底部热阻（RTH_CTA，RTH_CBA）将与上面给出的结与外壳之间的热阻（RTH_JCT，RTH_JCB）相结合，以计算结与环境之间的总热阻（RTH_JA）。外壳和环境之间的热阻（RTH_CTA、RTH_CBA）取决于外部系统（PCB、外壳）的特性，由用户负责。

结温可使用以下公式计算：TJ = TA + RTH_JA * PD，其中 RTH_JA 是结点与环境之间的总热阻。

采用“冷板法”（MIL SPEC-883 方法 1012.1）测量的热阻。

4 修订记录

0.4 版是本文档的第一个版本。

4.1 从 0.4 版本到 0.6 版本的变更

- Changes in chapter Summary of Features, table Platform Feature Overview
  - Corrected spelling “HSPDM”
  - Changed spelling for packages
  - Added packages

- Changes in chapter “Pin Definition and Function”
  - Changed package wording from BGA292 to LFBGA-292
  - Changed package wording from BGA180 to LFBGA-180
  - Changed package wording from QFP176 to LQFP-176
  - Changed package wording from QFP144 to LQFP-144
  - Added pinning for package LFBGA-180
  - Separated pinnings for package LQFP-144 and TQFP-144

- Changes in chapter 'LFBGA-292 Package Variant Pin Configuration of TC36x'
  - Changes in 'Port 00 Functions' table; P00.0, P00.1, P00.2, P00.3, P00.4, P00.5, P00.6, P00.9, P00.10, P00.11, P00.12
  - Changes in Port 02 Functions' table; P02.0, P02.1, P02.2, P02.3, P02.4, P02.5, P02.7, P02.8
  - Changes in 'Port 10 Functions' table; P10.2, P10.3, P10.7, P10.8
  - Changes in 'Port 11 Functions' table; P11.0, P11.1, P11.4, P11.5, P11.7, P11.8, P11.10, P11.12, P11.13
  - Changes in 'Port 12 Functions' table; P12.0, P12.1
  - Changes in 'Port 13 Functions' table; P13.0, P13.1, P13.2
  - Changes in 'Port 14 Functions' table; P14.0, P14.1, P14.6, P14.7, P14.8, P14.9, P14.10
  - Changes in 'Port 15 Functions' table; P15.0, P15.1, P15.2, P15.3, P15.4, P15.5
  - Changes in 'Port 20 Functions' table; P20.0, P20.3, P20.6, P20.7, P20.8, P20.9, P20.10, P20.14
  - Changes in 'Port 21 Functions' table; P21.0, P21.1, P21.2, P21.3, P21.4, P21.5, P21.6, P21.7
  - Changes in 'Port 23 Functions' table; P23.0, P23.1, P23.2, P23.3
  - Changes in 'Port 32 Functions' table; P32.2, P32.3, P32.4
  - Changes in 'Port 33 Functions' table; P33.0, P33.1, P33.2, P33.3, P33.4, P33.5, P33.6, P33.7, P33.8, P33.9, P33.10, P33.12, P33.13
  - Changes in table “Analog Inputs” - Changed function for ball W5; Changed function for ball U5
  - Changes in table “System I/O” - Removed symbol and function for ball L19; Changed I/O for symbol ESR1, ball G16; Changed I/O for symbol ESR0, ball F16

- Added chapter 'LFBGA-180 Package Variant Pin Configuration of TC36x'

- Changes in chapter 'LQFP-176 Package Variant Pin Configuration of TC36x'

  - Changes in 'Port 00 Functions' table; P00.0, P00.1, P00.2, P00.3, P00.4, P00.5, P00.6, P00.9, P00.10, P00.11, P00.12
  - Changes in 'Port 02 Functions' table; P02.0, P02.1, P02.2, P02.3, P02.4, P02.5, P02.7, P02.8
  - Changes in 'Port 10 Functions' table; P10.2, P10.3, P10.7, P10.8
  - Changes in 'Port 11 Functions' table; P11.10, P11.12
  - Changes in 'Port 13 Functions' table; P13.0, P13.1, P13.2
  - Changes in 'Port 14 Functions' table; P14.0, P14.1, P14.6, P14.7, P14.8, P14.9, P14.10
  - Changes in 'Port 15 Functions' table; P15.0, P15.1, P15.2, P15.3, P15.4, P15.5
  - Changes in 'Port 20 Functions' table; P20.0, P20.3, P20.6, P20.7, P20.8, P20.9, P20.10, P20.14
  - Changes in 'Port 21 Functions' table; P21.0, P21.1, P21.2, P21.3, P21.4, P21.5, P21.6, P21.7
  - Changes in 'Port 23 Functions' table; P23.0, P23.1, P23.2, P23.3
  - Changes in 'Port 32 Functions' table; P32.2, P32.3, P32.4
  - Changes in 'Port 33 Functions' table; P33.0, P33.1, P33.2, P33.3, P33.4, P33.5, P33.6, P33.7, P33.8, P33.9, P33.10, P33.12, P33.13
  - Changes in table “Analog Inputs” - Changed function for pin 50; Changed function for pin 49
  - Changes in table “System I/O” - Removed symbol and function for pin 114; Changed I/O for symbol ESR1, pin 120; Changed I/O for symbol ESR0, pin 122
  - Changes in table “Supply” - Changed symbol and function for pin 164; Changed symbol and function for pin 54; Changed pin 177 to E-PAD

- Changes in chapter 'LQFP-144 Package Variant Pin Configuration of TC36x'
  - Changes in 'Port 00 Functions' table; P00.0, P00.1, P00.2, P00.3, P00.4, P00.5, P00.6, P00.9, P00.12
  - Changes in 'Port 02 Functions' table; P02.0, P02.1, P02.2, P02.3, P02.4, P02.5, P02.7, P02.8
  - Changes in 'Port 10 Functions' table; P10.2, P10.3
  - Changes in 'Port 11 Functions' table; P11.10, P11.12
  - Changes in 'Port 13 Functions' table; P13.0, P13.1, P13.2
  - Changes in 'Port 14 Functions' table; P14.0, P14.1, P14.6
  - Changes in 'Port 15 Functions' table; P15.0, P15.1, P15.2, P15.3, P15.4, P15.5
  - Changes in 'Port 20 Functions' table; P20.0, P20.3, P20.6, P20.7, P20.8, P20.9, P20.10, P20.14
  - Changes in 'Port 21 Functions' table; P21.2, P21.3, P21.4, P21.5, P21.6, P21.7
  - Changes in 'Port 23 Functions' table; P23.1
  - Changes in 'Port 32 Functions' table; P32.4
  - Changes in 'Port 33 Functions' table; P33.4, P33.5, P33.6, P33.7, P33.8, P33.9, P33.10, P33.12, P33.13
  - Changes in table “Analog Inputs” - Changed function for pin 40, symbol EVADC_FC0CH0; Changed function for pin 39, symbol EVADC_FC1CH0
  - Changes in table “System I/O” - Removed symbol and function for pin 91; Changed I/O for symbol ESR1, ball 96; Changed I/O for symbol ESR0, ball 98
  - Changes in table “Supply” - Changed symbol and function for pin 136; Changed symbol and function for pin 44; Changed pin 145 to E-PAD

- Added chapter 'TQFP-144 Package Variant Pin Configuration of TC36x'

- Changes in chapter “Bare Die Variant Pin Configuration of TC36x”

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修订记录 从0.4版本到0.6版本的变更

  - Changes in table “Pad List” for different positions (Pad Names, Pad Types, X and Y values, and comments)

- Changes in chapter “Legend”

- Changes in chapter “Electrical Specification”

- Changes in table “Absolute Maximum Ratings”
  - Added footnote of parameter V_{DDM}
  - Changed footnote number of parameter V_{IN}
  - Changed footnote number of parameter I_{IN}
  - Changed footnote number of parameter $\sum I_{IN}$
  - Added footnote 2)
  - Changed order of footnotes

- Changes in table “Overload Parameters”
  - Changed note for parameter K_{OVAN}
  - Changed footnote number of parameter K_{OVAN}
  - Changed note for parameter K_{OVAP}
  - Changed footnote number of parameter K_{OVAP}
  - Added footnote 2)

- Changes in table “Operating Conditions”
  - Deleted parameter f_{EBU}
  - Added footnote number of parameter V_{DD}
  - Changed footnote number of parameter V_{DDM}
  - Changed footnote number of parameter V_{EXT}
  - Changed footnote number of parameter V_{FLEX}
  - Changed footnote number of parameter V_{DDP3}
  - Changed footnote number of parameter V_{EVRSB}
  - Changed footnote number of parameter V_{DDPPA}
  - Added footnote 1)
  - Changed order of footnotes

- Changes in table “PORST Pad”
  - Added footnote number of parameter I_{PDL}
  - Added values and notes for parameter V_{IH}
  - Added values and notes for parameter V_{IL}
  - Added footnote 2)

- Changes in table “Fast 5V GPIO”
  - Added footnote number of parameter I_{PUH}
  - Added footnote number of parameter I_{PDL}

  - Changed and deleted values of parameter I_{OZ}
  - Added footnotes 4) and 5)

- Changes in table “Fast 3.3V GPIO”
  - Added footnote number of parameter I_{PUH}
  - Added footnote number of parameter I_{PDL}
  - Changed and deleted values of parameter I_{OZ}
  - Added footnotes 4) and 5)

- Changes in table “Slow 5V GPIO”
  - Added footnote number of parameter I_{PUH}
  - Added footnote number of parameter I_{PDL}
  - Changed and deleted values of parameter I_{OZ}
  - Deleted footnote 4)
  - Added footnotes 4) and 5)

- Changes in table “Slow 3.3V GPIO”
  - Added footnote number of parameter I_{PUH}
  - Added footnote number of parameter I_{PDL}
  - Changed and deleted values of parameter I_{OZ}
  - Deleted footnote 4)
  - Added footnotes 4) and 5)

- Changes in table “RFast 5V GPIO”
  - Added footnote number of parameter I_{PUH}
  - Added footnote number of parameter I_{PDL}
  - Added footnotes 4) and 5)

- Changes in table “RFast 3.3V GPIO pad”
  - Added footnote number of parameter I_{PUH}
  - Added footnote number of parameter I_{PDL}
  - Added footnotes 4) and 5)

- Changes in table “Class S 5V”
  - Added footnote number of parameter I_{PUH}
  - Added footnote number of parameter I_{PDL}
  - Added footnotes 2) and 3)

- Changes in table “LVDS - IEEE standard LVDS general purpose link (GPL)”
  - Added footnote for parameter t_{rise20}
  - Added footnote for parameter t_{fall20}
  - Changed footnote number of parameter V_{OD}

  - Changed value for parameter V_I
  - Changed test conditions for parameter V_{idth}
  - Added values and test conditions for parameter V_{idth}
  - Changed test conditions for parameter R_{in}
  - Changed footnote number of parameter V_{ODSM}
  - Added footnotes 1) and 2)
  - Changed order of footnotes

- Changes in table “VADC 5V”
  - Added and changed values of parameter V_{AREF}
  - Added footnote number of parameter V_{AREF}
  - Added note for parameter V_{AIN}
  - Changed footnote numbers of parameter *TUE*
  - Changed footnote number of parameter EA_{INL}
  - Changed footnote numbers of parameter EA_{DNL}
  - Changed footnote number of parameter EA_{GAIN}
  - Added footnote number of parameter EA_{OFF}
  - Added and changed footnote numbers of parameter EN_{RMS}
  - Added footnote number of parameter Q_{CONV}
  - Changed footnote number of parameter Q_{AINS}
  - Changed footnote number of parameter R_{CSD}
  - Added footnote 1)
  - Changed order of footnotes

- Changes in table “DSADC 5V”
  - Changed value of parameter V_{AREF}
  - Added value of parameter I_{REF}
  - Added value of parameter I_{RMS}
  - Added and changed footnote numbers of parameter ED_{GAIN}
  - Changed footnote number of parameter ED_{OFF}
  - Changed footnote number of parameter *SNR*
  - Added footnote 4)
  - Changed order of footnotes

- Changes in table “OSC_XTAL”
  - Added values for parameter DC_{X1}
  - Added values for parameter J_{ABSX1}
  - Added values for parameter SR_{XTAL1}
  - Added footnote 3)

- Changes in table “Back-up Clock”
  - Changes in footnote 1)

修订记录 从0.4版本到0.6版本的变更

- Changes in table “DTS PMS”
  - Added note for parameter T_{NL}
- Changes in table “DTS Core”
  - Added note for parameter T_{NL}
- Changes in chapter “Power Supply Current”
  - Changed chapter description
- Changes in table “Current Consumption”
  - Changed values of parameter $I_{DDPORST}$
  - Changed value for parameter $I_{EXTRAIL}$
  - Changed value for parameter $I_{EXTFLEX}$
  - Changed value for parameter I_{DDTOT}
  - Added value for parameter $I_{DDTOTDC3}$
  - Changed test condition for parameter $I_{DDTOTDC3}$
  - Added value for parameter $I_{DDTOTDC5}$
  - Changed test condition for parameter $I_{DDTOTDC5}$
  - Changed values for parameter *PD*
  - Deleted footnote number of parameter $I_{EXTFLEX}$
  - Deleted footnote number of parameter $I_{DDP3RAIL}$
  - Changed footnotes 1) and 3)
- Changes in table “Module Current Consumption”
  - Changed value of parameter of $I_{EXTLVDS}$
  - Changed value of parameter of I_{SCRSB}
  - Changed footnote 5)
- Changes in table “Module Core Current Consumption”
  - Added values of parameter of I_{DDGTM}
  - Changed footnote 1)
- Changes in chapter “Power Supply Infrastructure and Supply Start-up”
  - Changed wording in descriptions for sub chapter “Supply Ramp-up and Ramp-down Behavior”
  - Changed numbers for HWCFG pins
  - Changed figure for 'Single Supply Mode (a)'
  - Changed figure for 'Single Supply Mode (e)'
  - Changed figure for 'External Supply Mode (d)'
  - Changed figure for 'External Supply Mode (h)'
- Changes in table “Reset”

  - Added values for parameter $t_{WARMRSTSEQ}$
  - Changed value for parameter t_{BWP}
  - Changed/ added values for parameter t_{SCR}

- Changes in table “EVR33 LDO”
  - Added footnote number of parameter dV_{OUT} / dI_{OUT}
  - Added footnote 7)

- Changes in table “Supply Monitors”
  - Changed note for parameter V_{RST33}
  - Added value for parameter V_{RSTC}
  - Changed note for parameter V_{RSTC}
  - Changed values of parameter V_{EXTMON}
  - Added footnote number of parameter V_{EXTMON}
  - Added footnote number of parameter $V_{DDP3MON}$
  - Added footnote number of parameter V_{DDMON}
  - Changed footnote 2)
  - Changed footnote 3)
  - Added footnote 5)

- Changes in table “EVRC SMPS”
  - Changed values of parameter V_{DDDC}
  - Changed values of parameter V_{DDDCT}
  - Added/ changed values of parameter f_{DCDC}
  - Changed value of parameter t_{STRDC}
  - Changed value of parameter ΔV_{DDDC}
  - Deleted/ changed values of parameter dV_{DDDCT} / dI_{OUT}
  - Changed value for parameter I_{MAX}
  - Deleted/ changed values of parameter dV_{DDDCT} / dV_{IN}
  - Changed values of parameter n_{DC}

- Changes in table “EVRC SMPS External components”
  - Deleted values of parameter C_{OUT}
  - Deleted values of parameter C_{IN}
  - Added values of parameter L_{DC}
  - Deleted values of parameter R_{ON}
  - Deleted values of parameter Q_G

- Changes in table “PLL System”
  - Deleted values of parameter f_{MV}

- Changes in table “Master Mode Timing, LVDS output pads for data and clock”

  - Added footnote numbers for all parameter values
  - Added footnote 1)

- Changes in table “LVDS clock/data (LVDS pads in LVDS mode) valid for 5V”
  - Added footnote numbers for all parameter values
  - Added footnote 3)

- Changes in subchapter “ETH RGMII Parameters”
  - Added figure for “ETH RGMII TX Signal Timing (Delay on Destination (DoD))”
  - Added figure for “ETH RGMII RX Signal Timing (Delay on Source (DoS))”

- Changes in table “Flash”
  - Changed value for parameter t_{RTU}
  - Changed description and note for parameter $t_{VER\text{-}PAGE\_DC}$
  - Changed description for parameter $t_{VER\text{-}PAGE\_DS}$

- Changes in table “Package Parameters”
  - Added values for all parameters

4.2 从 0.6 版本到 0.7 版本的变更

- Changes in chapter “Bare Die Variant Pin Configuration of TC36x”
  - Added comment to “Pad List” concerning “neighbor pads”

- Changes in chapter “Legend”
  - Added refering IO_Spirit_file version

Changes in chapter “Electrical Specification”
- Changes in table “Absolute Maximum Ratings”
  - Changed description of parameter V_{IN}
  - Changed description of parameter $\sum I_{IN}$
  - Added footnote number to parameter I_{IN}
  - Added footnote 5)
- Changes in table “Slow 3.3V GPIO”
  - Added value and note for parameter R_{DSON}
  - Changed notes of parameter I_{OZ}
- Changes in table “LVDS - IEEE standard LVDS general purpose link (GPL)”
  - Added notes to table “LVDS - IEEE standard LVDS general purpose link (GPL)”
- Changes in table “OSC_XTAL”
  - Changed spelling in footnote 2)
- Changes in table “Current Consumption”
  - Changed wording in footnote 6)

- Changes in table “Module Current Consumption”
  - Changed value and note of parameter $T_{EXTLVDS}$
  - Added value and note of parameter $T_{EXTLVDS}$
- Changes in table “Reset”
  - Changed value for parameter t_{PIP}
- Changes in table “EVR33 LDO”
  - Added parameter dV_{OUTTC}
- Changes in table “Supply Monitors”
  - Changed notes for all values of parameter V_{EXTMON}
  - Added values to parameter V_{EXTMON}
- Changes in table “EVRC SMPS”
  - Changed Controller Characteristics (CC) to System Requirements (SR) for parameter Δf_{DCSPR}
  - Changed Controller Characteristics (CC) to System Requirements (SR) for parameter n_{DC}
  - Added values to parameter $f_{DCDCSYNC}$
- Changes in table “PLL System”
  - Changed value of parameter f_{REF}
- Changes in table “Flash”
  - Changed value of parameter t_{PRPB5_PF}
  - Changed value of parameter $t_{ER\text{-}DEV}$
- Changes in table “Package Parameters”
  - Changed value of parameter V_{HBM1}

4.3 从 0.7 版本到 1.0 版本的变更

Changes in chapter “Summary of Features”

- Changed spelling in table "Platform Feature Overview"
  - Removed “ASIL” value from table “Platform Feature Overview”

Changes in chapter “TC36x Pin Definition and Functions”

- Changes in sub-chapter "Bare Die Variant Pin Configuration of TC36x"
  - Deleted redundant sentence in explanation following table “Pad List” regarding neighbor pads

Changes in chapter “Electrical Specification”

- Changes in sub-chapter “Absolute Maximum Ratings”
  - Changed wording for parameter V_{IN}
  - Changed spelling in footnote 3)
- Changes in sub-chapter “Pin Reliability in Overload”
  - Changed spelling for parameter I_{INSA} in table “Overload Parameters”
- Changes in sub-chapter “Operating Conditions”
  - Deleted parameter f_{ADAS} in table "Operating Conditions"
  - Changed values for parameter f_{GETH} in table "Operating Conditions"
- Changes in sub-chapter “5V / 3.3V switchable Pads”
  - Deleted value for parameter R_{DSON} in table "Slow 5V GPIO"
  - Deleted value for parameter R_{DSON} in table "Slow 3.3V GPIO"

- Changes in sub-chapter “High performance LVDS Pads”
  - Deleted value for parameter t_{fall20} in table "LVDS - IEEE standard LVDS general purpose link (GPL)"
  - Deleted footnote 2) for table "LVDS - IEEE standard LVDS general purpose link (GPL)"
  - Changed order of footnotes for table "LVDS - IEEE standard LVDS general purpose link (GPL)"
- Changes in sub-chapter “VADC Parameters”
  - Deleted footnote 9) for parameter Q_{CONV} in table "VADC 5V"
  - Changed spelling for parameter dV_{CSD} in table "VADC 5V"
  - Changed wording for footnote 7) for table "VADC 5V"
  - Changed footnote numbering for table "VADC 5V"
  - Changed figure "Equivalent Circuitry for Analog Inputs" for table "VADC 5V"
- Changes in sub-chapter “MHz Oscillator”
  - Changed wording of footnote 1) for table "OSC_XTAL"
- Changes in sub-chapter “Power Supply Current”
  - Changed value for parameter $T_{EXTRAIL}$ in table "Current Consumption"
  - Changed value for parameter T_{EVRSB} in table "Current Consumption"
  - Changed value for parameter I_{SRCSB} in table "Module Current Consumption"
- Changes in sub-chapter “Reset Timing”
  - Changed spelling for parameter t_{EVRPOR} in table "Reset"
  - Changed values for parameter t_{PI} in table "Reset"
- Changes in sub-chapter “EVR”
  - Changed Test Conditions for parameter $V_{DDP3MON}$ in table "Supply Monitors"
  - Changed Test Conditions for parameter V_{DDMON} in table "Supply Monitors"
  - Changed Test Conditions for parameter t_{MON} in table "Supply Monitors"
  - Changed spelling of footnote 2) for table "Supply Ramp"
  - Added description at table "Supply Ramp" regarding power cycles
  - Added values for parameter C_{OUT} in table "EVRC SMPS External components"
- Changes in sub-chapter “ETH RGMII Parameters”
  - Deleted note for parameter t_{21} in table "ETH RGMII Signal Timing Parameters valid for 3.3V"
- Changes in sub-chapter “Package Parameters”
  - Changed notes spelling in table "Package Parameters"

4.4 从 1.0 版本到 1.1 版本的变更

- Changes in chapter “Summary of Features”
  - Changed wording for “DFLASH”
  - Added description for “AEC-Q100”
  - Added description for “ISO 26262 Safety Element”
  - Added description for Data Flash in table “Platform Feature Overview”
  - Changed wording for Low Power Features in table “Platform Feature Overview” –
- Changes in chapter “TC36x Pin Definition and Functions”
  - Added notes to table “System I/O” for “LFBGA-292 Package Variant”

  - Added notes to table “System I/O” for “LFBGA-180 Package Variant”
  - Added note to sub-chapter “LQFP-176 Package Variant”
  - Added notes to table “System I/O” for “LQFP-176 Package Variant”
  - Added note to sub-chapter “LQFP-144 Package Variant”
  - Added notes to table “System I/O” for “LQFP-144 Package Variant”
  - Added note to sub-chapter “TQFP-144 Package Variant”
  - Added notes to table “System I/O” for “TQFP-144 Package Variant”
  - Changed sub-chapter title from “Bare Die Variant Pin Configuration of TC36x” to “Sequence of Pads in Pad Frame”
  –
- Changes in chapter “Legend”
  - Changed version number of “TC36xpd_IO_Spirit” file–
- Changes in chapter “Electrical Specification”
  - Typos corrected in footnotes for sub-chapter “Absolute Maximum Ratings”
  - Changed note for parameter t_{TX_ASYM} in table “Fast 5V GPIO” of sub-chapter “5V/3.3V switchable Pads”
  - Changed note for parameter t_{TX_ASYM} in table “Fast 3.3V GPIO” of sub-chapter “5V/3.3V switchable Pads”
  - Changed note for parameter t_{TX_ASYM} in table “Slow 5V GPIO” of sub-chapter “5V/3.3V switchable Pads”
  - Changed note for parameter t_{TX_ASYM} in table “Slow 3.3V GPIO” of sub-chapter “5V/3.3V switchable Pads”
  - Changed note for parameter t_{TX_ASYM} in table “RFast 5V GPIO” of sub-chapter “5V/3.3V switchable Pads”
  - Changed note for parameter t_{TX_ASYM} in table “RFast 3.3V pad” of sub-chapter “5V/3.3V switchable Pads”
  - Typos corrected in footnote 2) for table “LVDS – IEEE standard LVDS general purpose link (GPL)” in sub-chapter “High performance LVDS Pads”
  - Added footnote content for table “LVDS – IEEE standard LVDS general purpose link (GPL)” in sub-chapter “High performance LVDS Pads”
  - Changed footnotes 3) and 6) for table “VADC 5V” in sub-chapter “VADC Parameters”
  - Changed value of parameter I_{RMS} in table “DSADC 5V” in sub-chapter “DSADC Parameters”
  - Changed footnote 4) in sub-chapter “DSADC Parameters”
  - Added footnote 7) for parameter *PD* in table “Current Consumption” in sub-chapter “Power Supply Current”
  - Changed footnote 2) for table “Current Consumption” in sub-chapter “Power Supply Current”
  - Added footnote 7) for table “Current Consumption” in sub-chapter “Power Supply Current”
  - Added sentence to sub-chapter “Supply Ramp-up and Ramp-down Behavior”
  - Deleted value for parameter t_{52} in table “Master Mode Timing, LVDS output pads for data and clock” in sub-chapter “QSPI Timings, Master and Slave Mode”
  - Changed values (from Min. to Typ.) for parameter t_7 in table “ETH MII Signal Timing Parameters” for sub-chapter “ETH MII Parameters”
  - Changed symbols for parameters t_{13}, t_{14}, t_{15} in table “ETH RMII Signal Timing Parameters valid for 3.3V” in sub-chapter “ETH RMII Parameters”
  - Changed value (from Min. to Typ.) for parameter t_{13} in table “ETH RMII Signal Timing Parameters valid for 3.3V” in sub-chapter “ETH RMII Parameters”
  - Added footnote 3) for parameters t_{16}, t_{17} in table “ETH RMII Signal Timing Parameters valid for 3.3V” in sub-chapter “ETH RMII Parameters”

- Added footnote 3) for table “ETH RMII Signal Timing Parameters valid for 3.3V” in sub-chapter “ETH RMII Parameters”
- Added tables for “Exposed Pad Dimensions” to sub-chapter “Package Outlines”

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