# 英飞凌 512Mb/1Gb SEMPER™ 闪存存储器

## 八线接口，1.8V/3.0V

## 特性

- 英飞凌45纳米MIRRORBIT™ 技术，在每个存储单元中存储两个数据位
- 扇区布局选项
  - 全局统一：地址空间由所有 256 KB 扇区组成
  - 混合扇区：
    - 混合配置 1：地址空间由32个 4 KB 扇区组成，这些扇区组分别在顶部或底部，其余扇区均为 256 KB
    - 混合配置 2：地址空间由32个 4 KB 扇区组成，顶部和底部均等分配各一半，其余扇区均为 256 KB
- 256 或 512 字节的页写入缓存
- 1024字节（32 × 32字节） 的OTP安全硅阵列
- 八线接口（8S-8S-8S、8D-8D-8D）
  - 符合 JEDEC 扩展串行外设接口 (SPI) (JESD251) 标准
  - SDR 选项运行速度高达 200 MBps（200 MHz 时钟速度）
  - DDR 选项运行速度高达 400 MBps（200 MHz 时钟速度）
  - 支持数据选通（DS），简化高速系统中的读取数据捕获
- 功能安全特性
  - 功能安全符合 ISO26262 ASIL B 标准并符合 ASIL-D 标准
  - 英飞凌 Endurance Flex 架构提供高耐久性和长保留分区
  - 接口 CRC（循环冗余校验）检测主控控制器和SEMPER™闪存存储器之间通讯接口上的错误
  - 数据完整性CRC（循环冗余校验）检测内存阵列中的错误
  - SafeBoot 报告器件初始化失败、检测配置损坏并提供恢复选项
  - 内置纠错码 (ECC) 可以在内存阵列数据上纠正单比特错误并检测双比特错误 (SECDED)
  - 扇区擦除状态指示器可以提示擦除过程中的意外掉电
- 保护功能
  - 用于内存阵列和器件配置的传统扇区写保护
  - 针对每个内存阵列扇区的高级扇区保护
- 自动启动可支持上电后立即访问内存阵列
- 通过 CS# 信号方法 (JEDEC) 或单独的 RESET# 引脚进行硬件复位
- 串行闪存设备可发现参数 (SFDP)用来描述器件功能和特性
- 器件标识、制造商标识和唯一标识
- 数据完整性
  - 512 Mb 设备
    - 主阵列至少可进行 1,280,000 次写入-擦除循环
  - 1 Gb 设备
    - 主阵列至少可进行 2,560,000 次写入-擦除循环
  - 所有设备
    - 4KB 扇区至少可进行 300,000 次写入-擦除循环
    - 至少 25 年的数据保留时间

性能总结

- 供电电压
  - 1.7 V 至 2.0 V（HS-T）
  - 2.7 V 至 3.6 V（HL-T）
- 等级/温度范围
  - 工业级（–40°C ~ +85°C）
  - 扩展的工业级（ –40°C ~ +105°C）
  - 汽车级，AEC-Q100 3 级（–40°C ~ +85°C）
  - 汽车级，AEC-Q100 2 级（–40°C ~ +105°C）
  - 汽车级，AEC-Q100 1 级（–40°C ~ +125°C）
- 封装
  - 512 Mb：24球BGA6×88毫米
  - 1Gb：24球BGA8×8毫米

# 性能总结

**表 1　　最大读取率**

| Transaction | Initial access latency (Cycles) | Clock rate (MHz) | MBps |
|---|---|---|---|
| SPI Read | 0 | 50 | 6.25 |
| SPI Read Fast | 10 | 166 | 20.75 |
| Octal Read SDR (HS-T) | 16 | 200 | 200 |
| Octal Read SDR (HL-T) | 14 | 166 | 166 |
| Octal Read DDR (HS-T) | 23 | 200 | 400 |
| Octal Read DDR (HL-T) | 20 | 166 | 332 |

**表 2　　典型编程和擦除速率**

| Operation | KBps |
|---|---|
| 256B Page programming (4 KB Sector / 256 KB Sector) | 595 / 533 |
| 512B Page programming (4 KB Sector / 256 KB Sector) | 753 / 898 |
| 256KB Sector Erase | 331 |
| 4KB Sector Erase | 95 |

**表 3　　典型电流消耗**

| Operation | HL-T current (mA) | HS-T current (mA) |
|---|---|---|
| SDR Read 50 MHz | 10 | 10 |
| SDR Read (Octal) | 75 (166 MHz) | 156 (200 MHz) |
| DDR Read (Octal) | 75 (166 MHz) | 156 (200 MHz) |
| Program | 50 | 50 |
| Erase | 50 | 50 |
| Standby | 0.014 | 0.011 |
| Deep Power Down | 0.0022 | 0.0013 |

# 数据完整性

**表 4　　写入/擦除 (PE) 耐久性 - 高耐久性 (256KB 扇区)**

| Sectors in partition | Minimum PE cycles<br>512-Mb and 1-Gb products | Minimum retention time | Unit |
|---|---|---|---|
| 512 (Default for 1Gb devices) | 2,560,000 | 2 | Years |
| 508 | 2,540,000 | | |
| 504 | 2,520,000 | | |
| ... | ... | | |
| 256 (Default for 512Mb devices) | 1,280,000 | | |
| 252 | 1,260,000 | | |
| ... | ... | | |
| 28 | 140,000 | | |
| 24 | 120,000 | | |
| 20 | 100,000 | | |

**注释：**最小周期是针对整个高耐久性分区的。

**表 5　　写入/擦除耐久性 - 长数据保持分区（256 KB 扇区）**

| Minimum PE cycles | Minimum retention time | Unit |
|---|---|---|
| 500 | 25 | Years |

**注释：**最小周期针对每个扇区。

**表 6　　写入/擦除耐久性 4 KB 扇区和非易失性寄存器阵列**

| Flash memory type | Minimum cycles | Unit | Minimum retention time | Unit |
|---|---|---|---|---|
| Program/Erase cycles per 4KB sector | 500 | PE cycles | 25 | Years |
| | 300,000<br>**Note** It is required to restrict the power loss events to 300 times per sector during program or erase operation to achieve the mentioned endurance cycles. | | 2 | |
| Program/Erase cycles per Persistent Protection Bits (PPB) array or non-volatile register array<br>**Note** Each write transaction to a non-volatile register causes a PE cycle on the entire non-volatile register array. | 500 | | 25 | |

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# 1 引脚分配和信号描述

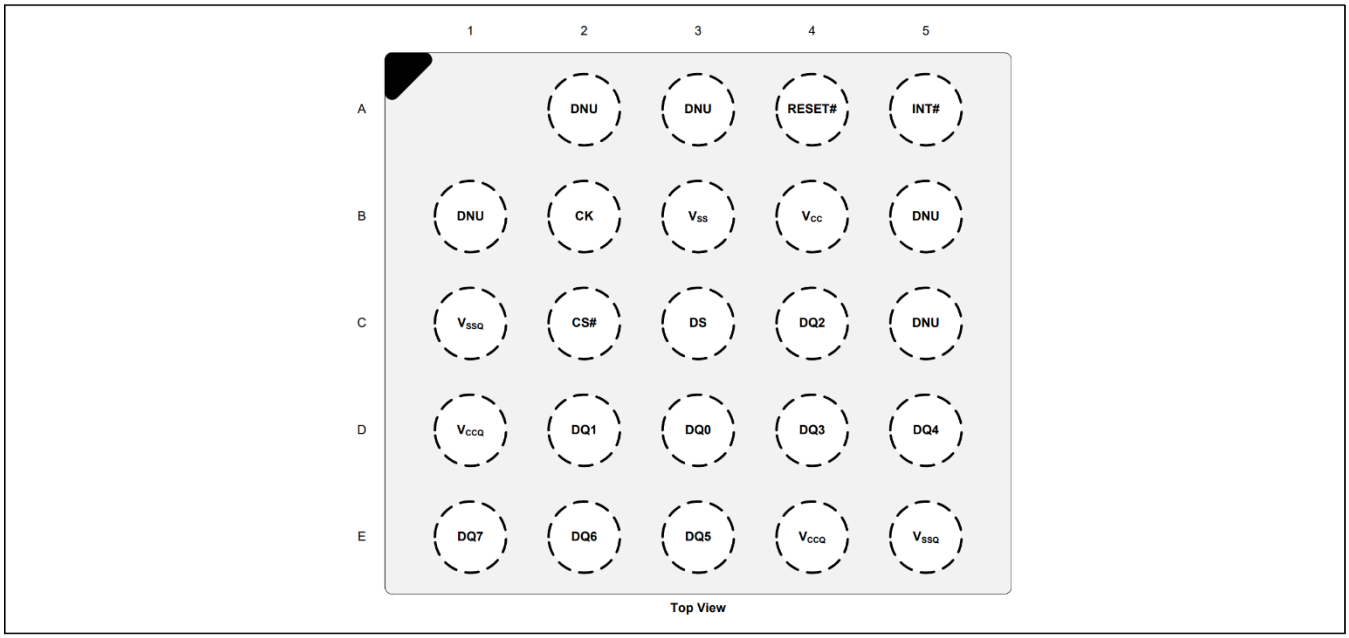


**图 1 24 球BGA引脚分布配置**[1]

**注释：**

1. 如果使用超声波清洁方法，BGA封装的闪存器件可能被损坏。如果封装体长时间暴露在 150°C 以上的温度下，封装和/或数据完整性可能会受到损害。

**表 7　　信号描述**

| Symbol | Type | Mandatory / optional | Description |
|---|---|---|---|
| CS# | Input | Mandatory | **Chip Select (CS#).** All bus transactions are initiated with a HIGH to LOW transition on CS# and terminated with a LOW to HIGH transition on CS#. Driving CS# LOW enables the device, placing it in the active mode. When CS# is driven HIGH, the device enters standby mode, unless an internal embedded operation is in progress. All other input pins are ignored and the output pins are put in high impedance state. On parts where the pin configuration offers a dedicated RESET# pin, it remains active when CS# is HIGH. |
| CK | | | **Clock (CK)**. Clock provides the timing of the serial interface. Transac- tions are latched on the rising edge of the clock. In SDR protocol, command, address and data inputs are latched on the rising edge of the clock, while data is output on the falling edge of the clock. In DDR protocol, command, address and data inputs are latched on both edges of the clock, and data is output on both edges of the clock. |
| DS | Output | | **Read Data Strobe (DS)**. DS is used for data read operations only and indicates output data valid for SDR/DDR modes. During a read trans- action while CS# is LOW, DS toggles to synchronize data output until CS# goes High. |
| DQ[7:0] | Input/ Output | | **Serial Data (DQ[7:0])**. Bidirectional signals that transfer command, address and data information.<br>**Legacy (x1) SPI Interface**. DQ[0] is an input (SI) and DQ[1] is an output (SO).<br>**Octal (x8) Interface**. DQ[7:0] are input and output. |
| RESET# | Input (weak pull-up) | Optional | **Hardware Reset (RESET#)**. When LOW, the device will self initialize and return to the array read state. DS and DQ[7:0] are placed into the high impedance state when RESET# is LOW. RESET# includes a weak pull-up, meaning, if RESET# is left unconnected it will be pulled up to the HIGH state on its own. |
| INT# | Output (Open Drain) | | **System Interrupt (INT#)**. When LOW, the device is indicating that an internal event has occurred. This signal is intended to be used as a system level interrupt for the device to indicate that an on-chip event has occurred. INT# is an open-drain output. The recommended pull-up resistor for the INT# outputs is 5 kΩ to 10 kΩ. |
| $V_{CC}$ | Power supply | Mandatory | Core Power Supply |
| $V_{CCQ}$ | | | Input / Output Power Supply |
| $V_{SS}$ | Ground supply | | Core Ground |
| $V_{SSQ}$ | | | Input / Output Ground |
| DNU | – | – | Do Not Use |

# 2 接口概述

## 2.1 概述

SEMPER™闪存存储器八线系列产品是符合JEDECJESD251 eXpandedSPI (xSPI) 规范的高速 CMOS, MIRRORBIT™ NOR 车载存储器件。SEMPER™闪存式存储器专为功能安全而设计，基于ISO 26262 标准进行开发，通过ASIL-B 等级认证并支持最高ASIL-D等级。

带有八线接口设备的SEMPER™闪存存储器同时支持八线外设接口 (OPI) 以及 Legacy x1 串行外设接口 ( SPI )。两个接口通过串行传输命令，从而减少了接口连接信号的数量。SPI 支持 SDR，而 OPI 同时支持 SDR 和 DDR。

从器件读取操作是并发导向的。读取传输可以配置为使用回卷并发或线性并发。回卷并发从单个页读取，而线性突发可以读取整个存储阵列。

每个存储器位的擦除状态为一个逻辑1。编程操作会将逻辑1（低电平）修改为逻辑0（高电平）。只有擦除操作才能将内存位从 0 更改为 1。擦除必须对完整扇区（4 KB 或 256 KB）执行擦除操作。

SEMPER™闪存存储器提供灵活的扇区布局。地址空间既可以配置为统一的 256 KB 扇区阵列，也可以配置为混合配置 1，其中32个 4 KB 扇区分组在顶部或底部，而剩余的扇区全部为 256 KB，或者配置为混合配置 2，其中32个 4 KB 扇区在顶部和底部之间平均分配各半，而剩余的扇区全部为 256 KB。

在单个写入操作期间使用的页写入缓存可配置为 256 字节或 512 字节。512 字节选项提供最高的写入吞吐量。

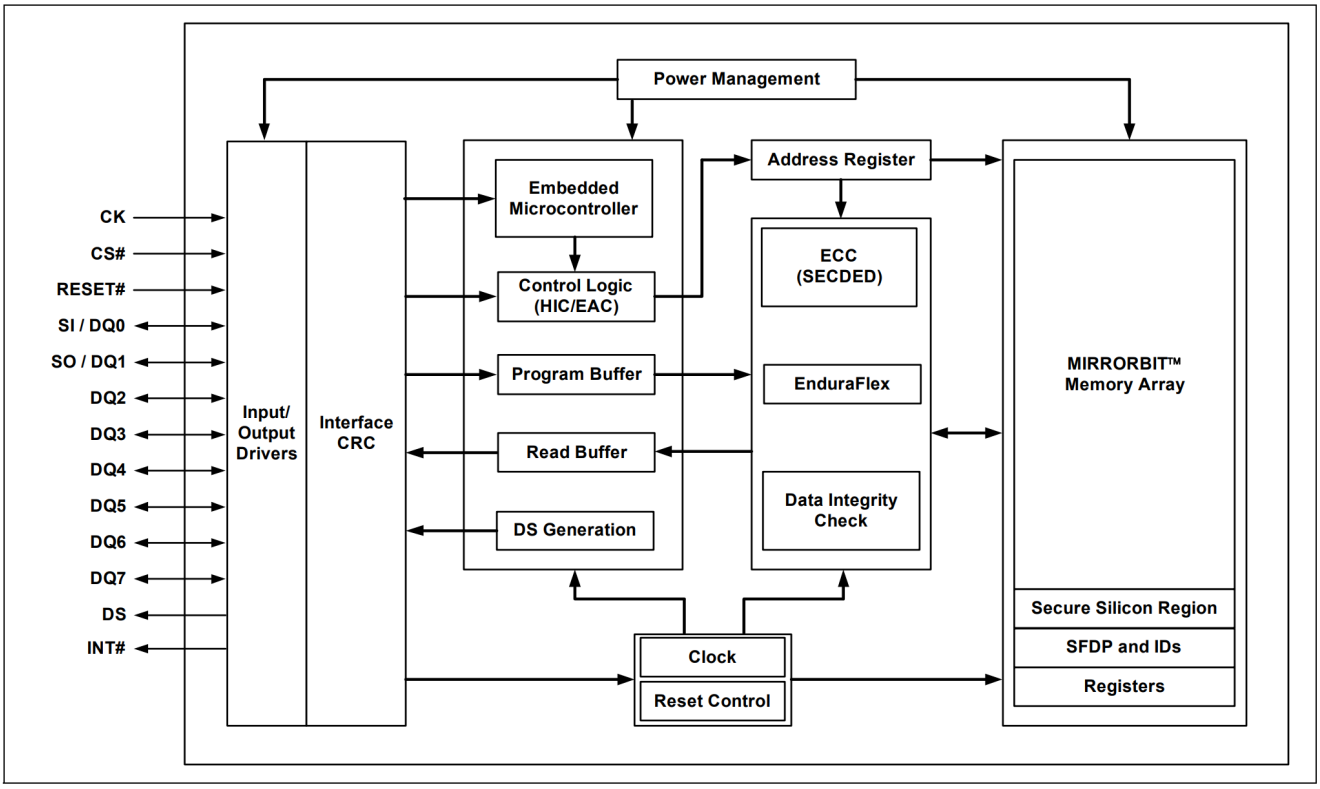


**图 2 逻辑框图**

接口概述

配备Qctal SPI接口的SEMPER™ 闪存式存储器由多种容量组成，具有 1.8 V 和 3.0 V 核心和 I/O 电压选项。

器件控制逻辑分成两个并行的操作区，Host Interface Controller（主机接口控制器，HIC）和Embedded Algorithm Controller（嵌入式算法控制器，EAC）。HIC监控器件输入的信号电平，并根据需要驱动输出，以完成与主机系统间的读取和写入数据传输。HIC在读取传输时将传递当前所在的地址映射中的数据；将写入传输地址和数据信息放入EAC指令存储器内；告知EAC电源转换以及写入传输。EAC在写入传输后查看指令存储器中的合法指令序列，并执行相关的嵌入式算法。

更改存储器阵列中的非易失性数据时，需要执行复杂的操作序列，这些操作被称为嵌入式算法（EA）。这些算法完全由器件内部的EAC来管理。主算法执行主阵列数据的写入和擦除。主机系统将指令代码写入到闪存器件中。EAC接收指令用于执行所有必要的步骤以完成指令，并在EA执行期间提供状态信息。

除了强制的SPI信号 CK、CS#、 SI /DQ0、SO/DQ1 和 DQ[7:2] 外，具有八线接口器件的SEMPER™闪存式存储器还包括 RESET#、 DS和 INT# 信号。RESET# 从低电平到高电平的转换将使器件返回到内部上电复位 (POR) 后发生的默认状态。数据选通（ DS ）在读取事务期间与输出数据同步，使主控系统能够以高时钟频率操作捕获数据。INT# 是一个漏极开路输出，可以向器件主控器提供一个中断信号，以指示器件在编程或擦除操作结束时从忙碌状态转换为就绪状态，或指示在读取过程中检测到错误 ( ECC )。

英飞凌 Endurance Flex 架构使得系统设计人员能够根据其特定应用来定制 NOR 闪存擦写耐久性和数据保持特性。主控定义高耐久性或长保留时间的分区，提供高达 100 万次以上的擦写循环或 25 年的数据保留时间。

配备Qctal SPI接口的SEMPER™ 闪存式存储器通过在存储器阵列写入期间生成嵌入式汉明纠错码来支持错误检测和纠正。然后，该 ECC 码用于读取过程中单比特位和双比特位错误检测以及单比特位错误纠正。

配备Qctal SPI接口的SEMPER™ 闪存式存储器具有内置诊断功能，为主控系统提供器件状态。

- 写入和擦除操作：报告写入或擦除成功、失败和暂停状态
- 错误检测与纠正：具有地址捕获和错误计数的 1 比特位和/或 2 比特位错误状态
- 数据完整性检查：对内存阵列内容进行错误检测
- 接口 CRC（循环冗余校验）：器件接口上的错误检测
- SafeBoot：报告正确的闪存式存储器初始化和配置损坏恢复
- 扇区擦除状态：报告每个扇区的擦除成功或失败状态
- 扇区擦除计数器：计算每个扇区的擦除次数

## 2.2 信号协议

### 2.2.1 SEMPER™ 闪存式存储器的Octal和SPI时钟模式

配备Qctal SPI接口的SEMPER™ 闪存式存储器可由嵌入式总线主设备以以下两种时钟模式之一驱动：

- **模式 0**，时钟极性在 CS# 下降时处于低电平，并保持低电平，直到捕获输入时变为高电平。
- **模式 3**，时钟极性在 CS# 下降时为高电平，然后在捕获输入时由低电平变为高电平。

对于这两种模式， SDR协议中数据在 CK 信号的上升沿被锁存到器件中，而 DDR 协议中数据在 CK 信号的两个边沿被锁存到器件中。SDR协议中的输出数据在CK时钟信号的下降沿可用，DDR协议中的输出数据在CK时钟信号的上升沿可用。

两种模式的区别在于当总线主机处于待机模式且不传输任何数据时的时钟极性。

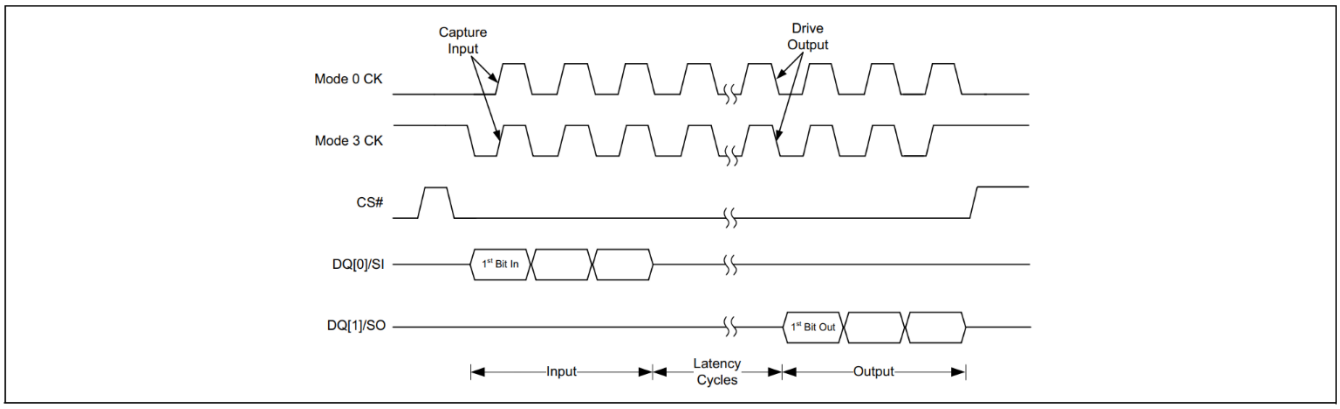


**图 3 SPI SDR 模式支持**

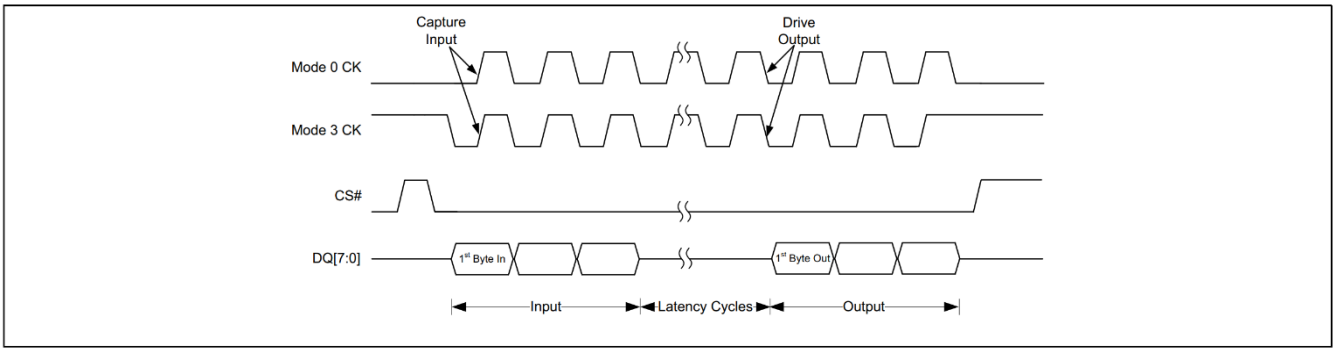


**图 4 八线SDR模式支持**

对于SEMPER™闪存式存储器八线 DDR 模式操作，仅支持时钟模式 0。

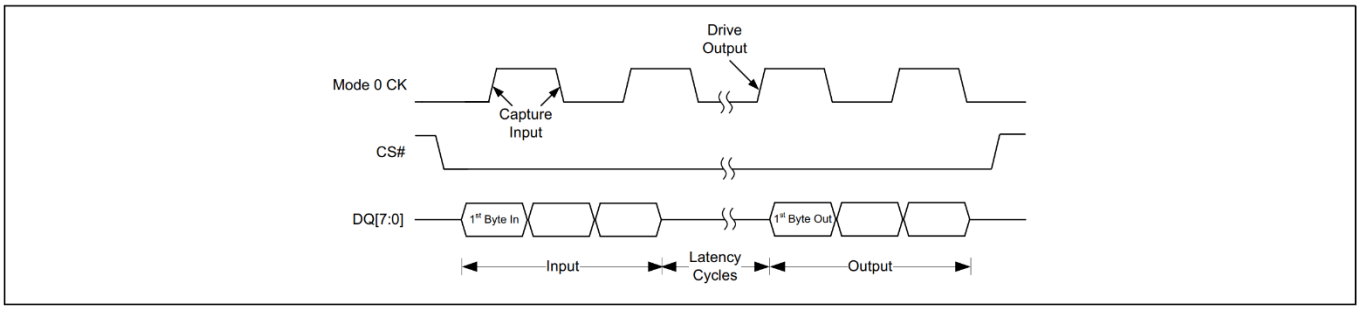


**图 5　　八线DDR模式支持**

## 2.3　　传输协议

### 命令传输

- 在 CS# 为选通（低电平）期间，时钟信号 (CK) 被切换，同时指令信息首先在数据 (DQ) 信号上传输，然后是地址和数据从主控传输到闪存式存储器器件。在从闪存式存储器件向主控传输读取数据或从主控向闪存式存储器件写入数据期间，时钟持续切换。当主控传输了所需数量的数据时，主控将驱动 CS# 处于非选通状态（高电平）。CS# 被选通的时间段称为总线上的一个命令传输。
- 当 CS# 处于非选通状态时，CK 无需切换。
- 指令发送发生在每次命令传输开始时。地址、延迟周期和数据传输阶段是可选的，它们的存在取决于传输的协议模式或指令。

### 传输采集

- CK 标记主控和存储器之间每个比特位或多个比特位的传输。指令、地址和写入数据位传输发生在SDR传输中的 CK 上升沿，或发生在 DDR 传输中的每个 CK 沿。

### 注释

- 在程序或擦除（嵌入式操作）期间，所有读取闪存阵列的尝试都将被忽略。嵌入式操作将继续执行，不会产生任何影响。在嵌入式操作期间，只能接受非常有限的指令。这些将在70页中的**“嵌入式操作的暂停与恢复”**小节中讨论。

### 协议术语

- 命令传输过程中使用的DQ信号的数量取决于当前的协议模式或传输的指令。延迟周期不使用 DQ 信号进行信息传输。协议模式选项由指令、地址和数据阶段使用的数据速率和 DQ 宽度（DQ 信号数）描述，格式如下：

  WR-WR-WR，其中：
  - 第一个WR是指令位宽度和速率。
  - 第二个WR是地址位宽度和速率。
  - 第三个WR是数据位宽度和速率。
- 位宽值可以是 1 或 8。R 的值为 S（对于 SDR）或 D（对于 DDR）。SDR在一个时钟周期的上升沿和下降沿具有相同的传输值。DDR 在每个时钟的上升沿和下降沿可以有不同的传输值。

- 示例：
  - 1S-1S-1S表示指令为1比特位宽SDR，地址为1比特位宽SDR，数据为1比特位宽SDR。
  - 8D-8D-8D 表示指令、地址和数据传输始终是 8 位宽 DDR。

### 协议定义

- SEMPER™闪存式存储器八线接口定义的协议模式：

  1.1S-1S-1S：指令传输、地址传输和数据传输期间使用一个 DQ 信号。 所有阶段均为 SDR。

  2.8S-8S-8S：指令传输、地址传输和数据传输期间使用八个 DQ 信号。 所有阶段均为 SDR。

  3.8D-8D-8D：指令传输、地址传输和数据传输期间使用八个 DQ 信号。 所有阶段均为 DDR。

### 1S-1S-1S 协议

- 1S-1S-1S 模式是上电复位 ( POR ) 后的首选默认协议，但闪存式存储器设备可配置为复位之后为八线模式。
- 每个传输都以一个 8 比特位（1 字节）指令开始。该指令选择要执行的信息传输类型或器件操作。
- 该协议使用SI/DQ[0]将信息从主控传输到闪存式存储器器件，使用SO/DQ[1]将信息从闪存式存储器器件传输到主控。在每个 DQ 上，信息按照每个字节内从最高有效位 (MSb) 到最低有效位 (LSb) 的顺序放置在 DQ 线上。连续地址字节按从最高顺序到最低顺序的顺序进行传输。连续数据字节按照从最低地址到最高地址的顺序进行传输。
- 在 1S-1S-1S 中，DQ[7:2] 不用于数据传输阶段。因此，DQ[7:2]信号将呈高阻态。

### 8S-8S-8S 和 8D-8D-8D 协议

- 每个传输都以一个 16 比特位（2个相同字节）指令开始。该指令选择要执行的信息传输类型或器件操作。
- 仅支持 4 字节寻址。
- 该协议使用 DQ[7:0] 信号。地址字节的 LSb 放置在 DQ[0] 上，每个高阶位放置在依次更高编号的 DQ 信号上。连续地址字节按从最高顺序到最低顺序的顺序进行传输。SDR 中的连续数据字节按照从最低地址到最高地址的顺序传输。DDR 中的连续数据字节仅以字节对（字）的形式传输，其中字节顺序取决于在该协议模式下写入或烧录字节的顺序。连续数据字节按照从最低地址到最高地址的顺序进行传输。
- 在该协议中，在读取事务的数据传输期间，数据选通（ DS ）信号由闪存式存储器器件驱动，并且转换与 DQ 信号数据转换同步（在 DDR 协议中为边缘对齐，在SDR协议中为中心对齐）。DS 用作附加输出信号，具有与其他数据输出相同的时序特性，但保证随着每个数据位的传输而发生转换。

13 页 **“串行外设接口 （ SPI， 1S-1S-1S）”** 按协议模式显示所有命令传输格式。

### 2.3.1 串行外设接口（SPI、1S-1S-1S）

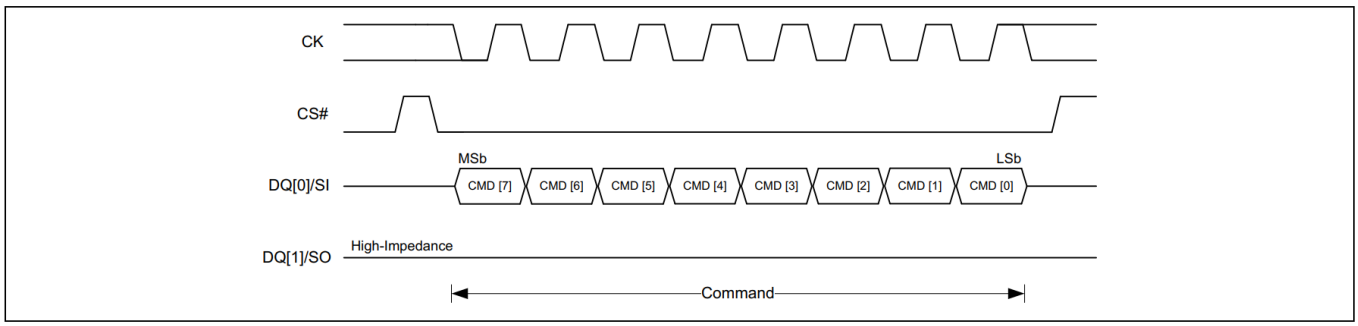


**图 6 带指令输入的SPI传输**

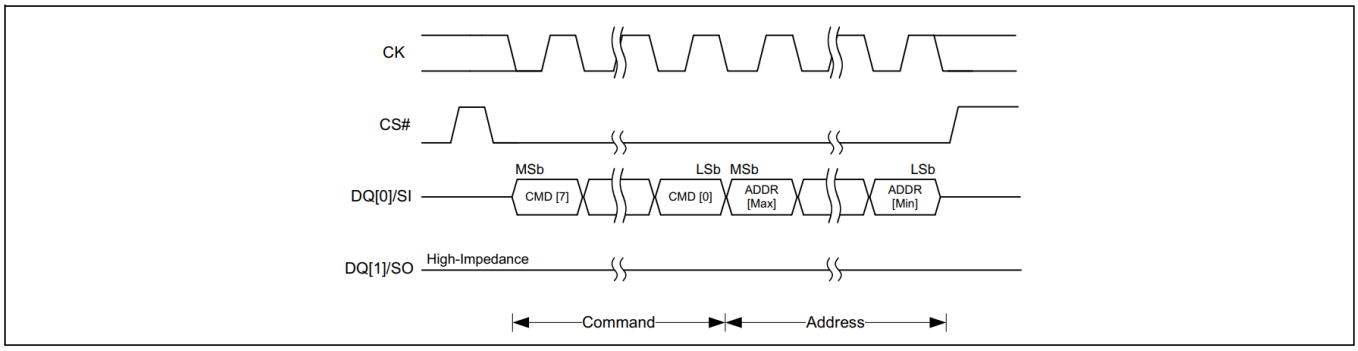


**图 7 带有指令和地址输入的SPI传输**

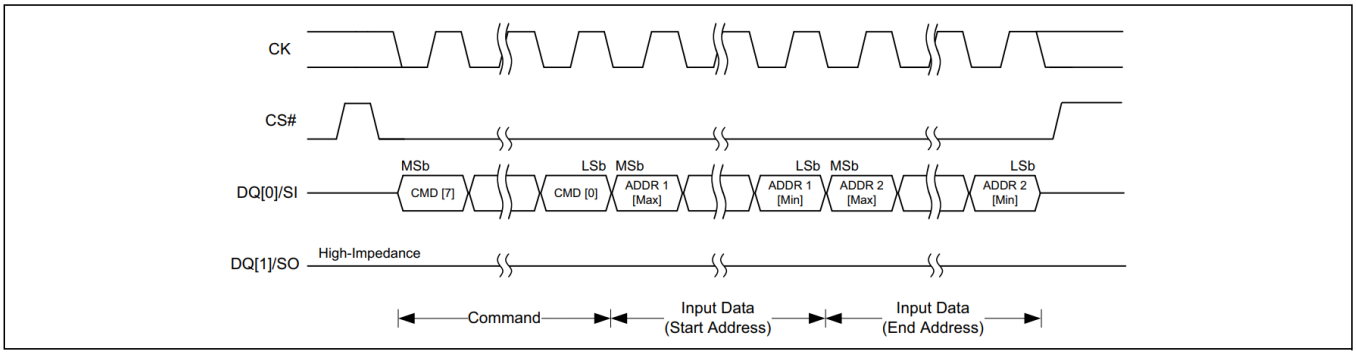


**图 8 带有指令和两个输入地址的SPI传输**

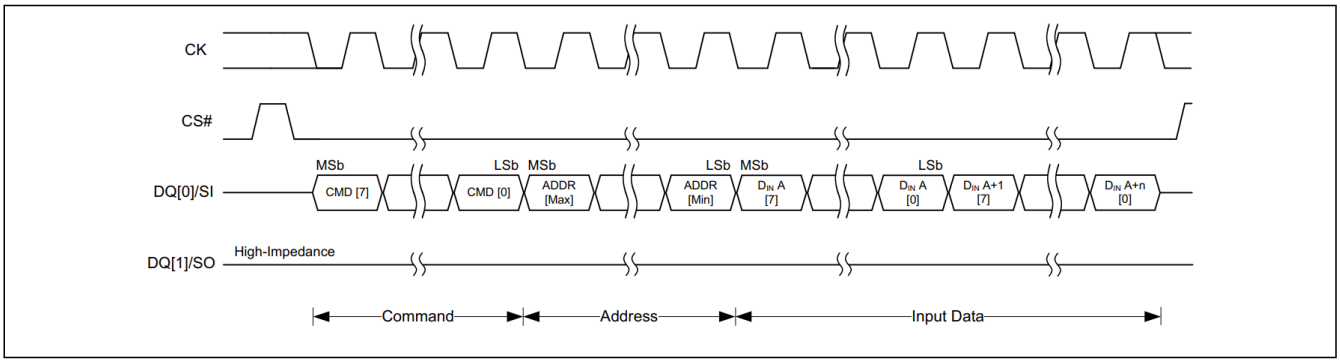


**图 9　　带有指令、地址和数据输入的SPI写入传输**

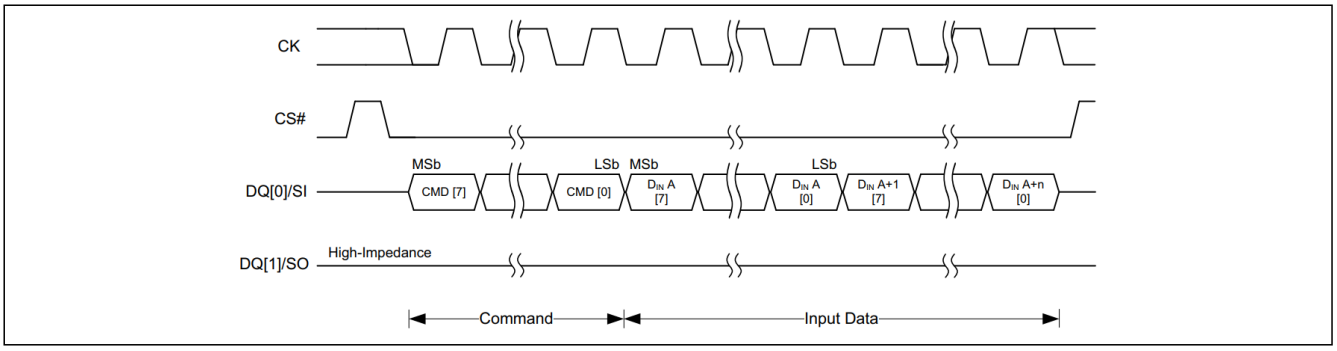


**图 10　　带有指令和数据输入的SPI写入传输**

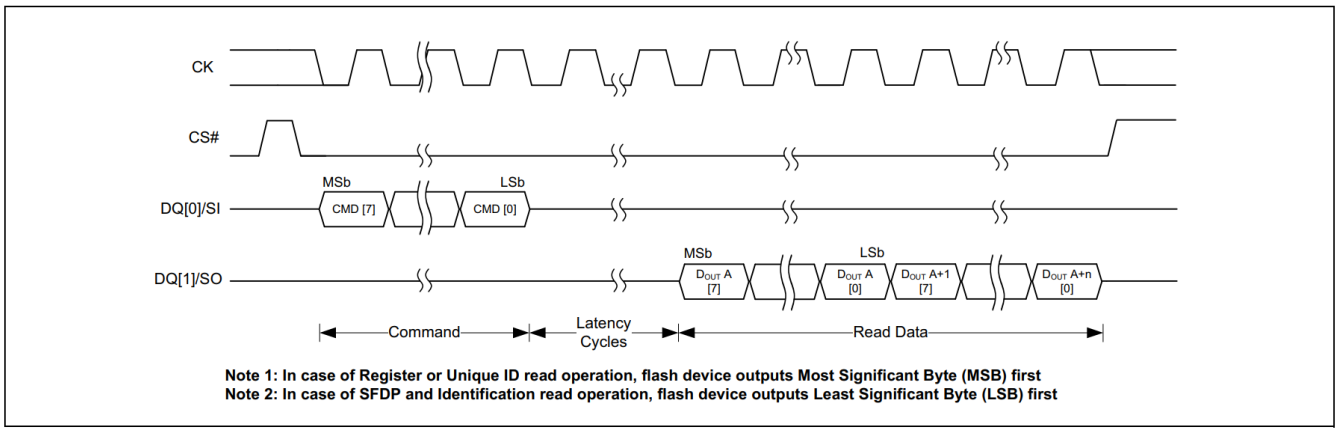


**图 11　　带有指令输入的SPI读取事务（输出延迟）**

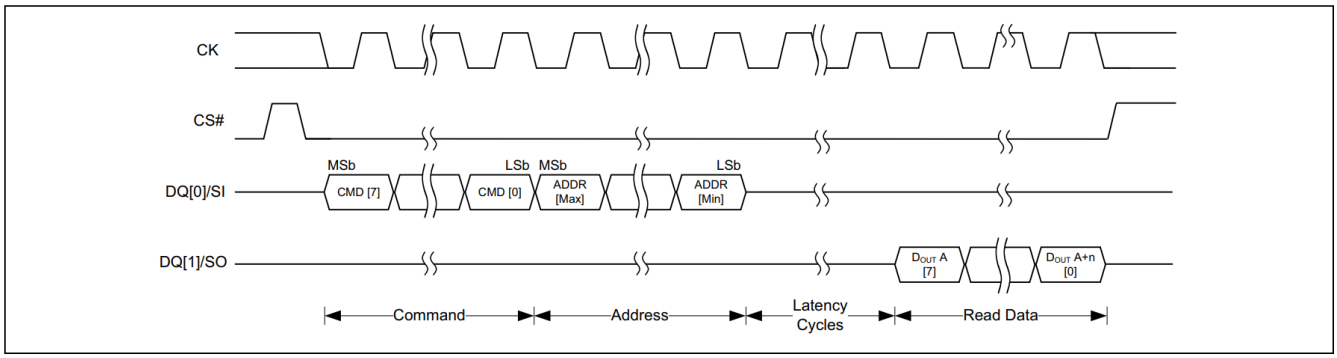


**图 12　　具有指令和地址输入的SPI读取传输（无输出延迟）**

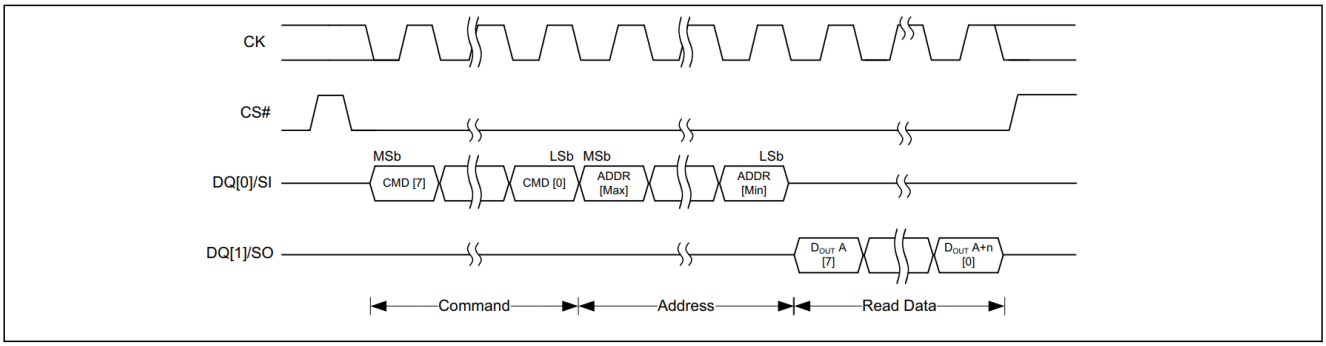


**图 13　　具有指令和地址输入的SPI读取传输（无输出延迟）**

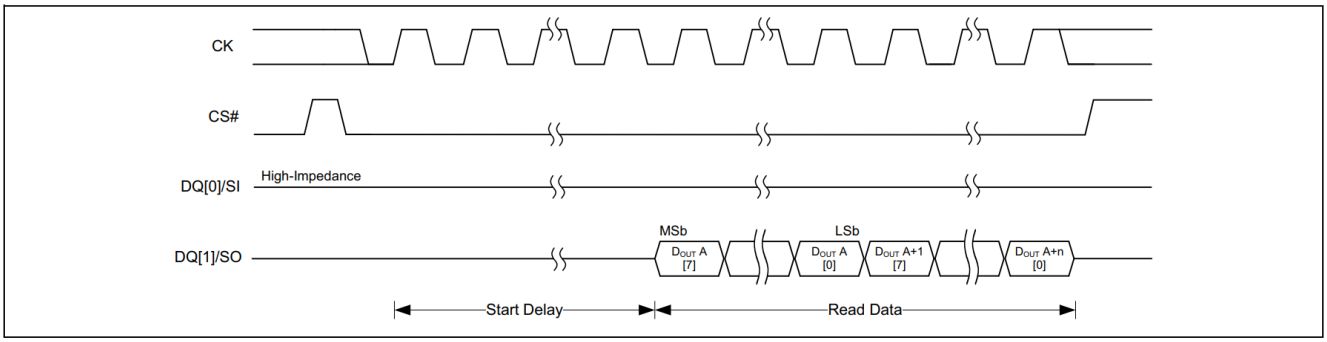


**图 14　　带输出数据序列的 SPI 传输（AutoBoot）**

### 2.3.2 八线外设接口（八线、8S-8S-8S 和 8D-8D-8D）

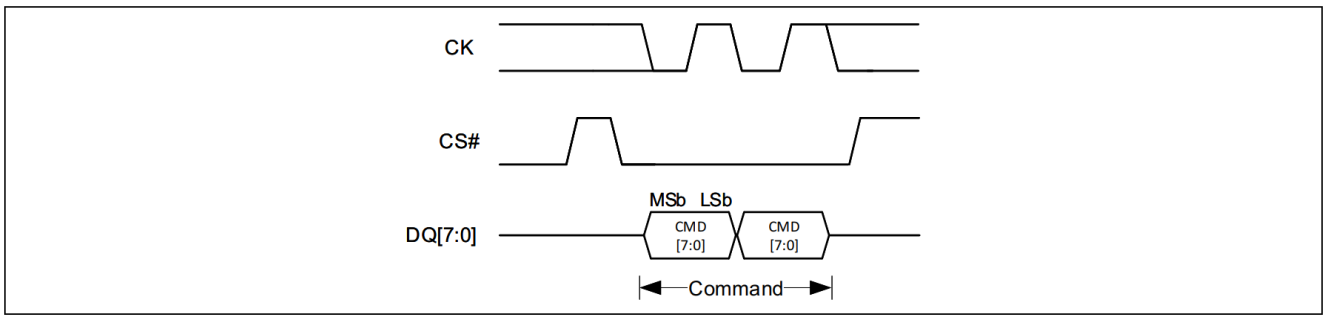


**图 15 带指令输入的 Octal SDR传输**

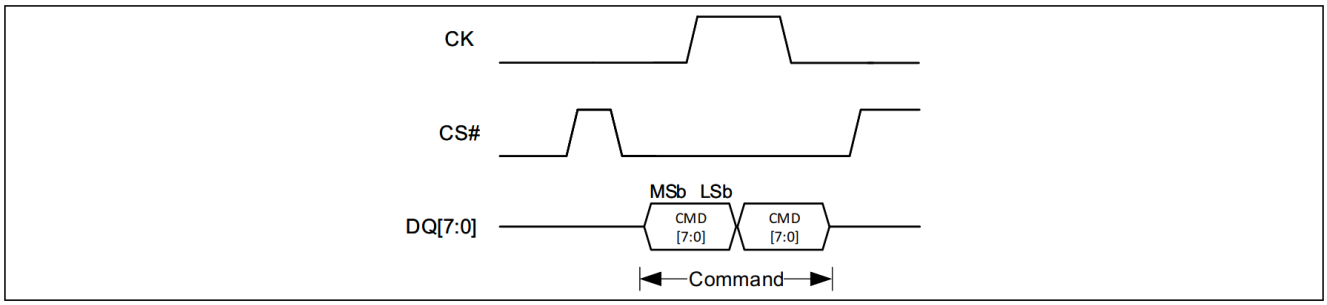


**图 16 带指令输入的 Octal SDR传输**

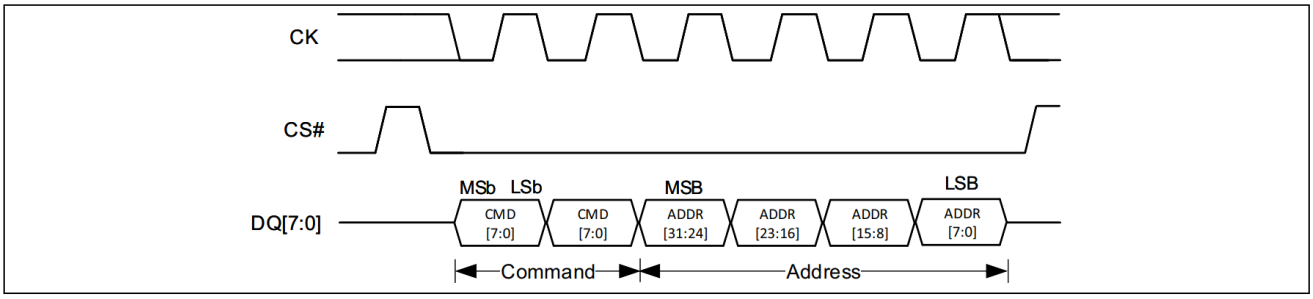


**图 17　　具有指令和地址输入的 Octal SDR 传输**

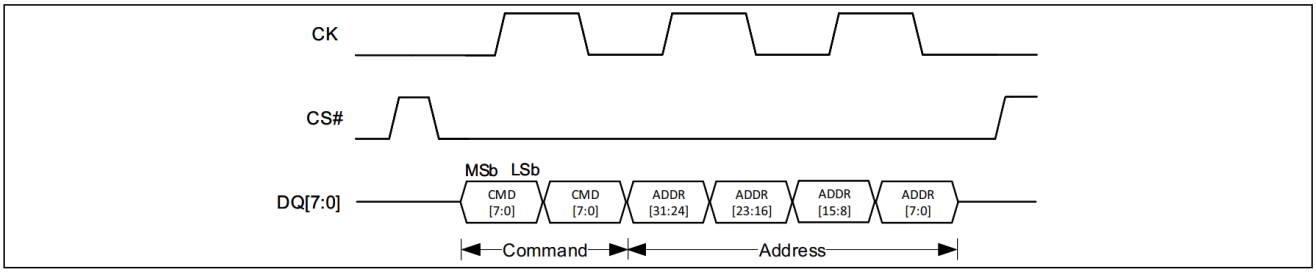


**图 18　　具有指令和地址输入的 Octal SDR传输**[2]

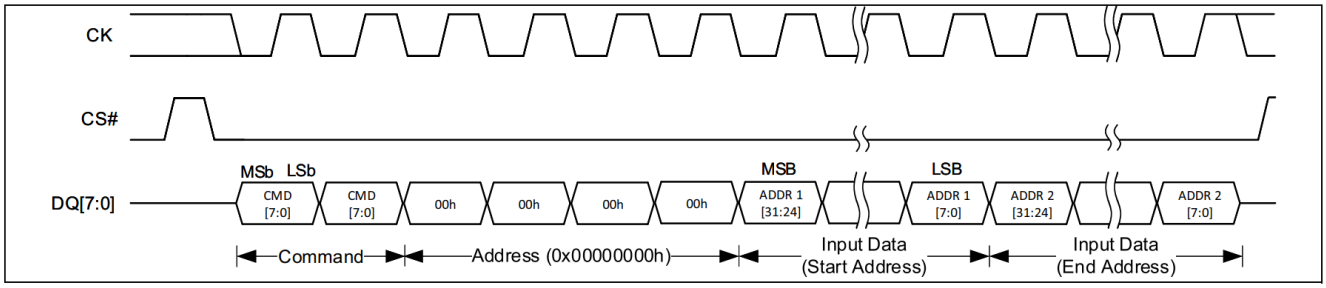


**图 19　　带有指令和两个输入地址的 Octal SDR 传输**

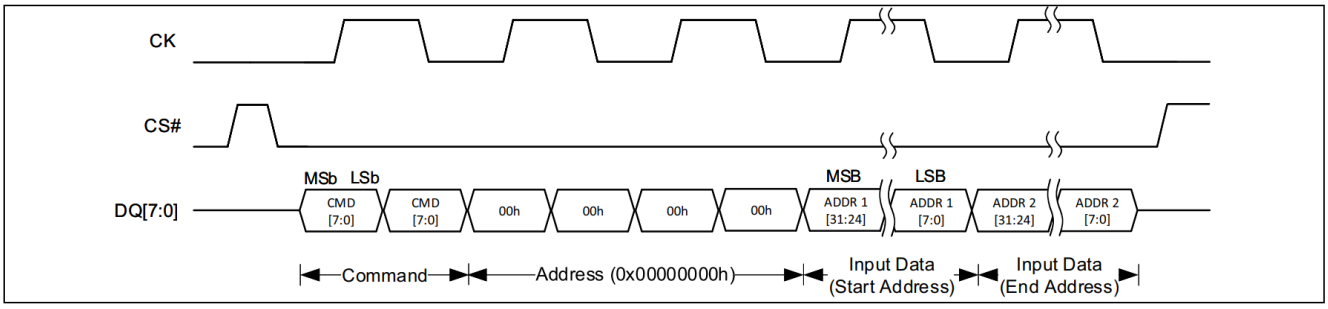


**图 20　　带有指令和两个输入地址的 Octal DDR 传输**

**注释：**
2. 在使用地址输入的任何八线 DDR 事务中，地址的 LSb 始终为零。

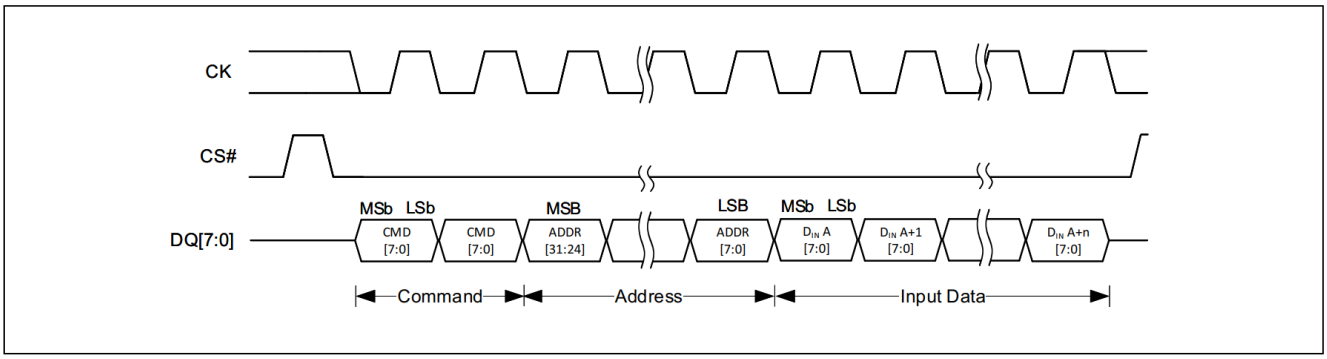


**图 21　　具有指令、地址和数据输入的 Octal SDR写入传输**

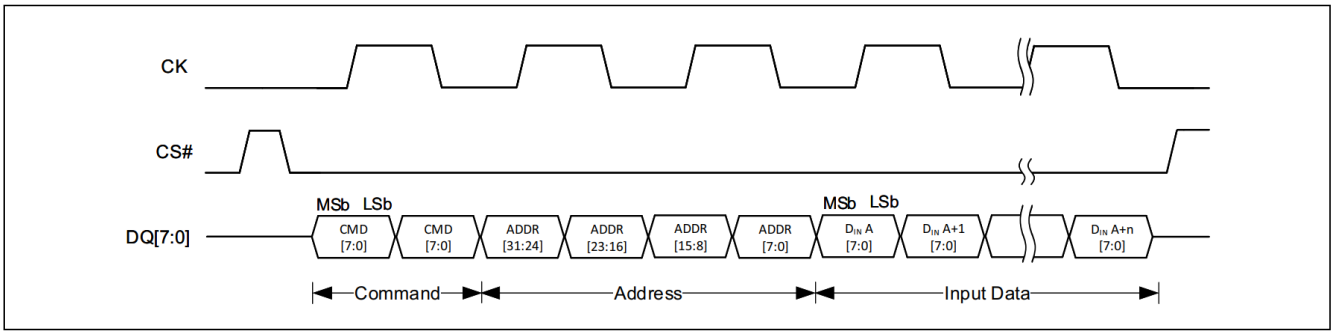


**图 22　　具有指令、地址和数据输入的 Octal DDR写入传输**[3]

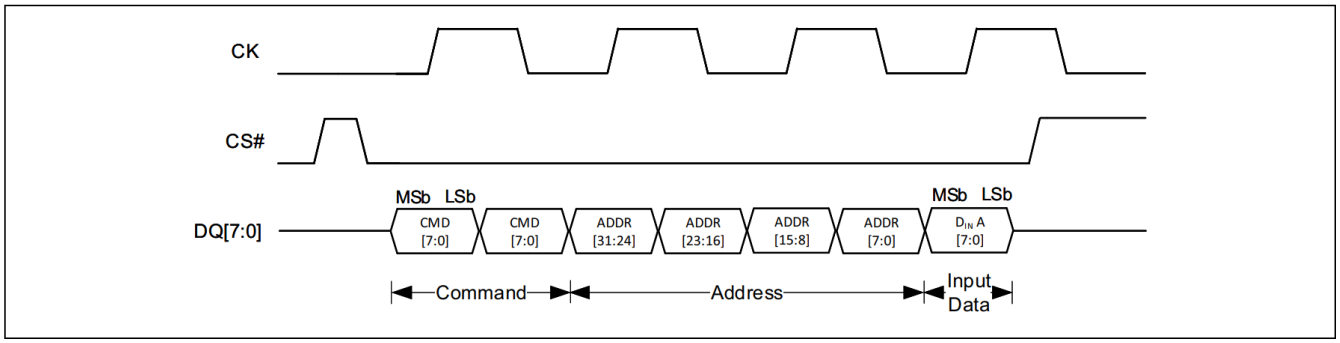


**图 23　　带有指令、地址和单字节数据输入的Octal DDR 写入传输**[3]

**注释：**
3. 在使用地址输入的任何八线 DDR 事务中，地址的 LSb 始终为零。

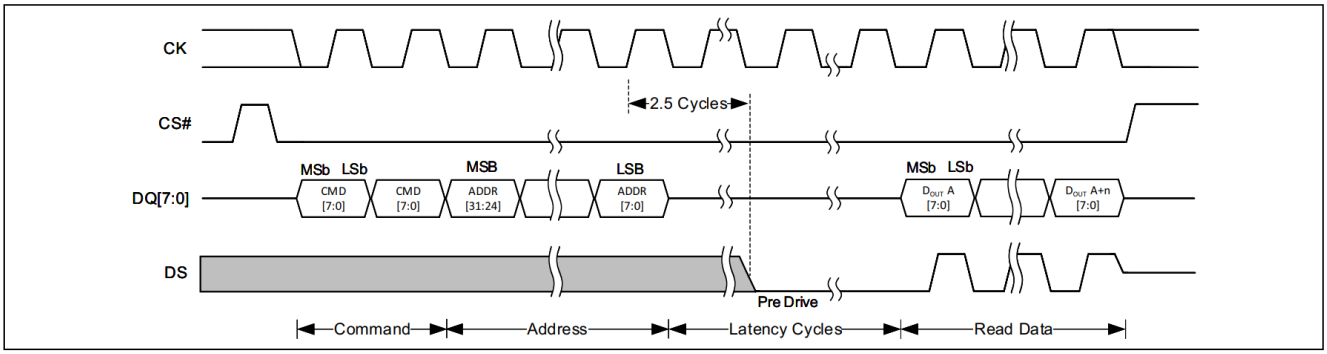


**图 24　　使用指令和地址输入的 Octal SDR 读取传输（输出延迟）**

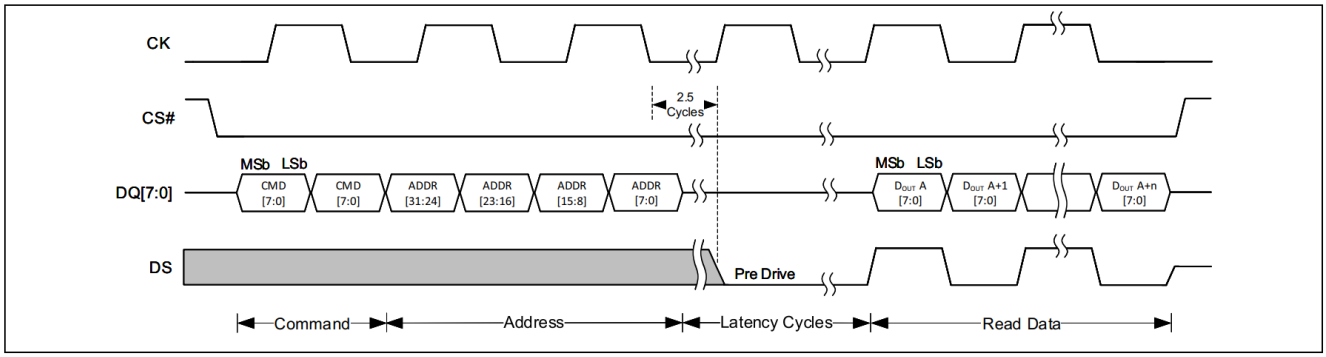


**图 25　　具有指令和地址输入的 Octal DDR 读取传输（输出延迟）** [4, 5]

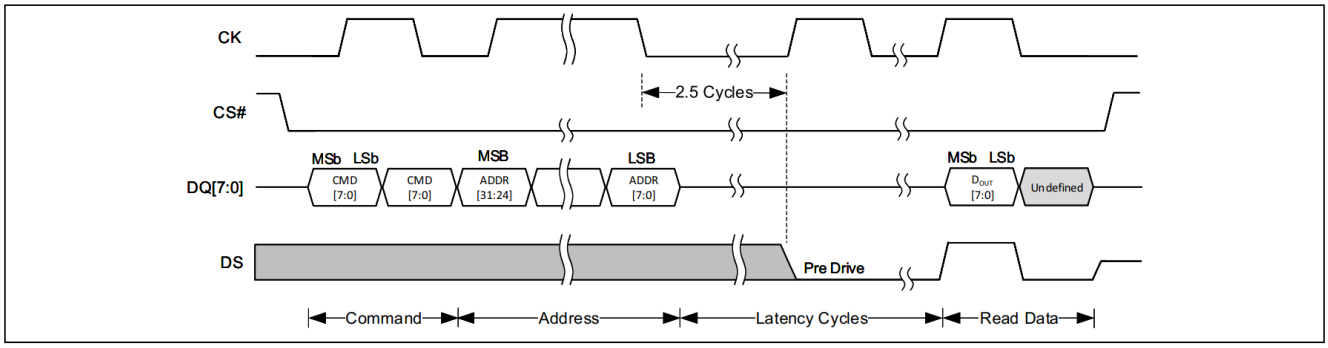


**图 26　　使用指令和地址输入的八线 DDR 读取传输（输出延迟）** [6]

**注释：**
4. 在使用地址输入的任何八线 DDR 事务中，地址的 LSb 始终为零。
5. 读取接口 CRC（循环冗余校验） 事务仅支持八线 DDR。

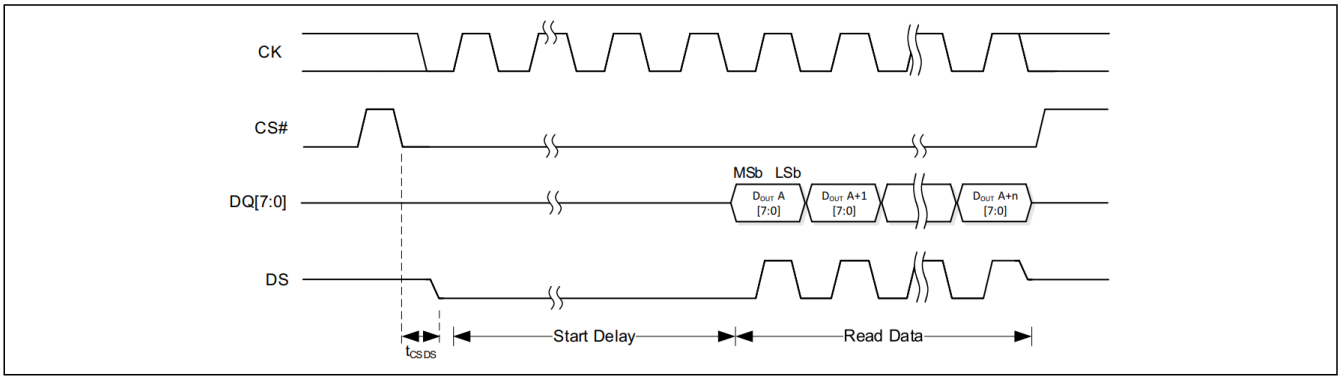


**图 27　　具有输出数据序列的 Octal SDR 传输（AutoBoot）**

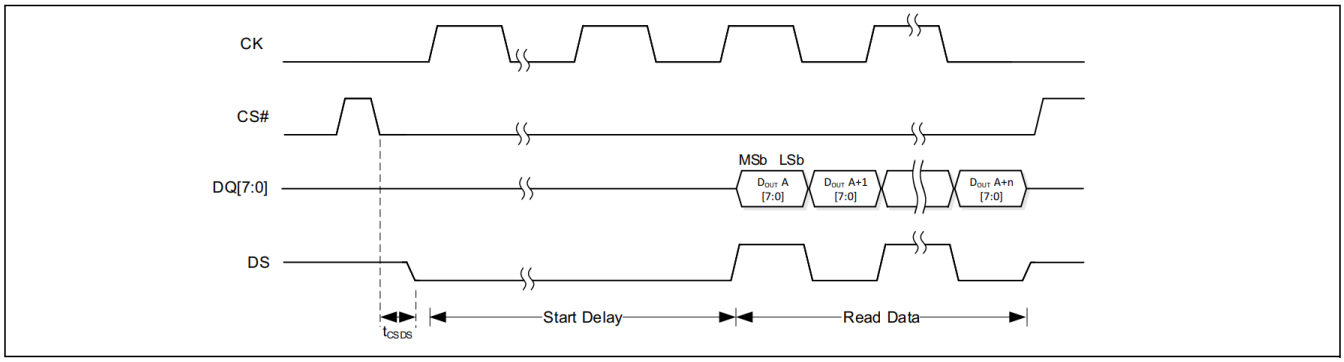


**图 28　　具有输出数据序列的 Octal DDR 传输（AutoBoot）**

## 2.4 寄存器命名规则

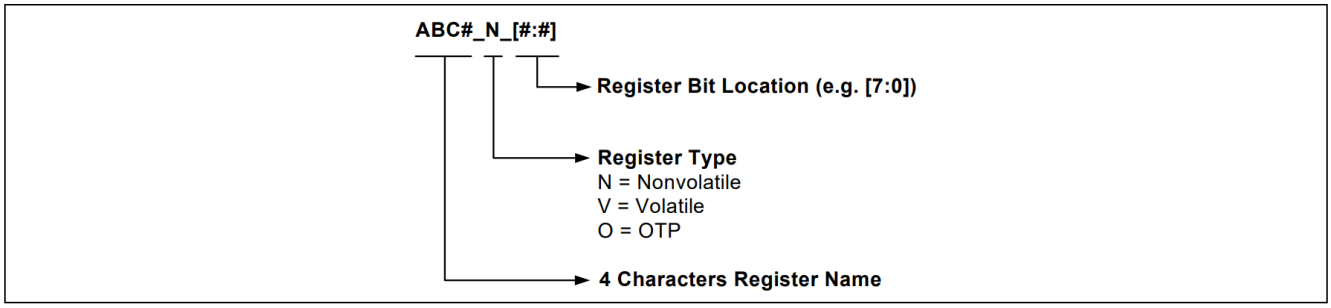


**图 29 寄存器命名规则**

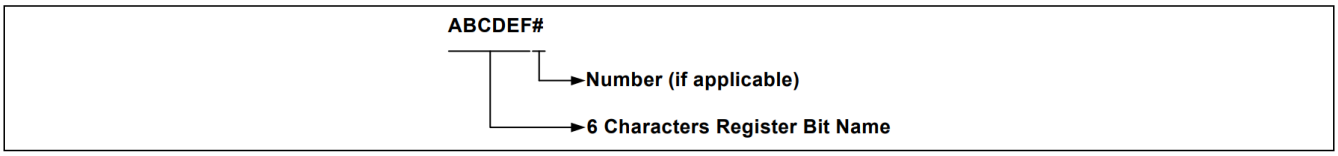


**图 30 寄存器位命名规则**

## 2.5 命令传输命名规则

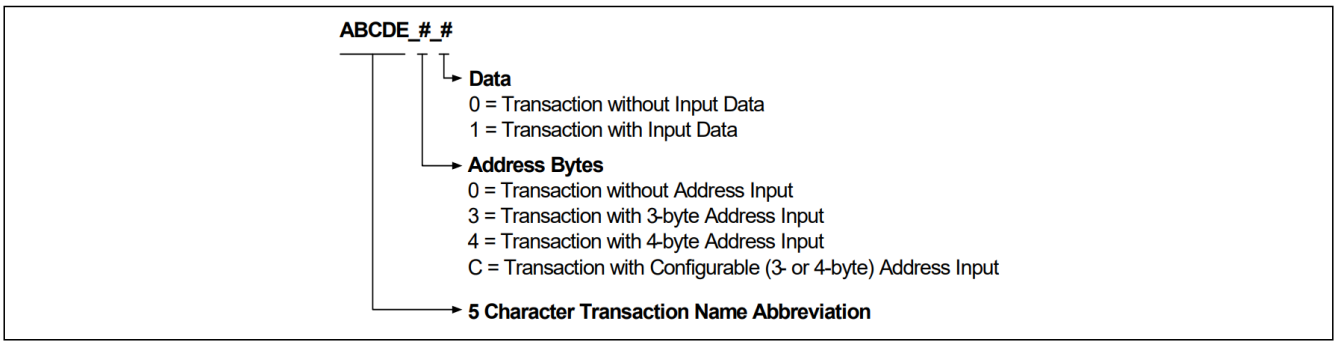


**图 31 命令传输命名规则**

# 3 地址空间映射

HL-T/HS-T系列支持24位和32位（4字节）地址，以支持512 Mb或1 Gb容量的设备。4 字节地址允许直接寻址最多 4 GB (32 Gb) 的地址空间。可以通过写入相应的配置寄存器来更改地址字节选项，或者也可以使用单独的传输进入（EN4BA_0_0）和退出（EX4BA_0_0）4 字节地址模式。

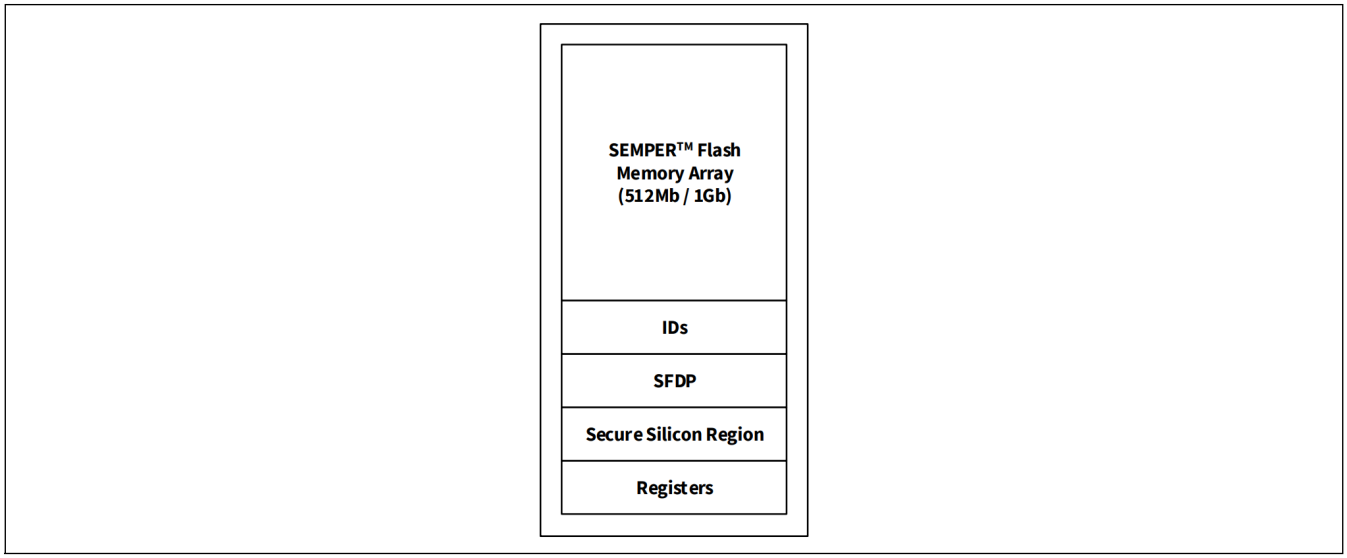


**图 32 HL-T/HS-T 地址空间映射概述**

## 3.1 SEMPER™闪存式存储器存储阵列

闪存式存储器主要的扇区结构被划分为单元并称之为物理扇区。

HL-T/HS-T系列扇区分布支持以下选项：

- 512 Mb、1 Gb 支持 256 KB 统一扇区选项
- 512 Mb、1 Gb 混合扇区选项
  - 物理的 32 个 4 KB 扇区和 1 个 128 KB 扇区配置为地址空间顶部或底部，其余所有扇区均为 256 KB
  - 地址空间的顶部和底部均设有各 16 个 4 KB 物理的扇区和 1 个 192 KB 扇区，其余所有扇区均为 256 KB

配置寄存器1和配置寄存器3中的扇区架构选择位的组合支持HL-T/HS-T家族的不同扇区架构选项。更多信息请参见82页 **“寄存器”** 。

地址空间映射

**表8　256KB统一扇区地址映射**[7]

| Sector size (KB) | S28HL01GT and S28HS01GT | | | S28HL512T and S28HS512T | | |
|---|---|---|---|---|---|---|
| | Sector count | Sector range | Byte address range (sector starting address–sector ending address) | Sector count | Sector range | Byte address range (sector starting address–sector ending address) |
| 256 | 512 | SA00 | 00000000h–0003FFFFh | 256 | SA00 | 00000000h–0003FFFFh |
| | | : | : | | : | : |
| | | SA511 | 07FC0000h–07FFFFFFh | | SA255 | 03FC0000h–03FFFFFFh |

**注：**
7. 配置：CFR3N[3] = 1。

**表 9　底部混合配置三十二个 4 KB 扇区和 256 KB 统一扇区地址映射**[8]

| Sector size (KB) | S28HL01GT and S28HS01GT | | | S28HL512T and S28HS512T | | |
|---|---|---|---|---|---|---|
| | Sector count | Sector range | Byte address range (sector starting address–sector ending address) | Sector count | Sector range | Byte address range (sector starting address–sector ending address) |
| 4 | 32 | SA00 | 00000000h–00000FFFh | 32 | SA00 | 00000000h–00000FFFh |
| | | : | : | | : | : |
| | | SA31 | 0001F000h–0001FFFFh | | SA31 | 0001F000h–0001FFFFh |
| 128 | 1 | SA32 | 00020000h–0003FFFFh | 1 | SA32 | 00020000h–0003FFFFh |
| 256 | 511 | SA33 | 00040000h–0007FFFFh | 255 | SA33 | 00040000h–0007FFFFh |
| | | : | : | | : | : |
| | | SA543 | 07FC0000h–07FFFFFFh | | SA287 | 03FC0000h–03FFFFFFh |

**注：**
8. 配置：CFR3N[3] = 0，CFR1N[6] = 0，CFR1N[2] = 0。

**表10　　顶部混合配置 32 个 4 KB 扇区和 256 KB 统一扇区地址映射**[9]

| Sector size (KB) | S28HL01GT and S28HS01GT | | | S28HL512T and S28HS512T | | |
|---|---|---|---|---|---|---|
| | Sector count | Sector range | Byte address range (Sector starting ad- dress–sector end- ing address) | Sector count | Sector range | Byte address range (Sector starting ad- dress–sector end- ing address) |
| 256 | 511 | SA00 | 00000000h–0003FFFFh | 255 | SA00 | 00000000h–0003FFFFh |
| | | : | : | | : | : |
| | | SA510 | 07F80000h–07FBFFFFh | | SA254 | 03F80000h–03FBFFFFh |
| 128 | 1 | SA511 | 07FC0000h–07FDFFFFh | 1 | SA255 | 03FC0000h–03FDFFFFh |
| 4 | 32 | SA512 | 07FE0000h–07FE0FFFh | 32 | SA256 | 03FE0000h–03FE0FFFh |
| | | : | : | | : | : |
| | | SA543 | 07FFF000h–07FFFFFFh | | SA287 | 03FFF000h–03FFFFFFh |

**注：**
9. 配置：CFR3N[3] = 0，CFR1N[6] = 0，CFR1N[2] = 1。

**表 11　　混合配置 2 底部十六个和顶部十六个 4 KB 扇区地址映射**[10]

| Sector size (KB) | S28HL01GT and S28HS01GT | | | S28HL512T and S28HS512T | | |
|---|---|---|---|---|---|---|
| | Sector count | Sector range | Byte address range (Sector starting address–sector ending address) | Sector count | Sector range | Byte address range (Sector starting ad- dress–sector ending address) |
| 4 | 16 | SA00 | 00000000h–00000FFFh | 16 | SA00 | 00000000h–00000FFFh |
| | | : | : | | : | : |
| | | SA15 | 0000F000h–0000FFFFh | | SA15 | 0000F000h–0000FFFFh |
| 192 | 1 | SA16 | 00010000h–0003FFFFh | 1 | SA16 | 00010000h–0003FFFFh |
| 256 | 510 | SA17 | 00040000h–0007FFFFh | 254 | SA17 | 00040000h–0007FFFFh |
| | | : | : | | : | : |
| | | SA526 | 07F80000h–07FBFFFFh | | SA270 | 03F80000h–03FBFFFFh |

**注：**
10. 配置：CFR3N[3] = 0，CFR1N[6] = 1。

**表 11　混合配置 2 底部十六个和顶部十六个 4 KB 扇区地址映射**[10]（续）

| Sector size (KB) | S28HL01GT and S28HS01GT | | | S28HL512T and S28HS512T | | |
|---|---|---|---|---|---|---|
| | Sector count | Sector range | Byte address range (Sector starting address–sector ending address) | Sector count | Sector range | Byte address range (Sector starting address–sector ending address) |
| 192 | 1 | SA527 | 07FC0000h–07FEFFFFh | 1 | SA271 | 03FC0000h–03FEFFFFh |
| 4 | 16 | SA528 | 07FF0000h–07FF0FFFh | 16 | SA272 | 03FF0000h–03FF0FFFh |
| | | : | : | | : | : |
| | | SA543 | 07FFF000h–07FFFFFFh | | SA287 | 03FFF000h–03FFFFFFh |

**注：**

10. 配置：CFR3N[3] = 0，CFR1N[6] = 1。

这些是使用几个扇区作为参考的简明表格。有一些地址范围未明确列出。所有 4 KB 扇区地址类型为 xxxxx000h–xxxxxFFFh。所有 256 KB 扇区地址类型为 xxx00000h–xxx3FFFFh、xxx40000h–xxx7FFFFh、xx80000h–xxxCFFFFh 或 xxD0000h–xxxFFFFFh。

## 3.2 ID地址空间

存储器的这个特定区域被分配给制造商、器件和唯一标识：

- 制造商标识由 JEDEC 分配（见**表 94**）。
- 器件标识由 Infineon 分配（见**表 94**）。
- 64 比特位唯一编号位于唯一器件 ID 地址空间的 8 个字节中。此唯一 ID 可用作软件可读的序列号，该序列号对于每个器件都是唯一的（见**表 95**）。

没有为这些 ID 定义地址空间，因为只能通过提供相应的命令传输来读取它们。读取这些ID的传输不需要地址。该地址空间中的数据是只读数据。

## 3.3 JEDEC JESD216 SFDP 空间

SFDP 标准提供了一种一致的方法，在内部参数表的标准设置中描述该串行闪存式存储器装置的功能和特性。主控系统软件可以查询这些参数表，以进行所需的调整，以适应不同的功能。SFDP 地址空间有一个从地址零开始的帧头，用于标识 SFDP 数据结构并为每个参数提供指针。 SFDP 地址空间由英飞凌烧录，对于主控系统是只读的（见**表 90** 至**表 93**）。

**表 12 SFDP 地址映射概述**

| Byte address | Description |
|---|---|
| 0000h | Location zero within JEDEC JESD216D SFDP space - start of SFDP header |
| ,,, | Remainder of SFDP header followed by undefined space |
| 0100h | Start of SFDP parameter tables The SFDP parameter table data starting at 0100h |
| ... | Remainder of SFDP parameter tables followed by either more parameters or undefined space |

## 3.4 SSR 地址空间

每个 HS/L-T 家族存储器器件都有一个 1024 字节的安全存储区域，即OTP地址空间。该地址空间与主闪存式存储器阵列是分开的。SSR 区域分为 32 个可单独锁定、32 字节对齐和长度的区域。

在从零地址开始的 32 字节区域中：

- 最低 16 个字节包含 128 位随机数。该随机数无法写入、擦除或烧录，任何尝试都会返回 PRGERR 标志。
- 接下来的 4 个字节用于为每个安全区域提供一个比特位（总共 32 位），一旦将位设置为“0”，便可永久防止其被写入、擦除或烧录。
- 所有其他字节均被保留。

剩余区域在从英飞凌出厂时会被擦除，并可用于对额外的永久性数据进行编程。

**表 13　　SSR 地址映射**

| Region | Byte address range | Contents | Initial delivery state |
|---|---|---|---|
| Region 0 | 000h | LSB of Infineon programmed random number | Infineon programmed random number |
| | ... | ... | |
| | 00Fh | MSB of Infineon programmed random number | |
| | 010h to 013h | Region locking bits<br>Byte 10h [bit 0] locks region 0 from programming when = 0<br>...<br>Byte 13h [bit 7] locks region 31 from programming when<br>= 0 | All Bytes = FFh |
| | 014h to 01Fh | Reserved for Future Use (RFU) | |
| Region 1 | 020h to 03Fh | Available for User Programming | |
| Region 2 | 040h to 05Fh | | |
| ... | ... | | |
| Region 31 | 3E0h to 3FFh | | |

## 3.5　　寄存器

寄存器是用于配置 HS/L-T 系列存储器器件的运行方式，或报告器件运行的状态的一小组存储单元。寄存器通过特定的指令和地址访问。
表 14 显示该器件中每个可用寄存器的地址映射。

**表 14　　寄存器地址分布**

| Function | Register type | Register name | Volatile component address (hex) | Non-volatile component address (hex) |
|---|---|---|---|---|
| Device status | Status Register 1 | STR1N[7:0], STR1V[7:0] | 0x00800000 | 0x00000000 |
| | Status Register 2 | STR2V[7:0] | 0x00800001 | N/A |
| Device configuration | Configuration Register 1 | CFR1N[7:0], CFR1V[7:0] | 0x00800002 | 0x00000002 |
| | Configuration Register 2 | CFR2N[7:0], CFR2V[7:0] | 0x00800003 | 0x00000003 |
| | Configuration Register 3 | CFR3N[7:0], CFR3V[7:0] | 0x00800004 | 0x00000004 |
| | Configuration Register 4 | CFR4N[7:0], CFR4V[7:0] | 0x00800005 | 0x00000005 |
| | Configuration Register 5 | CFR5N[7:0], CFR5V[7:0] | 0x00800006 | 0x00000006 |
| Interface CRC | Interface CRC Enable Register | ICEV[7:0] | 0x00800008 | N/A |

地址空间映射

**表 14　　寄存器地址映射（续）**

| Function | Register type | Register name | Volatile component address (hex) | Non-volatile component address (hex) |
|---|---|---|---|---|
| Infineon Endurance Flex architecture | Infineon Endurance Flex Architecture Selection Register 0 [1:0] | EFX0O[7:0] | N/A | 0x00000050 |
| | Infineon Endurance Flex Architecture Selection Register 1 [7:0] | EFX1O[7:0] | | 0x00000052 |
| | Infineon Endurance Flex Architecture Selection Register 1 [10:8] | EFX1O[10:8] | | 0x00000053 |
| | Infineon Endurance Flex Architecture Selection Register 2 [7:0] | EFX2O[7:0] | | 0x00000054 |
| | Infineon Endurance Flex Architecture Selection Register 2 [10:8] | EFX2O[10:8] | | 0x00000055 |
| | Infineon Endurance Flex Architecture Selection Register 3 [7:0] | EFX3O[7:0] | | 0x00000056 |
| Infineon Endurance Flex architecture | Infineon Endurance Flex Architecture Selection Register 3 [10:8] | EFX3O[10:8] | N/A | 0x00000057 |
| | Infineon Endurance Flex Architecture Selection Register 4 [7:0] | EFX4O[7:0] | | 0x00000058 |
| | Infineon Endurance Flex Architecture Selection Register 4 [10:8] | EFX4O[10:8] | | 0x00000059 |
| Interrupt pin | Interrupt Configuration Register | INCV[7:0] | 0x00800068 | N/A |
| | Interrupt Status Register | INSV[7:0] | 0x00800067 | |
| Error correction | ECC Status Register | ESCV[7:0] | 0x00800089 | |
| | ECC Error Detection Count Register [7:0] | ECTV[7:0] | 0x0080008A | |
| | ECC Error Detection Count Register [15:8] | ECTV[15:8] | 0x0080008B | |
| | ECC Address Trap Register [7:0] | EATV[7:0] | 0x0080008E | |
| | ECC Address Trap Register [15:8] | EATV[15:8] | 0x0080008F | |
| | ECC Address Trap Register [23:16] | EATV[23:16] | 0x00800040 | |
| | ECC Address Trap Register [31:24] | EATV[31:24] | 0x00800041 | |

地址空间映射

**表 14　　寄存器地址映射（续）**

| Function | Register type | Register name | Volatile component address (hex) | Non-volatile component address (hex) |
|---|---|---|---|---|
| AutoBoot | AutoBoot Register [7:0] | ATBN[7:0] | N/A | 0x00000042 |
| | AutoBoot Register [15:8] | ATBN[15:8] | | 0x00000043 |
| | AutoBoot Register [23:16] | ATBN[23:16] | | 0x00000044 |
| | AutoBoot Register [31:24] | ATBN[31:24] | | 0x00000045 |
| Erase Count | Sector Erase Count Register [7:0] | SECV[7:0] | 0x00800091 | N/A |
| | Sector Erase Count Register [15:8] | SECV[15:8] | 0x00800092 | |
| | Sector Erase Count Register [23:16] | SECV[23:16] | 0x00800093 | |
| Data Integrity Check | Data Integrity Check CRC Register [7:0] | DCRV[7:0] | 0x00800095 | |
| | Data Integrity Check CRC Register [15:8] | DCRV[15:8] | 0x00800096 | |
| | Data Integrity Check CRC Register [23:16] | DCRV[23:16] | 0x00800097 | |
| | Data Integrity Check CRC Register [31:24] | DCRV[31:24] | 0x00800098 | |
| Protection and Security | Advanced Sector Protection Register [7:0] | ASPO[7:0] | N/A | 0x00000030 |
| | Advanced Sector Protection Register [15:8] | ASPO[15:8] | | 0x00000031 |
| | ASP PPB Lock Register (Persistent Protection Block) | PPLV[7:0] | 0x0080009B | N/A |
| | ASP Password Register [7:0] | PWDO[7:0] | N/A | 0x00000020 |
| | ASP Password Register [15:8] | PWDO[15:8] | | 0x00000021 |
| | ASP Password Register [23:16] | PWDO[23:16] | | 0x00000022 |
| | ASP Password Register [31:24] | PWDO[31:24] | | 0x00000023 |
| | ASP Password Register [39:32] | PWDO[39:32] | | 0x00000024 |
| Protection and Security | ASP Password Register [47:40] | PWDO[47:40] | | 0x00000025 |
| | ASP Password Register [55:48] | PWDO[55:48] | | 0x00000026 |
| | ASP Password Register [63:56] | PWDO[63:56] | | 0x00000027 |

# 4 特性

## 4.1 错误检测和纠正

HL-T/HS-T系列设备通过在存储器阵列写入期间生成嵌入式汉明纠错码来支持错误检测和纠正。然后，该 ECC 代码用于读取操作期间的错误检测和纠正。ECC基于 16 字节数据单位。当 16 字节数据单位被加载到写入缓存并传输到 128 比特位队列线进行写入时（在擦除操作之后），每个数据单位的 8 比特位ECC也被写入到主控系统软件不可见的存储器阵列部分中。然后在每次读取操作期间检查此ECC信息。数据单位内的 1 比特位错误将由ECC逻辑纠正。16字节数据单位是启用ECC最小写入颗粒度。

当在 16 字节数据单位中首次编程任意数量的数据时，计算的ECC是整个数据单位的数值。如果随后将附加数据编程到相同的数据单位中，但没有擦除，则该数据单位的ECC被禁用，并且 1 比特的ECC禁用位会被置位。需要扇区擦除操作才能再次对该数据单位启用 ECC 功能。

这些是对用户公开的自动操作。无感的ECC特性增强了向每个数据单位写入一次数据这种典型写入操作的数据可靠性，同时还通过仍然允许单字节写入和比特位遍历（在这种情况下， ECC将被禁用）这种相同的数据单位被多次写入的方式来提升与前几代产品的软件兼容性。

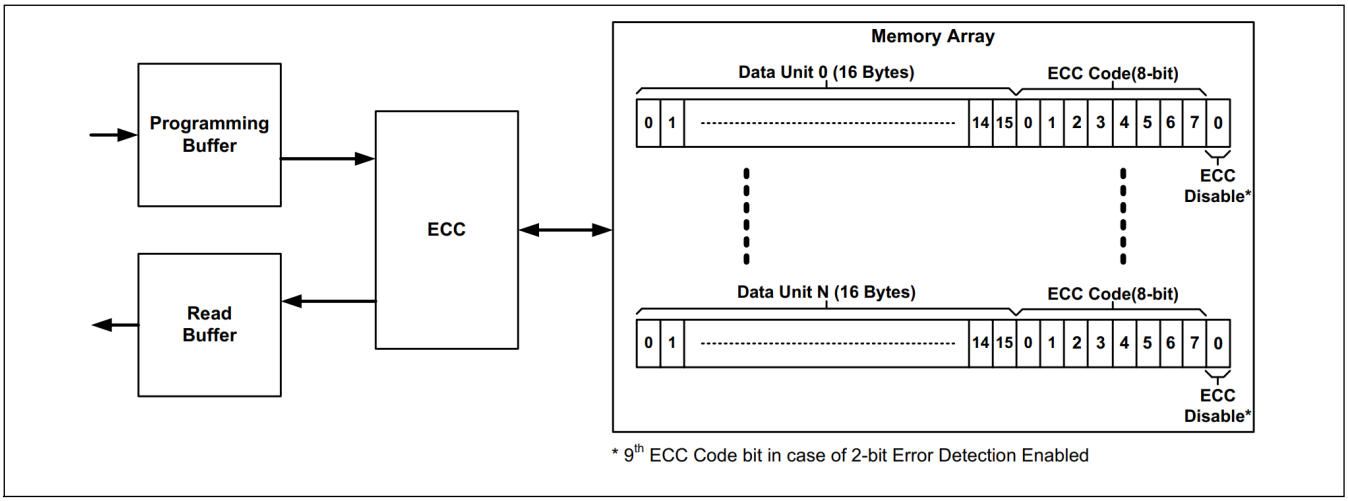


**图 33 16 字节ECC数据单位示例**

SEMPER™ NOR 闪存默认ECC配置为支持 2 比特位错误检测。在此配置中，任何数据单位中的 1 比特位错误得到纠正，并且任何 2比特位错误都被检测并报告。 16 字节单位数据需要 9 比特位纠错码以进行 2 比特位错误检测。 当启用 2 比特位错误检测时，不允许对同一数据单元（无擦除）进行字节写入、比特位遍历或多次写入操作，这将导致写入错误。 将 ECC 模式从 1 比特位错误检测更改为 2 比特位错误检测，或从 2 比特位错误检测更改为 1 比特位错误检测将使内存阵列中的所有数据无效。当改变ECC模式时，主控必须先将器件中的所有扇区内的数据擦除。如果在未擦除已写入数据的情况下更改 ECC 模式，则后续读取操作将导致未定义的行为。

### 4.1.1 ECC错误报告

当检测到ECC错误时，有五种方法可以向主控系统报告。

- ECC数据单位状态提供数据单位中 1 比特位或 2 比特位错误的状态。
- ECC状态寄存器提供自上次ECC清零或复位以来1比特位或2比特位错误的状态。
- ECC地址捕获寄存器捕获在POR或复位后遇到的存储器阵列读取期间第一个ECC错误的地址位置。
- ECC 错误检测计数器会记录读取过程中数据单位中发生的 1 比特位或 2 比特位错误的数量。
- 中断（INT#）输出可以启用，以指示在读取数据时检测到 1 位或 2 位错误。

#### 4.1.1.1 ECC数据单状态 (EDUS)

- 每个数据单位中的ECC状态由8比特位ECC数据单位状态提供。
- ECC状态传输输出所寻址的数据单位的ECC状态。 ECC数据单位状态的内容则指示对于所选择的数据单位，是否存在已纠正的1比特位错误、检测到的2比特位错误、或针对该数据单位的ECC是否已经被禁用。

**表 15 ECC数据单位状态**

| Bits | Field name | Function | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| EDUS[7:4] | RESRVD | Reserved For Future Use | V => R | 0000 | These bits are Reserved for future use. |
| EDUS[3] | ECC2BD | ECC Error 2-bit Error Detection Flag | V => R | 0 | This bit indicates whether a two bit error is detected in the data unit, if two bit ECC error detection is enabled CFR4V[3] = 1. When CFR4V[3] = 0 and 2-bit error detection is disabled, ECC2BD bit will always be ‘0’.<br>**Note:** If 2 bit error detection is enabled (CFR4V[3] = 1), the ECCOFF bit will not be set to 1b while performing single byte programming or bit walking in a data unit that was already partially programmed. An attempt to do such byte programming or bit walking will result in a Program Error.<br><br>Selection Options:<br>1 = Two Bit Error detected<br>0 = No error |
| EDUS[2] | RESRVD | Reserved For Future Use | V => R | 0 | This bit is Reserved for future use. |

表 15 ECC数据单位状态（续）

| Bits | Field name | Function | Read/Write N = Non-volatile V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| EDUS[1] | ECC1BC | ECC Error 1-bit Error Detection and Correction Flag | V => R | 0 | This bit indicates whether an error was corrected in the data unit.<br><br>Selection Options:<br>1 = Single Bit Error corrected in the addressed data unit<br>0 = No single bit error was corrected in the addressed data unit |
| EDUS[0] | ECCOFF | Data Unit ECC Off/On Flag | V => R | 0 | This bit indicates whether the ECC syndrome is off in the data unit.<br><br>Selection Options:<br>1 = ECC is OFFin the selected data unit<br>0 = ECC is ON in the selected data unit<br><br>Dependency: CFR4x[3] |

### 4.1.1.2 ECC 状态寄存器 (ECSV)

- 8 比特位ECC状态寄存器提供自上次ECC清零或复位后正常读取期间 1 比特位或 2 比特位错误的状态。ECC 状态寄存器没有用户可编程的非易失性比特位，所有定义的比特位都是易失性的只读比特位。这些位的默认状态是由硬件置位的。
- 可以通过 Read Any Register 命令来访问 ECC 状态寄存器。基于 Read Any Register 的 ECSV 的正确序列读取如下：
  - 使用任意读取操作从内存阵列读取数据
  - ECSV 由器件更新
  - ECSV 通过 Read Any Register 命令提供自上次清零、复位或复位以来任何ECC事件的状态。
- ECSV 通过POR 、 JEDEC串行闪存器件复位信号协议、硬件/软件复位或清除ECC状态复位操作来清除。

### 4.1.1.3 ECC 错误地址捕获 (EATV)

- 一个 32 比特位寄存器用于在读取闪存式存储器阵列单元期间首先遇到ECC错误时来捕获相应ECC数据单位地址。仅在POR 、硬件复位或ECC清零、复位传输后遇到的第一个使能的ECC错误类型（“仅 2 比特位”或“1 比特位或 2比特位”，取决于 CFR4N[3] 中选择）时的地址。EATV 寄存器仅在读取传输期间更新。

  EATV 寄存器包含检测到错误时访问的地址。故障位可能并不位于寄存器中指示的当前地址，而是位于检测到错误所在的对齐 16 字节ECC数据单位内。如果在单次读取操作期间在多个ECC数据单位中发现错误，则仅在 EATV 寄存器中捕获第一个失败的ECC单位的地址。

  当2比特位错误检测未启用且同一ECC单位被写入多次时，该ECC单位的ECC错误检测被禁用，因此无法识别错误并捕获该地址。

  当ECC状态寄存器 (ECSV) 比特位 3 或 4 = 1 时，地址捕获寄存器具有有效地址。
- 可以使用 Read Any Register 命令来读取地址捕获寄存器。
- 清除ECC状态寄存器传输、POR或JEDEC信号协议/硬件/软件复位会清除地址捕获寄存器。

### 4.1.1.4 ECC错误检测计数器（ECTV）

- 一个16位寄存器用于计数从闪存阵列读取数据时发生的1比特位或2比特位错误的数量。只有在主阵列中识别的错误才会导致错误检测计数器递增。ECTV 寄存器仅在读取传输期间更新。读取 ECC 状态传输不会影响 ECTV 寄存器。

  16 比特位错误检测计数器将不会递增超过 FFFFh。然而，ECC 仍在继续发挥作用。

  请注意在连续读取操作期间，当检测到 1 比特位或 2 比特位错误时，时钟可能会继续切换，并且存储器器件将继续增加数据地址并将新数据放置在 DQ 信号上；遇到的任何带有错误的额外数据单元都将被计数，直到 CS# 恢复为高电平。

  在读取命令传输期间，对于发现错误的每个数据单位，仅计为一个错误。每个读取传输将导致目标数据单位的新读取。如果多个读取命令传输访问包含错误的相同数据单位，则每次读取该数据单位时，错误计数器将递增。

  当 2 比特位错误检测未启用且同一数据单位被写入多次时，该数据单位的ECC错误检测将被禁用，因此无法识别或计数错误。

- 可以使用 Read Any Register 命令来读取 ECC 错误检测计数器寄存器。

- ECTV 寄存器在POR、JEDEC信号协议/硬件/软件复位或者使用清除ECC状态寄存器时置位为 0。

### 4.1.1.5 INT# 输出

- HL-T/HS-T 支持 INT# 输出引脚，以向主控系统指示中断/快闪式存储器器件内发生了事件。用户可以将 INT# 输出引脚配置为在以下情况下转换为有源（低电平）状态：
  - 检测到 2 位 ECC 错误
  - 检测到 1 位 ECC 错误
  - 从忙碌状态转换到就绪状态

  INT# 引脚仅在 BGA 封装中可用。操作由中断配置寄存器 (INCV) 控制，其中 INT# 输出（通常为高电平）是使能的。中断配置寄存器确定内部事件何时使能，以触发 INT# 输出引脚上的高电平到低电平转变。

  中断状态寄存器 (INSV) 指示自上次清除 INSV 以来发生的已使能的内部事件。

  如果使能，则 INT# 输出引脚将在发生使能事件时从高电平转换为低电平。一旦主控识别出 INT# 已转换为低电平状态，就可以读取 INSV 寄存器来确定哪个内部事件导致了该事件。POR、硬件复位、软件复位、DPD 退出或 CS# 信号复位期间的 INT# 输出状态无效。

- 可以通过SPI和八线接口的“Read Any Register”命令序列访问 INCV 和 INSV。通过 Write Any Register 命令序列向 INCV 写入仅在八线接口中受支持。

- 可以使用以下方法强制 INT# 输出转换回高电平（通过外部上拉电阻返回高电平）：
  - 通过将 1 加载到中断配置寄存器的位 7 中，来关闭 INT# 输出。
  - 在 INSV 位置位中重置适当的位置（通过写入 1），以指示发生哪个内部事件导致输出变为低电平。在 INT# 输出返回高电平之前，INSV 中所有低电平且启用的 INSV 位必须被复位。
  - 通过 CS# 信号复位、硬件复位（RESET# = 低电平）或POR，INT# 输出也将返回到默认（禁用、高阻）状态。通过设置中断配置寄存器为默认（所有中断禁用）状态来使硬件复位和POR禁止所有中断生效。
  - ECC 事件后清除 ECC 状态寄存器会强制 INT# 输出进入高电平状态。

### 4.1.2 ECC 相关寄存器和命令传输

**表16 ECC相关寄存器和命令传输**

| Related registers | Related SPI transactions (see Table 81) | Related octal transactions (see Table 82) |
|---|---|---|
| Configuration Register - 4 (CFR4N, CFR4V) (see Table 58) | Read Any Register (RDARG_C_0) | Read Any Register (RDARG_4_0) |
| ECC Status Register (ECSV) (see Table 64) | Write Enable (WRENB_0_0) | Write Enable (WRENB_0_0) |
| ECC Address Trap Register (EATV) (see Table 65) | Write Any Register (WRARG_C_1) | Write Any Register (WRARG_4_1) |
| ECC Error Detection Counter Register (ECTV) (see Table 66) | Read ECC Status (RDECC_4_0) | Read ECC Status (RDECC_4_0) |
| Interrupt Configuration Register (INCV) (see Table 74) | Clear ECC Status Register (CLECC_0_0) | Clear ECC Status Register (CLECC_0_0) |
| Interrupt Status Register (INSV) (see Table 75) | – | – |

## 4.2 英飞凌 Endurance Flex 架构（负载均衡）

英飞凌 Endurance Flex 架构允许将主存储器阵列划分为可配置成高耐久性或长数据保留时间的区域。英飞凌 Endurance Flex 架构在高耐久性区域实现负载均衡，其中写入/擦除周期均匀分布在负载均衡池的所有扇区中。通过避免单个扇区的过早磨损，这极大地提高了器件的可靠性。

从架构上看，英飞凌 Endurance Flex 架构的负载均衡算法基于逻辑扇区到物理扇区的映射。在部件的使用寿命周期内，此映射会发生改变，以保持所有物理扇区的写入/擦除周期的均匀分布。逻辑到物理的映射信息存储在专用的闪存式存储器阵列中，该阵列在交换扇区时更新。当擦除操作时，会发生扇区交换。

英飞凌 Endurance Flex 架构的高耐久性区域要求至少设置 20 个扇区。为了在配置长数据保留时间、高耐久性或两个区域之间提供灵活性，提供了四个指针边界架构。出厂默认设置将所有扇区指定为高耐久性，作为负载均衡池的一部分，并且所有指针边界均被禁用。这四个指针边界最多可用于划分成五个区域，每个区域均可配置为长数据保留时间或高耐久性。

图 34 概述了 Endurance Flex 架构。它展示了基于不同扇区架构的五个可能区域。

**注释：**4KB 扇区不属于英飞凌 Endurance Flex 架构的一部分。

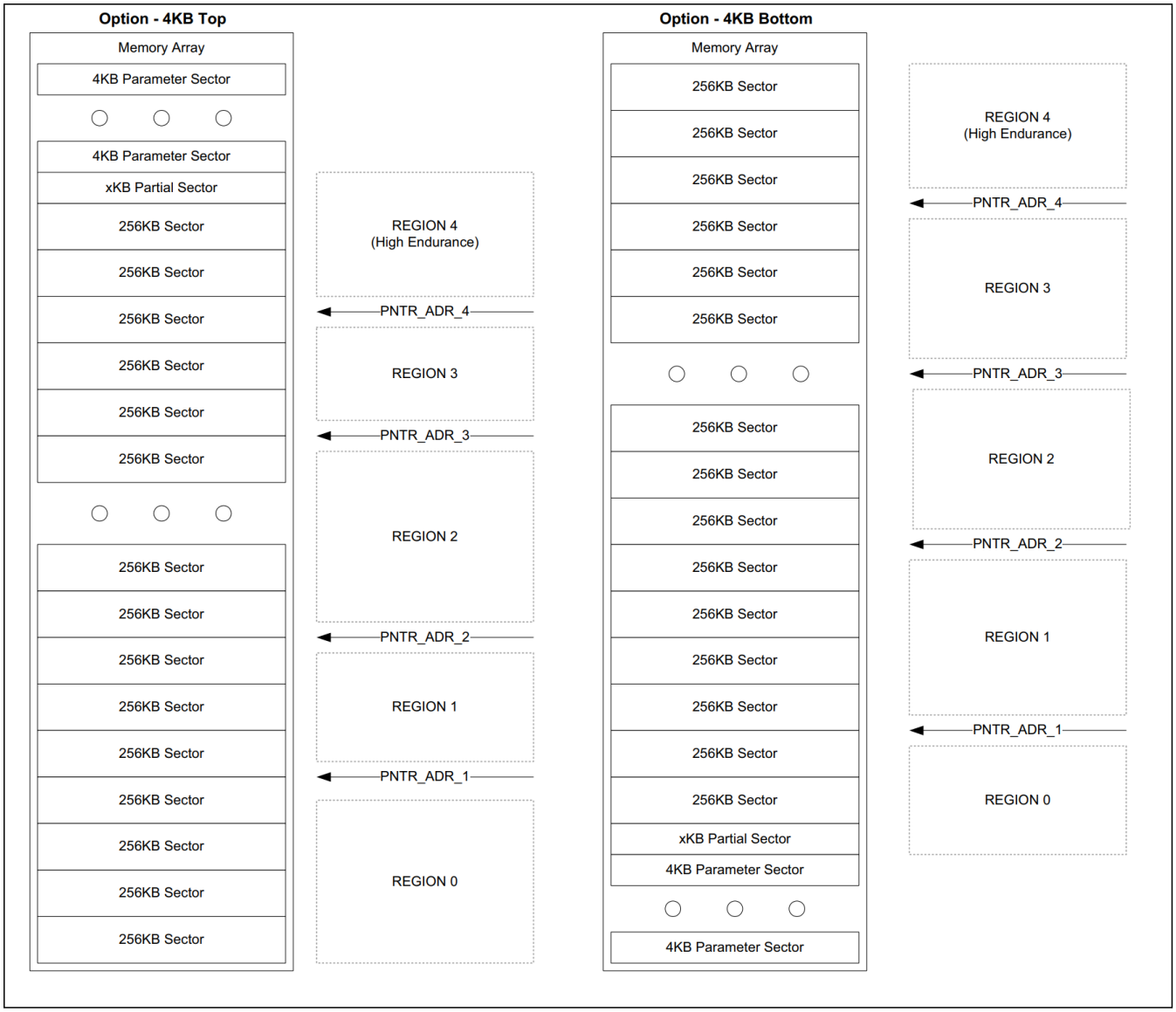


**图 34　　Endurance Flex 架构概述**

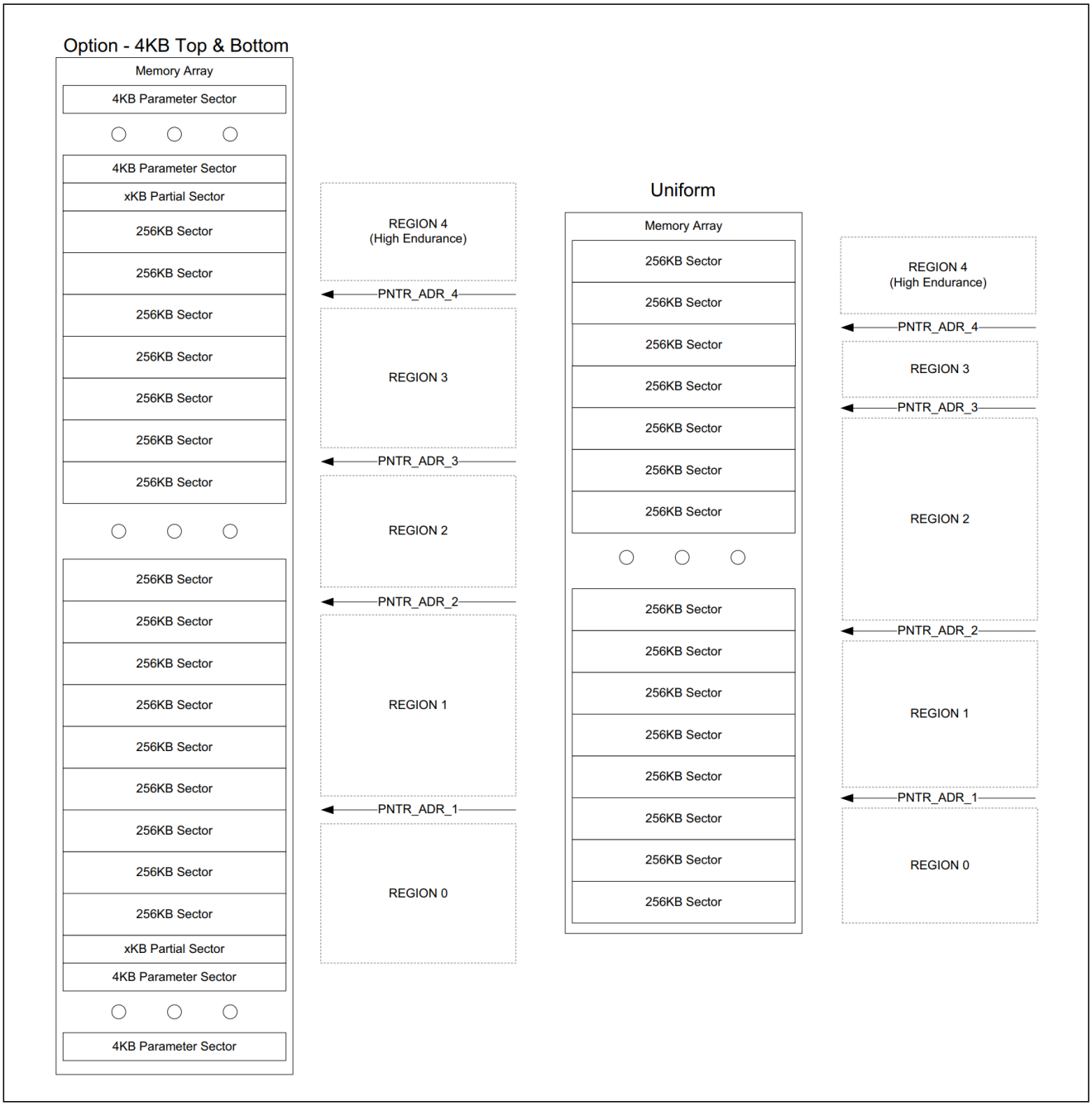


**图 35　　Endurance Flex 架构概述（续）**

**表 17　区域定义**[11, 12, 13, 14]

| Region | Lower limit | Upper limit |
|---|---|---|
| 0 | Sector 0 | Address Pointer 1 |
| 1 | Address Pointer 1 | Address Pointer 2 |
| 2 | Address Pointer 2 | Address Pointer 3 |
| 3 | Address Pointer 3 | Address Pointer 4 |
| 4 | Address Pointer 4 | Highest Sector |

**注释：**

11. 指针边界地址必须遵循以下规则：
    指针#4 地址>指针#3 地址
    指针#3 地址>指针#2 地址
    指针#2 地址>指针#1 地址
12. 4KB 扇区被排除在外。
13. 要求在客户首次为器件上电时配置高数据耐久性和长数据保留时间区域。一旦配置完成，就不能再更改。
14. 任何高耐久性区域的最少为 20 个扇区。

### 4.2.1　配置 1：最大耐久性 - 单一高耐久性区域

当所有 256 KB 扇区均指定为高耐久性时，可实现最大耐久性。使用 Endurance Flex 架构指针边界将所有扇区指定为高耐久性。最大耐久性指针边界配置如表18所示。

**表 18　最大耐久性配置的 Endurance Flex 指针值**[15]

| Pointer # | Pointer address EPTADn[8:0] | Region type ERGNTn | Pointer enable# EPTEBn | Global region selection GBLSEL | Wear leveling enable WRLVEN |
|---|---|---|---|---|---|
| 0 | N/A | N/A | N/A | 1’b1 | 1’b1 |
| 1 | 9'b111111111 | 1’b1 | 1’b1 | N/A | N/A |
| 2 | 9'b111111111 | | | | |
| 3 | 9'b111111111 | | | | |
| 4 | 9'b111111111 | | | | |

**注释：**

15. 这也是该器件的默认配置。

### 4.2.2　配置 2：两个区域选择 - 一个长数据保留时间区域和一个高耐久性区域

使用 Endurance Flex 架构指针边界来划分长数据保留时间或高耐久性扇区。区域 0 定义为长数据保留，由 16 个扇区组成。区域 1 定义为高耐久性，有 240 个扇区。表 19显示了两个区域配置的指针边界设置。定义的指针数量基于配置的区域数量。

**表 19　英飞凌 Endurance Flex 架构指针边界值（双区域配置）**

| Pointer # | Pointer address EPTADn[8:0] | Region type ERGNTn | Pointer enable# EPTEBn | Global region selection GBLSEL | Wear leveling enable WRLVEN |
|---|---|---|---|---|---|
| 0 | N/A | N/A | N/A | 1’b0 | 1’b1 |
| 1 | 9’b000010000 | 1’b1 | 1'b0 | N/A | N/A |
| 2 | 9’b111111111 | 1’b1 | 1'b1 | | |
| 3 | | | | | |
| 4 | | | | | |

### 4.2.3 Endurance Flex 相关寄存器及命令传输

**表 20 Endurance Flex 相关寄存器和命令传输**

| Related registers | Related SPI transactions (see Table 81) | Related octal transactions (see Table 82) |
|---|---|---|
| Endurance Flex architecture Selection Registers (EFX4O, EFX3O, EFX2O, EFX1O, EFX0O) (see **"Endurance Flex Architecture Selection Register (EFXx)"** on page 116) | Read Any Register (RDARG_C_0) | Read Any Register (RDARG_4_0) |
| | Write Any Register (WRARG_C_1) | Write Any Register (WRARG_4_1) |

## 4.3 接口 CRC

接口CRC对主控与器件之间的通讯进行硬件加速CRC计算，保证传输信息的完整性。CRC（循环冗余校验）是一种错误检测码，常用于设备检测原始数据的意外更改。接口 CRC（循环冗余校验）保护是一个配置选项（ICEV[0] - ITCRCE）。

HL-T/HS-T家族设备中的接口CRC（循环冗余校验）方法完全依赖于主控来验证CRC（循环冗余校验）校验值并采取适当的操作。 器件计算CRC（循环校验）校验值正是主控使用读取接口 CRC（循环校验）命令序列（RDCRC_4_0）来读取的。 计算出的校验值包括CS#为低电平时的所有命令传输内容，即命令、地址和数据。 这种 CRC（循环冗余校验）的校验和可以在单个或一系列的命令传输集合中生成。唯一的限制是，从机计算的数据大小CRC（循环校验）校验和必须小于 $2^{32}$位。

主控还必须在同一命令传输序列上计算 CRC（循环冗余校验）校验值。准备就绪后，主控可以读取器件计算出的 CRC（循环冗余校验）校验值，并将其与自身进行比较。如果不匹配，主控可以选择重复完整的命令传输序列。

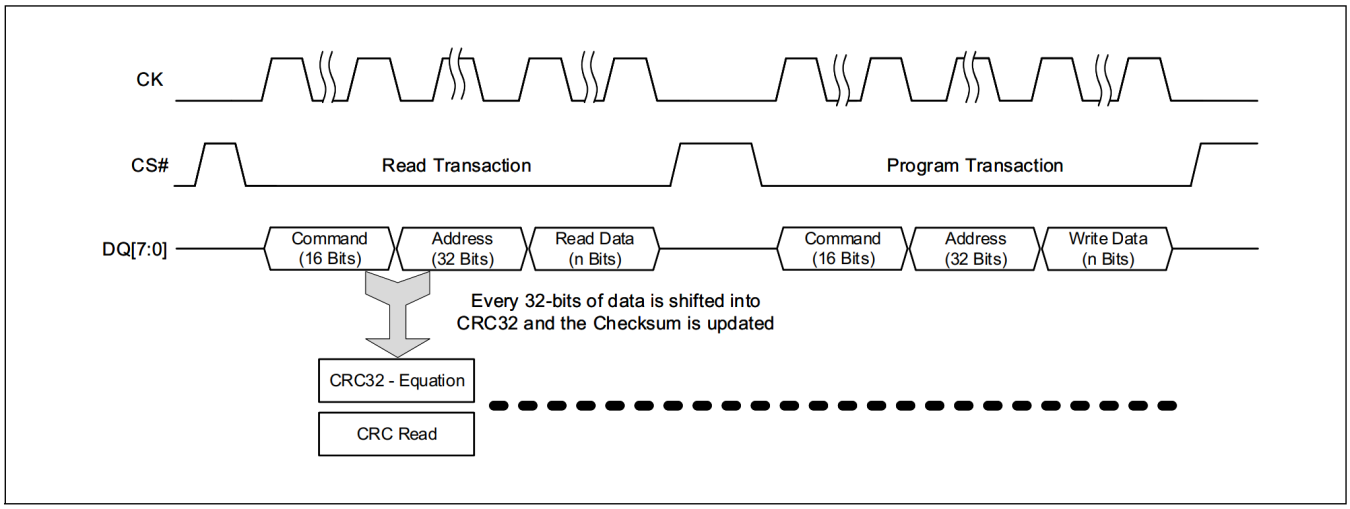


**图 36 CRC（循环冗余校验）计算概述**

**注释**

- 在 CRC 读取命令序列结束时，设备会重置 CRC 校验值并重新初始化 CRC 校验特征多项式。
  - CRC32 多项式: $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^{9} + X^{8} + X^{6} + 1$
- 主控和器件之间的CRC（循环冗余校验）的特征多项式必须相同。
- 接口 CRC（循环冗余校验）仅支持八线 DDR 协议。

- 在以下条件下，接口 CRC（循环冗余校验）校验值将重置为 0xFFFFFFFFh：
  - POR
  - 硬件复位
  - 软件复位
  - CS#信号复位
  - 读取接口 CRC（循环冗余校验）校验值
- 从深度掉电退出

**注释**

- 如果在合法接收指令之前中止命令传输，即通过提前取消 CS# 触发来缩短传输长度 - 传输的数据仍将被计入 CRC（循环冗余校验）校验值，但不再得到保证。当使用接口 CRC（循环冗余校验）时，只能使用有效的、非中止的命令传输。
- 要求在读取任何易失性状态寄存器之前读取接口 CRC（循环冗余校验）值，并在读取任何易失性状态寄存器后清零，清除接口 CRC（循环冗余校验）值。
- 当接口 CRC（循环冗余校验）被禁用时，接口 CRC（循环冗余校验）寄存器值变得不确定。建议在禁用接口 CRC 功能之前读取接口 CRC 寄存器，并在使能接口 CRC 功能后再次读取接口 CRC 寄存器，以重新初始化 CRC 计算。

### 4.3.1 读取

当主控指定READ事务且CS为低电平时，执行读操作。然后，该器件根据地址从内存中提供数据。可以将任意数量的字节读取（并发读取）到连续地址，而无需发出新的读取命令传输。

对于命令传输保护，器件使用 CRC32 特征多项式对整个命令传输序列（CS# 低电平状态）执行 CRC（循环冗余校验）。一旦 CS# 变为高电平，CRC（循环冗余校验）计算就会停止，并将校验值锁存到 CRC（循环冗余校验）寄存器中。如果主控执行多个读取命令传输，器件会在每个 CS# 低电平周期之间继续更新 CRC（循环冗余校验）校验值。

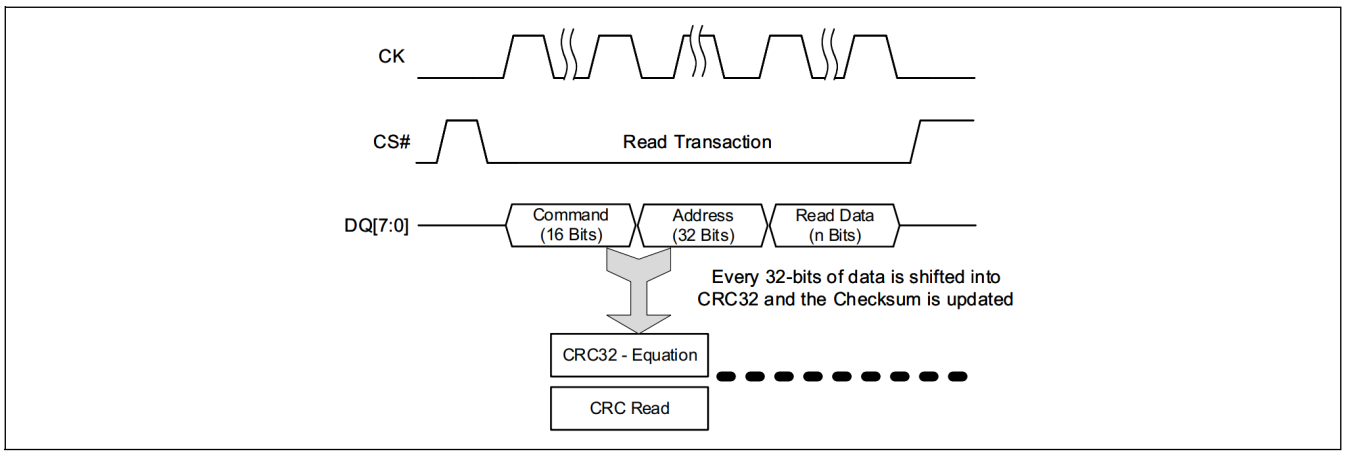


**图 37 读CRC（循环冗余校验）保护**

**注释：**背对背接口 CRC（循环冗余校验）读取事务不会显示 CRC（循环校验）校验和值正在被重置。在每个读取接口 CRC（循环冗余校验）寄存器命令传输结束时，接口 CRC（循环冗余校验）寄存器将在至少三个时钟周期内获得具有有效输入数据的命令传输后进行复位并使用新的 CRC（循环冗余校验）校验和值更新自身。

### 4.3.2 写入/擦除

当 CS# 为低电平时，主控指定一个程序事务，则执行写入操作。最多可将 256 字节/512 字节写入（并发写入）连续地址，而无需发出新的写入命令传输。当主控指定了擦除命令传输，而CS# 处于低电平时，则执行擦除操作。可以擦除单个扇区或整个器件。

为了进行命令传输保护，从设备将使用建议的 CRC32 特征多项式对整个指令序列（CS# 低电平状态）执行 CRC（循环冗余校验）。一旦 CS# 变为高电平以完成写入/擦除命令传输，CRC（循环冗余校验）计算将停止，并将校验和锁存到 CRC（循环冗余校验）寄存器中。如果主控执行多次写入/擦除命令传输，则从机将在每个 CS# 低电平周期之间继续更新 CRC（循环冗余校验）校验和。

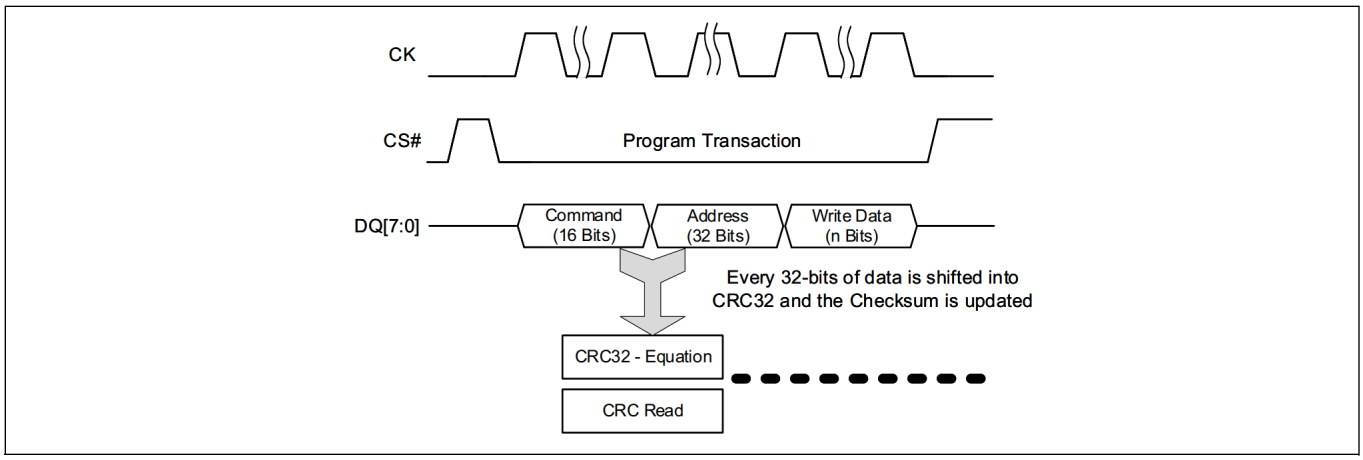


**图38 写入 CRC（循环校验校验）保护**

主控器件将使用读取接口 CRC（循环冗余校验）命令传输从从设备读取 CRC（循环冗余校验）校验和。从设备将包含 RDCRC_4_0 命令传输作为 CRC（循环冗余校验）校验和的一部分，然后将校验和数据放置在数据总线上。如果主控设备在收到从机的CRC校验和后发现与自己计算的CRC校验不匹配，则可以向从设备重新发出写入/擦除命令传输。对于闪存式存储器，由于CRC（循环冗余校验）校验和错误，多次编程/擦除到同一位置会影响数据耐久性。图 39 展示了该问题的解决方案。

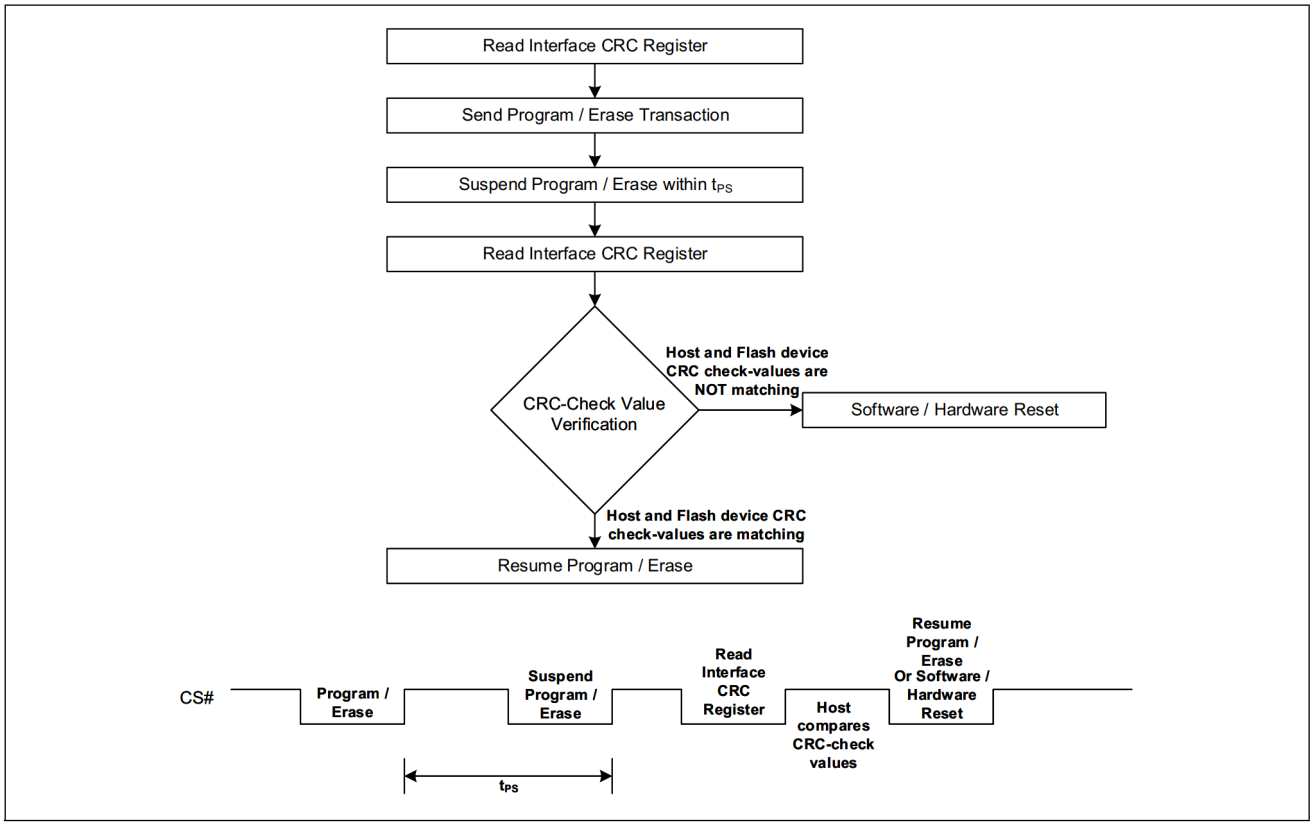


**图 39　　写入和擦除命令传输的接口 CRC（循环冗余校验）流程**

## 4.3.3　接口 CRC（循环校验）相关寄存器和命令传输

**表 21　　接口 CRC（循环校验）相关寄存器和命令传输**

| Related registers | Related SPI transactions (see Table 81) | Related octal transactions (see Table 82) |
|---|---|---|
| Interface CRC Enable Register (ICEV) (see Table 61) | N/A | Read Interface CRC Register (RDCRC_4_0) |

## 4.4 数据完整性 CRC（循环冗余校验）

HL-T/HS-T系列设备具有一组命令，用于在内存阵列中用户定义的地址范围上执行硬件加速的循环冗余校验（CRC）计算。CRC计算是另一种类似于写入或擦除的嵌入式操作，其在计算进行时器件处于繁忙状态。CRC（循环冗余校验）操作使用与接口 CRC（循环冗余校验）相同的 CRC32 特征多项式来确定 CRC（循环校验）校验值。

CRC32 多项式: $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^{9} + X^{8} + X^{6} + 1$

通过输入DICHK_4_1命令传输来启动校验值生成序列。该命令包括将起始地址加载到 CRC（循环冗余校验）开始地址寄存器中，该寄存器标识将由 CRC（循环冗余校验）计算覆盖的地址范围的开始。该命令还包括将结束地址加载到 CRC（循环冗余校验）结束地址寄存器中。将 CS# 拉高会启动 CRC（循环冗余校验）计算。CRC（循环校验）过程计算起始地址到结束地址中包含的数据的校验值。

在计算期间，器件进入忙碌状态 (STR1V[0] - RDYBSY = 1)。校验值计算完成后，器件将返回到空闲状态 (STR1V[0] - RDYBSY = 0)，并且可以读取计算出的校验值。校验值存储在数据完整性 CRC 寄存器 (DCRV[31:0]) 中，并且可以使用 Read Any Register (RDARG_C_0) 命令来读取。

仅当器件处于空闲状态时，才能启动校验值计算；并且一旦启动，就可以用 CRC 暂停命令（SPEPD_0_0）从存储器阵列读取数据。在暂停状态期间，状态寄存器 2 中的 CRC 暂停状态位将会置位 (STR2V[4] - DICRCS = 1)。一旦暂停，主控可以读取状态寄存器，从队列中读取数据，并可以通过CRC 恢复命令（RSEPD_0_0）来恢复CRC（循环冗余校验）计算。

结束地址 (ENDADD) 必须至少比起始地址 (STRADD) 高 4 个地址。如果 ENDADD < STRADD + 3，则检查值计算将中止/退出，器件将返回到就绪状态 (STR1V[0] - RDYBSY = 0)。数据完整性 CRC（循环冗余校验） 中止/退出状态位将会置位 (STR2V[3] - DICRCA = 1) 来指示中止条件。一旦置位，DICRCA 位可以通过软件复位或有效的后续 CRC（循环冗余校验）指令执行来清除。如果 ENDADD < STRADD + 3，则校验值将保留不确定的数据。

**注释：**CRC（循环冗余校验）校验值计算期间的任何无效命令传输都可能损坏校验值数据。

### 4.4.1 数据完整性检查相关寄存器和命令传输

**表 22 数据完整性 CRC（循环冗余校验）相关寄存器和命令传输**

| Related registers | Related SPI transactions (see Table 81) | Related octal transactions (see Table 82) |
|---|---|---|
| Status Register 1 (STR1N, STR1V) (see Table 47) | Data Integrity Check (DICHK_4_1) | Data Integrity Check (DICHK_4_1) |
| Status Register 2 (STR2V) (see Table 50) | Suspend Erase/Program/Data Integrity Check (SPEPD_0_0) | Suspend Erase/Program/Data Integrity Check (SPEPD_0_0) |
| Data Integrity CRC Check-Value Register (DCRV) (see Table 63) | Resume Erase/Program/ Data Integrity Check (RSEPD_0_0) | Resume Erase/Program/ Data Integrity Check (RSEPD_0_0) |

## 4.5 数据保护机制

数据保护用于防止对存储的数据和器件配置进行意外更改。这包括无意擦除或写入存储阵列以及写入配置寄存器，这些都可能改变器件的功能。本文将会介绍三种类型的保护机制，包括保护单个或一组扇区、保护部分或整个内存阵列。

图 40 显示不同保护机制以及适用数据区域的概述。

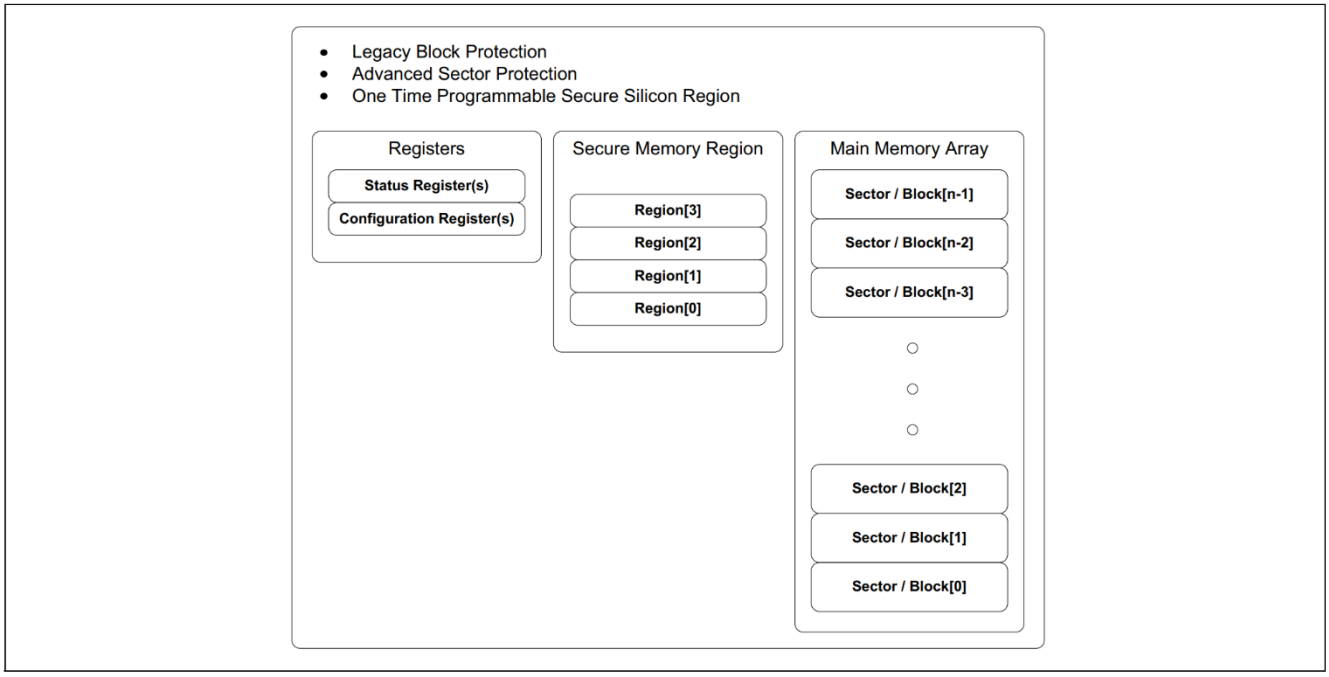


**图 40 数据保护和安全（写入/编程/擦除）机制**

### 4.5.1 传统块保护 (LBP)

传统块保护（LBP）是基于功能块的数据保护机制。LBP 支持与传统串行 NOR 闪存设备的兼容性。LBP通过保护状态寄存器和配置寄存器为存储器阵列和器件配置中的数据提供保护。

#### 4.5.1.1 存储阵列保护

存储器阵列的保护是通过功能块大小选择来实现的，这是通过状态寄存器 1 (STR1N[4:2]/STR1V[4:2] - LBPROT[2:0]) 和配置寄存器 1 (CFR1N[5]/CFR1V[5] - TBPROT) 中存在的位的组合来实现的。**表23** 提供LBP内存阵列功能块选择汇总。

**表 23 传统块存储阵列保护选择**

| CFR1N[5]/ CFR1V[5] TBPROT | STR1N[4]/ STR1V[4] LBPROT[2] | STR1N[3]/ STR1V[3] LBPROT[1] | STR1N[2]/ STR1V[2] LBPROT[0] | Memory array block size | 512 Mb (KBs) | 1 Mb (KBs) |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | None | 0 | 0 |
| 0 | 0 | 0 | 1 | Upper 64th | 1024 | 2048 |
| 0 | 0 | 1 | 0 | Upper 32nd | 2048 | 4096 |
| 0 | 0 | 1 | 1 | Upper 16th | 4096 | 8192 |
| 0 | 1 | 0 | 0 | Upper 8th | 8192 | 16384 |
| 0 | 1 | 0 | 1 | Upper 4th | 16384 | 32768 |
| 0 | 1 | 1 | 0 | Upper Half | 32768 | 65536 |
| 0 | 1 | 1 | 1 | All sectors | 65536 | 131072 |
| 1 | 0 | 0 | 0 | None | 0 | 0 |
| 1 | 0 | 0 | 1 | Lower 64th | 1024 | 2048 |
| 1 | 0 | 1 | 0 | Lower 32nd | 2048 | 4096 |
| 1 | 0 | 1 | 1 | Lower 16th | 4096 | 8192 |
| 1 | 1 | 0 | 0 | Lower 8th | 8192 | 16384 |
| 1 | 1 | 0 | 1 | Lower 4th | 16384 | 32768 |
| 1 | 1 | 1 | 0 | Lower Half | 32768 | 65536 |
| 1 | 1 | 1 | 1 | All sectors | 65536 | 131072 |

### 4.5.1.2 配置保护

LBP 在配置寄存器 1 （CFR1N[4,0]/CFR1V[4,0] - PLPROT、TLPROT）中具有选择位，可以永久或暂时保护状态和配置寄存器，从而再次保护器件的配置。临时保护在下一个掉电或硬件复位或CS#复位信号之前保持有效。

**表 24 选项 2 - 传统块配置保护选择**[16]

| CFR1N[4] / CFR1V[4] PLPROT | CFR1N[0] / CFR1V[0] TLPROT | Register protection status |
|---|---|---|
| 0 | 0 | Status and Configuration registers are unprotected |
| 1 | X | Status and Configuration registers are permanently protected (TBPROT, LBPROT[2:0], SP4KBS, TB4KBS) |
| 0 | 1 | Status and Configuration registers are Protected till next Power down (TBPROT, LBPROT[2:0], SP4KBS, TB4KBS) |

**注释：**

16.保护配置也会保护已被选择保护的存储阵列块。

### 4.5.1.3 传统块保护流程图

LBP保护机制流程图如图 41。

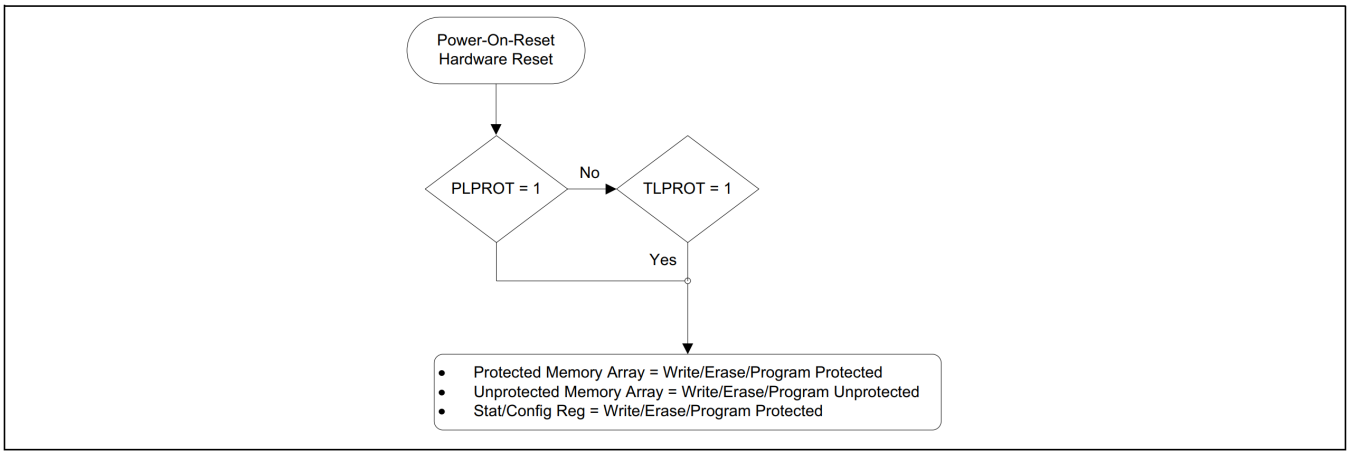


**图 41 传统块保护流程图**

### 4.5.1.4 LBP 相关寄存器和命令传输

**表 25 LBP相关寄存器和命令传输**

| Related registers | Related SPI transactions (see Table 81) | Related octal transactions (see Table 82) |
|---|---|---|
| Status Register 1 (STR1N, STR1V) (see Table 47) | Read Any Register (RDARG_C_0) | Read Any Register (RDARG_4_0) |
| Configuration Register 1 (CFR1N, CFR1V) (see Table 51) | Write Any Register (WRARG_C_1) | Write Any Register (WRARG_4_1) |
| | Read Status Register 1 (RDSR1_0_0) | Read Status Register 1 (RDSR1_4_0) |
| | Write Enable (WRENB_0_0) | Write Enable (WRENB_0_0) |

### 4.5.2 高级扇区保护（ASP）

高级扇区保护 (ASP) 机制允许每个存储器阵列扇区通过易失性或非易失性锁定功能进行独立控制，以防止擦除或写入。非易失性锁定配置也可以被锁定，也可以受密码保护。

主存储器阵列扇区通过多对易失性 ( DYB ) 和非易失性 (PPB) 保护位来防止擦除和写入。每个DYB /PPB 位对都可以单独置位为“0”以保护相关扇区，或清除为“1”以取消保护相关扇区。DYB 保护位可以根据需要随时置位和清除，而 PPB 位是非易失的，必须遵守各自工艺的耐久性要求。**图 42** 显示了 ASP 的概述。

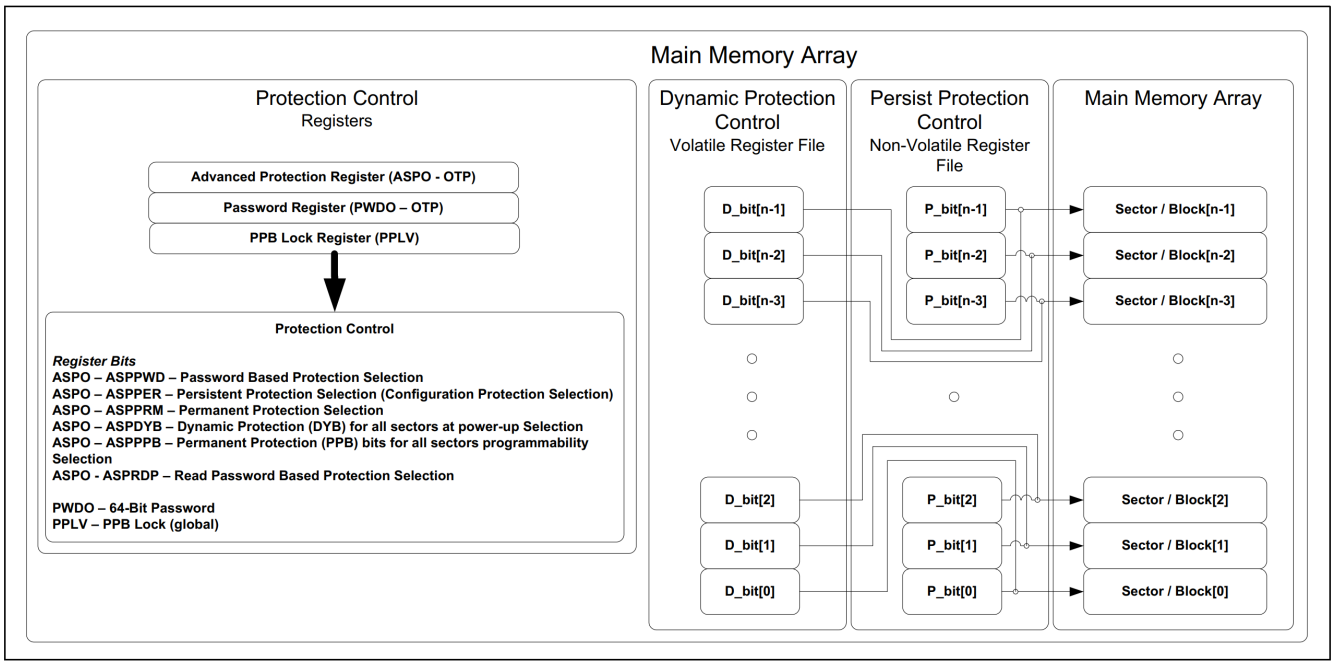


**图 42 高级扇区保护（非易失性）**

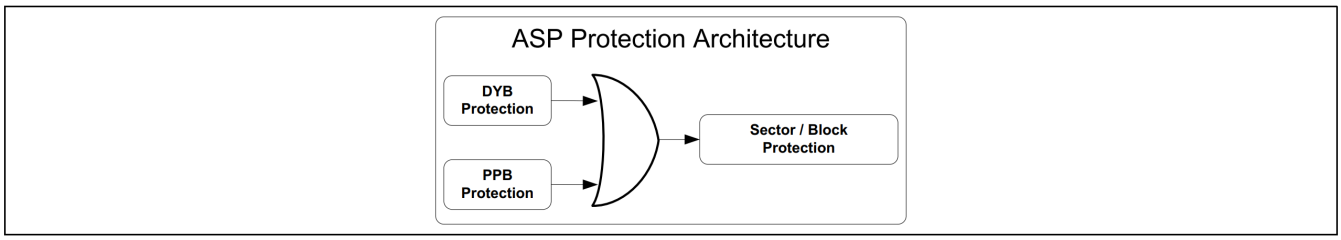


**图 43 DYB 和 PPB 保护控制**

ASP 提供了丰富的配置选项，可根据设计或系统需求生成多种数据保护机制。这些配置选项描述见第 47 页中的**“配置保护”**和第 52 页中的**“ASP 相关寄存器和命令传输”**。

### 4.5.2.1 配置保护

ASP 提供了通过持久保护机制来保护器件配置的措施。选择高级扇区保护寄存器 (ASPO[1] - ASPPER) 中的位 1 可选择持久保护机制并保护以下寄存器或寄存器位不被写入或编程：

- CFR1V[6,5,4,2]/CFR1N[6,5,4,2] - SP4KBS, TBPROT, PLPROT, TB4KBS
- CFR3N[3]/CFR3V[3] - UNHYSA
- ASPO[15:0]
- PWDO[63:0]

持久保护机制流程图如图 44所示。

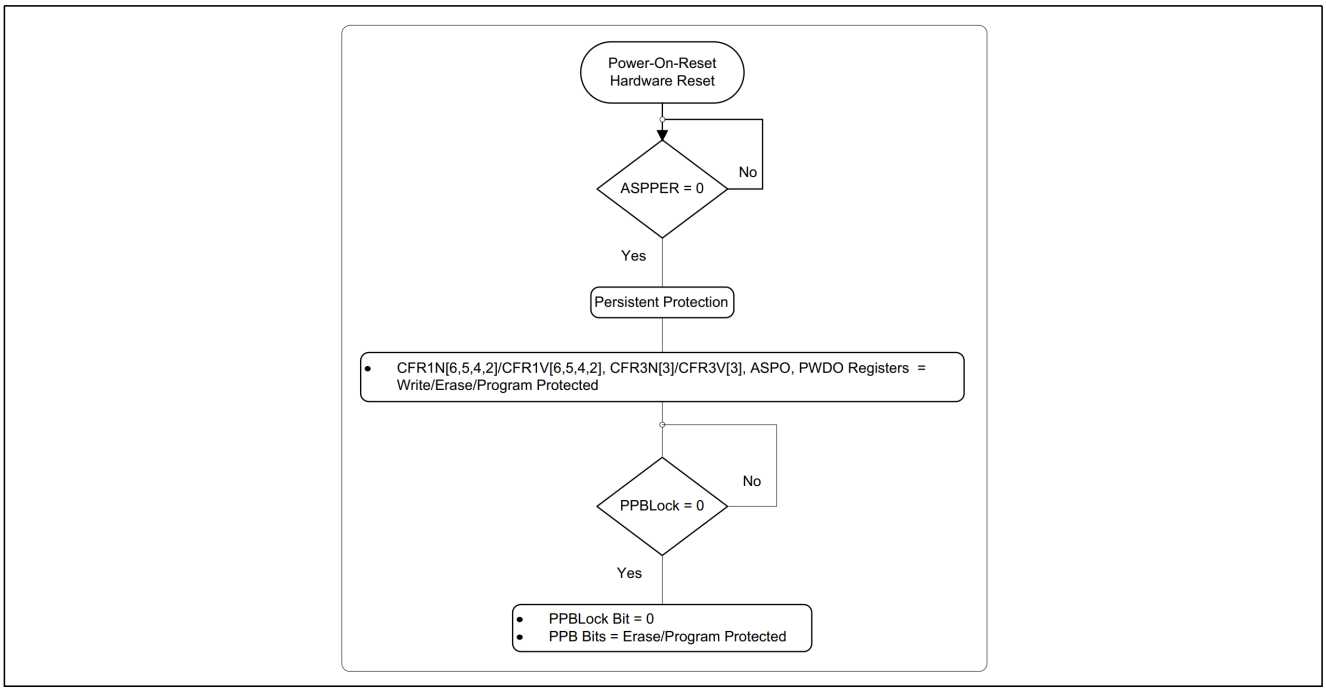


**图 44 持久保护机制流程图**

### 4.5.2.2 动态 DYB（易失性）扇区保护

动态保护比特(DYB)是易失性位，并且每个扇区只有一个唯一的DYB，可以按照扇区为单位单独进行修改。DYB只控制那些已清除PPB的扇区的保护。通过发出DYB写入命令传输，DYB被置位为“0”或清除为“1”，从而分别将每个扇区置于受保护或不受保护的状态。使用该功能，可以轻易保护扇区，避免意外改变相应扇区。另外需要更改时也可以轻易取消对其保护。DYB可以在需要时随时设为0或清除为1。

在动态扇区保护机制中，提供了一个选项，可以在上电（受保护）时将所有DYB易失性保护位重置为“0”，从本质上保护所有扇区免受擦除或写入的影响。在高级扇区保护寄存器 (ASPO[4] - ASPDYB) 中选择位 4 将为所有扇区在 Power-up 时选择动态保护 ( DYB )机制。如果需要，这些DYB位可以单独设置为“1”。上电动态扇区保护机制流程图如图 45所示。

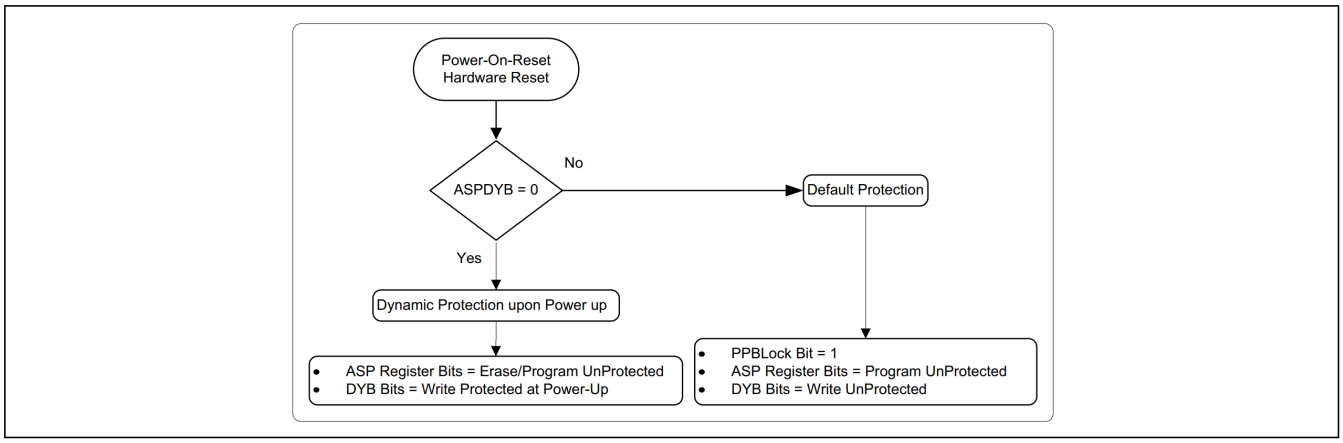


**图 45 动态扇区保护机制流程图**

### 4.5.2.3 永久/临时 PPB（非易失性）扇区保护

每个非易失位（PPB）为单个存储器扇区提供非易失保护，该扇区保持锁定（保护启用的），直到其相应的位被清除为1。控制 ASP 中基于 PPB 的非易失性选择有两种选项，即永久和临时。

### 4.5.2.4 永久性 PPB 保护机制

PPB位于一个单独的非易失性闪存阵列中。为每个扇区分配一个PPB位。当一个PPB位被写入为0时，相应的扇区受到保护，不能对它执行写入和擦除操作。PPB位可单独写入，但必须按组进行擦除。这与各个字可以在主阵列中单独写入，但整个扇区必须同时擦除的方式类似。编程一个PPB位需要典型的字编程时间。在 PPB 位写入操作或 PPB 位擦除期间，可以访问状态寄存器来确定操作是否完成。擦除所有PPB需要典型的扇区擦除时间。

永久性 PPB 保护机制，顾名思义，是永久性的并且永远不会改变。一旦决定了 PPB 保护架构，选择高级扇区保护寄存器（ASPO[0]）中的位 0 即可为所有 PPB 位启用永久保护，从而禁用所有 PPB 擦除和写入操作。ASPO 也受到保护以避免被写入或编程。

永久PPB保护机制流程图如图 46所示。

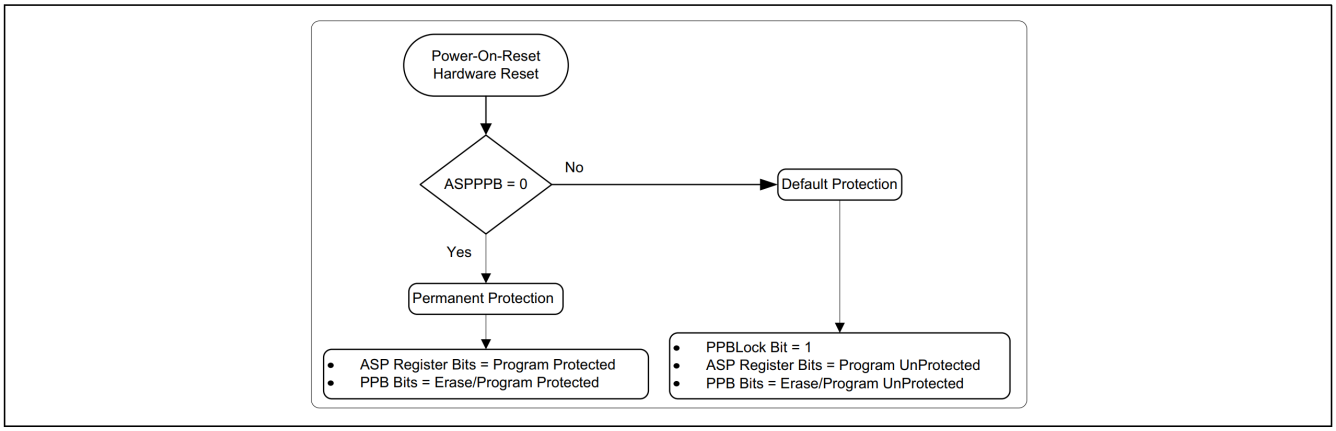


**图 46 永久PPB扇区保护流图**

### 4.5.2.5 临时 PPB 保护机制

基于 PPB 的非易失性保护架构可以被暂时锁定，从而禁止擦除和写入各个 PPB 位。持久保护位锁(PPBLock)是一个易失性位，用于保护所有PPB位。清除为0时，它锁定所有PPB；设成1时，允许更改PPB。每个器件只有一个PPB锁定位。PPB锁定命令传输 (WRPLB_0_0) 用于将该位清零。只有当所有PPB位均配置为所需的设置后，才将PPB锁定位清零。PPB 锁定位在POR或硬件复位期间置位为“1”。当使用 PPBLock 命令传输清除时，没有软件指令序列可以设置 PPBLock，只有额外的硬件复位或上电可以设置 PPBLock。

**注释：**临时 PPB 保护不需要任何 ASP 配置。

### 4.5.2.6 密码保护机制

密码保护机制要求使用 64 位密码来设置 PPBLock，从而实现更高级别的安全性。除了密码要求外，在上电和复位后，PPB锁定还将清除为0以确保在上电时提供保护。通过输入整个密码并成功执行密码解锁指令后，PPB锁定将设为1，从而允许修改扇区PPB。选择高级扇区保护寄存器 (ASPO[2] - ASPPWD) 中的位 2 可选择密码保护机制。密码保护机制还可以保护 ASPO 免遭写入或编程。

**注释：**在选择密码保护机制之前，必须先对密码进行编程。密码解锁SPI命令传输 (PWDUL_0_1) 或是八线命令传输 (PWDUL_4_1) 用于提供密码以进行比对。

密码保护机制流程图如**图 47**所示。

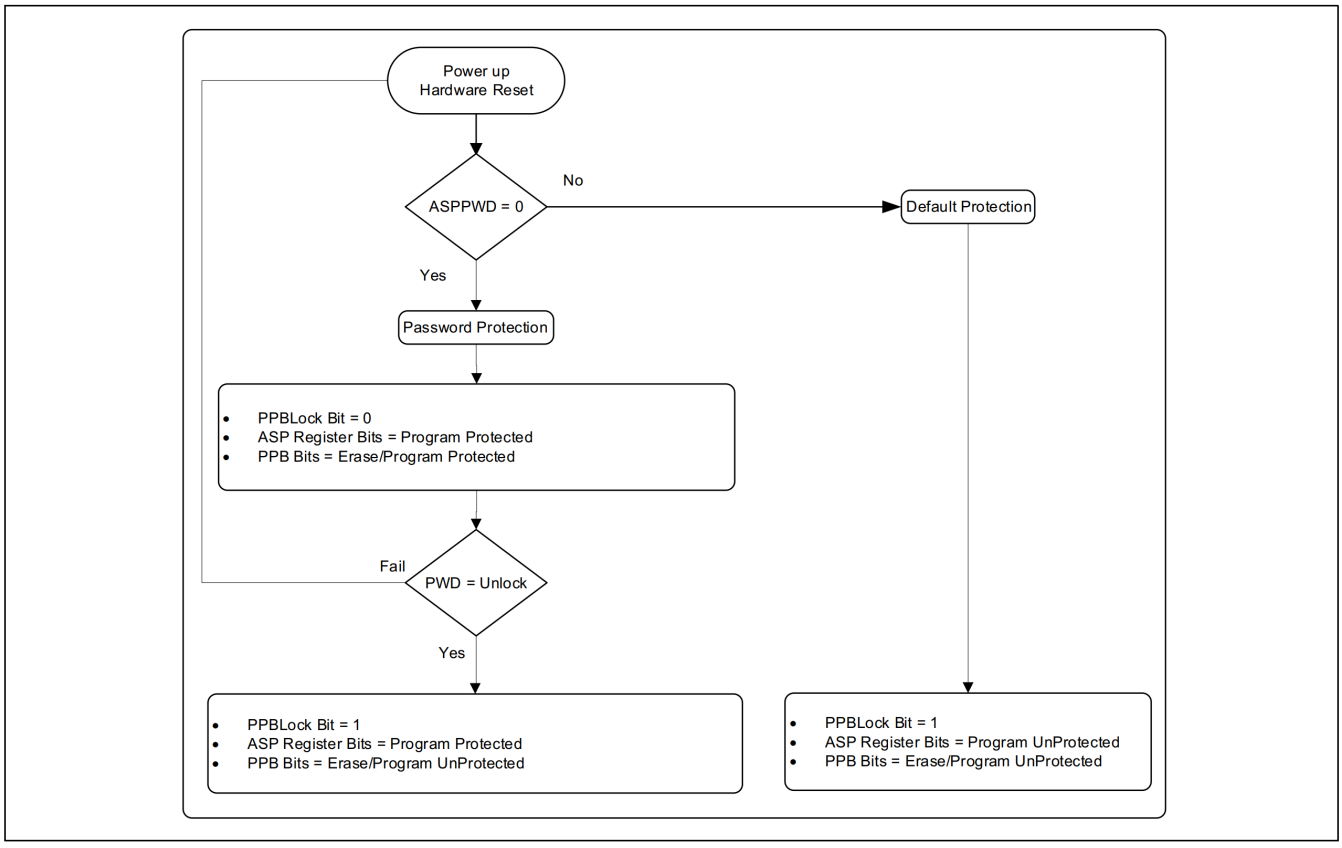


**图 47 密码保护机制流程图**

### 4.5.2.7 读取密码保护机制

读取密码保护机制可以用来取代密码保护机制，并提供最强大的数据保护。读取密码保护机制可以保护存储阵列免遭读取、写入和擦除。在密码解锁命令传输成功完成之前，只有配置寄存器 1 (CFR1x[5] - TBPROT) 的第 5 位选择的最低或最高 (256 KB) 扇区地址范围保持可读。无论读取命令传输中提供的扇区地址是什么，“0”都表示从最顶部的扇区选择，“1”则表示从最底部的扇区选择。注意，从阵列的读保护部分读取的数据将别名回到可读区域。

**注释：** 选择读取密码保护方案之前，必须先编程密码。密码解锁SPI 命令传输（PWDUL_0_1）或八线命令传输（PWDUL_4_1）用来提供用于比较的密码。读取密码保护方案流程图如 **图48**所示。

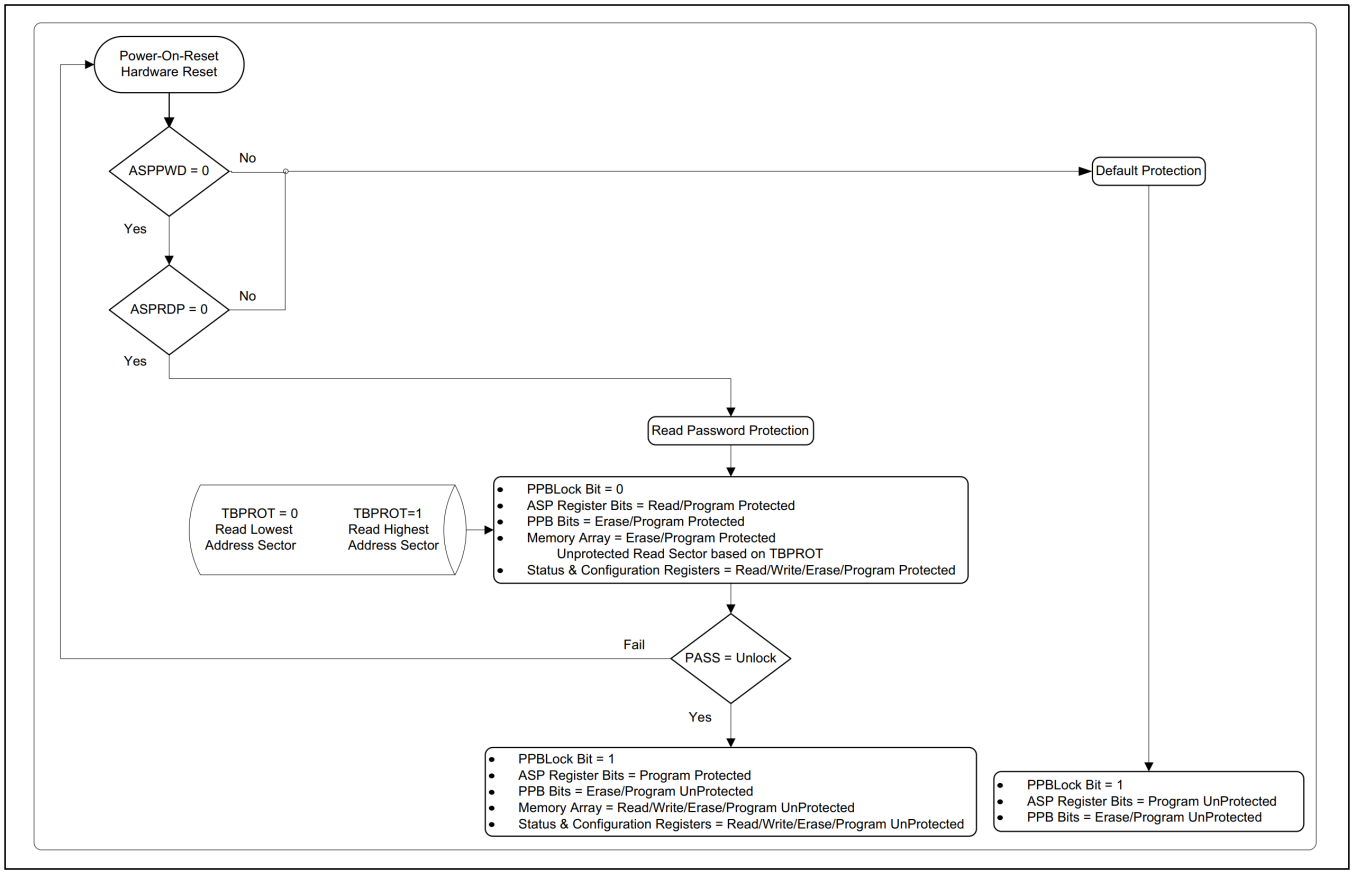


**图 48 读取密码保护机制流程图**

### 4.5.2.8 PPB 位 - OTP 选择

ASP 提供了一个配置选项来永久禁止 PPB 擦除命令传输(ERPPB_0_0)。这使得所有 PPB 位只能一次性可编程。使用此选项，一旦选择了 PPB 保护，将永远无法更改。选择高级扇区保护寄存器 (ASPO[3] - ASPPPB) 中的位 3 使得 PPB 位变成 OTP属性。

### 4.5.2.9 通用ASP使用准则

- 持久保护 (ASPPER) 和密码保护 (ASPPWD) 是互斥的 - 只能写入一个选项。
- 如果需要读取密码保护（ASPRDP），必须与密码保护（ASPPWD）同时进行编程。
- 一旦密码被烧录并验证，密码保护机制（ASPPWD）必须被写入（为 0）以防止读取密码。
- 当读取密码机制和密码保护机制启用时（即 ASPO[5] - ASPRDP, ASPO[2] - ASPPWD 写入为 0），则所有地址都会重定向到引导扇区，直到使用对的密码正确输入至密码解锁序列。此时，读取密码模式被禁用并且所有寻址都将选择至正确的位置。
- 当读密码保护模式激活时，不允许对存储空间进行写入或写入寄存器。

### 4.5.2.10 ASP 相关寄存器和命令传输

**表 26 ASP 相关寄存器和命令传输**

| Related registers | Related SPI transactions (see Table 81) | Related octal transactions (see Table 82) |
|---|---|---|
| Advanced Sector Protection Register (ASPO) (see Table 67) | Read Dynamic Protection Bit (RDDYB_4_0) | Read Dynamic Protection Bit (RDDYB_4_0) |
| Configuration Register 1 (CFR1N, CFR1V) (see Table 51) | Write Dynamic Protection Bit (WRDYB_4_1) | Write Dynamic Protection Bit (WRDYB_4_1) |
| | Read Persistent Protection Bit (RDPPB_4_0) | Read Persistent Protection Bit (RDPPB_4_0) |
| | Program Persistent Protection Bit (PRPPB_4_0) | Program Persistent Protection Bit (PRPPB_4_0) |
| | Erase Persistent Protection Bit (ERPPB_0_0) | Erase Persistent Protection Bit (ERPPB_0_0) |
| | Write PPB Protection Lock Bit (WRPLB_0_0) | Write PPB Protection Lock Bit (WRPLB_0_0) |
| | Read Password Protection Mode Lock Bit (RDPLB_0_0) | Read Password Protection Mode Lock Bit (RDPLB_4_0) |
| | Password Unlock (PWDUL_0_1) | Password Unlock (PWDUL_4_1) |
| | Write Enable (WRENB_0_0) | Write Enable (WRENB_0_0) |
| | Read Any Register (RDARG_C_0) | Read Any Register (RDARG_4_0) |
| | Write Any Register (WRARG_C_1) | Write Any Register (WRARG_4_1) |

### 4.5.3 安全存储区域（SSR）

安全存储区域（SSR）是一个 1024 字节的存储区域（与主存储阵列分开）。 1024 字节分为 32 个可单独锁定的 32 字节区域。图 49 提供了SSR的概述。

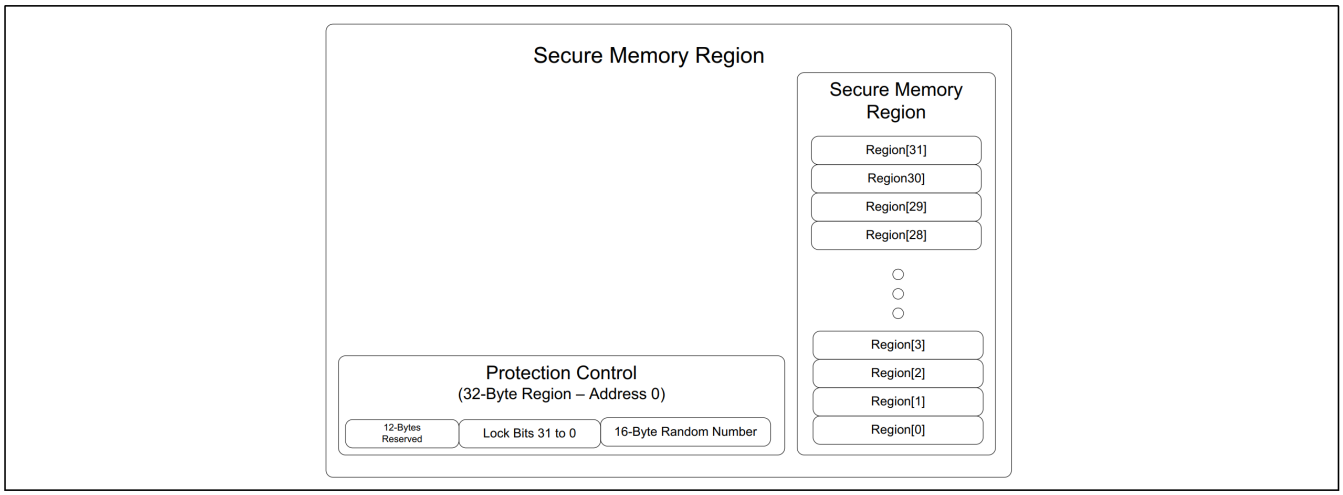


**图 49 OTP保护（非易失性）**

第一个 32 字节区域（从地址 0 开始）为其他 32 字节区域提供保护机制。该区域的最低十六个字节包含一个 128 位随机数。随机数不可写入、擦除或编程。接下来的四个字节（总共 32 位）如果置位为“0”可以为剩余的若干个32 字节区域提供写入保护 - 每 32 字节区域对应一个位。所有其他字节均被保留。

**注释：**尝试对 128 位随机数进行擦除和写入将分别导致 ERSERR 或 PRGERR。需要硬件复位才能使器件返回待机模式。

#### 4.5.3.1 SSR 相关寄存器和命令传输

**表 27 SSR 相关寄存器和命令传输**

| Related registers | Related SPI transactions (see Table 81) | Related octal transactions (see Table 82) |
|---|---|---|
| N/A | Program Secure Silicon Region (PRSSR_4_1) | Program Secure Silicon Region (PRSSR_4_1) |
| | Read Secure Silicon Region (RDSSR_4_0) | Read Secure Silicon Region (RDSSR_4_0) |

## 4.6 安全启动

SEMPER™闪存存储器包含一个嵌入式微处理器，用于初始化器件、管理嵌入式操作以及执行其他高级功能。该嵌入式设备的初始化失败或非易失性配置寄存器的配置损坏可能会导致闪存式存储器器件无法使用。除非发生灾难性事件，例如嵌入式硬件的永久损坏，一般情况下器件是可以恢复的。

SafeBoot 特性允许状态寄存器轮询通过错误编码的方式来检测嵌入式初始化故障或配置寄存器损坏。

### 4.6.1 微控制器初始化失败检测

如果嵌入在闪存式存储器器件中的中断未能初始化，则硬件复位可以恢复该器件，除非是灾难性故障。该硬件复位必须由主控控制器发起。一旦检测到失败的初始化，闪存式存储器器件会自动恢复到其默认启动引导模式 (1S-1S-1S)，并在其状态寄存器中提供故障错误码。**表 28** 显示检测到初始化失败时器件的状态寄存器位。

**表 28 状态寄存器 1 上电检测错误码**

| Bit | Field name | Function | Detection signature |
|---|---|---|---|
| STR1V[7] | RESRVD | Reserved for Future Use | 0 |
| STR1V[6] | PRGERR | Programming Error Status Flag | 1 |
| STR1V[5] | ERSERR | Erasing Error Status Flag | 1 |
| STR1V[4] | LBPROT[2:0] | Legacy Block Protection based memory Array size selection<br>**Note**: LBPRIT[2:0] can be anything from 000 to 111 based on Block Protection configuration | 0 |
| STR1V[3] | | | 0 |
| STR1V[2] | | | 0 |
| STR1V[1] | WRPGEN | Write/Program Enable Status Flag | 0 |
| STR1V[0] | RDYBSY | Device Ready/Busy Status Flag | 1 |

**表 29 检测到上电故障时的接口配置**[17]

| Interface | Transactions supported | Register type | Address (# of bytes) | Frequency of operation | Register read latency (# of clock cycles) | Output impedance |
|---|---|---|---|---|---|---|
| SPI (1S-1S-1S) | Read Status Register 1<br>Read Any Register | Status Register (Volatile Only) | 4 | Maximum (allowed for Read Status Register 1 and Read Any Register transaction) | 2 | 45 Ω |

**注释：**
17. 对于读取状态寄存器，向读取任意寄存器命令传输提供非易失性状态寄存器地址将产生不确定的结果。

### 4.6.1.1 主控轮询行为

主控将需要通过状态寄存器轮询序列来确定器件中是否发生初始化故障。该序列的流程图如图 50所示。

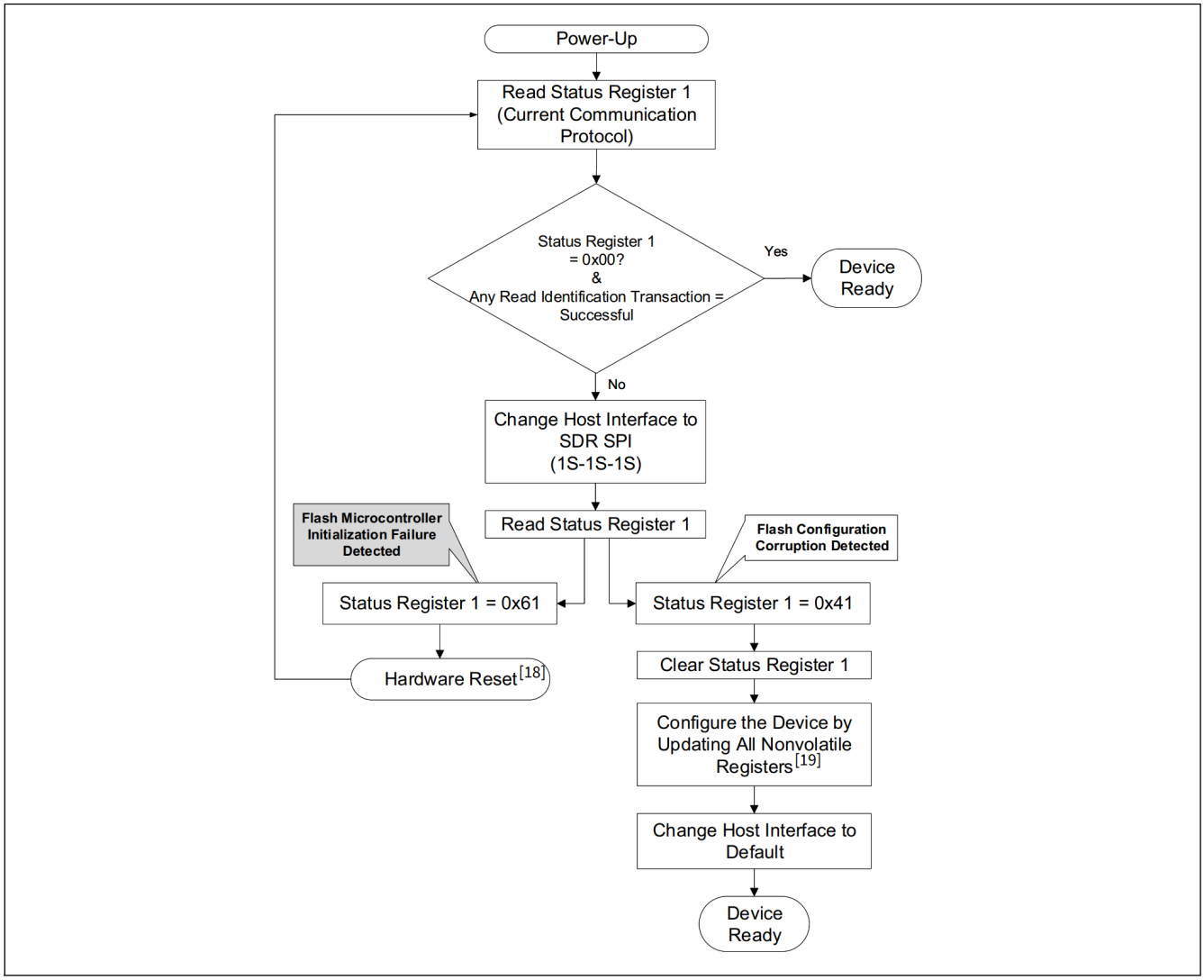


**图 50 用于微控制器初始化故障检测的主控轮询序列**

**注释：**轮询序列必须仅从较高的 I/O 接口配置开始到较低的 I/O 接口配置。例如，8D-8D-8D 至 1S-1S-1S。

**注释：**

18. 如果电路供电电压在规格范围内，并且硬件复位不能解决问题，请更换闪存式存储器器件。
19. 一旦第一个写入任意寄存器命令传输更新了非易失状态寄存器或配置寄存器，所有剩余的非易失状态和配置寄存器都会返回到预定义状态（STR1N = 0x00, CFR1N = 0x00, CFR2N = 0x00, CFR3N = 0x00, CFR4N = 0x00, CFR5N = 0x40). 建议启动

### 4.6.1.2 微控制器初始化初始化失败检测相关寄存器和命令序列

**表 30 微控制器初始化失败相关寄存器和命令序列**

| Related registers | Related SPI transactions (see Table 81) | Related octal transactions (see Table 82) |
|---|---|---|
| Status Register 1 Volatile (STR1V) (see Table 47) | Read Any Register (RDARG_C_0) | N/A |
| | Read Status Register -1 (RDSR1_0_0) | |

## 4.6.2 配置损坏检测

如果在器件的配置更新期间（例如写入非易失性寄存器时），发生掉电或硬件复位，则写入寄存器命令传输将被中断。器件将返回到待机模式，但由于嵌入式写入操作过早终止，非易失性寄存器数据很可能已被损坏。在下次上电时，将检测到配置损坏，并且器件将恢复为其默认的启动引导模式（1S-1S-1S）并允许再次重写配置。器件将维持配置的保护机制。

表 31 展示检测到配置损坏时器件的状态寄存器位。

**表 31 状态寄存器 1 配置损坏检测错误码**

| Bit | Field name | Function | Detection signature |
|---|---|---|---|
| STR1V[7] | RESRVD | Reserved for Future Use | 0 |
| STR1V[6] | PRGERR | Programming Error Status Flag | 1 |
| STR1V[5] | ERSERR | Erasing Error Status Flag | 0 |
| STR1V[4] | LBPROT[2:0] | Legacy Block Protection based memory Array size selection<br>**Note** LBPRIT[2:0] can be anything from 000 to 111 based on Block Protection configuration | 0 |
| STR1V[3] | | | 0 |
| STR1V[2] | | | 0 |
| STR1V[1] | WRPGEN | Write/Program Enable Status Flag | 0 |
| STR1V[0] | RDYBSY | Device Ready/Busy Status Flag | 1 |

**表 32 检测到配置损坏时的接口配置**

| Interface | Transactions supported | Address (# of bytes) | Frequency of operation | Register read latency (# of clock cycles) | Output impedance |
|---|---|---|---|---|---|
| SPI (1S-1S-1S) | All SPI (1S-1S-1S) Transactions | 4 | Maximum | 2 | 45 Ω |

### 4.6.2.1 主控轮询行为

主控将需要通过状态寄存器轮询序列来确定器件中是否发生配置损坏。该序列的流程图如图 51所示。

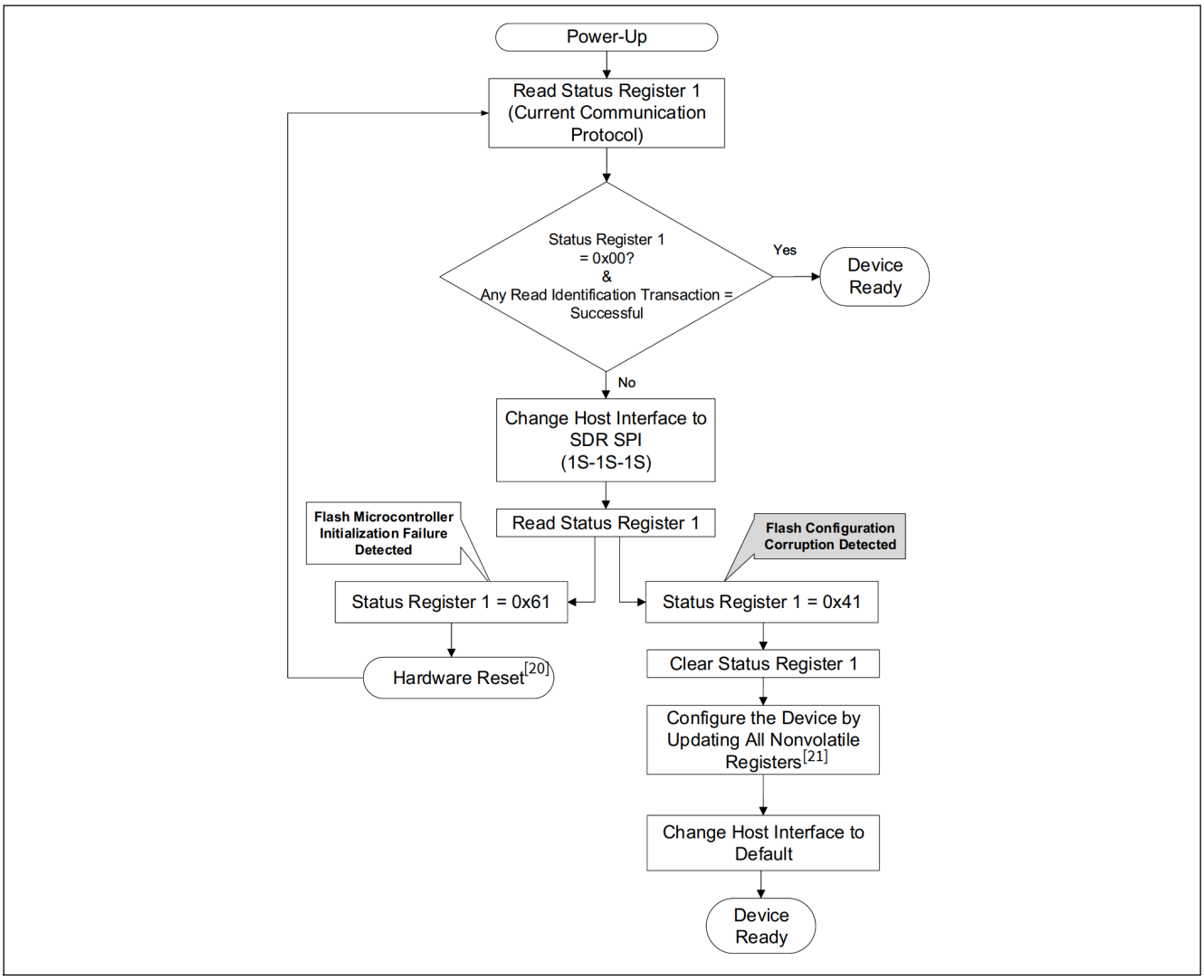


**图 51 配置损坏检测的主控轮询序列**

**注释：**轮询序列必须从较高的 I/O 接口配置开始到较低的 I/O 接口配置。例如，8D-8D-8D 至 1S-1S-1S。反之则不然。

**注释：**
20. 如果电路供电电压在规格范围内，并且硬件复位不能解决问题，请更换损坏/快闪式存储器器件。
21. 一旦第一个写入任意寄存器命令传输更新了非易失状态寄存器或配置寄存器，所有剩余的非易失状态和配置寄存器都会返回到预定义状态（STR1N = 0x00, CFR1N = 0x00, CFR2N = 0x00, CFR3N = 0x00, CFR4N = 0x00, CFR5N = 0x40). 建议启动

### 4.6.2.2 配置损坏检测相关寄存器

**表 33 配置损坏检测相关寄存器和传输命令**

| Related registers | Related SPI transactions (see Table 81) | Related octal transactions (see Table 82) |
|---|---|---|
| Status Register 1 Volatile (STR1V) (see Table 47) | All 1S-1S-1S Transactions | N/A |

## 4.7 自动启动

AutoBoot 允许主控在上电后或硬件复位后从 HL-T/HS-T 设备家族读取数据，而无需发送任何读取命令（包括地址）。根据器件配置，一旦 CS# 变为低电平并且 CK 被切换，数据就会在接口 I/O 上输出。

读取数据的起始地址在 AutoBoot 寄存器 (ATBN[31:9] - STADR[22:0]) 中指定。该起始地址可以位于内存中的任何页边界位置（512 字节页边界）。AutoBoot寄存器中还标识了启动延迟，它以时钟周期数 (ATBN[8:1] - STDLY[7:0]) 表示。这个延迟是在数据读取之前设定的。可以对延迟进行编程以满足主控的要求，但需要根据操作频率满足内存访问时间的最小量。强烈建议在AutoBoot执行成功或失败后检查状态寄存器 1 的值，以验证配置是否损坏（SafeBoot）。

**注释：**

- 必须禁用回卷功能才能实现AutoBoot。
- 作为高级扇区保护的一部分，当读取密码启用时，AutoBoot将被禁用。当读取密码功能启用时，建议禁用 AutoBoot (ATBN[0] - ATBTEN)。
- 启用接口 CRC（循环冗余校验）的AutoBoot需要读出至少 4 个字的数据。
- 强烈建议在长保留区域中分配第一个AutoBoot地址。

### 4.7.1 AutoBoot 相关的寄存器和命令传输

**表 34 AutoBoot 相关寄存器和命令传输**

| Related registers | Related SPI transactions (see Table 81) | Related octal transactions (see Table 82) |
|---|---|---|
| AutoBoot Register (ATBN) (see Table 72) | Read Any Register (RDARG_C_0) | Read Any Register (RDARG_4_0) |
| | Write Any Register (WRARG_C_1) | Write Any Register (WRARG_4_1) |
| | AutoBoot Transaction (see Figure 14) | AutoBoot Octal SDR Transaction (see Figure 27) / AutoBoot Octal DDR Transaction (see Figure 28) |

## 4.8 读取命令传输

HL-T/HS-T 支持不同的读命令传输来访问不同的存储器映射，即：读存储器阵列、读器件标识、读寄存器、读安全存储区域、读DYB和 PPB保护位。

这些读取命令传输可以使用以下三个接口和协议中的任何一个：

- SPI接口采用SDR (1S-1S-1S) 协议，传输一个字节指令，每个 CK 上升沿传输一位
- 八线接口采用SDR (8S-8S-8S) 协议，传输两个字节指令，每个 CK 上升沿传输八位
- 八线接口采用 DDR (8D-8D-8D) 协议，传输两个字节指令，每个 CK 上升沿和下降沿各传输八位

这些读取命令传输使用以下功能：

- 读取命令传输需要在地址之后增加延迟周期，以留出时间访问内存阵列（1S-1S-1S 协议的 RDAY1_4_0 和 RDAY1_C_0 除外）（参见**表 55**）。
- 数据选通 (DS ) 输出使存储控制器能够捕获数据眼中心的数据（请参阅63 页 **“数据选通 (DS )”**）。
- 读取命令传输具有 8、16、32 或 64 字节的回卷读取长度和对齐组选项（参见**表58** 和**表59** ）。

### 4.8.1 读取身份识别命令传输

有三种唯一标识命令传输，每种命令传输都支持所有三种协议（1S-1S-1S）、（8S-8S-8S）和（8D-8D-8D）（请参阅120页 **“命令传输表”**）。

#### 4.8.1.1 读取器件标识命令传输

读器件标识（RDIDN_0_0、RDIDN_4_0）命令传输提供器件制造商标识和器件标识的读访问。 SPI模式没有地址周期，而八线模式有四个虚拟地址 (00h)。该命令传输使用 (CFR3V[7:6]) 的延迟周期置位来使最大时钟频率在SPI模式下为 166 MHz，在 HL-T 八线模式下为 166 MHz，在 HS-T 八线模式下为 200MHz（见**表 55**)。八线模式支持DS捕获数据（见120页 **“命令传输表”**）。

#### 4.8.1.2 读取 SFDP 命令传输

读取串行闪存式存储器可发现参数（RSFDP_3_0、RSFDP_4_0）命令传输提供对JEDEC 串行闪存式存储器可发现参数（SFDP）的访问（请参阅120页 **“命令传输表”**)，该命令传输在 SPI 模式下使用 3 字节地址，在八线模式下使用 4 字节地址。如果设置了非零地址，则 SFDP 空间中的选定位置就是数据读取的起点。这可以支持随机访问 SFDP 空间中的任何参数。此命令传输支持连续（顺序）读取。需要八个延迟周期。在提供密码之前，读取密码模式不支持读取 SFDP 事务。读取 SFDP 事务的最大时钟频率在 SPI 模式下为 156 MHz，在八线 SDR 模式下为 92 MHz，在八线 DDR 模式下为 85MHz。

#### 4.8.1.3 读取唯一标识命令传输

读取唯一标识（RDUID_0_0）命令传输类似于读取器件标识命令传输，但访问每个器件唯一且不同的 64 位数字。它是工厂预烧录。

#### 4.8.1.4 读取身份识别相关寄存器及命令传输

**表 35 读取识别相关寄存器和命令传输**

| Related registers | Related SPI transactions (see Table 81) | Related octal transactions (see Table 82) |
|---|---|---|
| Configuration Register 3 (CFR3N, CFR3V) (see Table 56) | Read Identification (RDIDN_0_0) | Read Identification (RDIDN_4_0) |
| Configuration Register 5 (CFR5N, CFR5V) (see Table 60) | Read Serial Flash Discoverable (RSFDP_3_0) | Read Serial Flash Discoverable (RSFDP_4_0) |
| | Read Unique Identification (RDUID_0_1) | Read Unique Identification (RDUID_4_1) |

### 4.8.2 读取内存阵列命令传输

内存阵列数据可以从任意字节界限开始从内存中读取。数据字节按顺序从逐渐升高的字节地址读取，直到主控通过驱动 CS# 输入高电平来结束数据传输。如果字节地址达到闪存阵列的最大地址，则读取将从阵列的地址零继续。

#### 4.8.2.1 SPI 读取和快速读取命令传输

SPI读取和快速读取命令传输 (1S-1S-1S)SPI 用于支持需要向后兼容传统 SPI 的主控系统 。此协议不支持数据采集DS 。提供回卷读取长度选项。读取命令传输的最大时钟频率为 50 MHz，无需延迟周期。快速读取命令传输使用由 (CFR2V[3:0]) 设置的延迟周期，使最大时钟频率达到 166 MHz（参见120页 **“命令传输表”**）。

#### 4.8.2.2 读取八线SDR命令传输

读取八线SDR命令传输使用SDR (8S-8S-8S)协议提供高数据吞吐量。该协议支持DS数据捕获。提供回卷读取长度选项。此命令传输使用由CFR2V[3:0]设置的延迟周期，以实现最高166或200 MHz时钟频率（参见120页 **“命令传输表”**）。

#### 4.8.2.3 读取八线DDR命令传输

读取八线 DDR 命令传输使用 DDR (8D-8D-8D) 协议提供最快的数据吞吐量。该协议仅支持DS数据采集。提供回卷读取长度选项。此命令传输使用由 (CFR2V[3:0]) 设置的延迟周期，以实现最高 166 或 200 MHz 时钟频率（参见120页 **“命令传输表”**）。

#### 4.8.2.4 读取内存阵列相关的寄存器和命令传输

**表 36 读取存储器阵列相关寄存器和命令传输**

| Related registers | Related SPI transactions (see Table 81) | Related octal transactions (see Table 82) |
|---|---|---|
| Configuration Register 2 (CFR2N, CFR2V) (see Table 54) | Read (RDAY1_4_0, RDAY1_C_0) | Read Octal SDR (RDAY1_4_0) |
| Configuration Register 4 (CFR4N, CFR4V) (see Table 58) | Read Fast (RDAY2_C_0) | Read Octal DDR (RDAY2_4_0) |
| Configuration Register 5 (CFR5N, CFR5V) (see Table 60) | – | – |

### 4.8.3 读取寄存器命令传输

有多个寄存器用于报告嵌入式操作状态或控制器件配置选项。寄存器包含易失性和非易失性位。有两种读取寄存器的方法。“读取任意寄存器”事务提供一种读取所有器件寄存器的方法：通过地址选择读取非易失性和易失性寄存器。还有专用的寄存器读取命令传输，这些命令传输针对每个寄存器进行定义，并且仅读取该寄存器的内容。这些读取寄存器命令传输支持所有三种协议 (1S-1S-1S)、(8S-8S-8S) 和 (8D-8D-8D)（请参阅120页 **“命令传输表”**）。

#### 4.8.3.1 读取任何寄存器

读取任何寄存器命令传输是读取所有器件寄存器（包括非易失性和易失性）的最佳方式。命令传输包括要读取的寄存器的地址（详见120页 **“命令传输表”**）。接下来是一些延迟周期配置（CFR2V[3:0]）用于读取非易失寄存器，CFR3V[7:6]用于读取易失寄存器。NV寄存器延迟周期见**表 55**，易失性寄存器延迟周期见**表 57**。然后，返回选定的寄存器内容。在SPI 模式下，如果继续访问，则返回相同地址的寄存器内容，直到命令传输终止；每个“读取任意寄存器”命令传输仅读取一个字节的寄存器位置。对于包含多于一个字节数据的寄存器，必须再次使用“读取任意寄存器”命令传输来读取每个字节数据。八线模式支持使用DS 捕获数据（详见 120 页的**“命令传输表”**）。

读取任何寄存器命令传输的最大时钟频率在SPI模式下为 166 MHz，在 HL-T 八线模式下为 166 MHz，在 HS-T 八线模式下为 200 MHz。

读取任意寄存器 (RDARG_C_0) 命令传输可在嵌入式操作期间用于读取状态寄存器 1 (STR1V)。它不用于读取 ASP PPB 访问寄存器 (PPAV) 和 ASP 动态功能块访问寄存器 (DYAV) 等寄存器。需要单独的指令来选择和读取所访问阵列中的位置。如果通过编程 ASPR[2:0] 选择了 ASP 密码保护模式，则任意寄存器 (RDARG_C_0) 命令传输将从 PASS 寄存器位置读取无效数据。读取未定义的位置会提供未定义的数据。

#### 4.8.3.2 读取状态寄存器命令传输

读取状态寄存器（RDSR1_0_0/RDSR1_4_0、RDSR2_0_0/RDSR2_4_0）命令传输允许读取寄存器的易失性内容。SPI 模式没有地址周期，而八线模式有四个虚拟地址“00h”。该命令传输使用延迟周期置位 (CFR3V[7:6]) 来读取易失性寄存器，从而使最大时钟频率在SPI模式下为 166 MHz，在 HL-T 八线模式下为 166 MHz，在 HS-T 八线模式下为 200 MHz（见 **表55**）。八线模式支持DS 采集数据（参见120页 **“命令传输表”**）。

状态寄存器内容的易失性版本可随时读取，即使在烧录、擦除或写入操作正在进行时也是如此。

通过提供八个时钟周期的整倍数，可以连续读取状态寄存器 1。每读取八个周期就会更新一次状态。这仅限于 SPI 模式下。

### 4.8.3.3 读取动态保护位 ( DYB ) 访问寄存器命令传输

读取DYB访问寄存器 (RDDYB_4_0) 命令传输读取DYB访问寄存器的内容。该命令传输使用延迟周期设置位 (CFR3V[7:6]) 来读取易失性寄存器，从而使最大时钟频率在SPI模式下为 166 MHz，在 HL-T 八线模式下为 166 MHz，在 HS-T 八线模式下为 200 MHz（见**表 55**)。八线模式支持DS捕获数据（见120页 **“命令传输表”**)。可以连续读取DYB访问寄存器，但是DYB寄存器的地址不会递增，因此无法以这种方式读取整个DYB阵列。每个位置必须使用单独的“读取DYB命令传输进行读取。

### 4.8.3.4 读取持久保护位 (PPB) 访问寄存器命令传输

读取 PPB 访问寄存器 (RDPBB_4_0) 命令传输读取 PPB 访问寄存器的内容。该命令传输使用 (CFR2V[3:0]) 的延迟周期设置位来使最大时钟频率在SPI模式下为 166 MHz，在 HL-T 八线模式下为 166 MHz，在 HS-T 八线模式下为 200 MHz（参见**表55** ）。八线模式支持DS采集数据（参见120页 **“命令传输表”**)。可以连续读取 PPB 寄存器，但是 PPB 寄存器的地址不会递增，因此无法以这种方式读取整个 PPB 寄存器。每个位置必须使用单独的读取 PPB 命令传输进行读取。

### 4.8.3.5 读取 PPB 锁定寄存器命令传输

读取 PPB 锁定寄存器（RDPLB_0_0、RDPLB_4_0）命令传输允许读取非易失寄存器的内容。SPI 模式没有地址周期，而八线模式需要四个地址字节“00h”。该事务使用延迟周期设置位（CFR3V[7:6]）来读取易失性寄存器，以使最大时钟频率在SPI模式下为166 MHz，在HL-T 八线模式下为166 MHz，在HS-T 八线模式下为 200 MHz。八线模式支持DS 采集数据（参见120页 **“命令传输表”**）。可以连续读取 PPB 锁定位。

### 4.8.3.6 读取ECC数据单元状态

读取ECC数据单元状态 (RDECC_4_0) 命令传输用于确定所寻址的单位数据的ECC状态。在此命令传输中，地址的 LSb 必须与ECC数据单元对齐。该命令传输使用延迟周期设置位 (CFR3V[7:6]) 来读取易失性寄存器，从而使最大时钟频率在SPI模式下为 166 MHz，在 HL-T 八线模式下为 166 MHz，在 HS-T 八线模式下为 200 MHz。八线模式支持DS采集数据（参见120页 **“命令传输表”**）。

所选ECC单元的ECC状态的字节内容随之输出。任何后续数据都将是不确定的。要读取下一个ECC单元状态，应将另一个 RDECC_4_0 或 RDECC_C_0 命令传输发送到下一个地址，增量为 16 [数据单元大小/8] 字节。

### 4.8.3.7 读取寄存器相关的寄存器和命令传输

**表 37 读寄存器相关的寄存器和命令传输**

| Related registers | Related SPI transactions (see Table 81) | Related octal transactions (see Table 82) |
|---|---|---|
| Configuration Register 2 (CFR2N, CFR2V) (see Table 54) | Read Any Register (RDARG_C_0) | Read Any Register (RDARG_4_0) |
| Configuration Register 3 (CFR3N, CFR3V) (see Table 56) | | |
| Configuration Register 5 (CFR5N, CFR5V) (see Table 60) | Read Status Register 1 (RDSR1_0_0) | Read Status Register 1 (RDSR1_4_0) |
| | Read Status Register 2 (RDSR2_0_0) | Read Status Register 2 (RDSR2_4_0) |
| | Read DYB (RDDYB_4_0) | Read DYB (RDDYB_4_0) |
| | Read PPB (RDPPB_4_0) | Read PPB (RDPPB_4_0) |
| | Read PPB Lock (RDPLB_0_0) | Read PPB Lock (RDPLB_4_0) |
| | Read ECC Status (RDECC_4_0) | Read ECC Status (RDECC_4_0) |

## 4.8.4 数据选通（DS）

数据选通（DS）随数据一起向外传输，用于主控的数据捕获。在读取命令传输的数据传输期间， DS信号由器件驱动，并随着DQ信号数据转换而转换。DS 用作附加输出信号，具有与其他数据输出相同的时序特性，但保证随着每个数据位的传输而发生转换。DS与 DDR READ 的数据为边沿对齐，与SDR READ 的数据为中心对齐。DS上存在预驱动，以确保DS在最后一个地址字节输入到器件后的 2.5 个时钟周期后立即被驱动为低电平。

## 4.9 写入命令传输

有用于写入寄存器的写入命令传输。这些写入命令传输可以使用以下三种协议中的任何一种：

- SPI接口采用SDR (1S-1S-1S) 协议，传输一个字节指令，每个 CK 上升沿传输一位
- 八线接口采用SDR (8S-8S-8S) 协议，传输两个字节指令，每个 CK 上升沿传输八位
- 八线接口采用 DDR (8D-8D-8D) 协议，传输两个字节指令，每个 CK 上升沿和下降沿各传输八位

## 4.9.1 写使能命令传输

写入使能 (WRENB_0_0) 命令传输将状态寄存器 1 (STR1V[1]) 的写入程序使能状态 (WRPGEN) 位设置为“1”。通过发出写入使能 (WRENB_0_0) 命令传输来使能写入、编程和擦除命令传输，WRPGEN 位必须置位为“1”（参见120页 **“命令传输表”**）。

## 4.9.2 写无效命令传输

写无效（WRDIS_0_0）命令传输将状态寄存器1（STR1V[1]）的写使能状态（WRPGEN）位清除为“0”。

可以通过发出写无效 (WRDIS_0_0) 命令传输来将 WRPGEN 位清除为 0，来禁止那些需要将 WRPGEN 位置为 '1' 才能执行的命令。用户可以使用 WRDIS_0_0 命令传输来保护内存区域，防止无意的写入、烧录或擦除操作破坏内存内容。当 RDYBSY 位 = 1 (STR1V[0]) 时，WRDIS_0_0 命令传输在嵌入式操作期间被忽略（参见120页 **“命令传输表”**）。

### 4.9.3 清除写入和擦除失败标志命令传输

清除写入和擦除失败标志（CLPEF_0_0）命令传输将位STR1V[5]（擦除错误标志）和位STR1V[6]（写入错误标志）重置为“0”。即使当器件保持忙且 RDYBSY 置位为“1”时，该命令传输也会被接受，即使当任一故障位为置位且器件保持忙时。本次命令传输执行后，WRPGEN 位将保持不变（见120页 **“命令传输表”**）。

### 4.9.4 清除ECC状态寄存器命令传输

清除ECC状态寄存器(CLECC_0_0)命令传输会复位ECSV[4]（2位ECC检测）位、ECSV[3]（1位ECC校正）位、INSV[1:0] ECC检测状态位、地址捕获寄存器EATV[31:0]和ECC检测计数器ECTV[15:0]。此命令传输执行前无需置位 WRPGEN 位。即使器件保持忙且 WRPGEN 置位为“1”，清除ECC状态寄存器命令传输也会被接受，即使当任一故障位为置位且器件保持忙时。该指令执行后，WRPGEN 位将保持不变（见120页 **“命令传输表”**）。

### 4.9.5 写入任意寄存器命令传输

写入任意寄存器 (WRARG_C_1) 命令传输提供了一种写入任何器件寄存器（非易失性或易失性）的方法。该命令传输包括要写入的寄存器的地址，后面跟着要写入寻址寄存器的一个字节的数据（见120页 **“命令传输表”**）。

在器件接受 WRARG_C_1 / WRARG_4_1 命令传输之前，必须发出并解码写使能 (WRENB_0_0) 命令传输，这将状态寄存器中的写入/编程使能位 (WRPGEN) 设置为可以进行任何写入操作。可以检查 STR1V[0] 中的 RDYDSY 位来确定操作何时完成。可以检查 STR1V[6:5] 中的 PRGERR 和 ERSERR 位来确定操作期间是否发生任何错误。

一些寄存器混合了多种位类型和单独的规则来控制哪些位可以被修改。有些位是只读的，有些是 OTP，有些被指定为保留位（DNU）。

只读位永远不会被修改，并且 WRARG_C_1 / WRARG_4_1 命令传输数据字节中的相关位将被忽略，而不会设置编程或擦除错误指示（STR1V[6:5] 中的 PRGERR 或 ERSERR）。因此，WRARG_C_1 / WRARG_4_1 数据字节中这些位的值并不重要。

OTP位只能被编程为与其默认状态相反的位。将OTP位写回到其默认状态的操作将被忽略，并且不会发生任何错误。

由 WRARG_C_1 / WRARG_4_1 数据改变的非易失性位更新需要非易失性寄存器写入时间($t_W$)。更新过程涉及到对非易失性寄存器位的擦除和编程操作。如果这个过程中擦除或编程任意部分失败，SR1V 中的相关故障位和 WIP 将置位为“1”。

状态寄存器 1 可以被重复读取（轮询）来监测 RDYBSY 位（STR1V[0]）和错误位（STR1V[6,5]）并确定何时寄存器写入完成或失败。如果发生写入失败，则使用 CLPEF_0_0 命令传输清除错误状态并使器件返回待机状态。

ASP PPB 锁定寄存器 (PPLV) 寄存器不能通过 WRARG_C_1 / WRARG_4_1 命令传输写入。只有写 PPB 锁定位 (WRPLB_0_0) 命令传输可以写入 PPLV 寄存器。

数据完整性检查寄存器不能通过 WRARG_C_1 / WRARG_4_1 命令传输写入。通过运行数据完整性检查命令传输（DICHK_4_1）来加载数据完整性检查寄存器。

### 4.9.6 写入 PPB 锁定位

写入 PPB 锁定位 (WRPLB_0_0) 命令传输将 PPB 锁定寄存器 PPLV[0] 清零。 PPBLCK位用于保护PPB位。当 PPLV[0] = 0 时，PPB 编程/擦除命令传输将被中止。在读密码保护模式下，PPBLCK位还用于控制地址的高位，强制将地址范围限制在存储引导代码的扇区，直到提供读密码（参见120页 **“命令传输表”**）。

在器件接受 WRPLB_0_0 命令传输之前，必须发出写使能 (WRENB_0_0) 命令传输并器件对其进行解码，这会将状态寄存器中的写/编程使能 (WRPGEN) 设置为 1，以允许任何写操作。

操作正在进行时，仍然可以读取状态寄存器来检查 RDYBSY 位的值。WRPGEN 位在自定时操作期间为 1，完成后为 0。当写 PPB 锁定事务完成后，RDYBSY 位被置位为 0（参见120页 **“命令传输表”**）。

### 4.9.7 进入4字节地址模式

输入 4 字节地址模式 (EN4BA_0_0) 命令传输将易失性地址长度位 (CR2V[7]) 设置为“1”，以将大多数 3 字节地址指令更改为需要 4 字节地址。读取 SFDP（RSFDP_3_0）命令传输不受地址长度位的影响。JEDEC JESD216 标准要求 RSFDP_3_0 始终只有 3 个字节的地址。

POR、硬件或软件复位将根据非易失地址长度位 (CR2N[7]) 中的定义来设置地址长度。

### 4.9.8 退出4字节地址模式

退出 4 字节地址模式 (EX4BA_0_0）指令将易失性地址位 (CR2V[7]) 设置为“0”，以将大部分 3 字节地址指令更改为需要 3 字节地址。该指令不会仅影响 4 字节地址指令，该指令仍将继续要求 4 字节地址。

### 4.9.9 写入命令相关的寄存器和命令传输

**表 38 写入命令相关的寄存器和命令传输**

| Related registers | Related SPI transactions (see Table 81) | Related octal transactions (see Table 82) |
|---|---|---|
| Status Register 1 (STR1N, STR1V) (see **Table 47**) | Write Enable (WRENB_0_0) | Write Enable (WRENB_0_0) |
| Configuration Register 5 (CFR5N, CRF5V) (see **Table 60**) | Write Disable (WRDIS_0_0) | Write Disable (WRDIS_0_0) |
| ECC Status Register (ECSV) (see **Table 64**) | Clear Program and Erase Failure Flags (CLPEF_0_0) | Clear Program and Erase Failure Flags (CLPEF_0_0) |
| Interrupt Configuration (INCV) (see **Table 74**) | Clear ECC Status Register (CLECC_0_0) | Clear ECC Status Register (CLECC_0_0) |
| Address Trap Register (EATV) (see **Table 65**) | Write Any Register (WRARG_C_1) | Write Any Register (WRARG_4_1) |
| ECC Detection Counter (ECTV) (see **Table 66**) | Write PPB Lock Bit (WRPLB_0_0) | Write PPB Lock Bit (WRPLB_0_0) |
| Configuration Register 2 (CFR2V) (see **Table 51**) | Enter 4 Byte (EN4BA_0_0), Exit 4 Byte (EX4BA_0_0) | – |

## 4.10 编程

有用于将数据编程到存储器阵列、安全区域和持久保护位的写入命令传输。

这些写入命令传输可以使用如下三种协议：

- SPI接口采用SDR (1S-1S-1S) 协议，传输一个字节指令，每个 CK 上升沿传输一位
- 八线接口采用SDR (8S-8S-8S) 协议，传输两个字节指令，每个 CK 上升沿传输八位
- 八线接口采用 DDR (8D-8D-8D) 协议，传输两个字节指令，每个 CK 上升沿和下降沿各传输八位

在器件接受任何写入命令传输之前，必须先发出写使能 (WRENB_0_0) 命令传输并由器件解码。如果状态寄存器中的写/编程使能 (WRPGEN) 设置为“1”以允许程序操作，然后写入命令传输才能由器件执行。当一个写入命令传输完成时，WRPGEN 位被复位为‘0’。

当写入命令传输正在进行时，可以读取状态寄存器 1 以检查器件就绪/忙碌 (RDYBSY) 位的值。自定时写入命令传输期间，RDYBSY 位为“1”，完成时为“0”。

可以检查 STR1V[6] 中的 PGMERR 位来确定写入命令传输期间是否发生任何错误。

应用于已通过任何保护方式进行写保护的扇区的写入命令传输将不会被执行，并且将置位 PGMERR 状态失败。

当 CS# 被驱动到逻辑高电平状态时，写入命令传输将被启动。

### 4.10.1 编程粒度

HS/L-T家族支持多次写入（位遍历），其中在“1”上写入为“0”而不执行扇区擦除操作。此器件的非 AEC-Q100 工业温度范围（-40°C 至 +85°C）允许位遍历操作。每一个ECC数据单元在相邻两次擦除之间只允许进行一次写入操作（单次写入）的规则适用于较高温度范围（–40°C 至 +105°C）和（–40°C 至 +125°C）器件以及所有 AEC-Q100 器件。

没有执行擦除操作的多次写入将会使该器件的当前数据单元的ECC功能被禁用。注意如果启用了 2 位ECC ，则同一扇区内的多次写入将导致写入错误。

### 4.10.2 页编程

分页写入是通过将要写入的数据加载到页缓冲区并发出写入指令将数据从缓冲区移至闪存阵列内来完成的。这设置了可使用单个写入命令传输进行写入的数据量的上限。分页写入允许在一次操作中对最多 1 个分页大小（256 或 512 字节）进行写入。分页大小由配置寄存器 3 的CFR3V[4] 位来决定。分页在分页大小地址边界上对齐。可以从1位到分页大小来进行每个写入缓冲区的写入操作。建议写入16字节长度的整倍数并以对齐的写入块。这样可确保 ECC 不会被禁用。为了获得最佳的分页写入吞吐率，写入应以 512 字节边界对齐的整页 512 字节进行，并且每个分页只写入一次。

### 4.10.3 写入分页命令传输

写入分页（PRPGE_4_1）命令传输将数据写入到存储器阵列中。如果向器件发送的数据大于分页大小（256B 或 512B），则在起始地址和分页对齐结束边界之间的空间中，数据加载序列将从分页中的最后一个字节回卷到同一分页的零字节位置，并开始重写分页中先前加载的任何数据。如果向器件发送的数据少于分页，则发送的数据字节将从分页内提供的地址开始按顺序进行写入，而不会对同一分页的其他字节产生任何影响。写入过程由器件内部控制逻辑管理。PRGERR 位指示写入命令传输中是否发生了阻止写入成功完成的错误。这包括尝试对受保护区域进行写入（见120页 **“命令传输表”**）。

在八线SDR模式下，该命令传输可用于单字节指令，其地址可以从偶数或奇数地址开始。在DDR模式下，该指令只能用于编程2字节的倍数，并且地址必须从偶数地址开始。

### 4.10.4 写入安全区域命令传输

写入安全区域 (PRSSR_4_1) 命令传输将数据写入到SSR中，该 SSR 与主阵列数据位于不同的地址空间中，并且是OTP 属性。 SSR为 1024 字节，因此对于此命令传输，从 A31 到 A10 的地址位必须为零（见120页 **“命令传输表”**）。编程SSR空间时，需要将起始地址对齐到 32 位，即地址位 A1 和 A0 应为 0'b，主控应置位 CS# 以与 32 位对齐。

可以检查 STR1V[6] 中的 PRGERR 位来确定操作期间是否发生任何错误。为了以位颗粒度对OTP阵列进行写入，数据字节内的其余位可以设置为“1”。

每个 SSR 存储空间均可被写入一次或多次，前提是该区域未被锁定。尝试在锁定的区域中写入零将失败，并且 STR1V[6] 中的 PRGERR 位将置位为 1。写入一次，即使在受保护的区域也不会导致错误，也不会置位 PRGERR 位。后续写入仅可对未写入的位（即为“1”的数据）进行。在同一个ECC单元内写入多次将会使该数据单元上的ECC禁用。

### 4.10.5 写入持久保护位 (PPB)

写入持久保护位 (PRPPB_4_0) 命令传输对 PPB 寄存器中的位进行写入，以保护所提供地址的扇区不被写入或擦除（请参阅120页 **“命令传输表”**）。

可以检查 STR1V[6] 中的 PRGERR 位来确定操作期间是否发生任何错误。当尝试对受 ASPPPB （ASPO[3]）、ASPPRM （ASPO[0]）和 PPBLCK （PPLV[0]）位保护的 PPB 位进行写入时，写入 PPB 位命令传输将会中止/退出。

### 4.10.6 写入相关的寄存器和命令传输

**表 39 写入相关的寄存器和命令传输**

| Related registers | Related SPI transactions (see Table 81) | Related octal transactions (see Table 82) |
|---|---|---|
| Status Register 1 (STR1N, STR1V) (see **Table 47**) | Write Enable (WRENB_0_0) | Write Enable (WRENB_0_0) |
| Configuration Register 5 (CFR5N, CRF5V) (see **Table 60**) | Program Page (PRPGE_4_1) | Program Page (PRPGE_4_1) |
| Advance Sector Protect Register (ASPO) (see **Table 67**) | Program Secure Silicon (PRSSR_4_1) | Program Secure Silicon (PRSSR_4_1) |
| ASP PPB Lock (PPLV) (see **Table 69**) | Program Persistent Protection Bit (PRPPB_4_0) | Program Persistent Protection Bit (PRPPB_4_0) |
| ECC Status Register (ECSV) (see **Table 64**) | Clear Program and Erase Failure Flags (CLPEF_0_0) | Clear Program and Erase Failure Flags (CLPEF_0_0) |

## 4.11 擦除

对于内存阵列和持久保护位，有擦除命令传输可以将数据位变为“1”（所有字节均为 FFh）。

这些擦除命令传输可以使用以下三种协议中的任何一种：

- SPI接口采用SDR (1S-1S-1S) 协议，传输一个字节指令，每个 CK 上升沿传输一位
- 八线接口采用SDR (8S-8S-8S) 协议，传输两个字节指令，每个 CK 上升沿传输八位
- 八线接口采用 DDR (8D-8D-8D) 协议，传输两个字节指令，每个 CK 上升沿和下降沿各传输八位

在器件接受任何擦除命令传输之前，必须发出写使能 (WRENB_0_0) 命令传输并且被器件接收对其进行解码。如果状态寄存器中的 Write/Program 使能位 (WRPGEN) 置位为 '1' 来使能擦除操作，擦除命令传输才能被器件执行。当一个命令传输完成时，WRPGEN 位复位为“0”。

当命令传输处理正在进行时，可以读取状态 1 以检查器件就绪/忙 (RDYBSY) 位的值。自定时擦除命令传输期间，RDYBSY 位为“1”，完成时为“0”。

可以检查 STR1V[5] 中的 ERSERR 位来确定擦除命令传输期间是否发生任何错误。

应用于已通过块保护位或 ASP 写保护的扇区的擦除命令传输将不会被执行，并且将置位 ERSERR 状态失败位。

当 CS# 被驱动到逻辑高电平状态时，将启动擦除命令传输。

该器件出厂时的默认状态是所有字节均为 FFh。

### 4.11.1 擦除 4KB 扇区命令传输

擦除 4KB 扇区 (ER004_4_0) 事务将 4 KB 扇区的所有位设置为 1（所有字节均为 FFh）（参见120页 **“命令传输表”**）。

仅当器件配置为统一扇区（CFR3V [3] = 1）时，此命令传输将被忽略。如果将擦除 4KB 扇区命令传输发送到非 4KB 扇区地址，则器件将中止/退出该操作，并且不会设置 ERSERR 状态失败位。

### 4.11.2 擦除 256 KB 扇区命令传输

256 KB 扇区 (ER256_4_0) 命令传输将寻址扇区中的所有位设置为 1（所有字节均为 FFh）（请参阅120页 **“命令传输表”**）。

器件配置选项 (CFR3V[3]) 决定是否使用混合扇区架构。如果CFR3V[3] = 0, 4 KB 区扇覆盖器件地址空间的最高或最低地址 128 KB 或 64 KB 的一部分。如果将扇区擦除指令应用于被 4 KB 扇区覆盖的 256 KB 扇区，则被覆盖的 4 KB 扇区不受该扇区的影响。仅可见（非覆盖）的128 KB 或 192 KB 扇区的部分会被擦除。当 CFR3V[3] = 1 时，器件地址空间中没有 4 KB 扇区，扇区擦除命令传输始终在完全可见的 256 KB 扇区上操作。

当 BLKCHK 启用时，扇区擦除命令传输首先评估扇区的擦除状态。如果发现该扇区已被擦除，则擦除操作将中止。仅当在扇区中找到写入位时才会执行擦除操作。禁用 BLKCHK 将无条件执行擦除操作。

### 4.11.3 擦除芯片命令传输

擦除芯片（ERCHP_0_0）命令传输将整个闪存阵列内的所有位设置为“1”（所有字节均为 FFh）（参见120页 **“命令传输表”**）。

仅当块保护位（BP2、BP1、BP0）置位为0时，才能执行擦除芯片命令传输。若BP位不为零，则不执行命令传输，且ERSERR状态失败位不置位。命令传输将跳过任何受高级扇区保护DYB或 PPB 保护的扇区，并且 ERSERR 状态失败位将不会设置。

### 4.11.3.1 擦除持久保护位 (PPB) 命令传输

擦除 PPB（ERPPB_0_0）事务将所有 PPB 位设置为 1（参见120页 **“命令传输表”**）。如果 PPB 位受 ASPPPB (ASPO[3])、ASPPRM (ASPO[0]) 和 PPBLCK (PPLV[0]) 位保护，则此命令传输将中止/退出。

## 4.11.4 擦除状态及计数

### 4.11.4.1 评估擦除状态命令传输

评估擦除状态 (EVERS_4_0) 命令传输用于验证对寻址扇区的最后一个擦除操作是否已成功完成。如果所选扇区已成功擦除，则擦除状态位 (STR2V[2]) 置位为 1。如果所选扇区未完全擦除，则 STR2V[2] 为 0。在此命令传输之前无需执行写/编程使能事务（设置 WRPGEN 位）。但是，RDYBSY 位由器件自身设置，并在操作结束时清除，如读取状态时在 STR1V[0]中所示（请参阅120页 **“命令传输表”**）。

评估擦除状态命令传输可用于检测擦除操作是否因掉电、复位或擦除操作过程中的故障而失败。该命令传输需要 $t_{EES}$的时间完成并更新 STR2V 中的擦除状态。可以读取 RDYBSY 位 (STR1V[0]) 来确定评估擦除状态何时完成此命令传输。如果发现某个扇区未被擦除且 STR2V[2] = 0，则必须再次擦除该扇区以确保该扇区中数据的可靠存储。

### 4.11.4.2 扇区擦除计数命令传输

扇区擦除计数 (SEERC_4_0) 命令传输输出指定扇区的扇区擦除次数。扇区扇区计数存储在扇区扇区计数 (SECV[22:0]) 寄存器中，并且可以通过使用读取任何寄存器命令传输 (RDARG_C_0) 来读取。 RDYBSY 位由器件本身置位，并在操作结束时清除，如读取状态时在 STR1V[0] 中可见（见120页 **“命令传输表”**）。

该命令传输需要 $t_{SEC}$时间来完成并更新 SECV[22:0] 寄存器。可以读取 RDYBSY 位 (STR1V[0]) 以确定扇区计数命令传输何时完成。 SECV[23]位用于确定所报告的扇区擦除计数是否已损坏并已复位。

## 4.11.5 擦除相关寄存器及命令传输

**表 40 擦除相关寄存器和命令传输**

| Related registers | Related SPI transactions (see Table 81) | Related octal transactions (see Table 82) |
|---|---|---|
| Status Register 1 (STR1N, STR1V) (see **Table 47**) | Write Enable (WRENB_0_0) | Write Enable (WRENB_0_0) |
| Status Register 2 (STR2V) (see **Table 50**) | Erase 4KB Sector (ER004_4_0) | Erase 4KB Sector (ER004_4_0) |
| Configuration Register 5 (CFR5N, CFR5V) (see **Table 60**) | Erase 256KB Sector (ER256_4_0) | Erase 256KB Sector (ER256_4_0) |
| ASP PPB Lock (PPLV) (see **Table 69**) | Erase Chip (ERCHP_0_0) | Erase Chip (ERCHP_0_0) |
| ECC Status Register (ECSV) (see **Table 64**) | Evaluate Erase Status (EVERS_4_0) | Evaluate Erase Status (EVERS_4_0) |
| Sector Erase Count Register (SECV) (see **Table 73**) | Sector Erase Count (SEERC_4_0) | Sector Erase Count (SEERC_4_0) |
| | Erase Persistent Protection Bit (PPB) Transaction (ERPPB_0_0) | Erase Persistent Protection Bit (PPB) Transaction (ERPPB_0_0) |

## 4.12 暂停和恢复嵌入式操作

HL-T/HS-T 器件可以中断和暂停正在运行的嵌入式操作，例如擦除、写入或数据一致性检查。一旦主控完成中间操作并将相应的恢复命令传输发送到器件，它还可以恢复暂停的操作。

### 4.12.1 擦除、写入或数据完整性检查暂停

暂停命令传输允许系统中断写入、擦除或数据完整性检查操作，然后从任何其他非擦除暂停扇区、非编程暂停页面或阵列中读取数据。必须检查状态寄存器1 (STR1V[0]) 中的器件 Ready/Busy 状态标志 (RDYBSY)，以获得写入、擦除或数据一致性检查操作是否已经停止。

#### 4.12.1.1 写入暂停

- 写入暂停仅在写入操作期间有效。
- 状态寄存器 2（STR2V[0]）中的写入操作暂停状态标志（PROGMS）可用于确定在 RDYBSY 变为“0”时写入操作是否已暂停或已完成。
- 可以暂停写入操作以允许读取操作。
- 在写入暂停的分页内的任何地址读取都会产生不确定的数据。

#### 4.12.1.2 清除挂起

- 擦除挂起命令仅在扇区擦除操作期间有效。
- 状态寄存器 2 (STR2V[1]) 中的擦除操作暂停状态标志 (ERASES) 可用于确定在 RDYBSY 变为“0”时擦除操作是否已暂停或已完成。
- 全片擦除操作不能暂停。
- 可以暂停擦除操作以允许写入操作或读取操作。
- 在擦除暂停期间，可以读取 DYB 阵列来检查扇区保护情况。
- 在已暂停的擦除、写入或数据完整性检查操作的情况下，不允许进行新的擦除操作。在这种情况下，擦除指令将被忽略。
- 读取擦除暂停扇区内的任何地址都会产生不确定的数据。

#### 4.12.1.3 数据完整性检查暂停

- 数据完整性检查暂停仅在数据完整性检查计算操作期间有效。
- 状态寄存器 2（STR2V[4]）中的存储阵列数据完整性暂停状态标志位（DICRCS）可用于确定在 RDYBSY 变为“0”时数据完整性检查操作是否已暂停或已完成。
- 可以暂停数据完整性检查操作以允许读取操作。

在擦除、写入或数据完整性检查暂停期间，不允许执行写入任何寄存器或擦除持久保护位命令传输。因此，在暂停挂起期间不可能更改块保护或 PPB 位。如果有扇区在擦除暂停期间可能需要写入，则这些扇区应该仅受 DYB 位的保护，这些 DYB 位可以在擦除暂停期间关闭。

完成暂停操作所需的时间为$t_{PEDS}$。

当擦除暂停的写入操作完成后，器件返回到擦除暂停模式。系统可以通过读取状态寄存器1中的RDYBSY位来判断程序运行的状态，就像标准程序运行一样。**表 41** 列出暂停操作期间允许的命令传输。

**表 41　　暂停期间允许的命令传输**

| Transaction name | Allowed during erase suspend | 1. Allowed during program suspend | Allowed during data integrity check suspend |
|---|---|---|---|
| Write Disable (WRDIS_0_0) | Yes | No | No |
| Read Status Register 1 (RDSR1_0_0, RDSR1_4_0) | | Yes | Yes |
| Write Enable (WRENB_0_0) | | No | No |
| Read Status Register 2 (RDSR2_0_0, RDSR2_4_0) | | Yes | Yes |
| Program Page (PRPGE_4_1) | | No | No |
| Read ECC Status (RDECC_4_0) | | Yes | Yes |
| Clear ECC Status Register (CLECC_0_0) | | Yes | |
| Read PPB Lock Bit (RDPLB_0_0, RDPLB_4_0) | | | |
| Resume Program / Erase / Data Integrity Check (RSEPD_0_0) | | | |
| Program SSR (PRSSR_4_1) | | No | No |
| Read SSR (RDSSR_4_0) | | Yes | Yes |
| Read Unique ID (RDUID_0_0, RDUID_4_0) | | | |
| Read SFDP (RSFDP_3_0, RSFDP_4_0) | | | |
| Read Interface CRC Register (RDCRC_4_0) | | | |
| Read Any Register (RDARG_C_0, RDARG_4_0) | | | |
| Software Reset Enable (SRSTE_0_0) | | | |
| Clear Program and Erase Failure Flags (CLPEF_0_0) | | | |
| Software Reset (SFRST_0_0) | | | |
| Read Identification Register (RDIDIN_0_0, RDIDIN_4_0) (manufacturer and device identification) | | | |
| Suspend Program / Erase / Data Integrity Check (SPEPD_0_0) | | No | No |
| Read DYB (RDDYB_4_0) | | Yes | Yes |
| Read PPB (RDPPB_4_0) | | | |
| Read Octal SDR (RDAY1_4_0) | | | |
| Read Octal DDR (RDAY2_4_0) | | | |

### 4.12.2 擦除、写入或数据完整性检查恢复

必须通过发送擦除、写入或数据完整性检查恢复命令传输才能恢复暂停的操作。在写入、擦除或数据完整性检查暂停期间完成写入或读取操作后，将发送恢复命令传输以恢复暂停的操作。

发出擦除、写入或数据完整性检查恢复命令传输后，比特位 RDYBSY 位于状态寄存器 1 将置位为“1”，如果暂停，写入操作将恢复。如果没有暂停写入操作，则暂停的擦除操作将恢复。如果没有暂停的写入、擦除或数据完整性检查操作，则恢复命令传输将被忽略。

写入、擦除或数据一致性检查操作可以根据需要中断。例如，写入暂停命令传输可以紧跟在写入恢复命令传输之后，但为了使写入或擦除操作能够完成，在恢复和下一个暂停命令传输之间必须有一段大于或等于 $t_{PEDRS}$ 的时间间隔。图 52展示了暂停和恢复操作的流程。

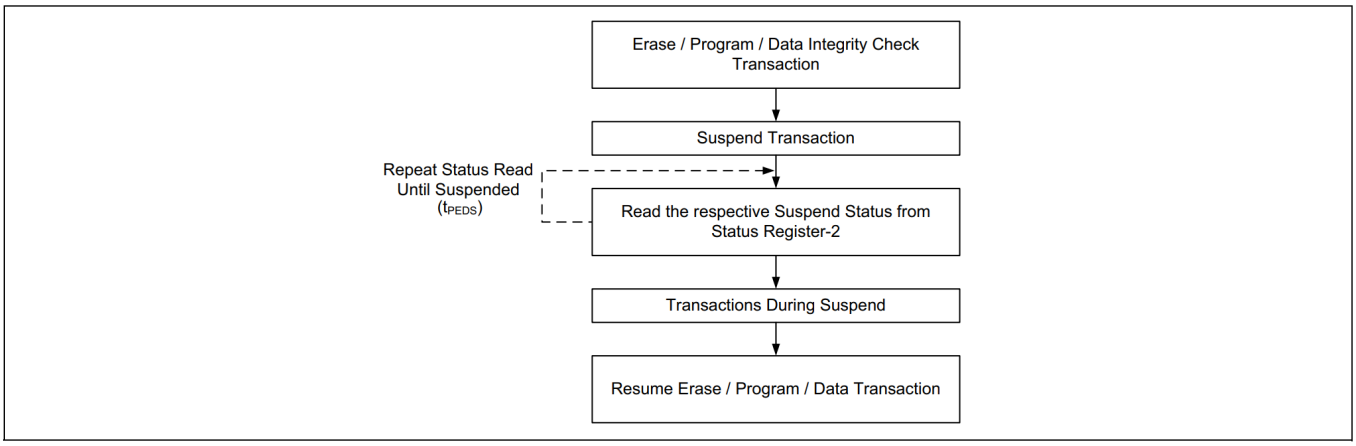


**图 52 暂停和恢复流程**

### 4.12.3 暂停及恢复相关寄存器及命令传输

**表 42 暂停及恢复相关寄存器及命令传输**

| Related registers | Related SPI transactions (see Table 81) | Related octal transactions (see Table 82) |
|---|---|---|
| Status Register 1 (STR1N, STR1V) (see Table 47) | Suspend Erase / Program / Data Integrity Check (SPEPD_0_0) | Suspend Erase / Program / Data Integrity Check (SPEPD_0_0) |
| Status Register 2 (STR2V) (see Table 50) | Resume Erase / Program / Data Integrity Check (RSEPD_0_0) | Resume Erase / Program / Data Integrity Check (RSEPD_0_0) |
| | Read Any Register (RDARG_C_0) | Read Any Register (RDARG_4_0) |
| | Read Status Register-1 (RDSR1_0_0) | Read Status Register-1 (RDSR1_4_0) |
| | Read Status Register-2 (RDSR2_0_0) | Read Status Register-2 (RDSR2_4_0) |

## 4.13 复位

HL-T/HS-T器件支持四种复位机制。

- 硬件复位（使用 RESET# 输入引脚）
- POR
- CS#信号复位
- 软件复位

### 4.13.1 硬件复位（使用 RESET# 输入引脚）

RESET# 输入启动复位操作，从逻辑高电平转换为逻辑低电平，持续时间 > $t_{RP}$ ，并使器件执行在 POR 期间执行的完整复位过程。硬件复位过程需要 $t_{RH}$ 时间才能完成。见**表89** 的时序规格。

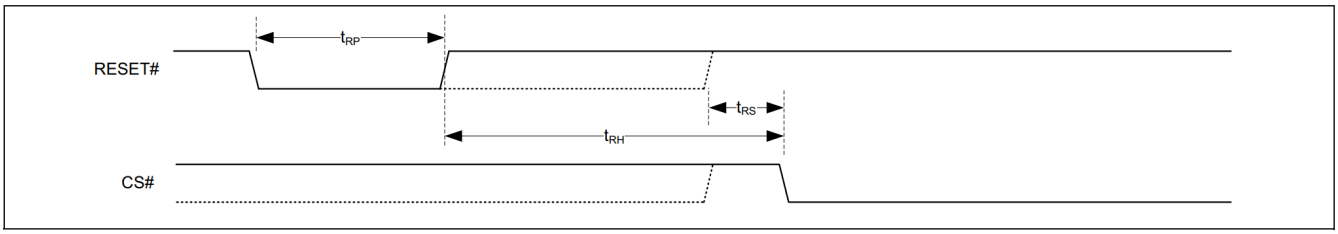


**图 53 使用 RESET# 输入进行硬件复位（复位脉冲 = $t_{RP}$ （最小值））**

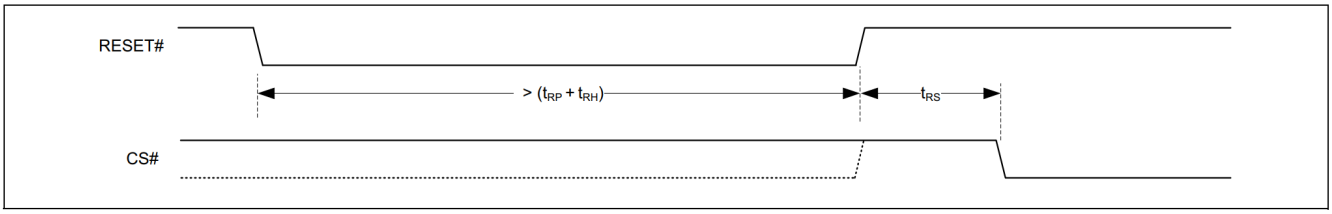


**图 54 使用 RESET# 输入进行硬件复位（复位脉冲 > ($t_{RP}$+ $t_{RH}$)）**

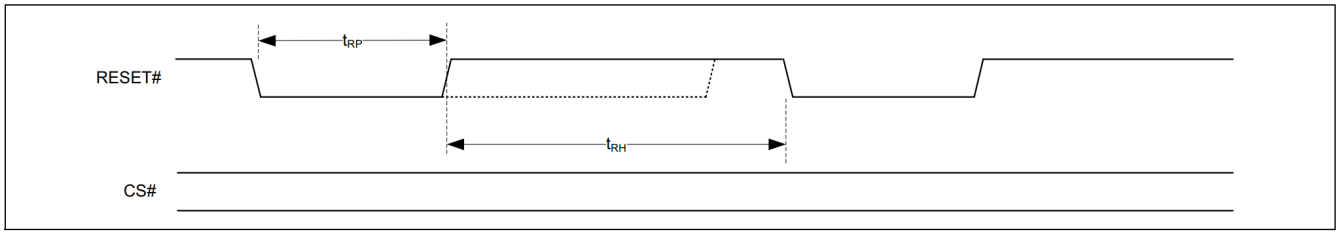


**图 55 使用 RESET# 输入的硬件复位（背对背硬件复位）**

### 4.13.2 上电复位 (POR)

该器件执行POR过程，直到 $V_{CC}$上升到最小 $V_{CC}$阈值之后经过 $t_{PU}$时间延迟 （见图 56 和 图57）。上电期间（$t_{PU}$）不得选通该器件。因此，CS# 必须随 $V_{CC}$ 上升。在 $t_{PU}$ 结束之前，不得向该器件发送任何指令。参见表89 的时序规格。

POR 期间会忽略 RESET#。如果 POR 期间 RESET# 为低电平，并在 $t_{PU}$ 结束后保持低电平 ，则 CS# 必须保持高电平，直到RESET# 返回高电平后并保持 $t_{RS}$为止。

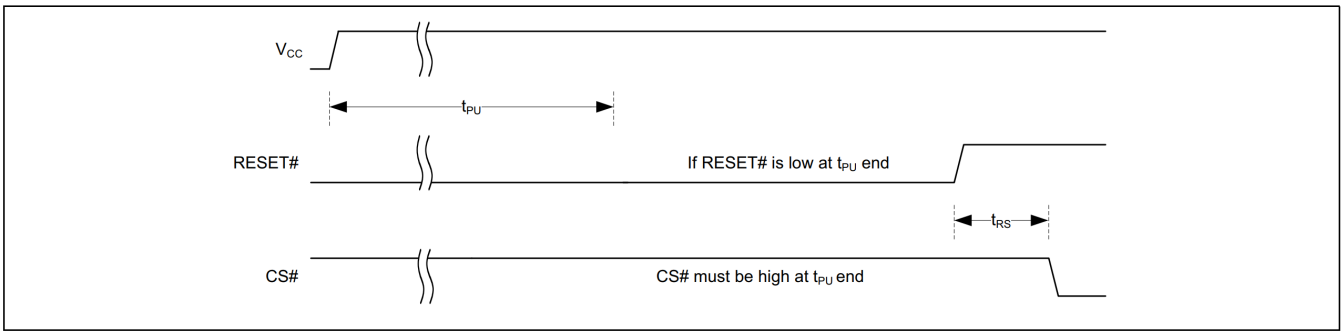


**图 56 POR 结束时复位为低电平**

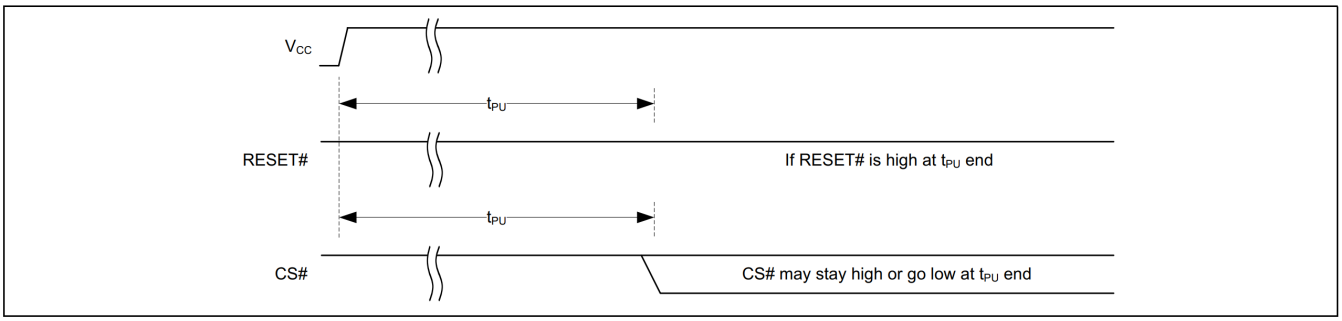


**图 57 POR 结束时复位为高电平**

### 4.13.3 CS#信号复位

CS#信号复位需要CS#和DQ0信号。该复位方法定义了一个信令协议，使用现有信号来启动SPI闪存式器件硬件复位，独立于器件运行模式或封装引脚数量。

信令协议如图 58所示。见表 89 的时序规范。CS#信号复位步骤如下：

- CS# 驱动为低电平有效。
- CK 在高电平或低电平状态下均保持稳定。
- CS# 和 DQ0 均被驱动为低电平。
- CS# 被驱动为高电平（无效）。
- 重复以上四个步骤，每次交替DQ0的状态总共四次。
- 复位发生在第四个 CS# 周期完成后，并且它变为高电平（非活动）时。

在第四个 CS# 脉冲后，从设备触发其内部复位，器件终止任何正在进行的操作，使所有输出为高阻态，并忽略 $t_{RESET}$ 期间的所有读/写命令传输。然后器件将处于待机状态。

该复位序列不适用于正常上电的情况，而仅适合在器件未对系统作出响应时使用。无论器件处于什么状态，此复位序列都可以运行。因此，JEDEC串行闪存式器件复位信号协议对于不支持 RESET# 引脚的封装非常有用，可提供与硬件复位相同的行为。

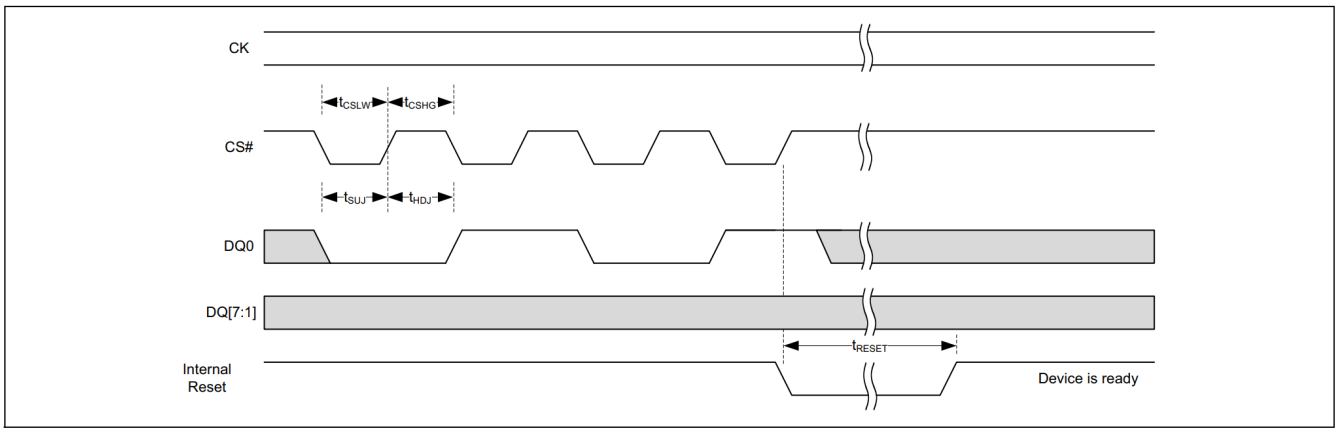


**图 58 CS#信令复位协议**

### 4.13.4 软件复位

软件控制的复位命令传输通过从非易失性默认值（保护寄存器除外）重新加载至易失寄存器，将器件恢复到其初始上电状态。它还会终止嵌入式操作。当 CS# 在命令传输结束时变为高电平时，将执行复位命令传输 (SFRST_0_0)，并需要 $t_{SR}$时间来执行。见**表 89** 的时序规范。

在复位命令传输 (SFRST_0_0) 之前需要立即执行复位使能 (SRSTE_0_0) 命令传输，以便软件复位执行两个命令传输的序列。SRSTE_0_0 命令传输之后除 SFRST_0_0 以外的任何命令传输都将清除复位使能条件，并防止后面的 SFRST_0_0 命令传输被识别。

复位（SFRST_0_0）命令传输紧接着 SRSTE_0_0 命令传输，从而启动软件复位过程。 在软件复位期间，在器件的易失性和非易失性配置状态相同时，仅支持状态寄存器 1 的 RDSR1_4_0 ， RDARG_C_0和RDARG_4_0 操作。 如果配置状态在软件复位期间发生变化，则只能在软件复位时间过去后才可读取状态寄存器 1。

软件复位与 RESET# 的状态无关。如果 RESET# 为高电平或未连接，并且发出软件复位命令传输，则器件将执行软件复位。

#### 4.13.4.1 软件复位相关寄存器和命令传输

**表 43 软件复位相关寄存器和命令传输**

| Related registers | Related SPI transactions (see Table 81) | Related octal transactions (see Table 82) |
|---|---|---|
| N/A | Software Reset Enable (SRSTE_0_0) | Software Reset Enable (SRSTE_0_0) |
| | Software Reset (SFRST_0_0) | Software Reset (SFRST_0_0) |

### 4.13.5 复位行为

**表 44 复位行为**

| Transaction / register name | POR | Hardware reset and CS# signaling reset | Software reset |
|---|---|---|---|
| Summary | • Device Reset<br>• Status Bits Reset<br>• All Volatile Registers Reset<br>• Configuration Reload to Default<br>• Volatile Protection Reset to Default<br>• Non-volatile Protection unchanged<br>• Reset all Embedded operations | • Device Reset<br>• Status Bits Reset<br>• All Volatile Registers Reset<br>• Configuration Reload to Default<br>• Volatile Protection Reset to Default<br>• Non-volatile Protection unchanged<br>• Reset all Embedded operations | • Device Reset<br>• Status Bits Reset<br>• Configuration Reload to Default<br>• Volatile Protection Reset to Default<br>• Non-volatile Protection unchanged<br>• Reset all Embedded operations |
| Interface Requirements | • All Inputs - Ignored<br>• All Outputs - Tristated | • All Inputs - Ignored<br>• All Outputs - Tristated | Transactions (SRSTE_0_0, SFRST_0_0) |
| Status Registers | Load from Non-volatile Registers | Load from Non-volatile Registers | Load from Non-volatile Registers |
| Configuration Registers | Load from Non-volatile Registers | Load from Non-volatile Registers | Load from Non-volatile Registers |
| Protection Registers | PPB Lock Register - Load based on ASPO[2:1] | PPB Lock Register - Load based on ASPO[2:1] | PPB Lock Register - No Change |
| | DYB Access Register - Load based on ASPO[4] | DYB Access Register - Load based on ASPO[4] | DYB Access Register - No Change |
| | Password Register - Load based on ASPO[2] and ASPO[0] | Password Register - Load based on ASPO[2] and ASPO[0] | Password Register - No Change |
| ECC Status Register | Load 0x00 | Load 0x00 | Load 0x00 |
| AutoBoot Register | Load from Non-volatile Registers | Load from Non-volatile Registers | No Change |
| Data Integrity Check Register | Load 0x00 | Load 0x00 | Load 0x00 |
| Interface CRC Register | Load 0x00 | Load 0x00 | Load 0x00 |
| ECC Error Count Register | Load 0x00 | Load 0x00 | Load 0x00 |
| Address Trap Register | Load 0x00 | Load 0x00 | Load 0x00 |
| Endurance Flex Register | Load from Non-volatile Registers | Load from Non-volatile Registers | No Change |
| I/O Mode | Load from Non-volatile Registers | Load from Non-volatile Registers | No Change |
| Memory/Register Erase in Progress | Not Applicable | Abort Erase | Abort Erase |

表 44　复位行为（续）

| Transaction / register name | POR | Hardware reset and CS# signaling reset | Software reset |
|---|---|---|---|
| Memory/Register Program in Progress | Not Applicable | Abort Program | Abort Program |
| Memory/Register Read in Progress | Not Applicable | Abort Read | Not Applicable |
| INT# Pin Configuration Register | Load 0xFF | Load 0xFF | Load 0xFF |
| INT# Pin Status Register | Load 0xFF | Load 0xFF | Load 0xFF |

## 4.14　电源模式

### 4.14.1　有源电源和备用电源模式

当片选 (CS#) 为低电平时，器件处于使能状态并处于有效的电源模式。当 CS# 为高电平时，器件被禁用，但可能仍处于有效电源模式，直到所有编程、寄存器和写操作完成。然后器件进入待机电源模式，功耗降至 $I_{SB}$。见表 87的参数规格。

### 4.14.2　深度掉电（DPD）模式

虽然正常运行期间的待机电流相对较低，但通过 DPD 模式可以进一步降低待机电流。较低的功率消耗使得 DPD 模式特别适用于电池供电的应用。

#### 4.14.2.1　进入 DPD 模式

器件可以通过两种方式进入 DPD 模式：

1. 使用命令传输进入 DPD 模式
2. 上电或复位后进入 DPD 模式

**使用进入深度掉电模式命令传输进入 DPD 模式**

通过发送进入深度掉电模式命令传输 (ENDPD_0_0) 然后等待 $t_{ENTDPD}$ 延迟，即可使能 DPD 模式。在锁存指令字节后，必须将 CS# 引脚驱动为高电平。否则，将不会执行 DPD 命令传输。在 CS# 引脚驱动为高电平后，将在 $t_{ENTDPD}$ 时间内进入电源下降状态（见表 89 的时序规范）并且功率消耗下降到 $I_{DPD}$（见表 87 的参数规范）。

DPD 只能从空闲状态进入。仅当器件未执行嵌入式算法（如易失性状态寄存器 1、器件就绪/忙状态标志 (RDYBSY) 位清除为零 (STR1V[0] = RDYBSY = 0) 所示）时，才接受 DPD 命令传输。在 $t_{ENDPD}$时间内不允许向器件发送任何命令传输。

**上电或复位后进入 DPD 模式**

如果 DPDPOR 配置位为使能（CFR4NV[2] = 1），则在上电、硬件复位或JEDEC串口闪存式器件复位信令协议完成后，器件将处于 DPD 模式。在POR 或复位期间，CS# 应跟随VCC上施加的电压进入 DPD 模式，如图 59所示。在$t_{ENTDPD}$时间内不允许向器件发送任何命令传输。

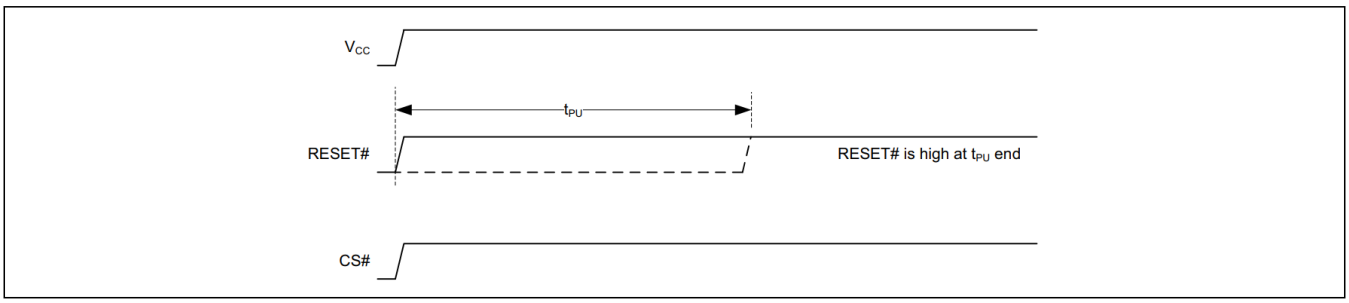


**图 59　　上电或复位时进入 DPD 模式**

### 4.14.2.2　退出 DPD 模式

器件离开 DPD 模式可通过以下方式之一：

**硬件复位后退出 DPD 模式**

当器件处于 DPD 且 CFR4NV[2] = 0 时，硬件复位会将器件返回到正确模式。

**CS# 脉冲触发后退出 DPD 模式**

器件在收到宽度为 $t_{CSDPD}$ 的CS# 脉冲后退出 DPD。 CS# 应在脉冲后驱动为高电平。 DPD退出后，需要CS# 上的高电平到低电平跳变来启动命令传输周期。退出 DPD 模式需要 $t_{EXTDPD}$时间。器件直到 $t_{EXTDPD}$之后才会响应。

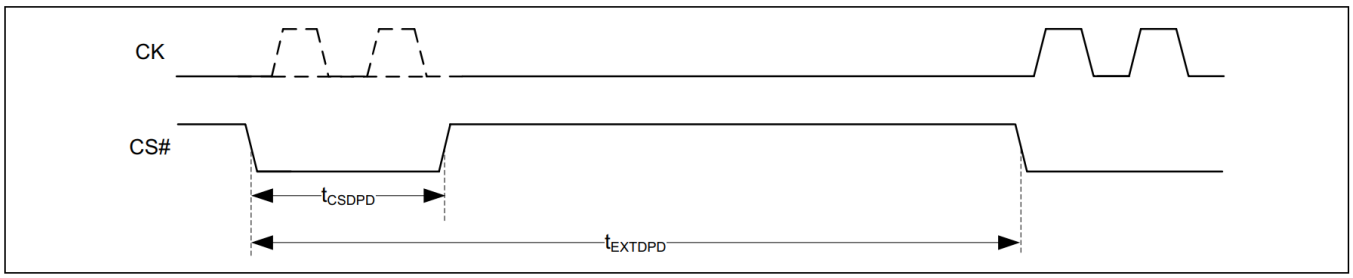


**图 60　　退出DPD模式**

器件在 DPD 期间保持其配置，这意味着器件退出 DPD 时的状态与进入 DPD 时的状态相同。ECC 状态、ECC 错误检测计数器、地址捕获和中断状态寄存器等寄存器将被清除。

### 4.14.2.3　DPD 相关寄存器和命令传输

**表 45　　DLP 相关寄存器和命令传输**

| Related registers | Related SPI transactions (see Table 81) | Related octal transactions (see Table 82) |
|---|---|---|
| Configuration Register 4 (CFR4N, CFR4V) (see Table 58) | Enter Deep Power Down Mode (ENDPD_0_0) | Enter Deep Power Down Mode (ENDPD_0_0) |

## 4.15 上电和断电

在 $V_{CC}$ 达到如下正确值之前，一定不要在电压上升或掉电时选通该器件：

- $V_{CC}$ （最小值）在电压上升时，然后再延迟 $t_{PU}$
- $V_{SS}$在掉电时

### 4.15.1 上电

该器件忽略所有事务，直到$V_{CC}$上升到最小 $V_{CC}$阈值之后且经过 $t_{PU}$ 的时间延迟 （见**图 61** )。但是，如果 $V_{CC}$在 $t_{PU}$期间恢复到 $V_{CC}$(min)以下，则不能保证器件的正确工作。在$t_{PU}$结束之前，不应向器件发送任何指令 。

器件在 $t_{PU}$期间吸收 $I_{POR}$ 电流。上电（$t_{PU}$）后，WRPGEN 位复位，可以选择处于 DPD 模式或 Standby 模式。在配置寄存器 4 (CFR4N[2]) 中的 DPDPOR 位控制在POR完成后器件是否处于 DPD 或Standby模式（参见**表 58** ）。如果 DPDPOR 位是启用的 (CFR4N[2] = 1) 上电后器件处于 DPD 模式。在POR之后，需要使用硬件复位 (RESET#) 将器件返回到待机模式

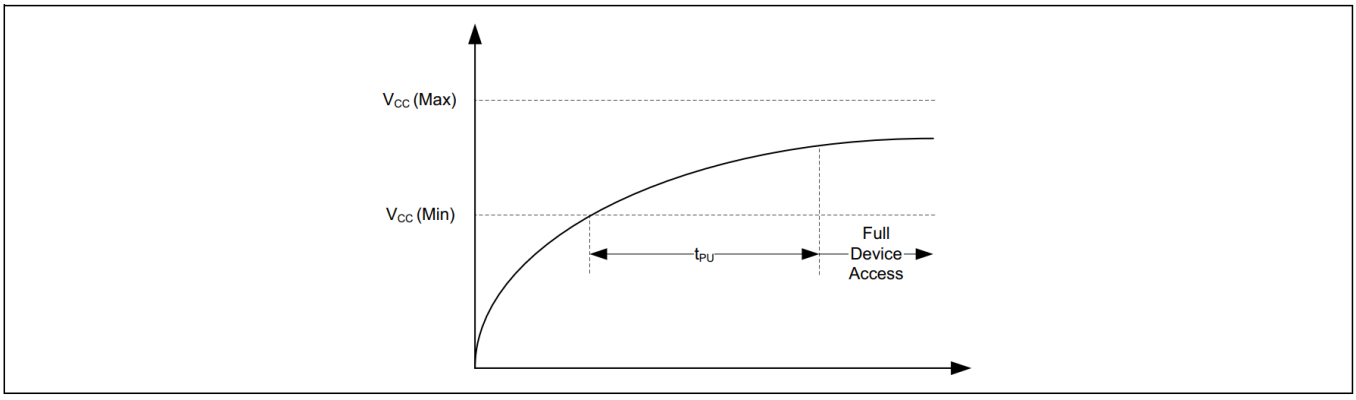


**图 61 上电**

### 4.15.2 掉电

在掉电或电压降至 $V_{CC}$ (截止)以下时，电压必须降至 $V_{CC}$ (低电平) 以下并持续 $t_{PD}$时间 ，以使部件正确初始化上电 (见**图62**）。如果在降压过程中 $V_{CC}$ 保持在 $V_{CC}$ (截止)以上，则器件将保持初始化状态，并在 $V_{CC}$ 再次高于$V_{CC}$ (最小值) 时正常工作。如果在上电后POR 未正确完成，则 RESET# 信号的置位将重新启动POR 过程。

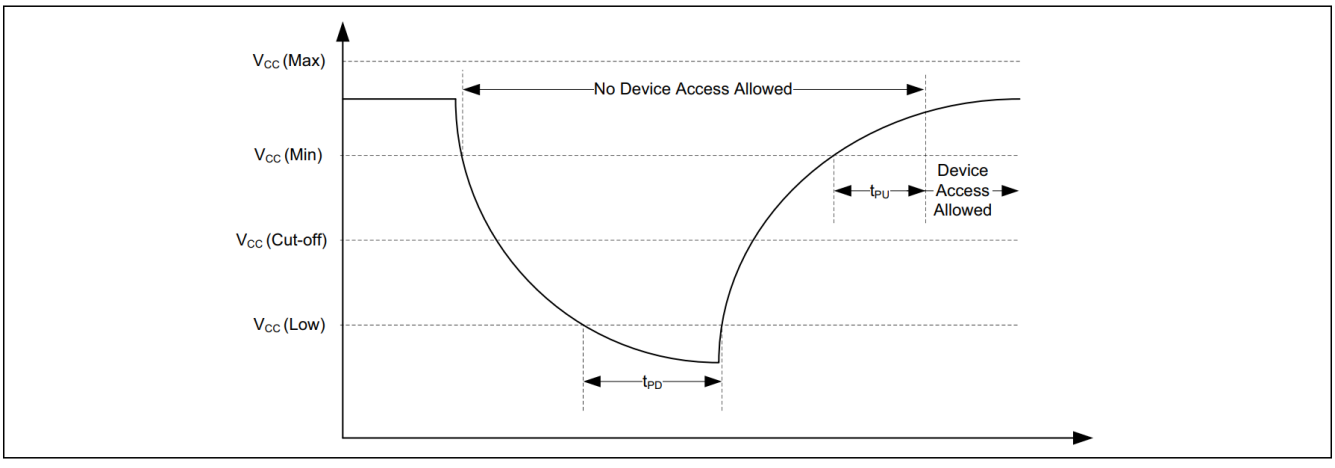


**图 62 下电或电压下降**

### 4.15.3 上电和下电顺序

为保证HL-T/HS-T设备可靠运行，需要遵循以下供电顺序：

- 在上电过程中， 先施加 $V_{CC}$，然后再施加 $V_{CCQ}$。在上电过程中，可以同时施加 $V_{CC}$ 和 $V_{CCQ}$，只要 $V_{CCQ}$ 不超过 $V_{CC}$。
- 在下电模式期间，先降低 $V_{CCQ}$ ，再降低 $V_{CC}$。下电期间可以同时降低 $V_{CC}$和 $V_{CCQ}$，只要 $V_{CCQ}$不超过 $V_{CC}$。
- 建议保持 $V_{CCQ} \leq V_{CC}$。

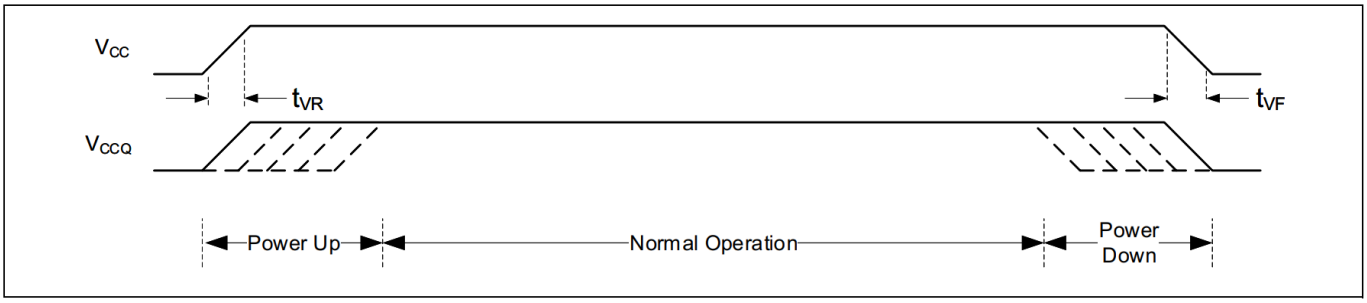


**图 63 上电和下电时序**

# 5 寄存器

寄存器是一小组存储单元，用于配置和报告器件操作的状态。HL-T/HS-T 系列器件使用单独的非易失性和易失性存储组来实现不同的寄存器位类型，以实现传统版兼容性和新功能。每个寄存器都由一组易失性位和关联的非易失性位（如果需要持久性）组成。在上电、硬件复位或软件复位期间，寄存器非易失性位中的数据将传输到易失性位，以提供易失性位的默认状态。将新数据写入寄存器的非易失性位时，易失性位也会使用新数据进行更新。但是，将新数据写入易失性寄存器位时，非易失性位将保留旧数据。寄存器结构如图 64所示。

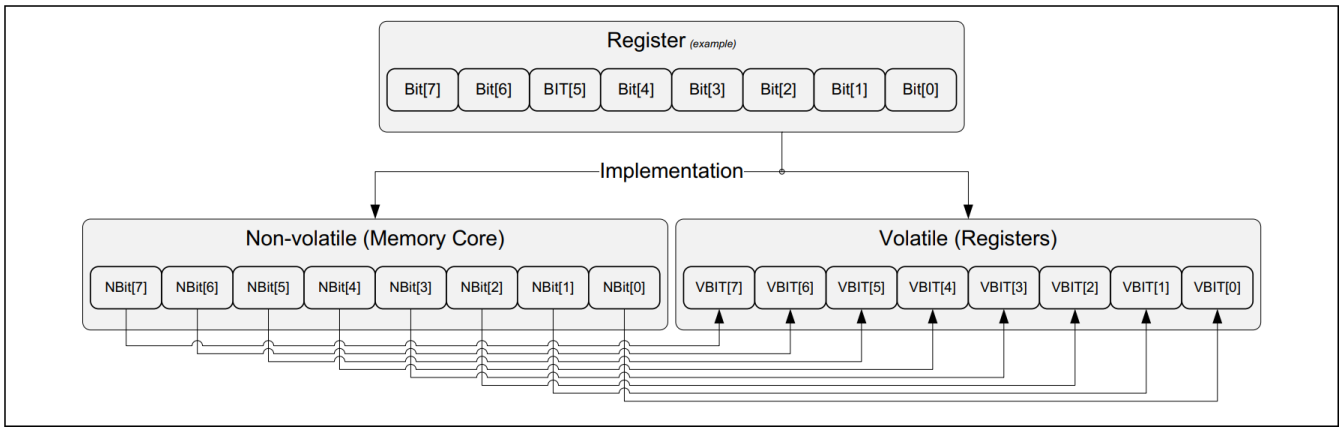


**图 64 寄存器结构**

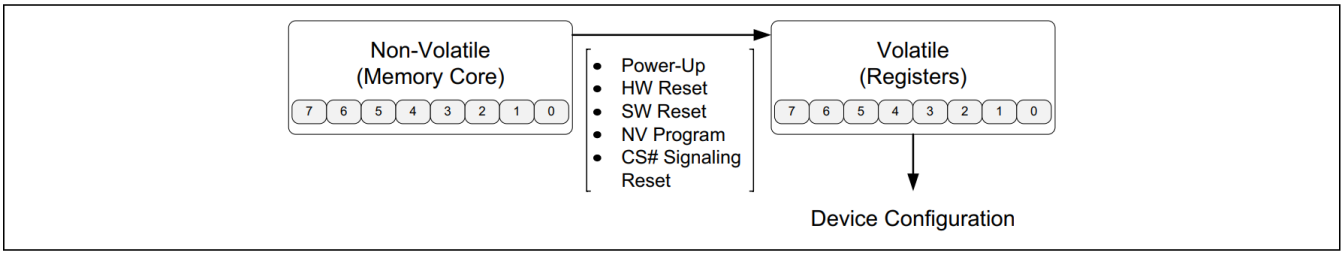


**图 65 寄存器组件内的数据移动**

## 5.1 寄存器命名规则

**表 46 寄存器位描述规则**

| Bit number | Name | Function | Read/write | Factory default (binary) | Description |
|---|---|---|---|---|---|
| REGNAME#T[x]<br>T = N, V, O<br><br>Descending order | – | – | Possible options:<br>N/A - Not applicable R - Readable only R/W - Readable and writable<br>R/1 - Readable and OTP | Possible options: 0<br>1 | Format:<br>Description of the configuration bit<br><br>Options:<br>0 = Option ‘0’ selection of the bit<br>1 = Option ‘1’ selection of the bit<br><br>Dependency: Is this bit part of a function which requires multiple bits for implementation? |

## 5.2 状态寄存器 1 (STR1x)

状态寄存器 1 包含状态位和控制位。 表 47描述了所支持的状态寄存器 1 类型的功能。

**表 47 状态寄存器 1**[22]

| Bit number | Name | Function | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| STR1N[7]<br>STR1V[7] | RESRVD | Reserved for Future Use | N->R<br>V->R | 0 | This bit is Reserved for future use. This bit must always be written/loaded to its default state. |
| STR1V[6] | PRGERR | Programming Error Status Flag | V -> R | 0 | Description: The PRGERR bit indicates program operation success or failure. When the PRGERR bit is set to a ‘1’, it indicates that there was an error in the last programming operation.<br>PRGERR bit is also set when a program operation is attempted within a protected memory region.<br>When PRGERR is set, it can only be cleared with the Clear Program and Erase Failure Flags (CLPEF_0_0) transaction or a hardware/software reset.<br>**Note** The device will only go to standby mode once the PRGERR flag is cleared.<br>Selection Options:<br>0 = Last programming operation was successful<br>1 = Last programming operation was unsuccessful<br>Dependency: N/A |

**注释：**

22. POR、硬件复位、软件复位、DPD 退出和 CS# 信号复位期间的 STR1x 值无效。

**表 47　　状态寄存器 1[22]（续）**

| Bit number | Name | Function | Read/Write N = Non-volatile V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| STR1V[5] | ERSERR | Erasing Error Status Flag | V -> R | 0 | Description: The ERSERR bit indicates erase operation success or failure.<br>When the ERSERR bit is set to a '1', it indicates that there was an error in the last erasing operation. ERSERR bit is also set when a erase operation is attempted within a protected memory sector. When ERSERR is set, it can only be cleared with the Clear Program and Erase Failure Flags (CLPEF_0_0) transaction or a hardware/software reset.<br>**Note** The device will only go to standby mode once the ERSERR flag is cleared.<br>Selection Options:<br>0 = Last erase operation was successful<br>1 = Last erase operation was unsuccessful<br>Dependency: N/A |
| STR1N[4:2]<br>STR1V[4:2] | LBPROT [2:0] | Legacy Block Protection based Memory Array size selection | If PLPROT = 0<br>N -> R/W<br>V -> R/W<br><br>If PLPROT = 1<br>N -> R<br>V -> R | 000 | Description: The LBPROT[2:0] bits define the memory array size to be protected against program and erase transactions. Based on the LBPROT[2:0] configuration, either top 1/64, 1/4, 1/2, etc. or bottom 1/64, 1/4, 1/2, etc., or up to the entire array is protected.<br>**Note** If PLPROT bit - Permanent Locking selection of Legacy Block Protection and 4KB Sector Architecture (CFR1x[4]) is set to a '1', the LBPROT[2:0] bits cannot be erased or programmed.<br>Selection Options:<br>000 = Protection is disabled<br>001 = 1/64th of the (top/bottom) array protection is enabled<br>010 = 1/32nd of the (top/bottom) array protection is enabled<br>…..<br>111 = All sectors are protected<br>Dependency: TBPROT (CFR1x[5]) |

**注释：**

22.POR、硬件复位、软件复位、DPD 退出和 CS# 信号复位期间的 STR1x 值无效。

**表 47　　状态寄存器 1[22]（续）**

| Bit number | Name | Function | Read/Write N = Non-volatile V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| STR1V[1] | WRPGEN | Write/Program Enable Status Flag | V -> R | 0 | Description:<br>The WRPGEN bit must be set to '1' to enable all program, erase or register write operations - it provides protection against inadvertent changes to memory or register values. The Write Enable (WRENB_0_0) transaction set the WRPGEN bit to '1' to allow program, erase or write transactions to execute. The Write Disable (WRDIS_0_0) transaction resets WRPGEN to a '0' to prevent all program, erase, and write transactions from execution. The WRPGEN bit is cleared to '0' at the end of any successful program, erase or register write operation. After a power down / power up sequence or a hardware/software reset, the Deep Power Down WRPGEN bit is cleared to '0'.<br>Selection Options:<br>0 = Program, erase or register write is disabled<br>1 = Program, erase or register write is enabled<br>Dependency: N/A |
| STR1V[0] | RDYBSY | Device Ready/Busy Status Flag | V -> R | 0 | Description:<br>The RDYBSY bit indicates whether the device is performing an embedded operation or is in standby mode ready to receive new transactions.<br>**Note** The PRGERR and ERSERR status bits are updated while RDYBSY is set. If PRGERR or ERSERR are set, the RDYBSY bit will remain set indicating the device is busy and unable to receive new transactions. A Clear Program and Erase Failure Flags (CLPEF_0_0) transaction must be executed to return the device to standby mode.<br>Selection Options:<br>0 = Device is in standby mode ready to receive new operation transactions<br>1 = Device is busy and unable to receive new operation transactions<br>Dependency: N/A |

**注释：**

22. POR、硬件复位、软件复位、DPD 退出和 CS# 信号复位期间的 STR1x 值无效。

寄存器

**表 48 PRGERR 汇总**

| Error flag | Symbol | Conditions |
|---|---|---|
| Program Error | PRGERR | Bits cannot be programmed ‘1’ to ‘0’ |
| | | Trying to program in a protected region |
| | | If ASP0[2] or ASP0[1] is 0, any non-volatile register write attempting to change the value of CFR1N[6:2]/CFR1V[6:2] |
| | | After the Password Protection Mode is selected and ASP Password Register update transaction executed |
| | | SafeBoot Failure |
| | | Configuration Failure |

**表 49 ERSERR 汇总**

| Error flag | Symbol | Conditions |
|---|---|---|
| Erase Error | ERSERR | Sector Device Erase - All bits cannot be erased to ‘1’s |
| | | Trying to erase a protected region |
| | | Register Erase - All bits cannot be erased to ‘1’s during Erase portion of Register Write |
| | | SafeBoot Failure |

## 5.3 状态寄存器 2 (STR2x)

状态寄存器 2 提供器件操作状态。表50描述了支持的状态寄存器2 类型的功能。

**表 50 状态寄存器 2** [23]

| Bit number | Name | Function | Read/Write N = Non-volatile V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| STR2V[7:5] | RESRVD | Reserved for Future Use | V -> R | 0 | This bit is Reserved for future use. This bit must always be written/loaded to its default state. |
| STR2V[4] | DICRCS | Memory Array Data Integrity Cyclic Redundancy Check Suspend Status Flag | V -> R | 0 | Description: The DICRCS bit is used to determine when the device is in Memory Array Data Integrity Cyclic Redundancy Check suspend mode.<br>Selection Options:<br>0 = Memory Array Data Integrity Cyclic Redundancy Check is not in suspend mode<br>1 = Memory Array Data Integrity Cyclic Redundancy Check is in suspend mode<br>Dependency: N/A |
| STR2V[3] | DICRCA | Memory Array Data Integrity Cyclic Redundancy Check Abort Status Flag | V -> R | 0 | Description: The DICRCA bit indicates that the Memory Array Data Integrity CRC calculation operation was aborted. The abort condition is based on ending address (ENDADD) and starting address (STRADD) relationship. If ENDADD < STRADD + 3, then DICRCA will be set and the device will return to the Standby state. DICRCA flag gets cleared at the next Data Integrity CRC calculation operation when ENDADD ≥ STRADD + 3.<br>Selection Options:<br>0 = Memory Array Data Integrity CRC calculation Is not aborted<br>1 = Memory Array Data Integrity CRC calculation is aborted<br>Dependency: N/A |
| STR2V[2] | SESTAT | Sector Erase Success/Failure Status Flag | V -> R | 0 | Description: The SESTAT bit indicates whether the erase operation on the sector completed successfully. Evaluate Erase Status transaction (EVERS_4_0) must be executed prior to reading SESTAT bit which specifies the sector address.<br>Selection Options:<br>1 = Addressed sector (EVERS_4_0) was erased successfully<br>0 = Addressed sector (EVERS_4_0) was not erased successfully<br>Dependency: N/A |

寄存器

**表 50　　状态寄存器 2 [23] （续）**

| Bit number | Name | Function | Read/Write N = Non-volatile V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| STR2V[1] | ERASES | Erase operation Suspend Status Flag | V -> R | 0 | Description: The ERASES bit is used to indicate if the Erase operation is suspended.<br>Selection Options:<br>0 = Erase operation is not in suspend mode<br>1 = Erase operation is in suspend mode<br>Dependency: N/A |
| STR2V[0] | PROGMS | Program operation Suspend Status Flag | V -> R | 0 | Description: The PROGMS bit is used to indicate if the Program operation is suspended.<br>Selection Options:<br>0 = Program operation is not in suspend mode<br>1 = Program operation is in suspend mode<br>Dependency: N/A |

**注释：**

23. POR、硬件复位、软件复位、DPD 退出和 CS# 信号复位期间的 STR2x 值无效。
仅当 STR1V[0] / RDYBSY = 0 时，STR2x 位才有效。

## 5.4 配置寄存器 1 (CFR1x)

配置寄存器 1 控制接口和数据保护功能。

**表 51 配置寄存器 1**

| Bit number | Name | Function | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| CFR1N[7]<br>CFR1V[7] | RESRVD | Reserved for Future Use | N -> R/W<br>V -> R/W | 0 | This bit is Reserved for future use. This bit must always be written/loaded to its default state. |
| CFR1N[6]<br>CFR1V[6] | SP4KBS | Split 4 KB Sectors selection between top and bottom address space | If PLPROT = 0<br>N -> R/W<br>V -> R<br><br>If PLPROT = 1<br>N -> R<br>V -> R | 0 | Description: The SP4KBS bit selects whether the 4 KB sectors are grouped together or evenly split between High and LOW address ranges.<br>Selection Options:<br>0 = 4 KB Sectors are grouped together<br>1 = 4 KB Sectors are split between High and Low Addresses Dependency: TB4KBS(CFR1N[2]) |
| CFR1N[5]<br>CFR1V[5] | TBPROT | Top or Bottom Protection selection for Legacy Protection Mode | If PLPROT = 0<br>N -> R/W<br>V -> R<br><br>If PLPROT = 1<br>N -> R<br>V -> R | 0 | Description: The TBPROT bit selects the reference point of the Legacy Block Protection bits (LBPROT[2:0]) in the Status Register on whether the protection starts from the top or starts from the bottom of the address range.<br>The bit also selects a memory address range (lowest or highest) to remain readable is available for reading during Read Password Protection mode even before a successful Password entry is completed.<br>Selection Options:<br>0 = Legacy Protection is applicable in the top half of the address range<br>1 = Legacy Protection is applicable in the bottom half of the address range Dependency: LBPROT[2:0] (STR1x[3:1]) |

**表 51　　配置寄存器 1（续）**

| Bit number | Name | Function | Read/Write N = Non-volatile V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| CFR1N[4]<br>CFR1V[4] | PLPROT | Permanent Locking selection of Legacy Block Protection and 4 KB Sector Architecture | N -> R/1<br>V -> R | 0 | Description: The PLPROT bit permanently protects the Legacy Block Protection and<br>4 KB Sector location. It thereby permanently protects the memory array protection scheme and sector architecture.<br>**Note** PLPROT protects LBPROT[2:0], SP4KBS, TBPROT, and TB4KBS bits from program and erase, and it is recommended to configure these bits before configuring the PLPROT bit.<br>Selection Options:<br>0 = Legacy Block Protection and 4 KB Sector Location are not protected<br>1 = Legacy Block Protection and 4 KB Sector Location are protected<br>Dependency: N/A |
| CFR1N[3]<br>CFR1V[3] | RESRVD | Reserved for Future Use | N -> R/W<br>V -> R/W | 0 | This bit is Reserved for future use. This bit must always be written/loaded to its default state. |
| CFR1N[2]<br>CFR1V[2] | TB4KBS | Top or Bottom Address Range selection for 4 KB Sector Block | If PLPROT = 0<br>N -> R/W<br>V -> R<br><br>If PLPROT = 1<br>N -> R<br>V -> R | 0 | Description:<br>The TB4KBS bit defines the logical address location of the 4 KB sector block. The 4 KB sector block replaces the fitting portion of the highest or lowest address sector.<br>Selection Options:<br>0 = 4 KB Sector Block is in the bottom of the memory address space<br>1 = 4 KB Sector Block is in the top of the memory address space<br>Dependency: SP4KBS (CFR1x[6]) |

**表 51　　配置寄存器 1（续）**

| Bit number | Name | Function | Read/Write N = Non-volatile V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| CFR1N[1] CFR1V[1] | RESRVD | Reserved for Future Use | N -> R/W V -> R/W | 0 | This bit is Reserved for future use. This bit must always be written/loaded to its default state. |
| CFR1N[0] CFR1V[0] | TLPROT | Temporary Locking selection of Legacy Block Protection and Sector Archi-tecture | N -> R V -> R/W | 0 | Description: The TLPROT bit temporarily protects the Legacy Block Protection and 4 KB Sector location. Upon power-up or a hardware reset, TLPROT is set to its default state. When selected, it protects the memory array protection scheme and sector archi- tecture from any changes. **Note** TLPROT protects LBPROT[2:0], SP4KBS, TBPROT, and TB4KBS bits from program and erase. Selection Options: 0 = Legacy Block Protection and 4 KB Sector Location are not protected 1 = Legacy Block Protection and 4 KB Sector Location are temporarily protected Dependency: N/A |

**表 52　　4KB参数扇区位置选择**

| SP4KBS | TB4KBS | 4 KB location |
|---|---|---|
| 0 | 0 | 4KB physical sectors at bottom (Low address) |
| 0 | 1 | 4KB physical sectors at top, (High address) |
| 1 | X | 4KB Parameter sectors are split between top (High Address) and bottom (Low Address) |

**表 53　　PLPROT 和 TLPROT 保护**

| PLPROT | TLPROT | Array protection and 4K sector |
|---|---|---|
| 0 | 0 | Unprotected (Unlocked) |
| 1 | X | TBPROT, LBPROTx, SP4KBS, TB4KBS - Permanently Protected (Locked) |
| 0 | 1 | TBPROT, LBPROTx, SP4KBS, TB4KBS - Protected (Locked) till next Power-down |

## 5.5 配置寄存器 2 (CFR2x)

配置寄存器 2 控制存储器读取延迟和地址字节长度选择。

**表 54 配置寄存器 2**

| Bit number | Name | Function | Read/Write N = Non-volatile V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| CFR2N[7] CFR2V[7] | ADRBYT | Address Byte Length selection between 3 or 4 bytes for Instructions | N -> R/W V -> R/W | 0 | Description: The ADRBYT bit controls the expected address length for all instructions that require address and is selectable between 3 Bytes or 4 Bytes.<br><br>Selection Options:<br>0 = Instructions will use 3 Bytes for address<br>1 = Instructions will use 4 Bytes for address<br><br>Dependency: N/A |
| CFR2N[6:4] CFR2V[6:4] | RESRVD | Reserved for Future Use | N -> R/W V -> R/W | 000 | These bits are Reserved for future use. This bit must always be written/loaded to its default state. |
| CFR2N[3:0] CFR2V[3:0] | MEMLAT[3:0] | Memory Array Read Latency selection - Dummy cycles required for initial data access | N -> R/W V -> R/W | 1000 | Description: The MEMLAT[3:0] bits control the read latency (dummy cycles) delay in all variable latency memory array and non-volatile register read transactions. MEMLAT selection allows the user to adjust the read latency during normal operation based on different operating frequencies.<br>Selection Options:<br>0000 = 0/5 Latency Cycles Selection based on transaction opcodes<br>…..<br>1111 = 15/28 Latency Cycles Selection based on transaction opcodes<br>Dependency: N/A |

**表 55　　延迟编码（周期）与频率**[24, 25, 27]

| Latency code | Number of cycles (1-1-1, 1-1-8 / 8-8-8) | SDR SPI read transactions (MHz) (1S-1S-1S / 1S-1S-8S) | SDR octal read transactions (MHz) (8S-8S-8S) | DDR octal read transactions (MHz) (8D-8D-8D) |
|---|---|---|---|---|
| | | **RDAY2_C_0<br>RDSSR_4_0** [26]**<br>RDARG_C_0<br>RDECC_4_0<br>RDPPB_4_0<br>RDAY3_4_0** | **RDAY1_4_0<br>RDSSR_4_0<br>RDARG_4_0**[26]**<br>RDECC_4_0<br>RDPPB_4_0** | **RDAY2_4_0<br>RDSSR_4_0<br>RDARG_4_0**[26]**<br>RDECC_4_0<br>RDPPB_4_0** |
| 0000 | 0 / 5 | 50 | 50 | 42 |
| 0001 | 1 / 6 | 68 | 64 | 57 |
| 0010 | 2 / 8 | 81 | 92 | 85 |
| 0011 | 3 / 10 | 93 | 121 | 107 |
| 0100 | 4 / 12 | 106 | 150 | 121 |
| 0101 | 5 / 14 | 118 | 166 (HL-T) / 178 (HS-T) | 135 |
| 0110 | 6 / 16 | 131 | 200 | 150 |
| 0111 | 7 / 18 | 143 | 200 | 164 |
| 1000 | 8 / 20 | 156 | 200 | 166 (HL-T) / 178 (HS-T) |
| 1001 | 9 / 22 | 166 | 200 | 192 |
| 1010 | 10 / 23 | 166 | 200 | 200 |
| 1011 | 11 / 24 | 166 | 200 | 200 |
| 1100 | 12 / 25 | 166 | 200 | 200 |
| 1101 | 13 / 26 | 166 | 200 | 200 |
| 1110 | 14 / 27 | 166 | 200 | 200 |
| 1111 | 15 / 28 | 166 | 200 | 200 |

**注释：**

24. 使用 ECC 错误报告机制时，读取的输出数据必须至少为 2 个字节才能正确进行 ECC 报告。
25. HS-T系列器件不支持 CK 频率 > 200 MHz的SDR或 > 200 MHz的DDR。
    > 166 MHz SDR，
    或 > 166 MHz DDR 不被HL-T系列支持。
26. RDARG_C_0 和 RDARG_4_0 使用这些延迟周期来读取非易失性寄存器。
27. RSFDP_3_0 始终具有八个虚拟周期，并且不同接口的最大频率与八个虚拟周期有关。

## 5.6 配置寄存器 3 (CFR3x)

配置寄存器 3 控制命令传输行为。

**表 56 配置寄存器 3**

| Bit number | Name | Function | Read/Write N = Non-volatile V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| CFR3N[7:6] CFR3V[7:6] | VRGLAT[1:0] | Volatile Register Read Latency selection - Dummy cycles required for initial data access | N -> R/W V -> R/W | 00 | Description: The VRGLAT[1:0] bits control the read latency (dummy cycles) delay in all variable latency register read transactions. VRGLAT[1:0] selection allows the user to adjust the read latency during normal operation based on different operating frequencies. Selection Options: 00, 01, 10, 11 Latency Cycles Selection based on transaction opcodes Dependency: N/A |
| CFR3N[5] CFR3V[5] | BLKCHK | Blank Check selection during Erase operation for better endurance | N -> R/W V -> R/W | 0 | Description: When this feature is enabled an erase transaction first evaluates the erase status of the sector. If the sector is found to erased, the erase operation is aborted. In other words, the erase operation is only executed if programmed bits are found in the sector. Disabling BLKCHK executes an erase operation unconditionally. Selection Options: 0 = Blank Check is disabled before executing an erase operation 1 = Blank Check evaluation is enabled before executing an erase operation Dependency: N/A |
| CFR3N[4] CFR3V[4] | PGMBUF | Program Buffer Size selection | N -> R/W V -> R/W | 0 | Description: The PGMBUF bit selects the Programming Buffer size which is used for page programming. Program buffer size affects the device programming time. **Note** If programming data exceeds the program buffer size, data gets wrapped. Selection Options: 0 = 256 Byte Write Buffer Size 1 = 512 Byte Write Buffer Size Dependency: N/A |

**表 56　　配置寄存器 3（续）**

| Bit number | Name | Function | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| CFR3N[3]<br>CFR3V[3] | UNHYSA | Uniform or Hybrid Sector Architecture Selection | N -> R/W<br>V -> R | 0 | Description: The UNHYSA bit selects between uniform (all 256 KB sectors) or hybrid (4 KB sectors and 256 KB sectors) sector architecture. If hybrid sector architecture is selected, 4 KB sector block is made part of the main Flash array address map.<br>The 4 KB sector block can overlay at either the highest or the lowest address range of the device. If uniform sector architecture is selected, 4KB sector block is removed from the address map and all sectors are of uniform size. **Note** Hybrid sector architecture also enables 4 KB Sector Erase transaction (20h). Otherwise, 4 KB Sector Erase transaction, if issued, is ignored by the device.<br>Selection Options:<br>0 = Hybrid Sector Architecture (combination of 4 KB sectors and 256 KB sectors)<br>1 = Uniform Sector Architecture (all<br>256 KB sectors)<br>Dependency: SP4KBS(CFR1N[6]), TB4KBS(CFR1N[2]) |
| CFR3N[2]<br>CFR3V[2] | RESRVD | Reserved for Future Use | N -> R/W<br>V -> R/W | 0 | This bit is Reserved for future use. This bit must always be written/loaded to its default state. |
| CFR3N[1]<br>CFR3V[1] | RESRVD | Reserved for Future Use | N -> R/W<br>V -> R/W | 0 | |
| CFR3N[0]<br>CFR3V[0] | RESRVD | Reserved for Future Use | N -> R/W<br>V -> R/W | 0 | |

**表 57　　寄存器延迟编码（周期）与频率**[28, 29]

| Latency code | SDR SPI register transaction latency dummy cycles (1S-1S-1S)[30] | | | SDR octal register transactions latency dummy cycle (8S-8S-8S) | | DDR octal register transactions latency dummy cycle (8D-8D-8D) | |
|---|---|---|---|---|---|---|---|
| | Frequency | RDARG_C_0[31] RDDYB_4_0 | RDPLB_0_0 RDIDN_0_0 RDSR1_0_0 RDSR2_0_0 | Frequency | RDARG_4_0[31] RDPLB_4_0 RDDYB_4_0 RDIDN_4_0 RDSR1_4_0 RDSR2_4_0 | Frequency | RDARG_4_0[31] RDPLB_4_0 RDDYB_4_0 RDIDN_4_0 RDSR1_4_0 RDSR2_4_0 |
| 00 | 50 MHz | 0 | 0 | 50 MHz | 3 | 25 MHz | 3 |
| 01 | 133 MHz | 1 | 0 | 133 MHz | 4 | 66 MHz | 4 |
| 10 | 133 MHz | 1 | 1 | 166 MHz | 5 | 166 MHz (HL-T) / 200 MHz (HS-T) | 5 |
| 11 | 166 MHz | 2 | 2 | 200 MHz | 6 | 200 MHz | 6 |

**注释：**

28. RDUID_4_0 和 RDUID_0_0 始终具有 32 个周期的延迟。SDR SPI下的最大频率为 166 MHz，HS-T SDR /DDR 八线下为 200 MHz，HL-T SDR /DDR 八线下为 166 MHz。
29. RDCRC_4_0 始终具有 8 个周期的延迟。SDR SPI下的最大频率为 166 MHz，HS-T SDR /DDR 八线下为 200 MHz，HL-T SDR /DDR 八线下为 166 MHz。
30. CK 频率 > 166 MHz SDR，不受支持。
31. RDARG_C_0 和 RDARG_4_0 使用这些虚拟周期来读取易失性寄存器。

## 5.7 配置寄存器 4 (CFR4x)

配置4控制主要的闪存式存储器读取命令传输并发回卷行为和输出驱动阻抗。

**表 58 配置寄存器 4**

| Bit number | Name | Function | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| CFR4N[7:5]<br>CFR4V[7:5] | IOIMPD[2:0] | I/O Driver Output Impedance selection | N -> R/W<br>V -> R/W | 101 | Description: The IOIMPD[2:0] bits select the IO driver output impedance (drive strength). The output impedance configuration<br>bits adjust the drive strength during normal device operation to meet system signal integrity requirements.<br>Selection Options:<br>000 = 45 Ω<br>001 = 120 Ω<br>010 = 90 Ω<br>011 = 60 Ω<br>100 = 45 Ω<br>101 = 30 Ω (Factory Default)<br>110 = 20 Ω<br>111 = 15 Ω<br>Dependency: N/A |
| CFR4N[4]<br>CFR4V[4] | RBSTWP | Read Burst Wrap Enable selection | N -> R/W<br>V -> R/W | 0 | Description: The RBSTWP bit selects the read burst wrap feature. It allows the device to enter and exit burst wrapped read mode during normal operation. The wrap length is selected by RBSTWL[1:0] bits.<br>Selection Options:<br>0 = Read Wrapped Burst disabled<br>1 = Read Wrapped Burst enabled<br>Dependency: RBSTWL[1:0] (CFR4x[1:0]) |

**表 58　　配置寄存器 4 （续）**

| Bit number | Name | Function | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| CFR4N[3]<br>CFR4V[3] | ECC12S | Error Correction Code (ECC) 1-bit or 1-bit/2-bit error correction selection | N -> R/W<br>V -> R/W | 1 | Description: The ECC12S bit selects between 1-bit ECC error detection/correction or both 1-bit ECC error detection and correction and 2-bit ECC error detection. This configuration option affects Address Trap Register and ECC Counter Register functionalities as well. The host needs to erase and reprogram the data in the SEMPER™ Flash memory upon ECC configuration change (1-bit correction to 1-bit correction and 2-bit detection or vice versa).<br>Selection Options:<br>0 = 1-bit ECC Error Detection/Correction<br>1 = 1-bit ECC Error Detection/Correction and 2-bit ECC error detection<br>Dependency: N/A |
| CFR4N[2]<br>CFR4V[2] | DPDPOR | Deep Power Down power saving mode entry selection upon POR | N -> R/W<br>V -> R | 0 | Description: The DPDPOR bit selects if the device will be in either Deep Power Down (DPD) mode or the Standby mode after the completion of POR. If enabled, DPDPOR configures the device to start in DPD mode to reduce current consumption until the device is needed. If the device is in DPD, a pulse on CS# or a Hardware reset will return the device to Standby mode.<br>Selection Options:<br>0 = Standby mode is entered upon the completion of POR<br>1 = Deep Power Down Power mode is entered upon the completion of POR<br>Dependency: N/A |

**表 58　　配置寄存器 4 （续）**

| Bit number | Name | Function | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| CFR4N[1:0]<br>CFR4V[1:0] | RBSTWL[1:0] | Read Burst Wrap Length selection | N -> R/W<br>V -> R/W | 00 | Description: The RBSTWL[1:0] bits select the read burst wrap length and alignment during normal operation. It selects the fixed length/aligned group of 8-, 16-, 32-, or 64-bytes.<br>Selection Options:<br>00 = 8 Bytes Wrap length<br>01 = 16 Bytes Wrap length<br>10 = 32 Bytes Wrap length<br>11 = 64 Bytes Wrap length<br>Dependency: RBSTWP (CFR4x[4]) |

**表 59　　输出数据回卷序列**

| Wrap boundary (bytes) | Start address (Hex) | Address sequence (Hex) |
|---|---|---|
| Sequential | XXXXXX03 | 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18. |
| 8 | XXXXXX00 | 00, 01, 02, 03, 04, 05, 06, 07, 00, 01, 02. |
| 8 | XXXXXX07 | 07, 00, 01, 02, 03, 04, 05, 06, 07, 00, 01. |
| 16 | XXXXXX02 | 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 00, 01, 02, 03. |
| 16 | XXXXXX0C | 0C, 0D, 0E, 0F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E. |
| 32 | XXXXXX0A | 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F. |
| 32 | XXXXXX1E | 1E, 1F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 00. |
| 64 | XXXXXX03 | 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, 2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F 00, 01, 02. |
| 64 | XXXXXX2E | 2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D. |

## 5.8 配置寄存器 5 (CFR5x)

配置 5 控制八线接口器件的行为。

**表 60 配置寄存器 5**

| Bit number | Name | Function | Read/Write N = Non-volatile V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| CFR5N[7]<br>CFR5V[7] | RESRVD | Reserved for Future Use | N -> R/W<br>V -> R/W | 0 | These bits are Reserved for future use. This bit must always be written/loaded to its default state. |
| CFR5N[6]<br>CFR5V[6] | RESRVD | Reserved for Future Use | N -> R/W<br>V -> R/W | 1 | |
| CFR5N[5:2]<br>CFR5V[5:2] | RESRVD | Reserved for Future Use | N -> R/W<br>V -> R/W | 0000 | |
| CFR5N[1]<br>CFR5V[1] | SDRDDR | Octal SPI SDR or DDR selection | N -> R/W<br>V -> R/W | 0 | Description: The SDRDDR bit selects between SDR or DDR for all data transfers to the device. Based on SDRDDR selection, all transactions either are SDR or DDR.<br>**Note** SDRDDR bit only controls the interface for Octal mode (8-8-8).<br>Selection Options:<br>0 = SDR enabled<br>1 = DDR enabled<br>Dependency: N/A |
| CFR5N[0]<br>CFR5V[0] | OPI-IT | Octal Interface and Protocol Selection - I/O width set to 8 bits (8-8-8) | N -> R/W<br>V -> R/W | 0 | Description: The OPI-IT bit selects the I/O width of the device to be 8-bits wide. When configured to 8-bits (OPI-IT) all transactions require Opcode, Address and Data always sent on all eight I/Os.<br>Selection Options:<br>0 = Data Width set to 1 bit wide (1S-1S-1S) - Legacy Single SPI Protocol<br>1 = Data Width set to 8 wide (8S-8S-8S, 8D-8D-8D) - Octal Protocol<br>Dependency: N/A |

## 5.9 接口 CRC（循环冗余校验）使能寄存器 (ICEV)

接口 CRC（循环冗余校验）使能寄存器控制接口 CRC（循环冗余校验）功能的启用/禁用。

**表 61 接口 CRC（循环冗余校验）使能寄存器**

| Bit number | Name | Function | Read/Write N = Non-volatile V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| ICEV[7:1] | RESVRD | Reserved for Future Use | V -> R | 0000000 | This bit is Reserved for future use. This bit must always be written/loaded to its default state. |
| ICEV[0] | ITCRCE | Interface CRC Selection | V -> R/W | 0 | Description: The ITCRCE bit controls enabling/disabling of the Interface CRC function.<br>Selection Options:<br>0 = Interface CRC Enabled<br>1 = Interface CRC Disabled<br>Dependency: N/A |

## 5.10 接口 CRC（循环冗余校验）校验值寄存器（ICRV）

接口CRC（循环冗余校验）校验值寄存器（ICRV）存储指令上的CRC（循环冗余校验）计算结果和接口上的数据内容以进行保护。

**表 62 接口 CRC（循环冗余校验）校验值寄存器**

| Bit number | Name | Function | Read/Write N = Non-volatile V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| ICRV[31:0] | ITCRCV[31:0] | Interface CRC Checksum Value | V -> R | 0xFFFFFFFF | Description: The ITCRCV[31:0] bits store the check-value of the CRC process on the memory array data contained within the starting address and the ending address.<br>Selection Options: Checksum Value<br>Dependency: N/A |

## 5.11 存储阵列数据完整性校验 CRC（循环冗余校验）寄存器 (DCRV)

存储阵列数据完整性检查CRC（循环冗余校验）寄存器（DCRV）存储对指定起始地址和结束地址之间包含的数据进行CRC（循环冗余校验）计算的结果。

**表 63 存储阵列数据完整性校验 CRC（循环冗余校验）寄存器**

| Bit number | Name | Function | Read/Write N = Non-volatile V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| DCRV[31:0] | DTCRCV[31:0] | Memory Array Data CRC Checksum Value | V -> R | 0x00000000 | Description: The DTCRCV[31:0 bits store the checksum value of the CRC process on the memory array data contained within the starting address and the ending address.<br>Selection Options: Checksum Value<br>Dependency: N/A |

## 5.12 ECC 状态寄存器 (ESCV)

ECC 状态寄存器（ECSV）包含对单位数据执行的任何纠错操作的ECC状态，该数据的字节在上次读取期间被寻址。

**注释：**单位数据定义为计算ECC字节数。HL-T/HS-T系列设备有16字节（128位）单位数据。

**表 64 ECC 状态寄存器**

| Bit number | Name | Function | Read/Write N = Non-volatile V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| ECSV[7:5] | RESRVD | Reserved for Future Use | V -> R | 000 | This bit is Reserved for future use. This bit must always be written/loaded to its default state. |
| ECSV[4] | ECC2BT | ECC Error 2-bit Error Detection Flag | V -> R | 0 | Description: The ECC2BT bit indicates that a 2-bit ECC Error was detected in the data unit (16 bytes). A Clear ECC Status Register transaction (CLECC_0_0) will reset ECC2BT.<br>**Note** ECC2BT is updated every time any memory address is read and is sticky, i.e. once it is set, it remains set. The ECC2BT status is maintained until a Clear ECC Status Register transaction (CLECC_0_0) is executed.<br>**Note** ECC1BT is not valid if ECC2BT status flag is set.<br>Selection Options:<br>0 = No 2-Bit ECC Error was detected in the data unit (16 bytes)<br>1 = 2-bit ECC Error was detected in the data unit (16 bytes)<br>Dependency: CFR4x[3] |

**表 64　　ECC 状态寄存器（续）**

| Bit number | Name | Function | Read/Write N = Non-volatile V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| ECSV[3] | ECC1BT | ECC Error 1-bit Error Detection and Correction Flag | V -> R | 0 | Description: The ECC1BT bit indicates that a 1-bit ECC Error was detected and corrected in the data unit (16 bytes). A Clear ECC Status Register transaction (CLECC_0_0) will reset ECC1BT. **Note** ECC1BT is updated every time any memory address is read and is sticky, i.e. once it is set, it remains set. The ECC1BT status is maintained until a Clear ECC Status Register transaction (CLECC_0_0) is executed.<br>Selection Options:<br>0 = No 1-Bit ECC Error was detected in the data unit (16 bytes)<br>1 = 1-bit ECC Error was detected in the data unit (16 bytes)<br>Dependency: N/A |
| ECSV[2:0] | RESRVD | Reserved for Future Use | V -> R | 000 | This bit is Reserved for future use. This bit must always be written/loaded to its default state. |

## 5.13 ECC 地址捕获寄存器 (EATV)

ECC 地址捕获寄存器 (EATV) 用于存储读操作期间发生 1 位/2 位错误或仅发生 1 位错误的ECC单位数据的地址。它存储自上次清除ECC命令传输以来在存储器读取操作期间捕获的第一个ECC错误的ECC单位数据地址。

**表 65 ECC 地址捕获寄存器**

| Bit number | Name | Function | Read/Write N = Non-volatile V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| EATV[31:0] | ECCATP[31:0] | ECC 1-bit and 2-bit Error Address Trap Register | V -> R | 0x00000000 | Description: The Address Trap Register (ECCATP[31:0]) stores the ECC unit data address where a 1-Bit/2-Bit error occurred during a read operation. ECCATP[31:0] stores the ECC unit address of the first ECC error captured during a memory read operation since the last Clear ECC Status Register transaction (CLECC_0_0).<br>**Note** ECCATP[31:0] is only updated during Read Instruction.<br>**Note** Mask non-valid upper ECCATP address bits from ECC unit address.<br>**Note** Clear ECC Status Register transaction (CLECC_0_0), POR or Hardware/Software reset clears the EATV[31:0] to 0x00000000.<br>Selection Options: ECC Error Data Unit Address<br>Dependency: N/A |

## 5.14 ECC错误检测计数寄存器（ECTV）

ECC 错误检测计数寄存器 (ECTV) 存储自上次 POR 或硬件/软件复位以来读取操作期间发生的 1 位/2 位或仅 1 位 ECC 错误的数量。

**表 66 ECC 计数寄存器**

| Bit number | Name | Function | Read/Write N = Non-volatile V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| ECTV[15:0] | ECCCNT[15:0] | ECC 1-bit and 2-bit Error Count Register | V -> R | 0x0000 | Description: The ECCCNT[15:0] stores the number of 1-bit/2-bit ECC errors occurred during read operations since the last POR or hardware/software reset.<br>**Note** ECCCNT[15:0] is only updated during Read Instruction.<br>**Note** Only one ECC error is counted for each data unit. If multiple read transactions access the same unit data containing an ECC error, the ECCCNT[15:0] will increment each time the unit data is read.<br>**Note** Once the count reaches 0xFFFF, the ECCCNT[15:0] will stop incrementing.<br>**Note** POR or Hardware/Software reset clears the ECCNT[15:0] to 0x0000.<br>Selection Options: ECC Error Count<br>Dependency: N/A |

## 5.15 高级扇区保护寄存器 (ASPO)

ASP 寄存器（ASPO）配置高级扇区保护方式的行为。

**表 67 高级扇区保护寄存器**

| Bit number | Name | Function | Read/Write N = Non-volatile V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| ASPO[15:6] | RESRVD | Reserved for Future Use | N -> R/1 | 1111111111 | This bit is Reserved for future use. This bit must always be written/loaded to its default state. |
| ASPO[5] | ASPRDP | Read Password Based Protection Selection | N -> R/1 | 1 | Description: The ASPRDP bit selects the Read Password Mode Protection mode. Read Password Protection mode works in conjunction with Password Protection mode to protect all sectors from Read/Erase/Program. Based on TBPROT configuration bit (CFR1x[5]), either the top or bottom sector is available for reading.<br>Selection Options:<br>0 = Read Password Protection Mode is enabled<br>1 = Read Password Protection Mode is disabled<br>Dependency: TBPROT (CFR1x[5]) |
| ASPO[4] | ASPDYB | Dynamic Protection (DYB) for all sectors at power-up Selection | N -> R/1 | 1 | Description: The ASPDYB bit selects whether all DYB bits (sectors) are in the protected state following power-up or hardware reset. DYB bits will individually need to be reset to change sector protections.<br>Selection Options:<br>0 = DYB based sector protection enabled at power-up or hardware reset<br>1 = DYB based sector protection disabled at power-up or hardware reset<br>Dependency: N/A |
| ASPO[3] | ASPPPB | Permanent Protection (PPB) bits for all sectors programmability Selection | N -> R/1 | 1 | Description: The ASPPPB bit selects whether all PPB bits are one-time programmable making PPB sector protection permanent. **Note** ASPPPB disables PPB erase transaction (ERPPB_0_0).<br>Selection Options:<br>0 = PPB bits are one-time programmable<br>1 = PPB bits can be erased and programmed as desired<br>Dependency: N/A |

**表 67　　高级扇区保护寄存器（续）**

| Bit number | Name | Function | Read/Write N = Non-volatile V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| ASPO[2] | ASPPWD | Password Based Protection Selection | N -> R/1 | 1 | Description: The ASPPWD bit selects the Password Protection Mode. Password Protection mode protects all PPB bits till the correct password is entered. The ASPPWD can also be used in combination with the ASPRDP to protect all registers and all memory from erase/program and to protect sectors from being read as well till the correct password is provided - except for top or bottom sector which is available for reading based on TBPROT configuration bit (CFR1x[5]).<br>**Note** When ASPPWD is selected, ASPO[15:0], CFR1N[7:2] and PWDO[63:0] are protected against Write operations.<br>Selection Options:<br>0 = Password Protection Mode is enabled<br>1 = Password Protection Mode is disabled<br>Dependency: N/A |

表 67 高级扇区保护寄存器（续）

| Bit number | Name | Function | Read/Write N = Non-volatile V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| ASPO[1] | ASPPER | Persistent Protection Selection (Register Protection Selection) | N -> R/1 | 1 | Description: The ASPPER bit selects the Persistent Protection Mode. The Persistent Protection mode (ASPPER) protects the ASPO[15:0], CFR1x[6, 5, 4, 2] and CFR3x[3] registers from erase or program.<br>Selection Options:<br>0 = Persistent Protection Mode is enabled<br>1 = Persistent Protection Mode is disabled<br>Dependency: N/A |
| ASPO[0] | ASPPRM | Permanent Protection Selection | N -> R/1 | 1 | Description: The ASPPRM bit selects the Permanent Protection Mode. The Permanent Protection mode (ASPPRM) permanently protects the PPB bits from erase or program. ASPPRM bit should be programmed once all the PPB based sector protections are finalized.<br>**Note** Permanent protection is independent of the PPBLOCK bit. Selection Options:<br>0 = Permanent Protection Mode is enabled<br>1 = Permanent Protection Mode is disabled<br>Dependency: N/A |

## 5.16 ASP 密码寄存器 (PWDO)

ASP 密码寄存器 (PWDO) 用于永久定义密码。

**表格 68 密码寄存器**

| Bit number | Name | Function | Read/Write N = Non-volatile V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| PWDO[63:0] | PASWRD[63:0] | Password Register | N -> R/1 | 0xFFFFFFFFFFFFFFFF | Description: The PASWRD[63:0] permanently stores a password used in password protected modes of operation. When the Password Protection Mode is enabled, this register will output the undefined data upon read password request.<br>Selection Options: Password<br>Dependency: N/A |

## 5.17 ASP PPB 锁定寄存器 (PPLV)

ASP PPB 锁定寄存器 (PPLV) 中的 PPBLCK 位用于保护 PPB 位。

**表 69 ASP PPB 锁定寄存器**

| Bit number | Name | Function | Read/Write N = Non-volatile V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| PPLV[7:1] | RESVRD | Reserved for Future Use | V -> R | 0000000 | This bit is Reserved for future use. This bit must always be written/loaded to its default state. |
| PPLV[0] | PPBLCK | PPB Temporary Protection Selection | V -> R/W | 1, ASPO[2:1] | Description: The PPBLCK bit is used to temporarily protect all the PPB bits.<br><br>Selection Options:<br>1 = PPB Bits can be erased or programmed<br>0 = PPB bits are protected against erase or program till the next POR or hardware reset<br>Dependency: N/A |

## 5.18 ASP PPB 访问寄存器 (PPAV)

ASP PPB 访问寄存器 (PPAV) 用于提供每个扇区的 PPB 保护位的状态。

**表 70 ASP PPB 访问寄存器**

| Bit number | Name | Function | Read/Write N = Non-volatile V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| PPAV[7:0] | PPBACS[7:0] | Sector Based PPB Protection Status | N -> R/W | 11111111 | Description: The PPBACS[7:0] bits are used to provide the state of the individual sector's PPB bit.<br>Selection Options:<br>FF = PPB for the sector addressed by the Read PPB transaction (RDPPB_4_0) is 1, not protecting that sector from program or erase operations<br>00 = PPB for the sector addressed by the Read PPB transaction (RDPPB_4_0) is 0, protecting that sector from program or erase operations<br>Dependency: N/A |

## 5.19 ASP 动态功能块访问寄存器 (DYAV)

ASP DYB访问寄存器 (DYAV) 用于提供每个扇区的DYB保护位的状态。

**表 71 ASP DYB访问寄存器**

| Bit number | Name | Function | Read/Write N = Non-volatile V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| DYAV[7:0] | DYBACS[7:0] | Sector Based DYB Protection Status | V -> R/W | 11111111 | Description: The DYBACS[7:0] bits are used to provide the state of the individual sector's DYB bit.<br>Selection Options:<br>FF = DYB for the sector addressed by the Read DYB transaction (RDDYB_4_0) is 1, not protecting that sector from program or erase operations<br>00 = DYB for the sector addressed by the Read DYB transaction (RDDYB_4_0) is 0, protecting that sector from program or erase operations<br>Dependency: N/A |

## 5.20 自动启动寄存器 (ATBN)

自动启动寄存器 (ATBN) 提供了一种自动读取启动代码的方法，作为加电复位或硬件复位过程的一部分。

**表 72 自动启动寄存器**

| Bit number | Name | Function | Read/Write N = Non-volatile V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| ATBN[31:9] | STADR[22:0] | Starting Address Selection where AutoBoot will start reading data from | N -> R/W | 00000000000000000000000 | Description: The STADR[22:0] bits set the starting address from which the device will output the read data.<br>Selection Options: Address Bits<br>Dependency: N/A |
| ATBN[8:1] | STDLY[7:0] | AutoBoot Read Starting Delay Selection | N -> R/W | 00000000 | Description: The STDLY[7:0] bits specify the initial delay (clock cycles) needed by the host before it can accept data.<br>**Note** STDLY[7:0] = 0x00 is valid for SPI up to 50 MHz. STDLY[7:0] = 0x01 or higher is valid for SPI up to 166 MHz. STDLY[7:0] = 0x05 or higher is valid for HL-T Octal up to 166 MHz and HS-T Octal up to 200 MHz.<br>Selection Options: Address Bits<br>Dependency: N/A |
| ATBN[0] | ATBTEN | AutoBoot Feature Selection | N -> R/W | 0 | Description: The ATBTEN bit enables or disables the AutoBoot feature.<br>Selection Options:<br>0 = AutoBoot feature disabled<br>1 = AutoBoot feature enabled<br>Dependency: N/A |

## 5.21 扇区擦除计数寄存器（SECV）

扇区擦除计数寄存器 (SECV) 包含指定扇区已擦除的次数。

**表 73 扇区擦除计数寄存器**

| Bit number | Name | Function | Read/Write N = Non-volatile V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| SECV[23] | SECCPT | Sector Erase Count Corruption Status Flag | V -> R | 0x0 | Description: The SECCPT bit is used to determine if the reported sector erase count is corrupted and was reset.<br>**Note** If SECCPT is set due to count corruption, it will reset to 0 on the next successful erase operation on the selected sector.<br>Selection Options:<br>0 = Sector Erase Count is not corrupted and is valid<br>1 = Sector Erase Count is corrupted and is not valid<br>Dependency: N/A |
| SECV[22:0] | SECVAL[22:0] | Sector Erase Count Value | V -> R | 0x000000 | Description: The SECVAL[22:0] bits store the number of times a sector has been erased<br>Selection Options: Value<br>Dependency: N/A |

## 5.22 INT# 引脚配置寄存器 (INCV) - 仅八线

INT# 引脚配置寄存器 (INCV) 配置哪个内部事件将触发 INT# 输出引脚上的高电平到低电平跳变。

**注释**

- 当 INCV 禁止特定特性驱动 INT# 引脚时，它将阻止相应的 INSV 位被更新。
- 清除 INCV 中的某个位置对 INSV 没有影响，并且根据需要独立清零、复位 INSV 是系统的责任。

**表 74 中断配置寄存器**

| Bit number | Name | Function | Read/Write N = Non-volatile V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| INCV[7] | INTBEN | INT# pin Enable Selection | V -> R/W | 1 | Description: The INT# pin is an open-drain output used to indicate to the host system that an event has occurred within the memory device. The INTBEN bit enables or disables the functionality controlling INT# pin.<br>Selection Options:<br>0 = INT# pin functionality is enabled<br>1 = INT# pin functionality is disabled<br>Dependency: N/A |
| INCV[6:5] | RESRVD | Reserved for Future Use | V -> R/W | 11 | These bits are Reserved for future use. This bit must always be written/loaded to its default state. |
| INCV[4] | REYBSY | Ready/Busy Transition Selection | V -> R/W | 1 | Description: The REYBSY bit enables or disables whether device ready/busy state will transition INT#.<br>Selection Options:<br>0 = A Busy to Ready transition will cause a HIGH to LOW transition on the INT# output<br>1 = Ready/Busy transitions will not transition the INT# output<br>Dependency: N/A |
| INCV[3:2] | RESRVD | Reserved for Future Use | V -> R/W | 11 | These bits are Reserved for future use. This bit must always be written/loaded to its default state. |
| INCV[1] | ECC2BT | ECC 2-bit Error Detection Selection0 | V -> R/W | 1 | Description: The ECC2BT bit enables or disables whether a 2-bit ECC detection error will transition INT#.<br>Selection Options:<br>0 = 2-bit ECC detection will cause a HIGH to LOW transition the INT# output<br>1 = 2-bit ECC detection will not transition the INT# output<br>Dependency: N/A |

寄存器

**表 74　　中断配置寄存器（续）**

| Bit number | Name | Function | Read/Write N = Non-volatile V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| INCV[0] | ECC1BT | ECC 1-bit Error Detection and Correction Selection | V -> R/W | 1 | Description: The ECC1BT bit enables or disables whether a 1-bit ECC detection and correction error will transition INT#.<br>Selection Options:<br>0 = 1-bit ECC detection and correction will cause a HIGH to LOW transition the INT# output<br>1 = 1-bit ECC detection and correction will not transition the INT# output<br>Dependency: N/A |

## 5.23 INT# 引脚状态寄存器 (INSV) - 仅八线

INT# 引脚状态寄存器 (INSV) 指示自上次清除 ISR 以来发生了哪些内部事件。

**表75 中断状态寄存器**

| Bit number | Name | Function | Read/Write N = Non-volatile V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| INSV[7:5] | RESRVD | Reserved for Future Use | V -> R/W | 111 | These bits are Reserved for future use. This bit must always be written/loaded to its default state. |
| INSV[4] | REYBSY | Ready/Busy Transition | V -> R/W | 1 | Description: The REYBSY bit indicates whether the device's ready/busy status has caused a transition on INT#.<br>Selection Options:<br>0 = A Busy to Ready transition has occurred<br>1 = A Busy to Ready transition has not occurred<br>Dependency: N/A |
| INSV[3:2] | RESRVD | Reserved for Future Use | V -> R/W | 11 | These bits are Reserved for future use. This bit must always be written/loaded to its default state. |
| INSV[1] | ECC2BT | ECC 2-bit Error Detection | V -> R/W | 1 | Description: The ECC2BT bit indicates whether a 2-bit ECC detection error has caused a transition on INT#.<br>Selection Options:<br>0 = 2-bit error detection has occurred<br>1 = 2-bit error detection has not occurred<br>Dependency: N/A |
| INSV[0] | ECC1BT | ECC 1-bit Error Detection and Correction | V -> R/W | 1 | Description: The ECC1BT bit indicates whether a 1-bit ECC correction error has caused a transition on INT#.<br>Selection Options:<br>0 = 1-bit error correction has occurred<br>1 = 1-bit error correction has not occurred<br>Dependency: N/A |

## 5.24 Endurance Flex 架构选择寄存器 (EFXx)

英飞凌 Endurance Flex 架构选择寄存器 (EFXx) 根据四个指针架构来定义长保留/高耐久性区域。

**表 76 Endurance Flex 架构选择寄存器（指针 4）**

| Bit number | Name | Function | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| EFX4O[10:2] | EPTAD4[8:0] | Endurance Flex Pointer 4 Address Selection | N -> R/1 | 111111111 | Description: The EPTAD4[8:0] bits define the 9-bit address of the beginning sector from where the long retention / high endurance region is defined.<br>Selection Options: Pointer Address<br>Dependency: N/A |
| EFX4O[1] | ERGNT4 | Endurance Flex Pointer 4 based Region Type Selection | N -> R/1 | 1 | Description: The ERGNT4 bit defines whether the region is long retention or high endurance.<br>Selection Options:<br>0 = Long Retention Sectors<br>1 = High Endurance Sectors<br>Dependency: N/A |
| EFX4O[0] | EPTEB4 | Endurance Flex Pointer 4 Enable# Selection | N -> R/1 | 1 | Description: The EPTEN4 bit define whether the wear leveling pointer is enabled/disabled.<br>Selection Options:<br>0 = Pointer Address Enabled<br>1 = Pointer Address Disabled<br>Dependency: N/A |

**表 77 Endurance Flex 架构选择寄存器（指针 3）**

| Bit number | Name | Function | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| EFX3O[10:2] | EPTAD3[8:0] | Endurance Flex Pointer 3 Address Selection | N -> R/1 | 111111111 | Description: The EPTAD3[8:0] bits define the 9-bit address of the beginning sector from where the long retention / high endurance region is defined.<br>Selection Options: Pointer Address<br>Dependency: N/A |

寄存器

**表 77　　Endurance Flex 架构选择寄存器（指针 3）（续）**

| Bit number | Name | Function | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| EFX3O[1] | ERGNT3 | Endurance Flex Pointer 3 based Region Type Selection | N -> R/1 | 1 | Description: The ERGNT3 bit defines whether the region is long retention or high endurance.<br>Selection Options:<br>0 = Long Retention Sectors<br>1 = High Endurance Sectors<br>Dependency: N/A |
| EFX3O[0] | EPTEB3 | Endurance Flex Pointer 3 Enable# Selection | N -> R/1 | 1 | Description: The EPTEN3 bit define whether the wear leveling pointer is enabled/disabled.<br>Selection Options:<br>0 = Pointer Address Enabled<br>1 = Pointer Address Disabled<br>Dependency: N/A |

**表 78　　Endurance Flex 架构选择寄存器（指针 2）**

| Bit number | Name | Function | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| EFX2O[10:2] | EPTAD2[8:0] | Endurance Flex Pointer 2 Address Selection | N -> R/1 | 111111111 | Description: The EPTAD2[8:0] bits define the 9-bit address of the beginning sector from where the long retention / high endurance region is defined.<br>Selection Options: Pointer Address<br>Dependency: N/A |
| EFX2O[1] | ERGNT2 | Endurance Flex Pointer 2 based Region Type Selection | N -> R/1 | 1 | Description: The ERGNT2 bit defines whether the region is long retention or high endurance.<br>Selection Options:<br>0 = Long Retention Sectors<br>1 = High Endurance Sectors<br>Dependency: N/A |
| EFX2O[0] | EPTEB2 | Endurance Flex Pointer 2 Enable# Selection | N -> R/1 | 1 | Description: EPTEN2 bit define whether the wear leveling pointer is enabled/disabled.<br>Selection Options:<br>0 = Pointer Address Enabled<br>1 = Pointer Address Disabled<br>Dependency: N/A |

**表 79　　Endurance Flex 架构选择寄存器（指针 1）**

| Bit number | Name | Function | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| EFX1O[10:2] | EPTAD1[8:0] | Endurance Flex Pointer 1 Address Selection | N -> R/1 | 111111111 | Description: The EPTAD1[8:0] bits define the 9-bit address of the beginning sector from where the long retention / high endurance region is defined.<br>Selection Options: Pointer Address<br>Dependency: N/A |
| EFX1O[1] | ERGNT1 | Endurance Flex Pointer 1 based Region Type Selection | N -> R/1 | 1 | Description: The ERGNT1 bit defines whether the region is long retention or high endurance.<br>Selection Options:<br>0 = Long Retention Sectors<br>1 = High Endurance Sectors<br>Dependency: N/A |

**表 79　　Endurance Flex 架构选择寄存器（指针 1）（续）**

| Bit number | Name | Function | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| EFX1O[0] | EPTEB1 | Endurance Flex Pointer 1 Enable# Selection | N -> R/1 | 1 | Description: The EPTEN1 bit define whether the wear leveling pointer is enabled/disabled.<br>Selection Options:<br>0 = Pointer Address Enabled<br>1 = Pointer Address Disabled<br>Dependency: N/A |

**表 80　　Endurance Flex 架构选择寄存器 (指针 0)**

| Bit number | Name | Function | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default (binary) | Description |
|---|---|---|---|---|---|
| EFX0O[1] | GBLSEL | All Sectors based Region type Selection | N -> R/1 | 1 | Description: The MbLSEL bit defines whether all sectors are defined as long retention region or high endurance region.<br>**Note** If all other pointer registers are disabled, this bit defines the behavior of the entire memory space and is hardwired to start at Sector 0.<br>Selection Options:<br>0 = Long Retention Sectors<br>1 = High Endurance Sectors<br>Dependency: N/A |
| EFX0O[0] | WRLVEN | Wear Leveling Enable Selection | N -> R/1 | 1 | Description: The WRLVEN bit enables/disables the wear leveling feature.<br>Selection Options:<br>0 = Wear Leveling Disabled<br>1 = Wear Leveling Enabled<br>Dependency: N/A |

# 6 命令传输表

## 6.1 SPI（1S-1S-1S）命令传输表

### 表 81 SPI（1S-1S-1S）命令传输表

| Function | Transaction name | Description | Prerequisite transaction | Byte 1 (Hex) | Byte 2 (Hex) | Byte 3 (Hex) | Byte 4 (Hex) | Byte 5 (Hex) | Byte 6 (Hex) | Byte 7 (Hex) | Byte 8 (Hex) | Byte 9 (Hex) | Transaction format | Max frequency (MHz) | Address length |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Read device ID | RDIDN_0_0 | **Read manufacturer and device identification** transaction provides read access to manufacturer and device identification. | - | 9F (CMD) | - | - | - | - | - | - | - | - | **Figure 11** | 166 | N/A |
| | RSFDP_3_0 | **Read JEDEC Serial Flash Discoverable Parameters** transaction sequentially accesses the Serial Flash Discovery Parameters (SFDP). | - | 5A (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | **Figure 12** | | 3 |
| | RDUID_0_0 | **Read Unique ID** accesses a factory programmed 64-bit number which is unique to each device. | - | 4C (CMD) | - | - | - | - | - | - | - | - | **Figure 11** | | N/A |
| Register access | RDSR1_0_0 | **Read Status Register 1** transaction allows the Status Register 1 contents to be read from DQ1/SO. | - | 05 (CMD) | - | - | - | - | - | - | - | - | | | N/A |
| | RDSR2_0_0 | **Read Status Register-2** transaction allows the Status Register-2 contents to be read from DQ1/SO. | - | 07 (CMD) | - | - | - | - | - | - | - | - | | | |
| | RDARG_C_0 | **Read Any Register** transaction provides a way to read all addressed non-volatile and volatile device registers. | - | 65 (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | **Figure 12** | | 3 |
| | | | - | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | | | 4 |
| | WRENB_0_0 | **Write Enable** sets the Write Enable Latch bit of the Status Register 1 to 1 to enable write, program and erase transactions. | - | 06 (CMD) | - | - | - | - | - | - | - | - | **Figure 6** | | N/A |
| | WRDIS_0_0 | **Write Disable** sets the Write Enable Latch bit of the Status Register 1 to 0 to disable write, program and erase transactions execution. | - | 04 (CMD) | - | - | - | - | - | - | - | - | | | |
| | WRARG_C_1 | **Write Any Register** transaction provides a way to write all addressed non-volatile and volatile device registers. | WRENB_0_0 | 71 (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Input Data [7:0] | - | - | - | - | **Figure 9** | | 3 |
| | | | | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Input Data [7:0] | - | - | - | | | 4 |

## 表 81 SPI（1S-1S-1S）命令传输表（续）

| Function | Transaction name | Description | Prerequisite transaction | Byte 1 (Hex) | Byte 2 (Hex) | Byte 3 (Hex) | Byte 4 (Hex) | Byte 5 (Hex) | Byte 6 (Hex) | Byte 7 (Hex) | Byte 8 (Hex) | Byte 9 (Hex) | Transaction format | Max frequency (MHz) | Address length |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Register access | CLPEF_0_0 | **Clear Program and Erase Failure Flags** transaction resets STR1V[5] (Erase failure flag) and STR1V[6] (Program failure flag). | - | 82 (CMD) | - | - | - | - | - | - | - | - | **Figure 6** | 166 | N/A |
| | EN4BA_0_0 | **Enter 4 Byte Address Mode** transaction sets the Address Length bit CFR2V[7] to 1 | | B7 (CMD) | | | | | | | | | | | |
| | EX4BA_0_0 | Exit 4 Byte Address Mode transaction sets the Address Length bit CFR2V[7] to 0 | | B8 (CMD) | | | | | | | | | | | |
| ECC | RDECC_4_0 | **Read ECC Status** is used to determine the ECC status of the addressed data unit. | - | 19 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | **Figure 12** | 166 | 4 |
| | CLECC_0_0 | **Clear ECC Status Register** transaction resets ECC Status Register bit[4] (2-bit ECC Detection), ECC Status Register bit[3] (1-bit ECC Correction), Address Trap Register and ECC Detection Counter. | - | 1B (CMD) | - | - | - | - | - | - | - | - | **Figure 6** | | N/A |
| CRC | DICHK_4_1 | **Data Integrity Check** transaction causes the device to perform a Data Integrity Check over a user defined address range. | - | 5B (CMD) | Start ADDR [31:24] | Start ADDR [23:16] | Start ADDR [15:8] | Start ADDR [7:0] | End ADDR [31:24] | End ADDR [23:16] | End ADDR [15:8] | End ADDR [7:0] | **Figure 8** | | 4 |
| Read flash array | RDAY1_C_0 | **Read** transaction reads out the memory contents at the given address. The maximum CK frequency for this transaction is 50MHz frequency. | - | 03 (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | **Figure 13** | 50 | 3 |
| | | | - | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | | | 4 |
| | RDAY1_4_0 | | - | 13 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | | | |
| | RDAY2_C_0 | **Read Fast** transaction reads out the memory contents at the given address. The maximum CK frequency for this transaction is 166MHz frequency. | - | 0B (CMD) | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | **Figure 12** | 166 | 3 |
| | | | - | | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | | | 4 |
| Program flash array | PRPGE_4_1 | **Program Page** programs 256B or 512B data to the memory array in one transaction. | WRENB_0_0 | 12 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Input Data 1 [7:0] | Input Data 2 [7:0] | (Continue) | - | **Figure 9** | | 4 |

## 81 SPI（1S-1S-1S）命令传输表（续）

| Function | Transaction name | Description | Prerequisite transaction | Byte 1 (Hex) | Byte 2 (Hex) | Byte 3 (Hex) | Byte 4 (Hex) | Byte 5 (Hex) | Byte 6 (Hex) | Byte 7 (Hex) | Byte 8 (Hex) | Byte 9 (Hex) | Transaction format | Max frequency (MHz) | Address length |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Erase flash array | ER004_4_0 | **Erase 4-KB Sector** transaction sets all the bits of a 4KB sector to 1 (all bytes are FFh). | WRENB_0_0 | 21 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | **Figure 7** | 166 | 4 |
| | ER256_4_0 | **Erase 256-KB Sector** transaction sets all the bits of a 256KB sector to 1 (all bytes are FFh). | WRENB_0_0 | DC (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | | | 4 |
| | ERCHP_0_0 | **Erase Chip** transaction sets all bits to 1 (all bytes are FFh) inside the entire flash memory array. | WRENB_0_0 | 60 or C7 (CMD) | - | - | - | - | - | - | - | - | **Figure 6** | | N/A |
| | EVERS_4_0 | **Evaluate Erase Status** transaction verifies that the last erase operation on the addressed sector was completed successfully. | - | D0 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | **Figure 7** | | 4 |
| | SEERC_4_0 | **Sector Erase Count** transaction outputs the number of erase cycles for the sector of the inputed address from the Sector Erase Count Register. | - | 5D (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | **Figure 12** | | 4 |
| Suspend / resume | SPEPD_0_0 | **Suspend Erase / Program / Data Integrity Check** transaction allows the system to interrupt a programming, erase or data integrity check operation. | - | B0 (CMD) | - | - | - | - | - | - | - | - | **Figure 6** | 166 | N/A |
| | RSEPD_0_0 | **Resume Erase / Program / Data Integrity Check** transaction allows the system to resume a programming, erase or data integrity check operation. | - | 7A (CMD) | - | - | - | - | - | - | - | - | | | |
| Secure silicon region | PRSSR_4_1 | **Program Secure Silicon Region** transaction programs data in 1024 bytes of Secure Silicon Region. | WRENB_0_0 | 42 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Input Data 1 [7:0] | Input Data 2 [7:0] | (Continue) | - | **Figure 9** | 166 | 4 |
| | RDSSR_4_0 | **Read Secure Silicon Region** transaction reads data from the SSR. | - | 4B (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | **Figure 12** | | |
| Advanced sector protection | RDDYB_4_0 | **Read Dynamic Protection Bit** transaction reads the contents of the DYB Access Register. | - | E0 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | **Figure 12** | 166 | 4 |
| | WRDYB_4_1 | **Write Dynamic Protection Bit** transaction writes to the DYB Access Register. | WRENB_0_0 | E1 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Input Data [7:0] | - | - | - | **Figure 9** | | |
| | RDPPB_4_0 | **Read Persistent Protection Bit** transaction reads the contents of the PPB Access Register. | - | E2 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | **Figure 12** | | |
| | PRPPB_4_0 | **Program Persistent Protection Bit** transaction programs / writes the PPB Register to enable the sector protection. | WRENB_0_0 | E3 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | **Figure 7** | | |
| | ERPPB_0_0 | **Erase Persistent Protection Bit** transaction sets all persistent protection bits to 1. | WRENB_0_0 | E4 (CMD) | - | - | - | - | - | - | - | - | **Figure 6** | | N/A |

**表 81　　SPI（1S-1S-1S）交易表（续）**

| Function | Transaction name | Description | Prerequisite transaction | Byte 1 (Hex) | Byte 2 (Hex) | Byte 3 (Hex) | Byte 4 (Hex) | Byte 5 (Hex) | Byte 6 (Hex) | Byte 7 (Hex) | Byte 8 (Hex) | Byte 9 (Hex) | Transaction format | Max frequency (MHz) | Address length |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Advanced sector protection | WRPLB_0_0 | **Write PPB Protection Lock Bit** transaction clears the PPB Lock to 0. | WRENB_0_0 | A6 (CMD) | - | - | - | - | - | - | - | - | | 166 | 4 |
| | RDPLB_0_0 | **Read Password Protection Mode Lock Bit** transaction shifts out the 8-bit PPB Lock Register contents with MSb first. | - | A7 (CMD) | - | - | - | - | - | - | - | - | **Figure 11** | | |
| | PWDUL_0_1 | **Password Unlock** transaction sends the 64-bit password to flash device. If the supplied password does not match the hidden password in the Password Register, the device is locked and only a hardware reset or POR will return the device to standby state, ready for new transactions such as a retry of the PWDUL_0_1. If the password does match, the PPB Lock bit is set to 1. | - | E9 (CMD) | Password [7:0] | Password [15:8] | Password [23:16] | Password [31:24] | Password [39:32] | Password [47:40] | Password [55:48] | Password [63:56] | **Figure 10** | | |
| Reset | SRSTE_0_0 | **Software Reset Enable** command is required immediately before a SFRST_0_0 transaction. | - | 66 (CMD) | - | - | - | - | - | - | - | - | **Figure 6** | 166 | N/A |
| | SFRST_0_0 | **Software Reset** transaction restores the device to its initial power up state, by reloading volatile registers from non-volatile default values. | SRSTE_0_0 | 99 (CMD) | - | - | - | - | - | - | - | - | | | |
| Deep power down | ENDPD_0_0 | **Enter Deep Power Down Mode** transaction shifts device in the lowest power consumption mode. | - | B9 (CMD) | - | - | - | - | - | - | - | - | | | |

## 6.2 八线（8S-8S-8S、8D-8D-8D）命令传输表

### 表82 八线（8S-8S-8S、8D-8D-8D）命令传输表

| Function | Transaction name | Description | Prerequisite transaction | Byte 1 (Hex) | Byte 2 (Hex) | Byte 3 (Hex) | Byte 4 (Hex) | Byte 5 (Hex) | Byte 6 (Hex) | Byte 7 (Hex) | Byte 8 (Hex) | Byte 9 (Hex) | Byte 10 (Hex) | Byte 11 (Hex) | Byte 12 (Hex) | Byte 13 (Hex) | Byte 14 (Hex) | Trans-action format (SDR/DDR) | HL-T / HS-T max frequency (MHz) | Address length |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | CK edge [32] ↑ | CK edge [32] ↓ | CK edge [32] ↑ | CK edge [32] ↓ | CK edge [32] ↑ | CK edge [32] ↓ | CK edge [32] ↑ | CK edge [32] ↓ | CK edge [32] ↑ | CK edge [32] ↓ | CK edge [32] ↑ | CK edge [32] ↓ | CK edge [32] ↑ | CK edge [32] ↓ | | | |
| Read device ID | RDIDN_4_0 | **Read manufacturer and device identification** transaction provides read access to manufacturer and device identification. | - | 9F (CMD) | 9F (CMD) | 00 (ADDR) | 00 (ADDR) | 00 (ADDR) | 00 (ADDR) | - | - | - | - | - | - | - | - | Figure 24 / Figure 25 | 166/200 | 4 |
| | RSFDP_4_0 | **Read JEDEC Serial Flash Discoverable Parameters** transaction sequentially accesses the Serial Flash Discovery Parameters (SFDP). | - | 5A (CMD) | 5A (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | - | - | - | | 92 (SDR) / 85 (DDR) | |
| | RDUID_4_0 | **Read Unique ID** accesses a factory programmed 64-bit number which is unique to each device. | - | 4C (CMD) | 4C (CMD) | 00 (ADDR) | 00 (ADDR) | 00 (ADDR) | 00 (ADDR) | - | - | - | - | - | - | - | - | | 166 / 200 | |
| Register access | RDSR1_4_0 | **Read Status Register 1** transaction allows the Status Register 1 contents to be read from DQ[7:0] | - | 05 (CMD) | 05 (CMD) | 00 (ADDR) | 00 (ADDR) | 00 (ADDR) | 00 (ADDR) | - | - | - | - | - | - | - | - | Figure 24 / Figure 26 | | |
| | RDSR2_4_0 | **Read Status Register-2** transaction allows the Status Register-2 contents to be read from DQ[7:0] | - | 07 (CMD) | 07 (CMD) | 00 (ADDR) | 00 (ADDR) | 00 (ADDR) | 00 (ADDR) | - | - | - | - | - | - | - | - | | | |
| | RDARG_4_0 | **Read Any Register** transaction provides a way to read all addressed non-volatile and volatile device registers. | - | 65 (CMD) | 65 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | - | - | - | Figure 24 / Figure 25 | | |
| | WRENB_0_0 | **Write Enable** sets the Write Enable Latch bit of the Status Register 1 to 1 to enable write, program and erase transactions. | - | 06 (CMD) | 06 (CMD) | - | - | - | - | - | - | - | - | - | - | - | - | Figure 15 / Figure 16 | | N/A |
| | WRDIS_0_0 | **Write Disable** sets the Write Enable Latch bit of the Status Register 1 to 0 to disable write, program and erase transactions execution. | - | 04 (CMD) | 04 (CMD) | - | - | - | - | - | - | - | - | - | - | - | - | | | |
| | WRARG_4_1 | **Write Any Register** transaction provides a way to write all addressed non-volatile and volatile device registers. | WRENB_0_0 | 71 (CMD) | 71 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Input Data [7:0] | - | - | - | - | - | - | - | Figure 21 / Figure 22 | | 4 |

**注释**

32. 如果是八线DDR协议。

**表 82　八线（8S-8S-8S、8D-8D-8D）命令传输表（续）**

| Function | Transaction name | Description | Prerequisite transaction | Byte 1 (Hex) CK ↑ edge [32] | Byte 2 (Hex) CK ↓ edge [32] | Byte 3 (Hex) CK ↑ edge [32] | Byte 4 (Hex) CK ↓ edge [32] | Byte 5 (Hex) CK ↑ edge [32] | Byte 6 (Hex) CK ↓ edge [32] | Byte 7 (Hex) CK ↑ edge [32] | Byte 8 (Hex) CK ↓ edge [32] | Byte 9 (Hex) CK ↑ edge [32] | Byte 10 (Hex) CK ↓ edge [32] | Byte 11 (Hex) CK ↑ edge [32] | Byte 12 (Hex) CK ↓ edge [32] | Byte 13 (Hex) CK ↑ edge [32] | Byte 14 (Hex) CK ↓ edge [32] | Trans-action format (SDR/DDR) | HL-T / HS-T max frequency (MHz) | Address length |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Register access | CLPEF_0_0 | **Clear Program and Erase Failure Flags** transaction resets STR1V[5] (Erase failure flag) and STR1V[6] (Program failure flag) | - | 82 (CMD) | 82 (CMD) | - | - | - | - | - | - | - | - | - | - | - | - | **Figure 15** / **Figure 16** | 166 / 200 | N/A |
| ECC | RDECC_4_0 | **Read ECC Status** is used to determine the ECC status of the addressed data unit. | - | 19 (CMD) | 19 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | - | - | - | **Figure 24** / **Figure 26** | | 4 |
| | CLECC_0_0 | **Clear ECC Status Register** transaction resets ECC Status Register bit[4] (2-bit ECC Detection), ECC Status Register bit[3] (1-bit ECC Correction), Address Trap Register and ECC Detection Counter. | - | 1B (CMD) | 1B (CMD) | - | - | - | - | - | - | - | - | - | - | - | - | **Figure 15** / **Figure 16** | | N/A |
| CRC | RDCRC_4_0 | **Read Interface CRC Register** transaction allows the volatile Interface CRC Register contents to be read | - | 64 (CMD) | 64 (CMD) | 00 (ADDR) | 00 (ADDR) | 00 (ADDR) | 00 (ADDR) | - | - | - | - | - | - | - | - | **Figure 24** / **Figure 25** | | 4 |
| | DICHK_4_1 | **Data Integrity Check** transaction causes the device to perform a Data Integrity Check over a user defined address range. | - | 5B (CMD) | 5B (CMD) | 00 (ADDR) | 00 (ADDR) | 00 (ADDR) | 00 (ADDR) | Start ADDR [31:24] | Start ADDR [23:16] | Start ADDR [15:8] | Start ADDR [7:0] | End ADDR [31:24] | End ADDR [23:16] | End ADDR [15:8] | End ADDR [7:0] | **Figure 19** / **Figure 20** | | |
| Read flash array | RDAY1_4_0 | **Read Octal SDR** transaction reads out the memory contents at the given address on DQ[7:0]. The maximum CK frequency for this SDR transaction is 200-MHz frequency | - | EC (CMD) | EC (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | - | - | - | **Figure 24** | | |
| | RDAY2_4_0 | **Read Octal DDR** transaction reads out the memory contents at the given address on DQ[7:0]. The maximum CK frequency for this DDR transaction is 200-MHz frequency | - | EE (CMD) | EE (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | - | - | - | **Figure 25** | | |
| Program flash array | PRPGE_4_1 | **Program Page** programs 256B or 512B data to the memory array in one transaction. | WRENB_0_0 | 12 (CMD) | 12 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Input Data 1 [7:0] | Input Data 2 [7:0] | (Continue) | - | - | - | - | - | **Figure 21** / **Figure 22** | | |

**注：**
32. 如果是八线DDR协议。

**表 82　八线（8S-8S-8S、8D-8D-8D）命令传输表（续）**

| Function | Transaction name | Description | Prerequisite transaction | Byte 1 (Hex) CK ↑ edge [32] | Byte 2 (Hex) CK ↓ edge [32] | Byte 3 (Hex) CK ↑ edge [32] | Byte 4 (Hex) CK ↓ edge [32] | Byte 5 (Hex) CK ↑ edge [32] | Byte 6 (Hex) CK ↓ edge [32] | Byte 7 (Hex) CK ↑ edge [32] | Byte 8 (Hex) CK ↓ edge [32] | Byte 9 (Hex) CK ↑ edge [32] | Byte 10 (Hex) CK ↓ edge [32] | Byte 11 (Hex) CK ↑ edge [32] | Byte 12 (Hex) CK ↓ edge [32] | Byte 13 (Hex) CK ↑ edge [32] | Byte 14 (Hex) CK ↓ edge [32] | Trans-action format (SDR/DDR) | HL-T / HS-T max frequency (MHz) | Address length |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Erase flash array | ER004_4_0 | **Erase 4-KB Sector** transaction sets all the bits of a 4KB sector to 1 (all bytes are FFh). | WRENB_0_0 | 21 (CMD) | 21 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | - | - | - | Figure 17 / Figure 18 | 166 / 200 | 4 |
| | ER256_4_0 | **Erase 256-KB Sector** transaction sets all the bits of a 256KB sector to 1 (all bytes are FFh). | WRENB_0_0 | DC (CMD) | DC (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | - | - | - | | | |
| | ERCHP_0_0 | **Erase Chip** transaction sets all bits to 1 (all bytes are FFh) inside the entire flash memory array. | WRENB_0_0 | 60 or C7 (CMD) | 60 or C7 (CMD) | - | - | - | - | - | - | - | - | - | - | - | - | Figure 15 / Figure 16 | | N/A |
| | EVERS_4_0 | **Evaluate Erase Status** transaction verifies that the last erase operation on the addressed sector was completed successfully. | - | D0 (CMD) | D0 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | - | - | - | Figure 17 / Figure 18 | | 4 |
| | SEERC_4_0 | **Sector Erase Count** transaction outputs the number of erase cycles for the sector of the inputed address from the Sector Erase Count Register. | - | 5D (CMD) | 5D (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | - | - | - | | | 4 |
| Suspend / resume | SPEPD_0_0 | **Suspend Erase / Program / Data Integrity Check** transaction allows the system to interrupt a programming, erase or data integrity check operation | - | B0 (CMD) | B0 (CMD) | - | - | - | - | - | - | - | - | - | - | - | - | Figure 15 / Figure 16 | | N/A |
| | RSEPD_0_0 | **Resume Erase / Program / Data Integrity Check** transaction allows the system to resume a programming, erase or data integrity check operation | - | 30 (CMD) | 30 (CMD) | - | - | - | - | - | - | - | - | - | - | - | - | | | |
| Secure silicon region | PRSSR_4_1 | **Program Secure Silicon Region** transaction programs data in 1024 bytes of Secure Silicon Region | WRENB_0_0 | 42 (CMD) | 42 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Input Data 1 [7:0] | Input Data 2 [7:0] | (Continue) | - | - | - | - | - | Figure 21 / Figure 22 | | 4 |
| | RDSSR_4_0 | **Read Secure Silicon Region** transaction reads data from the SSR. | - | 4B (CMD) | 4B (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | - | - | - | Figure 24 / Figure 25 | | |

**Note**
32. 如果是八线DDR协议。

**表 82　八线（8S-8S-8S、8D-8D-8D）命令传输表（续）**

| Function | Transaction name | Description | Prerequisite transaction | Byte 1 (Hex) CK ↑ edge [32] | Byte 2 (Hex) CK ↓ edge [32] | Byte 3 (Hex) CK ↑ edge [32] | Byte 4 (Hex) CK ↓ edge [32] | Byte 5 (Hex) CK ↑ edge [32] | Byte 6 (Hex) CK ↓ edge [32] | Byte 7 (Hex) CK ↑ edge [32] | Byte 8 (Hex) CK ↓ edge [32] | Byte 9 (Hex) CK ↑ edge [32] | Byte 10 (Hex) CK ↓ edge [32] | Byte 11 (Hex) CK ↑ edge [32] | Byte 12 (Hex) CK ↓ edge [32] | Byte 13 (Hex) CK ↑ edge [32] | Byte 14 (Hex) CK ↓ edge [32] | Trans-action format (SDR/DDR) | HL-T / HS-T max frequency (MHz) | Address length |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Advanced sector protection | RDDYB_4_0 | **Read Dynamic Protection Bit** transaction reads the contents of the DYB Access Register. | - | E0 (CMD) | E0 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | - | - | - | **Figure 24** / **Figure 26** | 166 / 200 | 4 |
| | WRDYB_4_1 | **Write Dynamic Protection Bit** transaction writes to the DYB Access Register | WRENB_0_0 | E1 (CMD) | E1 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | Input Data [7:0] | - | - | - | - | - | - | - | **Figure 21** / **Figure 23** | | |
| | RDPPB_4_0 | **Read Persistent Protection Bit** transaction reads the contents of the PPB Access Register | - | E2 (CMD) | E2 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | - | - | - | **Figure 24** / **Figure 26** | | |
| | PRPPB_4_0 | **Program Persistent Protection Bit** transaction programs / writes the PPB Register to enable the sector protection. | WRENB_0_0 | E3 (CMD) | E3 (CMD) | ADDR [31:24] | ADDR [23:16] | ADDR [15:8] | ADDR [7:0] | - | - | - | - | - | - | - | - | **Figure 17** / **Figure 18** | | |
| | ERPPB_0_0 | **Erase Persistent Protection Bit** transaction sets all persistent protection bits to 1. | WRENB_0_0 | E4 (CMD) | E4 (CMD) | - | - | - | - | - | - | - | - | - | - | - | - | **Figure 15** / **Figure 16** | | N/A |
| | WRPLB_0_0 | **Write PPB Protection Lock Bit** transaction clears the PPB Lock to 0 | WRENB_0_0 | 2C (CMD) | 2C (CMD) | - | - | - | - | - | - | - | - | - | - | - | - | | | |
| | RDPLB_4_0 | **Read Password Protection Mode Lock Bit** transaction shifts out the 8-bit PPB Lock Register contents with MSb first. | - | 2D (CMD) | 2D (CMD) | 00 (ADDR) | 00 (ADDR) | 00 (ADDR) | 00 (ADDR) | - | - | - | - | - | - | - | - | **Figure 24** / **Figure 26** | | 4 |
| | PWDUL_4_1 | **Password Unlock** transaction sends the 64-bit password to flash device. If the supplied password does not match the hidden password in the Password Register, the device is locked and only a hardware reset or POR will return the device to standby state, ready for new transactions such as a retry of the PWDUL_0_1. If the password does match, the PPB Lock bit is set to 1. | - | E9 (CMD) | E9 (CMD) | 00 (ADDR) | 00 (ADDR) | 00 (ADDR) | 00 (ADDR) | Password [7:0] | Password [15:8] | Password [23:16] | Password [31:24] | Password [39:32] | Password [47:40] | Password [55:48] | Password [63:56] | **Figure 21** / **Figure 22** | | N/A |

**Note**
32. 如果是八线DDR协议。

**表 82　八线（8S-8S-8S、8D-8D-8D）命令传输表（续）**

| Function | Transaction name | Description | Prerequisite transaction | Byte 1 (Hex) CK ↑ edge [32] | Byte 2 (Hex) CK ↓ edge [32] | Byte 3 (Hex) CK ↑ edge [32] | Byte 4 (Hex) CK ↓ edge [32] | Byte 5 (Hex) CK ↑ edge [32] | Byte 6 (Hex) CK ↓ edge [32] | Byte 7 (Hex) CK ↑ edge [32] | Byte 8 (Hex) CK ↓ edge [32] | Byte 9 (Hex) CK ↑ edge [32] | Byte 10 (Hex) CK ↓ edge [32] | Byte 11 (Hex) CK ↑ edge [32] | Byte 12 (Hex) CK ↓ edge [32] | Byte 13 (Hex) CK ↑ edge [32] | Byte 14 (Hex) CK ↓ edge [32] | Trans-action format (SDR/DDR) | HL-T / HS-T max frequency (MHz) | Address length |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reset | SRSTE_0_0 | **Software Reset Enable** command is required immediately before a SFRST_0_0 transaction | - | 66 (CMD) | 66 (CMD) | - | - | - | - | - | - | - | - | - | - | - | - | **Figure 15** / **Figure 16** | 166 / 200 | N/A |
| | SFRST_0_0 | **Software Reset** transaction restores the device to its initial power up state, by reloading volatile registers from non-volatile default values | SFRSE_0_0 | 99 (CMD) | 99 (CMD) | - | - | - | - | - | - | - | - | - | - | - | - | | | |
| Deep power down | ENDPD_0_0 | **Enter Deep Power Down Mode** transaction shifts device in the lowest power consumption mode | - | B9 (CMD) | B9 (CMD) | - | - | - | - | - | - | - | - | - | - | - | - | | | |

**注：**
32. 如果是八线DDR协议。

# 7 电气特性

## 7.1 绝对最大额定值[35]

| | |
|---|---|
| Storage temperature plastic packages | –65°C to +150°C |
| Ambient temperature with power applied | –65°C to +125°C |
| $V_{CC}$ (HL-T) | –0.5 V to +4.0 V |
| $V_{CC}$ (HS-T) | –0.5 V to +2.5 V |
| Input voltage with respect to ground ($V_{SS}$)[33] | –0.5 V to $V_{CC}$ + 0.5 V |
| Output short circuit current[34] | 100 mA |

**注释**

33. 信号转换期间允许的最大值请参阅131 页**“输入信号过冲”**。
34. 每一次只能有一个输出对地短接。短接时间不能超过一秒。
35. 如果使用大于129页**“绝对最大额定值[35]”**所列出的数值，则可能造成器件永久性损害。这只是压力额定值；并不表示器件在这些值或者在此数据手册操作部分所示值之上的任何其他情形下能正常运行。如果让器件长时间在绝对最大额定值情况下运行，会影响器件的可靠性。

## 7.2 工作范围

运行范围定义了一些限值，在这些限值之间可保证器件正常运行。

### 7.2.1 供电电压

| | |
|---|---|
| $V_{CC}$ / $V_{CCQ}$ (HL-T devices) | 2.7 V to 3.6 V |
| $V_{CC}$ / $V_{CCQ}$ (HS-T devices) | 1.7 V to 2.0 V |

### 7.2.2 温度范围

**表 83 温度范围**

| Parameter | Symbol | Devices | Spec | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| Ambient temperature | $T_A$ | Industrial / automotive AEC-Q100 grade 3 | –40 | +85 | °C |
| | | Industrial plus / automotive AEC-Q100 grade 2[36] | | +105 | |
| | | Automotive AEC-Q100 grade 1[36] | | +125 | |

**注释**

36. 扩展工业、汽车 2 级和汽车 1 级的工作和性能参数将由器件特性决定，并且可能与本规范中当前所示的标准工业或汽车 3 级温度范围设备有所不同。

## 7.3 热阻抗

**表 84 热阻抗**

| Parameter | Description | Test Condition | Device | 24-ball BGA | Unit |
|---|---|---|---|---|---|
| Theta JA | Thermal resistance (Junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance in accordance with EIA/JESD51. With Still Air (0 m/s) | 512T | 40.4 | °C/W |
| | | | 01GT | 37 | |
| Theta JB | Thermal resistance (Junction to board) | | 512T | 14.5 | |
| | | | 01GT | 9.7 | |
| Theta JC | Thermal resistance (Junction to case) | | 512T | 8 | |
| | | | 01GT | 7.5 | |

## 7.4 电容特性

**表 85 电容值**

| Symbol | Parameter | Test conditions | Typ | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance (applies to CK, CS#, RESET#) | 1 MHz | 3.0 | 7.50 | pF |
| $C_{OUT}$ | Output capacitance (applies to all I/O) | | 6.50 | | |

## 7.5 锁闭特性

**表 86 锁闭参数**[37]

| Description | Min | Max | Unit |
|---|---|---|---|
| **Input voltage with respect to $V_{SSQ}$ on all input only connections** | **–1.0** | **$V_{CCQ}$ + 1.0** | **V** |
| **Input voltage with respect to $V_{SSQ}$ on all I/O connections** | | | |
| **$V_{CCQ}$ current** | **–100** | **+100** | **mA** |

**注释**

37. 不包括电源 $V_{CC}$。测试条件：$V_{CC}$ = 1.8 V / 3.0 V，每次测试一个连接，未测试的连接$V_{SS}$。

## 7.6 直流特性

### 7.6.1 输入信号过冲

在DC条件下，输入或 I/O 信号应保持等于或介于 $V_{SSQ}$和 $V_{CCQ}$之间。在电压转换期间，输入或 I/O 可能会超过 $V_{SSQ}$至 –1.0 V 或超过 $V_{CCQ}$+ 1.0 V，持续时间最长为 20 ns。

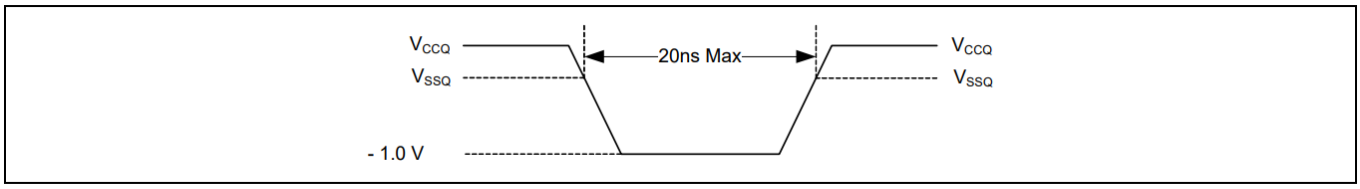


**图 66 最大负极过冲波形**

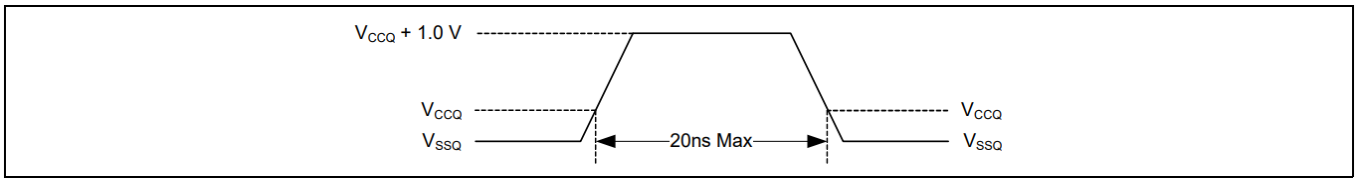


**图 67 最大正极过冲波形**

### 7.6.2 直流特性（所有温度范围）

**表 87 DC特性**[38, 40]

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit | Reference figure |
|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Input low voltage (all $V_{CC}$) | – | $V_{CCQ}$ × –0.15 | – | $V_{CCQ}$ × 0.35 | V | – |
| $V_{IH}$ | Input high voltage (all $V_{CC}$) | – | $V_{CCQ}$ × 0.65 | | $V_{CCQ}$ × 1.15 | | |
| $V_{OL}$ | Output low voltage (all $V_{CC}$) | At 0.1 mA | – | | 0.2 | | |
| $V_{OH}$ | Output high voltage (all $V_{CC}$) | At –0.1 mA | $V_{CCQ}$ – 0.20 | | | | |
| $I_{LI}$ | Input leakage current | $V_{CC}$ = $V_{CC}$ Max, $V_{IN}$ = $V_{IH}$ or $V_{SS}$, CS# = $V_{IH}$, 85 °C | – | – | ±2 | µA | – |
| | | $V_{CC}$ = $V_{CC}$ Max, $V_{IN}$ = $V_{IH}$ or $V_{SS}$, CS# = $V_{IH}$, 105 °C | | | ±3 | | |
| | | $V_{CC}$ = $V_{CC}$ Max, $V_{IN}$ = $V_{IH}$ or $V_{SS}$, CS# = $V_{IH}$, 125 °C | | | ±4 | | |

**注释**
38. 典型值为 $T_A$ = 25°C 和 $V_{CC}$ = 1.8 V / 3.0 V。
39. 读取数据返回期间输出未连接。不包括输出开关电流。
40. 推荐的INT#输出上拉电阻范围为5 kΩ to 10 kΩ.

电气特性

**表 87　　DC特性[38, 40]（续）**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit | Reference figure |
|---|---|---|---|---|---|---|---|
| $I_{LO}$ | Output leakage current | $V_{CC}$ = $V_{CC}$ Max, $V_{IN}$ = $V_{IH}$ or $V_{SS}$, CS# = $V_{IH}$, 85 °C | – | – | ±2 | µA | – |
| | | $V_{CC}$ = $V_{CC}$ Max, $V_{IN}$ = $V_{IH}$ or $V_{SS}$, CS# = $V_{IH}$, 105 °C | | | ±3 | | |
| | | $V_{CC}$ = $V_{CC}$ Max, $V_{IN}$ = $V_{IH}$ or $V_{SS}$, CS# = $V_{IH}$, 125 °C | | | ±4 | | |
| $I_{CC1}$ | Active power supply current (READ)[39] | SDR @ 50MHz (HL512T / HS512T) (HL01GT / HS01GT) | – | 10 / 10<br>18 / 14 | 21 / 18<br>25 / 25 | mA | – |
| | | SDR @ 166MHz (HL512T / HS512T) (HL01GT / HS01GT) | | 75 / 75<br>75 / 80 | 100 / 100<br>100 / 100 | | |
| | | DDR @ 200MHz (HL512T / HS512T) (HL01GT / HS01GT) | | 156 / 156<br>156 / 156 | 173 / 173<br>173 / 173 | | |
| $I_{CC2}$ | Active power supply current (page program) (512T / 01GT) | $V_{CC}$ = $V_{CC}$ Max, CS# = $V_{IH}$ | – | 50 | 58 / 66 | mA | – |
| $I_{CC3}$ | Active power supply current (write any register) (512T / 01GT) | $V_{CC}$ = $V_{CC}$ Max, CS# = $V_{IH}$ | – | 50 | 55 / 66 | mA | – |
| $I_{CC4}$ | Active power supply current (sector erase) (512T / 01GT) | $V_{CC}$ = $V_{CC}$ Max, CS# = $V_{IH}$ | – | 50 | 55 / 66 | mA | – |
| $I_{CC5}$ | Active power supply current (chip erase) (512T / 01GT) | $V_{CC}$ = $V_{CC}$ Max, CS# = $V_{IH}$ | – | 50 | 55 / 66 | mA | – |

**注释**

38. 典型值为 $T_{AI}$ = 25°C 和 $V_{CC}$ = 1.8 V / 3.0 V。
39. 读取数据返回期间输出未连接。不包括输出开关电流。
40. 推荐的INT#输出上拉电阻范围为5 kΩ to 10 kΩ.

电气特性

**表 87　　DC特性[38, 40]（续）**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit | Reference figure |
|---|---|---|---|---|---|---|---|
| $I_{SB}$ | Standby current (HS512T / HS01GTxx / HS01GTGZ) | RESET#, CS# = $V_{CCQ}$; All I/Os = $V_{CCQ}$ or $V_{SSQ}$, 85°C | – | 11 | 113 / 160 / 180 | µA | – |
| | | RESET#, CS# = $V_{CCQ}$; All I/Os = $V_{CCQ}$ or $V_{SSQ}$, 105°C | – | | 188 / 320 / 350 | | |
| | | RESET#, CS# = $V_{CCQ}$; All I/Os = $V_{CCQ}$ or $V_{SSQ}$, 125°C | – | | 340 / 490 / 650 | | |
| | Standby current (HL512T / HL01GT) | RESET#, CS# = $V_{CCQ}$; All I/Os = $V_{CCQ}$ or $V_{SSQ}$, 85°C | – | 14 | 126 / 160 | | |
| | | RESET#, CS# = $V_{CCQ}$; All I/Os = $V_{CCQ}$ or $V_{SSQ}$, 105°C | – | | 188 / 320 | | |
| | | RESET#, CS# = $V_{CCQ}$; All I/Os = $V_{CCQ}$ or $V_{SSQ}$, 125°C | – | | 340 / 490 | | |

**注释**

38. 典型值为 $T_{AI}$ = 25°C 和 $V_{CC}$ = 1.8 V / 3.0 V。
39. 读取数据返回期间输出未连接。不包括输出开关电流。
40. 推荐的INT#输出上拉电阻范围为5 kΩ to 10 kΩ.

**表 87　　DC特性[38, 40]（续）**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit | Reference figure |
|---|---|---|---|---|---|---|---|
| $I_{DPD}$ | DPD current (HS512T / HS01GTxx / HS01GTGZ) | RESET#, CS# = $V_{CCQ}$; All I/Os = $V_{CCQ}$ or $V_{SSQ}$, 85°C | – | 1.3 / 1.3 /1.3 | 18 / 24 / 24 | µA | – |
| | | RESET#, CS# = $V_{CCQ}$; All I/Os = $V_{CCQ}$ or $V_{SSQ}$, 105°C | – | | 18 /26 / 46 | | |
| | | RESET#, CS# = $V_{CCQ}$; All I/Os = $V_{CCQ}$ or $V_{SSQ}$, 125°C | – | | 31 / 52 / 80 | | |
| | DPD current (HL512T / HL01GT) | RESET#, CS# = $V_{CCQ}$; All I/Os = $V_{CCQ}$ or $V_{SSQ}$, 85°C | – | 2.2 / 2.2 | 18 / 26 | | |
| | | RESET#, CS# = $V_{CCQ}$; All I/Os = $V_{CCQ}$ or $V_{SSQ}$, 105°C | – | | 18 / 26 | | |
| | | RESET#, CS# = $V_{CCQ}$; All I/Os = $V_{CCQ}$ or $V_{SSQ}$, 125°C | – | | 31 / 52 | | |
| $I_{POR}$ | POR current | RESET#, CS# = $V_{CCQ}$; All I/Os = $V_{CCQ}$ or $V_{SSQ}$ | – | – | 80 | mA | – |
| Power up / Power down voltage | | | | | | | |
| $V_{CC}$ (min) | $V_{CC}$ (minimum operation voltage, HL-T) | – | 2.7 | – | – | V | **Figure 61**/ **Figure 63** |
| | $V_{CC}$ (minimum operation voltage, HS-T) | – | 1.7 | | | | |

**注释**

38. 典型值为 $T_A$ = 25°C 和 $V_{CC}$ = 1.8 V / 3.0 V。
39. 读取数据返回期间输出未连接。不包括输出开关电流。
40. 推荐的INT#输出上拉电阻范围为5 kΩ to 10 kΩ.

电气特性

**表 87　　DC特性[38, 40]（续）**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit | Reference figure |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ (cut-off) | $V_{CC}$ (cut off where re-initialization is needed, HL-T) | – | 2.4 | – | – | V | Figure 62 |
| | $V_{CC}$ (cut off where re-initialization is needed, HS-T) | – | 1.55 | | | | |
| $V_{CC}$ (Low) | $V_{CC}$ (low voltage for initialization to occur, HL-T) | – | 0.7 | – | – | V | |
| | $V_{CC}$ (low voltage for initialization to occur, HS-T) | – | 0.7 | | | | |

**注释**

38. 典型值为 $T_{AI}$ = 25°C 和 $V_{CC}$ = 1.8 V / 3.0 V。
39. 读取数据返回期间输出未连接。不包括输出开关电流。
40. 推荐的INT#输出上拉电阻范围为5 kΩ to 10 kΩ.

## 7.7 AC 测试条件

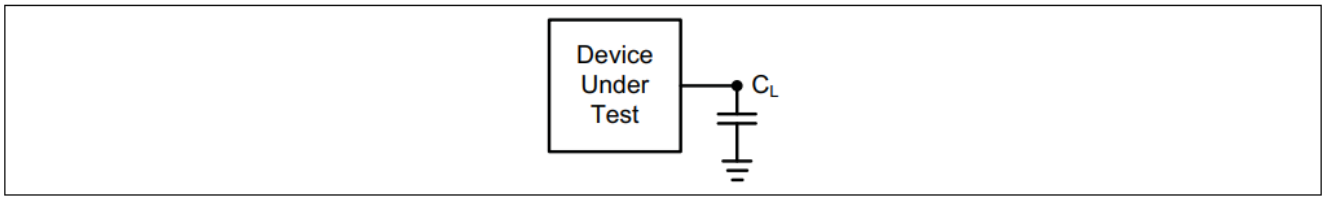


**图 68 测试设置**

**表 88 AC测量条件[42]**

| Parameter | Min | Max | Unit | Reference Figure |
|---|---|---|---|---|
| Load capacitance ($C_L$) | - | 15 | pF | Figure 68 |
| Input pulse voltage | 0 | $V_{CCQ}$ | V | Figure 70 |
| CK rise ($t_{CRT1}$) and fall ($t_{CFT1}$) slew rates at 200 MHz (HS-T)[41] | 1.13 | – | V/ns | Figure 73 |
| CK rise ($t_{CRT2}$) and fall ($t_{CFT2}$) slew rates at 166 MHz (HL-T)[41] | 1.72 | | | |
| Data rise ($t_{DRT1}$) and fall ($t_{DFT1}$) slew rates at 200 MHz (HS-T)[41] | 1.13 | | | Figure 70 |
| Data rise ($t_{DRT2}$) and fall ($t_{DFT2}$) slew rates at 166 MHz (HL-T)[41] | 1.72 | | | |
| $V_{IL(ac)}$ | $-0.30 \times V_{CCQ}$ | $0.30 \times V_{CCQ}$ | V | |
| $V_{IH(ac)}$ | $0.7 \times V_{CCQ}$ | $1.30 \times V_{CCQ}$ | | |
| $V_{OH(ac)}$ | $0.75 \times V_{CCQ}$ | – | | Figure 71 / Figure 72 |
| $V_{OL(ac)}$ | - | $0.25 \times V_{CCQ}$ | | |
| Input timing ref voltage | $0.5 \times V_{CC}$ | | | - |
| Output timing ref voltage | $0.5 \times V_{CC}$ | | | |

**注释**
41. 在 $V_{CC}$ 最大时测量从输入脉冲最小值到最大值的输入斜率。
42. AC特性表假设时钟和数据信号具有相同的斜率（斜率）。

# 8 时序特性

**表 89 时序特性**[45]

| Symbol | Parameter | Min | Typ | Max | Unit | Reference figure |
|---|---|---|---|---|---|---|
| **Octal SDR/DDR** | | | | | | |
| $f_{CK}$ | CK clock frequency for octal mode transactions using DS (HS-T) | 0 | – | 200 | MHz | – |
| | CK clock frequency for octal mode transactions using DS (HL-T) | 0 | – | 166 | | |
| $p_{CK}$ | CK clock period | $1/f_{CK}$ | – | ∞ | ns | **Figure 70** |
| $t_{CH}$ | Clock high time | 45% $p_{CK}$ | – | 55% $p_{CK}$ | ns | **Figure 73** |
| $t_{CL}$ | Clock low time | | – | | ns | |
| $t_{CS}$ | CS# high time (read transactions) | 10 | – | – | ns | **Figure 76** / **Figure 77** |
| | CS# high time between transactions (interface CRC Read Register and aborted transaction) | 50 | – | – | | |
| | CS# high time (program / erase transactions) | 50 | – | – | | |
| $t_{CSS}$ | CS# active setup time (relative to CK) | 4 | – | – | ns | |
| $t_{CSH0}$ | CS# active hold time (relative to CK in Mode 0) | 4 | – | – | ns | |
| $t_{CSH3}$ | CS# active hold time (relative to CK in Mode 3) | 6.5 | – | – | ns | |
| $t_{SU}$ | HS-T data setup time (all $V_{CC}$) | 0.5 | – | – | ns | |
| | HL-T data setup time (all $V_{CC}$) | 0.6 | – | – | | |
| $t_{HD}$ | HL-T data hold time (all $V_{CC}$) | 0.6 | – | – | ns | |
| | HS-T data hold time (all $V_{CC}$) | 0.5 | – | – | | |

**注释**

43. 完整 $V_{CC}$范围和 CL = 15 pF。
44. 输出 HI-Z 定义为数据不再驱动的点。
45. 适用于所有工作温度选项。
46. 如果在$t_{PU}$ 结束时Reset#有效，则器件将保持在复位状态，并且$t_{RH}$ 将决定CS何时可能变为低电平。
47. $t_{RP}$ 和 $t_{RH}$ 的总和不能小于$t_{RPH}$.
48. 典型写入和擦除时间假定以下条件：25°C，$V_{CC}$= 1.8 V 和 3.0 V；棋盘数据样式。
49. 任何OTP 写入命令传输的写入时间与 $t_{pp}$相同。这包含PRSSR_4_1。
50. PRPPB_4_0 命令传输的写入时间与 $t_{PP}$ 相同。ERPPB_0_0 命令传输的擦除时间与 $t_{SE}$相同 。
51. 这些值由特性保证，并未在生产中经过 100% 测试。
52. 由设计保证
53. 联合电子器件工程委员会（JEDEC）标准JESD22-A117根据一个合格规范对执行耐久性和保持时间测试的步骤要求进行了定义。该测试的目的在于确定闪存器件在无失败的条件下保持重复的数据更改的能力（写入/擦除耐久性）和在预期时间内保持数据的能力（数据保持）。耐久性和数据保持合格规范在JESD47中指定，也可以通过知识库方法进行开发，如JESD94中所示。

时序特性

**表 89　　时序特性[45]（续）**

| Symbol | Parameter | Min | Typ | Max | Unit | Reference figure |
|---|---|---|---|---|---|---|
| $t_V$[43] | Clock low to output valid (15 pF loading) (HS-T) | 2 | – | 5.45 | ns | Figure 76 / Figure 78 |
| | Clock low to output valid (15 pF loading) (HL-T) | | | 7.25 | | |
| $t_{CKDS}$ | DS valid (HS-T) | – | – | 5.45 | ns | |
| | DS valid (HL-T) | – | – | 7.25 | | |
| $t_{DSS}$[51] | DS transition to data valid | –0.4 | – | 0.4 | ns | |
| $t_{DSH}$[51] | DS transition to data invalid | –0.4 | – | 0.4 | ns | |
| $t_{HO}$ | Output hold time | 0.4 | – | – | ns | Figure 76 |
| $t_{DIS}$[44] | CS# inactive to output disable time (HL-T/HS-T) (SDR) | – | – | 6.5 / 7.5 | ns | Figure 76 / Figure 78 |
| | CS# inactive to output disable time (HL-T/HS-T) (DDR) | – | – | 6.0 / 7.5 | | |
| $t_{DSZ}$ | CS# inactive to DS disable time (HS-T) (SDR / DDR) | – | – | 6.50 / 6.0 | ns | |
| | CS# inactive to DS disable time (HL-T) | – | – | 7.50 | | |
| $t_{IO\_SKEW}$[51] | Data skew (first data bit to last data bit) | – | – | 0.5 | ns | – |
| $t_{PS}$ | Program/erase transaction CS# invalid to program suspend / erase suspend transaction CS# invalid (interface CRC) | – | – | 15 | µs | Figure 39 |
| $t_{CSDS}$ | CS# low to DS low | – | – | 10 | ns | Figure 27 / Figure 28 |
| **SPI SDR** | | | | | | |
| $f_{CK}$ | CK clock frequency | 0 | – | 166[53] | MHz | – |
| $p_{CK}$ | CK clock period | $1/f_{CK}$ | – | ∞ | ns | Figure 70 |
| $t_{CH}$ | Clock high time | 45% $p_{CK}$ | – | 55% $p_{CK}$ | ns | Figure 73 |
| $t_{CL}$ | Clock low time | | – | | | |

**注释**

43. 完整 $V_{CC}$范围和 CL = 15 pF。
44. 输出 HI-Z 定义为数据不再驱动的点。
45. 适用于所有工作温度选项。
46. 如果在$t_{PU}$ 结束时Reset#有效，则器件将保持在复位状态，并且$t_{RH}$ 将决定CS何时可能变为低电平。
47. $t_{RP}$和 $t_{RH}$ 的总和不能小于 $t_{RPH}$。
48. 典型程序和功耗时间假定以下条件：25°C，$V_{CC}$= 1.8 V 和 3.0 V；棋盘数据样式。
49. 任何OTP 写入命令传输的写入时间与 $t_{PP}$ 相同。这包括PRSSR_4_1。
50. PRPPB_4_0 命令传输的写入时间与 $t_{PP}$ 相同。ERPPB_0_0 命令传输的擦除时间与 $t_{SE}$ 相同。
51. 这些值由特性保证，并未在生产中经过 100% 测试。
52. 由设计保证
53. 联合电子器件工程委员会（JEDEC）标准JESD22-A117根据一个合格规范对执行耐久性和保持时间测试的步骤要求进行了定义。该测试的目的在于确定闪存器件在无失败的条件下保持重复的数据更改的能力（写入/擦除耐久性）和在预期时间内保持数据的能力（数据保持）。耐久性和数据保持合格规范在JESD47中指定，也可以通过知识库方法进行开发，如JESD94中所示。

时序特性

**表 89　　时序特性[45]（续）**

| Symbol | Parameter | Min | Typ | Max | Unit | Reference figure |
|---|---|---|---|---|---|---|
| $t_{CS}$ | CS# high time (read transactions) | 10 | – | – | ns | Figure 74 / Figure 75 |
| | CS# high time between transactions (aborted commands) | 20 | – | – | | |
| | CS# high time (program / erase transactions) | 50 | – | – | | |
| $t_{CSS}$ | CS# active setup time relative to CK ($f_{CK} \leq 50$ MHz / $f_{CK} > 50$ MHz) | 5 / 4 | – | – | ns | Figure 74 |
| $t_{CSH0}$ | CS# active hold time (relative to CK in Mode 0) | 4 | – | – | ns | |
| $t_{CSH3}$ | CS# active hold time (relative to CK in Mode 3) | 6 | – | – | ns | |
| $t_{SU}$ | Data setup time (all $V_{CC}$) | 2 | – | – | ns | |
| $t_{HD}$ | Data hold time (all $V_{CC}$) | 2 | – | – | ns | |

**注释**

43. 完整 $V_{CC}$范围和 CL = 15 pF。
44. 输出 HI-Z 定义为数据不再驱动的点。
45. 适用于所有工作温度选项。
46. 如果在$t_{PU}$ 结束时Reset#有效，则器件将保持在复位状态，并且$t_{RH}$ 将决定CS何时可能变为低电平。
47. $t_{RP}$和 $t_{RH}$ 的总和不能小于 $t_{RPH}$。
48. 典型程序和功耗时间假定以下条件：25°C，$V_{CC}$= 1.8 V 和 3.0 V；棋盘数据样式。
49. 任何OTP 写入命令传输的写入时间与 $t_{PP}$ 相同。这包括PRSSR_4_1。
50. PRPPB_4_0 命令传输的写入时间与 $t_{PP}$ 相同。ERPPB_0_0 命令传输的擦除时间与 $t_{SE}$ 相同。
51. 这些值由特性保证，并未在生产中经过 100% 测试。
52. 由设计保证
53. 联合电子器件工程委员会（JEDEC）标准JESD22-A117根据一个合格规范对执行耐久性和保持时间测试的步骤要求进行了定义。该测试的目的在于确定闪存器件在无失败的条件下保持重复的数据更改的能力（写入/擦除耐久性）和在预期时间内保持数据的能力（数据保持）。耐久性和数据保持合格规范在JESD47中指定，也可以通过知识库方法进行开发，如JESD94中所示。

时序特性

**表 89　　时序特性[45]（续）**

| Symbol | Parameter | Min | Typ | Max | Unit | Reference figure |
|---|---|---|---|---|---|---|
| $t_V$ | Clock low to output valid (15 pF loading, 3.0 V–3.6 V, 30 Ω output Impedance) (HL-T) | 2 | – | 6.5 | ns | Figure 75 |
| | Clock low to output valid (30pF Loading) (HS-T) (512T / 01GT) | 2 / 2 | – | 8 / 8 | | |
| | Clock low to output valid (30pF Loading) (HL-T) | 2 | – | 9 | | |
| | Clock low to output valid (15pF Loading) (HS-T) (512T / 01GT) | 2 / 2 | – | 6 / 6 | | |
| | Clock low to output valid (15pF Loading) (HL-T) | 2 | – | 8 | | |
| $t_{HO}$ | Output hold time | 1.5 / 1.5 | | – | ns | |
| $t_{DIS}$ | Output disable time (HL512T / HS512T) (HL01GT / HS01GT) | - | –<br>– | 7.5 / 6<br>7.4 / 6 | ns | |
| **Power up / power down timing** | | | | | | |
| $t_{PU}$ | $V_{CC}$(min) to read operation (HL512T / HS512T) (HL01GT / HS01GT) | – | – | 450 / 500<br>500 / 500 | µs | Figure 61 |
| $t_{PD}$ | $V_{CC}$(low) time | 25 | – | – | | Figure 62 |
| $t_{VR}$[52] | $V_{CC}$ / $V_{CC}$Q power up ramp rate | 1 | – | – | µs/V | Figure 63 |
| $t_{VF}$ | $V_{CC}$ / $V_{CC}$Q power down ramp rate (512T / 01GT) | 30 / 30 | – | – | | |
| **Deep power down mode timing** | | | | | | |
| $t_{ENTDPD}$[52] | Time to enter DPD mode | – | – | 3 | µs | – |

**注释**

43. 完整 $V_{CC}$范围和 CL = 15 pF。
44. 输出 HI-Z 定义为数据不再驱动的点。
45. 适用于所有工作温度选项。
46. 如果在$t_{PU}$ 结束时Reset#有效，则器件将保持在复位状态，并且$t_{RH}$ 将决定CS何时可能变为低电平。
47. $t_{RP}$和 $t_{RH}$ 的总和不能小于 $t_{RPH}$。
48. 典型程序和功耗时间假定以下条件：25°C，$V_{CC}$= 1.8 V 和 3.0 V；棋盘数据样式。
49. 任何OTP 写入命令传输的写入时间与 $t_{PP}$ 相同。这包括PRSSR_4_1。
50. PRPPB_4_0 命令传输的写入时间与 $t_{PP}$ 相同。ERPPB_0_0 命令传输的擦除时间与 $t_{SE}$ 相同。
51. 这些值由特性保证，并未在生产中经过 100% 测试。
52. 由设计保证
53. 联合电子器件工程委员会（JEDEC）标准JESD22-A117根据一个合格规范对执行耐久性和保持时间测试的步骤要求进行了定义。该测试的目的在于确定闪存器件在无失败的条件下保持重复的数据更改的能力（写入/擦除耐久性）和在预期时间内保持数据的能力（数据保持）。耐久性和数据保持合格规范在JESD47中指定，也可以通过知识库方法进行开发，如JESD94中所示。

时序特性

**表 89　　时序特性[45]（续）**

| Symbol | Parameter | Min | Typ | Max | Unit | Reference figure |
|---|---|---|---|---|---|---|
| $t_{EXTDPD}$ | Time to exit DPD mode<br>(HL512T / HS512T)<br>(HL01GT / HS01GT) | – | – | 380 / 430<br>430 / 430 | µs | Figure 60 |
| $t_{CSDPD}$ | Chip select pulse width to exit DPD | 0.02 | – | 3 | µs | |
| **复位时序[46,47]** | | | | | | |
| $t_{RS}$ | Reset setup - RESET# high before CS# low | 50 | – | – | ns | Figure 53 |
| $t_{RH}$ | Reset pulse hold - RESET# low to CS# low (HL512T / HS512T)<br>(HL01GT / HS01GT) | 450 / 500<br>500 / 500 | – | – | µs | |
| $t_{RP}$ | RESET# pulse width | 200 | – | – | ns | |
| $t_{SR}$ | Internal device reset from software reset transaction (512T / 01GT) | – | – | 83 / 83 | µs | – |
| **CS#信号复位时序** | | | | | | |
| $t_{CSLW}$ | Chip select low | 500 | – | – | ns | Figure 58 |
| $t_{CSHG}$ | Chip select high | 500 | – | – | ns | |
| $t_{RESET}$ | Internal device reset<br>(HL512T / HS512T)<br>(HL01GT / HS01GT) | – | – | 450 / 500<br>500 / 500 | µs | |
| $t_{SUJ}$ | Data in setup time (w.r.t CS#) | 50 | – | – | ns | |
| $t_{HDJ}$ | Data in hold time (w.r.t CS#) | 50 | – | – | ns | |

**注释**

43. 完整 $V_{CC}$范围和 CL = 15 pF。
44. 输出 HI-Z 定义为数据不再驱动的点。
45. 适用于所有工作温度选项。
46. 如果在$t_{PU}$ 结束时Reset#有效，则器件将保持在复位状态，并且$t_{RH}$ 将决定CS何时可能变为低电平。
47. $t_{RP}$和 $t_{RH}$ 的总和不能小于 $t_{RPH}$。
48. 典型程序和功耗时间假定以下条件：25°C，$V_{CC}$= 1.8 V 和 3.0 V；棋盘数据样式。
49. 任何OTP 写入命令传输的写入时间与 $t_{PP}$ 相同。这包括PRSSR_4_1。
50. PRPPB_4_0 命令传输的写入时间与 $t_{PP}$ 相同。ERPPB_0_0 命令传输的擦除时间与 $t_{SE}$ 相同。
51. 这些值由特性保证，并未在生产中经过 100% 测试。
52. 由设计保证
53. 联合电子器件工程委员会（JEDEC）标准JESD22-A117根据一个合格规范对执行耐久性和保持时间测试的步骤要求进行了定义。该测试的目的在于确定闪存器件在无失败的条件下保持重复的数据更改的能力（写入/擦除耐久性）和在预期时间内保持数据的能力（数据保持）。耐久性和数据保持合格规范在JESD47中指定，也可以通过知识库方法进行开发，如JESD94中所示。

时序特性

**表 89　　时序特性[45]（续）**

| Symbol | Parameter | Min | Typ | Max | Unit | Reference figure |
|---|---|---|---|---|---|---|
| **嵌入式算法 (擦除、写入和数据完整性检查) 性能[48, 49, 50, 53]** | | | | | | |
| $t_W$ | Non-volatile register write time (512T / 01GT) | – | 44 / 44 | 357.5 | ms | – |
| $t_{PP}$ | 256B page programming 4KB Sector (512T / 01GT) | – | 430 / 480 | 2175 | µs | – |
| | 256B page programming 256KB Sector | – | 430 | 1700 | | |
| | 512B Page Programming 4KB Sector | – | 680 | 2175 | | |
| | 512B Page Programming 256KB Sector) | – | 570 | 1700 | | |
| $t_{SE}$ | Sector Erase Time (4 KB physical sectors) | – | 42 | 335 | ms | – |
| | Sector Erase Time (256 KB Infineon Endurance Flex architecture disabled) | – | 773 | 2677 | | |
| | Sector Erase Time (256 KB Infineon Endurance Flex architecture enabled) | – | 773 | 5869 | | |
| $t_{BE}$ | Chip Erase Time (512 Mb) | – | 201 | 696 | sec | – |
| | Chip Erase Time (1 Gb) | – | 398 | 1381 | sec | – |
| $t_{EES}$ | Evaluate Erase Status Time for 4 KB physical sectors (HL512T / HS512T) (HL01GT / HS01GT) | – | 45/ 45<br>45 / 45 | 51 / 51<br>53 / 56 | µs | – |
| | Evaluate Erase Status Time for 256 KB physical sectors (HL512T / HS512T) (HL01GT / HS01GT) | – | | | | |
| $t_{DIC\_SETUP}$ | Data Integrity Check Calculation Setup Time (512T / 01GT) | – | 50 / 17 | – | MBps | – |

**注释**

43. 完整 $V_{CC}$范围和 CL = 15 pF。
44. 输出 HI-Z 定义为数据不再驱动的点。
45. 适用于所有工作温度选项。
46. 如果在$t_{PU}$ 结束时Reset#有效，则器件将保持在复位状态，并且$t_{RH}$ 将决定CS何时可能变为低电平。
47. $t_{RP}$和 $t_{RH}$ 的总和不能小于 $t_{RPH}$。
48. 典型程序和功耗时间假定以下条件：25°C，$V_{CC}$= 1.8 V 和 3.0 V；棋盘数据样式。
49. 任何OTP 写入命令传输的写入时间与 $t_{PP}$ 相同。这包括PRSSR_4_1。
50. PRPPB_4_0 命令传输的写入时间与 $t_{PP}$ 相同。ERPPB_0_0 命令传输的擦除时间与 $t_{SE}$ 相同。
51. 这些值由特性保证，并未在生产中经过 100% 测试。
52. 由设计保证
53. 联合电子器件工程委员会（JEDEC）标准JESD22-A117根据一个合格规范对执行耐久性和保持时间测试的步骤要求进行了定义。该测试的目的在于确定闪存器件在无失败的条件下保持重复的数据更改的能力（写入/擦除耐久性）和在预期时间内保持数据的能力（数据保持）。耐久性和数据保持合格规范在JESD47中指定，也可以通过知识库方法进行开发，如JESD94中所示。

时序特性

**表 89　　时序特性[45]（续）**

| Symbol | Parameter | Min | Typ | Max | Unit | Reference figure |
|---|---|---|---|---|---|---|
| $t_{DIC\_RATES}$ | Data Integrity Check Calculation Rate (Calculation rate over a large (>1024-byte) block of data) (512T / 01GT) | 55 / 56 | 65 / 65 | – | MBps | – |
| $t_{SEC}$ | Sector Erase Count Time (HL512T / HS512T) (HL01GT / HS01GT) | – | 55/ 55<br>55 / 55 | 63 / 63<br>70 / 70 | µs | – |
| $t_{BEC1}$ | Blank Check single 256 KB sector | – | 15 | 17 | ms | – |
| $t_{BEC2}$ | Blank Check single 4 KB sector | – | 1 | 2 | | – |
| $t_{PASSWORD}$ | Password Comparison Time | 80 | 100 | 120 | µs | – |
| **Program, Erase, or Data Integrity Check Suspend/Resume Timing** | | | | | | |
| $t_{PEDS}$ | Program/Erase/Data Integrity Check Suspend | – | – | 100 | µs | – |
| $t_{PEDRS}$ | Program/Erase/Data Integrity Check Resume to next Program/Erase/Data Integrity Check Suspend | – | 100 | – | | – |

**注释**

43. 完整 $V_{CC}$范围和 CL = 15 pF。
44. 输出 HI-Z 定义为数据不再驱动的点。
45. 适用于所有工作温度选项。
46. 如果在$t_{PU}$ 结束时Reset#有效，则器件将保持在复位状态，并且$t_{RH}$ 将决定CS何时可能变为低电平。
47. $t_{RP}$和 $t_{RH}$ 的总和不能小于 $t_{RPH}$。
48. 典型程序和功耗时间假定以下条件：25°C，$V_{CC}$= 1.8 V 和 3.0 V；棋盘数据样式。
49. 任何OTP 写入命令传输的写入时间与 $t_{PP}$ 相同。这包括PRSSR_4_1。
50. PRPPB_4_0 命令传输的写入时间与 $t_{PP}$ 相同。ERPPB_0_0 命令传输的擦除时间与 $t_{SE}$ 相同。
51. 这些值由特性保证，并未在生产中经过 100% 测试。
52. 由设计保证
53. 联合电子器件工程委员会（JEDEC）标准JESD22-A117根据一个合格规范对执行耐久性和保持时间测试的步骤要求进行了定义。该测试的目的在于确定闪存器件在无失败的条件下保持重复的数据更改的能力（写入/擦除耐久性）和在预期时间内保持数据的能力（数据保持）。耐久性和数据保持合格规范在JESD47中指定，也可以通过知识库方法进行开发，如JESD94中所示。

## 8.1 时序波形

### 8.1.1 时序波形

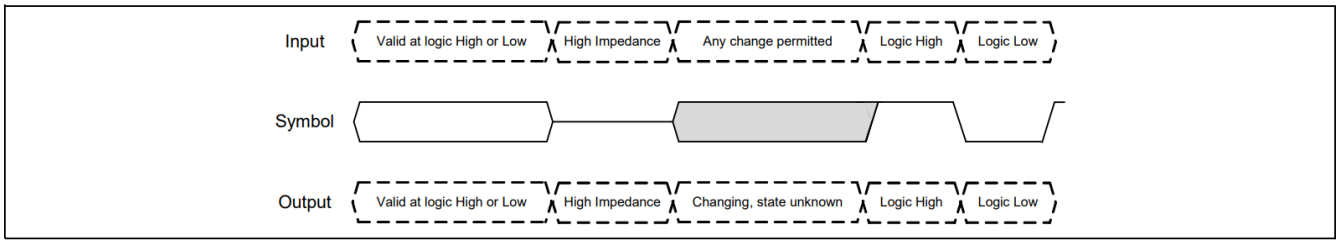


图 69 波形因素含义

### 8.1.2 时序参考电平

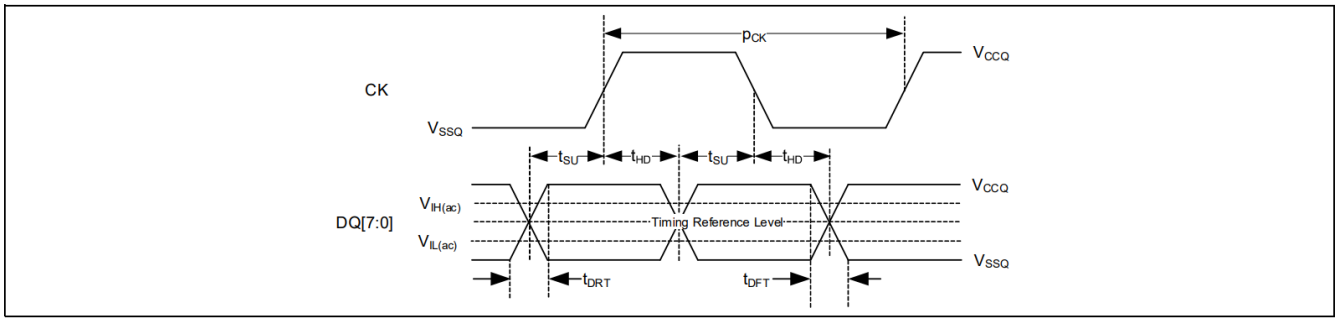


图 70 输入参考电平

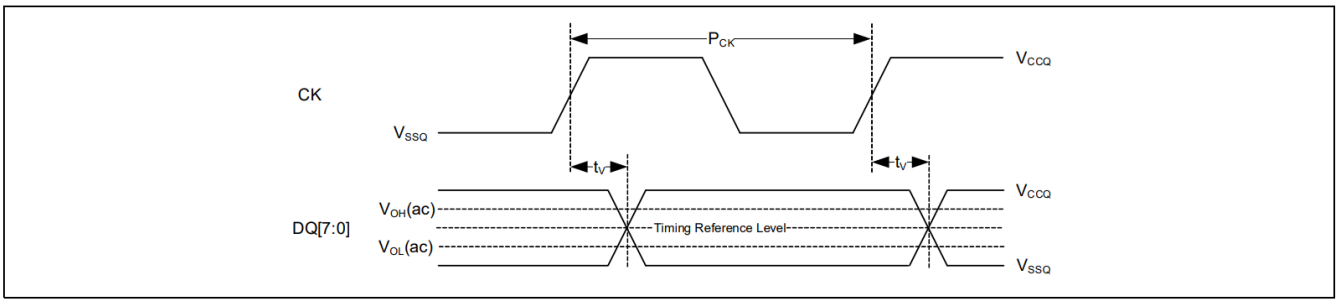


图 71 SDR 输出参考电平

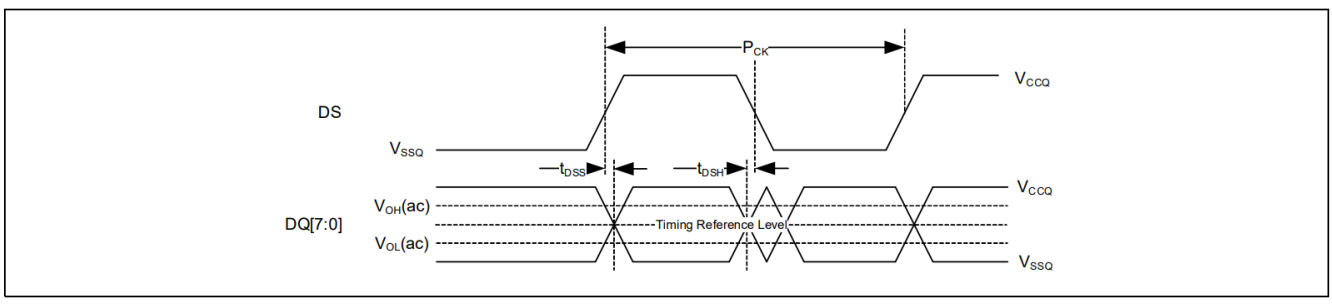


图 72 DDR 输出参考电平

### 8.1.3 时钟时序

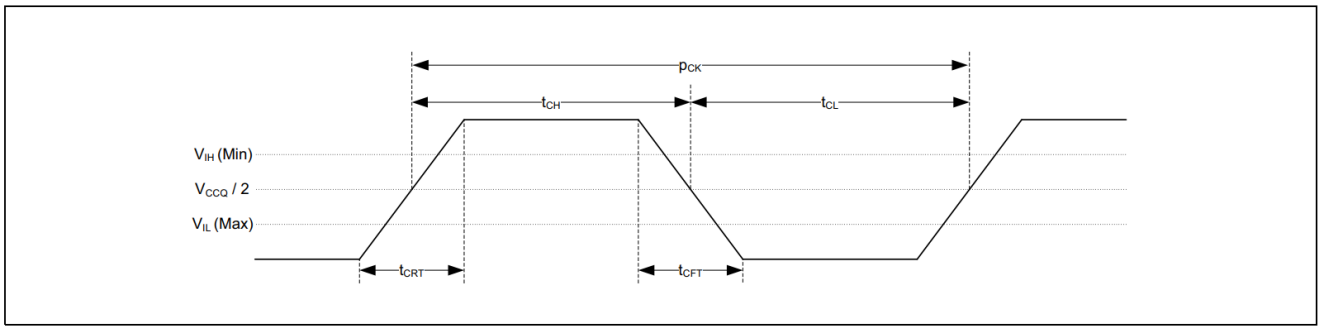


**图 73 时钟时序**

### 8.1.4 输入/输出时序

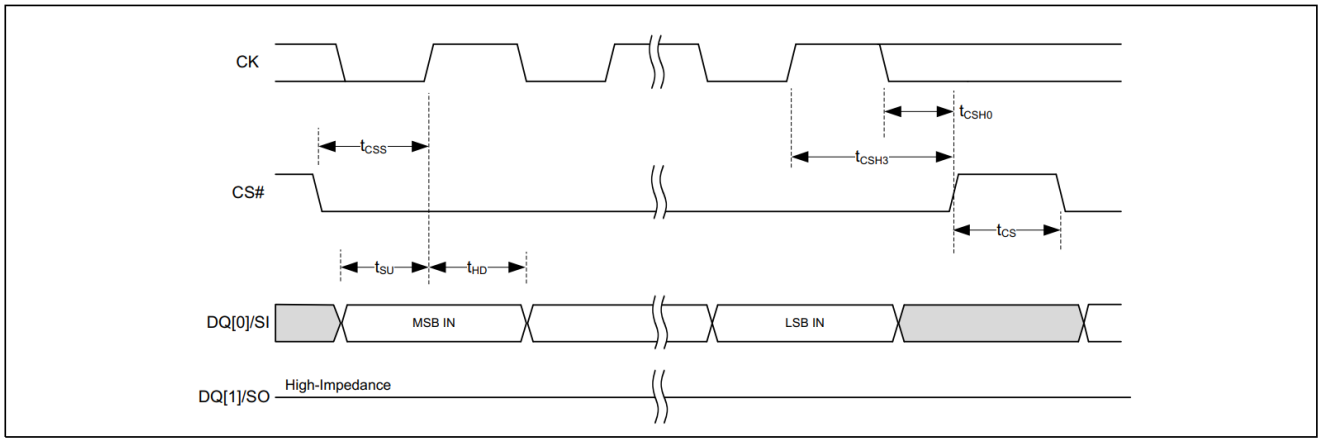


**图 74 SPI输入时序**

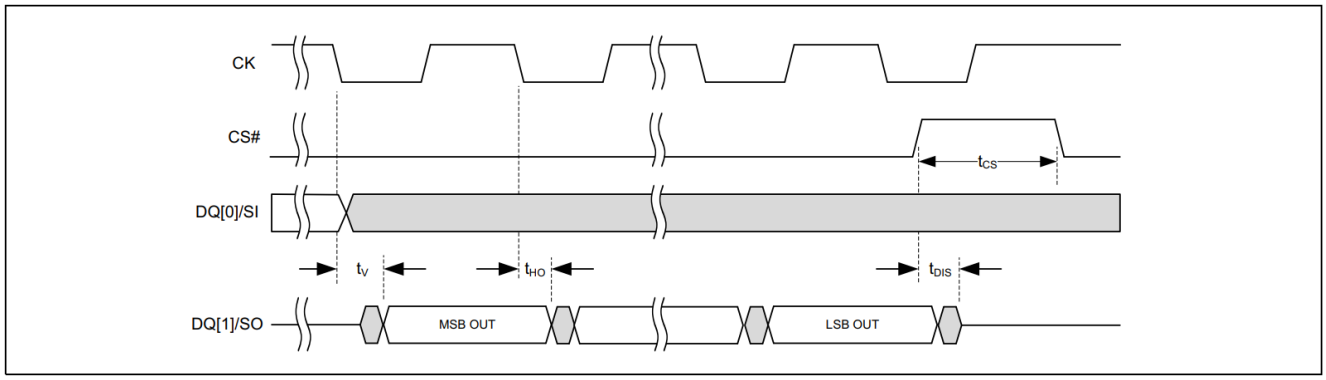


**图 75 SPI输出时序**

时序特性

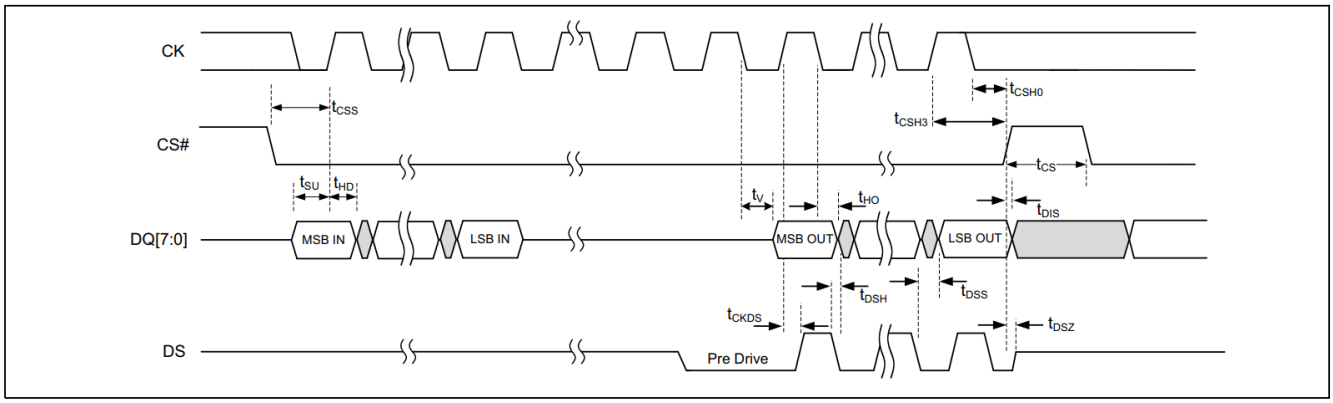


**图 76　　八线SDR输入输出时序**

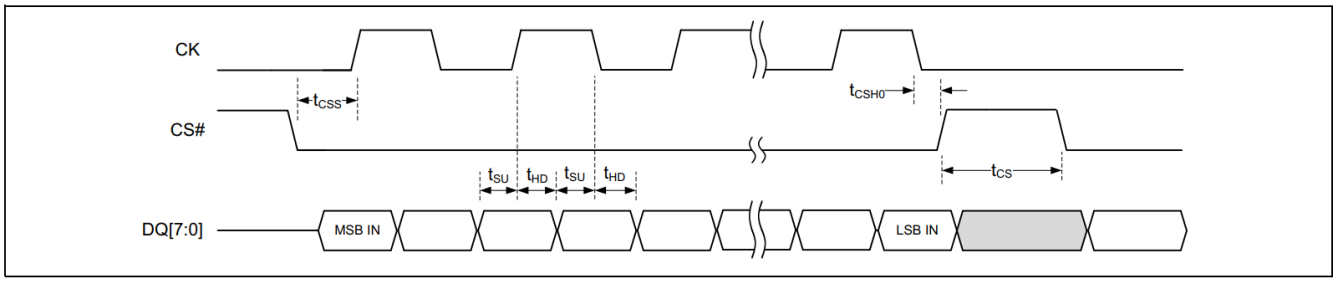


**图 77　　八线DDR输入时序**

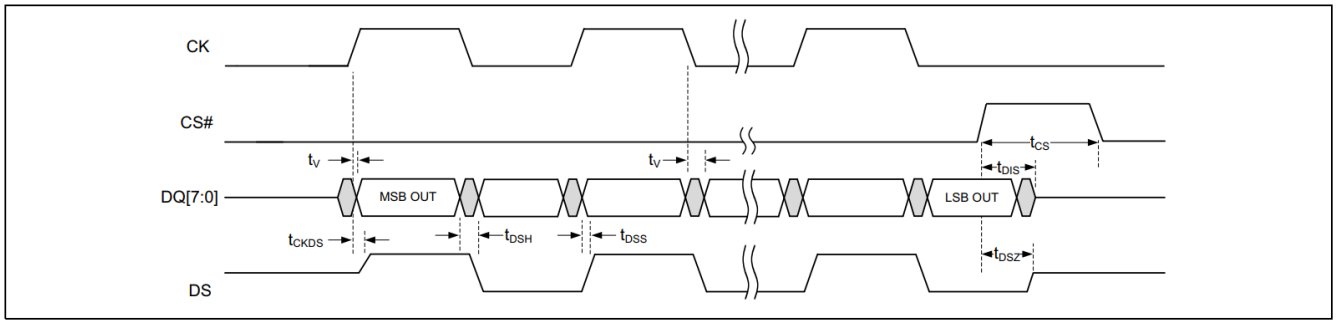


**图 78　　八线DDR输出时序**

# 9 器件标识

## 9.1 JEDEC SFDP REV D

### 9.1.1 JEDEC SFDP Rev D 帧头表

**表 90 JEDEC SFDP Rev D 帧头表**

| SFDP byte address | SFDP DWORD name | Data | Description |
|---|---|---|---|
| 00h | SFDP Header | 53h | This is the entry point for Read SFDP (5Ah) command i.e., location zero within SFDP space ASCII “S” |
| 01h | | 46h | ASCII “F” |
| 02h | | 44h | ASCII “D” |
| 03h | | 50h | ASCII “P” |
| 04h | | 08h | SFDP Minor Revision (08h = JEDEC JESD216 Revision D) |
| 05h | | 01h | SFDP Major Revision (01h = JEDEC JESD216 Revision D) |
| 06h | | 05h | Number of Parameter Headers (zero based, 05h = 6 parameters) |
| 07h | | FEh | xSPI NOR Profile 1 Octal, (8D, 8D, 8D) operation, 4-byte addressing for SFDP command, 8 WAIT states (Booting up in 1S-1S-1S mode) |
| 08h | 1st Parameter Header | 00h | Parameter ID LSB (00h = JEDEC SFDP Basic SPI Flash Parameter) |
| 09h | | 00h | Parameter Table Minor Revision (00h = JEDEC JESD216 Revision D) |
| 0Ah | | 01h | Parameter Table Major Revision (01h = JEDEC JESD216 Revision D) |
| 0Bh | | 14h | Parameter Table Length (14h = 20 DWORDs are in the Parameter table) |
| 0Ch | | 00h | Parameter Table Pointer Byte 0 (DWORD = 4 byte aligned) JEDEC Basic SPI Flash parameter byte offset = 0100h address |
| 0Dh | | 01h | Parameter Table Pointer Byte 1 |
| 0Eh | | 00h | Parameter Table Pointer Byte 2 |
| 0Fh | | FFh | Parameter ID MSB (FFh = JEDEC defined Parameter) |
| 10h | 2nd Parameter Header | 84h | Parameter ID LSB (84h = 4-Byte Address Instruction Table) |
| 11h | | 00h | Parameter Table Minor Revision (00h = JEDEC JESD216 Revision D) |
| 12h | | 01h | Parameter Table Major Revision (01h = JEDEC JESD216 Revision D) |
| 13h | | 02h | Parameter Table Length (2h = 2 DWORDs are in the Parameter table) |
| 14h | | 50h | Parameter Table Pointer Byte 0 (DWORD = 4-byte aligned) 4-Byte Address Instruction Table byte offset = 0150h address |
| 15h | | 01h | Parameter Table Pointer Byte 1 |
| 16h | | 00h | Parameter Table Pointer Byte 2 |
| 17h | | FFh | Parameter ID MSB (FFh = JEDEC defined Parameter) |

**表 90　　JEDEC SFDP Rev D 帧头表（续）**

| SFDP byte address | SFDP DWORD name | Data | Description |
|---|---|---|---|
| 18h | 3rd Parameter Header | 05h | Parameter ID LSB (05h = JEDEC xSPI Profile 1.0) |
| 19h | | 00h | Parameter Table Minor Revision (00h = JEDEC JESD216 Revision D) |
| 1Ah | | 01h | Parameter Table Major Revision (01h = JEDEC JESD216 Revision D) |
| 1Bh | | 05h | Parameter Table Length (5h = 5 DWORDs are in the Parameter table) |
| 1Ch | | 58h | Parameter Table Pointer Byte 0 (DWORD = 4-byte aligned) JEDEC xSPI Profile 1.0 = 0158h address |
| 1Dh | | 01h | Parameter Table Pointer Byte 1 |
| 1Eh | | 00h | Parameter Table Pointer Byte 2 |
| 1Fh | | FFh | Parameter ID MSB (FFh = JEDEC defined Parameter) |
| 20h | 4th Parameter Header | 87h | Parameter ID LSB (87h = JEDEC Status, Control and Configuration Register Map) |
| 21h | | 00h | Parameter Table Minor Revision (00h = JEDEC JESD216 Revision D) |
| 22h | | 01h | Parameter Table Major Revision (01h = JEDEC JESD216 Revision D) |
| 23h | | 1Ch | Parameter Table Length (1Ch = 28 DWORDs are in the Parameter table) |
| 24h | | 6Ch | Parameter Table Pointer Byte 0 (DWORD = 4-byte aligned) JEDEC Status, Control and Configuration Register Map = 016Ch address |
| 25h | | 01h | Parameter Table Pointer Byte 1 |
| 26h | | 00h | Parameter Table Pointer Byte 2 |
| 27h | | FFh | Parameter ID MSB (FFh = JEDEC defined Parameter) |
| 28h | 5th Parameter Header | 0Ah | Parameter ID LSB (0Ah = Command Sequences to change to Octal DDR (8D-8D-8D) mode) |
| 29h | | 00h | Parameter Table Minor Revision (00h = JEDEC JESD216 Revision D) |
| 2Ah | | 01h | Parameter Table Major Revision (01h = JEDEC JESD216 Revision D) |
| 2Bh | | 04h | Parameter Table Length (4h = 4 DWORDs are in the Parameter table) |
| 2Ch | | DCh | Parameter Table Pointer Byte 0 (DWORD = 4-byte aligned) Command Sequences to Change to Octal DDR (8D-8D-8D) Mode = 1DCh address |
| 2Dh | | 01h | Parameter Table Pointer Byte 1 |
| 2Eh | | 00h | Parameter Table Pointer Byte 2 |
| 2Fh | | FFh | Parameter ID MSB (FFh = JEDEC defined Parameter) |

器件标识

**表 90　　JEDEC SFDP Rev D 帧头表（续）**

| SFDP byte address | SFDP DWORD name | Data | Description |
|---|---|---|---|
| 30h | 6th Parameter Header | 81h | Parameter ID LSB (81h = JEDEC Sector Map) |
| 31h | | 00h | Parameter Table Minor Revision (00h = JEDEC JESD216 Revision D) |
| 32h | | 01h | Parameter Table Major Revision (01h = JEDEC JESD216 Revision D) |
| 33h | | 16h | Parameter Table Length (16h = 22 DWORDs are in the Parameter table) |
| 34h | | ECh | Parameter Table Pointer Byte 0 (DWORD = 4-byte aligned) JEDEC Sector Map = 1ECh address |
| 35h | | 01h | Parameter Table Pointer Byte 1 |
| 36h | | 00h | Parameter Table Pointer Byte 2 |
| 37h | | FFh | Parameter ID MSB (FFh = JEDEC defined Parameter) |

器件标识

**表 91　　JEDEC SFDP Rev D 参数表**

| SFDP byte address | SFDP DWORD name | Data | Description |
|---|---|---|---|
| 100h | JEDEC Basic Flash Parameter DWORD-1 | F7h | Bits 7:5 = unused = 111b<br>Bit 4 = 1b<br>Bit 3 = Block Protect Bits are non-volatile / volatile = 0b<br>Bit 2 = Program Buffer > 64 Bytes = 1b<br>Bits 1:0 = Uniform 4KB erase is unavailable = 11b |
| 101h | | 21h | Bits 15:8 = 4KB erase instruction = 21h |
| 102h | | 8Ah | Bit 23 = Unused = 1b<br>Bit 22 = (1-1-4) Fast Read NOT supported = 0b<br>Bit 21 = (1-4-4) Fast Read NOT supported = 0b<br>Bit 20 = (1-2-2) Fast Read NOT supported = 0b<br>Bit19 = Supports DDR, Yes = 1b<br>Bit 18:17 = 3- or 4-Byte addressing (for example, defaults to 3-Byte mode; enters 4-Byte mode on command) = 01b<br>Bit 16 = (1-1-2) Fast Read NOT supported = 0b |
| 103h | | FFh | Bits 31:24 = Unused = FFh |
| 104h | JEDEC Basic Flash Parameter DWORD-2 | FFh | Density in bits, zero based, 512Mb = 1FFFFFFFh<br>Density in bits, zero based, 1Gb = 3FFFFFFFh |
| 105h | | FFh | |
| 106h | | FFh | |
| 107h | | 1Fh for 512Mb<br>3Fh for 1Gb | |
| 108h | JEDEC Basic Flash Parameter DWORD-3 | 00h | Not Supported |
| 109h | | 00h | |
| 10Ah | | 00h | |
| 10Bh | | 00h | |
| 10Ch | JEDEC Basic Flash Parameter DWORD-4 | 00h | Not Supported |
| 10Dh | | 00h | |
| 10Eh | | 00h | |
| 10Fh | | 00h | |
| 110h | JEDEC Basic Flash Parameter DWORD-5 | EEh | Bits 7:5 = Reserved = 111b<br>Bit 4 = Not Supported = 0b<br>Bit 3:1 = Reserved = 111b<br>Bits 0 = Not Supported = 0b |
| 111h | | FFh | Reserved |
| 112h | | FFh | |
| 113h | | FFh | |
| 114h | JEDEC Basic Flash Parameter DWORD-6 | FFh | Reserved |
| 115h | | FFh | |
| 116h | | 00h | Not Supported |
| 117h | | 00h | |

**表 91　　JEDEC SFDP Rev D 参数表（续）**

| SFDP byte address | SFDP DWORD name | Data | Description |
|---|---|---|---|
| 118h | JEDEC Basic Flash Parameter DWORD-7 | FFh | Reserved |
| 119h | | FFh | |
| 11Ah | | 00h | Not Supported |
| 11Bh | | 00h | |
| 11Ch | JEDEC Basic Flash Parameter DWORD-8 | 0Ch | Erase Type 1 Size, 4KB erase instruction = Erase type size = 2^N (where N = 12) = 0Ch |
| 11Dh | | 21h | Erase Type 1 Instruction |
| 11Eh | | 00h | Erase Type 2 Not Supported |
| 11Fh | | FFh | Erase Type 2 Not Supported |
| 120h | JEDEC Basic Flash Parameter DWORD-9 | 00h | Erase Type 3 Not Supported |
| 121h | | FFh | Erase Type 3 Not Supported |
| 122h | | 12h | Erase Type 4 Size, 256KB erase instruction = Erase type size = 2^N (where N = 18) = 12h |
| 123h | | DCh | Erase Type 4 Instruction |
| 124h | JEDEC Basic Flash Parameter DWORD-10 | 23h | Bits 31:30 = Erase type 4 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 128 ms = 10b Bits 29:25 = Erase type 4 Erase, Typical time count = 00101b Bits 24:23 = Erase type 3 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 1S = 11b (RFU) Bits 22:18 = Erase type 3 Erase, Typical time count = 11111b (RFU) Bits 17:16 = Erase type 2 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 1S = 11b (RFU) Bits 15:11 = Erase type 2 Erase, Typical time count = 11111b (RFU) Bits 10:9 = Erase type 1 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 16ms = 01b Bits 8:4 = Erase type 1 Erase, Typical time count = 00010b (typ erase time = count + 1 * units = 3 * 16 ms = 48 ms) Bits 3:0 = Count = (Max Erase time / (2 * Typical Erase time)) - 1 = 0011b |
| 125h | | FAh | |
| 126h | | FFh | |
| 127h | | 8Bh | |
| 128h | JEDEC Basic Flash Parameter DWORD-11 | 82h | Bits 31 = Reserved = 1b Bits 30:29 = Chip Erase Typical time units (00b: 16 ms, 01b: 256 ms, 10b: 4 s, 11b: 64 s) = 11b Bits 28:24 = Chip Erase Typical time count = 00011b (512M), and 00110b (1G) Bits 23:19 = Byte Program Typical Time, additional byte = 11111b Bits 18:14 = Byte Program Typical Time, first byte = 11111b Bits 13 = Page Program Typical Time unit (0: 8 µs, 1: 64 µs) = 64 µs = 1b Bits 12:8 = Page Program Typical Time Count = = 00111 Bits 7:4 = Page Size (256B) = 2^N bytes = 1000h Bits 3:0 = Count = [Max page program time / (2 * Typical page program time)] - 1 = 0010b |
| 129h | | E7 | |
| 12Ah | | FFh | |
| 12Bh | | E3h for 512Mb E6h for 1Gb | |

**表 91　　JEDEC SFDP Rev D 参数表（续）**

| SFDP byte address | SFDP DWORD name | Data | Description |
|---|---|---|---|
| 12Ch | JEDEC Basic Flash Parameter DWORD-12 | ECh | Bit 31 = Suspend and Resume supported = 0b<br>Bits 30:29 = Suspend in-progress erase max latency units (00b: 128 ns, 01b: 1 µs, 10b: 8 µs, 11b: 64 µs) = 8 µs =10b<br>Bits 28:24 = Suspend in-progress erase max latency count = 01001b = 10 * 8 µs = 80 µs<br>Bits 23:20 = Erase resume to suspend interval count = 0001b<br>Bits 19:18 = Suspend in-progress program max latency units (00b: 128 ns, 01b: 1 µs, 10b: 8 µs, 11b: 64 µs)<br>8 µs =10b<br>Bits 17:13 = Suspend in-progress program max latency count = 01001b = 10 * 8 µs = 80 µs<br>Bits 12:9 = Program resume to suspend interval count = 0001b<br>Bit 8 = Reserved = 1b<br>Bits 7:4 = Prohibited operations during erase suspend<br>= xxx0b: May not initiate a new erase anywhere (erase nesting not permitted)<br>+ xx1xb: May not initiate a page program in the erase suspended sector size<br>+ x1xxb: May not initiate a read in the erase suspended sector size<br>+ 1xxxb: The erase and program restrictions in bits 5:4 are sufficient = 1110b<br>Bits 3:0 = Prohibited Operations During Program Suspend<br>= xxx0b: May not initiate a new erase anywhere (erase nesting not permitted)<br>+ xx0xb: May not initiate a new page program anywhere (program nesting not permitted)<br>+ x1xxb: May not initiate a read in the program suspended page size<br>+ 1xxxb: The erase and program restrictions in bits 1:0 are sufficient = 1100b |
| 12Dh | | 23h | |
| 12Eh | | 19h | |
| 12Fh | | 49h | |
| 130h | JEDEC Basic Flash Parameter DWORD-13 | 7Ah | Bits 7:0 = Program Resume Instruction = 7Ah (1S-1S-1S) |
| 131h | | B0h | Bits 15:8 = Program Suspend Instruction = B0h |
| 132h | | 7Ah | Bits 23:16 = Erase Resume Instruction = 7Ah (1S-1S-1S) |
| 133h | | B0h | Bits 31:24 = Erase Suspend Instruction = B0h |
| 134h | JEDEC Basic Flash Parameter DWORD-14 | F7h | Bits 7:4 = RFU = Fh<br>Bit 3:2 = Status Register Polling Device Busy = 01b: Legacy status polling supported = Use legacy polling by reading the Status Register with 05h instruction and checking WIP bit[0] (0 = ready; 1 = busy).<br>Bits 1:0 = RFU = 11b |
| 135h | | 66h | Bit 31 = DPD Supported = supported = 0<br>Bits 30:23 = Enter DPD Instruction = B9h<br>Bits 22:15 = Exit DPD Instruction not supported = 00h<br>Bits 14:13 = Exit DPD to next operation delay units = (00b: 128 ns, 01b: 1 µs, 10b: 8 µs, 11b: 64 µs) = 64 µs = 11b<br>Bits 12:8 = Exit DPD to next operation delay count = 00110, Exit DPD to next operation delay = (count + 1) * units = (6 + 1) * 64 µs = 448 µs |
| 136h | | 80h | |
| 137h | | 5Ch | |

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**表 91　　JEDEC SFDP Rev D 参数表（续）**

| SFDP byte address | SFDP DWORD name | Data | Description |
|---|---|---|---|
| 138h | JEDEC Basic Flash Parameter DWORD-15 | 00h | Bits 31:24 = Reserved = FFh<br>Bit 23 = Hold or RESET Disable = Not Supported = 0b<br>Bits 22:0 = Not supported = 000000h |
| 139h | | 00h | |
| 13Ah | | 00h | |
| 13Bh | | FFh | |
| 13Ch | JEDEC Basic Flash Parameter DWORD-16 | F9h | Bit 7 = Reserved = 1<br>Bits 6:0 = Volatile or Non-volatile Register and Write Enable Instruction for Status Register 1<br>xxx_xxx1b: Non-volatile Status Register 1, powers-up to last written value, use instruction 06h to enable write.<br>+ xxx_1xxxb: Non-volatile/Volatile Status Register 1 powers-up to last written value in the non-volatile status register, use instruction 06h to enable write to non-volatile status register. Volatile status register may be activated after power-up to override the non-volatile status register, use instruction 50h to enable write and activate the volatile status register.<br>+ xx1_xxxxb: Status Register 1 contains a mix of volatile and non-volatile bits. The 06h instruction is used to enable writing of the register.<br>+ x1x_xxxxb: Reserved<br>+ 1xx_xxxxb: Reserved<br>= 1111001b |
| 13Dh | JEDEC Basic Flash Parameter DWORD-16 | 10h | Bits 23:14 = Exit 4-Byte Addressing<br>= xx_xx1x_xxxxb: Hardware reset<br>+ xx_x1xx_xxxxb: Software reset (see bits 13:8 in this DWORD)<br>+ xx_1xxx_xxxxb: Power cycle<br>+ x1_xxxx_xxxxb: Reserved<br>+ 1x_xxxx_xxxxb: Reserved<br>= 11_1110_0000b<br>Bits 13:8 = Soft Reset and Rescue Sequence Support<br>+ x1_xxxxb: issue reset enable instruction 66h, then issue reset instruction 99h. The reset enable, reset sequence may be issued on 1, 2, or 4 wires depending on the device operating mode.<br>= 010000b |
| 13Eh | JEDEC Basic Flash Parameter DWORD-16 | F8h | |
| 13Fh | JEDEC Basic Flash Parameter DWORD-16 | A1h | Bits 31:24 = Enter 4-byte Addressing<br>+ xxxx_xxx1b: Issue instruction B7h (Preceding write enable not required<br>+ xx1x_xxxxb: Supports dedicated 4-Byte address instruction set. Refer the vendor datasheet for the instruction set definition<br>+ 1xxx_xxxxb: Reserved = 1010_0001b |
| 140h | JEDEC Basic Flash Parameter DWORD-17 | 00h | |
| 141h | | 00h | |
| 142h | | 00h | |
| 143h | | 00h | |

**表 91　　JEDEC SFDP Rev D 参数表（续）**

| SFDP byte address | SFDP DWORD name | Data | Description |
|---|---|---|---|
| 144h | JEDEC Basic Flash Parameter DWORD-18 | 00h | Bit 31 = High byte and low byte of 16-bit words are in the same order when read in 1-1-1 mode and 8-8-8 mode = 0b<br>Bit 30:29 = The Command Extension is the same as the Command = 00b<br>Bit 28 = Reserved = 0b<br>Bit 27:26 = Not supported = 00b<br>Bits 25:24 = First rising edge of DS in the middle of the first data bit, start of first data bit aligned with the first falling edge of DS = 10b<br>Bit 23 = JEDEC SPI Protocol Reset Supported = 1b Bit 22:18 = 01111b<br>Bits 17:0 = Reserved = 00000h |
| 145h | | 00h | |
| 146h | | BCh | |
| 147h | | 02h | |
| 148h | JEDEC Basic Flash Parameter DWORD-19 | 00h | Not Supported |
| 149h | | 00h | |
| 14Ah | | 00h | |
| 14Bh | | 00h | |
| 14Ch | JEDEC Basic Flash Parameter DWORD-20 | FFh | Bits 31:28 = Maximum operation speed of device in 8D-8D-8D mode when utilizing Data Strobe = 1000b (200 MHz) / 0111b (166 MHz)<br>Bits 27:24 = 8D-8D-8D mode without using Data Strobe is not characterized = 1110b<br>Bits 23:20 = Maximum operation speed of device in 8S-8S-8S mode when utilizing Data Strobe = 1000b (200 MHz) / 0111b (166 MHz)<br>Bits 19:16 = 8S-8S-8S mode without using Data Strobe is not characterized = 1110b<br>Bit 15:0 = Not supported = FFFFh |
| 14Dh | | FFh | |
| 14Eh | | 8Eh for HS-T 7Eh for HL-T | |
| 14Fh | | 8Eh for HS-T 7Eh for HL-T | |

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**表 91　　JEDEC SFDP Rev D 参数表（续）**

| SFDP byte address | SFDP DWORD name | Data | Description |
|---|---|---|---|
| 150h | JEDEC 4-Byte Address Instruc- tions Parameter DWORD-1 | 41h | Supported = 1, Not Supported = 0<br>Bits 31:25 = Reserved = 1111_111b<br>Bit 24 = Support for (1-8-8) Page Program Command, Instruction<br>= 8Eh = 0b<br>Bit 23 = Support for (1-1-8) Page Program Command, Instruction<br>= 84h = 0b<br>Bit 22 = Support for (1-8-8) DTR READ Command, Instruction = FDh = 0b<br>Bit 21 = Support for (1-8-8) FAST_READ Command, Instruction = CCh = 0b<br>Insert<br>Bit 20 = Support for (1-1-8) FAST_READ Command, Instruction = 7Ch = 0b<br>Bit 19 = Support for non-volatile individual sector lock write command, Instruction = E3h = 1b<br>Bit 18 = Support for non-volatile individual sector lock read command, Instruction = E2h = 1b<br>Bit 17 = Support for volatile individual sector lock Write command, Instruction = E1h = 1b<br>Bit 16 = Support for volatile individual sector lock Read command, Instruction = E0h = 1b<br>Bit 15 = Support for (1-4-4) DTR_Read Command, Instruction = EEh = 0b<br>Bit 14 = Support for (1-2-2) DTR_Read Command, Instruction = BEh = 0b<br>Bit 13 = Support for (1-1-1) DTR_Read Command, Instruction = 0Eh = 0b<br>Bit 12 = Support for Erase Command – Type 4 = 1b Bit 11 = Support for Erase Command – Type 3 = 0b Bit 10 = Support for Erase Command – Type 2 = 0b Bit 9 = Support for Erase Command – Type 1 = 1b<br>Bit 8 = Support for (1-4-4) Page Program Command, Instruction = 3Eh = 0b<br>Bit 7 = Support for (1-1-4) Page Program Command, Instruction = 34h = 0b<br>Bit 6 = Support for (1-1-1) Page Program Command, Instruction = 12h = 1b<br>Bit 5 = Support for (1-4-4) FAST_READ Command, Instruction = ECh = 0b<br>Bit 4 = Support for (1-1-4) FAST_READ Command, Instruction = 6Ch = 0b<br>Bit 3 = Support for (1-2-2) FAST_READ Command, Instruction = BCh = 0b<br>Bit 2 = Support for (1-1-2) FAST_READ Command, Instruction = 3Ch = 0b<br>Bit 1 = Support for (1-1-1) FAST_READ Command, Instruction = 0Ch = 0b<br>Bit 0 = Support for (1-1-1) READ Command, Instruction = 13h = 1b |
| 151h | | 12h | |
| 152h | | 0F | |
| 153h | | FE | |

**表 91　　JEDEC SFDP Rev D 参数表（续）**

| SFDP byte address | SFDP DWORD name | Data | Description |
|---|---|---|---|
| 154h | JEDEC 4-Byte Address Instruc- tions Parameter DWORD-2 | 21h | Bits 31:24 = DCh = Instruction for Erase Type 4<br>Bits 23:16 = Instruction for Erase Type 3: RFU<br>Bits 15:8 = Instruction for Erase Type 2: RFU<br>Bits 7:0 = 21h = Instruction for Erase Type 1 |
| 155h | | FFh | |
| 156h | | FFh | |
| 157h | | DCh | |
| 158h | JEDEC xSPI Profile 1.0 DWORD-1 | 00h | Bits 7:0 = Read Fast Wrapped command not supported = 00h |
| 159h | | EEh | Bits 15:8 = Read Fast command = EEh (DDR Read) |
| 15Ah | | 80h | Bit 23 = Number of Additional Modifier Bytes Used for Write any Register command = 4 bytes = 1b<br>Bit 22 = Number of Data Bytes Used for Write Register command<br>=<br>1 byte = 0b<br>Bits 21:16 = Reserved = 000000b |
| 15Bh | | 0Bh | Bit 31 = xSPI Support, Device implements the SFDP command in 8D-8D-8D protocol mode as defined in the Jedec xSPI spec = 0b<br>Bit 30 = SFDP Command in 8D-8D-8D mode – Dummy Cycles = 8 bytes = 0b<br>Bit 29 = Number of Additional Modifier Bytes Used for Read Status Register command = 0 bytes = 0b<br>Bit 28 = Initial Latency (CK cycles) for Read Status Register command = 3 CK Cycle = 0b<br>Bit 27 = Number of Additional Modifier Bytes Used for Read Register command = 4 bytes = 1b<br>Bit 26 = Initial Latency (CK cycles) for Read Volatile Register command = 4CK = 0b<br>Bit 25 = Initial Latency (CK cycles) for Read Volatile Non-Register command = 8 CK cycles = 1b<br>Bit 24 = Number of Additional Modifier Bytes Used for Write Status-Cfg Register command= 4 bytes = 1b |
| 15Ch | JEDEC xSPI Profile 1.0 DWORD-2 | 71h | Write Non-volatile Register command |
| 15Dh | | 71h | Write Volatile Register command |
| 15Eh | | 65h | Read NV Register command |
| 15Fh | | 65h | Read Volatile Register command |

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**表 91　　JEDEC SFDP Rev D 参数表（续）**

| SFDP byte address | SFDP DWORD name | Data | Description |
|---|---|---|---|
| 160h | JEDEC xSPI Profile 1.0 DWORD-3 | 00h | Bits 7:0 = Reserved = 00h |
| 161h | | B0h | Bit 31 = Read SFDP 8D-8D-8D command supported = 1b<br>Bit 30 = Read Fast Wrapped command not supported = 0b<br>Bit 29 = Setup Read Wrap command not supported = 0b<br>Bit 28 = Erase 4KB command supported = 1b<br>Bit 27 = Erase 32KB command not supported = 0b<br>Bit 26 = Erase Chip command supported = 1b<br>Bit 25 = Read Configuration Register command supported = 1b<br>Bit 24 = Read Flag Status Register command not supported = 0b<br>Bit 23 = Read Register command supported = 1b<br>Bit 22 = Read Volatile Register command supported = 1b<br>Bit 21 = Read NV Register command supported = 1b<br>Bit 20 = Write Status-Configuration Register command supported = 1b<br>Bit 19 = Clear Flag Status Reg command supported = 1b<br>Bit 18 = Write Register command supported = 1b<br>Bit 17 = Write volatile register command supported = 1b<br>Bit 16 = Write NV register command supported = 1b<br>Bit 15 = Enter Deep Power Down command not supported = 1b<br>Bit 14 = Exit Deep Power Down command not supported = 0b<br>Bit 13 = Soft Reset command supported = 1b<br>Bit 12 = Reset Enable command supported = 1b<br>Bit 11 = Soft Reset and Enter default protocol mode command supported = 0b<br>Bit 10 = Enter default protocol mode command not supported = 0b<br>Bits 9:8 = Reserved = 00b |
| 162h | | FFh | |
| 163h | | 96h | |
| 164h | JEDEC xSPI Profile 1.0 DWORD-4 | A8h | Bits 31:12 = 00000h<br>Bits 11:7 = 200MHz operation: number of dummy cycles required = 23 = 10111b<br>Bit 6:2 = 200MHz operation: configuration bit pattern to set this number of dummy cycles = 01010b<br>Bits 1:0 = Reserved = 00b |
| 165h | | 0Bh | |
| 166h | | 00h | |
| 167h | | 00h | |
| 168h | JEDEC xSPI Profile 1.0 DWORD-5 | 0Ch | Bits 31:27 = 166 MHz operation: number of dummy cycles required = 20 = 10100b<br>Bit 26:22 = 166 MHz operation: configuration bit pattern to set this number of dummy cycles = 01000b<br>Bits 21:17 = 133 MHz operation: number of dummy cycles required = 14 = 01110b<br>Bit 16:12 = 133 MHz operation: configuration bit pattern to set this number of dummy cycles = 00101b<br>Bits 11:7 = 100 MHz operation: number of dummy cycles required = 10 = 01010b<br>Bit 6:2 = 100 MHz operation: configuration bit pattern to set this number of dummy cycles = 00011b<br>Bits 1:0 = Reserved = 00b |
| 169h | | 55h | |
| 16Ah | | 1Ch | |
| 16Bh | | A2h | |
| 16Ch | Status, Control and Configuration Register Map DWORD-1 | 00h | Bits 31:0 = Address offset for volatile registers = 00800000h |
| 16Dh | | 00h | |
| 16Eh | | 80h | |
| 16Fh | | 00h | |

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**表 91　　JEDEC SFDP Rev D 参数表（续）**

| SFDP byte address | SFDP DWORD name | Data | Description |
|---|---|---|---|
| 170h | Status, Control and Configuration Register Map DWORD-2 | 00h | Bits 31:0 = Address offset for non-volatile registers = 00000000h |
| 171h | | 00h | |
| 172h | | 00h | |
| 173h | | 00h | |
| 174h | Status, Control and Configuration Register Map DWORD-3 | C0h | Bit 31 = Generic Addressable Read Status/Control register command for volatile registers supported for some (or all) registers = 1b<br>Bit 30 = Generic Addressable Write Status/Control register command for volatile registers supported for some (or all) registers = 1b<br>Bits 29:28 = Number of address bytes used for Generic Addressable Read/Write Status/Control register commands for volatile registers =<br>3 byte (default) = 10b<br>Bit 27:26 = Number of dummy bytes used for Generic Addressable Read Status/Control register command for volatile registers in (1S-1S-1S) mode = 10b<br>Bit 25:14 = Not supported = FFFh<br>Bit 13:10 = Number of dummy cycles used for Generic Addressable Read Status/Control register command for volatile registers in (8S-8S-8S) mode = 3 = 0011b<br>Bit 9:6 = Number of dummy cycles used for Generic Addressable Read Status/Control register command for volatile registers in (8D-8D-8D) mode = 3 = 0011b<br>Bit 5:4 = Reserved = 00b<br>Bit 3:0 = Number of dummy cycles used for Generic Addressable Read Status/Control register command for volatile registers in (1S-1S-1S) mode = 0000b |
| 175h | | CCh | |
| 176h | | FFh | |
| 177h | | EBh | |

**表 91　　JEDEC SFDP Rev D 参数表（续）**

| SFDP byte address | SFDP DWORD name | Data | Description |
|---|---|---|---|
| 178h | Status, Control and Configuration Register Map DWORD-4 | 88h | Bit 31 = Generic Addressable Read Status/Control register command for non-volatile registers supported for some (or all) registers = 1b<br>Bit 30 = Generic Addressable Write Status/Control register command for non-volatile registers supported for some (or all) registers = 1b<br>Bits 29:28 = Number of address bytes used for Generic Addressable Read/Write Status/Control register commands for non-volatile registers = 3 byte (default) = 10b<br>Bit 27:26 = Number of dummy bytes used for Generic Addressable Read Status/Control register command for non-volatile registers in (1S-1S-1S) mode = 10b<br>Bit 25:14 = Not supported = FFFh<br>Bit 13:10 = Number of dummy cycles used for Generic Addressable Read Status/Control register command for non-volatile registers in (8S-8S-8S) mode = 20 = 1110b (Max available option is 14 cycles)<br>Bit 9:6 = Number of dummy cycles used for Generic Addressable Read Status/Control register command for non-volatile registers in (8D-8D-8D) mode = 20 = 1110b (Max available option is 14 cycles)<br>Bit 5:4 = Reserved = 00b<br>Bit 3:0 = Number of dummy cycles used for Generic Addressable Read Status/Control register command for non-volatile registers in (1S-1S-1S) mode = 1000b |
| 179h | | FBh | |
| 17Ah | | FFh | |
| 17Bh | | EBh | |
| 17Ch | Status, Control and Configuration Register Map DWORD-5 | 00h | Bits 7:0 = Command used for write access = read only = 00h |
| 17Dh | | 65h | Bits 15:8 = Command used for read access = 65h |
| 17Eh | | 00h | Bits 23:16 = Address of register where WIP is located = 00h (status reg -1 volatile) |
| 17Fh | | 90h | Bit 31 = Write In Progress (WIP) bit is supported = 1b<br>Bit 30 = Write In Progress polarity, WIP = 1 indicates write is in progress = 0b<br>Bits 29 = Reserved = 0b<br>Bits 28 = Bit is set /cleared by commands using address = 1b<br>Bit 27 = Not supported = 0b<br>Bits 26:24 = Bit location of WIP bit in register = bit [0] = 000b |
| 180h | Status, Control and Configuration Register Map DWORD-6 | 06h | Bits 7:0 = Command used for write access |
| 181h | | 05h | Bits 15:8 = Command used for read access |
| 182h | | 00h | Bits 23:16 = Address of register where WEL is located = 00h (status reg -1 volatile) |
| 183h | | A1h | Bit 31 = Write Enable (WEL) bit is supported = 1b<br>Bit 30 = Write Enable polarity, WEL = 1 means write is in progress = 0b<br>Bits 29 = Write command is a direct command to wet WEL bit = 1b<br>Bits 28 = Bit is accessed by direct commands to set WEL bit = 1b<br>Bit 27 = Local address for WEL bit is found in last byte of the address = 0b<br>Bits 26:24 = Bit location of WEL bit in register = bit [1] = 001b |

**表 91　　JEDEC SFDP Rev D 参数表（续）**

| SFDP byte address | SFDP DWORD name | Data | Description |
|---|---|---|---|
| 184h | Status, Control and Configuration Register Map DWORD-7 | 00h | Bits 7:0 = Command used for write access = read only = 00h = Read Only |
| 185h | | 65h | Bits 15:8 = Command used for read access = 65h |
| 186h | | 00h | Bits 23:16 = Address of register where Program Error is located = 00h (status reg -1 volatile) |
| 187h | | 96h | Bit 31 = Program Error bit supported = 1b<br>Bit 30 = Positive polarity (Program Error = 0 indicates no error, Program Error = 1 indicates last Program operation created an error) = 0b<br>Bit 29 = The device has separate bits for Program Error and Erase Error = 0b<br>Bits 28 = Bit is set/cleared by commands using address = 1b<br>Bit 27 = Not Supported = 0b<br>Bits 26:24 = Bit location of Program Error bit in register = bit [6] = 110b |
| 188h | Status, Control and Configuration Register Map DWORD-8 | 00h | Bits 7:0 = Command used for write access = read only = 00h = Read Only |
| 189h | | 65h | Bits 15:8 = Command used for read access = 65h |
| 18Ah | | 00h | Bits 23:16 = Address of register where Erase Error is located = 00h |
| 18Bh | | 95h | Bit 31 = Erase Error bit supported = 1b<br>Bit 30 = Positive polarity Erase Error = 0 indicates no error, Erase Error = 1 indicates last erase operation created an error) = 0b<br>Bit 29 = The device has separate bits for Program Error and Erase Error = 0b<br>Bits 28 = Bit is set/cleared by commands using address = 1b<br>Bit 27 = Not Supported = 0b<br>Bits 26:24 = Bit location of erase Error bit in register = bit [5] = 101b |
| 18Ch | Status, Control and Configuration Register Map DWORD-9 | 71h | Bits 7:0 = Command used for write access = read only = 71h |
| 18Dh | | 65h | Bits 15:8 = Command used for read access = 65h |
| 18Eh | | 03h | Address of register where wait states bits are located = 03h (Configuration Reg - 2 Non-volatile) |
| 18Fh | | D0h | Bit 31 = Variable number of dummy cycles supported = 1b<br>Bits 30:29 = Number of physical bits used to set wait states - 4 bit = 10b<br>Bits 28 = Bit is set/cleared by commands using address = 1b<br>Bit 27 = Not Supported = 0b<br>Bits 26:24 = Bit location of LSB of physical bits in register = bit [0] = 000b |

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**表 91　　JEDEC SFDP Rev D 参数表（续）**

| SFDP byte address | SFDP DWORD name | Data | Description |
|---|---|---|---|
| 190h | Status, Control and Configuration Register Map DWORD-10 | 71h | Bits 7:0 = Command used for write access = 71h |
| 191h | | 65h | Bits 15:8 = Command used for read access = 65h |
| 192h | | 03h | Address of register where wait states bits are located = 03h (Configuration Reg - 2 non-volatile) |
| 193h | | D0h | Bit 31 = Variable number of dummy cycles supported = 1b<br>Bits 30:29 = Number of physical bits used to set wait states - 4 bit = 10b<br>Bits 28 = Bit is set/cleared by commands using address = 1b<br>Bit 27 = Not Supported = 0b<br>Bits 26:24 = Bit location of LSB of physical bits in register = bit [0] = 000b |
| 194h | Status, Control and Configuration Register Map DWORD-11 | A4h | Bit 31 = 30 dummy cycles supported = 0b<br>Bit 30:26 = Bit pattern used to set 30 dummy cycles = 00000b<br>Bit 25 = 28 dummy cycles supported = 1b<br>Bit 24:20 = Bit pattern used to set 28 dummy cycles = 01111b<br>Bit 19 = 26 dummy cycles supported = 1b<br>Bit 18:14 = Bit pattern used to set 26 dummy cycles = 01101b<br>Bit 13 = 24 dummy cycles supported = 1b<br>Bit 12:8 = Bit pattern used to set 24 dummy cycles = 01011b Bit 7 = 22 dummy cycles supported = 1b<br>Bit 6:2 = Bit pattern used to set 22 dummy cycles = 01001b<br>Bits 1:0 = Reserved = 00b |
| 195h | | 6Bh | |
| 196h | | FBh | |
| 197h | | 02h | |
| 198h | Status, Control and Configuration Register Map DWORD-12 | 90h | Bit 31 = 20 dummy cycles supported = 1b<br>Bit 30:26 = Bit pattern used to set 20 dummy cycles = 01000b<br>Bit 25 = 18 dummy cycles supported = 1b<br>Bit 24:20 = Bit pattern used to set 18 dummy cycles = 00111b<br>Bit 19 = 16 dummy cycles supported = 1b<br>Bit 18:14 = Bit pattern used to set 16 dummy cycles = 00110b<br>Bit 13 = 14 dummy cycles supported = 1b<br>Bit 12:8 = Bit pattern used to set 14 dummy cycles = 00101b<br>Bit 7 = 12 dummy cycles supported = 1b<br>Bit 6:2 = Bit pattern used to set 12 dummy cycles = 00100b<br>Bits 1:0 = Reserved = 00b |
| 199h | | A5h | |
| 19Ah | | 79h | |
| 19Bh | | A2h | |
| 19Ch | Status, Control and Configuration Register Map DWORD-13 | 00h | Bit 31 = 10 dummy cycles supported = 1b<br>Bit 30:26 = Bit pattern used to set 10 dummy cycles = 00011b<br>Bit 25 = 8 dummy cycles supported = 1b<br>Bit 24:20 = Bit pattern used to set 8 dummy cycles = 00010b<br>Bit 19 = 6 dummy cycles supported = 1b<br>Bit 18:14 = Bit pattern used to set 6 dummy cycles = 00001b<br>Bit 13 = 4 dummy cycles supported = 0b<br>Bit 12:8 = Bit pattern used to set 4 dummy cycles = 00000b<br>Bit 7 = 2 dummy cycles supported = 0b<br>Bit 6:2 = Bit pattern used to set 2 dummy cycles = 00000b<br>Bits 1:0 = Reserved = 00b |
| 19Dh | | 40h | |
| 19Eh | | 28h | |
| 19Fh | | 8Eh | |
| 1A0h | Status, Control and Configuration Register Map DWORD-14 | 00h | Not Supported |
| 1A1h | | 00h | |
| 1A2h | | FFh | |
| 1A3h | | 00h | |

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**表 91　　JEDEC SFDP Rev D 参数表（续）**

| SFDP byte address | SFDP DWORD name | Data | Description |
|---|---|---|---|
| 1A4h | Status, Control and Configuration Register Map DWORD-15 | 00h | Not Supported |
| 1A5h | | 00h | |
| 1A6h | | FFh | |
| 1A7h | | 00h | |
| 1A8h | Status, Control and Configuration Register Map DWORD-16 | 71h | Bits 7:0 = Command used for write access = 71h |
| 1A9h | | 65h | Bits 15:8 = Command used for read access = 65h |
| 1AAh | | 06h | Bits 23:16 = Address of register where Octal Mode Enable volatile bit is located = 800006h<br>(Configuration Reg - 5 volatile) |
| 1ABh | | 90h | Bit 31 = Octal Mode Enable volatile bit supported = 1b<br>Bits 30 = Octal Mode Enable volatile bit polarity: Positive (Octal Mode Enable bit = 1 indicates Octal mode is enabled) = 0b<br>Bits 29 = Reserved = 0b<br>Bits 28 = Bit is set/cleared by commands using address = 1b<br>Bit 27 = Not supported = 0b<br>Bits 26:24 = Bit location of Octal Mode enable bit in register = bit [0] = 000b |
| 1ACh | Status, Control and Configuration Register Map DWORD-17 | 71h | Bits 7:0 = Command used for write access = 71h |
| 1ADh | | 65h | Bits 15:8 = Command used for read access = 65h |
| 1AEh | | 06h | Address of register where Octal Mode Enable non-volatile bit is located = 06h (Configuration Reg - 5 non-volatile) |
| 1AFh | | 90h | Bit 31 = Octal Mode Enable non-volatile bit supported = 1b<br>Bits 30 = Octal Mode Enable non-volatile bit polarity: Positive (Octal Mode Enable bit = 1 indicates Octal mode is enabled) = 0b<br>Bit 29 = No OTP Bit = 0b<br>Bits 28 = Bit is set/cleared by commands using address = 1b<br>Bit 27 = Not supported = 0b<br>Bits 26:24 = Bit location of Octal Mode enable bit in register = bit [0] = 000b |
| 1B0h | Status, Control and Configuration Register Map DWORD-18 | 00h | Not Supported |
| 1B1h | | 00h | |
| 1B2h | | 00h | |
| 1B3h | | 00h | |
| 1B4h | Status, Control and Configuration Register Map DWORD-19 | 00h | Not Supported |
| 1B5h | | 00h | |
| 1B6h | | 00h | |
| 1B7h | | 00h | |

**表 91　　JEDEC SFDP Rev D 参数表（续）**

| SFDP byte address | SFDP DWORD name | Data | Description |
|---|---|---|---|
| 1B8h | Status, Control and Configuration Register Map DWORD-20 | 71h | Bits 7:0 = Command used for write access = 71h |
| 1B9h | | 65h | Bits 15:8 = Command used for read access = 65h |
| 1BAh | | 06h | Address of register where STR Octal Mode Enable bit is located = 800006h (Configuration Reg - 5 Volatile) |
| 1BBh | | D1h | Bit 31 = STR Octal Mode Enable volatile bit supported = 1b<br>Bits 30 = STR Octal Mode Enable volatile bit polarity: Inverted (STR Octal Mode Enable = 0 indicates STR Octal Mode is enabled) = 1b<br>Bit 29 = Reserved = 0b<br>Bits 28 = Bit is set/cleared by commands using address = 1b<br>Bit 27 = Not supported = 0b<br>Bits 26:24 = Bit location of STR Octal Mode Enable bit in register = bit [1] = 001b |
| 1BCh | Status, Control and Configuration Register Map DWORD-21 | 71h | Bits 7:0 = Command used for write access = 71h |
| 1BDh | | 65h | Bits 15:8 = Command used for read access = 65h |
| 1BEh | | 06h | Address of register where STR Octal Mode Enable bit is located = 06h (Configuration Reg - 5 Non-volatile) |
| 1BFh | | D1h | Bit 31 = STR Octal Mode Enable non-volatile bit supported = 1b<br>Bits 30 = STR Octal Mode Enable non-volatile bit polarity: Inverted (STR Octal Mode Enable = 0 indicates STR Octal Mode is enabled) = 1b<br>Bit 29 = No OTP Bit = 0b<br>Bits 28 = Bit is set/cleared by commands using address = 1b<br>Bit 27 = Not supported = 0b<br>Bits 26:24 = Bit location of STR Octal Mode Enable non-volatile bit in register = bit [1] = 001b |
| 1C0h | Status, Control and Configuration Register Map DWORD-22 | 71h | Bits 7:0 = Command used for write access = 71h |
| 1C1h | | 65h | Bits 15:8 = Command used for read access = 65h |
| 1C2h | | 06h | Address of register where DTR Octal Mode Enable volatile bit is located = 800006h (Configuration Reg - 5 Volatile) |
| 1C3h | | 91h | Bit 31 = DTR Octal Mode Enable volatile bit supported = 1b<br>Bits 30 = DTR Octal Mode Enable volatile bit polarity positive (DSTR Octal Mode Enable = 1 indicates DTR Octal Mode is enabled) = 0b<br>Bit 29 = Reserved = 0b<br>Bits 28 = Bit is set/cleared by commands using address = 1b<br>Bit 27 = Not supported = 0b<br>Bits 26:24 = Bit location of DTR Octal Mode Enable volatile bit in register = bit [1] = 001b |

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**表 91　　JEDEC SFDP Rev D 参数表（续）**

| SFDP byte address | SFDP DWORD name | Data | Description |
|---|---|---|---|
| 1C4h | Status, Control and Configuration Register Map DWORD-23 | 71h | Bits 7:0 = Command used for write access = 71h |
| 1C5h | | 65h | Bits 15:8 = Command used for read access = 65h |
| 1C6h | | 06h | Address of register where DTR Octal Mode Enable non-volatile bit is located = 06h<br>(Configuration Reg - 5 non-volatile) |
| 1C7h | | 91h | Bit 31 = DTR Octal Mode Enable non-volatile bit supported = 1b<br>Bits 30 = DTR Octal Mode Enable non-volatile bit polarity positive (DSTR Octal Mode Enable = 1 indicates DTR Octal Mode is enabled) = 0b<br>Bit 29 = No OTP Bit = 0b<br>Bits 28 = Bit is set/cleared by commands using address = 1b<br>Bit 27 = Not supported = 0b<br>Bits 26:24 = Bit location of DTR Octal Mode Enable bit in register = bit [1] = 001b |
| 1C8h | Status, Control and Configuration Register Map DWORD-24 | 00h | Not Supported |
| 1C9h | | 00h | |
| 1CAh | | FFh | |
| 1CBh | | 00h | |
| 1CCh | Status, Control and Configuration Register Map DWORD-25 | 00h | Not Supported |
| 1CDh | | 00h | |
| 1CEh | | FFh | |
| 1CFh | | 00h | |
| 1D0h | Status, Control and Configuration Register Map DWORD-26 | 71h | Bits 7:0 = Command used for write access = 71h |
| 1D1h | | 65h | Bits 15:8 = Command used for read access = 65h |
| 1D2h | | 05h | Address of register where Output Driver Strength volatile bits are located = 800005h (Configuration Reg - 4 Volatile) |
| 1D3h | | D5h | Bits 31: 30 = Number of physical bits used to set Output Driver Strength = 3 bits = 11b<br>Bit 29 = Reserved = 0b<br>Bits 28 = Bit is set/cleared by commands using address = 1b<br>Bit 27 = Not Supported = 0b<br>Bits 26:24 = Bit location of Least Significant Output Driver Strength bit in register = bit [5] = 101b |
| 1D4h | Status, Control and Configuration Register Map DWORD-27 | 71h | Bits 7:0 = Command used for write access = 71h |
| 1D5h | | 65h | Bits 15:8 = Command used for read access = 65h |
| 1D6h | | 05h | Address of register where Output Driver Strength non-volatile bits are located = 05h<br>(Configuration Reg - 4 non- volatile) |
| 1D7h | | D5h | Bits 31: 30 = Number of physical bits used to set Output Driver Strength = 3 bits = 11b<br>Bit 29 = Reserved = 0b<br>Bits 28 = Bit is set/cleared by commands using address = 1b<br>Bit 27 = Not Supported = 0b<br>Bits 26:24 = Bit location of Least Significant Output Driver Strength bit in register = bit [5] = 101b |

**表 91　　JEDEC SFDP Rev D 参数表（续）**

| SFDP byte address | SFDP DWORD name | Data | Description |
|---|---|---|---|
| 1D8h | Status, Control and Configuration Register Map DWORD-28 | 00h | Bit 7:0 = Reserved = 00h |
| 1D9h | | 00h | Bit 15:8 = Reserved = 00h |
| 1DAh | | A0h | Bits 31:29 = Bit pattern to support Driver type 0 = 45 Ohms = 000b<br>Bits 28:26 = Bit pattern to support Driver type 1 = 30 Ohm = 101b<br>Bits 25:23 = Bit pattern to support Driver type 2 = 60 Ohm = 011b<br>Bits 22:20 = Bit pattern to support Driver type 3 = 90 Ohm = 010b<br>Bits 19:17 = Bit pattern to support Driver type 4 = Not supported = 000b<br>Bit 16 = Reserved = 0b |
| 1DBh | | 15h | |
| 1DCh | Command Sequences to Change to Octal DDR (8D-8D-8D) mode DWORD-1 | 00h | Bits 7:0 = Byte 3 of first command sequence |
| 1DDh | | 00h | Bits 15:8 = Byte 2 of first command sequence |
| 1DEh | | 06h | Bits 23:16 = Byte 1 of first command sequence |
| 1DFh | | 01h | Bits 31:24 = Length of first command sequence = 1 byte |
| 1E0h | Command Sequences to Change to Octal DDR (8D-8D-8D) mode DWORD-2 | 00h | Bits 7:0 = Byte 7 of first command sequence |
| 1E1h | | 00h | Bits 15:8 = Byte 6 of first command sequence |
| 1E2h | | 00h | Bits 23:16 = Byte 5 of first command sequence |
| 1E3h | | 00h | Bits 31:24 = Byte 4 of first command sequence |
| 1E4h | Command Sequences to Change to Octal DDR (8D-8D-8D) mode DWORD-3 | 00h | Bits 7:0 = Byte 3 of second command sequence - volatile register address |
| 1E5h | | 80h | Bits 15:8 = Byte 2 of second command sequence - volatile register address |
| 1E6h | | 71h | Bits 23:16 = Byte 1 of second command sequence |
| 1E7h | | 05h | Bits 31:24 = Length of second command sequence = 5 bytes |
| 1E8h | Command Sequences to Change to Octal DDR (8D-8D-8D) mode DWORD-4 | 00h | Bits 7:0 = Byte 7 of second command sequence |
| 1E9h | | 00h | Bits 15:8 = Byte 6 of second command sequence |
| 1EAh | | 43h | Bits 23:16 = Byte 5 of second command sequence |
| 1EBh | | 06h | Bits 31:24 = Byte 4 of second command sequence - volatile register address |

### 扇区映射参数表说明

表 92 提供了一种方法来识别器件地址映射的配置方式，并为每个支持的配置提供扇区映射。这是通过定义一系列指令来读取影响地址映射选择的相关配置寄存器位来完成的。当必须读取多个配置位时，所有位都连接成一个索引值，用于选择当前地址映射。

为了识别器件中的扇区图配置，按以下 MSb 到 LSb 的顺序读取以下配置位，以形成配置图索引值：

- CFR3V[3] - 0 = 混合架构，1 = 统一架构
- CFR1V[2] - 0 = 底部有 4 KB 参数扇区，1 = 顶部有 4 KB 扇区
- CFR1V[6] - 0 = 4KB 参数扇区组合在一起，1 = 4 KB 扇区分别位于底部和顶部
- 某些配置位的值可能会使其他配置位值不相关（无关紧要），因此并非所有可能的索引值组合都能定义有效的地址映射。SFDP 扇区映射参数表仅支持选定的配置位组合（参见表 93）。使用此 SFDP 参数表确定扇区映射时，不得使用其他组合来配置扇区地址映射。支持以下索引值组合。

**表 92　　扇区映射参数**

| CFR3V[3] | CFR1V[6] | CFR1V[2] | Index value | Description |
|---|---|---|---|---|
| 0 | 0 | 0 | 00h | 4 KB sectors at bottom with remainder 256 KB sectors |
| 0 | 0 | 1 | 01h | 4 KB sectors at top with remainder 256 KB sectors |
| 0 | 1 | 0 | 02h | 4 KB sectors split between top and bottom with remainder 256 KB sectors |
| 1 | 0 | 0 | 04h | Uniform 256 KB sectors |

**表 93　　JEDEC SFDP Rev D，扇区映射参数**

| SFDP byte address | SFDP DWORD name | Data | Description |
|---|---|---|---|
| 1ECh | JEDEC Sector Map Parameter DWORD-1 Config. Detect-1 | FCh | Config. Detect -1 Uniform 256 KB Sectors or Hybrid Sectors<br>Bits 31:24 = Read data mask = 0000_1000b: Select bit 3 of the data byte for UNHYSA value 0 = Hybrid map with 4KB parameter sectors 1 = Uniform map<br>Bits 23:22 = Configuration detection command address length = 11b: Variable length<br>Bits 21:20 = RFU = 11b<br>Bits 19:16 = Configuration detection command latency = 1111b: variable latency<br>Bits 15:8 = Configuration detection instruction = 65h: Read any register<br>Bits 7:2 = RFU = 111111b<br>Bit 1 = Command Descriptor = 0<br>Bit 0 = Not the end descriptor = 0 |
| 1EDh | | 65h | |
| 1EEh | | FFh | |
| 1EFh | | 08h | |
| 1F0h | JEDEC Sector Map Parameter DWORD-2 Config. Detect-1 | 04h | Bits 31:0 = Address Value Configuration Register 3 (bit 3) = 00800004h |
| 1F1h | | 00h | |
| 1F2h | | 80h | |
| 1F3h | | 00h | |
| 1F4h | JEDEC Sector Map Parameter DWORD-3 Config. Detect-2 | FCh | Config. Detect-2 4 KB Hybrid Sectors Split between Top and Bottom<br>Bits 31:24 = Read data mask = 0100_0000b: Select bit 6 of the data byte for SP4KBS value<br>0 = 4 KB parameter sectors are grouped together<br>1 = 4 KB parameter sectors are split between High and Low Addresses<br>Bits 23:22 = Configuration detection command address length = 11b: Variable length<br>Bits 21:20 = RFU = 11b<br>Bits 19:16 = Configuration detection command latency = 1111b: variable latency<br>Bits 15:8 = Configuration detection instruction = 65h: Read any register<br>Bits 7:2 = RFU = 111111b<br>Bit 1 = Command Descriptor = 0<br>Bit 0 = Not the end descriptor = 0 |
| 1F5h | | 65h | |
| 1F6h | | FFh | |
| 1F7h | | 40h | |
| 1F8h | JEDEC Sector Map Parameter DWORD-4 Config. Detect-2 | 02h | Bits 31:0 = Address Value Configuration Register 1 (bit 6)= 00800002h |
| 1F9h | | 00h | |
| 1FAh | | 80h | |
| 1FBh | | 00h | |

**表 93　　JEDEC SFDP Rev D，扇区映射参数（续）**

| SFDP byte address | SFDP DWORD name | Data | Description |
|---|---|---|---|
| 1FCh | JEDEC Sector Map Parameter DWORD-5 Config. Detect-3 | FDh | Config Detect-3 4 KB Hybrid Sectors on Top or Bottom<br>Bits 31:24 = Read data mask = 0000_0100b: Select bit 2 of the data byte for TB4KBS value<br>0 = 4 KB parameter sectors at bottom<br>1 = 4 KB parameter sectors at top<br>Bits 23:22 = Configuration detection command address length = 11b: Variable length<br>Bits 21:20 = RFU = 11b<br>Bits 19:16 = Configuration detection command latency = 1111b: variable latency<br>Bits 15:8 = Configuration detection instruction = 65h: Read any register<br>Bits 7:2 = RFU = 111111b<br>Bit 1 = Command Descriptor = 0<br>Bit 0 = End of command descriptor = 1 |
| 1FDh | | 65h | |
| 1FEh | | FFh | |
| 1FFh | | 04h | |
| 200h | JEDEC Sector Map Parameter DWORD-6 Config. Detect-3 | 02h | Bits 31:0 = Address Value Configuration Register 1 (bit 2)= 00800002h |
| 201h | | 00h | |
| 202h | | 80h | |
| 203h | | 00h | |
| 204h | JEDEC Sector Map Parameter DWORD-7 Config-0 Header | FEh | Configuration Index 00h 4 KB sectors at bottom with remainder 256 KB<br>Bits 31:24 = RFU = FFh<br>Bits 23:16 = Region count (DWORDs -1) = 02h: Three regions<br>Bits 15:8 = Configuration ID = 00h, 4KB sectors bottom with remainder 256 KB<br>Bits 7:2 = RFU = 111111b<br>Bit 1 = Map Descriptor = 1<br>Bit 0 = Not the end descriptor = 0 |
| 205h | | 00h | |
| 206h | | 02h | |
| 207h | | FFh | |
| 208h | JEDEC Sector Map Parameter DWORD-8 Config-0 Region-0 | F1h | Region 0 of 4 KB sectors<br>Bits 31:8 = Region size (32 4 KB) = 0001FFh: Region size as count-1 of 256 Byte units = 32 x 4 KB sectors = 128 KB Count = 128KB/256<br>= 512, value = count -1 = 512 – 1 = 511 = 1FFh<br>Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1<br>Bit 3 = Erase Type 4 support = 0b ---Erase Type 4 is not defined<br>Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is 256 KB erase and is not supported in the 4 KB sector region<br>Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is 64 KB erase and is not supported<br>Bit 0 = Erase Type 1 support = 1b ---Erase Type 1 is 4 KB erase and is supported in the 4 KB sector region |
| 209h | | FFh | |
| 20Ah | | 01h | |
| 20Bh | | 00h | |

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**表 93　　JEDEC SFDP Rev D，扇区映射参数（续）**

| SFDP byte address | SFDP DWORD name | Data | Description |
|---|---|---|---|
| 20Ch | JEDEC Sector Map Parameter DWORD-9 Config-0 Region-1 | F8h | Region 1 of 128 KB sector<br>Bits 31:8 = Region size = 0001FFh: Region size as count - 1 of 256 Byte units = 1 x 128 KB sectors<br>= 128 KB Count = 128 KB/256 = 512, value = count – 1 = 512 – 1 = 511 = 1FFh<br>Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1<br>Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 128 KB sector region<br>Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined<br>Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined<br>Bit 0 = Erase Type 1 support = 0b --- Erase Type 1 is 4KB erase and is not supported in the 4 KB sector region |
| 20Dh | | FFh | |
| 20Eh | | 01h | |
| 20Fh | | 00h | |
| 210h | JEDEC Sector Map Parameter DWORD-10 Config-0 Region-2 | F8h | Region 2 Uniform 256 KB sectors<br>Bits 31:8 = 512 Mb device Region size = 03FBFFh:<br>Region size as count-1 of 256 Byte units = 255 x 256 KB sectors = 65,280 KB Count = 65,280 KB/256 = 261,120 value = count – 1 = 261,120 – 1 = 261119 = 3FBFFh<br>Bits 31:8 = 1 Gb device Region size = 01FEFFh: Region size as count – 1 of 256 Byte units = 511 x 256 KB sectors = 130,816 KB Count =<br>130,816 KB/256 = 523,364, value = count – 1 = 523,364 – 1 = 523263 = 07FBFFh<br>Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1<br>Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 256 KB sector region<br>Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined<br>Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined<br>Bit 0 = Erase Type 1 support = 0b --- Erase Type 1 is 4 KB erase and is not supported in the 256 KB sector region |
| 211h | | FFh | |
| 212h | | FBh | |
| 213h | | 03h (512 Mb)<br>07h (1 Gb) | |
| 214h | JEDEC Sector Map Parameter DWORD-11 Config-3 Header | FEh | Configuration Index 01h 4 KB sectors at Top with remainder 256 KB<br>Bits 31:24 = RFU = FFh<br>Bits 23:16 = Region count (DWORDs -1) = 02h: Three regions<br>Bits 15:8 = Configuration ID = 01h: 4KB sectors at top with remainder 256 KB sectors<br>Bits 7:2 = RFU = 111111b<br>Bit 1 = Map Descriptor = 1<br>Bit 0 = Not the end descriptor = 0 |
| 215h | | 01h | |
| 216h | | 02h | |
| 217h | | FFh | |

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**表 93　　JEDEC SFDP Rev D，扇区映射参数（续）**

| SFDP byte address | SFDP DWORD name | Data | Description |
|---|---|---|---|
| 218h | JEDEC Sector Map Parameter DWORD-12 Config-3 Region-0 | F8h | Region 0 Uniform 256KB sectors<br>Bits 31:8 = 512 Mb device Region size = 03FBFFh:<br>Region size as count – 1 of 256 Byte units = 255 x 256 KB sectors = 65,280 KB Count = 65,280 KB/256 = 261,120 value = count – 1 = 261,120 – 1= 261119 =3FBFFh<br>Bits 31:8 = 1 Gb device Region size = 07FBFFh: Region size as count – 1 of 256 Byte units = 511 x 256 KB sectors = 130,816 KB Count =<br>130,816 KB/256 = 523,264, value = count – 1 = 523,364 – 1 = 523263 = 07FBFFh<br>Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1<br>Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 256 KB sector region<br>Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined<br>Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined<br>Bit 0 = Erase Type 1 support = 0b ---Erase Type 1 is 4 KB erase and is not supported in the 256 KB sector region |
| 219h | | FFh | |
| 21Ah | | FBh | |
| 21Bh | | 03h (512 Mb)<br>07h (1 Gb) | |
| 21Ch | JEDEC Sector Map Parameter DWORD-13 Config-3 Region-1 | F8h | Region 1 of 128 KB sector<br>Bits 31:8 = Region size = 0001FFh: Region size as count – 1 of 256 Byte units = 1 x 128 KB sectors =<br>128 KB Count = 128 KB/256 = 512, value = count – 1 = 512 – 1 = 511 = 1FFh<br>Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1<br>Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 128 KB sector region<br>Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined<br>Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined<br>Bit 0 = Erase Type 1 support = 0b ---Erase Type 1 is 4 KB erase and is not supported in the 4 KB sector region |
| 21Dh | | FFh | |
| 21Eh | | 01h | |
| 21Fh | | 00h | |
| 220h | JEDEC Sector Map Parameter DWORD-14 Config-3 Region-2 | F1h | Region 2 of 4 KB sectors<br>Bits 31:8 = Region size (32 4 KB) = 0001FFh: Region size as count – 1 of 256 Byte units = 32 x 4 KB sectors = 128 KB Count = 128 KB/256 = 512, value = count – 1 = 512 – 1 = 511 = 1FFh<br>Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1<br>Bit 3 = Erase Type 4 support = 0b ---Erase Type 4 is not defined<br>Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is 256 KB erase and is not supported in the 4 KB sector region<br>Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is 64 KB erase and is not supported<br>Bit 0 = Erase Type 1 support = 1b ---Erase Type 1 is 4 KB erase and is supported in the 4 KB sector region |
| 221h | | FFh | |
| 222h | | 01h | |
| 223h | | 00h | |
| 224h | JEDEC Sector Map Parameter DWORD-15 Config-1 Header | FEh | Configuration Index 02h 4 KB sectors split between Bottom and Top with remainder 256 KB<br>Bits 31:24 = RFU = FFh<br>Bits 23:16 = Region count (DWORDs – 1) = 04h: Five regions Bits 15:8 = Configuration ID = 02h: 4 KB sectors split between bottom and top with remainder 256 KB sectors<br>Bits 7:2 = RFU = 111111b<br>Bit 1 = Map Descriptor = 1<br>Bit 0 = Not the end descriptor = 0 |
| 225h | | 02h | |
| 226h | | 04h | |
| 227h | | FFh | |

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**表 93　　JEDEC SFDP Rev D，扇区映射参数（续）**

| SFDP byte address | SFDP DWORD name | Data | Description |
|---|---|---|---|
| 228h | JEDEC Sector Map Parameter DWORD-16 Config-1 Region-0 | F1h | Region 0 of 4 KB sectors<br>Bits 31:8 = Region size (16 x 4 KB) = 0000FFh: Region size as count – 1 of 256 Byte units = 16 x 4 KB sectors = 64 KB Count = 64 KB/256<br>= 256, value = count – 1 = 256 – 1 = 255 = FFh<br>Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1<br>Bit 3 = Erase Type 4 support = 0b ---Erase Type 4 is not defined<br>Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is 256 KB erase and is not supported in the 4 KB sector region<br>Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is 64 KB erase and is not supported<br>Bit 0 = Erase Type 1 support = 1b ---Erase Type 1 is 4 KB erase and is supported in the 4 KB sector region |
| 229h | | FFh | |
| 22Ah | | 00h | |
| 22Bh | | 00h | |
| 22Ch | JEDEC Sector Map Parameter DWORD-17 Config-1 Region-1 | F8h | Region 1 of 192 KB sector<br>Bits 31:8 = Region size = 0002FFh: Region size as count – 1 of 256 Byte units = 1 x 192KB sectors = 192KB Count = 192KB/256 = 768, value = count -1 = 768 – 1 = 767 = 2FFh<br>Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1<br>Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 192 KB sector region<br>Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined<br>Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined<br>Bit 0 = Erase Type 1 support = 0b --- Erase Type 1 is 4 KB erase and is not supported in the 4 KB sector region |
| 22Dh | | FFh | |
| 22Eh | | 02h | |
| 22Fh | | 00h | |
| 230h | JEDEC Sector Map Parameter DWORD-18 Config-1 Region-2 | F8h | Region 2 Uniform 256 KB sectors<br>Bits 31:8 = 512 Mb device Region size = 03F7FF:<br>Region size as count – 1 of 256 Byte units = 254 x 256 KB sectors = 65,024 KB Count = 65,024 KB/256 = 260,096 value = count – 1 = 260,096 – 1 = 260,095 = 3F7FFh<br>Bits 31:8 = 1 Gb device Region size = 07F7FFh: Region size as count – 1 of 256 Byte units = 510 x 256 KB sectors = 130,560 KB Count =<br>130,560 KB/256 = 522,240, value = count – 1 = 522,240 – 1 = 522,239 = 7F7FFh<br>Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1<br>Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 256 KB sector region<br>Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined<br>Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined<br>Bit 0 = Erase Type 1 support = 0b ---Erase Type 1 is 4 KB erase and is not supported in the 256 KB sector region |
| 231h | | FFh | |
| 232h | | F7h | |
| 233h | | 03h (512 Mb)<br>07h (1 Gb) | |
| 234h | JEDEC Sector Map Parameter DWORD-19 Config-1 Region-3 | F8h | Region 3 of 192 KB sector<br>Bits 31:8 = Region size = 0002FFh: Region size as count – 1 of 256 Byte units = 1 x 192 KB sectors = 192 KB Count = 192 KB/256 = 768, value = count -1 = 768 – 1 = 767 = 2FFh<br>Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1<br>Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 192 KB sector region<br>Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined<br>Bit 1 = Erase Type 2 support = 0b ---Erase Type 22 is not defined<br>Bit 0 = Erase Type 1 support = 0b ---Erase Type 1 is 4KB erase and is not supported in the 4 KB sector region |
| 235h | | FFh | |
| 236h | | 02h | |
| 237h | | 00h | |

**表 93　　JEDEC SFDP Rev D，扇区映射参数（续）**

| SFDP byte address | SFDP DWORD name | Data | Description |
|---|---|---|---|
| 238h | JEDEC Sector Map Parameter DWORD-20 Config-1 Region-5 | F1h | Region 5 of 4KB sectors<br>Bits 31:8 = Region size (16 x 4 KB) = 0000FFh: Region size as count – 1 of 256 Byte units = 16 x 4 KB sectors = 64 KB Count = 64 KB/256<br>= 256, value = count – 1 = 256 – 1 = 255 = FFh<br>Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1<br>Bit 3 = Erase Type 4 support = 0b ---Erase Type 4 is not defined<br>Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is 256 KB erase and is not supported in the 4 KB sector region<br>Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is 64 KB erase and is not supported<br>Bit 0 = Erase Type 1 support = 1b ---Erase Type 1 is 4 KB erase and is supported in the 4 KB sector region |
| 239h | | FFh | |
| 23Ah | | 00h | |
| 23Bh | | 00h | |
| 23Ch | JEDEC Sector Map Parameter DWORD-21 Config-4 Header | FFh | Configuration Index 04h Uniform 256 KB sectors Bits 31:24 = RFU = FFh<br>Bits 23:16 = Region count (DWORDs – 1) = 00h: One region Bits 15:8 = Configuration ID = 04h: Uniform 256KB sectors Bits 7:2 = RFU = 111111b<br>Bit 1 = Map Descriptor = 1<br>Bit 1= End of map descriptor = 1 |
| 23Dh | | 04h | |
| 23Eh | | 00h | |
| 23Fh | | FFh | |
| 240h | JEDEC Sector Map Parameter DWORD-22 Config-4 Region-0 | F8h | Region 0 Uniform 256 KB sectors<br>Bits 31:8 = 512 Mb device Region size = 03FFFFh:<br>Region size as count – 1 of 256 Byte units = 256 x 256 KB sectors = 65,536 KB Count = 65,280 KB/256 = 262,144 value = count – 1 = 262,144 – 1 = 262,143 = 3FFFFh<br>Bits 31:8 = 1 Gb device Region size = 07FFFFh: Region size as count – 1 of 256 Byte units = 512 x 256 KB sectors = 131,072 KB Count =<br>131,072 KB/256 = 524,288, value = count – 1 = 524,288 – 1 = 524,287 = 7FFFFh<br>Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1<br>Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 256 KB sector region<br>Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined<br>Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined<br>Bit 0 = Erase Type 1 support = 0b ---Erase Type 1 is 4 KB erase and is not supported in the 256 KB sector region |
| 241h | | FFh | |
| 242h | | FFh | |
| 243h | | 03h (512 Mb)<br>07h (1 Gb) | |

## 9.2 制造商和器件 ID

**表 94 制造商和器件ID**

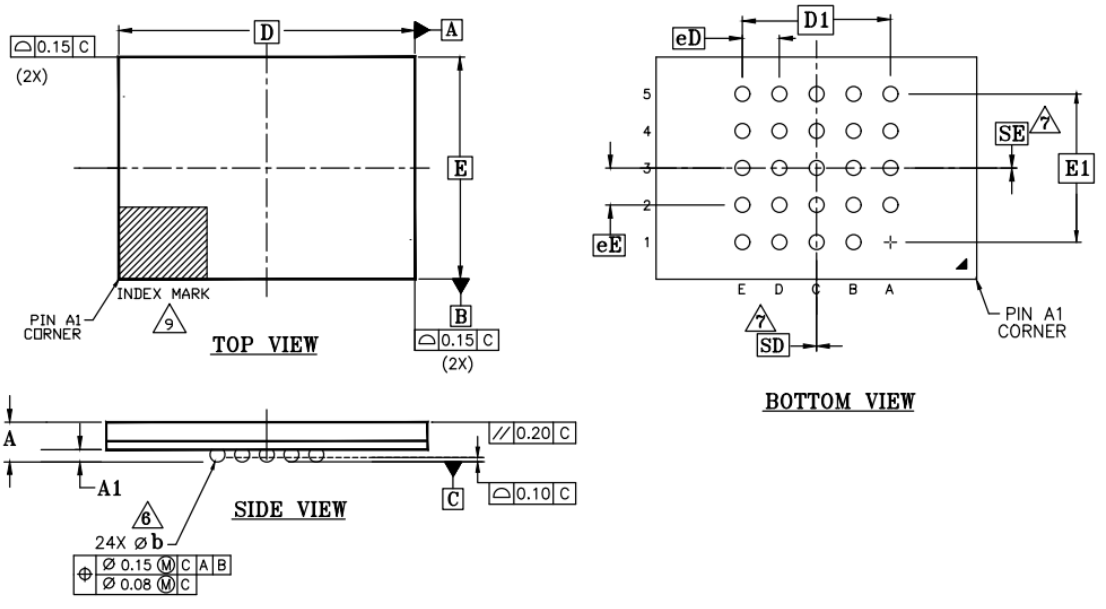
| Byte address | Data | Description |
|---|---|---|
| 00h | 34h | Manufacturer ID for Infineon |
| 01h | 5Ah (HL-T) /<br>5Bh (HS-T) | Device ID MSB - Memory Interface Type |
| 02h | 1Ah (512Mb) /<br>1Bh (1Gb) | Device ID LSB - Density |
| 03h | 0Fh | ID Length - number bytes following. Adding this value to the current location of 03h gives the address of the last valid location in the ID legacy address map. |
| 04h | 03h<br>(Default Configuration) | Physical Sector Architecture<br>The HS/L-T family may be configured with or without 4 KB parameter sectors in addition to the uniform sectors.<br>03h = Uniform 256 KB with thirty-two 4 KB Parameter Sectors) |
| 05h | 90h<br>(HL-T/HS-T Family) | Family IDs |

## 9.3 唯一器件 ID

**表 95 唯一器件 ID**

| Byte address | Data | Description |
|---|---|---|
| 00h to 07h | 8-Byte Unique Device ID | 64-bit unique ID number |

# 10 封装图




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | - | - | 1.00 |
| A1 | 0.20 | - | - |
| D | 8.00 BSC | | |
| E | 6.00 BSC | | |
| D1 | 4.00 BSC | | |
| E1 | 4.00 BSC | | |
| MD | 5 | | |
| ME | 5 | | |
| N | 24 | | |
| Ø b | 0.35 | 0.40 | 0.45 |
| eE | 1.00 BSC | | |
| eD | 1.00 BSC | | |
| SD | 0.00 BSC | | |
| SE | 0.00 BSC | | |

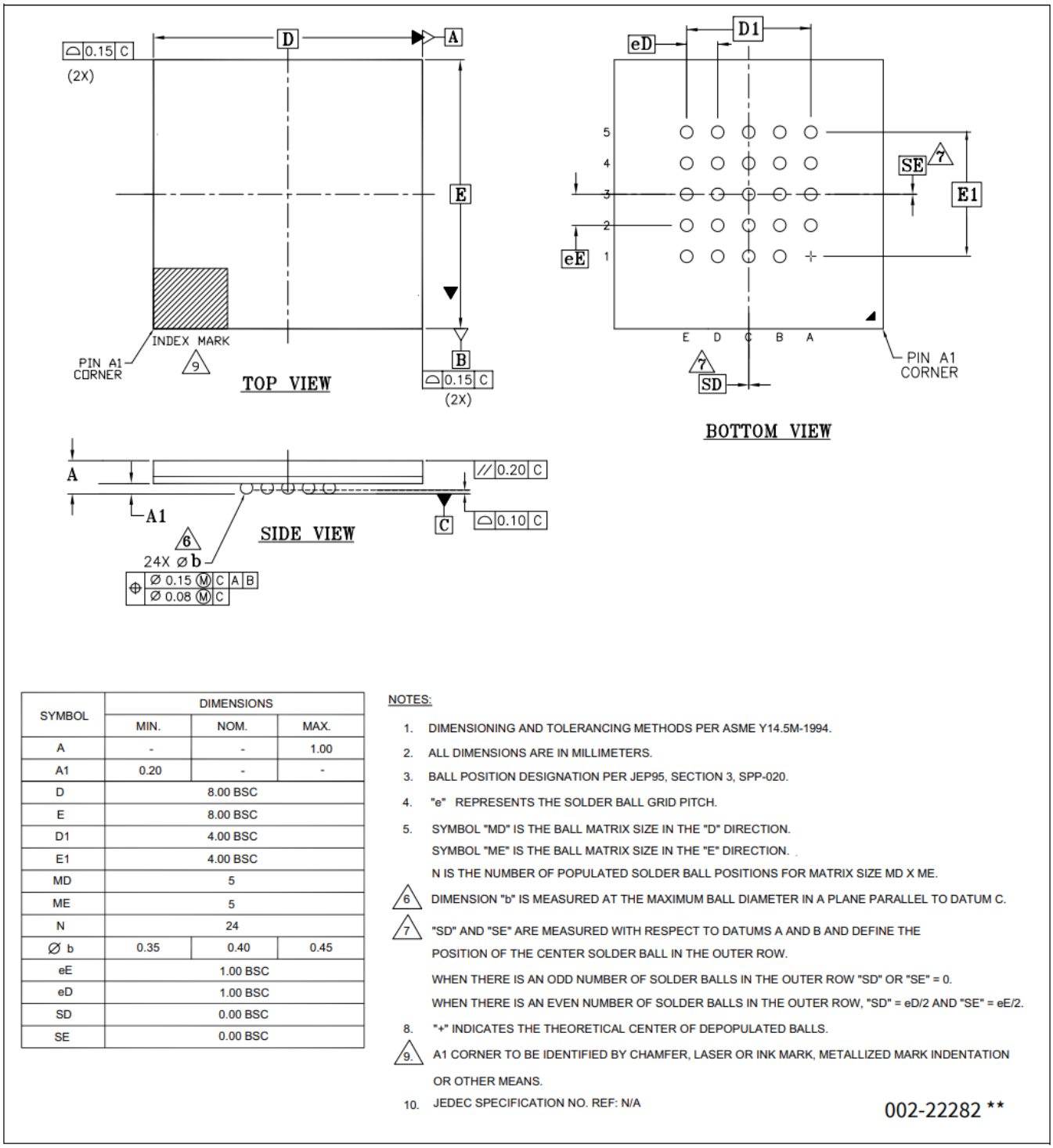
NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. JEDEC SPECIFICATION NO. REF: MO-234E

002-15550 *B

**图 79 24 球 BGA（8 × 6 × 1 毫米）VAA024/ELA024/E2A024 封装外形（PG-BGA-24），002-15550**

封装图




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | - | - | 1.00 |
| A1 | 0.20 | - | - |
| D | 8.00 BSC | | |
| E | 8.00 BSC | | |
| D1 | 4.00 BSC | | |
| E1 | 4.00 BSC | | |
| MD | 5 | | |
| ME | 5 | | |
| N | 24 | | |
| ∅ b | 0.35 | 0.40 | 0.45 |
| eE | 1.00 BSC | | |
| eD | 1.00 BSC | | |
| SD | 0.00 BSC | | |
| SE | 0.00 BSC | | |

NOTES:

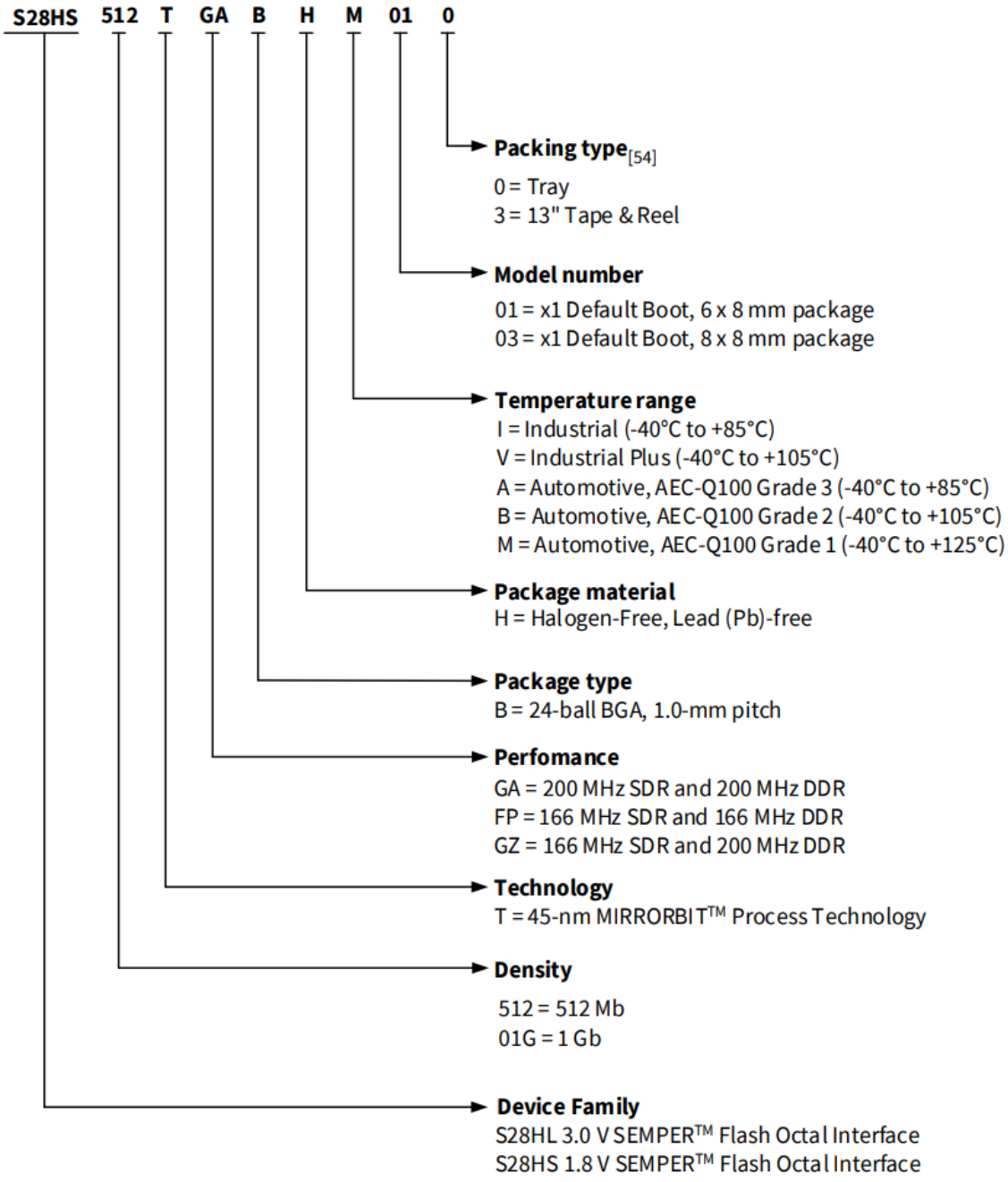
1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. JEDEC SPECIFICATION NO. REF: N/A

002-22282 **

**图 80　　24 球BGA (8 × 8 × 1 mm) VAC024 封装封装外形 (PG- BGA -24)，002-22282**

# 11 订购信息

订购部件编号由以下有效组合形成：




**注释**

54. 请参阅 **www.infineon.cn** 上的包装和封装手册以了解更多信息。

订购信息

## 11.1 有效组合 — 标准等级

表 96 列出计划批量支持的此器件的配置。接点，触点，联系您当地的销售办事处，以确认特定有效组合的可用性并检查新发布的组合。

**表96 有效组合 — 标准等级**

| Base ordering part number | Speed option | Package and materials | Temperature range | Model number | Packing type | Ordering part number (x = Packing type) | Package marking |
|---|---|---|---|---|---|---|---|
| S28HL512T | FP | BH | I, V | 01 | 0, 3 | S28HL512TFPBHI01x | 28HL512TPI01 |
| | | | | | | S28HL512TFPBHV01x | 28HL512TPV01 |
| S28HS512T | GA | | | | | S28HS512TGABHI01x | 28HS512TAI01 |
| | | | | | | S28HS512TGABHV01x | 28HS512TAV01 |
| S28HL01GT | FP | | | 03 | | S28HL01GTFPBHI03x | 28HL01GTPI03 |
| | | | | | | S28HL01GTFPBHV03x | 28HL01GTPV03 |
| S28HS01GT | FP | | | | | S28HS01GTFPBHI03x | 28HS01GTPI03 |
| | | | | | | S28HS01GTFPBHV03x | 28HS01GTPV03 |
| S28HS01GT | GZ | | | | | S28HS01GTGZBHI03x | 28HS01GTZI03 |
| | | | | | | S28HS01GTGZBHV03x | 28HS01GTZV03 |

## 11.2 有效组合 – 汽车级/AEC-Q100

表 97 列出了符合汽车级/AEC-Q100 认证并计划批量供货的配置。该表将随着新组合的发布而更新。如要确认特定组合的可用性并了解最新推出的组合，请咨询您当地的销售代表。

仅为 AEC-Q100 级产品提供生产部件批准程序（PPAP）支持。

用于需要符合 ISO/TS-16949 标准的端到端应用的产品必须是与 PPAP 结合使用的 AEC-Q100 级产品。非 AEC-Q100 级产品的制造或记录不完全符合 ISO/TS-16949 的要求。对于不需要符合 ISO/TS-16949 标准的端到端应用，我们还提供不含 PPAP 支持的 AEC-Q100 级产品。

**表 97 有效组合 – 汽车级/AEC-Q100**

| Base ordering part number | Speed option | Package and materials | Temperature range | Model number | Packing type | Ordering part number (x = Packing type) | Package marking |
|---|---|---|---|---|---|---|---|
| S28HL512T | FP | BH | A, B, M | 01 | 0, 3 | S28HL512TFPBHA01x | 28HL512TPA01 |
| | | | | | | S28HL512TFPBHB01x | 28HL512TPB01 |
| | | | | | | S28HL512TFPBHM01x | 28HL512TPM01 |
| S28HS512T | GA | | | | | S28HS512TGABHA01x | 28HS512TAA01 |
| | | | | | | S28HS512TGABHB01x | 28HS512TAB01 |
| | | | | | | S28HS512TGABHM01x | 28HS512TAM01 |
| S28HL01GT | FP | | | 03 | | S28HL01GTFPBHA03x | 28HL01GTPA03 |
| | | | | | | S28HL01GTFPBHB03x | 28HL01GTPB03 |
| | | | | | | S28HL01GTFPBHM03x | 28HL01GTPM03 |
| S28HS01GT | FP | | | | | S28HS01GTFPBHA03x | 28HS01GTPA03 |
| | | | | | | S28HS01GTFPBHB03x | 28HS01GTPB03 |
| | | | | | | S28HS01GTFPBHM03x | 28HS01GTPM03 |
| S28HS01GT | GZ | | | | | S28HS01GTGZBHA03x | 28HS01GTZA03 |
| | | | | | | S28HS01GTGZBHB03x | 28HS01GTZB03 |
| | | | | | | S28HS01GTGZBHM03x | 28HS01GTZM03 |

# 修订记录

| Document revision | Date | Description of changes |
|---|---|---|
| *X | 2022-04-08 | Publish to web. |
| *Y | 2022-11-10 | Updated **“Valid combinations — automotive grade / AEC-Q100”** on page 178 and **“Valid combinations — automotive grade / AEC-Q100”** on page 178. |
| *Z | 2023-08-09 | Updated **Table 91**, **Table 93**.<br>Updated **Figure 79**. |
| AA | 2024-03-25 | Updated “Data integrity” under **Features**.<br>Updated “SPI (1S-1S-8S, 1S-8S-8S 256T only)” under **Features**.<br>Updated “Program / erase (PE) endurance - high endurance (256KB sectors)” under **Data integrity**.<br>Updated **Table 57**, **Table 81**, **Table 76**, **Table 87**, **Table 89**, **Table 91**, and **Table 93**. |
| AB | 2024-05-13 | Removed Device S28HL256T & S28HS256T. Devices move to separate datasheet. Removed the typo that present in the description of changes in Rev. AA revision history. |
| AC | 2024-10-09 | Updated the parameter for $t_{DIS}$ and unit of $t_{BE}$ in **Table 89**.<br>Updated **Table 84**. |
| AD | 2025-06-30 | Updated parameter and minimum value for $t_{SU}$ and $t_{HD}$ in **Table 89**. |

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