

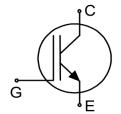
EDT3 IGBT for Automotive Applications

IGBT

Quality Requirement Category: Automotive

Features

- 750V trench + field stop technology
- Low V_{CE(sat)}
- Low switching losses
- Short tail current
- Positive temperature coefficient
- Integrated gate resistor
- Easy paralleling
- 185°C maximum junction temperature



Applications

• Drives

Description

• Recommended for power modules

Product Validation

• Technology qualified for Automotive Applications. Product validation according to AEC-Q101.

Key Performance Parameters

Chip Type	V _{CE}	I _{Cn}	Die Size	Package
IGC100T75H12RYA	750V	320A	99.93mm²	Sawn on foil

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1 Parameters and Characteristics

Table 1 Mechanical Parameters

Raster size		9.27 x 10.78	mm²			
Area total		99.93	mm²			
Emitter pad size		See chip drawing				
Gate pad size		See chip drawing				
Silicon thickness		77	μm			
Wafer size		300	mm			
Maximum possible chips per wafer		612				
Passivation frontside		Photoimide				
Pad metal		AlCu				
Backside metal		Ni Ag system				
Die bond¹		Soft solder				
Frontside interconnect ¹		Wire bond: Al, ≤ 500 μm				
Reject ink dot size		Inkless				
Storage environment (<6 months) For original and sealed MBB bags²		Ambient atmosphere air, temperature 17°C – 25°C				

¹ Depending on customer specific assembly process

² https://www.infineon.com/dgdl/Storage of Products Supplied by Infineon Technologie.pdf?fileId=5546d461641369bf01643b95d8500011

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v1.00

Maximum Ratings¹ Table 2

Parameter	Symbol	Conditions	Value	Unit	
Callactor emittervaltage	17	25°C ≤ <i>T_{vj}</i> ≤ 185°C	750	V	
Collector-emitter voltage	V_{CES}	$T_{vj} = -40^{\circ}C^{2}$	710		
DC collector current, limited by T_{vjmax}	Ic		_3	Α	
Pulsed collector current, t_p limited by $T_{vj max}$	I _{C,pulse}		960	Α	
Gate-emitter voltage	V_{GE}		±20	V	
Virtual junction temperature	$T_{\nu j}$		-40 +185	°C	
		$V_{GE} \le 15 \text{V}, V_{CC} \le 470 \text{V}, T_{vj}$ \$\leq 175°C	3		
Short circuit withstand time 4/5	t_{sc}	$V_{GE} \le 15$ V, $V_{CC} \le 470$ V, T_{vj} ≤ 185 °C	2.5	μs	
Reverse bias safe operating area	RBSOA	$I_{C,max}$ = 640A, $V_{CE,max}$ = V_{CES} , -40°C $\leq T_{vj} \leq 185$ °C			

Static Characteristics (Tested on Wafer), T_{vj} =25°C Table 3

Davamatav	Cymahal	Canditions	Value			Unit
Parameter	Symbol	Conditions	min.	typ.	max.	Oilit
Collector-emitter saturation voltage	V _{CEsat}	$V_{GE} = 15V, I_C = 64A$	-	0.94	1.03	V
Gate-emitter threshold voltage	$V_{GE(th)}$	$I_C = 3.2 \text{mA}$, $V_{GE} = V_{CE}$	5.2	5.9	6.5	V
Zero gate voltage collector current	I _{CES}	$V_{CE} = 750 \text{V}, V_{GE} = 0 \text{V}$	-	-	100	μΑ
Gate-emitter leakage current	I _{GES}	$V_{CE} = 0V, V_{GE} = 20V$	-	-	600	nA
Integrated gate resistor	r_{G}		-	2	-	Ω

 $^{^{1}\,\}mbox{Not}$ subject to production test - verified by design/characterization.

² V_{CES} increases linearly between -40°C and 25°C.

³ Depending on thermal properties of assembly.

⁴ Allowed number of short circuits: <1000; time between short circuits: >1s.

⁵ Depending on electrical design of assembly.

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Table 4 Electrical Characteristics¹

Parameter	Complete	Conditions		Value			11
Parameter	Symbol			min.	typ.	max.	Unit
	$V_{\it CEsat}$	V_{GE} = 15V,	<i>T_{vj}</i> = 25°C	-	1.15	1.28	V
Collector emitter caturation voltage		$I_{C} = 200A$	<i>T_{vj}</i> = 185°C	-	1.2	-	
Collector-emitter saturation voltage		V_{GE} = 15V,	<i>T_{vj}</i> = 25°C	-	1.29	1.44	V
_		$I_{C} = 320A$	<i>T_{vj}</i> = 185°C	-	1.43	-	
Input capacitance	C _{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 100kHz T_{vj} = 25°C			18600		pF
Output capacitance	Coes				670		
Reverse transfer capacitance	C _{res}				120		
Gate charge	Q _G	$V_{CE} = 470V$ $V_{GE} = -8V$		-	820	-	nC

2 Further Electrical Characteristics

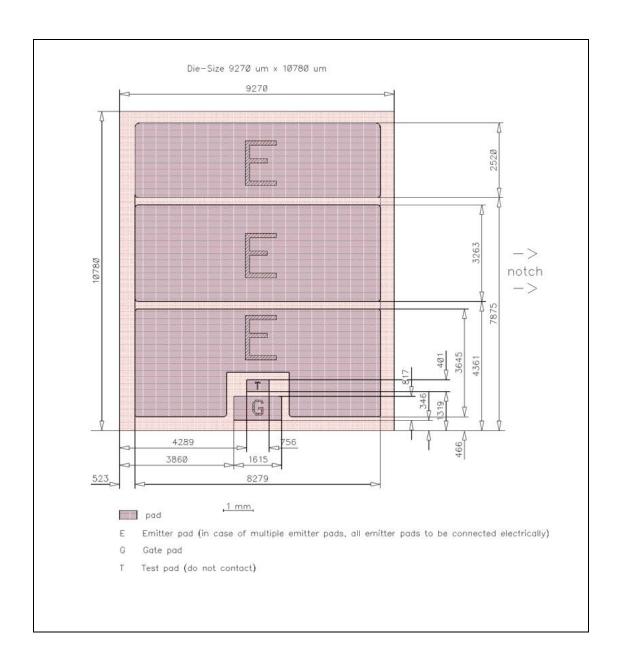
Note:

Switching characteristics and thermal properties are dependent on module design and mounting technology and can therefore not be specified for a bare die.

 $^{^{\}rm 1}$ Not subject to production test - verified by design/characterization. Datasheet



3 Chip Drawing



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Bare Die Product Specifics 4

Note:

Test coverage at wafer level for IGBTs cannot cover the full range of customer application conditions. Therefore it is the responsibility of the customer to test all performance characteristics, which are relevant for their specific application, at the package level, including RBSOA and SCSOA.

Description

• AQL 0.1 for visual inspection according to failure catalogue

Revision History

Document version	Date of release	Description of changes
V1.00	2025-March-06	Initial datasheet

Trademarks

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