

CoolGaN™
CoolGaN™ Automotive Transistor 100V G1

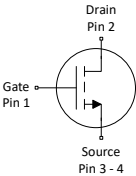
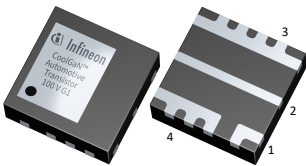
PG-TSON-4

Features

- Industrial grade products qualified according to AEC-Q101
- Ultra fast switching and high efficiency
- Space saving and highly robust package
- No reverse recovery charge
- Ultra low gate charge and output charge
- Exposed die for top-side thermal excellence
- Moisture rating MSL1
- Industrial grade 3x3 package

Potential applications

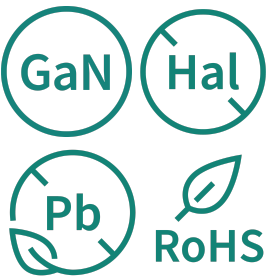
- Automotive DC/DC
- Drives
- Class D Audio
- USB-PD



Top side is exposed silicon substrate,
internally connected to source terminal.
Not recommended to use as an electrical
connection.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max@25^{\circ}C}$	11	mΩ
I_D	23	A
Q_{oss}	14	nC
Q_G	3.4	nC
Q_{rr}	0	nC



Type / Ordering code	Package	Marking	Related links
IGB110S10S1Q	PG-TSON-4	B1Q	see Appendix A

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1 Maximum ratings

at $T_j = 25\text{ °C}$, unless otherwise specified. Stresses beyond max ratings may cause permanent damage to the device. For optimum lifetime and reliability, Infineon recommends operating conditions that do not continuously exceed 80 % of the maximum ratings stated (unless otherwise explicitly stated). For further information, contact your local Infineon sales office.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain-source voltage	V_{DS}	-	-	100	V	$V_{GS}=0\text{ V}$
Pulsed drain-source voltage ¹⁾	$V_{DS, pulse}$	-	-	120	V	$V_{GS}=0\text{ V}$, 1 h total time
Continuous drain current	I_D	-	-	23 9.0	A	$V_{GS}=5\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=5\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=50\text{ °C/W}$ ²⁾
Pulsed drain current ³⁾	$I_{D, pulse}$	-	-	210 97	A	$T_j=25\text{ °C}$ $T_j=150\text{ °C}$
Pulsed gate-source voltage ¹⁾	V_{GS}	-6.5	-	6.5	V	Pulsed 100 h total time
Power dissipation	P_{tot}	-	-	15 2.5	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=50\text{ °C/W}$ ²⁾
Storage temperature	T_{stg}	-55	-	150	°C	-
Junction temperature	T_j	-40	-	150	°C	

¹⁾ Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation.

²⁾ Device on 4-layer FR4 PCB, vertical in still air.

³⁾ Pulse current limited by transfer characteristic.

2 Recommended operating conditions

Table 3 Recommended operating conditions

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate-source voltage	V_{GS}	-4.0	5.0	5.5	V	-

3 Thermal characteristics

Table 4 Thermal characteristics 4)

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, top	R_{thJC}	-	1.4	1.7	°C/W	-
Thermal resistance, junction - case, bottom	R_{thJC}	-	5.6	8.1	°C/W	
Thermal resistance, junction - ambient 1s0p	R_{thJA}	-	70	-	°C/W	On 1 layer PCB, vertical in still air.
Thermal resistance, junction - ambient 2s2p	R_{thJA}	-	50	-	°C/W	With vias on 4 layer PCB, vertical in still air.

4) Defined by design. Not subject to production test.

4 Electrical Characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	1.2	2.0	2.9	V	$V_{DS}=V_{GS}$, $I_D=3.0\text{ mA}$
Drain-source leakage current	I_{DSS}	-	0.1 2.0	0.5 20	μA	$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	5.0 0.003 40 0.003	50 0.009 370 0.012	μA	$V_{GS}=5\text{ V}$, $T_j=25\text{ °C}$ $V_{GS}=-4\text{ V}$, $T_j=25\text{ °C}$ $V_{GS}=5\text{ V}$, $T_j=125\text{ °C}$ $V_{GS}=-4\text{ V}$, $T_j=125\text{ °C}$
Drain-source on-state resistance	$R_{DS(on)}$	-	9.4	11	$\text{m}\Omega$	$V_{GS}=5\text{ V}$, $I_D=10\text{ A}$
Gate resistance ⁵⁾	R_G	-	0.5	-	Ω	-

⁵⁾ Defined by design. Not subject to production test.

Table 6 Capacitance characteristics ⁶⁾

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	300	340	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	-	140	150	pF	
Reverse transfer capacitance	C_{rss}	-	2.3	3.0	pF	

⁶⁾ Defined by design. Not subject to production test.

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	1.0	-	nC	$V_{DS}=50\text{ V}$, $I_D=10\text{ A}$, $V_{GS}=0\text{ to }5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	0.7	-	nC	
Gate to drain charge ⁷⁾	Q_{gd}	-	0.9	-	nC	
Switching charge	Q_{sw}	-	1.2	-	nC	
Gate charge total ⁷⁾	Q_g	-	3.4	4.4	nC	
Gate plateau voltage	$V_{plateau}$	-	2.8	-	V	
Output charge ⁷⁾	Q_{oss}	-	14	15	nC	$V_{DS}=50\text{ V}$, $V_{GS}=0\text{ V}$

⁷⁾ Defined by design. Not subject to production test.

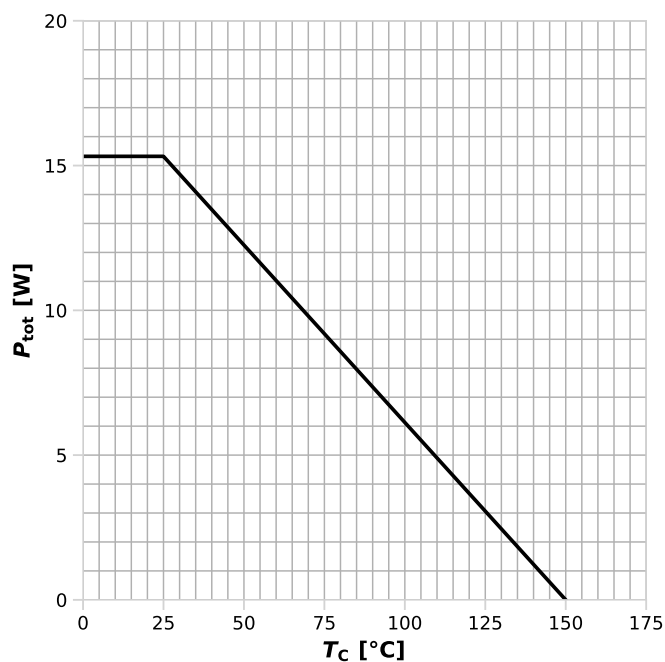
Table 8 Reverse operation

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Reverse continuous current	I_S	-	-	5.0	A	$T_C = 25\text{ °C}$
Pulsed current, reverse	$I_{S,pulse}$	-	-	92	A	
Source-Drain reverse voltage	V_{SD}	-	2.6 2.2	3.4 -	V	$V_{GS}=0\text{ V}, I_{S,pulse}=10\text{ A}, T_j=25\text{ °C}$ $V_{GS}=0\text{ V}, I_{S,pulse}=0.5\text{ A}, T_j=25\text{ °C}$
Reverse recovery charge ⁸⁾	Q_{rr}	-	0	-	nC	$V_R=50\text{ V}, I_{S,pulse}=10\text{ A}, di_{S,pulse}/dt=100\text{ A}/\mu\text{s}$

⁸⁾ Defined by design. Not subject to production test.

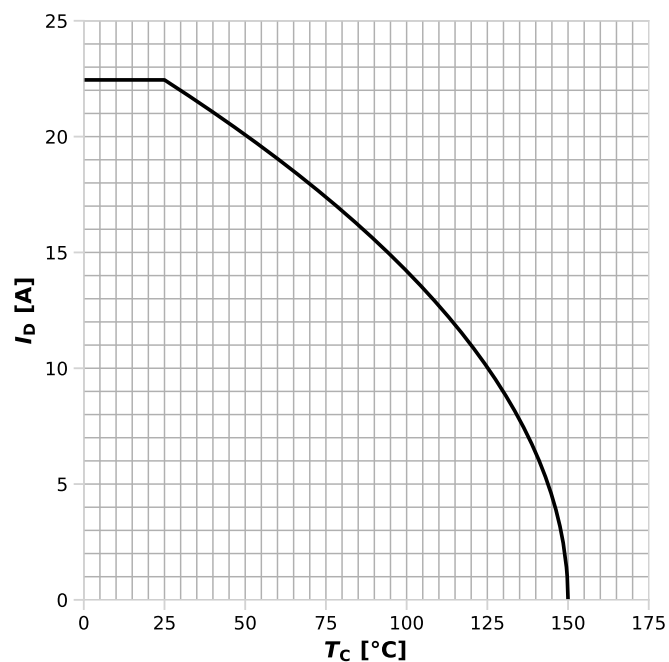
5 Electrical characteristics diagrams

Diagram 1: Power dissipation



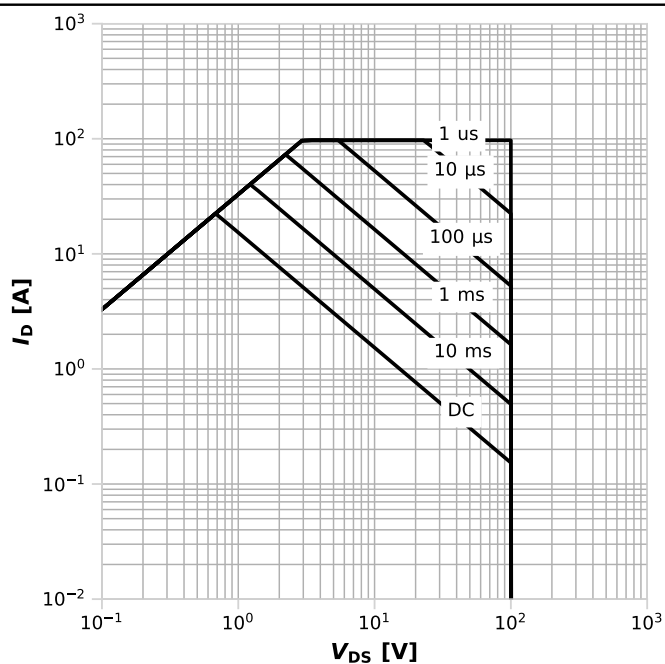
$$P_{tot}=f(T_c)$$

Diagram 2: Drain Current



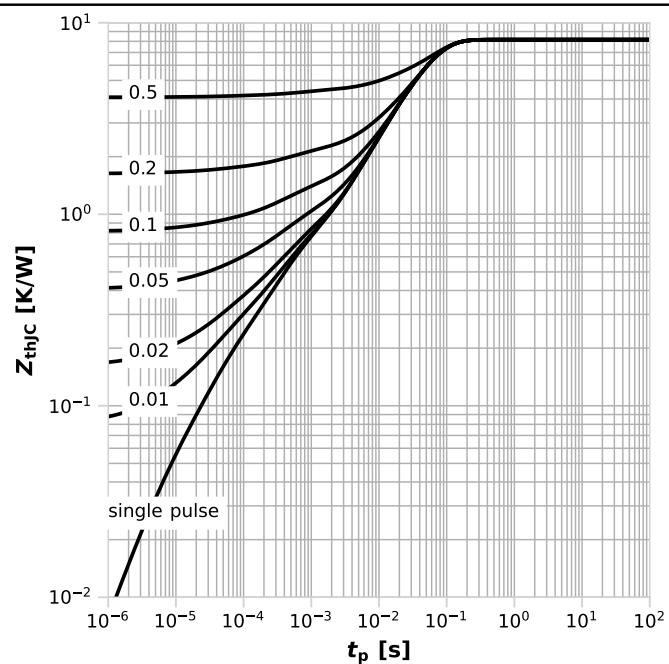
$$I_D=f(T_c)$$

Diagram 3: Safe operating area



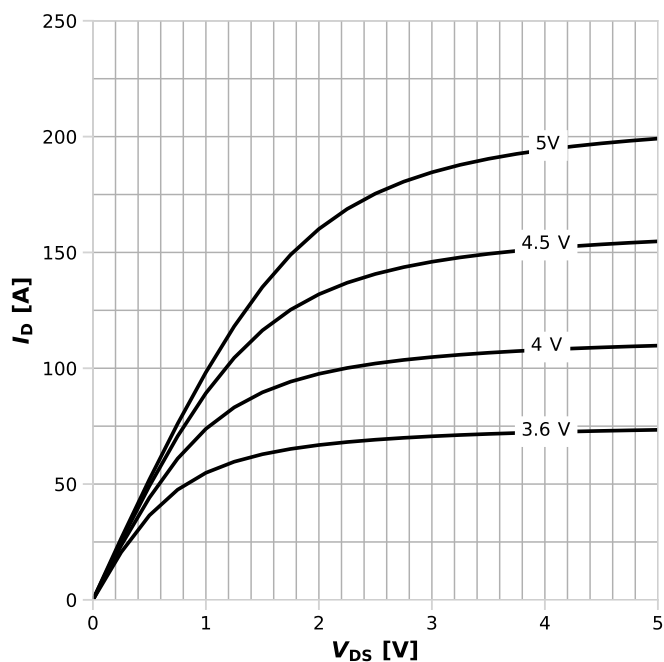
$$I_D=f(V_{DS}); T_c=25\text{ °C}; D=0; \text{parameter: } t_p$$

Diagram 4: Max. transient thermal impedance



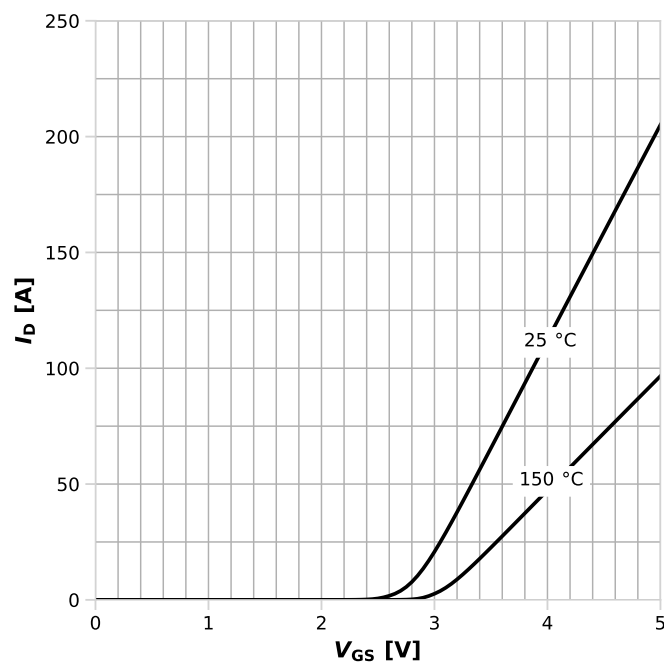
$$Z_{thJC}=f(t_p); \text{parameter: } D=t_p/T$$

Diagram 5: Typ. output characteristics



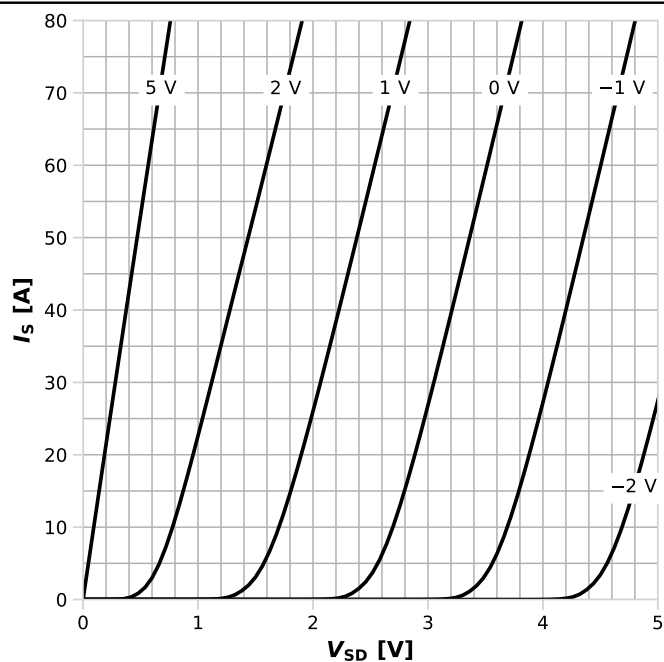
$I_D = f(V_{DS})$; $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. transfer characteristics



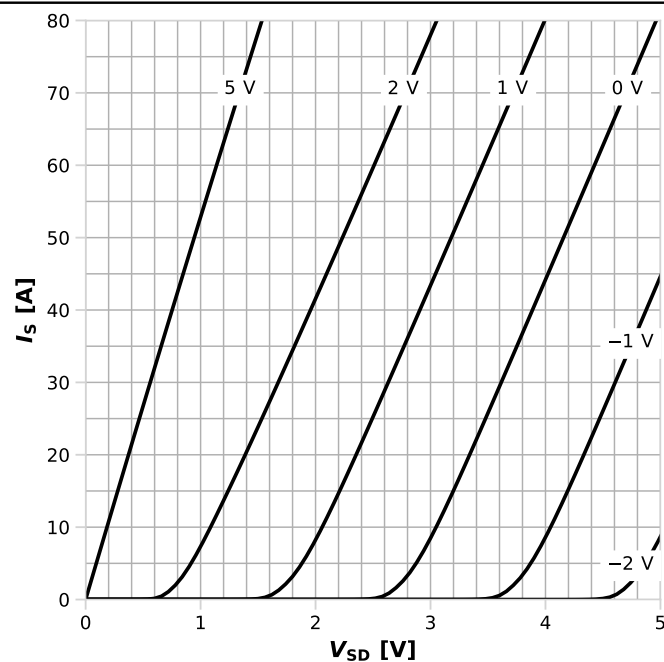
$I_D = f(V_{GS})$; $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 7: Typ. channel reverse characteristics



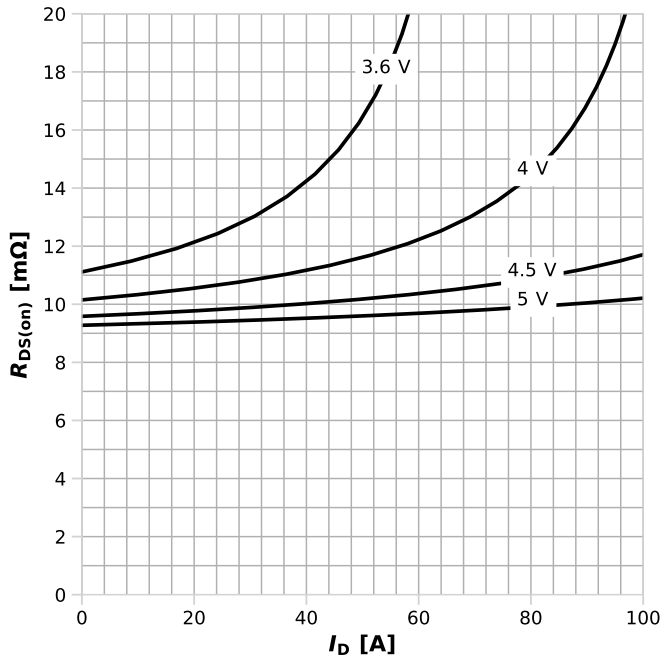
$I_S = f(V_{SD})$; $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 8: Typ. channel reverse characteristics



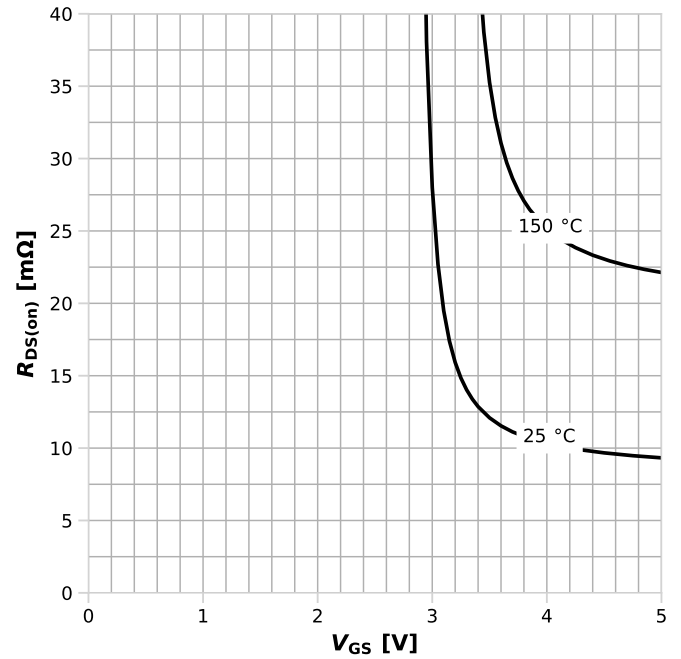
$I_S = f(V_{SD})$; $T_j = 125^\circ\text{C}$; parameter: V_{GS}

Diagram 9: Typ. drain-source on-state resistance



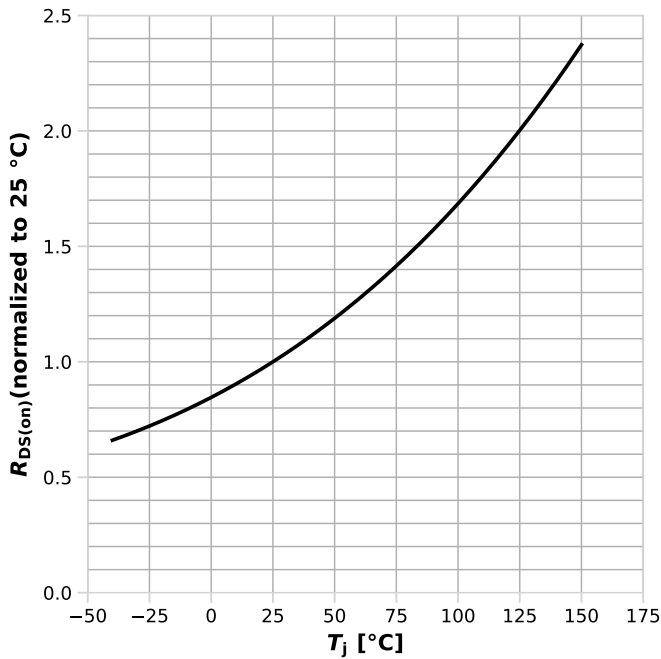
$$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$$

Diagram 10: Typ. Drain-source on-state resistance



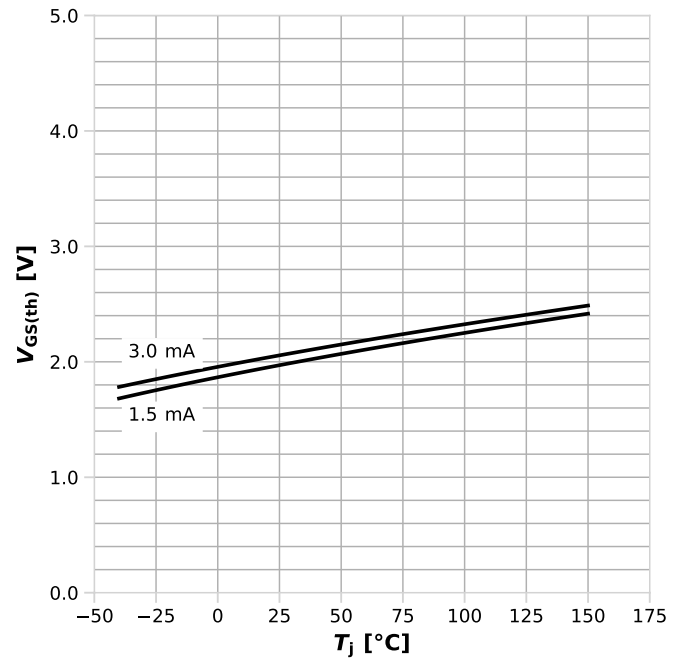
$$R_{DS(on)} = f(V_{GS}); I_D = 10 \text{ A}; \text{parameter: } T_j$$

Diagram 11: Drain-source on-state resistance



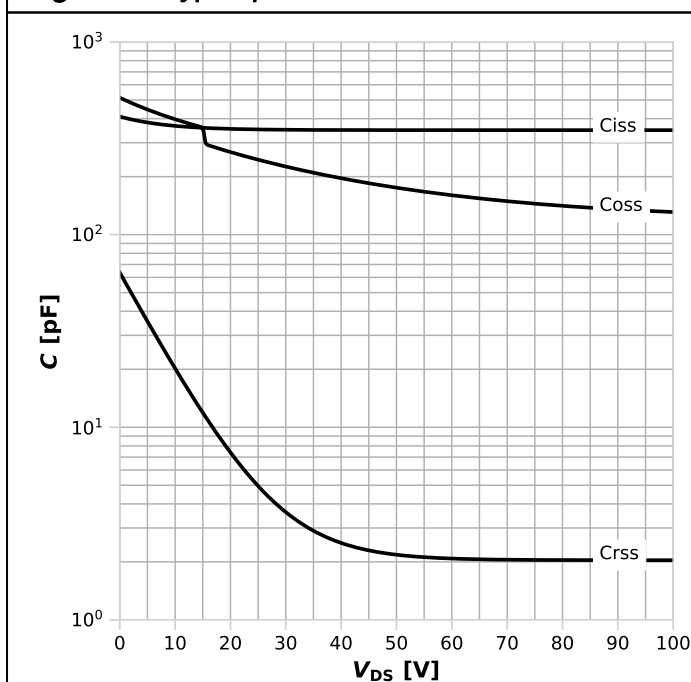
$$R_{DS(on)} = f(T_j); I_D = 10 \text{ A}, V_{GS} = 5 \text{ V}$$

Diagram 12: Typ. gate threshold voltage



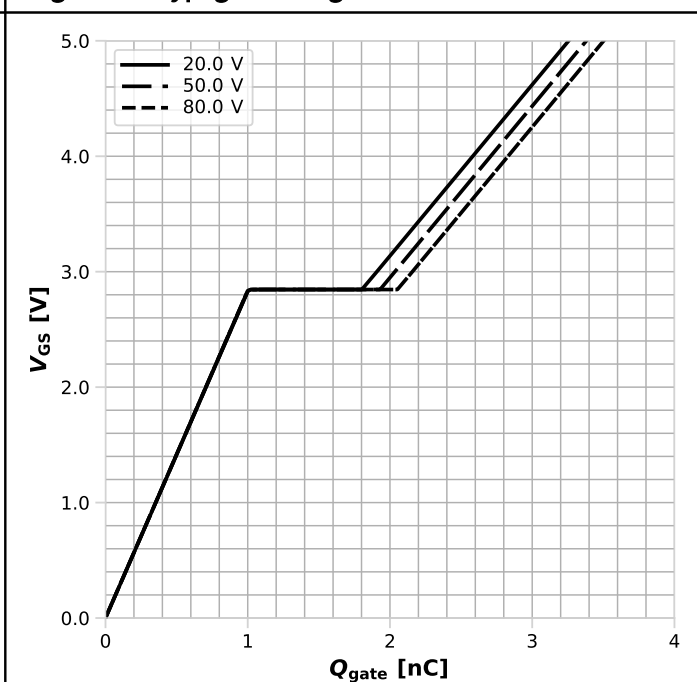
$$V_{GS(th)} = f(T_j), V_{GS} = V_{DS}; \text{parameter: } I_D$$

Diagram 13: Typ. capacitances



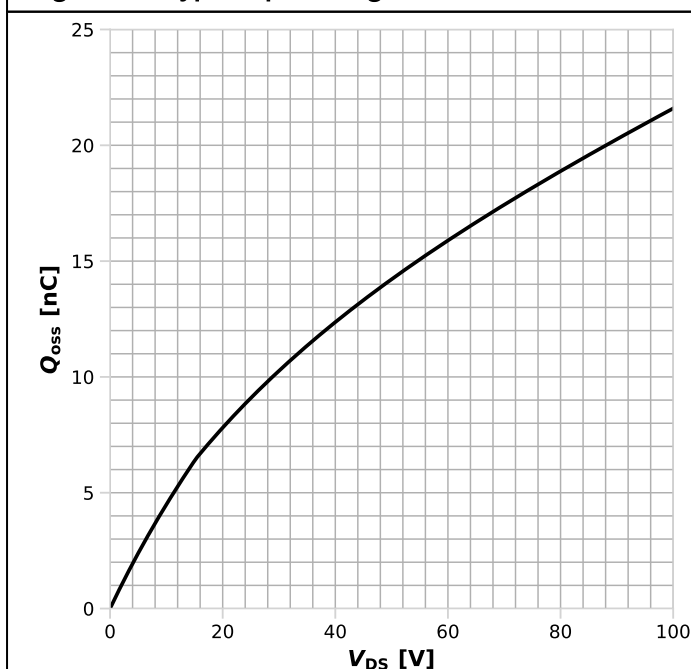
$$C=f(V_{DS}); V_{GS}=0\text{ V}$$

Diagram 14 Typ. gate charge



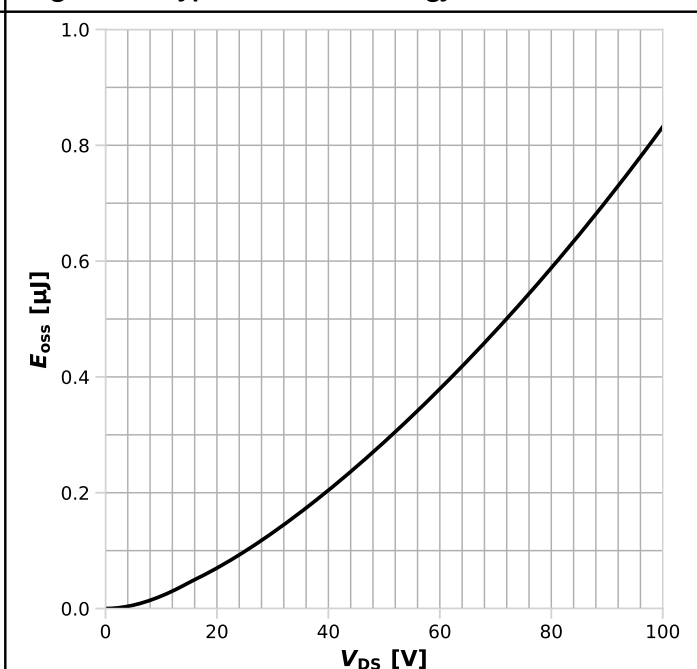
$$V_{GS}=f(Q_{gate}); I_D=10\text{ A pulsed; parameter: }V_{DS}$$

Diagram 15: Typ. output charge



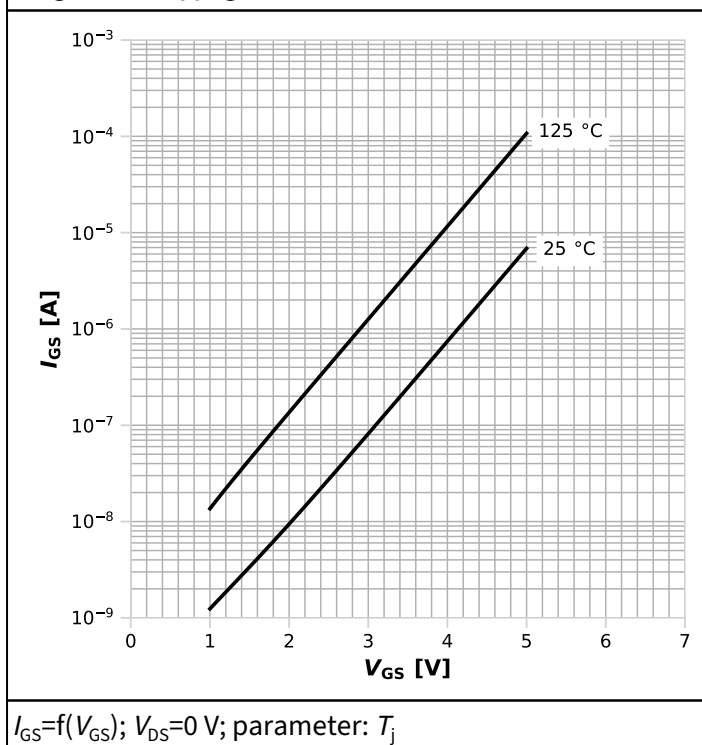
$$Q_{oss}=f(V_{DS}), V_{GS}=0\text{ V}$$

Diagram 16: Typ. Coss stored Energy

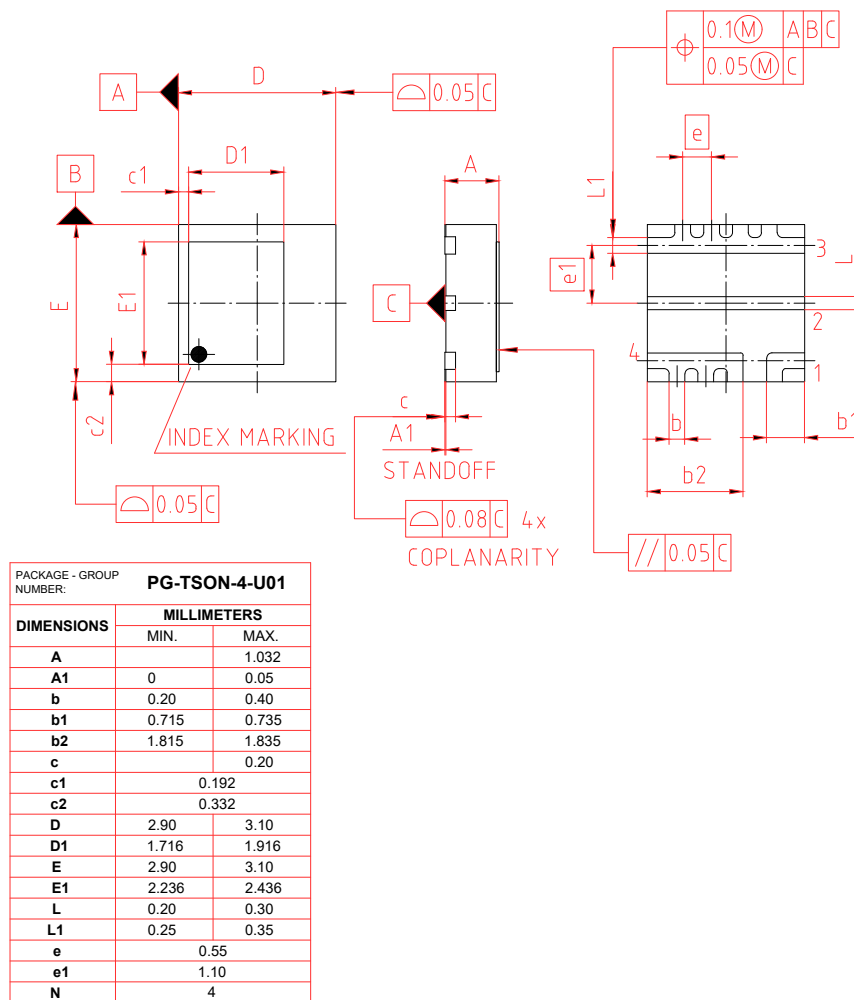


$$E_{oss}=f(V_{DS}), V_{GS}=0\text{ V}$$

Diagram 17: Typ. gate characteristics forward



6 Package outlines



NOTE:
 DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 1 Outline PG-TSON-4, dimensions in mm

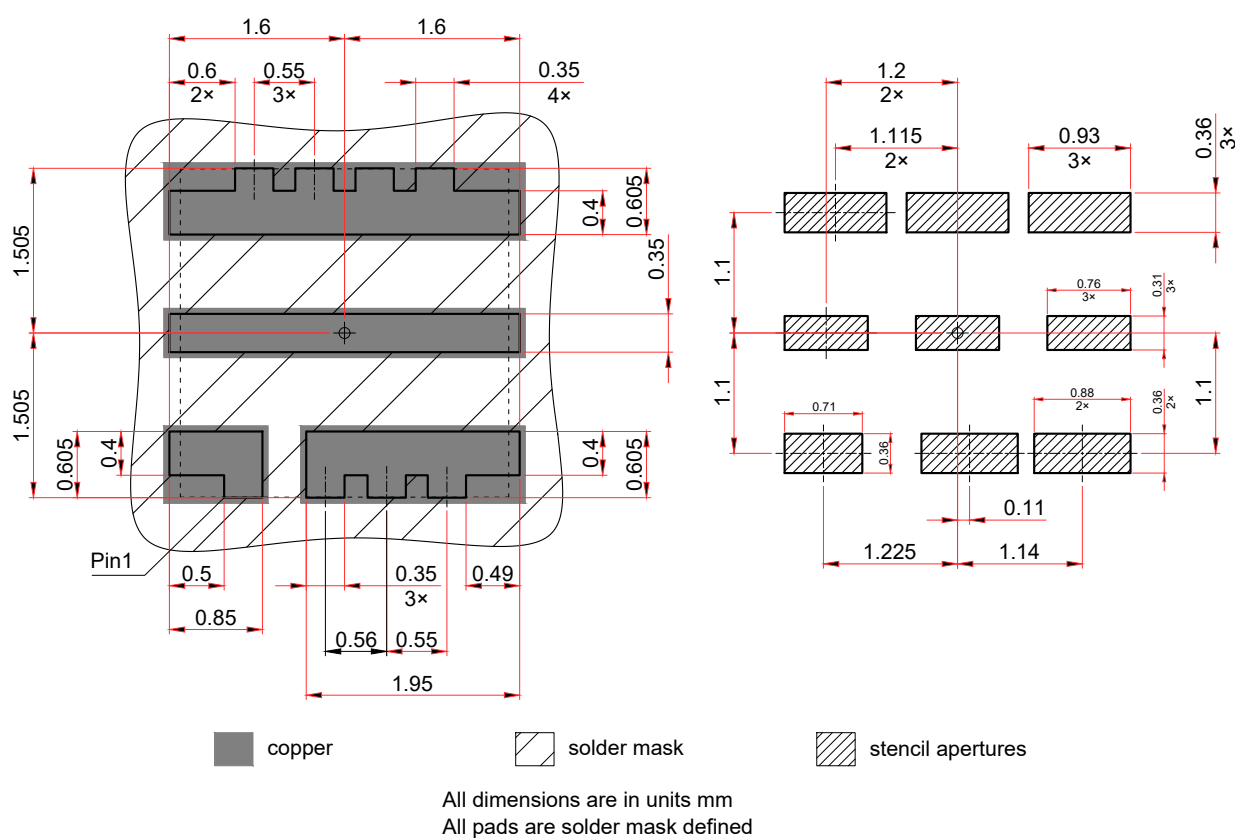
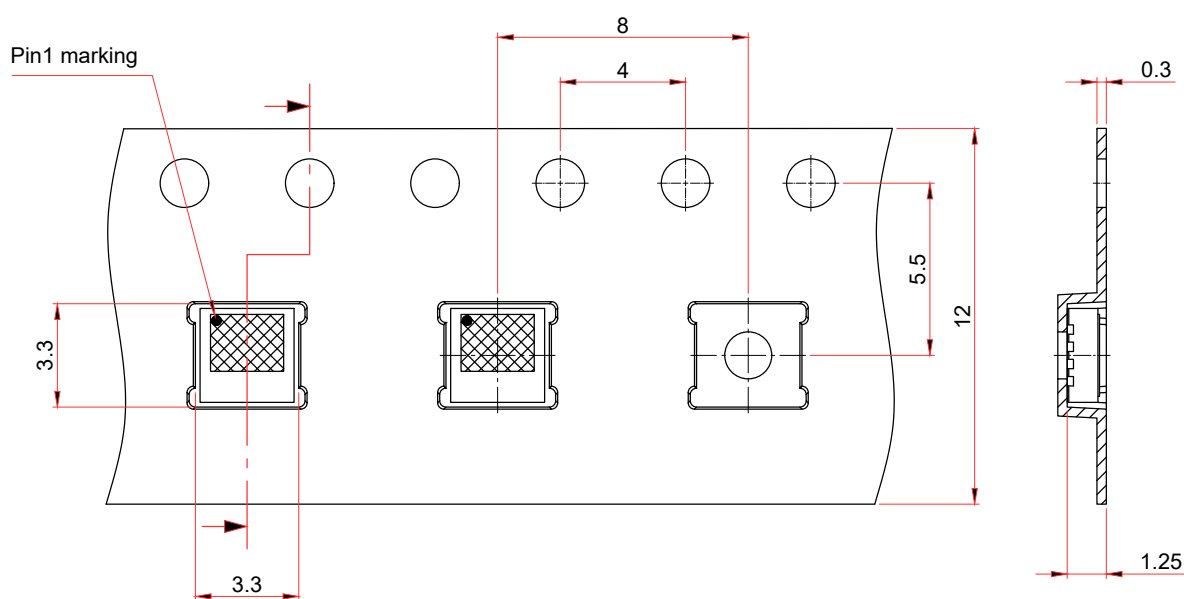


Figure 2 Footprint drawing PG-TSON-4, dimensions in mm



All dimensions are in units mm

The drawing is in compliance with ISO 128-30, Projection Method 1 []

Figure 3 Packaging variant PG-TSON-4, dimensions in mm

7 Appendix A

Table 9 **Related links**

- [IFX CoolGaN™ GaN webpage](#)
- [IFX CoolGaN™ reliability white paper](#)
- [IFX CoolGaN™ gate driver application note](#)
- [IFX Packages Description-PG-TSON-4-2](#)

Revision history

IGB110S10S1Q

Revision 2025-01-17, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2025-01-17	Release of final version

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